



**THE DATASHEET OF  
MAX6316MUK46CY+T**



## MAX6316–MAX6322

## 5-Pin $\mu$ P Supervisory Circuits with Watchdog and Manual Reset

### General Description

The MAX6316–MAX6322 family of microprocessor ( $\mu$ P) supervisory circuits monitors power supplies and microprocessor activity in digital systems. It offers several combinations of push/pull, open-drain, and bidirectional (such as Motorola 68HC11) reset outputs, along with watchdog and manual reset features. The *Selector Guide* below lists the specific functions available from each device.

These devices are available in 26 factory-trimmed reset threshold voltages (from 2.5V to 5V, in 100mV increments), featuring four minimum power-on reset timeout periods (from 1ms to 1.12s), and four watchdog timeout periods (from 6.3ms to 25.6s). Thirteen standard versions are available with an order increment requirement of 2500 pieces (see *Standard Versions* table); contact the factory for availability of other versions, which have an order increment requirement of 10,000 pieces.

The MAX6316–MAX6322 are offered in a miniature 5-pin SOT23 package.

### Applications

- Portable Computers
- Computers
- Controllers
- Intelligent Instruments
- Portable/Battery-Powered Equipment
- Embedded Control Systems

### Benefits and Features

- Integrated Configuration Enables Flexible Designs
  - Available in 26 Reset-Threshold Voltages
    - 2.5V to 5V, in 100mV Increments
  - Four Reset Timeout Periods
    - 1ms, 20ms, 140ms, or 1.12s (min)
  - Four Watchdog Timeout Periods
    - 6.3ms, 102ms, 1.6s, or 25.6s (typ)
  - Four Reset Output Stages
    - Active-High, Push/Pull
    - Active-Low, Push/Pull
    - Active-Low, Open-Drain
    - Active-Low, Bidirectional
- Integrated Features Increase Robustness
  - Guaranteed Reset Valid to  $V_{CC} = 1V$
  - Immune to Short-Negative  $V_{CC}$  Transients
- Saves Board Space
  - No External Components
  - Small 5-Pin SOT23 Package
  - AEC-Q100 Qualified

[Typical Operating Circuit and Pin Configurations](#) appears at end of data sheet.

[Ordering Information](#) appears at end of data sheet.

### Selector Guide

PART	WATCHDOG INPUT	MANUAL RESET INPUT	RESET OUTPUTS*			
			ACTIVE-LOW PUSH/PULL	ACTIVE-HIGH PUSH/PULL	ACTIVE-LOW BIDIRECTIONAL	ACTIVE-LOW OPEN-DRAIN
MAX6316L	✓	✓	✓	—	—	—
MAX6316M	✓	✓	—	—	✓	—
MAX6317H	✓	✓	—	✓	—	—
MAX6318LH	✓	—	✓	✓	—	—
MAX6318MH	✓	—	—	✓	✓	—
MAX6319LH	—	✓	✓	✓	—	—
MAX6319MH	—	✓	—	✓	✓	—
MAX6320P	✓	✓	—	—	—	✓
MAX6321HP	✓	—	—	✓	—	✓
MAX6322HP	—	✓	—	✓	—	✓

\*The MAX6318/MAX6319/MAX6321/MAX6322 feature two types of reset output on each device.

**Absolute Maximum Ratings**

Voltage (with respect to GND)	Operating Temperature Range.....	-40°C to +125°C
$V_{CC}$ .....	Junction Temperature.....	+150°C
$\overline{RESET}$ (MAX6320/MAX6321/MAX6322 only) ....	Storage Temperature Range.....	-65°C to +160°C
All Other Pins.....	Lead Temperature (soldering, 10s) .....	+300°C
Input/Output Current, All Pins.....	Soldering Temperature (reflow)	
Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )	Leaded Package.....	+240°C
SOT23 (derate 3.9mW/°C above +70°C).....	Lead-Free Package.....	+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**Package Information**

**SOT23-5**

PACKAGE CODE	U5+2/U5+2A
Outline Number	<a href="#">21-0057</a>
Land Pattern Number	<a href="#">90-0174</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	324.3°C/W
Junction to Case ( $\theta_{JC}$ )	82°C/W
<b>Thermal Resistance, Multi-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	255.9°C/W
Junction to Case ( $\theta_{JC}$ )	81°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

**Electrical Characteristics**

( $V_{CC} = 2.5V$  to  $5.5V$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	$V_{CC}$	$T_A = -40^\circ C$ to $+125^\circ C$	1.0		5.5	V
Supply Current	$I_{CC}$	MAX6316/MAX6317/MAX6318/MAX6320/MAX6321	$V_{CC} = 5.5V$	10	20	$\mu A$
			$V_{CC} = 3.6V$	5	12	
		MAX6319/MAX6322: MR unconnected	$V_{CC} = 5.5V$	3	12	
			$V_{CC} = 3.6V$	3	8	
Reset Threshold Temperature Coefficient	$\Delta V_{TH}/^\circ C$		40			ppm/ $^\circ C$
Reset Threshold (Note 2)	$V_{RST}$	$T_A = +25^\circ C$	$V_{TH} - 1.5\%$	$V_{TH}$	$V_{TH} + 1.5\%$	V
		$T_A = -40^\circ C$ to $+125^\circ C$	$V_{TH} - 2.5\%$	$V_{TH}$	$V_{TH} + 2.5\%$	
Reset Threshold Hysteresis				3		mV
Reset Active Timeout Period	$t_{RP}$	MAX63__A_-T	1	1.4	2	ms
		MAX63__B_-T	20	28	40	
		MAX63__C_-T	140	200	280	
		MAX63__D_-T	1120	1600	2240	
$V_{CC}$ to $\overline{RESET}$ Delay	$t_{RD}$	$V_{CC}$ falling at $1mV/\mu s$		40		$\mu s$
<b>PUSH/PULL RESET OUTPUT (MAX6316L/MAX6317H/MAX6318_H/MAX6319_H/MAX6321HP/MAX6322HP)</b>						
$\overline{RESET}$ Output Voltage	$V_{OL}$	$V_{CC} \geq 1.0V$ , $I_{SINK} = 50\mu A$			0.3	V
		$V_{CC} \geq 1.2V$ , $I_{SINK} = 100\mu A$			0.3	
		$V_{CC} \geq 2.7V$ , $I_{SINK} = 1.2mA$			0.3	
		$V_{CC} \geq 4.5V$ , $I_{SINK} = 3.2mA$			0.4	
	$V_{OH}$	$V_{CC} \geq 2.7V$ , $I_{SOURCE} = 500\mu A$	$0.8 \times V_{CC}$			
		$V_{CC} \geq 4.5V$ , $I_{SOURCE} = 800\mu A$	$V_{CC} - 1.5$			
RESET Rise Time (MAX6316L, MAX6318LH, MAX6319LH)	$t_R$	Rise time is measured from 10% to 90% of $V_{CC}$ ; $C_L = 5pF$ , $V_{CC} = 3.3V$ (Note 3)		5	25	ns
RESET Output Voltage	$V_{OL}$	$V_{CC} \geq 2.7V$ , $I_{SINK} = 1.2mA$			0.3	V
		$V_{CC} \geq 4.5V$ , $I_{SINK} = 3.2mA$			0.4	
	$V_{OH}$	$V_{CC} \geq 1.8V$ , $I_{SOURCE} = 150\mu A$	$0.8 \times V_{CC}$			
		$V_{CC} \geq 2.7V$ , $I_{SOURCE} = 500\mu A$	$0.8 \times V_{CC}$			
		$V_{CC} \geq 4.5V$ , $I_{SOURCE} = 800\mu A$	$0.8 \times V_{CC}$			
			$V_{CC} - 1.5$			

**Note 1:** Overtemperature limits are guaranteed by design, not production tested.

**Note 2:** A factory-trimmed voltage divider programs the nominal reset threshold ( $V_{TH}$ ). Factory-trimmed reset thresholds are available in 100mV increments from 2.5V to 5V (see Table 1 at end of data sheet).

**Note 3:** Guaranteed by design.

## Electrical Characteristics (continued)

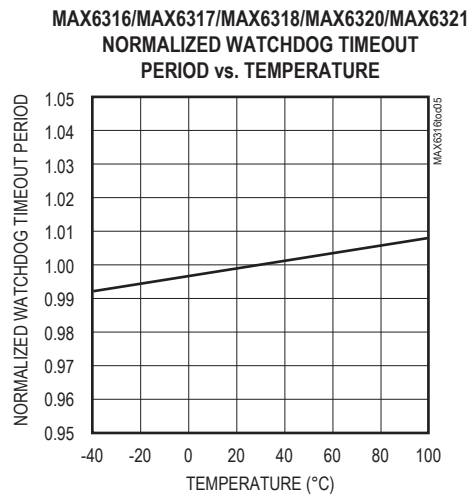
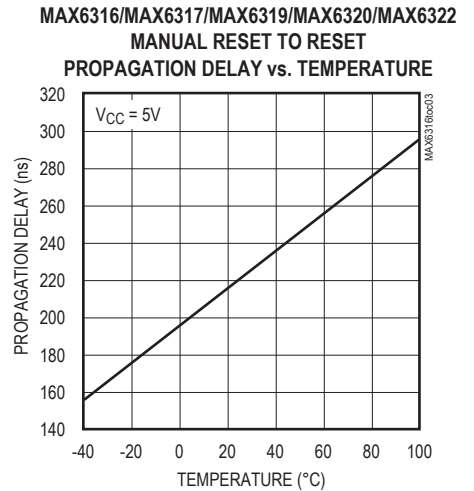
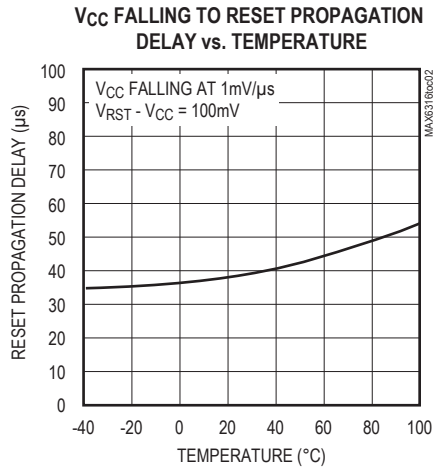
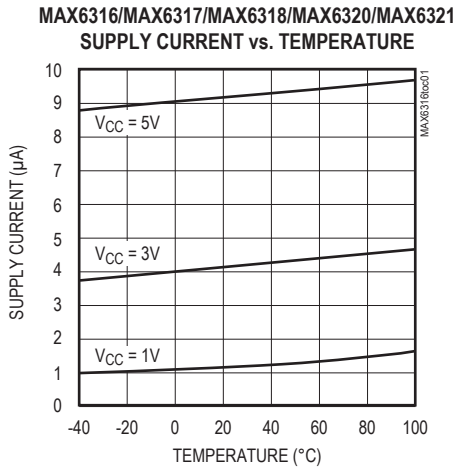
(V<sub>CC</sub> = 2.5V to 5.5V, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>BIDIRECTIONAL <math>\overline{\text{RESET}}</math> OUTPUT (MAX6316M/MAX6318MH/MAX6319MH)</b>						
Transitional Flip-Flop Setup Time	t <sub>S</sub>	(Note 4)		400		ns
$\overline{\text{RESET}}$ Output Rise Time (Note 5)	t <sub>R</sub>	V <sub>CC</sub> = 3.0V, C <sub>L</sub> = 120pF			333	ns
		V <sub>CC</sub> = 5.0V, C <sub>L</sub> = 200pF			333	
		V <sub>CC</sub> = 3.0V, C <sub>L</sub> = 250pF			666	
		V <sub>CC</sub> = 5.0V, C <sub>L</sub> = 400pF			666	
Active Pullup Enable Threshold	V <sub>PTH</sub>	V <sub>CC</sub> = 5.0V	0.4	0.65		V
$\overline{\text{RESET}}$ Active Pullup Current		V <sub>CC</sub> = 5.0V		20		mA
$\overline{\text{RESET}}$ Pullup Resistance		T <sub>A</sub> = -40°C to +85°C	4.2	4.7	5.2	k $\Omega$
		T <sub>A</sub> = -40°C to +125°C	3.6	4.7	5.8	
<b>OPEN-DRAIN <math>\overline{\text{RESET}}</math> OUTPUT (MAX6320P/MAX6321HP/MAX6322HP)</b>						
$\overline{\text{RESET}}$ Output Voltage	V <sub>OL</sub>	V <sub>CC</sub> $\geq$ 1.0V, I <sub>SINK</sub> = 50 $\mu$ A			0.3	V
		V <sub>CC</sub> $\geq$ 1.2V, I <sub>SINK</sub> = 100 $\mu$ A			0.3	
		V <sub>CC</sub> $\geq$ 2.7V, I <sub>SINK</sub> = 1.2mA			0.3	
		V <sub>CC</sub> $\geq$ 4.5V, I <sub>SINK</sub> = 3.2mA			0.4	
Open-Drain Reset Output Leakage Current	I <sub>LKG</sub>				1.0	$\mu$ A
<b>WATCHDOG INPUT (MAX6316/MAX6317H/MAX6318_H/MAX6320P/MAX6321HP)</b>						
Watchdog Timeout Period	t <sub>WD</sub>	MAX63__W-T	4.3	6.3	9.3	ms
		MAX63__X-T	71	102	153	
		MAX63__Y-T	1.12	1.6	2.4	s
		MAX63__Z-T	17.9	25.6	38.4	
WDI Pulse Width	t <sub>WDI</sub>	V <sub>IL</sub> = 0.3 x V <sub>CC</sub> , V <sub>IH</sub> = 0.7 x V <sub>CC</sub>	50			ns
WDI Input Threshold	V <sub>IL</sub>	(Note 6)	0.3 x V <sub>CC</sub>		0.7 x V <sub>CC</sub>	V
	V <sub>IH</sub>					
WDI Input Current (Note 7)	I <sub>WDI</sub>	WDI = V <sub>CC</sub> , time average		120	160	$\mu$ A
		V <sub>WDI</sub> = 0V, time average	-20	-15		
<b>MANUAL RESET INPUT (MAX6316_/MAX6317H/MAX6319_H/MAX6320P/MAX6322HP)</b>						
$\overline{\text{MR}}$ Input Threshold	V <sub>IL</sub>	V <sub>TH</sub> > 4.0V	0.8		2.0	V
	V <sub>IH</sub>					
	V <sub>IL</sub>	V <sub>TH</sub> < 4.0V	0.3 x V <sub>CC</sub>			
	V <sub>IH</sub>		0.7 x V <sub>CC</sub>			
$\overline{\text{MR}}$ Input Pulse Width		T <sub>A</sub> = -40°C to +85°C	1			$\mu$ s
		T <sub>A</sub> = -40°C to +125°C	1.5			
$\overline{\text{MR}}$ Glitch Rejection				100		ns
$\overline{\text{MR}}$ Pullup Resistance			35	52	75	k $\Omega$
$\overline{\text{MR}}$ to Reset Delay		V <sub>CC</sub> = 5V		230		ns

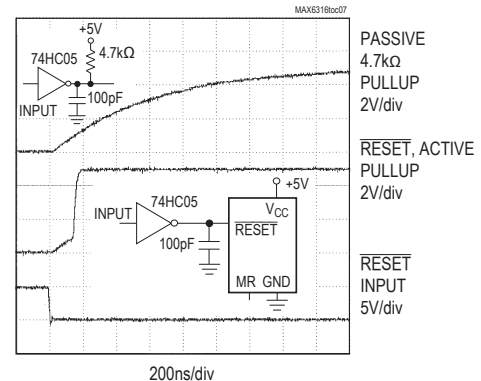
**Note 4:** This is the minimum time  $\overline{\text{RESET}}$  must be held low by an external pulldown source to set the active pullup flip-flop.**Note 5:** Measured from  $\overline{\text{RESET}}$  V<sub>OL</sub> to (0.8 x V<sub>CC</sub>), R<sub>LOAD</sub> =  $\infty$ .**Note 6:** WDI is internally serviced within the watchdog period if WDI is left unconnected.**Note 7:** The WDI input current is specified as the average input current when the WDI input is driven high or low. The WDI input is designed for a three-stated-output device with a 10 $\mu$ A maximum leakage current and capable of driving a maximum capacitive load of 200pF. The three-state device must be able to source and sink at least 200 $\mu$ A when active.

Typical Operating Characteristics

$T_A = +25^\circ\text{C}$ , unless otherwise noted.)



**MAX6316M/6318MH/6319MH**  
BIDIRECTIONAL  
PULLUP CHARACTERISTICS



Pin Description

PIN				NAME	FUNCTION
MAX6316L MAX6316M MAX6320P	MAX6317H	MAX6318LH MAX6318MH MAX6321HP	MAX6319LH MAX6319MH MAX6322HP		
1	—	1	1	RESET	<p>MAX6316L/MAX6318LH/MAX6319LH: Active-Low, Reset Output. CMOS push/pull output (sources and sinks current).</p> <p>MAX6316M/MAX6318MH/MAX6319MH: Bidirectional, Active-Low, Reset Output. Intended to interface directly to microprocessors with bidirectional resets such as the Motorola 68HC11.</p> <p>MAX6320P/MAX6321HP/MAX6322HP: Open-Drain, Active-Low, Reset Output. NMOS output (sinks current only). Connect a pullup resistor from RESET to any supply voltage up to 6V.</p>
—	1	3	3	RESET	Active-High, Reset Output. CMOS push/pull output (sources and sinks current). Inverse of RESET.
2	2	2	2	GND	Ground
3	3	—	4	$\overline{\text{MR}}$	Active-Low, Manual Reset Input. Pull low to force a reset. Reset remains asserted for the duration of the Reset Timeout Period after MR transitions from low to high. Leave unconnected or connected to $V_{CC}$ if not used.
4	4	4	—	WDI	Watchdog Input. Triggers a reset if it remains either high or low for the duration of the watchdog timeout period. The internal watchdog timer clears whenever a reset asserts or whenever WDI sees a rising or falling edge. To disable the watchdog feature, leave WDI unconnected or three-state the driver connected to WDI.
5	5	5	5	$V_{CC}$	Supply Voltage. Reset is asserted when $V_{CC}$ drops below the Reset Threshold Voltage ( $V_{RST}$ ). Reset remains asserted until $V_{CC}$ rises above $V_{RST}$ and for the duration of the Reset Timeout Period ( $t_{RP}$ ) once $V_{CC}$ rises above $V_{RST}$ .



Figure 1. Functional Diagram

### Detailed Description

A microprocessor’s ( $\mu$ P) reset input starts or restarts the  $\mu$ P in a known state. The reset output of the MAX6316–MAX6322  $\mu$ P supervisory circuits interfaces with the reset input of the  $\mu$ P, preventing code-execution errors during power-up, power-down, and brownout conditions (see the *Typical Operating Circuit*). The MAX6316/MAX6317/MAX6318/MAX6320/MAX6321 are also capable of asserting a reset should the  $\mu$ P become stuck in an infinite loop.

### Reset Output

The MAX6316L/MAX6318LH/MAX6319LH feature an active-low reset output, while the MAX6317H/MAX6318\_H/MAX6319\_H/MAX6321HP/MAX6322HP feature an active-high reset output.  $\overline{\text{RESET}}$  is guaranteed to be a logic low and RESET is guaranteed to be a logic high for  $V_{CC}$  down to 1V.

The MAX6316–MAX6322 assert reset when  $V_{CC}$  is below the reset threshold ( $V_{RST}$ ), when  $\overline{\text{MR}}$  is pulled low (MAX6316\_/MAX6317H/MAX6319\_H/MAX6320P/MAX6322HP only), or if the WDI pin is not serviced

within the watchdog timeout period ( $t_{WD}$ ). Reset remains asserted for the specified reset active timeout period ( $t_{RP}$ ) after  $V_{CC}$  rises above the reset threshold, after  $\overline{\text{MR}}$  transitions low to high, or after the watchdog timer asserts the reset (MAX6316\_/MAX6317H/MAX6318\_H/MAX6320P/MAX6321HP). After the reset active timeout period ( $t_{RP}$ ) expires, the reset output deasserts, and the watchdog timer restarts from zero (Figure 2).



Figure 2. Reset Timing Diagram

**Bidirectional RESET Output**

The MAX6316M/MAX6318MH/MAX6319MH are designed to interface with  $\mu$ Ps that have bidirectional reset pins, such as the Motorola 68HC11. Like an open-drain output, these devices allow the  $\mu$ P or other devices to pull the bidirectional reset ( $\overline{\text{RESET}}$ ) low and assert a reset condition. However, unlike a standard open-drain output, it includes the commonly specified 4.7k $\Omega$  pullup resistor with a P-channel active pullup in parallel.

This configuration allows the MAX6316M/MAX6318MH/MAX6319MH to solve a problem associated with  $\mu$ Ps that have bidirectional reset pins in systems where several devices connect to  $\overline{\text{RESET}}$  (Figure 3). These  $\mu$ Ps can often determine if a reset was asserted by an external device (i.e., the supervisor IC) or by the  $\mu$ P itself (due to a watchdog fault, clock error, or other source), and then jump to a vector appropriate for the source of the reset. However, if the  $\mu$ P does assert reset, it does not retain the information, but must determine the cause after the reset has occurred.

The following procedure describes how this is done in the Motorola 68HC11. In all cases of reset, the  $\mu$ P pulls  $\overline{\text{RESET}}$  low for about four external-clock cycles. It then releases  $\overline{\text{RESET}}$ , waits for two external-clock cycles, then checks  $\overline{\text{RESET}}$ 's state. If  $\overline{\text{RESET}}$  is still low, the  $\mu$ P concludes that the source of the reset was external and, when  $\overline{\text{RESET}}$  eventually reaches the high state, it jumps to the normal reset vector. In this case, stored-state information

is erased and processing begins from scratch. If, on the other hand,  $\overline{\text{RESET}}$  is high after a delay of two external-clock cycles, the processor knows that it caused the reset itself and can jump to a different vector and use stored-state information to determine what caused the reset.

A problem occurs with faster  $\mu$ Ps; two external-clock cycles are only 500ns at 4MHz. When there are several devices on the reset line, and only a passive pullup resistor is used, the input capacitance and stray capacitance can prevent  $\overline{\text{RESET}}$  from reaching the logic high state ( $0.85 \times V_{CC}$ ) in the time allowed. If this happens, all resets will be interpreted as external. The  $\mu$ P output stage is guaranteed to sink 1.6mA, so the rise time can not be reduced considerably by decreasing the 4.7k $\Omega$  internal pullup resistance. See Bidirectional Pullup Characteristics in the *Typical Operating Characteristics*.

The MAX6316M/MAX6318MH/MAX6319MH overcome this problem with an active pullup FET in parallel with the 4.7k $\Omega$  resistor (Figures 4 and 5). The pullup transistor holds  $\overline{\text{RESET}}$  high until the  $\mu$ P reset I/O or the supervisory circuit itself forces the line low. Once  $\overline{\text{RESET}}$  goes below  $V_{PTH}$ , a comparator sets the transition edge flip-flop, indicating that the next transition for  $\overline{\text{RESET}}$  will be low to high. When  $\overline{\text{RESET}}$  is released, the 4.7k $\Omega$  resistor pulls  $\overline{\text{RESET}}$  up toward  $V_{CC}$ . Once  $\overline{\text{RESET}}$  rises above  $V_{PTH}$  but is below ( $0.85 \times V_{CC}$ ), the active P-channel pullup turns on. Once  $\overline{\text{RESET}}$  rises above ( $0.85 \times V_{CC}$ ) or the 2 $\mu$ s one-shot times out, the active pullup turns off. The parallel combination of the 4.7k $\Omega$  pullup and the

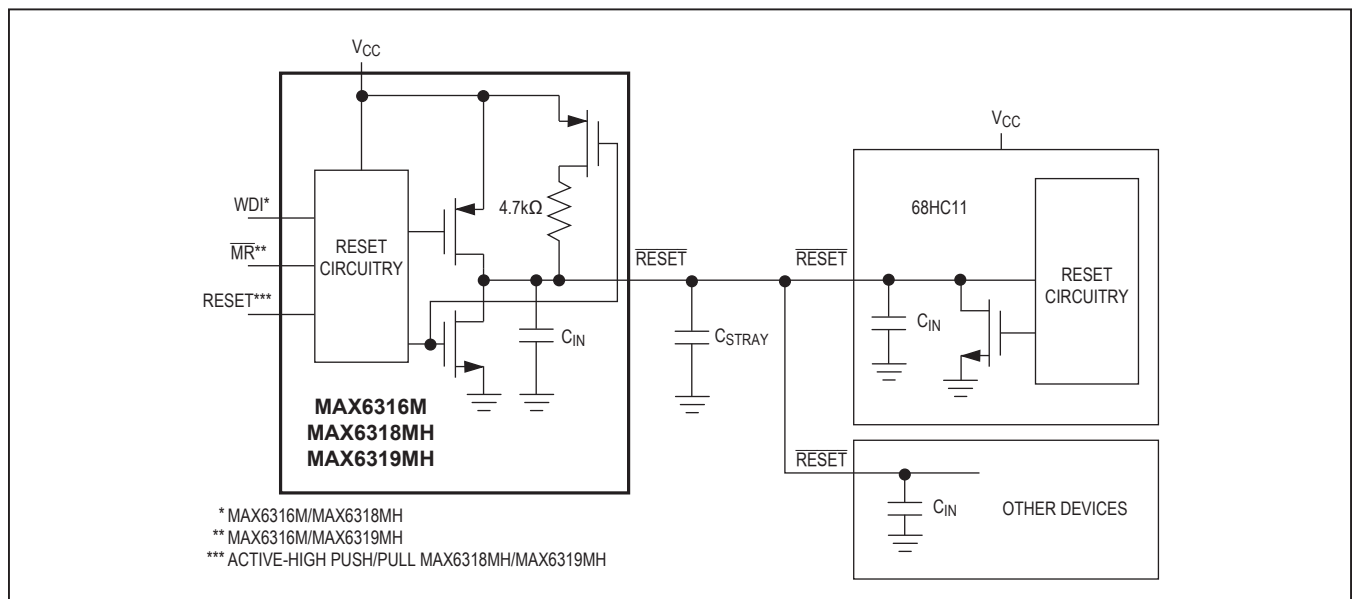


Figure 3. MAX6316M/MAX6318MH/MAX6319MH Supports Additional Devices on the Reset Bus



Figure 4. MAX6316/MAX6318MH/MAX6319MH Bidirectional Reset Output Functional Diagram

P-channel transistor on-resistance quickly charges stray capacitance on the reset line, allowing  $\overline{\text{RESET}}$  to transition from low to high within the required two electronic-clock cycles, even with several devices on the reset line. This process occurs regardless of whether the reset was caused by  $V_{CC}$  dipping below the reset threshold, the watchdog timing out,  $\overline{\text{MR}}$  being asserted, or the  $\mu$ P or other device asserting  $\overline{\text{RESET}}$ . The parts do not require an external pullup. To minimize supply current consumption, the internal  $4.7\text{k}\Omega$  pullup resistor disconnects from the supply whenever the MAX6316M/MAX6318MH/MAX6319MH assert reset.

**Open-Drain  $\overline{\text{RESET}}$  Output**

The MAX6320P/MAX6321HP/MAX6322HP have an active-low, open-drain reset output. This output structure will sink current when  $\overline{\text{RESET}}$  is asserted. Connect a pullup resistor from  $\overline{\text{RESET}}$  to any supply voltage up to 6V (Figure 6). Select a resistor value large enough to regis-



Figure 5. Bidirectional  $\overline{\text{RESET}}$  Timing Diagram



Figure 6. MAX6320P/MAX6321HP/MAX6322HP Open-Drain  $\overline{\text{RESET}}$  Output Allows Use with Multiple Supplies

ter a logic low (see *Electrical Characteristics*), and small enough to register a logic high while supplying all input current and leakage paths connected to the  $\overline{\text{RESET}}$  line. A  $10\text{k}\Omega$  pullup is sufficient in most applications.

**Manual-Reset Input**

The MAX6316\_/MAX6317H/MAX6319\_H/MAX6320P/MAX6322HP feature a manual reset input. A logic low on  $\overline{\text{MR}}$  asserts a reset. After  $\overline{\text{MR}}$  transitions low to high, reset remains asserted for the duration of the reset timeout period ( $t_{RP}$ ). The  $\overline{\text{MR}}$  input is connected to  $V_{CC}$  through an internal  $52\text{k}\Omega$  pullup resistor and therefore can be left unconnected when not in use.  $\overline{\text{MR}}$  can be driven with TTL-logic levels in 5V systems, with CMOS-logic levels in 3V systems, or with open-drain or open-collector output devices. A normally-open momentary switch from  $\overline{\text{MR}}$  to ground can also be used; it requires no external debouncing circuitry.  $\overline{\text{MR}}$  is designed to reject fast, negative-going transients (typically  $100\text{ns}$  pulses). A  $0.1\mu\text{F}$  capacitor from  $\overline{\text{MR}}$  to ground provides additional noise immunity.

The  $\overline{\text{MR}}$  input pin is equipped with internal ESD-protection circuitry that may become forward biased. Should  $\overline{\text{MR}}$  be driven by voltages higher than  $V_{CC}$ , excessive current would be drawn, which would damage the part. For example, assume that  $\overline{\text{MR}}$  is driven by a +5V supply other than  $V_{CC}$ . If  $V_{CC}$  drops lower than +4.7V,  $\overline{\text{MR}}$ 's absolute maximum rating is violated [ $-0.3\text{V}$  to ( $V_{CC} + 0.3\text{V}$ )], and undesirable current flows through the ESD structure from  $\overline{\text{MR}}$  to  $V_{CC}$ . To avoid this, use the same supply for  $\overline{\text{MR}}$  as the supply monitored by  $V_{CC}$ . This guarantees that the voltage at  $\overline{\text{MR}}$  will never exceed  $V_{CC}$ .

**Watchdog Input**

The MAX6316\_/MAX6317H/MAX6318\_H/MAX6320P/MAX6321HP feature a watchdog circuit that monitors the  $\mu$ P's activity. If the  $\mu$ P does not toggle the watchdog input (WDI) within the watchdog timeout period ( $t_{WDT}$ ), reset asserts. The internal watchdog timer is cleared by reset or by a transition at WDI (which can detect pulses as short as  $50\text{ns}$ ). The watchdog timer remains cleared while reset is asserted. Once reset is released, the timer begins counting again (Figure 7).

The WDI input is designed for a three-stated output device with a  $10\mu\text{A}$  maximum leakage current and the capability of driving a maximum capacitive load of  $200\text{pF}$ . The three-state device must be able to source and sink at least  $200\mu\text{A}$  when active. Disable the watchdog function by leaving WDI unconnected or by three-stating the driver connected to WDI. When the watchdog timer is left open circuited, the timer is cleared internally at intervals equal to  $7/8$  of the watchdog period.



Figure 7. Watchdog Timing Relationship



Figure 8. Ensuring  $\overline{\text{RESET}}$  Valid to  $V_{CC} = 0V$  on Active-Low Push/Pull and Bidirectional Outputs

## Applications Information

### Watchdog Input Current

The WDI input is internally driven through a buffer and series resistor from the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog timeout period. When high, WDI can draw as much as 160 $\mu$ A. Pulsing WDI high at a low duty cycle will reduce the effect of the large input current. When WDI is left unconnected, the watchdog timer is serviced within the watchdog timeout period by a low-high-low pulse from the counter chain.

### Negative-Going VCC Transients

These supervisors are immune to short-duration, negative-going  $V_{CC}$  transients (glitches), which usually do not require the entire system to shut down. Typically, 200ns large-amplitude pulses (from ground to  $V_{CC}$ ) on the supply will not cause a reset. Lower amplitude pulses result in greater immunity. Typically, a  $V_{CC}$  transient that goes 100mV under the reset threshold and lasts less than 4 $\mu$ s will not trigger a reset. An optional 0.1 $\mu$ F bypass capacitor mounted close to  $V_{CC}$  provides additional transient immunity.

### Ensuring Valid Reset Outputs Down to $V_{CC} = 0V$

The MAX6316\_/MAX6317H/MAX6318\_H/MAX6319\_H/MAX6321HP/MAX6322HP are guaranteed to operate properly down to  $V_{CC} = 1V$ . In applications that require valid reset levels down to  $V_{CC} = 0V$ , a pull-down resistor to active-low outputs (push/pull and bidirectional only, Figure 8) and a pullup resistor to active-high outputs (push/pull only, Figure 9) will ensure that the reset line is valid while the reset output can no longer sink or source current. This



Figure 9. Ensuring  $\overline{\text{RESET}}$  Valid to  $V_{CC} = 0V$  on Active-High Push/Pull Outputs

scheme does not work with the open-drain outputs of the MAX6320/MAX6321/MAX6322. The resistor value used is not critical, but it must be large enough not to load the reset output when  $V_{CC}$  is above the reset threshold. For most applications, 100k $\Omega$  is adequate.

### Watchdog Software Considerations (MAX6316/MAX6317/MAX6318/MAX6320/MAX6321)

One way to help the watchdog timer monitor software execution more closely is to set and reset the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop, in which the watchdog timer would continue to be reset inside the loop, keeping the watchdog from timing out.

Figure 10 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the end of every subroutine or loop, then set high again when the program returns to the beginning. If the program should hang in any subroutine, the problem would be quickly corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued. As described in the *Watchdog Input Current* section, this scheme results in higher time average WDI current than does leaving WDI low for the majority of the timeout period and periodically pulsing it low-high-low.



Figure 10. Watchdog Flow Diagram

Pin Configurations



Typical Operating Circuit



**Table 1. Factory-Trimmed Reset Thresholds**

PART	$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	
	MIN	TYP	MAX	MIN	MAX
MAX63__50__-T	4.925	5.000	5.075	4.875	5.125
MAX63__49__-T	7.827	4.900	4.974	4.778	5.023
MAX63__48__-T	4.728	4.800	4.872	4.680	4.920
MAX63__47__-T	4.630	4.700	4.771	4.583	4.818
MAX63__46__-T	4.561	4.630	4.699	4.514	4.746
MAX63__45__-T	4.433	4.500	4.568	4.388	4.613
MAX63__44__-T	4.314	4.390	4.446	4.270	4.490
MAX63__43__-T	4.236	4.300	4.365	4.193	4.408
MAX63__42__-T	4.137	4.200	4.263	4.095	4.305
MAX63__41__-T	4.039	4.100	4.162	3.998	4.203
MAX63__40__-T	3.940	4.000	4.060	3.900	4.100
MAX63__39__-T	3.842	3.900	3.959	3.803	3.998
MAX63__38__-T	3.743	3.800	3.857	3.705	3.895
MAX63__37__-T	3.645	3.700	3.756	3.608	3.793
MAX63__36__-T	3.546	3.600	3.654	3.510	3.690
MAX63__35__-T	3.448	3.500	3.553	3.413	3.588
MAX63__34__-T	3.349	3.400	3.451	3.315	3.485
MAX63__33__-T	3.251	3.300	3.350	3.218	3.383
MAX63__32__-T	3.152	3.200	3.248	3.120	3.280
MAX63__31__-T	3.034	3.080	3.126	3.003	3.157
MAX63__30__-T	2.955	3.000	3.045	2.925	3.075
MAX63__29__-T	2.886	2.930	2.974	2.857	3.000
MAX63__28__-T	2.758	2.800	2.842	2.730	2.870
MAX63__27__-T	2.660	2.700	2.741	2.633	2.768
MAX63__26__-T	2.591	2.630	2.669	2.564	2.696
MAX63__25__-T	2.463	2.500	2.538	2.438	2.563

**Table 2. Standard Versions**

PART	RESET THRESHOLD (V)	MINIMUM RESET TIMEOUT (ms)	TYPICAL WATCHDOG TIMEOUTS (s)	SOT TOP MARK
MAX6316LUK29CY-T	2.93	140	1.6	ACDE
MAX6316LUK46CY-T	4.63	140	1.6	ACDD
MAX6316MUK29CY-T	2.93	140	1.6	ACDG
MAX6316MUK46CY-T	4.63	140	1.6	ACDF
MAX6317HUK46CY-T	4.63	140	1.6	ACDQ
MAX6318LHUK46CY-T	4.63	140	1.6	ACDH
MAX6318MHUK46CY-T	4.63	140	1.6	ACDJ
MAX6319LHUK46C-T	4.63	140	—	ACDK
MAX6319MHUK46C-T	4.63	140	—	ACDM

**Table 2. Standard Versions (continued)**

PART	RESET THRESHOLD (V)	MINIMUM RESET TIMEOUT (ms)	TYPICAL WATCHDOG TIMEOUTS (s)	SOT TOP MARK
MAX6320PUK29CY-T	2.93	140	1.6	ACDO
MAX6320PUK46CY-T	4.63	140	1.6	ACDN
MAX6321HPUK46CY-T	4.63	140	1.6	ACGL
MAX6322HPUK46C-T	4.63	140	1.6	ACGN

**Note:** Thirteen standard versions are available, with a required order increment of 2500 pieces. Sample stock is generally held on standard versions only. The required order increment for nonstandard versions is 10,000 pieces. Contact factory for availability.

**Table 3. Reset/Watchdog Timeout Periods**

RESET TIMEOUT PERIODS				
SUFFIX	MIN	TYP	MAX	UNITS
A	1	1.6	2	ms
B	20	30	40	
C	140	200	280	
D	1.12	1.60	2.24	s
WATCHDOG TIMEOUT				
W	4.3	6.3	9.3	ms
X	71	102	153	
Y	1.12	1.6	2.4	s
Z	17.9	25.6	38.4	

## Chip Information

SUBSTRATE IS INTERNALLY CONNECTED TO V+

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6316LUK____-T	-40°C to +125°C	5 SOT23
MAX6316LUK____/V+T	-40°C to +125°C	5 SOT23
MAX6316MUK____-T	-40°C to +125°C	5 SOT23
MAX6317HUK____-T	-40°C to +125°C	5 SOT23
MAX6318HUK____-T	-40°C to +125°C	5 SOT23
MAX6318MHUK____-T	-40°C to +125°C	5 SOT23
MAX6319LHUK____-T	-40°C to +125°C	5 SOT23
MAX6319MHUK____-T	-40°C to +125°C	5 SOT23
MAX6320PUK____-T	-40°C to +125°C	5 SOT23
MAX6320PUK____/V+T	-40°C to +125°C	5 SOT23
MAX6321HPUK____-T	-40°C to +125°C	5 SOT23
MAX6322HPUK____-T	-40°C to +125°C	5 SOT23

Devices are available in both leaded and lead(Pb)-free packaging. Specify lead-free by replacing “-T” with “+T” when ordering. /V Denotes an automotive-qualified part.

**Note:** These devices are available with factory-set  $V_{CC}$  reset thresholds from 2.5V to 5V, in 0.1V increments. Insert the desired nominal reset threshold (25 to 50, from Table 1) into the blanks following the letters UK. All devices offer factory-programmed reset timeout periods. Insert the letter corresponding to the desired reset timeout period (A, B, C, or D from Table 3) into the blank following the reset threshold suffix. Parts that offer a watchdog feature (see Selector Guide) are factory-trimmed to one of four watchdog timeout periods. Insert the letter corresponding to the desired watchdog timeout period (W, X, Y, or Z from Table 3) into the blank following the reset timeout suffix.

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/98	Initial release.	—
1	4/98	Update to show MAX6319 as an existing part.	1, 2, 12
2	7/98	Update specifications, <i>Selector Guide</i> , and Table 2.	1, 12, 14
3	1/99	Include extended temperature range in <i>EC</i> table globals, Table 1, <i>Ordering Information</i> .	1, 2, 3, 12, 13, 14
4	11/99	Update available products and versions in Table 2 and <i>Ordering Information</i> .	1, 12, 14
5	9/02	Addition of $\overline{\text{RESET}}$ rise time specification to <i>Electrical Characteristics</i> table.	1, 2
6	12/05	Add lead-free option to <i>Ordering Information</i> .	1, 13, 14
7	11/07	Add automotive temperature to <i>Ordering Information</i> , <i>Electrical Characteristics</i> table, Table 1, and updated <i>Package Information</i> .	1, 2, 3, 12, 13, 14
8	8/09	Updated <i>Ordering Information</i> .	13
9	6/10	Added automotive part and soldering temperatures.	2, 13
10	10/11	Added automotive-qualified part ordering option for MAX6316 family	1
11	2/13	Changed <i>V-T</i> suffix to <i>V+T</i> in <i>Ordering Information</i>	1
12	4/15	Updated the <i>General Description</i> and <i>Benefits and Features</i> sections	1
13	5/17	Added AEC-Q100 qualification	1
13.1		Corrected typo	1
14	11/18	Updated <i>Package Information</i>	2

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