THE DATASHEET OF

MAX5952AUAX+

19-0858; Rev 1; 1/10

EVALUATION KIT AVAILABLE

High-Power, Quad, PSE Controller for Power-Over-Ethernet

MAX5952

General Description

The MAX5952 is a quad -48V power controller designed for use in IEEE® 802.3af-compliant/pre-IEEE 802.3at-compatible power-sourcing equipment (PSE). This device provides powered device (PD) discovery, classification, current limit, DC and AC load disconnect detections in compliance with the IEEE 802.3af standard. The MAX5952 is pin compatible with MAX5945/LTC4258/LTC4259A PSE controllers and provides additional features.

The MAX5952 features high-power mode that provides up to 45W per port. The MAX5952 provides instantaneous readout of each port current through the I²C interface. The MAX5952 also provides high-capacitance detection for legacy PDs.

The device features an I²C-compatible, 3-wire serial interface, and is fully software configurable and programmable. The class-overcurrent detection function enables system power management to detect if a PD draws more than the allowable current. The MAX5952's extensive programmability enhances system flexibility, enables field diagnosis, and allows for uses in other applications.

The MAX5952 provides four operating modes to suit different system requirements. Auto mode allows the device to operate automatically without any software supervision. Semi-automatic mode automatically detects and classifies a device connected to a port after initial software activation, but does not power up that port until instructed to by software. Manual mode allows total software control of the device and is useful for system diagnostics. Shutdown mode terminates all activities and securely turns off power to the ports.

The MAX5952 provides input undervoltage lockout (UVLO), input undervoltage detection, input overvoltage lockout, overtemperature detection, output voltage slew-rate limit during startup, power-good status, and fault status. The MAX5952's programmability includes startup timeout, overcurrent timeout, and load-disconnect detection timeout.

The MAX5952 is available in a 36-pin SSOP package and is rated for both extended (-40°C to +85°C) and upper commercial (0°C to +85°C) temperature ranges.

Applications

Power-Sourcing Equipment (PSE)

Switches/Routers

Midspan Power Injectors

IEEE is a registered service mark of the Institute of Electrical and Electronics Engineers, Inc.

Features

- **IEEE 802.3af Compliant/Pre-IEEE 802.3at Compatible**
- **Instantaneous Readout of Port Current Through I²C Interface**
- **High-Power Mode Enables Up to 45W Per Port**
- **High-Capacitance Detection for Legacy Devices**
- **Pin Compatible to MAX5945 and LTC4258/LTC4259A**
- **Four Independent Power-Switch Controllers**
- **PD Detection and Classification**
- **Supports Both DC and AC Load Removal Detections**
- **I²C-Compatible, 3-Wire Serial Interface**
- **Current Foldback and Duty-Cycle-Controlled Current Limit**
- **Open-Drain $\overline{INT}$ Signal**
- **Direct Fast Shutdown Control Capability**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5952AEAX+*	-40°C to +85°C	36 SSOP
MAX5952AUAX+	0°C to +85°C	36 SSOP
MAX5952CEAX+*	-40°C to +85°C	36 SSOP
MAX5952CUAX+*	0°C to +85°C	36 SSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

**Future product—contact factory for availability.*

Pin Configuration and Selector Guide appear at end of data sheet.

High-Power, Quad, PSE Controller for Power-Over-Ethernet

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to V_{EE}, unless otherwise noted.)
AGND, DGND, DET_, V_{DD}, $\overline{RESET}$, A3–A0, $\overline{SHD\_}$, OSC, SCL, SDAIN, and AUTO .....-0.3V to +80V
OUT_.....-12V to (AGND + 0.3V)
GATE_ (internally clamped) (Note 1) .....-0.3V to +11.4V
SENSE_ .....-0.3V to +24V
V_{DD}, $\overline{RESET}$, MIDSPAN, A3–A0, $\overline{SHD\_}$, OSC, SCL, SDAIN and AUTO to DGND .....-0.3V to +7V
$\overline{INT}$ and SDAOUT to DGND.....-0.3V to +12V
AGND to DGND.....-0.3V to +7V
Maximum Current into $\overline{INT}$, SDAOUT, DET_.....80mA
Maximum Power Dissipation (T_A = +70°C)
36-Pin SSOP (derate 11.4mW/°C above +70°C) 941mW
Operating Temperature Ranges:
MAX5952_EAX.....-40°C to +85°C
MAX5952_UAX .....0°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: GATE_ is internally clamped to 11.4V above V_{EE}. Driving GATE_ higher than 11.4V above V_{EE} may damage the device.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AGND} = 32V to 60V, V_{EE} = 0V, V_{DD} to V_{DGND} = +3.3V, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Operating Voltage Range	V_{AGND}	V_{AGND} - V_{EE}	32		60	V
	V_{DGND}		0		60	
	V_{DD}	V_{DD} to V_{DGND}, V_{DGND} = V_{AGND}	1.71		5.50	
		V_{DD} to V_{DGND}, V_{DGND} = V_{EE}	3.0		5.5	
Supply Currents	I_{EE}	$V_{OUT\_}$ = V_{EE}, $V_{SENSE\_}$ = V_{EE}, DET_ = AGND, all logic inputs open, SCL = SDAIN = V_{DD}. $\overline{INT}$ and SDAOUT open. Measured at AGND in power mode after GATE_ pullup		4.8	6.8	mA
	I_{DIG}	All logic inputs high, measured at V_{DD}		3.0	5.6	
GATE DRIVER AND CLAMPING						
GATE_ Pullup Current	I_{PU}	Power mode, gate drive on, V_{GATE} = V_{EE}	-40	-50	-60	µA
Weak GATE_ Pulldown Current	I_{PDW}	$\overline{SHD\_}$ = DGND, $V_{GATE\_}$ = V_{EE} + 10V	30	42	55	µA
Maximum Pulldown Current	I_{PDS}	V_{SENSE} = 600mV, $V_{GATE\_}$ = V_{EE} + 2V		70		mA
External Gate Drive	V_{GS}	V_{GATE} - V_{EE}, power mode, gate drive on	9	10	11	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} = 32V to 60V, V_{EE} = 0V, V_{DD} to V_{DGND} = +3.3V, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT LIMIT							
Current-Limit Clamp Voltage	V_{SU_LIM}	Maximum $V_{SENSE\_}$ allowed during current limit, $V_{OUT\_}$ = 0V (ICUT = 000) (Note 3)	IVEE = 00	202	212	220	mV
			IVEE = 01	192	202	212	
			IVEE = 10	186	190	200	
			IVEE = 11	170	180	190	
Overcurrent Threshold After Startup	V_{FLT_LIM}	Overcurrent $V_{SENSE\_}$ threshold allowed for t ≤ t_{FAULT} after startup; $V_{OUT\_}$ = 0V, (IVEE = 00)	ICUT = 000 (Class 0/3)	177	186	196	mV
			ICUT =110 (Class 1)	47	55	62	
			ICUT = 111 (Class 2)	86	94	101	
			ICUT = 001	265	280	295	
			ICUT = 010	310	327	345	
			ICUT = 011	355	374	395	
			ICUT = 100	398	419	440	
			ICUT =101	443	466	488	
Foldback Initial OUT_ Voltage	V_{FLBK_ST}	$V_{OUT\_}$ - V_{EE}, above which the current-limit trip voltage starts folding back, IVEE = 00	ICUT = 000, ICUT = 110, ICUT = 111		28		V
			ICUT = 001…101		10		
Foldback Final OUT_ Voltage	V_{FLBK_END}	IVEE = 00, ICUT = 000, V_{OUT} - V_{EE} above which the current-limit trip voltage reaches V_{TH_FB}			50		V
Minimum Foldback Current-Limit Threshold	V_{TH_FB}	$V_{OUT\_}$ = V_{AGND} = 60V, IVEE = 00, ICUT = 000			64		mV
SENSE_ Input Bias Current		$V_{SENSE\_}$ = V_{EE}		-2		+2	µA

High-Power, Quad, PSE Controller for Power-Over-Ethernet

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} = 32V to 60V, V_{EE} = 0V, V_{DD} to V_{DGND} = +3.3V, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY MONITORS							
V_{EE} Undervoltage Lockout	V_{EEUVLO}	V_{AGND} - V_{EE}, V_{AGND} - V_{EE} increasing			28.5		V
V_{EE} Undervoltage Lockout Hysteresis	$V_{EEUVLOH}$	Ports shut down if V_{AGND} - V_{EE} < V_{UVLO} - $V_{EEUVLOH}$			3		V
V_{EE} Overvoltage Lockout	V_{EE_OV}	V_{EE_OV} event bit sets and ports shut down if V_{AGND} - V_{EE} > V_{EE_OV}, V_{AGND} increasing			62.5		V
V_{EE} Overvoltage Lockout Hysteresis	V_{OVH}				1		V
V_{EE} Undervoltage	V_{EE_UV}	V_{EE_UV} event bit is set if V_{AGND} - V_{EE} < V_{EE_UV}, V_{EE} increasing			40		V
V_{DD} Overvoltage	V_{DD_OV}	V_{DD_OV} event bit is set if V_{DD} - V_{DGND} > V_{DD_OV}; V_{DD} increasing	MAX5952A		3.82		V
			MAX5952C		5.7		
V_{DD} Undervoltage	V_{DD_UV}	V_{DD_OV} is set if V_{DD} - V_{DGND} > V_{DD_UV}, V_{DD} decreasing	MAX5952A		2.7		V
			MAX5952C		4.2		
V_{DD} Undervoltage Lockout	V_{DDUVLO}	Device operates when V_{DD} - V_{DGND} > V_{DDUVLO}, V_{DD} increasing			2		V
V_{DD} Undervoltage Lockout Hysteresis	V_{DDHYS}				120		mV
Thermal Shutdown Threshold	T_{SHD}	Ports shut down and device resets if its junction temperature exceeds this limit, temperature increasing (Note 4)			150		°C
Thermal Shutdown Hysteresis	T_{SHDH}	Thermal hysteresis, temperature decreasing (Note 5)			20		°C
OUTPUT MONITOR							
OUT_ Input Current	I_{BOUT}	V_{OUT} = V_{AGND}, all modes				2	µA
Idle Pullup Current at OUT_	I_{DIS}	OUT_ discharge current, detection and classification off, port shutdown, $V_{OUT\_}$ = V_{AGND} - 2.8V		200		260	µA
PGOOD High Threshold	PG_{TH}	$V_{OUT\_}$ - V_{EE}, OUT_ decreasing		1.5	2.0	2.5	V
PGOOD Hysteresis	PG_{HYS}				220		mV
PGOOD Low-to-High Glitch Filter	t_{PGOOD}	Minimum time PGOOD has to be high to set bit in register 10h			3		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} = 32V to 60V, V_{EE} = 0V, V_{DD} to V_{DGND} = +3.3V, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOAD DISCONNECT							
DC Load Disconnect Threshold	V_{DCTH}	Minimum V_{SENSE} allowed before disconnect (DC disconnect active), $V_{OUT\_}$ = 0V		2.5	3.75	5.0	mV
AC Load Disconnect Threshold (Note 6)	I_{ACTH}	Current into DET_, for I < I_{ACTH} the port powers off, ACD_EN_ bit = H; V_{OSC_IN} = 2.2V		300	320	350	µA
Oscillator Buffer Gain	A_{OSC}	$V_{DET\_}/V_{OSC}$, ACD_EN_ bit = H		2.9	3.0	3.1	V/V
OSC Fail Threshold (Note 7)	V_{OSC_FAIL}	Port does not power on if V_{OSC} < V_{OSC_FAIL} and ACD_EN_ bit is high		1.8		2.2	V
OSC Input Impedance	Z_{OSC}	OSC input impedance when all the ACD_EN_ are active		100			kΩ
Load Disconnect Timer	t_{DISC}	Time from V_{SENSE} < V_{DCTH} to gate shutdown (Note 8)		300		400	ms
DETECTION							
Detection Probe Voltage (First Phase)	V_{DPH1}	V_{AGND} - $V_{DET\_}$ during the first detection phase		3.8	4	4.2	V
Detection Probe Voltage (Second Phase)	V_{DPH2}	V_{AGND} - $V_{DET\_}$ during the second detection phase		9.0	9.3	9.6	V
Current-Limit Protection	I_{DLIM}	$V_{DET\_}$ = V_{AGND}, during detection, measure current through DET_		1.5	1.75	2.0	mA
Short-Circuit Threshold	V_{DCP}	If V_{AGND} - V_{OUT} < V_{DCP} after the first detection phase a short circuit to AGND is detected			1		V
Open-Circuit Threshold	I_{D_OPEN}	First point measurement current threshold for open condition			12.5		µA
Resistor Detection Window	R_{DOK}	(Note 9)		19.0		26.5	kΩ
Resistor Rejection Window	R_{DBAD}	Detection rejects lower values				15.2	kΩ
		Detection rejects higher values		32			
CLASSIFICATION							
Classification Probe Voltage	V_{CL}	V_{AGND} - $V_{DET\_}$ during classification		16		20	V
Current-Limit Protection	I_{CILIM}	DET_ = AGND, during classification, measure current through DET_		68		81	mA
Classification Current Thresholds	I_{CL}	Classification current thresholds between classes	Class 0, Class 1	5.5	6.5	7.5	mA
			Class 1, Class 2	13	14.5	16	
			Class 2, Class 3	21	23	25	
			Class 3, Class 4	31	33	35	
			Class 4, Class 5	45	48	51	

High-Power, Quad, PSE Controller for Power-Over-Ethernet

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} = 32V to 60V, V_{EE} = 0V, V_{DD} to V_{DGND} = +3.3V, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS/OUTPUTS (Referred to DGND)							
Digital Input Low	V_{IL}					0.9	V
Digital Input High	V_{IH}			2.4			V
Internal Input Pullup/Pulldown Resistor	R_{DIN}	Pullup (pulldown) resistor to V_{DD} (DGND) to set default level		25	50	75	kΩ
Open-Drain Output Low Voltage	V_{OL}	I_{SINK} = 15mA				0.4	V
Digital Input Leakage	I_{DL}	Input connected to the pull voltage				2	µA
Open-Drain Leakage	I_{OL}	Open-drain high impedance, V_O = 3.3V				2	µA
TIMING							
Startup Time	t_{START}	Time during which a current limit set by V_{SU_LIM} is allowed, starts when the GATE_ is turned on (Note 5)		50	60	70	ms
Fault Time	t_{FAULT}	Maximum allowed time for an overcurrent condition set by V_{FLT_LIM} after startup (Note 5)		50	60	70	ms
Port Turn-Off Time	t_{OFF}	Minimum delay between any port turning off, does not apply in case of a reset			0.5		ms
Detection Reset Time		Time allowed for the port voltage to reset before detection starts			80	90	ms
Detection Time	t_{DET}	Maximum time allowed before detection is completed				330	ms
Midspan Mode Detection Delay	t_{DMID}			2.0		2.4	s
Classification Time	t_{CLASS}	Time allowed for classification			19	23	ms
V_{EEUVLO} Turn-On Delay	t_{DLY}	Time V_{AGND} must be above the V_{EEUVLO} thresholds before the device operates		2		4	ms
Restart Timer	$t_{RESTART}$	Time a port has to wait before turning on after an overcurrent fault, RSTR_EN_ bits = high	RSTR bits = 00		16 x t_{FAULT}		ms
			RSTR bits = 01		32 x t_{FAULT}		
			RSTR bits = 10		64 x t_{FAULT}		
			RSTR bits = 11		0		
Watchdog Clock Period	t_{WD}	Rate of decrement of the watchdog timer			164		ms
ADC PERFORMANCE							
Resolution					9		Bits
Range					0.51		V
LSB Step Size					1		mV
Integral Nonlinearity (Relative)	INL				0.5		LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AGND} = 32V to 60V, V_{EE} = 0V, V_{DD} to V_{DGND} = +3.3V, all voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = +48V, V_{DGND} = +48V, V_{DD} = (V_{DGND} + 3.3V), T_A = +25°C. Currents are positive when entering the pin and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Nonlinearity	DNL			0.1		LSB
ADC Absolute Accuracy		V_{SENSE} = 100mV	5B (91)	62 (98)	68 (104)	Hex (Dec)
		V_{SENSE} = 250mV	F0 (240)	FC (252)	108 (264)	
		V_{SENSE} = 400mV	186 (390)	196 (406)	1A6 (422)	
TIMING CHARACTERISTICS (For 2-Wire Fast Mode, Note 10)						
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.2			µs
Hold Time for a START Condition	$t_{HD, STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.2			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition (Sr)	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$		0		150	ns
Data in Setup Time	$t_{SU, DAT}$		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R		20 + 0.1C_B		300	ns
Fall Time of SDA Transmitting	t_F		20 + 0.1C_B		300	ns
Setup Time for STOP Condition	$t_{SU, STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B				400	pF
Pulse Width of Spike Suppressed	t_{SP}				50	ns

Note 2: Limits to T_A = -40°C are guaranteed by design.

Note 3: Default values. The current-limit thresholds are programmed through the I²C-compatible serial interface (see the *Register Map and Description* section).

Note 4: Functional test is performed over thermal shutdown entering test mode.

Note 5: Default values. The startup and fault times can be also programmed through the I²C serial interface (see the *Register Map and Description* section).

Note 6: This is the default value. Threshold can be programmed through serial interface R23h[2:0].

Note 7: AC disconnect works only if (V_{DD} - V_{DGND}) ≥ 3V and DGND is connected to AGND.

Note 8: t_{DISC} can also be programmed through the serial interface (R16H) (see the *Register Map and Description* section).

Note 9: R_D = (V_{OUT_2} - V_{OUT_1}) / (I_{DET_2} - I_{DET_1}). V_{OUT_1}, V_{OUT_2}, I_{DET_2} and I_{DET_1} represent the voltage at OUT_ and the current at DET_ during phase 1 and 2 of the detection.

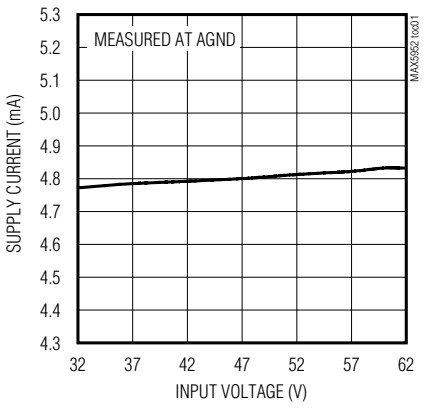
Note 10: Guaranteed by design. Not subject to production testing.

High-Power, Quad, PSE Controller for Power-Over-Ethernet

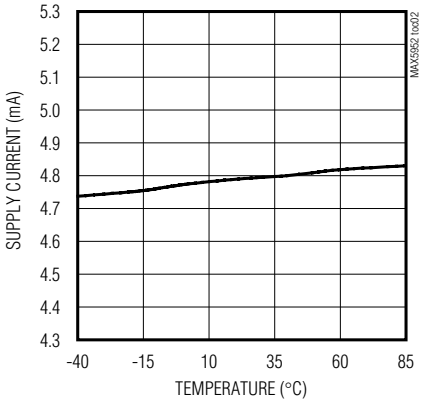
Typical Operating Characteristics

(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, R_{SENSE} = 0.5Ω, IVEE = 00, ICUT = 000, T_A = +25°C, all registers = default setting, unless otherwise noted.)

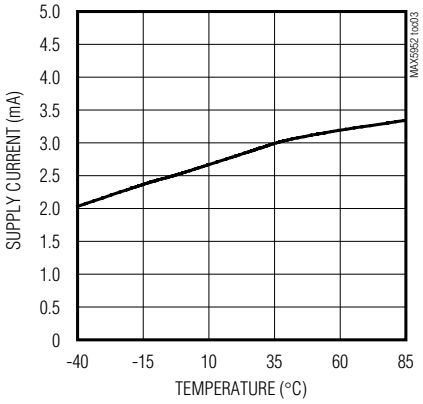
ANALOG SUPPLY CURRENT vs. INPUT VOLTAGE



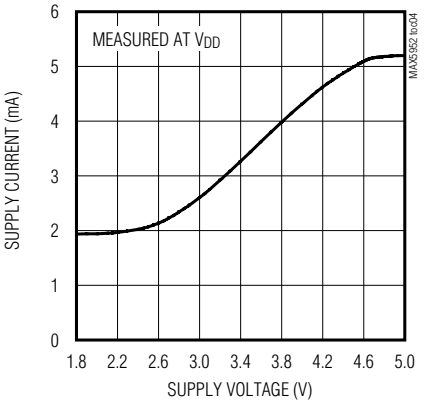
ANALOG SUPPLY CURRENT vs. TEMPERATURE



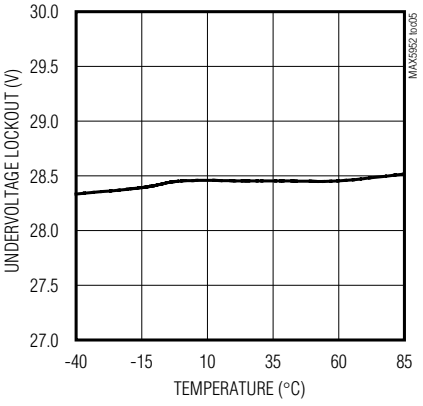
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



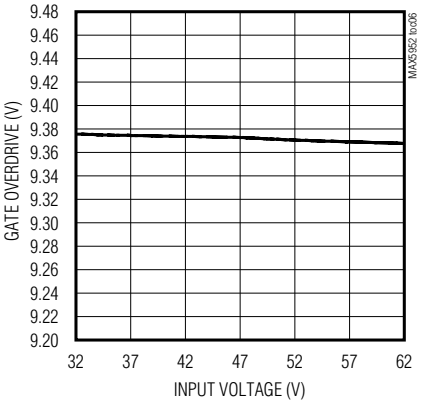
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



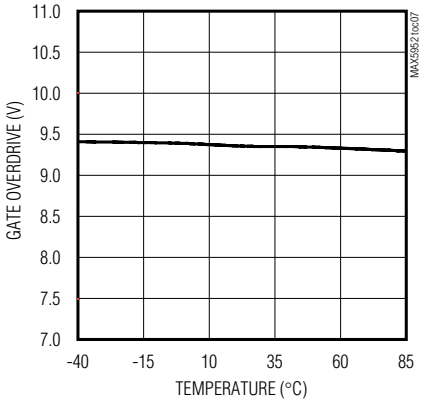
VEE UNDERVOLTAGE LOCKOUT vs. TEMPERATURE



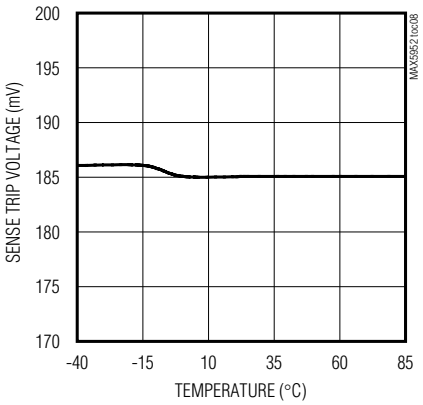
GATE OVERDRIVE vs. INPUT VOLTAGE



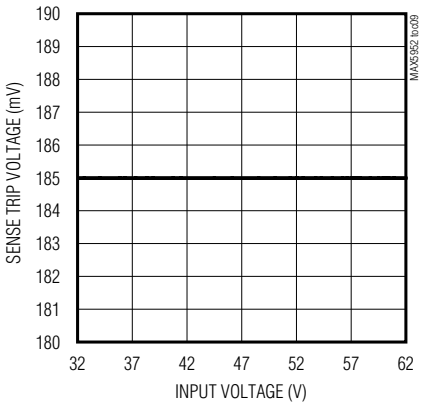
GATE OVERDRIVE vs. TEMPERATURE



SENSE TRIP VOLTAGE vs. TEMPERATURE



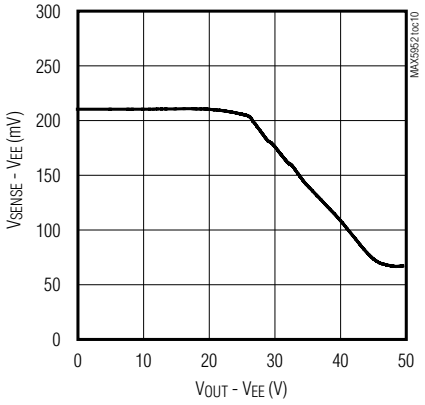
SENSE TRIP VOLTAGE vs. INPUT VOLTAGE



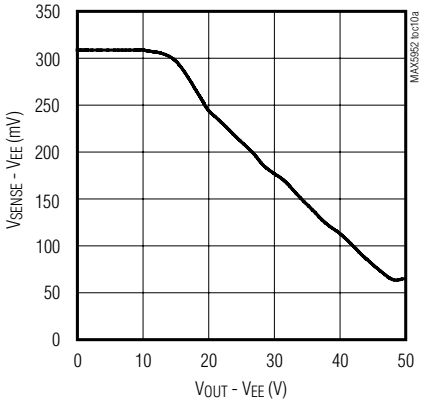
Typical Operating Characteristics (continued)

(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, R_{SENSE} = 0.5Ω, IVEE = 00, ICUT = 000, T_A = +25°C, all registers = default setting, unless otherwise noted.)

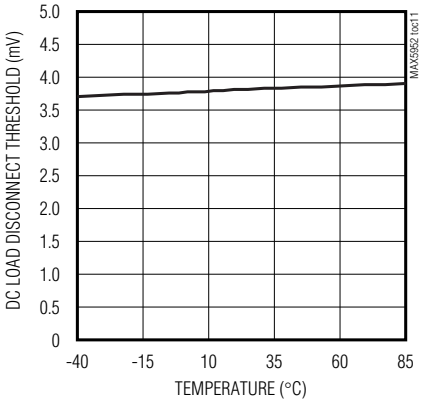
FOLDBACK CURRENT-LIMIT THRESHOLD vs. OUTPUT VOLTAGE



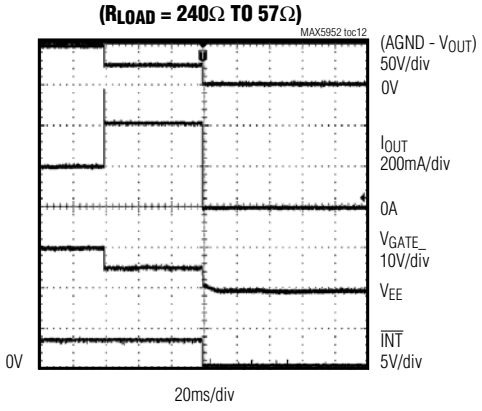
FOLDBACK CURRENT-LIMIT THRESHOLD vs. OUTPUT VOLTAGE



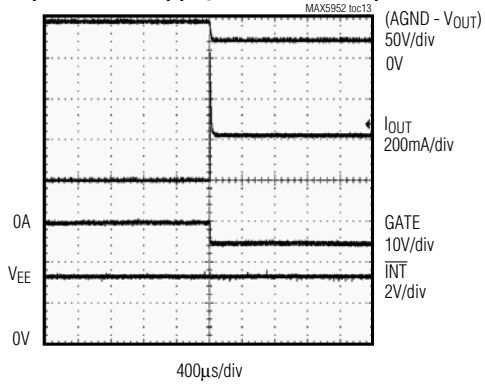
DC LOAD DISCONNECT THRESHOLD vs. TEMPERATURE



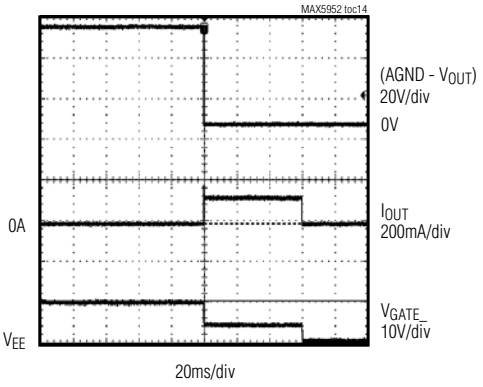
OVERCURRENT TIMEOUT (R_{LOAD} = 240Ω TO 57Ω)



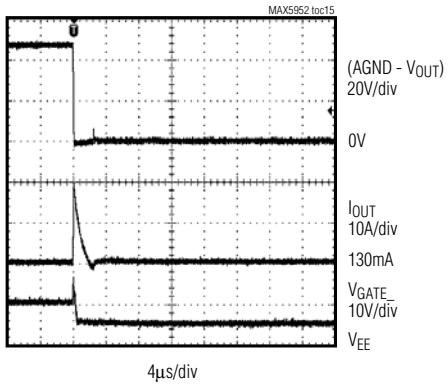
OVERCURRENT RESPONSE WAVEFORM (MAX5952AUAX) (R_{LOAD} = 240Ω TO 57Ω)



SHORT-CIRCUIT RESPONSE TIME



SHORT-CIRCUIT RESPONSE TIME

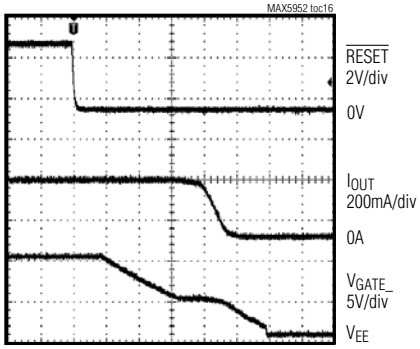


High-Power, Quad, PSE Controller for Power-Over-Ethernet

Typical Operating Characteristics (continued)

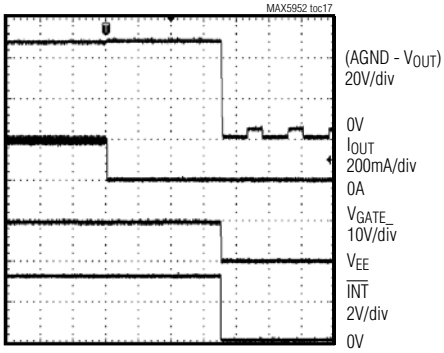
(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, R_{SENSE} = 0.5Ω, IVEE = 00, ICUT = 000, T_A = +25°C, all registers = default setting, unless otherwise noted.)

$\overline{RESET}$ TO OUT TURN-OFF DELAY



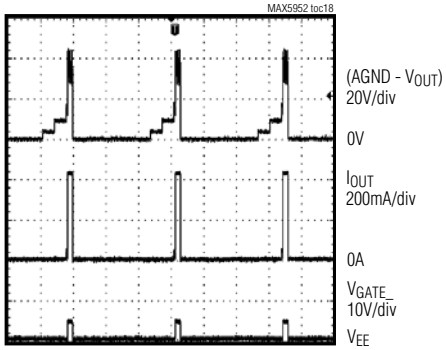
100µs/div

ZERO-CURRENT DETECTION WAVEFORM



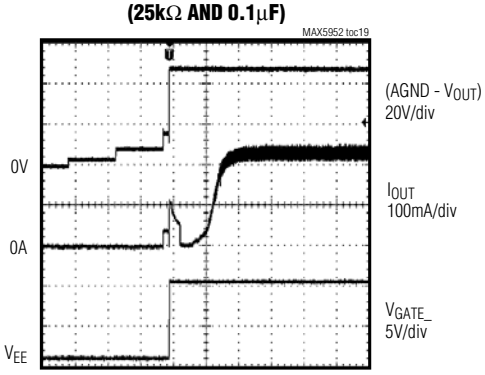
100ms/div

OVERCURRENT RESTART DELAY



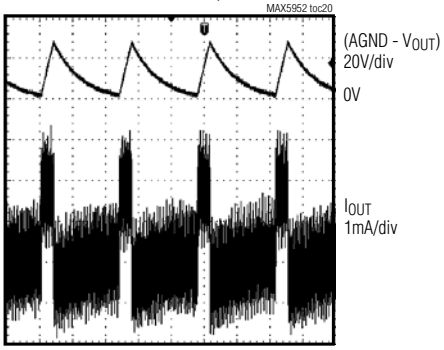
400ms/div

STARTUP WITH VALID PD (25kΩ AND 0.1µF)



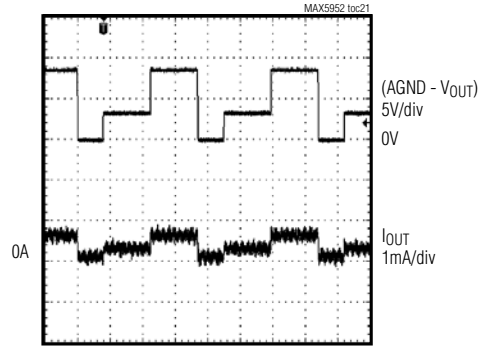
100ms/div

DETECTION WITH INVALID PD (25kΩ AND 10µF)



40ms/div

DETECTION WITH INVALID PD (15kΩ)

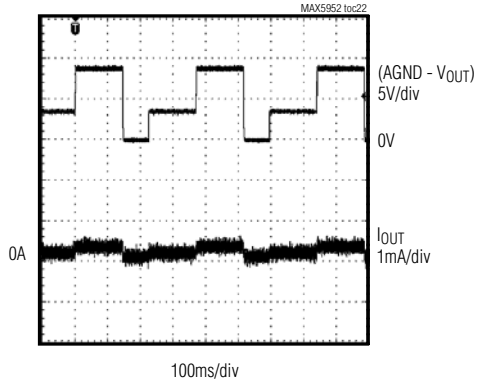


100ms/div

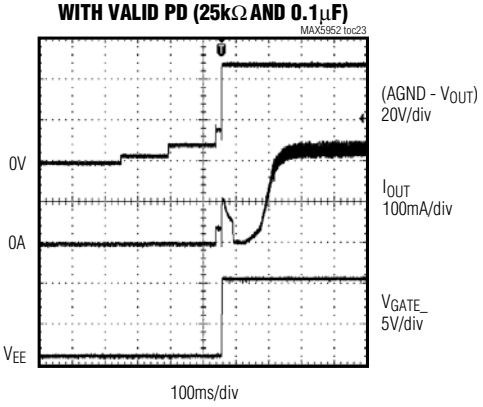
Typical Operating Characteristics (continued)

(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, R_{SENSE} = 0.5Ω, IVEE = 00, ICUT = 000, T_A = +25°C, all registers = default setting, unless otherwise noted.)

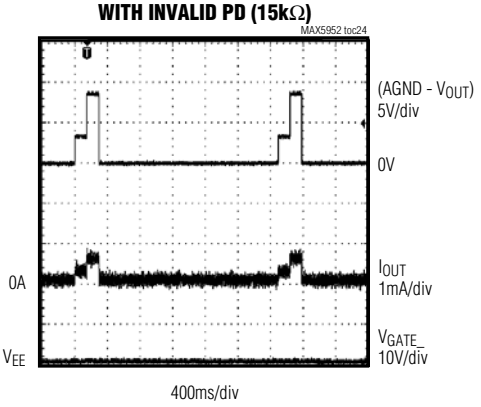
DETECTION WITH INVALID PD (33kΩ)



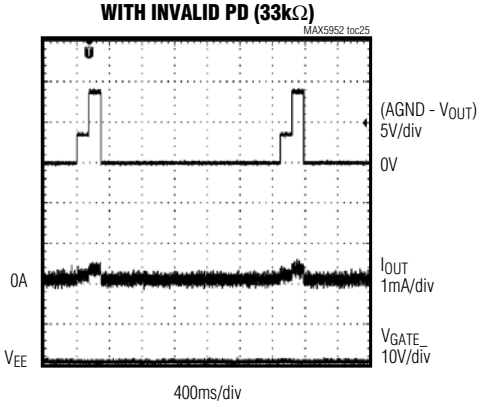
STARTUP IN MIDSPAN MODE WITH VALID PD (25kΩ AND 0.1µF)



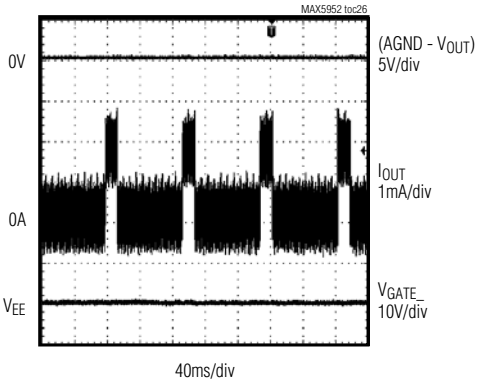
DETECTION WITH MIDSPAN MODE WITH INVALID PD (15kΩ)



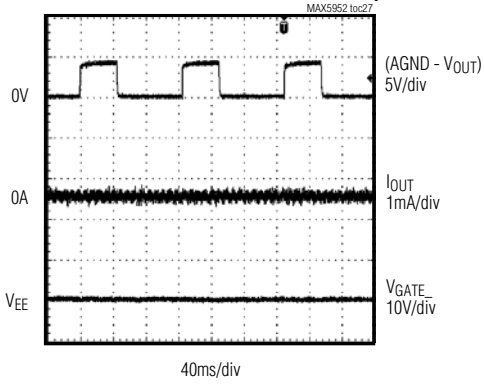
DETECTION WITH MIDSPAN MODE WITH INVALID PD (33kΩ)



DETECTION WITH OUTPUT SHORTED



DETECTION WITH INVALID PD (OPEN CIRCUIT, USING *TYPICAL OPERATING CIRCUIT 1*)

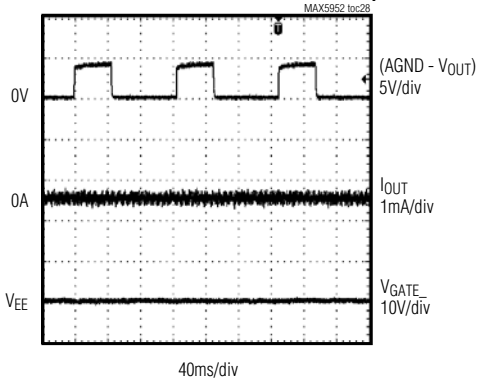


High-Power, Quad, PSE Controller for Power-Over-Ethernet

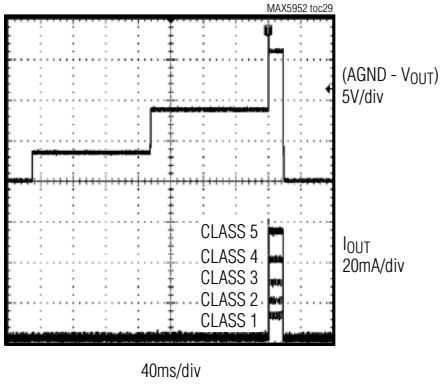
Typical Operating Characteristics (continued)

(V_{EE} = -48V, V_{DD} = +3.3V, V_{AUTO} = V_{AGND} = V_{DGND} = 0V, $\overline{RESET}$ = $\overline{SHD\_}$ = unconnected, R_{SENSE} = 0.5Ω, IVEE = 00, ICUT = 000, T_A = +25°C, all registers = default setting, unless otherwise noted.)

DETECTION WITH INVALID PD (OPEN CIRCUIT, USING *TYPICAL OPERATING CIRCUIT 2*)



STARTUP WITH DIFFERENT PD CLASSES



Pin Description

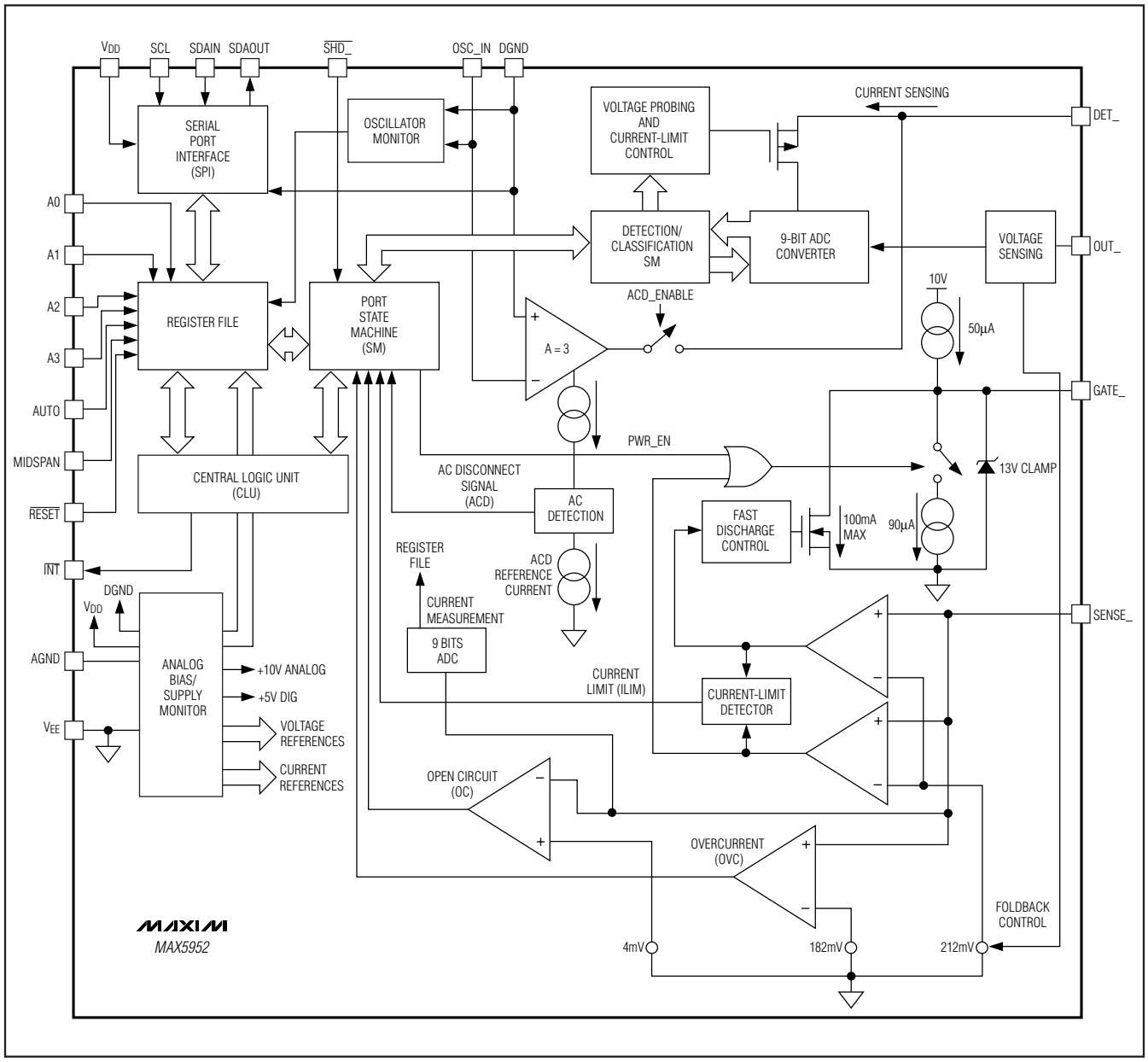
PIN	NAME	FUNCTION
1	$\overline{RESET}$	Hardware Reset. Pull $\overline{RESET}$ low for at least 300µs to reset the device. All internal registers reset to their default value. The address (A0–A3), and AUTO and MIDSPAN input-logic levels latch on during low-to-high transition of $\overline{RESET}$. $\overline{RESET}$ is internally pulled up to V_{DD} with a 50kΩ resistor.
2	MIDSPAN	Midspan Mode Input. An internal 50kΩ pulldown resistor to DGND sets the default mode to end-point PSE operation (power-over-signal pairs). Pull MIDSPAN to V_{DIG} to set midspan operation. The MIDSPAN value latches after the IC is powered up or reset (see the *PD Detection* section).
3	$\overline{INT}$	Open-Drain Interrupt Output. $\overline{INT}$ goes low whenever a fault condition exists. Reset the fault condition using software or by pulling $\overline{RESET}$ low (see the *Interrupt* section for more information about interrupt management).
4	SCL	Serial Interface Clock Line Input
5	SDAOUT	Serial Output Data Line. Connect the data line optocoupler input to SDAOUT (see the *Typical Operating Circuits*). Connect SDAOUT to SDAIN if using a 2-wire, I^2C-compatible system.
6	SDAIN	Serial Interface Input Data Line. Connect the data line optocoupler output to SDAIN (see the *Typical Operating Circuits*). Connect SDAIN to SDAOUT if using a 2-wire, I^2C-compatible system.

Pin Description (continued)

PIN	NAME	FUNCTION
7–10	A3–A0	Address Bits. A3–A0 form the lower part of the device's address. Address inputs default high with an internal 50kΩ pullup resistor to V_{DD}. The address values latch when V_{DD} or V_{EE} ramps up and exceeds its UVLO threshold or after a reset. The 3 MSBs of the address are set to 010.
11–14	DET1–DET4	Detection/Classification Voltage Outputs. Use DET1 to set the detection and classification probe voltages on port 1. Use DET1 for the AC voltage sensing of port 1 when using the AC disconnect scheme (see the *Typical Operating Circuits*).
15	DGND	Digital Ground. Connect to digital ground.
16	V_{DD}	Positive Digital Supply. Connect to a digital power supply (reference to DGND).
17– 20	$\overline{SHD1}$–$\overline{SHD4}$	Port Shutdown Inputs. Pull $\overline{SHD\_}$ low to turn off the external FET on port_. Internally pulled up to V_{DD} with a 50kΩ resistor.
21	AGND	Analog Ground. Connect to the high-side analog supply.
22, 25, 29, 32	SENSE4, SENSE3, SENSE2, SENSE1	MOSFET Source Current-Sense Negative Inputs. Connect to the source of the power MOSFET and connect a current-sense resistor between SENSE_ and V_{EE} (see the *Typical Operating Circuits*).
23, 26, 30, 33	GATE4, GATE3, GATE2, GATE1	Port_ MOSFET Gate Drivers. Connect GATE_ to the gate of the external MOSFET (see the *Typical Operating Circuits*).
24, 27, 31, 34	OUT4, OUT3, OUT2, OUT1	MOSFET Drain-Output Voltage Senses. Connect OUT_ to the power MOSFET drain through a resistor (100Ω to 100kΩ). The low leakage at OUT_ limits the drop across the resistor to less than 100mV (see the *Typical Operating Circuits*).
28	V_{EE}	Low-Side Analog Supply Input. Connect the low-side analog supply to V_{EE} (-48V). Bypass with a 1µF capacitor between AGND and V_{EE}.
35	AUTO	Auto or Shutdown Mode Input. Force AUTO high to enter auto mode after a reset or power-up. Drive low to put the MAX5952 into shutdown mode. In shutdown mode, software controls the operational modes of the MAX5952. A 50kΩ internal pulldown resistor defaults to AUTO low. AUTO latches when V_{DD} or V_{EE} ramps up and exceeds its UVLO threshold or when the device resets. Software commands can take the MAX5952 out of AUTO while AUTO is high.
36	OSC	Oscillator Input. AC-disconnect detection function uses OSC. Connect a 100Hz ±10%, $2V_{P-P}$ ±5%, +1.2V offset sine wave to OSC. If the oscillator positive peak falls below the OSC_FAIL threshold of 2V, the ports that have the AC function enabled shut down and are not allowed to power-up. When not using the AC-disconnect detection function, leave OSC unconnected.

High-Power, Quad, PSE Controller for Power-Over-Ethernet

Functional Diagram



Detailed Description

The MAX5952 is a quad -48V power controller designed for use in IEEE 802.3af-compliant/pre-IEEE 802.3at-compatible PSE. This device provides PD discovery, classification, current limit, DC and AC load disconnect detections in compliance with the IEEE 802.3af standard. The MAX5952 is pin compatible with the MAX5945/LTC4258/LTC4259A PSE controllers and provides additional features.

The MAX5952 features a high-power mode which provides up to 45W per port. The device allows the user to program the current-limit and overcurrent thresholds up to 2.5 times the default thresholds. The MAX5952 can also be programmed to decrease the current-limit and overcurrent threshold by 15% for high operating voltage conditions to keep the output power constant.

The MAX5952 provides instantaneous readout of each port current through the I^2C interface. The MAX5952 also provides high-capacitance detection for legacy PDs.

The MAX5952 is fully software configurable and programmable through an I^2C-compatible, 3-wire serial interface with 49 registers. The class-overcurrent detection function enables system power management to detect if a PD draws more than the allowable current. The MAX5952's extensive programmability enhances system flexibility, enables field diagnosis, and allows for uses in other applications.

The MAX5952 provides four operating modes to suit different system requirements. Auto mode allows the device to operate automatically without any software supervision. Semi-auto mode automatically detects and classifies a device connected to a port after initial software activation but does not power up that port until instructed to by software. Manual mode allows total software control of the device and is useful for system diagnostics. Shutdown mode terminates all activities and securely turns off power to the ports.

The MAX5952 provides input undervoltage lockout, input undervoltage detection, input overvoltage lockout, overtemperature detection, output voltage slew-rate limit during startup, power-good, and fault status. The MAX5952's programmability includes startup timeout, overcurrent timeout, and load-disconnect detection timeout.

The MAX5952 communicates with the system microcontroller through an I^2C-compatible interface. The MAX5952 features separate input and output data lines (SDAIN and SDAOUT) for use with optocoupler isolation. As a slave device, the MAX5952 includes four address inputs allowing 16 unique addresses. A separate $\overline{INT}$ output and four independent shutdown inputs ($\overline{SHD\_}$) provide fast response from a fault to port shutdown between the MAX5952 and the microcontroller. A $\overline{RESET}$ input allows hardware reset of the device.

Reset

Reset is a condition the MAX5952 enters after any of the following conditions:

1) After power-up (V_{EE} and V_{DD} rise above their UVLO thresholds).
2) Hardware reset. The $\overline{RESET}$ input is driven low and back high again any time after power-up.
3) Software reset. Writing a 1 into R1Ah[4] any time after power-up.
4) Thermal shutdown.

During a reset, the MAX5952 resets its register map to the reset state as shown in Table 37 and latches in the state of AUTO (pin 35) and MIDSPAN (pin 2). During normal operation, change at the AUTO and MIDSPAN input is ignored. While the condition that caused the reset persists (i.e. high temperature, $\overline{RESET}$ input low, or UVLO conditions) the MAX5952 does not acknowledge any addressing from the serial interface.

Port Reset (R1Ah[3:0])

Set high anytime during normal operation to turn off power and clear the events and status registers of the corresponding port. Port reset only resets the events and status registers.

Midspan Mode

In midspan mode, the device adopts cadence timing during the detection phase. When cadence timing is enabled and a failed detection occurs, the port waits between 2s and 2.4s before attempting to detect again. Midspan mode is activated by setting R11[1] high. The status of the MIDSPAN pin is written to R11[1] during power-up or after a reset. MIDSPAN is internally pulled low by a 50kΩ resistor.

High-Power, Quad, PSE Controller for Power-Over-Ethernet

Operation Modes

The MAX5952 contains four independent, but identical state machines to provide reliable and real-time control of the four network ports. Each state machine has four operating modes: auto mode, semi-auto mode, manual, and shutdown. Auto mode allows the device to operate automatically without any software supervision. Semi-auto mode, upon request, continuously detects and classifies a device connected to a port but does not power up that port until instructed by software. Manual mode allows total software control of the device and is useful in system diagnostics. Shutdown mode terminates all activities and securely turns off power to the ports.

Switching between auto, semi, or manual mode does not interfere with the operation of the port. When the port is set into shutdown mode, all the port operations are immediately stopped and the port remains idle until shutdown is exited.

Automatic (Auto) Mode

Enter automatic (auto) mode by forcing the AUTO input high prior to a reset, or by setting R12h[P_M1,P_M0] to [1,1] during normal operation (see Tables 16 and 16a). In auto mode, the MAX5952 performs detection, classification, and powers up the port automatically once a valid PD is detected at the port. If a valid PD is not connected at the port, the MAX5952 repeats the detection routine continuously until a valid PD is connected.

Going into auto mode, the DET_EN and CLASS_EN bits are set to high and stay high unless changed by software. Using software to set DET_EN and/or CLASS_EN low causes the MAX5952 to skip detection and/or classification. As a protection, disabling the detection routine in auto mode does not allow the corresponding port to power up, unless the DET_BY (R23H[4]) is set to 1.

The AUTO status is latched into the register only during a reset. Any changes to the AUTO input after reset are ignored.

Semi-Automatic (Semi-Auto) Mode

Enter semi-auto mode by setting R12h[P_M1,P_M0] to [1,0] during normal operation (see Tables 16 and 16a). In semi-auto mode, the MAX5952, upon request, performs detection and/or classification repeatedly but does not power up the port(s), regardless of the status of the port connection.

Setting R19h[PWR_ON_] (Table 22) high immediately terminates detection/classification routines and turns on power to the port(s).

R14h[DET_EN_, CLASS_EN_] default to low in semi-auto mode. Use software to set R14h[DET_EN_, CLASS_EN_] to high to start the detection and/or classification routines. R14h[DET_EN_, CLASS_EN_] are reset every time the software commands a power off of the port (either through reset or PWR_OFF). In any other case, the status of the bits is left unchanged (including when the state machine turns off the power because a load disconnect or a fault condition is encountered).

Manual Mode

Enter manual mode by setting R12h[P_M1,P_M0] to [0,1] during normal operation (see Tables 16 and 16a). Manual mode allows the software to dictate any sequence of operation. Write a 1 to both R14h[DET_EN_] and R14h[CLASS_EN_] to start detection and classification operations, respectively, and in that priority order. After execution, the command is cleared from the register(s). PWR_ON_ has highest priority. Setting PWR_ON_ high at any time causes the device to immediately enter the powered mode. Setting DET_EN and CLASS_EN high at the same time causes detection to be performed first. Once in the powered state, the device ignores DET_EN_ or CLASS_EN_ commands.

When switching to manual mode from another mode, DET_EN_, CLASS_EN_ default to low. These bits become pushbutton rather than configuration bits (i.e., writing ones to these bits while in manual mode commands the device to execute one cycle of detection and/or classification. The bits are reset back to zeros at the end of the execution).

Shutdown Mode

Enter shutdown mode by forcing the AUTO input low prior to a reset, or by setting R12h[P_M1,P_M0] to [0,0] during normal operation (see Tables 16 and 16a). Putting the MAX5952 into shutdown mode immediately turns off power and halts all operations to the corresponding port. The event and status bits of the affected port(s) are also cleared. In shutdown mode, the DET_EN_, CLASS_EN_ and PWR_ON_ commands are ignored.

In shutdown mode, the serial interface operates normally.

PD Detection

When PD detection is activated, the MAX5952 probes the output for a valid PD. After each detection cycle, the device sets the DET_END_ bit R04h/05h[3:0] high and reports the detection results in the status registers R0Ch[2:0], R0Dh[2:0], R0Eh[2:0], and R0Fh[2:0]. The DET_END_ bit is reset to low when read through R05h or after a port reset.

A valid PD has a 25kΩ discovery signature characteristic as specified in the IEEE 802.3af/at standard. Table 1 shows the IEEE 802.3af/at specification for a PSE detecting a valid PD signature. See the *Typical Operating Circuits* and Figure 1 (Detection, Classification, and Power-Up Port Sequence). The MAX5952 can probe and categorize different types of devices connected to the port such as: a valid PD, an open circuit, a low resistive load, a high resistive load, a high capacitive load, a positive DC supply, or a negative DC supply.

During detection, the MAX5952 keeps the external MOSFET off and forces two probe voltages through the DET_ input. The current through the DET_ input is measured as well as the voltage at OUT_. A two-point slope measurement is used as specified by the IEEE 802.3af standard to verify the device connected to the port. The MAX5952 implements appropriate settling times and a 100ms digital integration to reject 50Hz/60Hz power-line noise coupling.

An external diode, in series with the DET_ input, restricts PD detection to the first quadrant as specified by the IEEE 802.3af/at standard. To prevent damage to non-PD devices, and to protect itself from an output short circuit, the MAX5952 limits the current into DET_ to less than 2mA maximum during PD detection.

In midspan mode, the MAX5952 waits 2.2s before attempting another detection cycle after every failed detection. The first detection, however, happens immediately after issuing the detection command.

High-Capacitance Detection

The CLC_EN bit in register R23h[5] enables the large capacitor detection feature for legacy PD devices. When CLC_EN = 1, the high-capacitance detection limit is extended up to 100µF. CLC_EN = 0 is the default condition for the normal capacitor size detection. See Table 1 and the *Register Map and Description* section.

Table 1. PSE PI Detection Modes Electrical Requirement (Table 33-2 of the IEEE 802.3af Standard)

PARAMETER	SYMBOL	MIN	MAX	UNITS	ADDITIONAL INFORMATION
Open-Circuit Voltage	V_{OC}	—	30	V	In detection mode only
Short-Circuit Current	I_{SC}	—	5	mA	In detection mode only
Valid Test Voltage	V_{VALID}	2.8	10	V	
Voltage Difference Between Test Points	ΔV_{TEST}	1	—	V	
Time Between Any Two Test Points	t_{BP}	2	—	ms	This timing implies a 500Hz maximum probing frequency
Slew Rate	V_{SLEW}		0.1	V/µs	
Accept Signature Resistance	R_{GOOD}	19	26.5	kΩ	
Reject Signature Resistance	R_{BAD}	< 15	> 33	kΩ	
Open-Circuit Resistance	R_{OPEN}	500	—	kΩ	
Accept Signature Capacitance	C_{GOOD}	—	150	nF	
Reject Signature Capacitance	C_{BAD}	10	—	µF	
Signature Offset Voltage Tolerance	V_{OS}	0	2.0	V	
Signature Offset Current Tolerance	I_{OS}	0	12	µA	

High-Power, Quad, PSE Controller for Power-Over-Ethernet

Powered Device Classification (PD Classification)

During the PD classification mode, the MAX5952 forces a probe voltage (-18V) at DET_ and measures the current into DET_. The measured current determines the class of the PD.

After each classification cycle, the device sets the CL_END_ bit (R04h/05h[7:4]) high and reports the classification results in the status registers R0Ch[6:4], R0Dh[6:4], R0Eh[6:4], and R0Fh[6:4]. The CL_END_ bit is reset to low when read through register R05h or after a port reset. Both status registers, R04h, and R05h are cleared after the port powers down. Table 2 shows the IEEE 802.3af requirement for a PSE classifying a PD at the power interface (PI).

The MAX5952 supports high power beyond the IEEE 802.3af standard by providing additional classifications (Class 5 and ping-pong classification).

Powered State

When the MAX5952 enters a powered state, the t_{START} and t_{DISC} timers are reset. Before turning on the port power, the MAX5952 checks if any other port is not turning on and if the t_{FAULT} timer is zero. Another check is performed if the ACD_EN bit is set, in this case the OSC_FAIL bit must be low (oscillator is okay) for the port to be powered.

Table 2. PSE Classification of a PD (Table 33-4 of the IEEE 802.3af)

MEASURED I_{CLASS} (mA)	CLASSIFICATION
0 to 5	Class 0
> 5 and < 8	May be Class 0 and 1
8 to 13	Class 1
> 13 and < 16	May be Class 1 or 2
16 to 21	Class 2
> 21 and < 25	May be Class 2 or 3
25 to 31	Class 3
> 31 and < 35	May be Class 3 or 4
35 to 45	Class 4
> 45 and < 51	May be Class 4 or 5
51 to 68	Class 5

If these conditions are met, the MAX5952 enters startup where it turns on power to the port. An internal signal, POK_, asserts high when V_{OUT} is within 2V from V_{EE}. PGOOD_ status bits are set high if POK_ stays high longer than t_{PGOOD}. PGOOD immediately resets when POK goes low.

The PG_CHG_ bit sets when a port powers up or down. PWR_EN sets when a port powers up and resets when a port shuts down. The port shutdown timer lasts 0.5ms and prevents other ports from turning off during that period, except in the case of emergency shutdowns ($\overline{RESET}$ = L, RESET_IC = H, V_{EEUVLO}, V_{DDUVLO}, and TSHD).

The MAX5952 always checks the status of all ports before turning off. A priority logic system determines the order to prevent the simultaneous turn-on or turn-off of the ports. The port with the lesser ordinal number gets priority over the others (i.e., port 1 turns on first, port 2 second, port 3 third and port 4 fourth). Setting PWR_OFF_ high turns off power to the corresponding port.

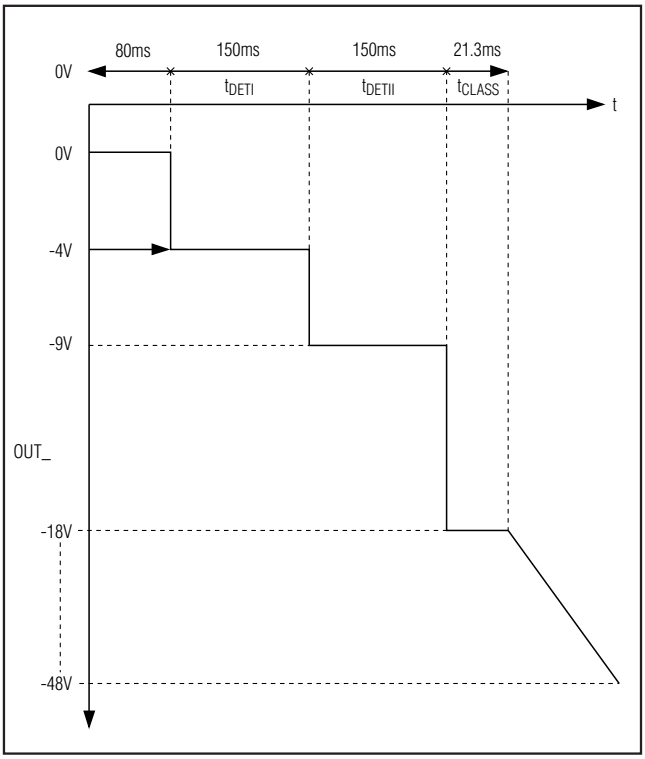


Figure 1. Detection, Classification, and Power-Up Port Sequence

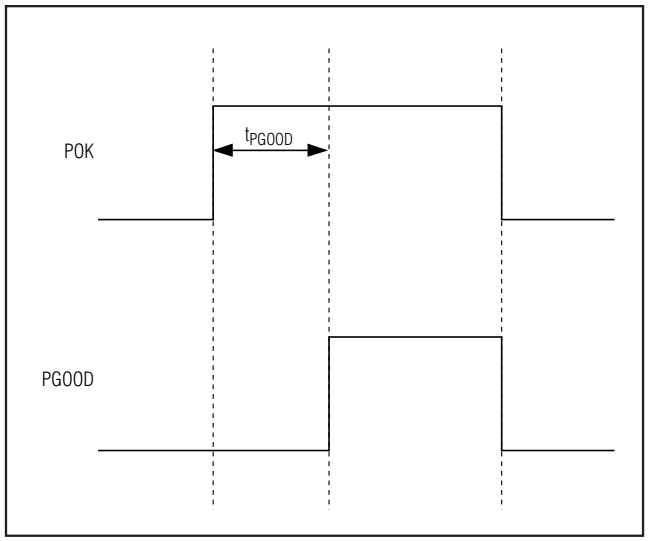


Figure 2. PGOOD Timing

Overcurrent Protection

A sense resistor R_S connected between SENSE_ and V_{EE} monitors the load current. Under normal operating conditions, the voltage across R_S (V_{RS}) never exceeds the threshold V_{SU_LIM}. If V_{RS} exceeds V_{SU_LIM}, an internal current-limiting circuit regulates the GATE voltage, limiting the current to $I_{LIM} = V_{SU\_LIM} / R_S$. During transient conditions, if V_{RS} exceeds V_{SU_LIM} by more than 1V, a fast pulldown circuit activates to quickly recover from the current overshoot. During startup, if the current-limit condition persists, when the startup timer, t_{START}, times out, the port shuts off, and the STRT_FLT_ bit is set. In the normal powered state, the MAX5952 checks for overcurrent conditions as determined by V_{FLT_LIM} = ~88% of V_{SU_LIM}. The t_{FAULT} counter sets the maximum allowed continuous overcurrent period. The t_{FAULT} counter increases when V_{RS} exceeds V_{FLT_LIM} and decreases at a slower pace when V_{RS} drops below V_{FLT_LIM}. A slower decrement for the t_{FAULT} counter allows for detecting repeated short-duration overcurrents. When the counter reaches the t_{FAULT} limit, the MAX5952 powers off the port and asserts the IMAX_FLT_ bit. For a continuous overstress, a fault latches exactly after a period of t_{FAULT}. V_{SU_LIM} is programmable through the ICUT registers R2Ah[6:4], R2Ah[2:0], R2Bh[6:4], R2Bh[2:0], and the IVEE bits in register R29h[1:0]. See the *High-Power Mode* section for more information on the ICUT register.

After power-off due to an overcurrent fault, and if the RSTR_EN bit is set, the t_{FAULT} timer is not immediately reset but starts decrementing at the same slower pace. The MAX5952 allows the port to be powered on only when the t_{FAULT} counter is at zero. This feature sets an automatic duty-cycle protection to the external MOSFET avoiding overheating.

The MAX5952 continuously flags when the current exceeds the maximum current allowed for the class as indicated in the CLASS status register. When class overcurrent occurs, the MAX5952 sets the IVC bit in register R09h.

ICUT Register and High-Power Mode

ICUT Register

The ICUT register determines the maximum current limits allowed for each port of the MAX5952. The 3 ICUT bits (R2Ah[6:4], R2Ah[2:0], R2Bh[6:4], and R2Bh[2:0]) allow programming of the current-limit and overcurrent thresholds in excess of the IEEE standard limit (see Tables 34a, 34b, and 34c). The ICUT registers can be written to directly through the I^2C interface when CL_DISC (R17h[2]) is set to 0 (see Table 3). In this case, the current limit of the port is configured regardless of the status of the classification.

By setting the CL_DISC bit to 1, the MAX5952 automatically sets the ICUT register based upon the classification result of the port. See Table 3 and the *Register Map and Description* section.

Table 3. Automatic ICUT Programming

CL_DISC	PORT CLASSIFICATION RESULT	RESULTING ICUT REGISTER BITS
0	Any	User programmed
1	1	ICUT = 110
1	2	ICUT = 111
1	0, 3	ICUT = 000

High-Power, Quad, PSE Controller for Power-Over-Ethernet

High-Power Mode

When CL_DISC (R17h[2]) is set to 0, high-power mode is configured by setting the ICUT bits to any combination other than 000, 110, or 111 (note that 000 is the default value for the IEEE standard limit). See Table 3 and the *Register Map and Description* section.

Foldback Current

During startup and normal operation, an internal circuit senses the voltage at OUT_ and reduces the current-limit value when ($V_{OUT\_}$ - V_{EE}) > 28V. The foldback function helps to reduce the power dissipation on the FET. The current limit eventually reduces to 1/3 of I_{LIM} when ($V_{OUT\_}$ - V_{EE}) > 48V (see Figure 3a). For high-power mode, the foldback starts when ($V_{OUT\_}$ - V_{EE}) > 10V (see Figure 3b). In high-power mode, the current limit (I_{LIM}) is reduced up to 1/8 of its programmed value when ($V_{OUT\_}$ - V_{EE}) > 48V.

MOSFET Gate Driver

Connect the gate of the external n-channel MOSFET to GATE_. An internal 50µA current source pulls GATE_ to (V_{EE} + 10V) to turn on the MOSFET. An internal 40µA current source pulls down GATE_ to V_{EE} to turn off the MOSFET.

The pullup and pulldown current controls the maximum slew rate at the output during turn-on or turn-off. Use the following equation to set the maximum slew rate:

$$\frac{\Delta V_{OUT}}{\Delta t} = \frac{I_{GATE}}{C_{GD}}$$

where C_{GD} is the total capacitance between GATE and DRAIN of the external MOSFET. Current limit and the capacitive load at the drain control the slew rate during startup. During current-limit regulation, the MAX5952 manipulates the GATE_ voltage to control the voltage at SENSE_ (V_{RS}). A fast pulldown activates if V_{RS} overshoots the limit threshold (V_{SU_LIM}). The fast pulldown current increases with the amount of overshoot. The maximum fast pulldown current is 100mA.

During turn-off, when the GATE voltage reaches a value lower than 1.2V, a strong pulldown switch is activated to keep the MOSFET securely off.

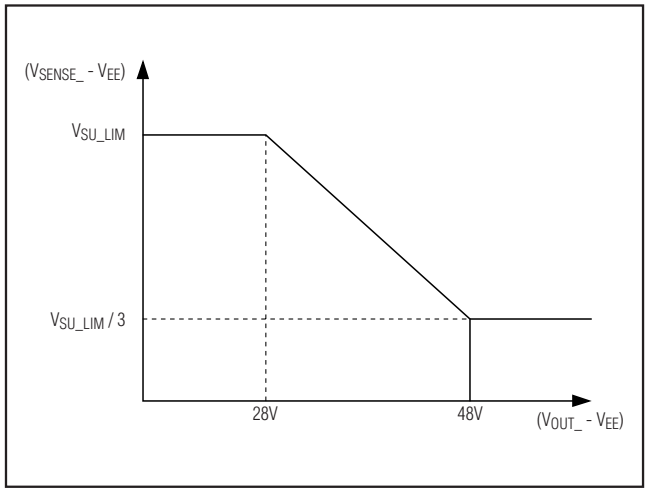


Figure 3a. Foldback Current Characteristics

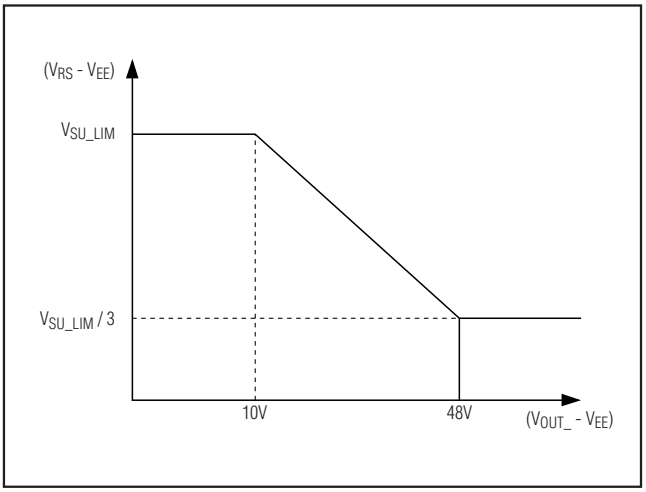


Figure 3b. Foldback Current Characteristics for High-Power Mode

Digital Logic

V_{DD} supplies power for the internal logic circuitry. V_{DD} ranges from +3.0V to +5.5V and determines the logic thresholds for the CMOS connections (SDAIN, SDAOUT, SCL, AUTO, $\overline{SHD\_}$, A_). This voltage range enables the MAX5952 to interface with a nonisolated low-voltage microcontroller. The MAX5952 checks the digital supply for compatibility with the internal logic. The MAX5952 also features a V_{DD} undervoltage lockout (V_{DDUVLO}) of +2.0V. A V_{DDUVLO} condition keeps the MAX5952 in reset and the ports shut off. Bit 0 in the supply event register shows the status of V_{DDUVLO} (Table 12) after V_{DD} has recovered. All logic inputs and outputs reference to DGND. DGND and AGND must be connected together externally. Connect DGND to AGND at a single point in the system as close as possible to the MAX5952.

Hardware Shutdown

$\overline{SHD\_}$ shuts down the respective ports without using the serial interface. Hardware shutdown offers an emergency turn-off feature that allows a fast disconnect of the power supply from the port. Pull $\overline{SHD\_}$ low to remove power. $\overline{SHD\_}$ also resets the corresponding events and status register bits.

Interrupt

The MAX5952 contains an open-drain logic output ($\overline{INT}$) that goes low when an interrupt condition exists. R00h and R01h (Tables 6 and 7) contain the definitions of the interrupt registers. The mask register R01h determines events that trigger an interrupt. As a response to an interrupt, the controller reads the status of the event register to determine the cause of the interrupt and takes subsequent actions. Each interrupt event register also contains a Clear on Read (CoR) register. Reading through the CoR register address clears the interrupt. $\overline{INT}$ remains low when reading the interrupt through the read-only addresses. For example, to clear a startup fault on the port 4 read address 09h (see Table 11). Use the global pushbutton bit in register 1Ah (bit 7, Table 23) to clear interrupts, or use a software or hardware reset.

Undervoltage and Overvoltage Protection

The MAX5952 contains several undervoltage and overvoltage protection features. Table 12 in the *Register Map and Description* section shows a detailed list of the undervoltage and overvoltage protection features. An internal V_{EE} undervoltage lockout (V_{EEUVLO}) circuit keeps the MOSFET off and the MAX5952 in reset until V_{AGND} - V_{EE} exceeds 29V for more than 3ms. An internal V_{EE} overvoltage (V_{EE_OV}) circuit shuts down the ports when (V_{AGND} - V_{EE}) exceeds 60V. The digital supply also contains an undervoltage lockout (V_{DDUVLO}). The MAX5952 also features three other undervoltage and overvoltage interrupts: V_{EE} undervoltage interrupt (V_{EEUV}), V_{DD} undervoltage interrupt (V_{DDUV}), and V_{DD} overvoltage interrupt (V_{DDOV}). A fault latches into the supply events register (Table 12), but the MAX5952 does not shut down the ports with V_{EEUV}, V_{DDUV}, or V_{DDOV}.

DC Disconnect Monitoring

Setting R13h[DCD_EN_] bits high enable DC load monitoring during a normal powered state. If V_{RS} (the voltage across R_S) falls below the DC load disconnect threshold, V_{DCTH}, for more than t_{DISC}, the device turns off power and asserts the LD_DISC_ bit of the corresponding port.

AC Disconnect Monitoring

The MAX5952 features AC load disconnect monitoring. Connect an external sine wave to OSC. The oscillator requirements are:

1) V_{P-P} x Frequency = 200V_{P-P} x Hz ±15%
2) Positive peak voltage > +2V
3) Frequency > 60Hz

A 100Hz ±10%, 2V_{P-P} ±5%, with +1.2V offset (V_{PEAK} = +2.2V typical) is recommended.

The MAX5952 buffers and amplifies 3x the external oscillator signal and sends the signal to DET_, where the sine wave is AC-coupled to the output. The MAX5952 senses the presence of the load by monitoring the amplitude of the AC current returned to DET_ (see the *Functional Diagram*).

Setting R13h[ACD_EN_] bits high enable AC load disconnect monitoring during a normal powered state. If the AC current peak at the DET_ input falls below I_{ACTH} for more than t_{DISC}, the device turns off power and asserts the LD_DISC_ bit of the corresponding port. I_{ACTH} is programmable using R23h[0-3].

An internal comparator checks for a proper amplitude of the oscillator input. If the positive peak of the input sinusoid falls below a safety value of 2V, OSC_FAIL sets and the port shuts down. Power cannot be applied to the ports when ACD_EN is set high and OSC_FAIL is set high. Leave OSC unconnected or connect it to DGND when not using AC-disconnect detection.

Thermal Shutdown

If the MAX5952 die temperature reaches +150°C, an overtemperature fault generates and the MAX5952 shuts down. The MOSFETs turn off. The die temperature of the MAX5952 must cool down below 130°C to remove the overtemperature fault condition. After a thermal shutdown, the part is reset.

High-Power, Quad, PSE Controller for Power-Over-Ethernet

Watchdog

R1Dh, R1Eh, and R1Fh registers control the watchdog operation. The watchdog function, when enabled, allows the MAX5952 to gracefully take over control or securely shuts down the power to the ports in case of software/firmware crashes. Contact the factory for more details.

Address Inputs

A3, A2, A1, and A0 represent the four LSBs of the chip address. The complete chip address is 7 bits (see Table 4).

Table 4. MAX5952 Address

0	1	0	A3	A2	A1	A0	R/$\overline{W}$

The four LSBs latch on the low-to-high transition of $\overline{RESET}$ or after a power-supply start (either on V_{DD} or V_{EE}). Address inputs default high through an internal 50kΩ pullup resistor to V_{DD}. The MAX5952 also responds to the call through a global address 30h (see the *Global Addressing and Alert Response Protocol* section).

I²C-Compatible Serial Interface

The MAX5952 operates as a slave that sends and receives data through an I²C-compatible, 2-wire or 3-wire interface. The interface uses a serial-data input line (SDAIN), a serial-data output line (SDAOUT), and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX5952, and generates the SCL clock that synchronizes the data transfer. In most applications, connect the SDAIN and the SDAOUT lines together to form the serial-data line (SDA).

Using the separate input and output data lines allows optocoupling with the controller bus when an isolated supply powers the microcontroller.

The MAX5952 SDAIN line operates as an input. The MAX5952 SDAOUT operates as an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDAOUT. The MAX5952 SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters, or if the master in a single-master system has an open-drain SCL output.

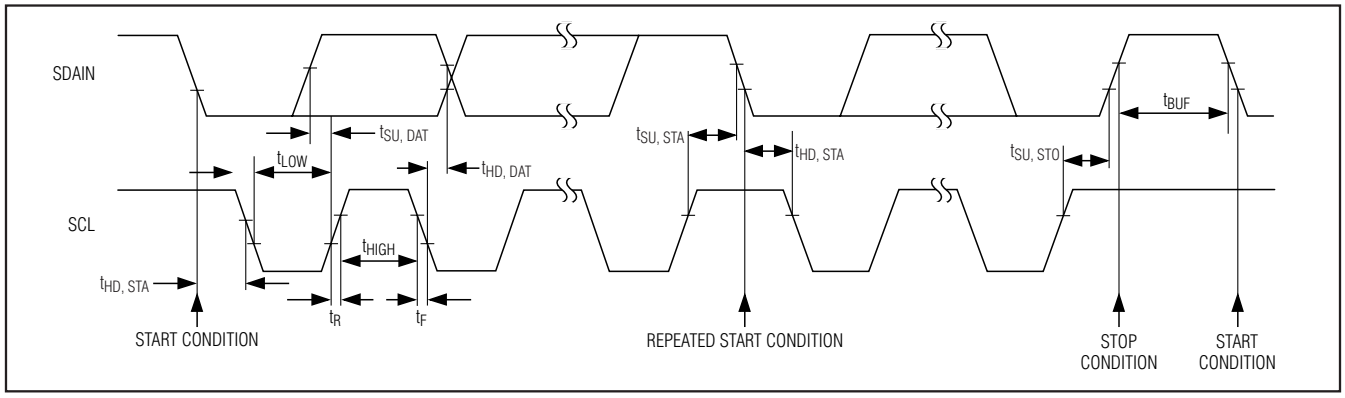


Figure 4. 2-Wire Serial Interface Timing Details

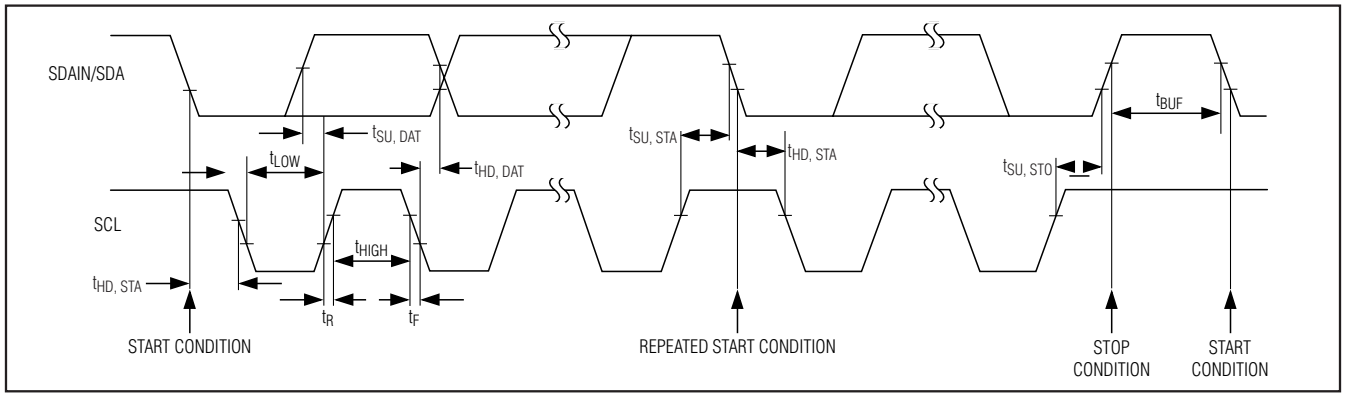


Figure 5. 3-Wire Serial Interface Timing Details

Serial Addressing

Each transmission consists of a START condition (Figure 6) sent by a master, followed by the MAX5952 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master finishes communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The STOP condition frees the bus for another transmission.

Bit Transfer

Each clock pulse transfers one data bit (Figure 7). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 8) that the recipient uses to handshake receipt of each byte of data. Thus each byte effectively transferred requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA (or the SDAOUT in the 3-wire interface) during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the clock pulse. When the master transmits to the MAX5952, the MAX5952 generates the acknowledge bit. When the MAX5952 transmits to the master, the master generates the acknowledge bit.

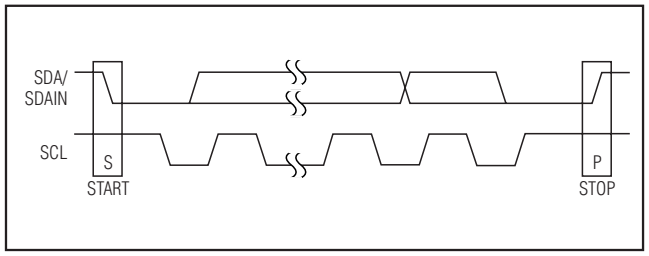


Figure 6. START and STOP Conditions

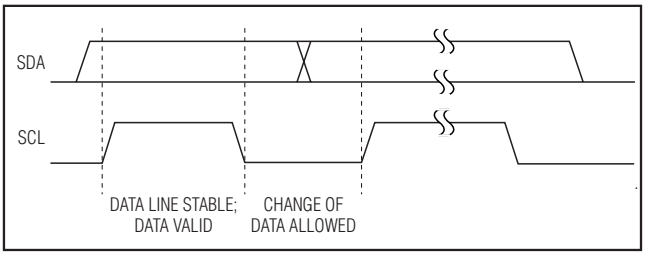


Figure 7. Bit Transfer

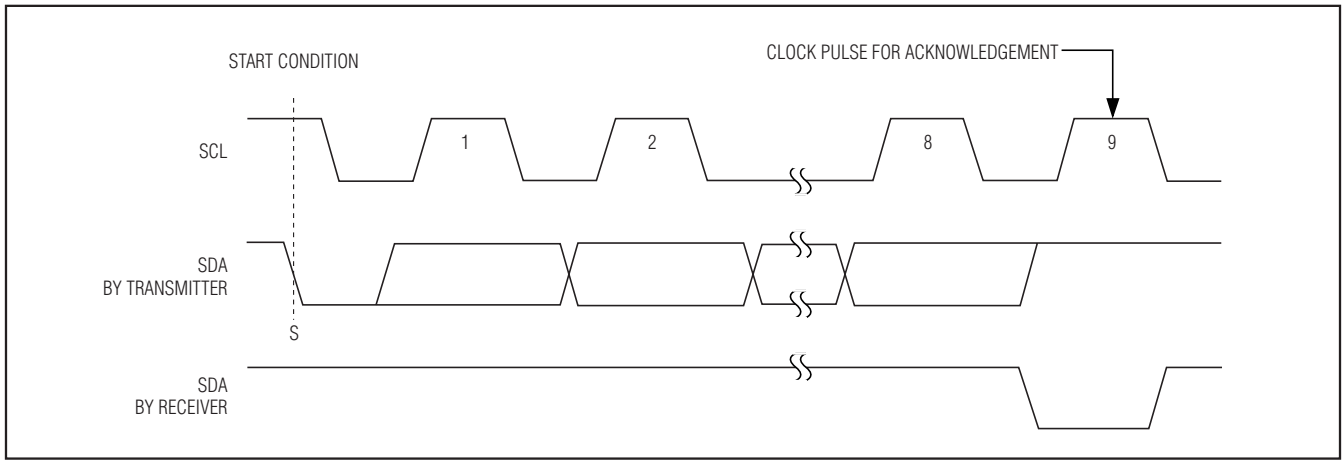


Figure 8. Acknowledge

High-Power, Quad, PSE Controller for Power-Over-Ethernet

Slave Address

The MAX5952 has a 7-bit long slave address (Figure 9). The bit following the 7-bit slave address (bit eight) is the R/$\overline{W}$ bit, which is low for a write command and high for a read command.

010 always represents the first three bits (MSBs) of the MAX5952 slave address. Slave address bits A3, A2, A1, and A0 represent the states of the MAX5952's A3, A2, A1, and A0 inputs, allowing up to sixteen MAX5952 devices to share the bus. The states of the A3, A2, A1 and A0 latch in upon the reset of the MAX5952 into register R11h. The MAX5952 monitors the bus continuously, waiting for a START condition followed by the MAX5952's slave address. When a MAX5952 recognizes its slave address, the MAX5952 acknowledges and is then ready for continued communication.

Global Addressing and Alert Response Protocol

The global address call is used in writing mode to write the same register to multiple devices (address 0x60). In read mode (address 0x61), the global address call is used as the alert response address. When responding to a global call, the MAX5952 puts out on the data line its own address whenever its interrupt is active. So does every other device connected to the SDAOUT line that has an active interrupt. After every bit transmitted, the MAX5952 checks that the data line effectively corresponds to the data it is delivering. If it is not, it then backs off and frees the data line. This litigation protocol always allows the part with the lowest address to complete the transmission. The microcontroller can then respond to the interrupt and take proper actions. The MAX5952 does not reset its own interrupt at the end of the alert response protocol. The microcontroller has to do it by clearing the event register through their CoR adresses or activating the CLR_INT pushbutton.

Message Format for Writing to the MAX5952

A write to the MAX5952 comprises of the MAX5952's slave address transmission with the R/$\overline{W}$ bit set to 0, followed by at least one byte of information. The first byte of information is the command byte (Figure 10). The command byte determines which register of the MAX5952 is written to by the next byte, if received. If the MAX5952 detects a STOP condition after receiving the command byte, the MAX5952 takes no further action beyond storing the command byte. Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX5952 selected by the command byte. If the MAX5952 transmits multiple data bytes before the MAX5952 detects a STOP condition, these bytes store in subsequent MAX5952 internal registers because the control byte address auto-increments.

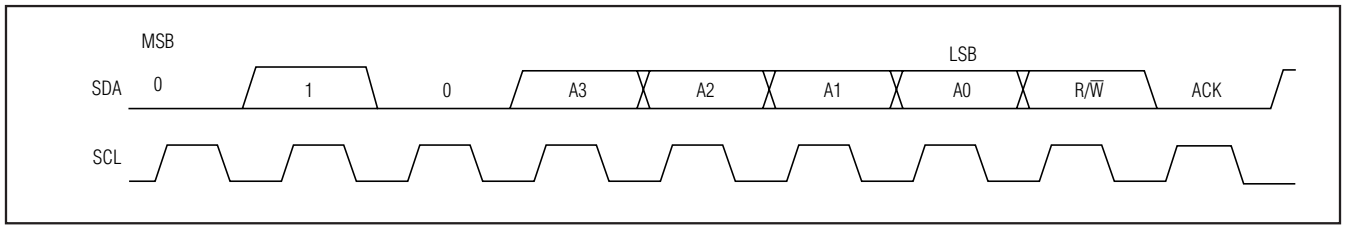


Figure 9. Slave Address

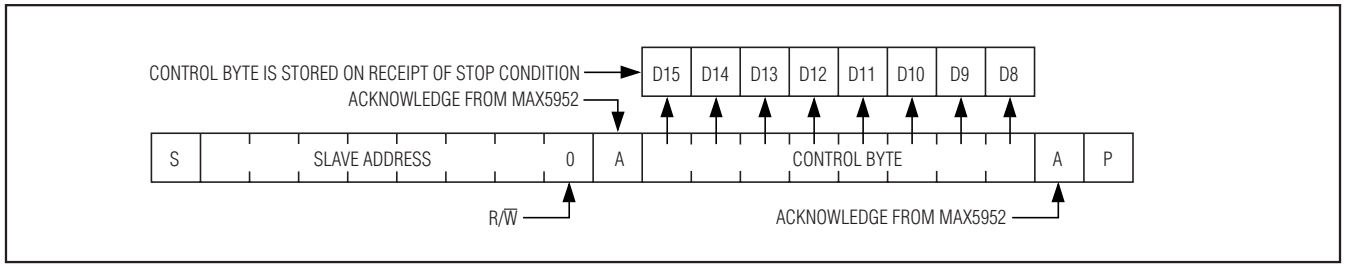


Figure 10. Control Byte Received

Message Format for Reading

The MAX5952 reads using the MAX5952's internally stored command byte as an address pointer, the same way the stored command byte is used as an address pointer for a write. The pointer auto-increments after reading each data byte using the same rules as for a write. Thus, a read is initiated by first configuring the MAX5952's command byte by performing a write (Figure 11). The master now reads 'n' consecutive bytes from the MAX5952, with the first data byte read from the register addressed by the initialized command byte (Figure 12). When performing read-after-write verification, remember to reset the command byte's address because the stored control byte address auto-increments after the write.

Operation with Multiple Masters

When the MAX5952 operates on a 2-wire interface with multiple masters, a master reading the MAX5952 should use repeated starts between the write which sets the MAX5952's address pointer, and the read(s) that take the data from the location(s). It is possible for master 2 to take over the bus after master 1 has set up the MAX5952's address pointer but before master 1 has read the data. If master 2 subsequently resets the MAX5952's address pointer then master 1's read may be from an unexpected location.

Command Address Auto-Incrementing

Address auto-incrementing allows the MAX5952 to be configured with fewer transmissions by minimizing the number of times the command address needs to be sent. The command address stored in the MAX5952 generally increments after each data byte is written or read (Table 5). The MAX5952 is designed to prevent overwrites on unavailable register addresses and unintentional wrap-around of addresses.

Table 5. Auto-Increment Rules

COMMAND BYTE ADDRESS RANGE	AUTO-INCREMENT BEHAVIOR
0x00 to 0x26	Command address auto-increments after byte read or written
0x26	Command address remains at 0x26 after byte written or read

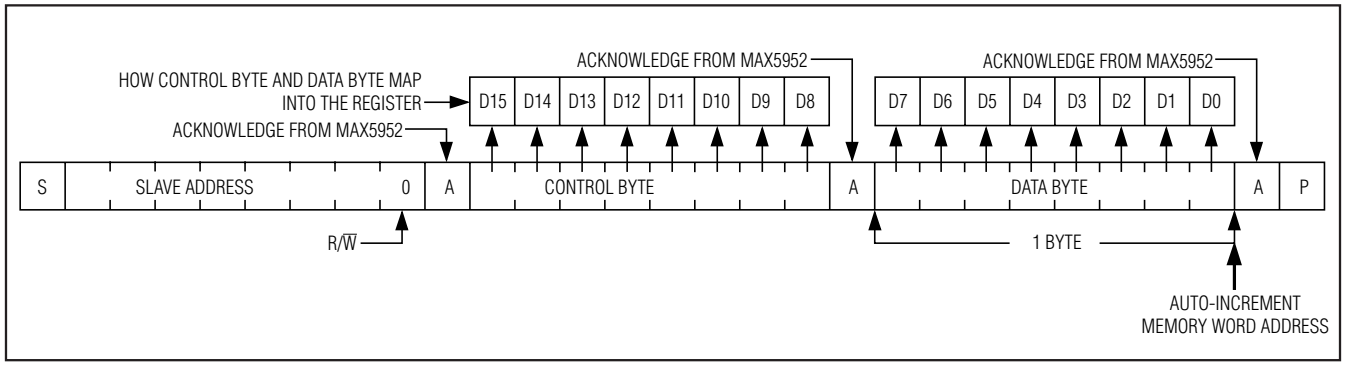


Figure 11. Control and Single Data Byte Received

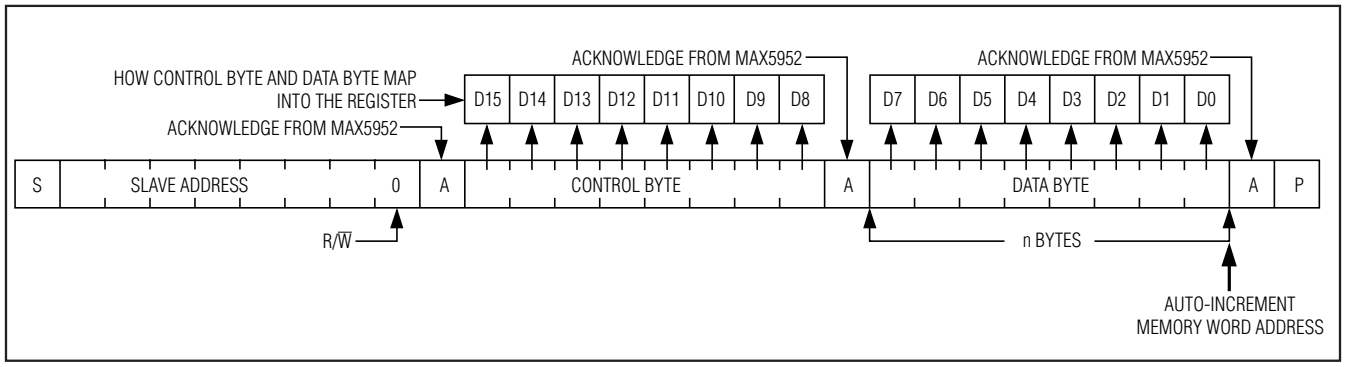


Figure 12. 'n' Data Bytes Received

High-Power, Quad, PSE Controller for Power-Over-Ethernet

Register Map and Description

The interrupt register (Table 6) summarizes the event register status and is used to send an interrupt signal ($\overline{INT}$ goes low) to the controller. Writing a 1 to R1Ah[7] clears all interrupt and events registers. A reset sets R00h to 00h.

INT_EN (R17h[7]) is a global interrupt mask (Table 7). The MASK_ bits activate the corresponding interrupt bits in register R00h. Writing a 0 to INT_EN (R17h[7]) disables the $\overline{INT}$ output.

A reset sets R01h to AAA00A00b where A is the state of the AUTO input prior to the reset.

Table 6. Interrupt Register

ADDRESS = 00h			DESCRIPTION
SYMBOL	BIT	R/W	
SUP_FLT	7	R	Interrupt signal for supply faults. SUP_FLT is the logic OR of all the bits [7:0] in register R0Ah/R0Bh (Table 12).
TSTR_FLT	6	R	Interrupt signal for startup failures. TSTR_FLT is the logic OR of bits [7:0] in register R08h/R09h (Table 11).
IMAX_FLT	5	R	Interrupt signal for current-limit violations. IMAX_FLT is the logic OR of bits [3:0] in register R06h/R07h (Table 10).
CL_END	4	R	Interrupt signal for completion of classification. CL_END is the logic OR of bits [7:4] in register R04h/R05h (Table 9).
DET_END	3	R	Interrupt signal for completion of detection. DET_END is the logic OR of bits [3:0] in register R04h/R05h (Table 9).
LD_DISC	2	R	Interrupt signal for load disconnection. LD_DISC is the logic OR of bits [7:4] in register R06h/R07h (Table 10).
PG_INT	1	R	Interrupt signal for PGOOD status change. PG_INT is the logic OR of bits [7:4] in register R02h/R03h (Table 8).
PE_INT	0	R	Interrupt signal for power-enable status change. PEN_INT is the logic OR of bits [3:0] in register R02h/R03h (Table 8).

Table 7. Interrupt Mask Register

ADDRESS = 01h			DESCRIPTION
SYMBOL	BIT	R/W	
MASK7	7	R/W	Interrupt mask bit 7. A logic-high enables the SUP_FLT interrupts. A logic-low disables the SUP_FLT interrupts.
MASK6	6	R/W	Interrupt mask bit 6. A logic-high enables the TSTR_FLT interrupts. A logic-low disables the TSTR_FLT interrupts.
MASK5	5	R/W	Interrupt mask bit 5. A logic-high enables the IMAX_FLT interrupts. A logic-low disables the IMAX_FLT interrupts.
MASK4	4	R/W	Interrupt mask bit 4. A logic-high enables the CL_END interrupts. A logic-low disables the CL_END interrupts.
MASK3	3	R/W	Interrupt mask bit 3. A logic-high enables the DET_END interrupts. A logic-low disables the DET_END interrupts.
MASK2	2	R/W	Interrupt mask bit 2. A logic-high enables the LD_DISC interrupts. A logic-low disables the LD_DISC interrupts.
MASK1	1	R/W	Interrupt mask bit 1. A logic-high enables the PG_INT interrupts. A logic-low disables the PG_INT interrupts.
MASK0	0	R/W	Interrupt mask bit 0. A logic-high enables the PEN_INT interrupts. A logic-low disables the PEN_INT interrupts.

The power event register (Table 8) records changes in the power status of the four ports. Any change in PGOOD_ (R10h[7:4]) sets PG_CHG_ to 1. Any change in the PWR_EN_ (R10h[3:0]) sets PWEN_CHG_ to 1. PG_CHG_ and PWEN_CHG_ trigger on the edges of PGOOD_ and PWR_EN_ and do not depend on the actual level of the bits. The power event register has two addresses. When read through the R02h address, the content of the register is left unchanged. When read through the CoR R03h address, the register content is cleared. A reset sets R02h/R03h = 00h.

Table 8. Power Event Register

ADDRESS =		02h	03h	DESCRIPTION
SYMBOL	BIT	R/W	R/W	
PG_CHG4	7	R	CoR	PGOOD change event for port 4
PG_CHG3	6	R	CoR	PGOOD change event for port 3
PG_CHG2	5	R	CoR	PGOOD change event for port 2
PG_CHG1	4	R	CoR	PGOOD change event for port 1
PWEN_CHG4	3	R	CoR	Power enable change event for port 4
PWEN_CHG3	2	R	CoR	Power enable change event for port 3
PWEN_CHG2	1	R	CoR	Power enable change event for port 2
PWEN_CHG1	0	R	CoR	Power enable change event for port 1

DET_END_/CL_END_ is set high whenever detection/classification is completed on the corresponding port. A 1 in any of the CL_END_ bits forces R00h[4] to 1. A 1 in any of the DET_END_ bits forces R00h[3] to 1. As with any of the other events register, the detect event register has two addresses. When read through the R04h address, the content of the register is left unchanged. When read through the CoR R05h address, the register content is cleared. A reset sets R04h/R05h = 00h.

Table 9. Detect Event Register

ADDRESS =		04h	05h	DESCRIPTION
SYMBOL	BIT	R/W	R/W	
CL_END4	7	R	CoR	Classification completed on port 4
CL_END3	6	R	CoR	Classification completed on port 3
CL_END2	5	R	CoR	Classification completed on port 2
CL_END1	4	R	CoR	Classification completed on port 1
DET_END4	3	R	CoR	Detection completed on port 4
DET_END3	2	R	CoR	Detection completed on port 3
DET_END2	1	R	CoR	Detection completed on port 2
DET_END1	0	R	CoR	Detection completed on port 1

LD_DISC_ is set high whenever the corresponding port shuts down due to detection of load removal. IMAX_FLT_ is set high when the port shuts down due to an extended overcurrent event after a successful start-up. A 1 in any of the LD_DISC_ bits forces R00h[2] to 1. A 1 in any of the IMAX_FLT_ bits forces R00h[5] to 1.

As with any of the other events register, the fault event register has two addresses. When read through the R06h address, the content of the register is left unchanged. When read through the CoR R07h address, the register content is cleared. A reset sets R06h/R07h = 00h.

Table 10. Fault Event Register

ADDRESS =		06h	07h	DESCRIPTION
SYMBOL	BIT	R/W	R/W	
LD_DISC4	7	R	CoR	Disconnect on port 4
LD_DISC3	6	R	CoR	Disconnect on port 3
LD_DISC2	5	R	CoR	Disconnect on port 2
LD_DISC1	4	R	CoR	Disconnect on port 1
IMAX_FLT4	3	R	CoR	Overcurrent on port 4
IMAX_FLT3	2	R	CoR	Overcurrent on port 3
IMAX_FLT2	1	R	CoR	Overcurrent on port 2
IMAX_FLT1	0	R	CoR	Overcurrent on port 1

If the port remains in current limit or the PGOOD condition is not met at the end of the startup period, the port shuts down and the corresponding STRT_FLT_ is set to 1. A 1 in any of the STRT_FLT_ bits forces R00h[6] to 1. IVC_ is set to 1 whenever the port current exceeds the maximum allowed limit for the class (determined during the classification process). A 1 in any of IVC_ forces R00h[6] to 1. When the CL_DISC (R17h[2]) is set to 1, the port also limits the load current according to its class as specified in the *Electrical Characteristics* table. As with any of the other events register, the start-up event register has two addresses. When read through the R08h address, the content of the register is left unchanged. When read through the CoR R09h address, the register content is cleared. A reset sets R08h/R09h = 00h.

Table 11. Startup Event Register

ADDRESS =		08h	09h	DESCRIPTION
SYMBOL	BIT	R/W	R/W	
IVC4	7	R	CoR	Class overcurrent flag for port 4
IVC3	6	R	CoR	Class overcurrent flag for port 3
IVC2	5	R	CoR	Class overcurrent flag for port 2
IVC1	4	R	CoR	Class overcurrent flag for port 1
STRT_FLT4	3	R	CoR	Startup failed on port 4
STRT_FLT3	2	R	CoR	Startup failed on port 3
STRT_FLT2	1	R	CoR	Startup failed on port 2
STRT_FLT1	0	R	CoR	Startup failed on port 1

The MAX5952 continuously monitors the power supplies and sets the appropriate bits in the supply event register (Table 12). V_{DD_OV}/V_{EE_OV} is set to 1 whenever V_{DD}/V_{EE} exceeds its overvoltage threshold. V_{DD_UV}/V_{EE_UV} is set to 1 whenever V_{DD}/V_{EE} falls below its undervoltage threshold.

OSC_FAIL is set to 1 whenever the amplitude of the oscillator signal at the OSC_ input falls below a level that might compromise the AC disconnect detection function. OSC_FAIL generates an interrupt only if at least one of the ACD_EN (R13h[7:4]) bits is set high.

A thermal shutdown circuit monitors the temperature of the die and resets the MAX5952 if the temperature exceeds +150°C. TSD is set to 1 after the MAX5952 returns to normal operation. TSD is also set to 1 after every UVLO reset.

When V_{DD} and/or $|V_{EE}|$ is below its UVLO threshold, the MAX5952 is in reset mode and securely holds all ports off. When V_{DD} and $|V_{EE}|$ rise to above their respective UVLO thresholds, the device comes out of reset as soon as the last supply crosses the UVLO threshold. The last supply corresponding UV and UVLO bits in the supply event register is set to 1.

A 1 in any supply event register's bits forces R00h[7] to 1. As with any of the other events register, the supply event register has two addresses. When read through the R0Ah address, the content of the register is left unchanged. When read through the CoR R0Bh address, the register content is cleared. A reset sets R0Ah/R0Bh to 10100001b if V_{DD} comes up after V_{EE} or to 10010100b if V_{EE} comes up after V_{DD}.

Table 12. Supply Event Register

ADDRESS =		0Ah	0Bh	DESCRIPTION
SYMBOL	BIT	R/W	R/W	
TSD	7	R	CoR	Overtemperature shutdown
V_{DD_OV}	6	R	CoR	V_{DD} overvoltage condition
V_{DD_UV}	5	R	CoR	V_{DD} undervoltage condition
V_{EE_UVLO}	4	R	CoR	V_{EE} undervoltage lockout condition
V_{EE_OV}	3	R	CoR	V_{EE} overvoltage condition
V_{EE_UV}	2	R	CoR	V_{EE} undervoltage condition
OSC_FAIL	1	R	CoR	Oscillator amplitude is below limit
V_{DD_UVLO}	0	R	CoR	V_{DD} undervoltage lockout condition

High-Power, Quad, PSE Controller for Power-Over-Ethernet

The port status register (Table 13a) records the results of the detection and classification at the end of each phase in three encoding bits each. R0Ch contains the detection and classification status of port 1. R0Dh corresponds to port 2, R0Eh corresponds to port 3, and R0Fh corresponds to port 4. Tables 13b and 13c show the detection/classification result decoding charts, respectively. For CLC_EN = 0, the detection result is shown in Table 13b. When CLC_EN is set high, the MAX5952 allows valid detection of high capacitive load of up to 100µF.

When ping-pong classification is not enabled (ENx_CL6 = 0), the classification status is reported in Table 13c. When ping-pong classification is enabled (ENx_CL6 = 1), the CLASS_[2:0] bits are set to 000 and the classification result is reported in locations R2Ch–R2Fh.

As a protection, when POFF_CL (R17h[3], Table 21) is set to 1, the MAX5952 prohibits turning on power to the port that returns a status 111 after classification. A reset sets 0Ch, 0Dh, 0Eh, and 0Fh = 00h.

Table 13a. Port Status Registers

ADDRESS = 0Ch, 0Dh, 0Eh, 0Fh			DESCRIPTION
SYMBOL	BIT	R/W	
Reserved	7	R	Reserved
CLASS_	6	R	CLASS_[2]
	5	R	CLASS_[1]
	4	R	CLASS_[0]
Reserved	3	R	Reserved
DET_ST_	2	R	DET_[2]
	1	R	DET_[1]
	0	R	DET_[0]

Table 13b. Detection Result Decoding Chart

DET_ST_[2:0] (ADDRESS = 0Ch, 0Dh, 0Eh, 0Fh)	DETECTED	DESCRIPTION
000	None	Detection status unknown
001	DCP	Positive DC supply connected at the port (AGND - $V_{OUT\_}$ < 1V)
010	HIGH CAP	High capacitance at the port (> 8.5µF)
011	RLOW	Low resistance at the port, R_{PD} < 15kΩ
100	DET_OK	Detection pass, 15kΩ > R_{PD} > 33kΩ
101	RHIGH	High resistance at the port, R_{PD} > 33kΩ
110	OPEN0	Open port (I < 10µA)
111	DCN	Negative DC supply connected to the port (V_{OUT} - V_{EE} < 2V)

Table 13c. Classification Result Decoding Chart

CLASS_[2:0] (ADDRESS = 0Ch, 0Dh, 0Eh, 0Fh)	CLASS RESULT
000	Unknown
001	1
010	2
011	3
100	4
101	5
110	0
111	Current limit (> I_{CILIM})

PGOOD_ is set to 1 (Table 14) at the end of the power-up startup period if the power-good condition is met (0 < (V_{OUT} - V_{EE}) < PG_{TH}). The power-good condition must remain valid for more than t_{PGOOD} to assert PGOOD_. PGOOD_ is reset to 0 whenever the output falls out of the power-good condition. A fault condition immediately forces PGOOD_ low.

PWR_EN_ is set to 1 when the port power is turned on. PWR_EN resets to 0 as soon as the port turns off. Any transition of PGOOD_ and PWR_EN_ bits set the corresponding bit in the power event registers R02h/R03h (Table 8). A reset sets R10h = 00h.

Table 14. Power Status Register

ADDRESS = 10h			DESCRIPTION
SYMBOL	BIT	R/W	
PGOOD4	7	R	Power-good condition on port 4
PGOOD3	6	R	Power-good condition on port 3
PGOOD2	5	R	Power-good condition on port 2
PGOOD1	4	R	Power-good condition on port 1
PWR_EN4	3	R	Power is enabled on port 4
PWR_EN3	2	R	Power is enabled on port 3
PWR_EN2	1	R	Power is enabled on port 2
PWR_EN1	0	R	Power is enabled on port 1

A3, A2, A1, A0 (Table 15) represent the four LSBs of the MAX5952 address (Table 4). During a reset, the device latches into R11h. These four bits address from the corresponding inputs as well as the state of the MIDSPAN and AUTO inputs. Changes to those inputs during normal operation are ignored.

Table 15. Address Input Status Register

ADDRESS = 11h			DESCRIPTION
SYMBOL	BIT	R/W	
Reserved	7	R	Reserved
Reserved	6	R	Reserved
A3	5	R	Device address, A3 pin latched-in status
A2	4	R	Device address, A2 pin latched-in status
A1	3	R	Device address, A1 pin latched-in status
A0	2	R	Device address, A0 pin latched-in status
MIDSPAN	1	R	MIDSPAN input's latched-in status
AUTO	0	R	AUTO input's latched-in status

High-Power, Quad, PSE Controller for Power-Over-Ethernet

The MAX5952 uses two bits for each port to set the mode of operation. Set the modes according to Table 16a.

A reset sets R12h = AAAAAAAA where A represents the latched-in state of the AUTO input prior to the reset.

Use software to change the mode of operation. Software resets of ports (RESET_P_ bit, Table 23) do not affect the mode register.

Table 16. Mode Register

ADDRESS = 12h			DESCRIPTION
SYMBOL	BIT	R/W	
P4_M1	7	R/W	MODE[1] for port 4
P4_M0	6	R/W	MODE[0] for port 4
P3_M1	5	R/W	MODE[1] for port 3
P3_M0	4	R/W	MODE[0] for port 3
P2_M1	3	R/W	MODE[1] for port 2
P2_M0	2	R/W	MODE[0] for port 2
P1_M1	1	R/W	MODE[1] for port 1
P1_M0	0	R/W	MODE[0] for port 1

Table 16a. Mode Status

MODE	DESCRIPTION
00	Shutdown
01	Manual
10	Semi-auto
11	Auto

Setting DCD_EN_ to 1 enables the DC load disconnect detection feature (Table 17). Setting ACD_EN_ to 1 enables the AC load disconnect feature. If enabled, the load disconnect detection starts during power mode and after startup when the corresponding PGOOD_ bit in register R10h (Table 14) goes high. A reset sets R13h = 0000AAAA where A represents the latched-in state of the AUTO input prior to the reset.

Table 17. Load Disconnect Detection Enable Register

ADDRESS = 13h			DESCRIPTION
SYMBOL	BIT	R/W	
ACD_EN4	7	R/W	Enable AC disconnect detection on port 4
ACD_EN3	6	R/W	Enable AC disconnect detection on port 3
ACD_EN2	5	R/W	Enable AC disconnect detection on port 2
ACD_EN1	4	R/W	Enable AC disconnect detection on port 1
DCD_EN4	3	R/W	Enable DC disconnect detection on port 4
DCD_EN3	2	R/W	Enable DC disconnect detection on port 3
DCD_EN2	1	R/W	Enable DC disconnect detection on port 2
DCD_EN1	0	R/W	Enable DC disconnect detection on port 1

Setting DET_EN_/CLASS_EN_ to 1 (Table 18) enables load detection/classification, respectively. Detection always has priority over classification. To perform classification without detection, set the DET_EN_ bit low and CLASS_EN_ bit high.

In manual mode, R14h works like a pushbutton. Set the bits high to begin the corresponding routine. The bit clears after the routine finishes.

When entering auto mode, R14h defaults to FFh. When entering semi or manual modes, R14h defaults to 00h. A reset or power-up sets R14h = AAAAAAAAb where A represents the latched-in state of the AUTO input prior to the reset.

Table 18. Detection and Classification Enable Register

ADDRESS = 14h			DESCRIPTION
SYMBOL	BIT	R/W	
CLASS_EN4	7	R/W	Enable classification on port 4
CLASS_EN3	6	R/W	Enable classification on port 3
CLASS_EN4	5	R/W	Enable classification on port 2
CLASS_EN3	4	R/W	Enable classification on port 1
DET_EN4	3	R/W	Enable detection on port 4
DET_EN3	2	R/W	Enable detection on port 3
DET_EN2	1	R/W	Enable detection on port 2
DET_EN1	0	R/W	Enable detection on port 1

CL_DISC (R17h[2]) and ENx_CL6 (R1Ch[7:4]) are used to program the high-power mode. See Table 3 for details.

Setting BCKOFF_ to 1 (Table 19) enables cadence timing on each port where the port backs off and waits 2.2s after each failed load discovery detection. The IEEE 802.3af standard requires a PSE that delivers power through the spare pairs (midspan PSE) to have cadence timing.

A reset or power-up sets R15h = 0000XXXXb where 'X' is the logic AND of the MIDSPAN and AUTO inputs.

Table 19. Backoff and High-Power Enable Register

ADDRESS = 15h			DESCRIPTION
SYMBOL	BIT	R/W	
BCKOFF4	3	R/W	Enable cadence timing on port 4
BCKOFF3	2	R/W	Enable cadence timing on port 3
BCKOFF2	1	R/W	Enable cadence timing on port 2
BCKOFF1	0	R/W	Enable cadence timing on port 1

High-Power, Quad, PSE Controller for Power-Over-Ethernet

TSTART[1,0] (Table 20a) programs the startup timers. Startup time is the time the port is allowed to be in current limit during startup. TFAULT[1,0] programs the fault time. Fault time is the time allowed for the port to be in current limit during normal operation. RSTR[1,0] programs the discharge rate of the TFAULT_ counter and effectively sets the time the port remains off after an overcurrent fault. TDISC[1,0] programs the load disconnect detection time. The device turns off power to the port if it fails to provide a minimum power maintenance signal for longer than the load disconnect detection time (TDISC).

Set the bits in R16h to scale the t_{START}, t_{FAULT}, and t_{DISC} to a multiple of their nominal value specified in the *Electrical Characteristics* table.

When the MAX5952 shuts down a port due to an extended overcurrent condition (either during startup or normal operation), if RSTR_EN is set high, the part does not allow the port to power back on before the restart timer (Table 20b) returns to zero. This effectively sets a minimum duty cycle that protects the external MOSFET from overheating during a prolonged output overcurrent conditions. A reset sets R16h = 00h.

Table 20a. Timing Register

ADDRESS = 16h			DESCRIPTION
SYMBOL	BIT	R/W	
RSTR[1]	7	R/W	Restart timer programming bit 1
RSTR[0]	6	R/W	Restart timer programming bit 0
TSTART[1]	5	R/W	Startup timer programming bit 1
TSTART[0]	4	R/W	Startup timer programming bit 0
TFAULT[1]	3	R/W	Overcurrent timer programming bit 1
TFAULT[0]	2	R/W	Overcurrent timer programming bit 0
TDISC[1]	1	R/W	Load disconnect timer programming bit 1
TDISC[0]	0	R/W	Load disconnect timer programming bit 0

Table 20b. Startup, Fault, and Load Disconnect Timer Values for Timing Register

BIT [1:0] (ADDRESS = 16h)	RSTR	t_{DISC}	t_{START}	t_{FAULT}
00	16 x t_{FAULT}	t_{DISC} nominal (350ms, typ)	t_{START} nominal (60ms, typ)	t_{FAULT} nominal (60ms, typ)
01	32 x t_{FAULT}	$^1/_4$ x t_{DISC} nominal	$^1/_2$ x t_{START} nominal	$^1/_2$ x t_{FAULT} nominal
10	64 x t_{FAULT}	$^1/_2$ x t_{DISC} nominal	2 x t_{START} nominal	2 x t_{FAULT} nominal
11	0 x t_{FAULT}	2 x t_{DISC} nominal	4 x t_{START} nominal	4 x t_{FAULT} nominal

Setting CL_DISC to 1 (Table 21) enables port over class current protection, where MAX5952 scales down the overcurrent limit (V_{FLT_LIM}) according to the port classification status. This feature provides protection to the system against PDs that violate their maximum class current allowance.

The higher current setting is enabled only after a successful startup so that the PD powers up as a normal 15W device.

CL_DISC, together with EN_HP_CL_ (R15h[6:4]), EN_HP_ALL (R15h[7]), and ENx_CL6 (R1Ch[7:4]) are used to program the high-power mode. See Table 3 for details.

Setting OUT_ISO high (Table 21), forces DET_ to a high-impedance state.

A reset sets R17h = 0xC0.

Table 21. Miscellaneous Configurations 1

ADDRESS = 17h			DESCRIPTION
SYMBOL	BIT	R/W	
INT_EN	7	R/W	A logic-high enables $\overline{INT}$ functionality
RSTR_EN	6	R	A logic-high enables the autorestart protection time off (as set by the RSTR[1:0] bits)
Reserved	5	R	Reserved
Reserved	4	R	Reserved
POFF_CL	3	R	A logic-high prevents power-up after a classification failure (I > 50mA, valid only in AUTO mode)
CL_DISC	2	R/W	A logic-high enables reduced current-limit voltage threshold (V_{FLT_LIM}) according to port
OUT_ISO	1	R/W	Forces DET_ to high impedance. Does not interfere with other circuit operation.

Power-enable pushbutton for semi and manual modes is found in Table 22. Setting PWR_ON_ to 1 turns on power to the corresponding port. Setting PWR_OFF_ to 1 turns off power to the port. PWR_ON_ is ignored when the port is already powered and during shutdown. PWR_OFF_ is ignored when the port is already off and during shutdown. After execution, the bits reset to 0. During detection or classification, if PWR_ON_ goes high, the MAX5952 gracefully terminates the current operation and turns on power to the port. The MAX5952 ignores the PWR_ON_ in auto mode. A reset sets R19h = 00h.

Table 22. Power-Enable Pushbuttons

ADDRESS = 19h			DESCRIPTION
SYMBOL	BIT	R/W	
PWR_OFF4	7	W	A logic-high powers off port 4
PWR_OFF3	6	W	A logic-high powers off port 3
PWR_OFF2	5	W	A logic-high powers off port 2
PWR_OFF1	4	W	A logic-high powers off port 1
PWR_ON4	3	W	A logic-high powers on port 4
PWR_ON3	2	W	A logic-high powers on port 3
PWR_ON2	1	W	A logic-high powers on port 2
PWR_ON1	0	W	A logic-high powers on port 1

High-Power, Quad, PSE Controller for Power-Over-Ethernet

Writing a 1 to CLR_INT (Table 23) clears all the event registers and the corresponding interrupt bits in register R00h. Writing a 1 to RESET_P_ turns off power to the corresponding port and resets only the status and event registers of that port. After execution, the bits reset to 0. Writing a 1 to RESET_IC causes a global software reset, after which the register map is set back to its reset state. A reset sets R1Ah = 00h.

Table 23. Global Pushbuttons

ADDRESS = 1Ah			DESCRIPTION
SYMBOL	BIT	R/W	
CLR_INT	7	W	A logic-high clears all interrupts
Reserved	6		Reserved
Reserved	5		Reserved
RESET_IC	4	W	A logic-high resets the MAX5952
RESET_P4	3	W	A logic-high softly resets port 4
RESET_P3	2	W	A logic-high softly resets port 3
RESET_P2	1	W	A logic-high softly resets port 2
RESET_P1	0	W	A logic-high softly resets port 1

The ID register (Table 24) keeps track of the device ID number and revision. The MAX5952's ID_CODE[4:0] = 11000b. Contact the factory for REV[2:0] value.

Table 24. ID Register

ADDRESS = 1Bh			DESCRIPTION
SYMBOL	BIT	R/W	
ID_CODE	7	R	ID_CODE[4]
	6	R	ID_CODE[3]
	5	R	ID_CODE[2]
	4	R	ID_CODE[1]
	3	R	ID_CODE[0]
REV	2	R	REV [2]
	1	R	REV [1]
	0	R	REV [0]

Enable the SMODE function (Table 25) by setting EN_WHDOG (R1Fh[7]) to 1. SMODE_ bit goes high when the watchdog counter reaches zero and the port(s) switch over to hardware-controlled mode. SMODE_ also goes high each and every time the software tries to power on a port, but is denied since the port is in hardware mode. A reset sets R1Ch = 00h.

Table 25. SMODE Enable Register

ADDRESS = 1Ch			DESCRIPTION
SYMBOL	BIT	CoR	
SMODE4	3	CoR	Port 4 hardware control flag
SMODE3	2	CoR	Port 3 hardware control flag
SMODE2	1	CoR	Port 2 hardware control flag
SMODE1	0	CoR	Port 1 hardware control flag

Set EN_WHDOG (R1Fh[7]) to 1 to enable the watchdog function. When activated, the watchdog timer counter, WDTIME[7:0], continuously decrements toward zero once every 164ms. Once the counter reaches zero (also called watchdog expiry), the MAX5952 enters hardware-controlled mode and each port shifts to a mode set by the HWMODE_ bit in register R1Fh (Table 27). Use software to set WDTIME (Table 26) and continuously set this register to some nonzero value before the register reaches zero to prevent a watchdog expiry. In this way, the software gracefully manages the power to ports upon a system crash or switchover.

While in hardware-controlled mode, the MAX5952 ignores all requests to turn the power on and the flag SMODE_ indicates that the hardware has taken control of the MAX5952 operation. In addition, the software is not allowed to change the mode of operation in hardware-controlled mode. A reset sets R1Eh = 00h.

Table 26. Watchdog Register

ADDRESS = 1Eh			DESCRIPTION
SYMBOL	BIT	R/W	
WDTIME	7	R/W	WDTIME[7]
	6	R/W	WDTIME[6]
	5	R/W	WDTIME[5]
	4	R/W	WDTIME[4]
	3	R/W	WDTIME[3]
	2	R/W	WDTIME[2]
	1	R/W	WDTIME[1]
	0	R/W	WDTIME[0]

Setting EN_WHDOG (Table 27) high activates the watchdog counter. When the counter reaches zero, the port switches to the hardware-controlled mode determined by the corresponding HWMODE_ bit. A low in HWMODE_ switches the port into shutdown by setting the bits in register R12h to 00. A high in HWMODE_ switches the port into auto mode by setting the bits in register R12h to 11. If WD_INT_EN is set, an interrupt is sent if any of the SMODE bits are set. A reset sets R1Fh = 00h.

Table 27. Switch Mode Register

ADDRESS = 1Fh			DESCRIPTION
SYMBOL	BIT	R/W	
EN_WHDOG	7	R/W	A logic-high enables the watchdog function
WD_INT_EN	6	R/W	Enables interrupt on SMODE_ bits
Reserved	5	—	Reserved
Reserved	4	R/W	Reserved
HWMODE4	3	R/W	Port 4 switches to AUTO if logic-high and to SHUTDOWN if logic-low when watchdog timer expires
HWMODE3	2	R/W	Port 3 switches to AUTO if logic-high and to SHUTDOWN if logic-low when watchdog timer expires
HWMODE2	1	R/W	Port 2 switches to AUTO if logic-high and to SHUTDOWN if logic-low when watchdog timer expires
HWMODE1	0	R/W	Port 1 switches to AUTO if logic-high and to SHUTDOWN if logic-low when watchdog timer expires

The CLC_EN enables the large capacitor detection feature. When CLC_EN is set the device can recognize a capacitor load up to 100µF. If the CLC_EN is reset, the MAX5952 performs normal detection.

AC_TH allows programming of the threshold of the AC disconnect comparator. The threshold is defined as a current since the comparators verify that the peak of the current pulses sensed at the DET_ input exceed a preset threshold. The current threshold is defined as follows:

$$IAC\_TH = 226.68\mu A + 28.33 \times NAC\_TH$$

where NAC_TH is the decimal value of AC_TH.

When set low, DET_BY inhibits port power-on if the discovery detection was bypassed in auto mode. When set high, DET_BY allows the device to turn on power to a non-IEEE 802.3af load without doing detection. If OSCF_RS is set high, the OSC_FAIL bit is ignored. A reset or power-up sets R23h = 04h. Default IAC_TH is 340µA.

Table 28. Program Register

ADDRESS = 23h			DESCRIPTION
SYMBOL	BIT	R/W	
Reserved	7	—	Reserved
Reserved	6	—	Reserved
CLC_EN	5	R/W	Large capacitor detection enable
DET_BY	4	R/W	Enables skipping detection in AUTO mode
OSCF_RS	3	R/W	OSC_FAIL reset bit
AC_TH	2	R/W	AC_TH[2]
	1	R/W	AC_TH[1]
	0	R/W	AC_TH[0]

Table 29. High-Power Mode Register

ADDRESS = 24h			DESCRIPTION
SYMBOL	BIT	R/W	
Reserved	7	—	Reserved
	3	—	Reserved
	2	—	Reserved
	1	—	Reserved
	0	—	Reserved

Table 30. Reserved

ADDRESS = 25h			DESCRIPTION
SYMBOL	BIT	R/W	
Reserved	7	—	Reserved
	6	—	Reserved
	5	—	Reserved
	4	—	Reserved
	3	—	Reserved
	2	—	Reserved
	1	—	Reserved
	0	—	Reserved

Table 31. Reserved

ADDRESS = 26h			DESCRIPTION
SYMBOL	BIT	R/W	
Reserved	7	—	Reserved
	6	—	Reserved
	5	—	Reserved
	4	—	Reserved
	3	—	Reserved
	2	—	Reserved
	1	—	Reserved
	0	—	Reserved

The IVEE bits enable the current-limit scaling (Table 32). This feature is used to reduce the current limit for systems running at higher voltage to maintain the desired output power. Table 33 sets the current-limit scaling register. A reset or power-up sets R29h = 00h.

Table 32. Miscellaneous Configurations 2

ADDRESS = 29h			DESCRIPTION
SYMBOL	BIT	R/W	
Reserved	7	—	Reserved
	6	—	Reserved
	5	—	Reserved
	4	—	Reserved
	3	—	Reserved
	2	—	Reserved
IVEE	1	R/W	IVEE[1]
	0	R/W	IVEE[0]

Table 33. Current-Limit Scaling Register

IVEE[1:0] (ADDRESS = 29h)	CURRENT LIMIT (%)
00	Default
01	-5
10	-10
11	-15

The three ICUT_ bits (Tables 34a and 34b) allow programming of the current-limit and overcurrent thresholds in excess of the IEEE 802.3af standard limit. The MAX5952 can automatically set the ICUT register or can be manually written to by the software (see Table 3).

Class 1 and 2 limits can also be programmed by software independently from the classification status. See Table 3. A reset or power-up sets R2Ah = R2Bh = 00h.

Table 34a. ICUT Registers 1 and 2

ADDRESS = 2Ah			DESCRIPTION
SYMBOL	BIT	R/W	
Reserved	7	—	Reserved
ICUT2	6	R/W	ICUT2[2]
	5	R/W	ICUT2[1]
	4	R/W	ICUT2[0]
Reserved	3	—	Reserved
ICUT1	2	R/W	ICUT1[2]
	1	R/W	ICUT1[1]
	0	R/W	ICUT1[0]

Table 34b. ICUT Registers 3 and 4

ADDRESS = 2Bh			DESCRIPTION
SYMBOL	BIT	R/W	
Reserved	7	—	Reserved
ICUT4	6	R/W	ICUT4[2]
	5	R/W	ICUT4[1]
	4	R/W	ICUT4[0]
Reserved	3	—	Reserved
ICUT3	2	R/W	ICUT3[2]
	1	R/W	ICUT3[1]
	0	R/W	ICUT3[0]

Table 34c. ICUT Register Bit Values for Current-Limit Threshold

ICUT_[2:0] (ADDRESS = 2Ah, 2Bh)	SCALE FACTOR	TYPICAL CURRENT-LIMIT THRESHOLD (mA)
000	1x	375
001	1.5x	563
010	1.75x	656
011	2x	750
100	2.25x	844
101	2.5x	938
110	0.3x	Class 1
111	0.53x	Class 2

Table 35. Classification Status Registers

ADDRESS = 2Ch, 2Dh, 2Eh, 2Fh			DESCRIPTION
SYMBOL	BIT	R/W	
Reserved	7	—	Reserved
	6	—	Reserved

The MAX5952 provides current readout for each port during classification and normal power mode. The current per port information is separated into 9 bits. They are organized into 2 consecutive registers for each one of the ports. The information can be quickly retrieved using the auto-increment option of the address pointer. To avoid the LSB register changing while reading the MSB, the information is frozen once the addressing byte points to any of the current readout registers.

During power mode, the current value can be calculated as

$$I_{PORT} = N_{IPD\_} \times 1.953125mA$$

During classification, the current is

$$I_{CLASS} = N_{IPD\_} \times 0.0975mA$$

where $N_{IPD\_}$ is the decimal value of the 9-bit word. The ADC saturates both at full scale and at zero. A reset sets R30h–R37h = 00h.

Table 36. Current Registers

ADDRESS = 30h, 31h, 32h, 33h, 34h, 35h, 36h, 37h			DESCRIPTION
SYMBOL	BIT	R/W	
IPD_	7	W	IPD_[8]
	6	W	IPD_[7]
	5	W	IPD_[6]
	4	W	IPD_[5]
	3	W	IPD_[4]
	2	W	IPD_[3]
	1	W	IPD_[2]
	0	W	IPD_[1]/IPD_[0]

High-Power, Quad, PSE Controller for Power-Over-Ethernet

Table 37. Register Summary

ADDR	REGISTER NAME	R/W	PORT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET STATE
INTERRUPTS												
00h	Interrupt	RO	G	SUP_FLT	TSTR_FLT	IMAX_FLT	CL_END	DET_END	LD_DISC	PG_INT	PE_INT	0000,0000
01h	Int Mask	R/W	G	MASK7	MASK6	MASK5	MASK4	MASK3	MASK2	MASK1	MASK0	AAA0,0A00
EVENTS												
02h	Power Event	RO	4321	PG_CHG4	PG_CHG3	PG_CHG2	PG_CHG1	PWEN_ CHG4	PWEN_ CHG3	PWEN_ CHG2	PWEN_ CHG1	0000,0000
03h	Power Event CoR	CoR										
04h	Detect Event	RO	4321	CL_END4	CL_END3	CL_END2	CL_END1	DET_END4	DET_END3	DET_END2	DET_END1	0000,0000
05h	Detect Event CoR	CoR										
06h	Fault Event	RO	4321	LD_DISC4	LD_DISC3	LD_DISC2	LD_DISC1	IMAX_FLT4	IMAX_FLT3	IMAX_FLT2	IMAX_FLT1	0000,0000
07h	Fault Event CoR	CoR										
08h	Tstart Event	RO	4321	IVC4	IVC3	IVC2	IVC1	STRT_FLT4	STRT_FLT3	STRT_FLT2	STRT_FLT1	0000,0000
09h	Tstart Event CoR	CoR										
0Ah	Supply Event	RO	4321	TSD	VDD_OV	VDD_UV	VEE_UVLO	VEE_OV	VEE_UV	OSC_FAIL	VDD_UVLO	0001,0000*
0Bh	Supply Event CoR	CoR										
STATUS												
0Ch	Port 1 Status	RO	1	Reserved	CLASS1[2]	CLASS1[1]	CLASS1[0]	Reserved	DET_ST1[2]	DET_ST1[1]	DET_ST1[0]	0000,0000
0Dh	Port 2 Status	RO	2	Reserved	CLASS2[2]	CLASS2[1]	CLASS2[0]	Reserved	DET_ST2[2]	DET_ST2[1]	DET_ST2[0]	0000,0000
0Eh	Port 3 Status	RO	3	Reserved	CLASS3[2]	CLASS3[1]	CLASS3[0]	Reserved	DET_ST3[2]	DET_ST3[1]	DET_ST3[0]	0000,0000
0Fh	Port 4 Status	RO	4	Reserved	CLASS4[2]	CLASS4[1]	CLASS4[0]	Reserved	DET_ST4[2]	DET_ST4[1]	DET_ST4[0]	0000,0000
10h	Power Status	RO	4321	PGOOD4	PGOOD3	PGOOD2	PGOOD1	PWR_EN4	PWR_EN3	PWR_EN2	PWR_EN1	0000,0000
11h	Pin Status	RO	G	Reserved	Reserved	A3	A2	A1	A0	MIDSPAN	AUTO	00A3A2, A1A0MA
CONFIGURATION												
12h	Operating Mode	R/W	4321	P4_M1	P4_M0	P3_M1	P3_M0	P2_M1	P2_M0	P1_M1	P1_M0	AAAA,AAAA
13h	Disconnect Enable	R/W	4321	ACD_EN4	ACD_EN3	ACD_EN2	ACD_EN1	DCD_EN4	DCD_EN3	DCD_EN2	DCD_EN1	0000,AAAA
14h	Det/Class Enable	R/W	4321	CLASS_EN4	CLASS_EN3	CLASS_EN2	CLASS_EN1	DET_EN4	DET_EN3	DET_EN2	DET_EN1	AAAA,AAAA
15h	Backoff Enable	R/W	4321	—	—	—	—	BCKOFF4	BCKOFF3	BCKOFF2	BCKOFF1	0000,XXXX
16h	Timing Config	R/W	G	RSTR[1]	RSTR[0]	TSTART[1]	TSTART[0]	TFAULT[1]	TFAULT[0]	TDISC[1]	TDISC[0]	0000,0000
17h	Misc Config 1	R/W	G	INT_EN	RSTR_EN	Reserved	Reserved	POFF_CL	CL_DISC	OUT_ISO	HP_TIME	1100,0000
PUSHBUTTONS												
18h	Reserved	R/W	G	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
19h	Power Enable	WO	4321	PWR_OFF4	PWR_OFF3	PWR_OFF2	PWR_OFF1	PWR_ON4	PWR_ON3	PWR_ON2	PWR_ON1	0000,0000
1Ah	Global	WO	G	CLR_INT	Reserved	Reserved	RESET_IC	RESET_P4	RESET_P3	RESET_P2	RESET_P1	0000,0000
GENERAL												
1Bh	ID	RO	G	ID_CODE[4]	ID_CODE[3]	ID_CODE[2]	ID_CODE[1]	ID_CODE[0]	REV [2]	REV [1]	REV [0]	1100,0000
1Ch	SMODE Register	CoR	4321	—	—	—	—	SMODE4	SMODE3	SMODE2	SMODE1	0000,0000
1Dh	Reserved		G	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
1EH	Watchdog Register	R/W	G	WDTIME[7]	WDTIME[6]	WDTIME[5]	WDTIME[4]	WDTIME[3]	WDTIME[2]	WDTIME[1]	WDTIME[0]	0000,0000
1FH	Switch Mode Register	R/W	4321	EN_WHDOG	WD_INT_EN	reserved	CSCM	HWMODE4	HWMODE3	HWMODE2	HWMODE1	0000,0000

Table 37. Register Summary (continued)

ADDR	REGISTER NAME	R/W	PORT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET STATE
MAXIM RESERVED												
20H	Reserved		G	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
21H	Reserved		G	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
22H	Reserved		G	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
23H	Program 1	R/W	4321	Reserved	Reserved	CLC_EN	DET_BY	OSCF_RS	AC_TH[2]	AC_TH[1]	AC_TH[0]	0000,0000
24h	High Power Mode	R/W	G	Reserved	—	—	—	Reserved	Reserved	Reserved	Reserved	0000,0000
25h	Reserved	—	G	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0000,0000
26h	Reserved	—	G	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0000,0000
27H	Reserved		G	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
28H	Reserved		G	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
29H	Misc Config 2	R/W	1234	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IVEE[1]	IVEE[0]	0000,0000
2AH	ICUT Register 1	R/W	21	Reserved	ICUT2[2]	ICUT2[1]	ICUT2[0]	Reserved	ICUT1[2]	ICUT1[1]	ICUT1[0]	0000,0000
2BH	ICUT Register 2	R/W	43	Reserved	ICUT4[2]	ICUT4[1]	ICUT4[0]	Reserved	ICUT3[2]	ICUT3[1]	ICUT[30]	0000,0000
CLASSIFICATION REGISTERS												
2CH	Port 1 Class	RO	1	Reserved	Reserved	—	—	—	—	—	—	0000,0000
2DH	Port 2 Class	RO	2	Reserved	Reserved	—	—	—	—	—	—	0000,0000
2EH	Port 3 Class	RO	3	Reserved	Reserved	—	—	—	—	—	—	0000,0000
2FH	Port 4 Class	RO	4	Reserved	Reserved	—	—	—	—	—	—	0000,0000
CURRENT REGISTER												
30H	Current Port 1 (MSB)	RO	1	IPD1[8]	IPD1[7]	IPD1[6]	IPD1[5]	IPD1[4]	IPD1[3]	IPD1[2]	IPD1[1]	0000,0000
31H	Current Port 1 (LSB)	RO	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IPD1[0]	0000,0000
32H	Current Port 2 (MSB)	RO	2	IPD2[8]	IPD2[7]	IPD2[6]	IPD2[5]	IPD2[4]	IPD2[3]	IPD2[2]	IPD2[1]	0000,0000
33H	Current Port 2 (LSB)	RO	2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IPD2[0]	0000,0000
34H	Current Port 3 (MSB)	RO	3	IPD3[8]	IPD3[7]	IPD3[6]	IPD3[5]	IPD3[4]	IPD3[3]	IPD3[2]	IPD3[1]	0000,0000
35H	Current Port 3 (LSB)	RO	3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IPD3[0]	0000,0000
36H	Current Port 4 (MSB)	RO	4	IPD4[8]	IPD4[7]	IPD4[6]	IPD4[5]	IPD4[4]	IPD4[3]	IPD4[2]	IPD4[1]	0000,0000
37H	Current Port 4 (LSB)	RO	4	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IPD4[0]	0000,0000

**UV and UVLO bits of V_{EE} and V_{DD} asserted depends on the order V_{EE} and V_{DD} supplies are brought up.*

A = AUTO pin state before reset.

M = MIDSPAN state before reset.

A3...0 = ADDRESS input states before reset.

High-Power, Quad, PSE Controller for Power-Over-Ethernet

Applications Information

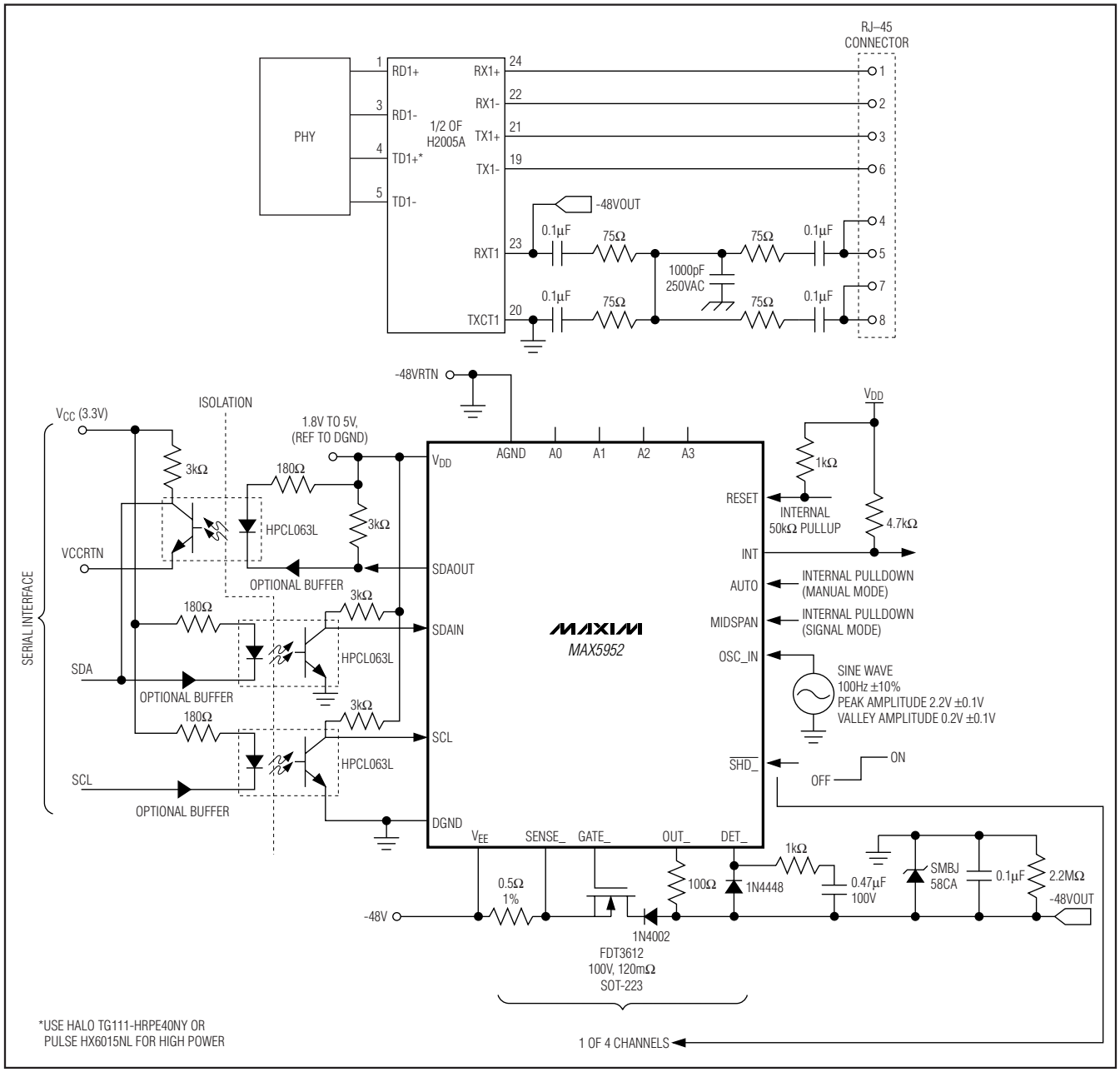


Figure 13. PoE System Block Diagram

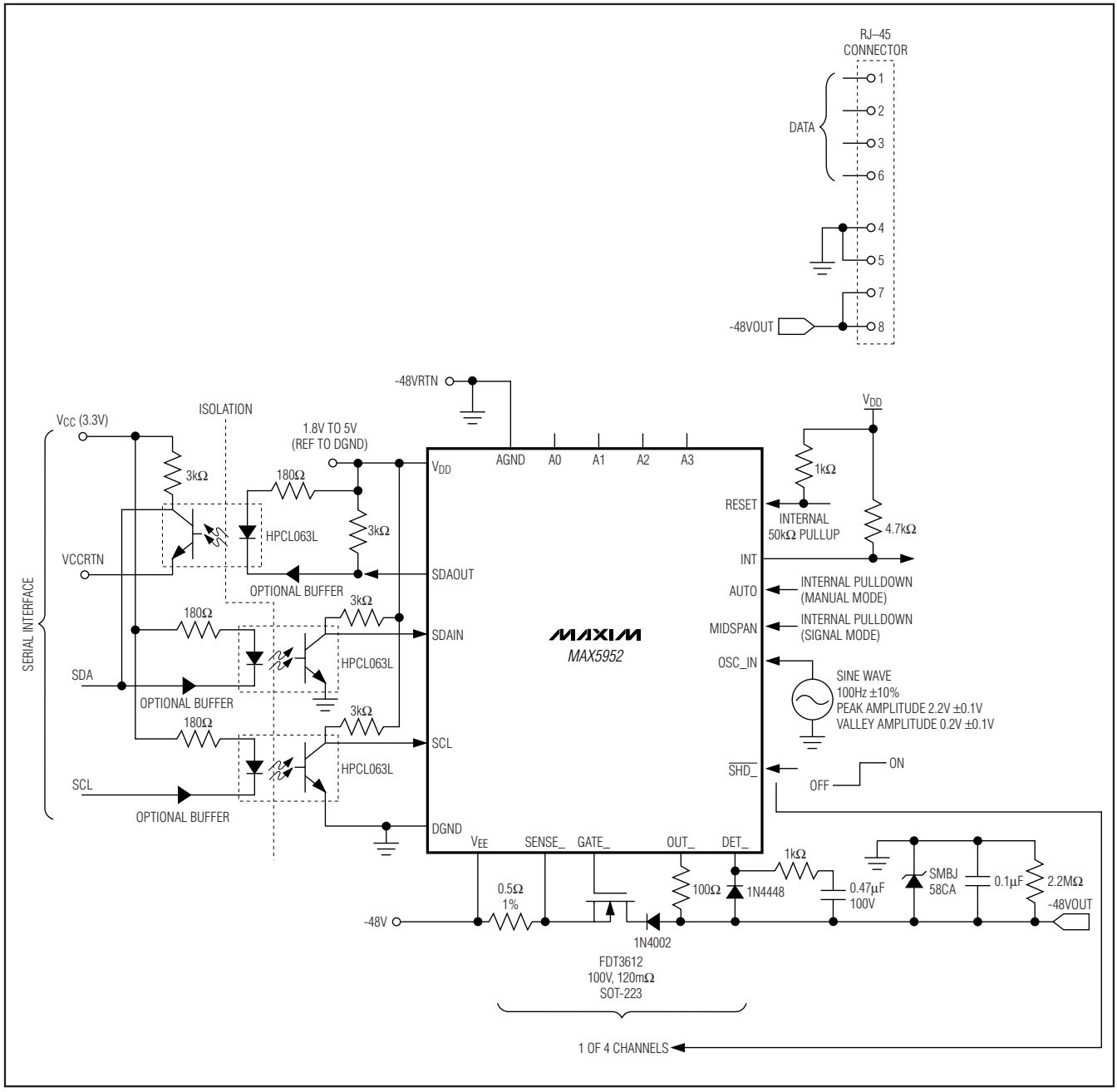


Figure 14. PoE System Block Diagram

High-Power, Quad, PSE Controller for Power-Over-Ethernet

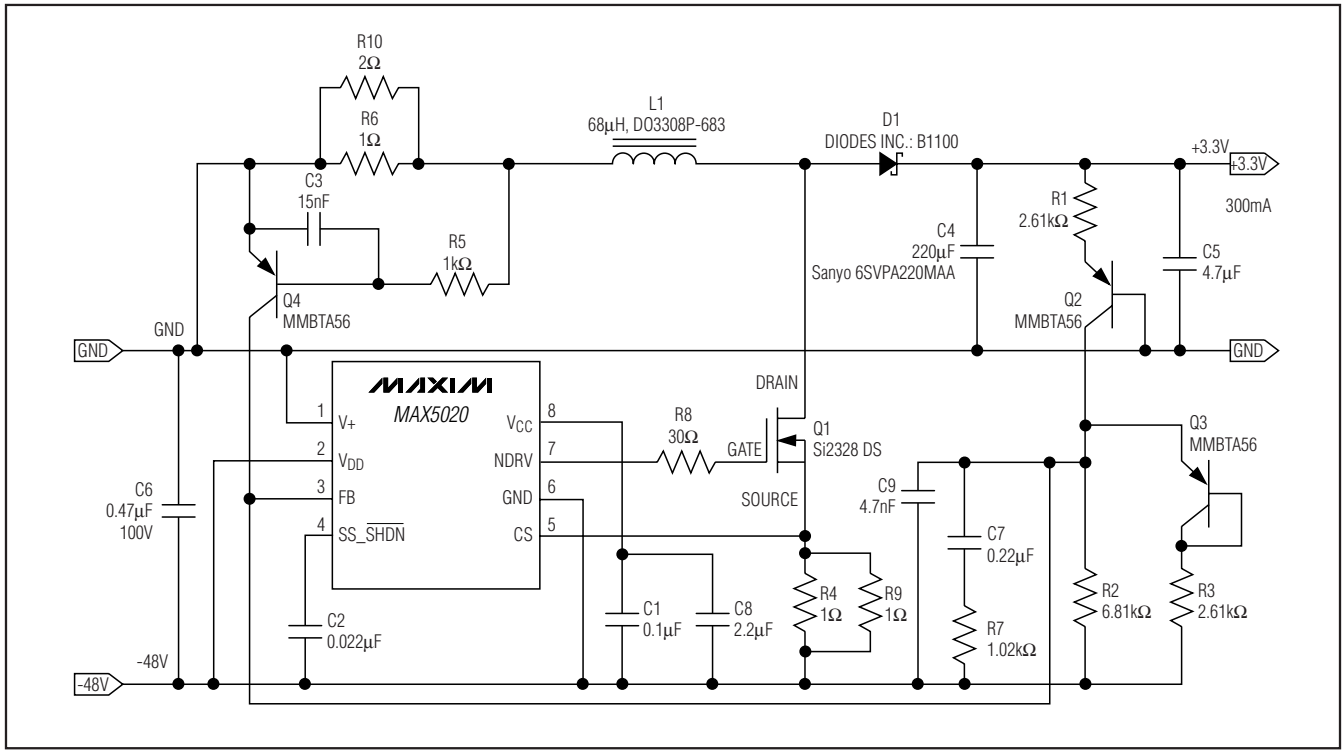


Figure 15. -48V to +3.3V (300mA) Boost Converter Solution for V_{DIG}

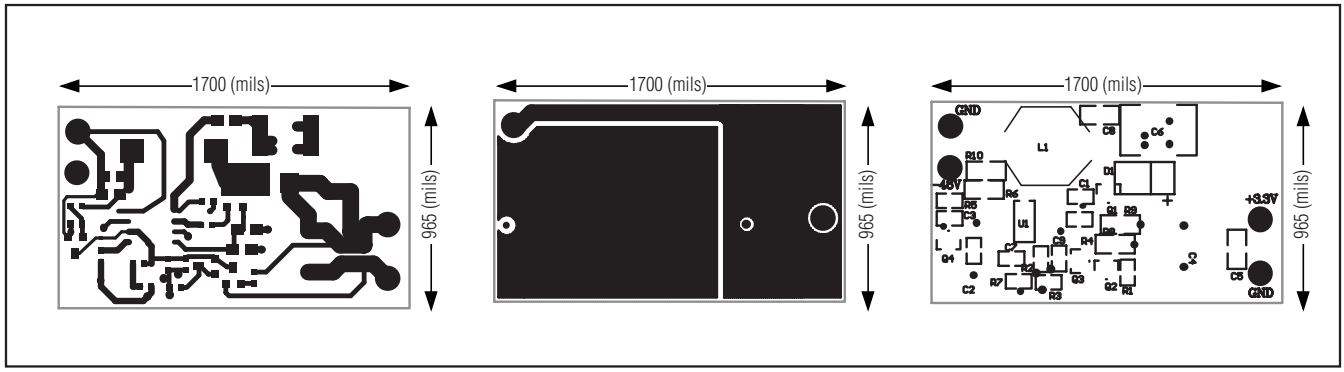


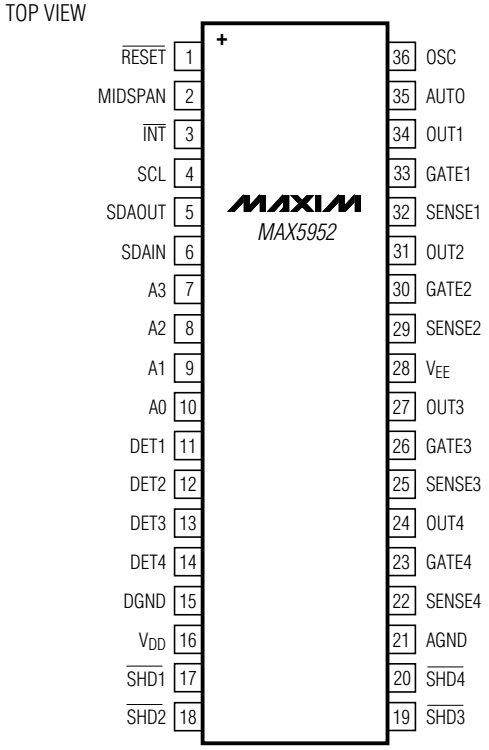
Figure 16. Layout Example for Boost Converter Solution for V_{DIG}

Component List for V_{DIG} Supply

DESIGNATION	DESCRIPTION
C1	0.1µF, 25V ceramic capacitor
C2	0.022µF, 25V ceramic capacitor
C3	15nF, 25V ceramic capacitor
C4	220µF capacitor Sanyo 6SVPA220MAA
C5	4.7µF, 16V ceramic capacitor
C6	0.47µF, 100V ceramic capacitor
C7	0.22µF, 16V ceramic capacitor
C8	2.2µF, 16V ceramic capacitor
C9	4.7nF, 16V ceramic capacitor
D1	B1100 100V Schottky diode
L1	68µH inductor Coilcraft DO3308P-683 or equivalent

DESIGNATION	DESCRIPTION
Q1	Si2328DS Vishay n-channel MOSFET, SOT23
Q2, Q3, Q4	MMBTA56 small-signal PNP
R1, R3	2.61kΩ ±1% resistors
R2	6.81kΩ ±1% resistor
R4, R6, R9	1Ω ±1% resistors
R5	1kΩ ±1% resistor
R7	1.02kΩ ±1% resistor
R8	30Ω ±1% resistor
R10	2Ω ±1% resistor
U1	High-voltage PWM IC MAX5020ESA (8-pin SO)

Pin Configuration



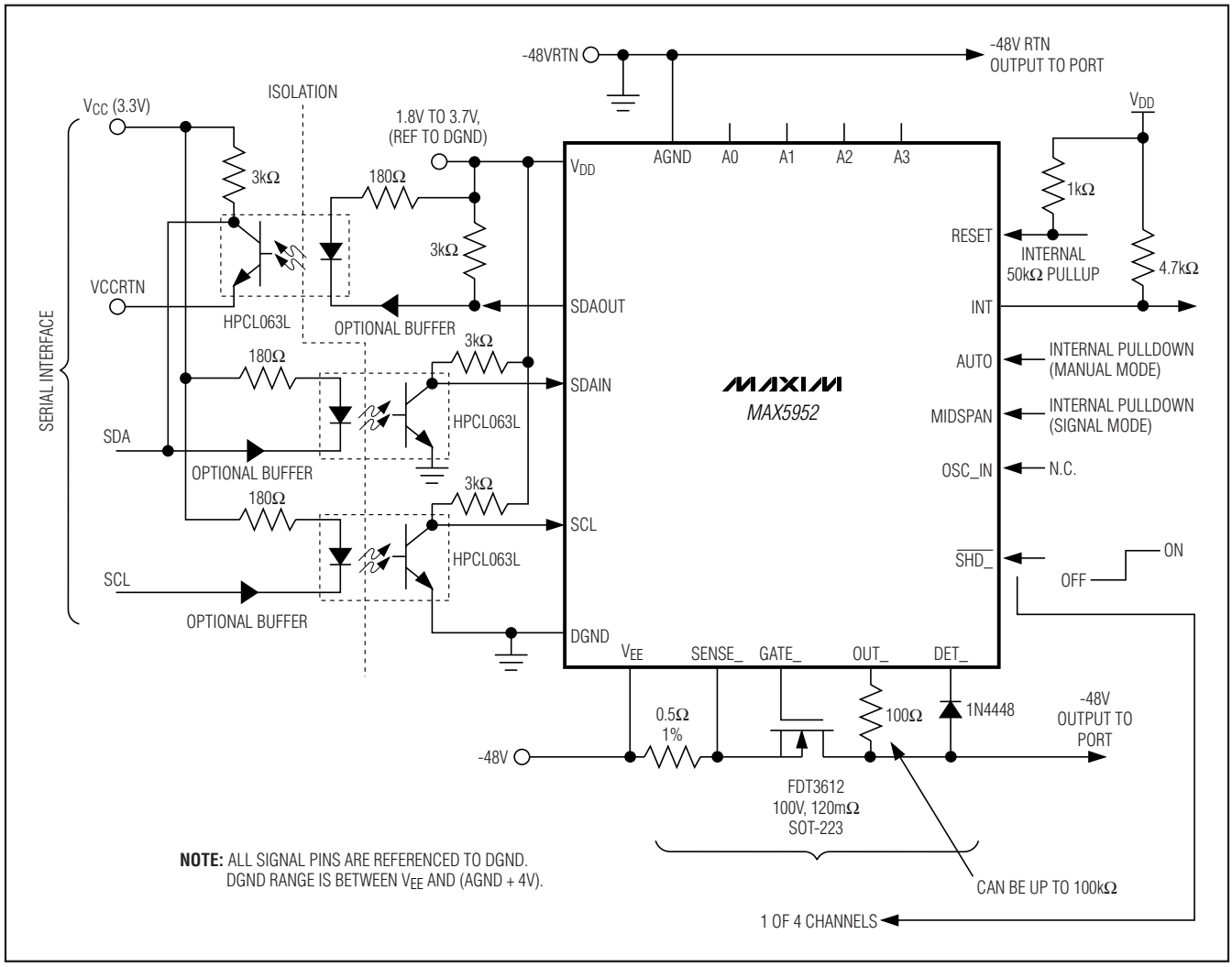
SSOP

Selector Guide

PART	SENSE RESISTOR (Ω)	V_{DD} (V)
MAX5952A_	0.5	3.3
MAX5952C_	0.5	5

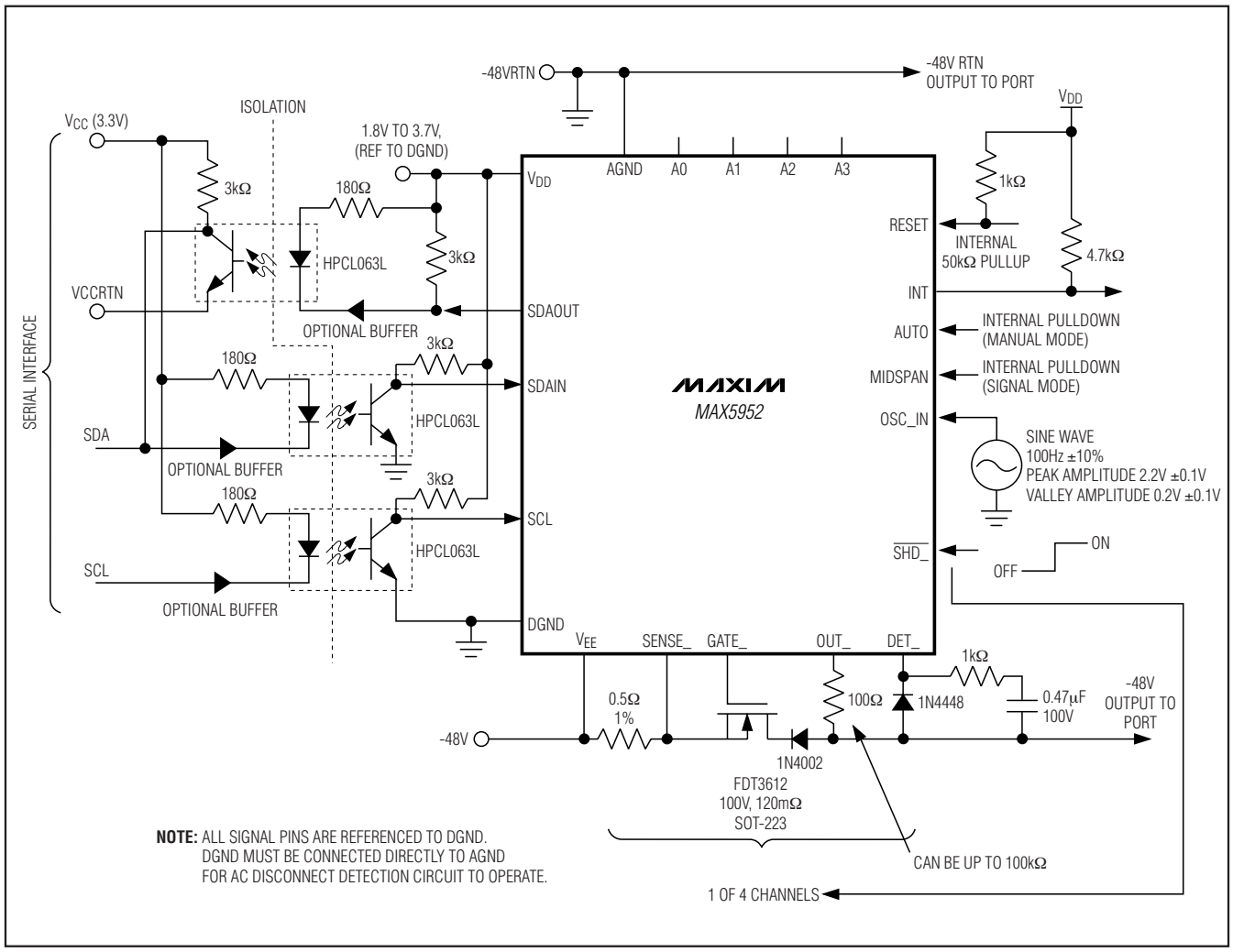
High-Power, Quad, PSE Controller for Power-Over-Ethernet

Typical Operating Circuits



Typical Operating Circuit 1 (without AC Load Removal Detection)

Typical Operating Circuits (continued)



Typical Operating Circuit 2 (with AC Load Removal Detection)

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
36 SSOP	A36-4	21-0040

High-Power, Quad, PSE Controller for Power-Over-Ethernet

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/07	Initial release	—
1	1/10	Revised the *General Description, Features, Electrical Characteristics* table, and *Detailed Description*.	1, 7, 15

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MAX5952AUAX+ on WIN SOURCE
- Maxim Integrated Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management