



**THE DATASHEET OF
MAX504CSD+T**



5V, Low-Power, Voltage-Output Serial 10-Bit DACs

ABSOLUTE MAXIMUM RATINGS

| | |
|---|--|
| V _{DD} to DGND and V _{DD} to AGND | -0.3V, +6V |
| V _{SS} to DGND and V _{SS} to AGND | -6V, +0.3V |
| V _{DD} to V _{SS} | -0.3V, +12V |
| AGND to DGND | -0.3V, +0.3V |
| Digital Input Voltage to DGND | -0.3V, (V _{DD} + 0.3V) |
| REFIN | (V _{SS} - 0.3V), (V _{DD} + 0.3V) |
| REFOUT to AGND | -0.3V, (V _{DD} + 0.3V) |
| RFB | (V _{SS} - 0.3V), (V _{DD} + 0.3V) |
| BIPOFF | (V _{SS} - 0.3V), (V _{DD} + 0.3V) |
| V _{OUT} (Note 1) | V _{SS} , V _{DD} |
| Continuous Current, Any Pin | -20mA, +20mA |

| | |
|---|-----------------|
| Continuous Power Dissipation (T _A = +70°C) | |
| 8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) | 727mW |
| 8-Pin SO (derate 5.88mW/°C above +70°C) | 471mW |
| 14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) | 800mW |
| 14-Pin SO (derate 8.33mW/°C above +70°C) | 667mW |
| Operating Temperature Ranges | |
| MAX5_C_ | 0°C to +70°C |
| MAX5_E_ | -40°C to +85°C |
| Storage Temperature Range | -65°C to +165°C |
| Lead Temperature (soldering, 10sec) | +300°C |

Note 1: The output may be shorted to V_{DD}, V_{SS}, or AGND if the package power dissipation limit is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V_{DD} = 5V, V_{SS} = 0V, AGND = DGND = 0V, REFIN = 2.048V (external), RFB = BIPOFF = V_{OUT} (MAX504), C_{REFOUT} = 33μF (MAX504), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------|---|-----|-----|-----------------------|--------|
| STATIC PERFORMANCE | | | | | | |
| Resolution | N | | 10 | | | Bits |
| Relative Accuracy (Note 2) | INL | | | | ±0.5 | LSB |
| Differential Nonlinearity | DNL | Guaranteed monotonic | | | ±1 | LSB |
| Unipolar Offset Error | V _{OS} | | 0 | | 3 | LSB |
| Unipolar Offset Tempco | TCV _{OS} | | | 3 | | ppm/°C |
| Unipolar Offset-Error Power-Supply Rejection Ratio | PSRR | 4.5V ≤ V _{DD} ≤ 5.5V | | 0.1 | | LSB/V |
| Gain Error (Note 2) | GE | | | | ±1 | LSB |
| Gain-Error Tempco | | | | 1 | | ppm/°C |
| Gain-Error Power-Supply Rejection Ratio | PSRR | 4.5V ≤ V _{DD} ≤ 5.5V | | 0.1 | | LSB/V |
| VOLTAGE OUTPUT (V_{out}) | | | | | | |
| Output Voltage Range | | MAX504 (G = 1) | 0 | | V _{DD} - 2 | V |
| | | MAX504 (G = 2), MAX515 | 0 | | V _{DD} - 0.4 | |
| Output Load Regulation | | V _{OUT} = 2V, R _L = 2kΩ | | | 0.5 | LSB |
| Short-Circuit Current | I _{SC} | | | 12 | | mA |
| REFERENCE INPUT (REFIN) | | | | | | |
| Voltage Range | | | 0 | | V _{DD} - 2 | V |
| Input Resistance | | Code dependent, minimum at code 0101... | 40 | | | kΩ |
| Input Capacitance | | Code dependent (Note 3) | 10 | | 50 | pF |
| AC Feedthrough | | REFIN = 1kHz, 2Vp-p | | -80 | | dB |

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

MAX504/MAX515

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

($V_{DD} = 5V$, $V_{SS} = 0V$, $AGND = DGND = 0V$, $REFIN = 2.048V$ (external), $RFB = BIPOFF = VOUT$ (MAX504), $C_{REFOUT} = 33\mu F$ (MAX504), $R_L = 10k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------|---|--------------|-------|---------|-----------------|
| REFERENCE OUTPUT (REFOUT—MAX504 Only) | | | | | | |
| Reference Output Voltage | | $T_A = +25^\circ C$ | 2.024 | 2.048 | 2.072 | V |
| | | MAX504C | 2.015 | | 2.081 | |
| | | MAX504E | 2.011 | | 2.085 | |
| Temperature Coefficient | TC_{REFOUT} | | | 30 | | ppm/ $^\circ C$ |
| Resistance | R_{REFOUT} | (Note 4) | | 0.5 | 2 | Ω |
| Power-Supply Rejection Ratio | PSRR | $4.5V \leq V_{DD} \leq 5.5V$ | | 200 | | $\mu V/V$ |
| Noise Voltage | e_n | 0.1Hz to 10kHz | | 400 | | μV_{p-p} |
| Required External Capacitor | C_{REFOUT} | | 3.3 | | | μF |
| DIGITAL INPUTS (DIN, SCLK, \overline{CS}, CLR) | | | | | | |
| Input High | V_{IH} | | 2.4 | | | V |
| Input Low | V_{IL} | | | | 0.8 | V |
| Input Current | I_{IN} | $V_{IN} = 0V$ or V_{DD} | | | ± 1 | μA |
| Input Capacitance | C_{IN} | | | 8 | | pF |
| DIGITAL OUTPUT (DOUT) | | | | | | |
| Output High | V_{OH} | $I_{SOURCE} = 2mA$ | $V_{DD} - 1$ | | | V |
| Output Low | V_{OL} | $I_{SINK} = 2mA$ | | | 0.4 | V |
| DYNAMIC PERFORMANCE | | | | | | |
| Voltage-Output Slew Rate | SR | $T_A = +25^\circ C$ | 0.15 | 0.25 | | V/ μs |
| Voltage-Output Settling Time | | $T_o \pm 1/2LSB$, $V_{OUT} = 2V$ | | 25 | | μs |
| Digital Feedthrough | | $\overline{CS} = V_{DD}$, $DIN = 100kHz$ | | 5 | | nV-s |
| Signal-to-Noise Plus Distortion | SINAD | $REFIN = 1kHz$, $2V_{p-p}$ ($G = 1$ or 2), code = 1111... | | 68 | | dB |
| POWER SUPPLY | | | | | | |
| Positive Supply Voltage | V_{DD} | | 4.5 | | 5.5 | V |
| Power-Supply Current | I_{DD} | All inputs = $0V$ or V_{DD} , output = no load | MAX504 | 260 | 400 | μA |
| | | | MAX515 | 140 | 300 | |
| SWITCHING CHARACTERISTICS (Note 5) | | | | | | |
| \overline{CS} Setup Time | t_{CSS} | | 20 | | | ns |
| SCLK Fall to \overline{CS} Fall Hold Time | t_{CSH0} | | 15 | | | ns |
| SCLK Fall to \overline{CS} Rise Hold Time | t_{CSH1} | | 0 | | | ns |
| SCLK High Width | t_{CH} | | 35 | | | ns |
| SCLK Low Width | t_{CL} | | 35 | | | ns |
| DIN Setup Time | t_{DS} | | 45 | | | ns |
| DIN Hold Time | t_{DH} | | 0 | | | ns |
| DOUT Valid Propagation Delay | t_{DO} | $C_L = 50pF$ | | | 80 | ns |
| \overline{CS} High Pulse Width | t_{CSW} | | 20 | | | ns |
| \overline{CLR} Pulse Width | t_{CLR} | | 25 | | | ns |
| \overline{CS} Rise to SCLK Rise Setup Time | t_{CS1} | | 50 | | | ns |

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ELECTRICAL CHARACTERISTICS—Dual $\pm 5V$ Supplies (MAX504 Only)

($V_{DD} = 5V$, $V_{SS} = -5V$, $AGND = DGND = 0V$, $REFIN = 2.048V$ (external), $R_{FB} = BIPOFF = V_{OUT}$, $C_{REFOUT} = 33\mu F$, $R_L = 10k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------|---|--------------|-------|--------------|------------------|
| Resolution | N | | 10 | | | Bits |
| Relative Accuracy | INL | | | | ± 0.5 | LSB |
| Differential Nonlinearity | DNL | Guaranteed monotonic | | | ± 1 | LSB |
| Bipolar Offset Error | V_{OS} | $BIPOFF = REFIN$ | | | ± 3 | LSB |
| Bipolar Offset Tempco | TCV_{OS} | $BIPOFF = REFIN$ | | 3 | | ppm/ $^{\circ}C$ |
| Offset-Error Power-Supply Rejection Ratio | PSRR | $4.5V \leq V_{DD} \leq 5.5V$, $-5.5V \leq V_{SS} \leq -4.5V$ | | 0.1 | | LSB/V |
| Gain Error (Unipolar or Bipolar) | GE | | | | ± 1 | LSB |
| Gain-Error Tempco | | | | 1 | | ppm/ $^{\circ}C$ |
| Gain-Error Power-Supply Rejection Ratio | PSRR | $4.5V \leq V_{DD} \leq 5.5V$, $-5.5V \leq V_{SS} \leq -4.5V$ | | 0.1 | | LSB/V |
| REFERENCE INPUT (REFIN) | | | | | | |
| Voltage Range | | | $V_{SS} + 2$ | | $V_{DD} - 2$ | V |
| Input Resistance | | Code dependent, minimum at code 0101... | 40 | | | $k\Omega$ |
| Input Capacitance | | Code dependent (Note 3) | 10 | | 50 | pF |
| AC Feedthrough | | $REFIN = 1kHz$, $2.0V_{p-p}$ | | -80 | | dB |
| REFERENCE OUTPUT (REFOUT—MAX504 Only) | | | | | | |
| Reference Output Voltage | | $T_A = +25^{\circ}C$ | 2.024 | 2.048 | 2.072 | V |
| | | MAX504C | 2.015 | | 2.081 | |
| | | MAX504E | 2.011 | | 2.085 | |
| Temperature Coefficient | TC_{REFOUT} | | | 30 | | ppm/ $^{\circ}C$ |
| Resistance | R_{REFOUT} | (Note 4) | | 0.5 | 2 | Ω |
| Power-Supply Rejection Ratio | PSRR | $4.5V \leq V_{DD} \leq 5.5V$ | | 200 | | $\mu V/V$ |
| Noise Voltage | e_n | 0.1Hz to 10kHz | | 400 | | μV_{p-p} |
| Required External Capacitor | C_{REFOUT} | | 3.3 | | | μF |
| DIGITAL INPUTS (DIN, SCLK, CS) | | | | | | |
| Input High | V_{IH} | | 2.4 | | | V |
| Input Low | V_{IL} | | | | 0.8 | V |
| Input Current | I_{IN} | $V_{IN} = 0V$ or V_{DD} | | | ± 1 | μA |
| Input Capacitance | C_{IN} | | | 8 | | pF |
| DIGITAL OUTPUT (DOUT) | | | | | | |
| Output High | V_{OH} | $I_{SOURCE} = 2mA$ | $V_{DD} - 1$ | | | V |
| Output Low | V_{OL} | $I_{SINK} = 2mA$ | | | 0.4 | V |

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MAX504/MAX515

ELECTRICAL CHARACTERISTICS—Dual ±5V Supplies (MAX504 Only) (continued)

($V_{DD} = 5V$, $V_{SS} = -5V$, $AGND = DGND = 0V$, $REFIN = 2.048V$ (external), $R_{FB} = BIPOFF = V_{OUT}$, $C_{REFOUT} = 33\mu F$, $R_L = 10k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------------------|--|----------------|------|----------------|------------|
| VOLTAGE OUTPUT (V_{OUT}) | | | | | | |
| Output Voltage Range | | (G = 1) | $V_{SS} + 2$ | | $V_{DD} - 2$ | V |
| | | (G = 2) | $V_{SS} + 0.4$ | | $V_{DD} - 0.4$ | |
| Output Load Regulation | | $V_{OUT} = 2V$, $R_L = 2k\Omega$ | | | 0.5 | LSB |
| Short-Circuit Current | I _{SC} | | | 12 | | mA |
| DYNAMIC PERFORMANCE | | | | | | |
| Voltage-Output Slew Rate | SR | | 0.15 | 0.25 | | V/ μ s |
| Voltage-Output Settling Time | | To $\pm 1/2$ LSB, $V_{OUT} = 2V$ | | 16 | | μ s |
| Digital Feedthrough | | Step all 0s to all 1s | | 5 | | nV-s |
| Signal-to-Noise Plus Distortion | SINAD | $REFIN = 1kHz$, 2Vp-p (G = 1) | | 68 | | dB |
| | | $REFIN = 1kHz$, 2Vp-p (G = 2) | | 68 | | |
| POWER SUPPLY | | | | | | |
| Positive Supply Voltage | V _{DD} | | 4.5 | | 5.5 | V |
| Negative Supply Voltage | V _{SS} | | -5.5 | | 0 | V |
| Positive Supply Current | I _{DD} | All inputs = 0V or V _{DD} , no load | | 260 | 400 | μ A |
| Negative Supply Current | I _{SS} | All inputs = 0V or V _{DD} , no load | | -120 | -200 | μ A |
| SWITCHING CHARACTERISTICS | | | | | | |
| \overline{CS} Setup Time | t _{CSS} | | 20 | | | ns |
| SCLK Fall to \overline{CS} Fall Hold Time | t _{CSH0} | | 15 | | | ns |
| SCLK Fall to \overline{CS} Rise Hold Time | t _{CSH1} | | 0 | | | ns |
| SCLK High Width | t _{CH} | | 35 | | | ns |
| SCLK Low Width | t _{CL} | | 35 | | | ns |
| DIN Setup Time | t _{DS} | | 45 | | | ns |
| DIN Hold Time | t _{DH} | | 0 | | | ns |
| DO _{UT} Valid Propagation Delay | t _{DO} | $C_L = 50pF$ | | | 80 | ns |
| \overline{CS} High Pulse Width | t _{C_{SW}} | | 20 | | | ns |
| \overline{CLR} Pulse Width | t _{CLR} | | 25 | | | ns |
| \overline{CS} Rise to SCLK Rise Setup Time | t _{CS1} | | 50 | | | ns |

Note 2: In single-supply operation, INL and GE calculated from Code 3 to Code 1023.

Note 3: Guaranteed by design.

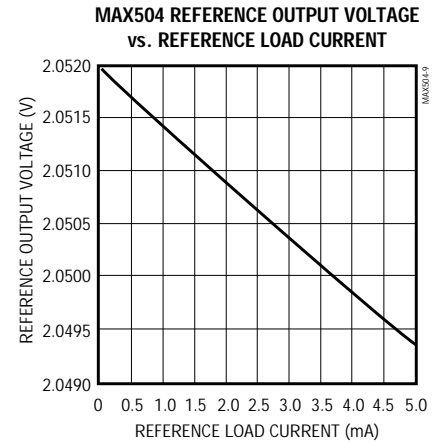
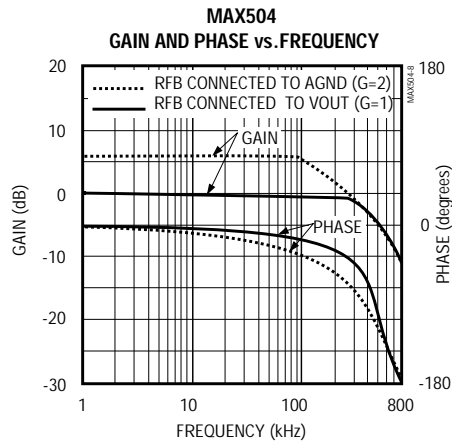
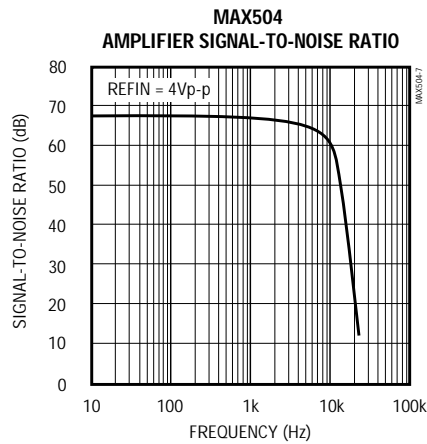
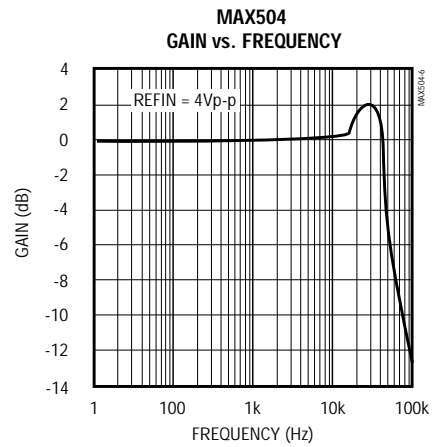
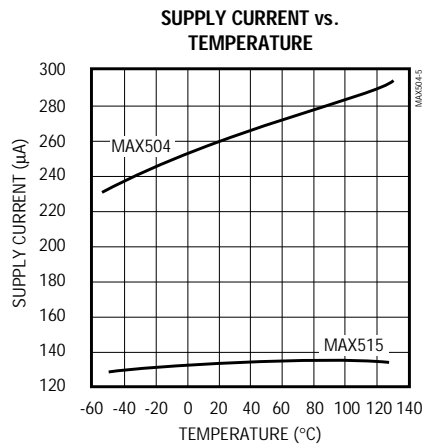
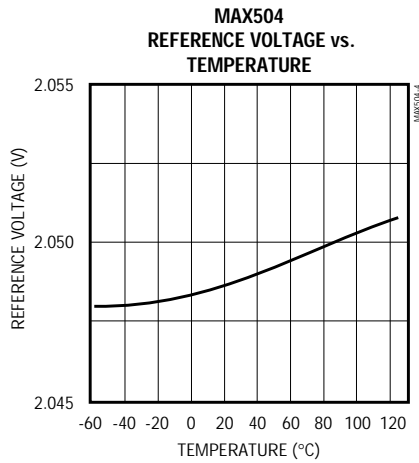
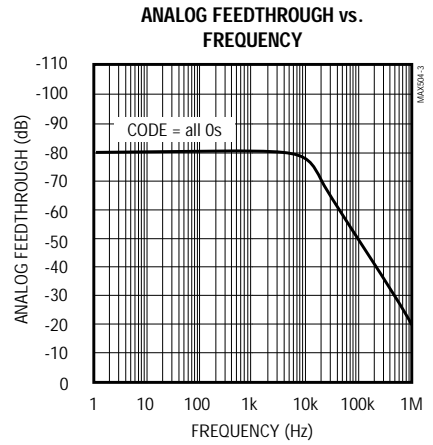
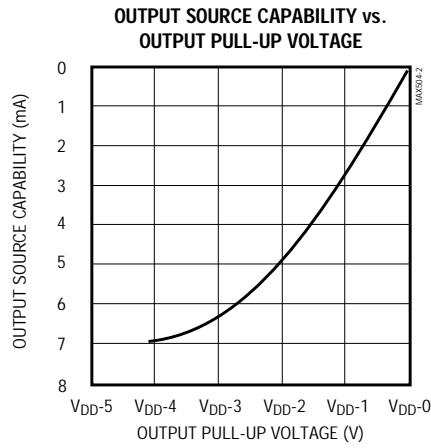
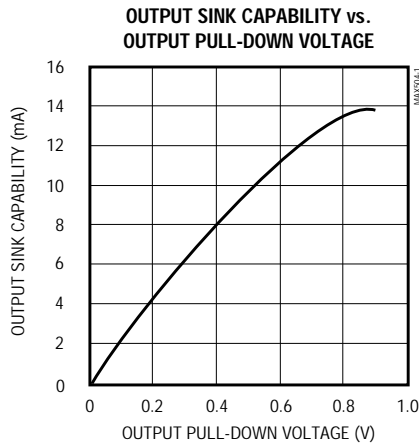
Note 4: Tested at I_{OUT} = 100 μ A. The reference can typically source up to 5mA (see *Typical Operating Characteristics*).

Note 5: The timing characteristics limits for the MAX515 are guaranteed by design.

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

Typical Operating Characteristics

($V_{DD} = +5V$, $V_{REFIN} = 2.048V$, $T_A = +25^{\circ}C$, unless otherwise noted.)

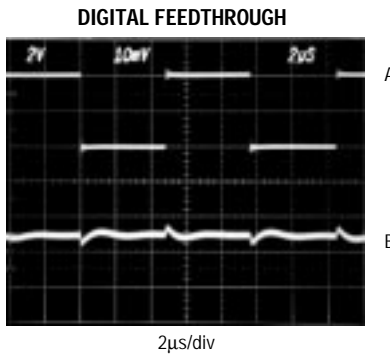


5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

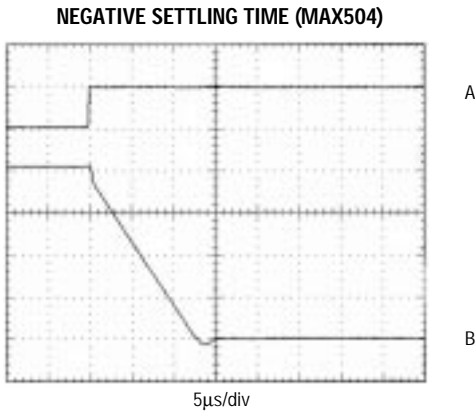
MAX504/MAX515

Typical Operating Characteristics (continued)

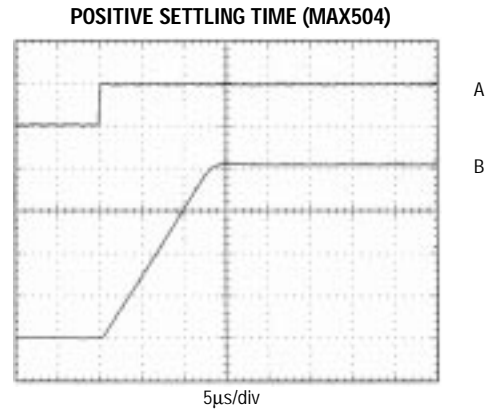
(VDD = +5V, VREFIN = 2.048V, TA = +25°C, unless otherwise noted.)



\overline{CS} = HIGH
 A: DIN = 4Vp-p, 100kHz
 B: VOUT, 10mV/div



A: \overline{CS} RISING EDGE, 5V/div
 B: VOUT, NO LOAD, 1V/div
 DUAL SUPPLY ±5V
 BIPOLAR CONFIGURATION
 VREFIN = 2V



A: \overline{CS} RISING EDGE, 5V/div
 B: VOUT, NO LOAD, 1V/div
 DUAL SUPPLY ±5V
 BIPOLAR CONFIGURATION
 VREFIN = 2V

5V, Low-Power, Voltage-Output Serial 10-Bit DACs

Pin Description

| PIN | | NAME | FUNCTION |
|--------|--------|-------------------------|--|
| MAX504 | MAX515 | | |
| 1 | — | BIPOFF | Bipolar offset/gain resistor |
| 2 | 1 | DIN | Serial data input |
| 3 | — | $\overline{\text{CLR}}$ | Clear. Asynchronously sets DAC register to all 0s. |
| 4 | 2 | SCLK | Serial clock input |
| 5 | 3 | $\overline{\text{CS}}$ | Chip select, active low |
| 6 | 4 | DOUT | Serial data output for daisy-chaining |
| 7 | — | DGND | Digital ground |
| 8 | 5 | AGND | Analog ground |
| 9 | 6 | REFIN | Reference input |
| 10 | — | REFOUT | Reference output, 2.048V. Connect to V_{DD} if not used. |
| 11 | — | V_{SS} | Negative power supply |
| 12 | 7 | VOOUT | DAC output |
| 13 | 8 | V_{DD} | Positive power supply |
| 14 | — | RFB | Feedback resistor |

Detailed Description

General DAC Discussion

The MAX504/MAX515 use an “inverted” R-2R ladder network with a single-supply CMOS op amp to convert 10-bit digital data to analog voltage levels (see *Functional Diagram*). The term “inverted” describes the ladder network because the REFIN pin in current-output DACs is the summing junction, or virtual ground, of an op amp. However, such use would result in the output voltage being the inverse of the reference voltage. The MAX504/MAX515's topology makes the output the same polarity as the reference input.

An internal reset circuit forces the DAC register to reset to all 0s on power-up. Additionally, a clear ($\overline{\text{CLR}}$) pin, when held low, sets the DAC register to all 0s. $\overline{\text{CLR}}$ operates asynchronously and independently from the chip select ($\overline{\text{CS}}$) pin.

Buffer Amplifier

The output buffer is a unity-gain stable, rail-to-rail output, BiCMOS op amp. Input offset voltage and CMRR are trimmed to achieve better than 10-bit performance. Settling time is 25 μ s to 0.01% of final value. The output is short-circuit protected and can drive a 2k Ω load with more than 100pF load capacitance.

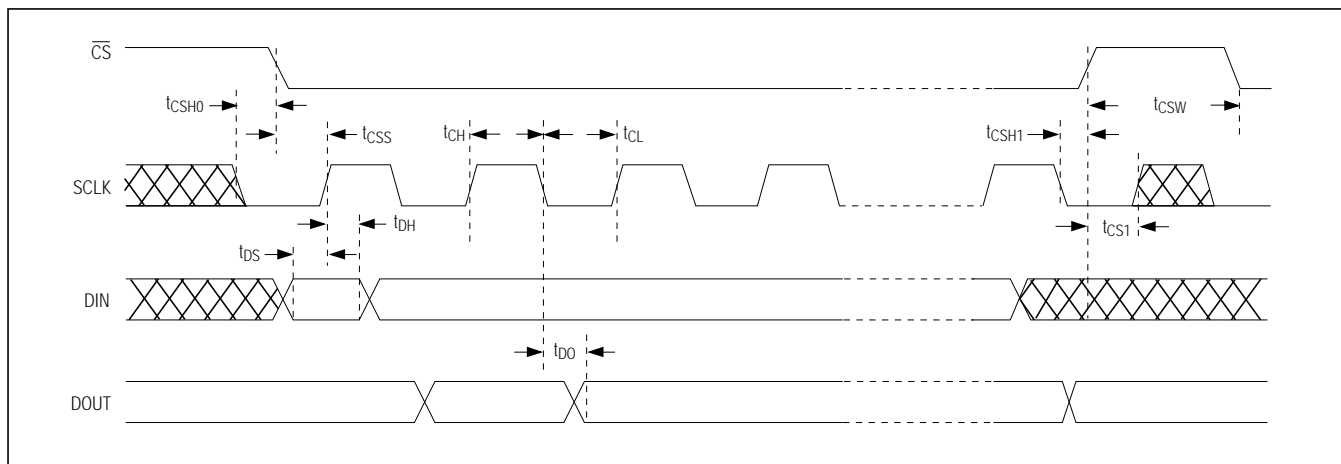


Figure 1. Timing Diagram

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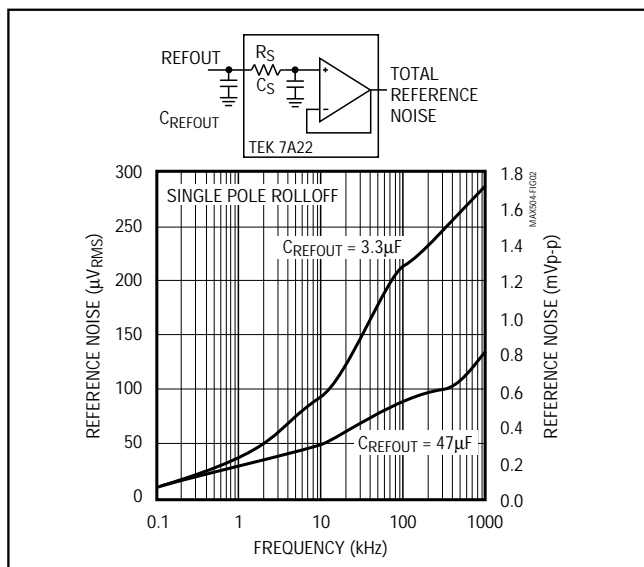


Figure 2. Reference Noise vs. Frequency

Internal Reference (MAX504 only)

The on-chip reference is laser trimmed to generate 2.048V at REFOUT. The output stage can source and sink current so REFOUT can settle to the correct voltage quickly in response to code-dependent loading changes. Typically, source current is 5mA and sink current is 100 μ A.

REFOUT connects the internal reference to the R-2R DAC ladder at REFIN. The R-2R ladder draws 50 μ A maximum load current. If any other connection is made to REFOUT, ensure that the total load current is less than 100 μ A to avoid gain errors.

For applications requiring very low-noise performance, connect a 33 μ F capacitor from REFOUT to AGND. If noise is not a concern, a lower value (3.3 μ F min) capacitor may be used. To reduce noise further, insert a buffered RC filter between REFOUT and REFIN (Figure 2). The reference bypass capacitor CREFOUT is still required for reference stability. In applications not requiring the reference, connect REFOUT to VDD (to save power and to eliminate the need for CREFOUT) or use the MAX515 (no internal reference).

External Reference

An external reference in the range (VSS + 2V) to (VDD - 2V) may be used with the MAX504 in dual-supply operation. With the MAX515 or the MAX504 in single-supply use, the reference must be positive and may not exceed VDD - 2V. The reference voltage determines the DAC's full-scale output. The DAC input resistance is code dependent and is minimum (40k Ω) at code 0101... and virtually infinite at

code 0000.... REFIN's input capacitance is also code dependent and has a 50pF maximum value at several codes.

If an upgrade to the internal reference is required, the 2.5V MAX873A is suitable: ± 15 mV initial accuracy, TCVOUT = 7ppm/ $^{\circ}$ C (max).

Logic Interface

The MAX504/MAX515 logic inputs are designed to be compatible with TTL or CMOS logic levels. However, to achieve the lowest power dissipation, drive the digital inputs with rail-to-rail CMOS logic. With TTL logic levels, the power requirement increases by a factor of approximately 2.

Serial Clock and Update Rate

Figure 1 shows the MAX504/MAX515 timing. The maximum serial clock rate is given by $1/(t_{CH} + t_{CL})$, approximately 14MHz. The digital update rate is limited by the chip-select period, which is $16 \times (t_{CH} + t_{CL}) + t_{CSW}$. This equals a 1.14 μ s, or 877kHz, update rate. However, the DAC settling time to 10 bits is 25 μ s, which may limit the update rate to 40kHz for full-scale step transitions.

Applications Information

Refer to Figures 3a and 3b for typical operating connections.

Serial Interface

The MAX504/MAX515 use a three-wire serial interface that is compatible with SPI[™], QSPI[™] (CPOL = CPHA = 0), and Microwire[™] standards as shown in Figures 4 and 5. The DAC is programmed by writing two 8-bit words (see Figure 1 and the *Functional Diagram*). 16 bits of serial data are clocked into the DAC in the following order: 4 fill (dummy) bits, 10 data bits, and 2 sub-LSB 0s. The 4 dummy bits are not normally needed, and are required **only** when DACs are daisy chained. The 2 sub-LSB 0s, however, are **always** needed, and allow hardware and software compatibility with the 12-bit MAX531/MAX538/MAX539. Transitions at \overline{CS} should occur while SCLK is low. Data is clocked in on SCLK's rising edge while \overline{CS} is low. The serial input data is held in a 16-bit serial shift register. On \overline{CS} 's rising edge, the 10 data-bits are transferred to the DAC register and update the DAC. With \overline{CS} high, data cannot be clocked into the MAX504/MAX514.

The MAX504/MAX515 inputs data in 16-bit blocks. The SPI and Microwire interfaces output data in 8-bit blocks, thereby requiring two write cycles to input data to the DAC. The QSPI interface allows variable data input from 8 to 16 bits, and can be loaded into the DAC in one write cycle.

SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

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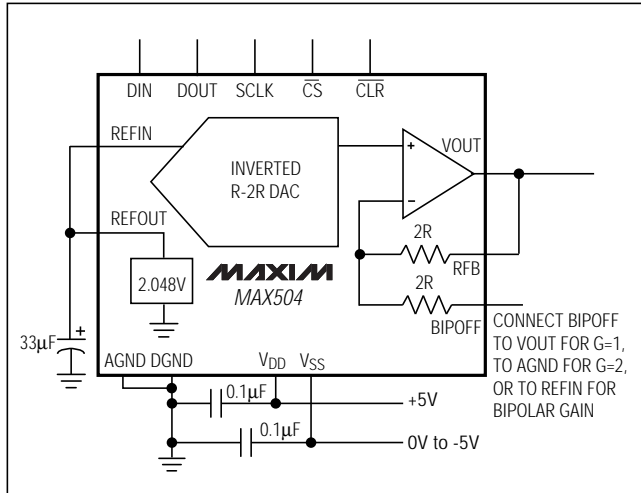


Figure 3a. MAX504 Typical Operating Circuit

Daisy-Chaining Devices

The serial output, DOUT, allows cascading of two or more DACs. The data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width. For low power, DOUT is a CMOS output that does not require an external pull-up resistor. DOUT does **not** go into a high-impedance state when \overline{CS} is high. DOUT changes on SCLK's falling edge when \overline{CS} is low. When \overline{CS} is high, DOUT remains in the state of the last data bit.

Any number of MAX504/MAX515 DACs can be daisy-chained by connecting the DOUT of one device to the DIN of the next device in the chain. For proper timing, ensure that t_{CL} (SCLK low) is greater than $t_{DO} + t_{DS}$.

Unipolar Configuration

The MAX504 is configured for a gain of 1 (0V to V_{REFIN} unipolar output) by connecting BIPOFF and RFB to VOUT (Figure 6). The converter operates from either single or dual supplies in this configuration. See Table 1 for the DAC-latch contents (input) vs. the analog VOUT (output). In this range, $1\text{LSB} = V_{REFIN}(2^{-10})$, where V_{REF} is the voltage on REFIN.

A gain of 2 (0V to $2V_{REFIN}$ unipolar output) is set up by connecting BIPOFF to AGND and RFB to VOUT (Figure 7). Table 2 shows the DAC-latch contents vs. VOUT. The MAX504 operates from either single or dual supplies in this mode. In this range,

$$1\text{LSB} = (2)(V_{REFIN})(2^{-10}) = (V_{REFIN})(2^{-9}).$$

The MAX515 is internally configured for unipolar gain of 2 operation.

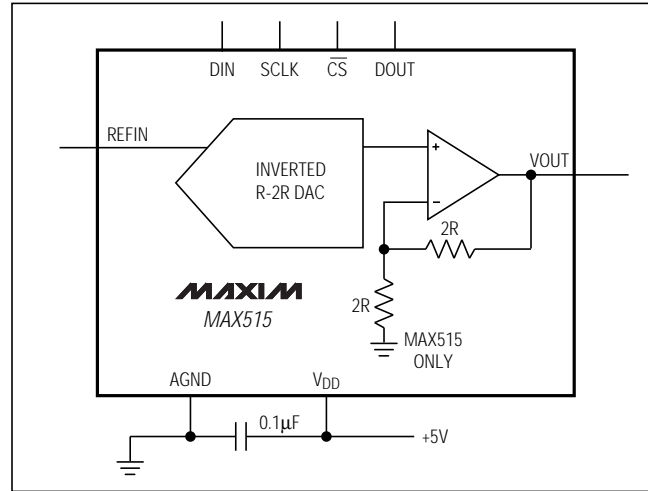


Figure 3b. MAX515 Typical Operating Circuit

Bipolar Configuration

A bipolar range is set up by connecting BIPOFF to REFIN and RFB to VOUT, and operating from dual ($\pm 5\text{V}$) supplies (Figure 8). Table 3 shows the DAC-latch contents (input) vs. VOUT (output). In this range, $1\text{LSB} = V_{REFIN}(2^{-9})$.

Four-Quadrant Multiplication

The MAX504 can be used as a four-quadrant multiplier by connecting BIPOFF to REFIN and RFB to VOUT, and using (1) an offset binary digital code, (2) bipolar power supplies, and (3) a bipolar analog input at REFIN within the range $V_{SS} + 2\text{V}$ to $V_{DD} - 2\text{V}$, as shown in Figure 9.

In general, a 10-bit DAC's output is $(D)(V_{REFIN})(G)$, where "G" is the gain (1 or 2) and "D" is the binary representation of the digital input divided by 2^{10} or 1,024. This formula is precise for unipolar operation. However, for bipolar, offset binary operation, the MSB is really a polarity bit. No resolution is lost because the number of steps is the same. The output voltage, however, has been shifted from a range of, for example, 0V to 4.096V ($G = 2$) to a range of -2.048V to +2.048V.

Keep in mind that when using the DAC as a four-quadrant multiplier, the scale is skewed. Negative full scale is $-V_{REFIN}$, while positive full scale is $+V_{REFIN} - 1\text{LSB}$.

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

MAX504/MAX515

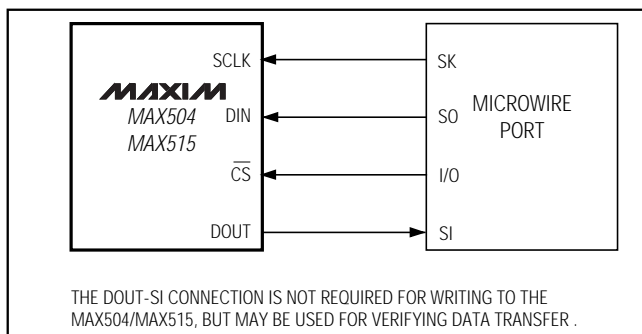


Figure 4. Microwire Connection

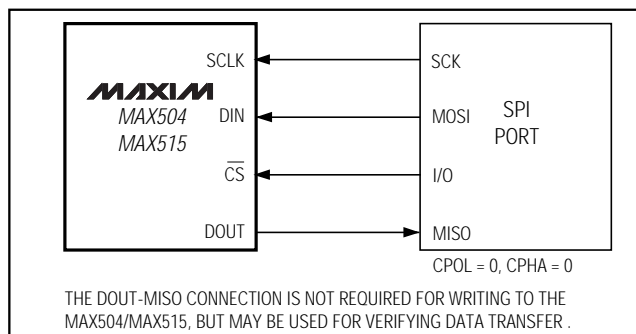


Figure 5. SPI/QSPI Connection

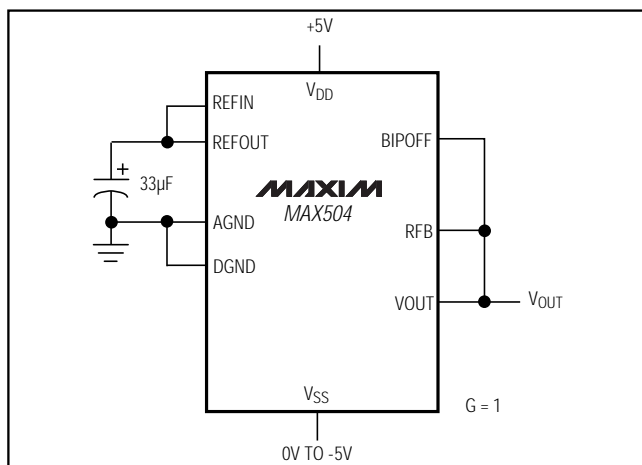


Figure 6. Unipolar Configuration (0V to +2.048V Output)

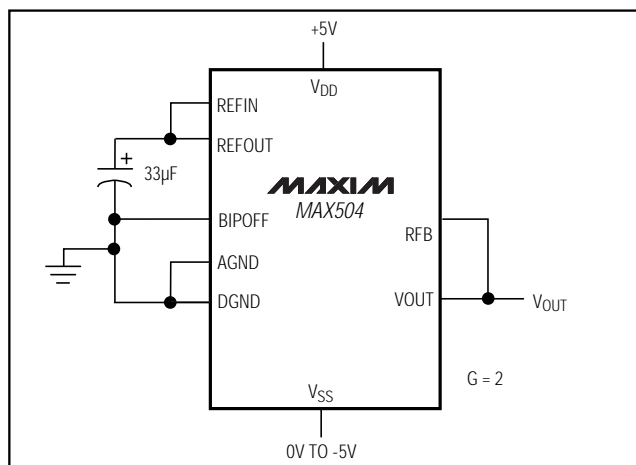


Figure 7. Unipolar Configuration (0V to +4.096V Output)

Table 1. Unipolar Binary Code Table (0V to VREFIN Output), Gain = 1

| INPUT* | OUTPUT |
|------------------|---|
| 1111 1111 11(00) | $(V_{REFIN}) \frac{1023}{1024}$ |
| 1000 0000 01(00) | $(V_{REFIN}) \frac{513}{1024}$ |
| 1000 0000 00(00) | $(V_{REFIN}) \frac{512}{1024} = +V_{REFIN}/2$ |
| 0111 1111 11(00) | $(V_{REFIN}) \frac{511}{1024}$ |
| 0000 0000 01(00) | $(V_{REFIN}) \frac{1}{1024}$ |
| 0000 0000 00(00) | 0V |

* Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

Table 2. Unipolar Binary Code Table (0V to 2VREFIN Output), Gain = 2

| INPUT* | OUTPUT |
|------------------|--|
| 1111 1111 11(00) | $+2 (V_{REFIN}) \frac{1023}{1024}$ |
| 1000 0000 01(00) | $+2 (V_{REFIN}) \frac{513}{1024}$ |
| 1000 0000 00(00) | $+2 (V_{REFIN}) \frac{512}{1024} = +V_{REFIN}$ |
| 0111 1111 11(00) | $+2 (V_{REFIN}) \frac{511}{1024}$ |
| 0000 0000 01(00) | $+2 (V_{REFIN}) \frac{1}{1024}$ |
| 0000 0000 00(00) | 0V |

* Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

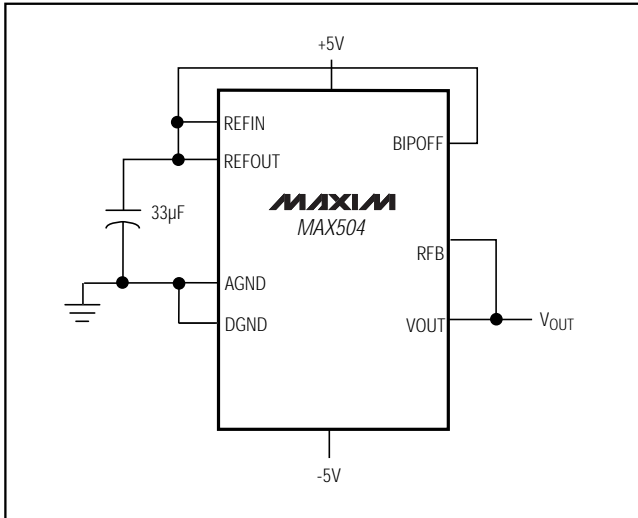


Figure 8. Bipolar Configuration (-2.048V to +2.048V Output)

Single-Supply Linearity

As with any amplifier, the MAX504/MAX515's output buffer offset can be positive or negative. When the offset is positive, it is easily accounted for (Figure 10). However, when the offset is negative, the buffer output cannot follow linearly when there is no negative supply. In that case, the amplifier output (VOUT) remains at ground until the DAC voltage is sufficient to overcome the offset and the output becomes positive.

Normally, linearity is measured after accounting for zero error and gain error. Since, in single-supply operation, the actual value of a negative offset is unknown, it cannot be accounted for during test. Additionally, the output buffer amplifier exhibits a nonlinearity near-zero output when operating with a single supply. To account for this nonlinearity in the MAX504/MAX515, linearity and gain error are measured from code 3 to code 1023. The output buffer's offset and nonlinearity do not affect monotonicity, and these DACs are guaranteed monotonic starting with code zero. In dual-supply operation, linearity and gain error are measured from code 0 to 1023.

Power-Supply Bypassing and Ground Management

Best system performance is obtained with printed circuit boards that use separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be connected together at the low-impedance power-supply source.

Table 3. Bipolar (Offset Binary) Code Table (-VREFIN to +VREFIN Output)

| INPUT* | | | OUTPUT |
|--------|------|--------|---|
| 1111 | 1111 | 11(00) | $(+V_{REFIN}) \frac{511}{512}$ |
| 1000 | 0000 | 01(00) | $(+V_{REFIN}) \frac{1}{512}$ |
| 1000 | 0000 | 00(00) | 0V |
| 0111 | 1111 | 11(00) | $(-V_{REFIN}) \frac{1}{512}$ |
| 0000 | 0000 | 01(00) | $(-V_{REFIN}) \frac{511}{512}$ |
| 0000 | 0000 | 00(00) | $(-V_{REFIN}) \frac{512}{512} = -V_{REFIN}$ |

* Write 10-bit data words with two sub-LSB 0s because the DAC input latch is 12 bits wide.

DGND and AGND should be connected together at the chip. For the MAX504 in single-supply applications, connect VSS to AGND at the chip. The best ground connection may be achieved by connecting the DAC's DGND and AGND pins together and connecting that point to the system analog ground plane. If the DAC's DGND is connected to the system digital ground, digital noise may get through to the DAC's analog portion.

Bypass VDD (and VSS in dual-supply mode) with a 0.1µF ceramic capacitor connected between VDD and AGND (and between VSS and AGND). Mount it with short leads close to the device. Ferrite beads may also be used to further isolate the analog and digital power supplies.

Figures 11a and 11b illustrate the grounding and bypassing scheme described.

Saving Power

When the DAC is not being used by the system, minimize power consumption by setting the appropriate code to minimize load current. For example, in bipolar mode, with a resistive load to ground, set the DAC code to mid-scale (see Table 3). If there is no output load, minimize internal loading on the reference by setting the DAC to all 0s (on the MAX504, use CLR). Under this condition, REFIN is high impedance and the op amp operates at its minimum quiescent current.

Due to these low currents, the output settling time for a zero input code typically increases to 60µs (100µs max).

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

MAX504/MAX515

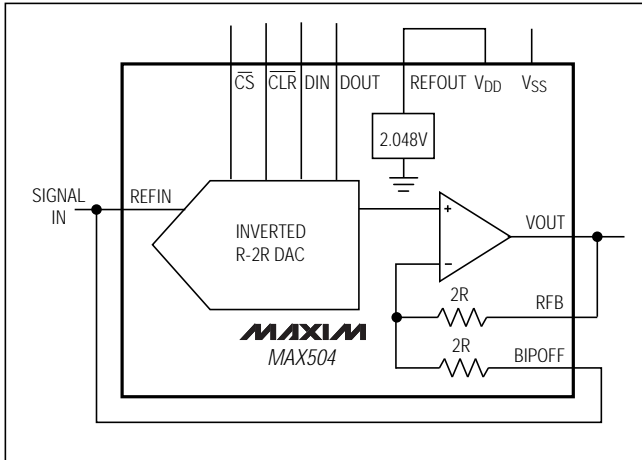


Figure 9. MAX504 Connected as Four-Quadrant Multiplier. The unused REFOUT is connected to VDD.

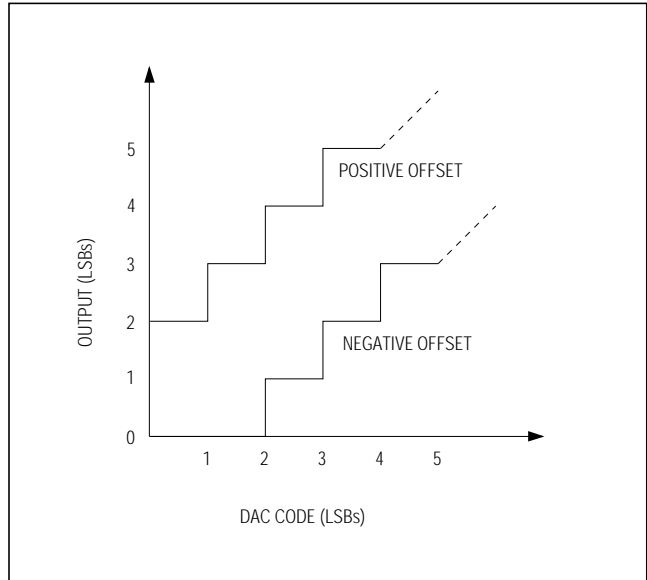


Figure 10. Single-Supply Offset

AC Considerations

Digital Feedthrough

High-speed serial data at any of the digital input or output pins may couple through the DAC package and cause internal stray capacitance to appear at the DAC output as noise, even though \overline{CS} is held high (see *Typical Operating Characteristics*). This digital feedthrough is tested by holding \overline{CS} high transmitting 0101... from DIN to DOUT.

Analog Feedthrough

Because of internal stray capacitance, higher frequency analog input signals may couple to the output as shown in the Analog Feedthrough vs. Frequency graph in the *Typical Operating Characteristics*. It is tested by holding \overline{CS} high, setting the DAC code to all 0s, and sweeping REFIN.

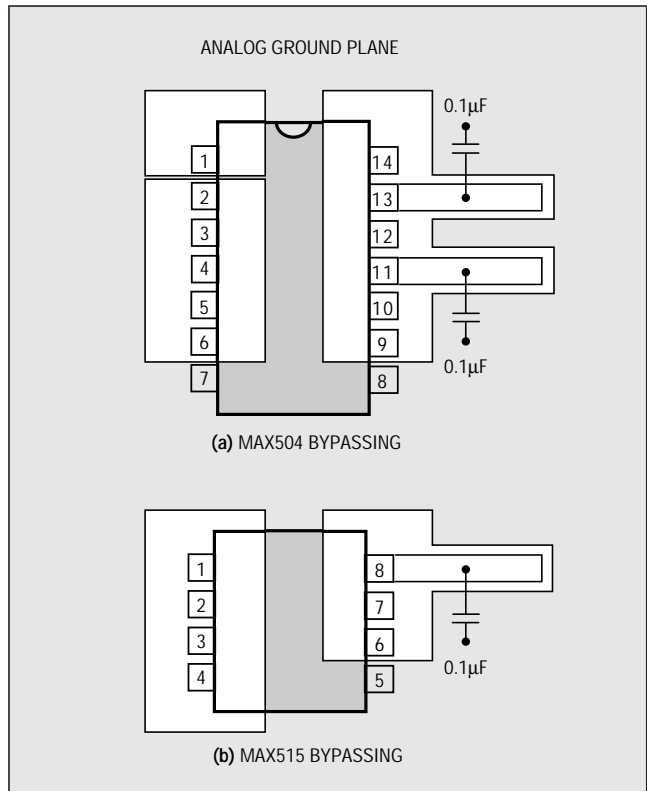


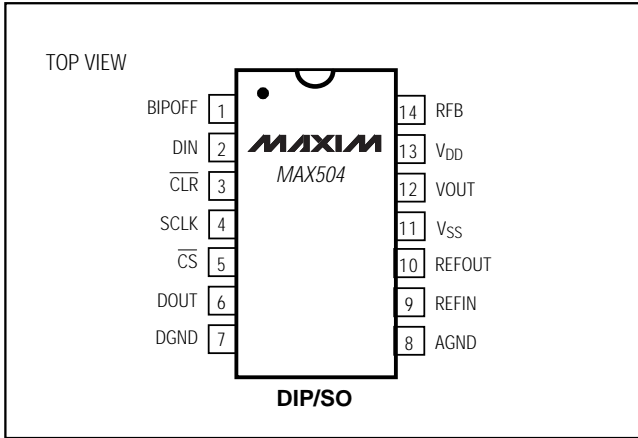
Figure 11. Power-Supply Bypassing

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

Pin Configurations (continued)

Chip Information

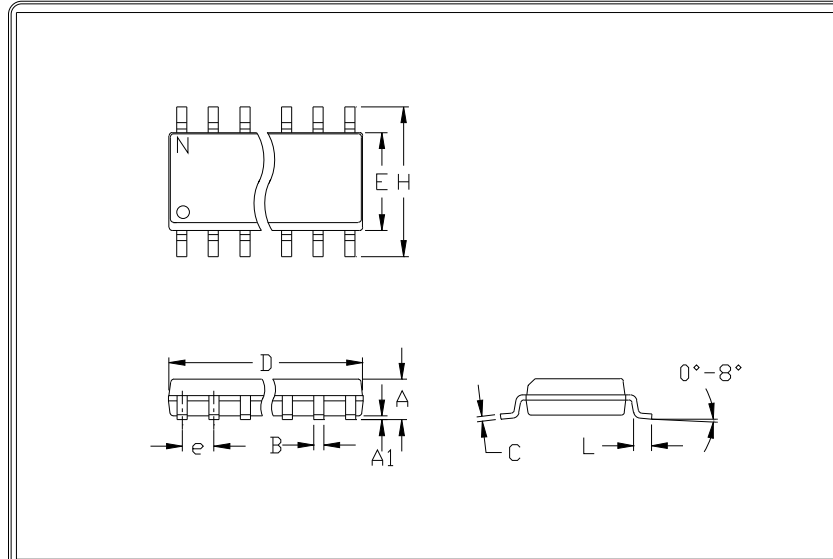
TRANSISTOR COUNT: 922



5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

Package Information

MAX504/MAX515



| | INCHES | | MILLIMETERS | |
|----|--------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 | | 1.27 | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| h | 0.010 | 0.020 | 0.25 | 0.50 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

| | INCHES | | MILLIMETERS | | N | MS012 |
|---|--------|-------|-------------|-------|----|-------|
| | MIN | MAX | MIN | MAX | | |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | A |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | B |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | C |

NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS



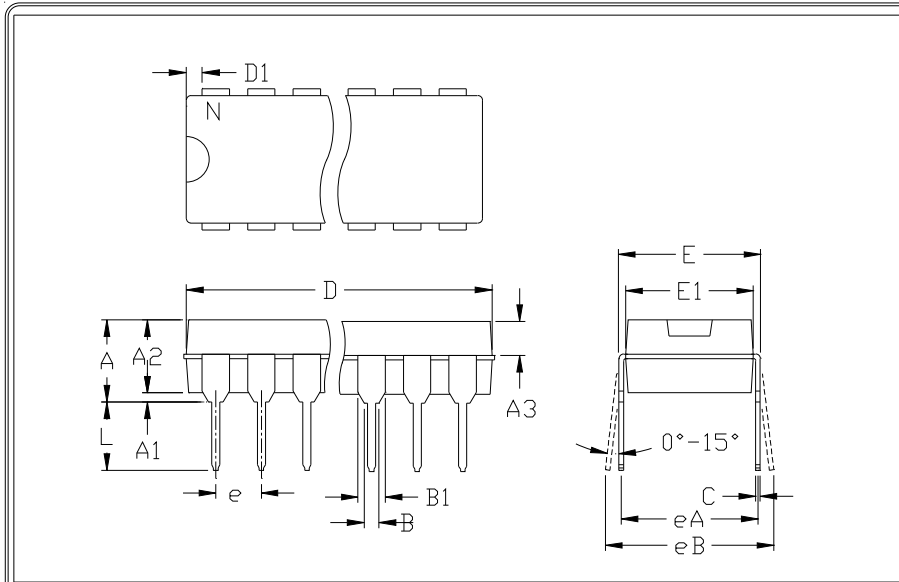
PACKAGE FAMILY OUTLINE: SOIC .150"



21-0041 A
DOCUMENT CONTROL NUMBER REV

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

Package Information (continued)



| | INCHES | | MILLIMETERS | |
|----|--------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 0.200 | --- | 5.08 |
| A1 | 0.015 | --- | 0.38 | --- |
| A2 | 0.125 | 0.175 | 3.18 | 4.45 |
| A3 | 0.055 | 0.080 | 1.40 | 2.03 |
| B | 0.016 | 0.022 | 0.41 | 0.56 |
| B1 | 0.045 | 0.065 | 1.14 | 1.65 |
| C | 0.008 | 0.012 | 0.20 | 0.30 |
| D1 | 0.005 | 0.080 | 0.13 | 2.03 |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.310 | 6.10 | 7.87 |
| e | 0.100 | --- | 2.54 | --- |
| eA | 0.300 | --- | 7.62 | --- |
| eB | --- | 0.400 | --- | 10.16 |
| L | 0.115 | 0.150 | 2.92 | 3.81 |

| | INCHES | | MILLIMETERS | | N | MS001 |
|---|--------|-------|-------------|-------|----|-------|
| | MIN | MAX | MIN | MAX | | |
| D | 0.348 | 0.390 | 8.84 | 9.91 | 8 | AB |
| D | 0.735 | 0.765 | 18.67 | 19.43 | 14 | AC |
| D | 0.745 | 0.765 | 18.92 | 19.43 | 16 | AA |
| D | 0.885 | 0.915 | 22.48 | 23.24 | 18 | AD |
| D | 1.015 | 1.045 | 25.78 | 26.54 | 20 | AE |
| D | 1.14 | 1.265 | 28.96 | 32.13 | 24 | AF |
| D | 1.360 | 1.380 | 34.54 | 35.05 | 28 | *5 |

- NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
 3. CONTROLLING DIMENSION: MILLIMETER
 4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
 5. SIMILAR TO JEDEC MQ-058AB
 6. N = NUMBER OF PINS



PACKAGE FAMILY OUTLINE: PDIP .300"



21-0043 A
DOCUMENT CONTROL NUMBER REV

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