



# THE DATASHEET OF MAX4885EETG+



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MAXIM

# Ultra-Low Capacitance 1:2 VGA Switch with $\pm 15\text{kV}$ ESD

MAX4885E

## General Description

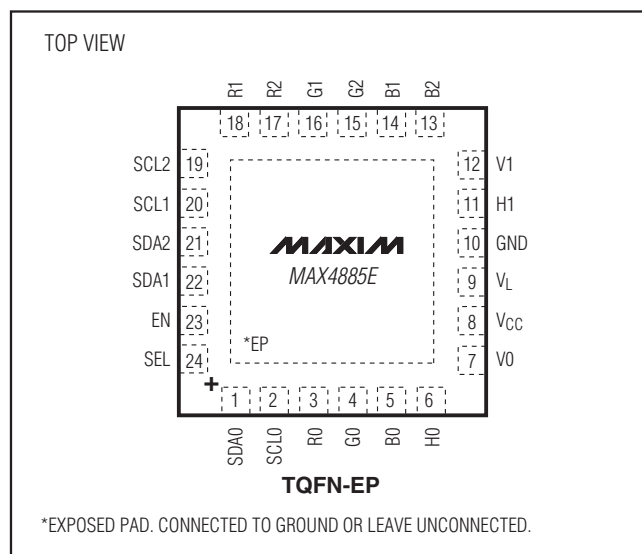
The MAX4885E integrates high-bandwidth analog switches and level-translating buffers to implement a complete 1:2 multiplexer for VGA signals. The device provides switching for RGB, display data channel (DDC), Horizontal and vertical synchronization (HSYNC/VSYNC) inputs feature level-shifting buffers to support low-voltage CMOS or standard TTL-compatible graphics controllers, meeting the VESA requirement of  $\pm 8\text{mA}$ . DDC, consisting of SDA<sub>-</sub> and SCL<sub>-</sub>, is a bidirectional active-level translating switch that reduces capacitive load. The MAX4885E features high ESD protection to  $\pm 15\text{kV}$  Human Body Model (HBM) on all twelve externally routed terminals. See the *Pin Description* section. All other pins are protected to  $\pm 10\text{kV}$  Human Body Model (HBM).

The MAX4885E is specified over the extended  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range, and is available in the 24-pin, 4mm x 4mm TQFN package.

## Applications

Notebook Computers/Docking Stations  
Digital Projectors  
Computer Monitors  
Servers/Storage  
KVM Switches

## Pin Configuration



## Features

- ◆  $\pm 15\text{kV}$  HBM ESD Protection on Externally Routed Terminals
- ◆ 1GHz Bandwidth
- ◆ Low  $5\Omega$  (typ) On-Resistance (R, G, B Signals)
- ◆ Low 6pF (typ) On-Capacitance (R, G, B Signals)
- ◆ Low R, G, B Skew -50ps (typ)
- ◆ Near Zero Power Consumption ( $< 2\mu\text{A}$ )
- ◆ Ultra-Small, 24-Pin (4mm x 4mm) TQFN Package

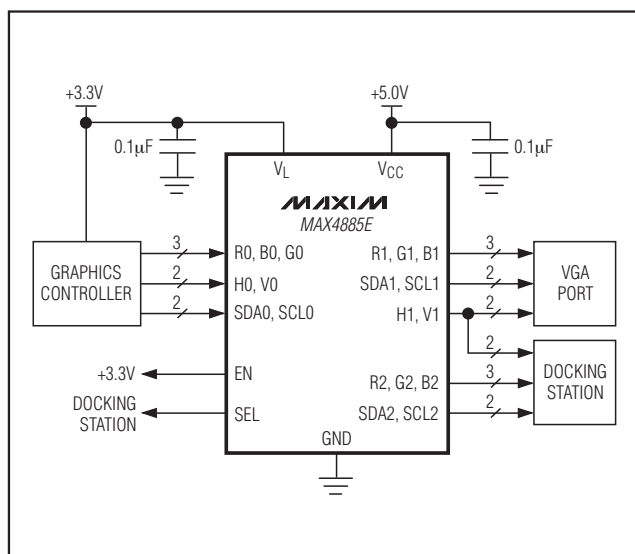
## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4885EETG+	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	24 TQFN-EP*

\*EP = Exposed pad.

+ Denotes lead-free package/RoHS-compliant package.

## Typical Operating Circuit



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# Ultra-Low Capacitance 1:2 VGA Switch with $\pm 15\text{kV}$ ESD

## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

$V_{CC}$ , $V_L$ .....	-0.3V to +6V
$R_-$ , $G_-$ , $B_-$ , SDA1, SCL1, SDA2, SCL2, H1, V1, (Note 1).....	-0.3V to $V_{CC} + 0.3\text{V}$
H0, V0, SDA0, SCL0, EN, SEL.....	-0.3V to $V_L + 0.3\text{V}$
Continuous Current through RGB Switches.....	$\pm 30\text{mA}$
Continuous Current through DDC Switches.....	$\pm 30\text{mA}$
Peak Current through RGB Switches (pulsed at 1ms, 10% duty cycle).....	$\pm 90\text{mA}$
Peak Current through DDC Switches (pulsed at 1ms, 10% duty cycle).....	$\pm 90\text{mA}$

Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )

24-Pin TQFN (derate 27.8mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ ).....	2222mW
Junction to Ambient Thermal Resistance ( $\theta_{JA}$ ) (Note 2) 24-Pin TQFN.....	36 $^\circ\text{C}/\text{W}$
Junction to Ambient Thermal Resistance ( $\theta_{JC}$ ) (Note 2) 24-Pin TQFN.....	3 $^\circ\text{C}/\text{W}$
Operating Temperature Range.....	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Storage Temperature Range.....	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Junction Temperature.....	$+150^\circ\text{C}$
Lead Temperature (soldering, 10s).....	$+300^\circ\text{C}$

**Note 1:** Signals exceeding  $V_{CC}$  or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

**Note 2:** Package thermal resistances were obtained using the method described in JEDEC specifications. For detailed information on package thermal considerations, refer to [www.maxim-ic.com/thermal-tutorial](http://www.maxim-ic.com/thermal-tutorial).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{CC} = +5.0\text{V} \pm 10\%$ ,  $V_L = +2\text{V}$  to  $+5.5\text{V}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = +5.0\text{V}$ ,  $V_L = +3.3\text{V}$  and  $T_A = +25^\circ\text{C}$ .) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CC}$ Quiescent Supply Current	$I_{CC}$	$V_{CC} = +5.0\text{V}$ EN = $V_L$ EN = GND			1	$\mu\text{A}$
$V_L$ Quiescent Supply Current	$I_{VL}$	$V_L = +3.3\text{V}$ EN = $V_L$ EN = GND			1	$\mu\text{A}$
<b>RGB ANALOG SWITCHES</b>						
On-Resistance	$R_{ON}$	$V_{CC} = +5.0\text{V}$ , $I_{IN} = -10\text{mA}$ , $V_{IN} = +0.7\text{V}$ (Note 4)		6		$\Omega$
On-Resistance Matching	$\Delta R_{ON}$	$0 \leq V_{IN} \leq 0.7\text{V}$ , $I_{IN} = -10\text{mA}$		0.5		$\Omega$
On-Resistance Flatness	$R_{FLAT(ON)}$	$0 \leq V_{IN} \leq 0.7\text{V}$ , $I_{IN} = -10\text{mA}$		0.5		$\Omega$
Off-Leakage Current	$I_{L(OFF)}$	$V_{CC} = +5.5\text{V}$ , $V_{IN} = +0.3\text{V}$ or $+5.5\text{V}$ , $V_{EN} = 0$ or $V_L$	-1		+1	$\mu\text{A}$
On-Leakage Current	$I_{L(ON)}$	$V_{CC} = +5.5\text{V}$ , $V_{IN} = +0.3\text{V}$ or $+5.5\text{V}$ , $V_{EN} = V_L$	-1		+1	$\mu\text{A}$
<b>HV BUFFER</b>						
Input Voltage Low	$V_{ILHV}$				$0.33 \times V_L$	V
Input Voltage High	$V_{IHV}$		$0.66 \times V_L$			V
Input Logic Hysteresis	$V_{HYST}$			75		mV
Input Leakage Current	$I_{INH}$	$V_{CC} = +5.5\text{V}$ , $V_L = +5.5\text{V}$ , $V_{IN} = 0$ or $V_L$	-1		+1	$\mu\text{A}$
High-Output Drive Current	$I_{OHV}$	$V_{OHV} \geq 3.0\text{V}$	8.0			mA
Low-Output Drive Current	$I_{OLV}$	$V_{OLV} \leq 0.6\text{V}$	8.0			mA

# Ultra-Low Capacitance 1:2 VGA Switch with $\pm 15\text{kV}$ ESD

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +5.0\text{V} \pm 10\%$ ,  $V_L = +2\text{V}$  to  $+5.5\text{V}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = +5.0\text{V}$ ,  $V_L = +3.3\text{V}$  and  $T_A = +25^\circ\text{C}$ .) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SDA_, SCL_</b>						
Supply Voltage	$V_L$		2.0		5.5	V
On-Resistance	$R_{ON}$	$V_{IN} = +0.4\text{V}$ , $I_{IN} = \pm 2\text{mA}$ , $V_L = +2.0\text{V}$		10		$\Omega$
On-Capacitance	$C_{ON}$	$f = 100\text{kHz}$		15		pF
High-Impedance Input Leakage Current	$I_{INHIZ}$	EN = GND, $V_{CC} = +5.5\text{V}$ , $V_L = +3.6\text{V}$ , SCL0, SDA0, SCL1, SCL2, SDA1, SDA2 = GND or $V_L$ (Note 5)	-1		+1	$\mu\text{A}$
Off-Input Leakage Current	$I_{INOFF}$	EN = $V_L$ , $V_L = +3.6\text{V}$ , $V_{IN} = V_L - 0.2\text{V}$	-1		+1	$\mu\text{A}$
<b>CONTROL LOGIC (SEL, EN)</b>						
Input Voltage Low	$V_{ILLOG}$				$0.33 \times V_L$	V
Input Voltage High	$V_{IHLOG}$		$0.66 \times V_L$			V
Input Logic Hysteresis	$V_{HYST}$			75		mV
Input Leakage Current	$I_{INLEK}$	$V_{CC} = +5.5\text{V}$ , $V_L = +3.6\text{V}$ , $V_{IN} = 0$ or $V_L$	-1		+1	$\mu\text{A}$
<b>ESD PROTECTION</b>						
ESD Protection		Human Body Model; R1, G1, B1, R2, G2, B2, SDA1, SCL1, SDA2, SCL2, H1, V1		$\pm 15$		kV
		Human Body Model; all other pins		$\pm 10$		

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +5.0\text{V} \pm 10\%$ ,  $V_L = +2\text{V}$  to  $+5.5\text{V}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = +5.0\text{V}$ ,  $V_L = +3.3\text{V}$  and  $T_A = +25^\circ\text{C}$ .) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bandwidth	$f_{MAX}$	$R_S = R_L = 50\Omega$		1		GHz
Insertion Loss	$I_{LOS}$	$f = 1\text{MHz}$ , $R_S = R_L = 50\Omega$ , Figure 1		0.6		dB
Crosstalk	$V_{CT}$	$f = 50\text{MHz}$ , $R_S = R_L = 50\Omega$ , Figure 1		-40		dB
Off-Capacitance	$C_{OFF}$	$f = 250\text{MHz}$		4.5		pF
On-Capacitance	$C_{ON}$	$f = 250\text{MHz}$		6.4		pF

# Ultra-Low Capacitance 1:2 VGA Switch with ±15kV ESD

## TIMING CHARACTERISTICS

( $V_{CC} = +5.0V \pm 10\%$ ,  $V_L = +2V$  to  $+5.5V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = +5.0V$ ,  $V_L = +3.3V$  and  $T_A = +25^\circ C$ .) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>RGB ANALOG SWITCHES</b>						
Output Skew Between Ports	t <sub>SKEW</sub>	Skew between any two ports: R <sub>-</sub> , G <sub>-</sub> , B <sub>-</sub> , Figure 2		50		ps
<b>HV BUFFER</b>						
Propagation Delay	t <sub>PD</sub>	R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 10pF, Figure 2		15		ns

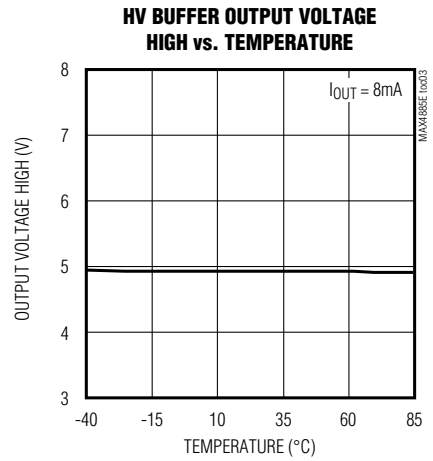
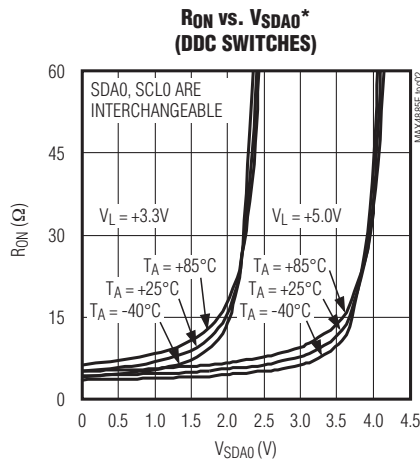
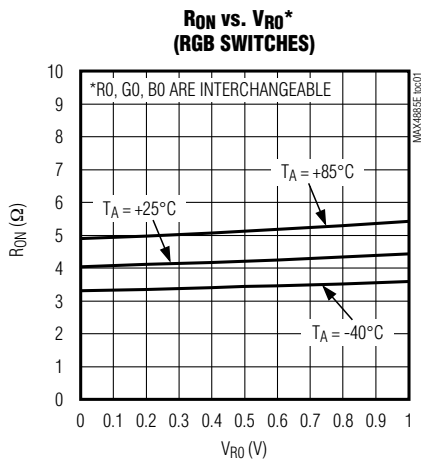
**Note 3:** All devices are 100% production tested at  $T_A = +25^\circ C$ . Specifications over the full temperature range are guaranteed by design.

**Note 4:** On-resistance guarantees the low-static logic level.

**Note 5:** SDA<sub>-</sub>, SCL<sub>-</sub> off-input leakage current guarantees the high-static logic level.

## Typical Operating Characteristics

( $V_{CC} = +5.0V$ ,  $V_L = +3.3V$  and  $T_A = +25^\circ C$ , unless otherwise noted.)

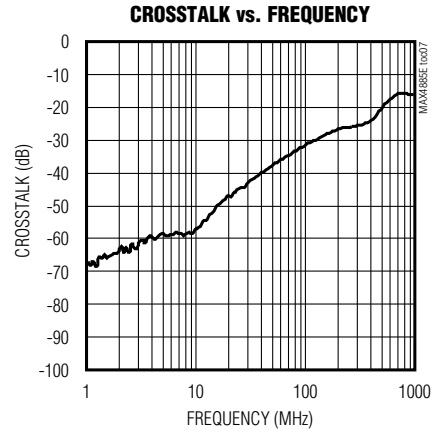
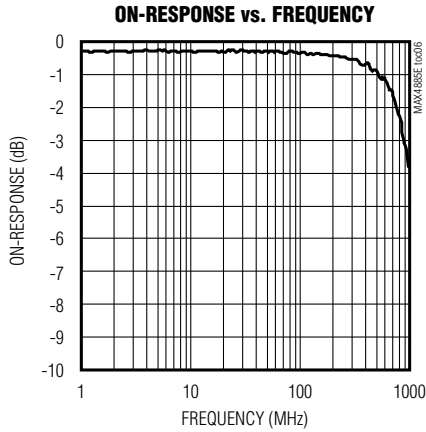
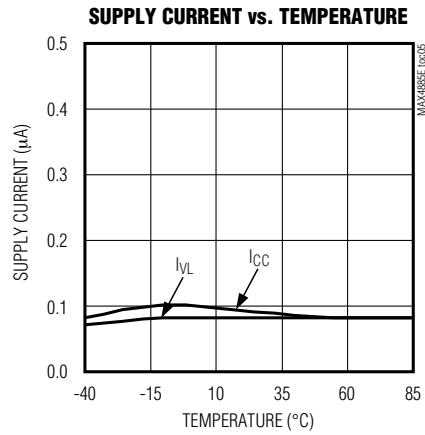
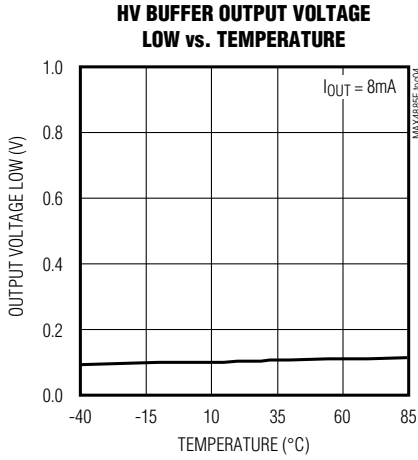


# Ultra-Low Capacitance 1:2 VGA Switch with $\pm 15\text{kV}$ ESD

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## Typical Operating Characteristics (continued)

( $V_{CC} = +5.0\text{V}$ ,  $V_L = +3.3\text{V}$  and  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# Ultra-Low Capacitance 1:2 VGA Switch with ±15kV ESD

## Timing Circuits/Timing Diagrams

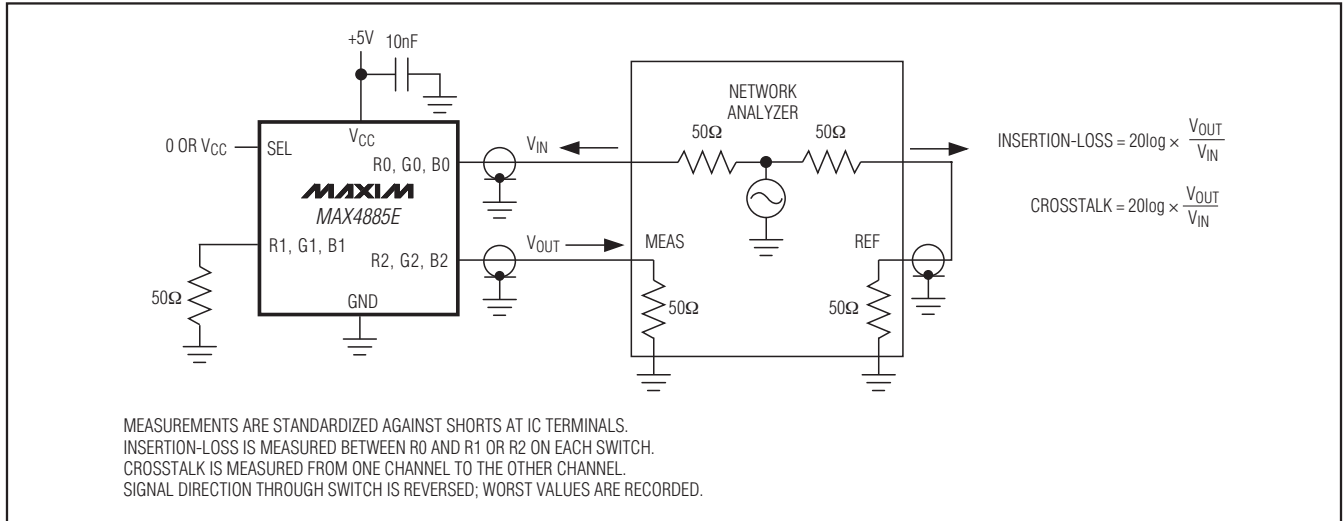


Figure 1. Insertion-Loss and Crosstalk

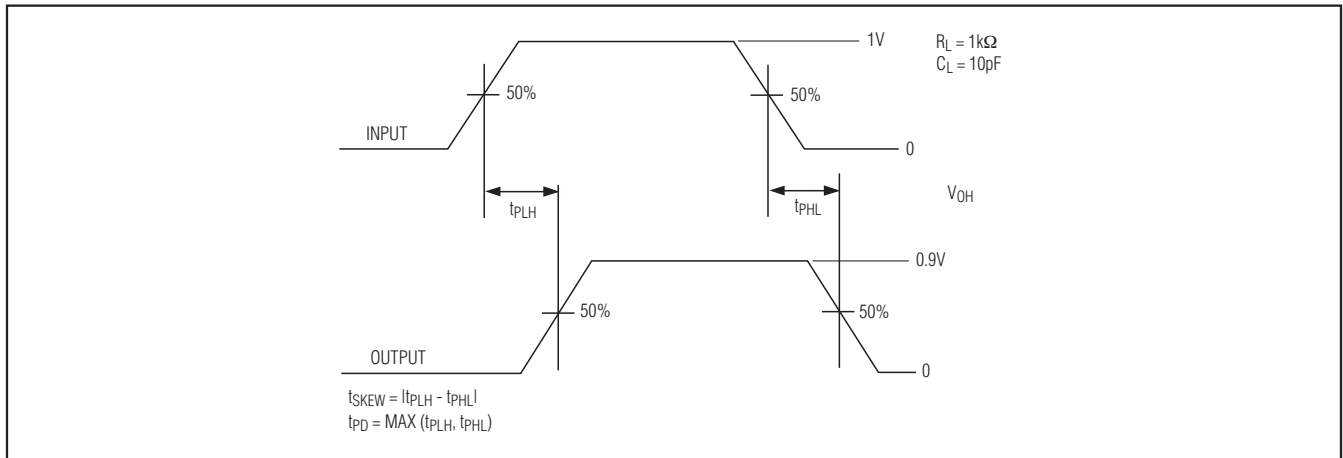


Figure 2. Propagation Delay and Skew Waveforms

# Ultra-Low Capacitance 1:2 VGA Switch with $\pm 15\text{kV}$ ESD

## Pin Description

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PIN	NAME	FUNCTION
1	SDA0	SDA I/O
2	SCL0	SCL I/O
3	R0	RGB Analog I/O
4	G0	RGB Analog I/O
5	B0	RGB Analog I/O
6	H0	Horizontal Sync Input
7	V0	Vertical Sync Input
8	V <sub>CC</sub>	Supply Voltage. V <sub>CC</sub> = +5.0V $\pm 10\%$ . Bypass V <sub>CC</sub> to GND with a 0.1 $\mu$ F or larger ceramic capacitor.
9	V <sub>L</sub>	Supply Voltage. +2V $\leq$ V <sub>L</sub> $\leq$ +5.5V. Bypass V <sub>L</sub> to GND with a 0.1 $\mu$ F or larger ceramic capacitor.
10	GND	Ground
11	H1	Horizontal Sync Output*
12	V1	Vertical Sync Output*
13	B2	RGB Analog I/O*
14	B1	RGB Analog I/O*
15	G2	RGB Analog I/O*
16	G1	RGB Analog I/O*
17	R2	RGB Analog I/O*
18	R1	RGB Analog I/O*
19	SCL2	SCL I/O*
20	SCL1	SCL I/O*
21	SDA2	SDA I/O*
22	SDA1	SDA I/O*
23	EN	Enable Input. Drive EN high for normal operation. Drive EN low to disable the device.
24	SEL	Select Input. Logic input for switching RGB and DDC switches.
—	EP	Exposed Pad. Connect exposed pad to ground or leave unconnected.

\*Terminal as  $\pm 15\text{kV}$  ESD protection—Human Body Model.

### Detailed Description

The MAX4885E integrates high-bandwidth analog switches and level-translating buffers to implement a complete 1:2 multiplexer for VGA signals. The device provides switching for RGB, HSYNC, VSYNC, SDA\_ and SCL\_ signals.

The HSYNC and VSYNC inputs feature level-shifting buffers to support TTL output logic levels from low-voltage graphics controllers. These buffered switches may be driven from as little as +2.0V up to +5.5V. RGB signals are routed with the same high-performance analog switches, and SDA\_, SCL\_ signals are voltage clamped to a diode drop less than V<sub>L</sub>. Voltage clamping provides protection and compatibility with SDA\_ and SCL\_ signals and low-voltage ASICs. In keyboard/video/

mouse (KVM) applications, V<sub>L</sub> is normally set to +5V because low-voltage clamping is not required, as specified by the VESA standard.

Drive EN logic-low to shut down the MAX4885E. In shutdown mode, all switches are high impedance, providing high-signal rejection. The RGB, HSYNC, VSYNC, SDA\_, and SCL\_ outputs are ESD protected to  $\pm 15\text{kV}$  by the Human Body Model.

### RGB Switches

The MAX4885E provides three SPDT high-bandwidth switches to route standard VGA R, G, and B signals (see Table 1). The R, G, and B analog switches are identical, and any of the three switches can be used to route red, green, or blue video signals.

# Ultra-Low Capacitance 1:2 VGA Switch with $\pm 15\text{kV}$ ESD

**Table 1. RGB Truth Table**

EN	SEL	FUNCTION
1	0	R0 to R1 G0 to G1 B0 to B1
1	1	R0 to R2 G0 to G2 B0 to B2
0	X	R <sub>+</sub> , B <sub>+</sub> , and G <sub>+</sub> , high impedance

X = Don't care.

**Table 2. HV Truth Table**

EN	FUNCTION
0	H <sub>+</sub> , V <sub>+</sub> = 0

X = Don't care.

**Table 3. DDC Truth Table**

EN	SEL	FUNCTION
1	0	SDA0 to SDA1 SCL0 to SCL1
1	1	SDA0 to SDA2 SCL0 to SCL2
0	X	SDA <sub>+</sub> , SCL <sub>+</sub> , high impedance

X = Don't care.

## Horizontal/Vertical Sync Level Shifter

HSYNC/VSYNC are buffered to provide level shifting and drive capability to meet the VESA specification.

## Display-Data Channel Multiplexer

The MAX4885E provides two voltage-clamped switches to route DDC signals (see Table 3). Each switch clamps signals to a diode drop less than the voltage applied on V<sub>L</sub>. Supply +3.3V on V<sub>L</sub> to provide voltage clamping for VESA I<sup>2</sup>C-compatible signals. If voltage clamping is not required, connect V<sub>L</sub> to V<sub>CC</sub>. The SDA<sub>+</sub> and SCL<sub>+</sub> switches are identical, and each switch can be used to route either SDA<sub>+</sub> and SCL<sub>+</sub> signals.

## ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. Additionally, the MAX4885E is protected to  $\pm 15\text{kV}$  on RGB, HSYNC, VSYNC, SDA<sub>+</sub> and SCL<sub>+</sub>

outputs by the Human Body Model (HBM). See the *Pin Description* section. For optimum ESD performance, bypass each V<sub>CC</sub> pin to ground with a 0.1 $\mu\text{F}$  or larger ceramic capacitor.

## Human Body Model (HBM)

Several ESD testing standards exist for measuring the robustness of ESD structures. The ESD protection of the MAX4885E is characterized with the Human Body Model. Figure 3 shows the model used to simulate an ESD event resulting from contact with the human body. The model consists of a 100pF storage capacitor that is charged to a high voltage, then discharged through a 1.5k $\Omega$  resistor. Figure 4 shows the current waveform when the storage capacitor is discharged into a low impedance.

## ESD Test Conditions

ESD performance depends on a variety of conditions. Please contact Maxim for a reliability report documenting test setup, methodology, and results.

## Applications Information

The MAX4885E provides the level shifting necessary to drive two standard VGA ports from a graphics controller as low as +2.2V. Internal buffers drive the HSYNC and VSYNC signals to VGA standard TTL levels. The DDC multiplexer provides level shifting by clamping signals to a diode drop less than V<sub>L</sub> (see the *Typical Operating Circuit*). Connect V<sub>L</sub> to +3.3V for normal operation, or to V<sub>CC</sub> to disable voltage clamping for DDC signals.

## Power-Supply Decoupling

Bypass each V<sub>CC</sub> pin and V<sub>L</sub> to ground with a 0.1 $\mu\text{F}$  or larger ceramic capacitor as close as possible to the device.

## PCB Layout

High-speed switches such as the MAX4885E require proper PCB layout for optimum performance. Ensure that impedance-controlled PCB traces for high-speed signals are matched in length and as short as possible. Connect the exposed pad to a solid ground plane.

## Chip Information

PROCESS: BiCMOS

# Ultra-Low Capacitance 1:2 VGA Switch with $\pm 15\text{kV}$ ESD

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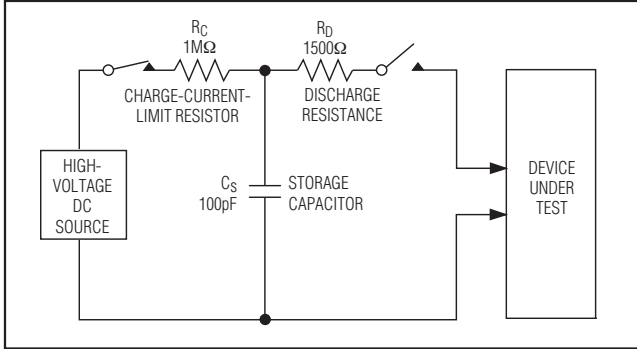


Figure 3. Human Body ESD Test Model

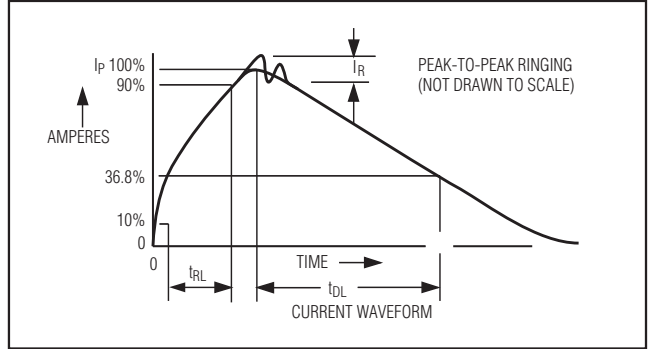
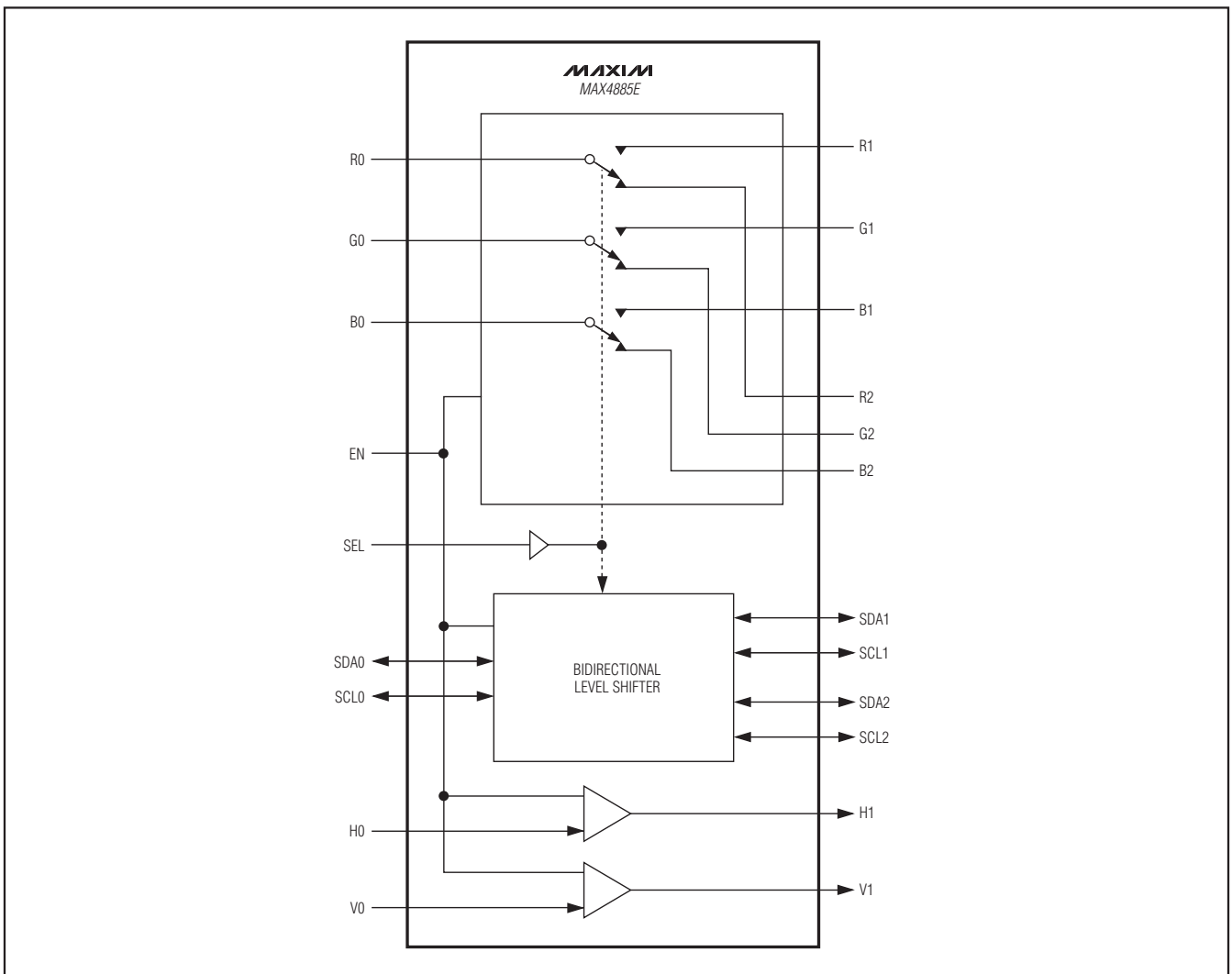


Figure 4. HBM Discharge Current Waveform

## Functional Diagram



# Ultra-Low Capacitance 1:2 VGA Switch with $\pm 15\text{kV}$ ESD

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).



PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
24 TQFN-EP	T2444-4	<a href="#">21-0139</a>

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