

Two-Channel, Triple/Quad RGB Video Switches and Buffers

ABSOLUTE MAXIMUM RATINGS

Power-Supply Ranges	24-Pin Narrow Plastic DIP
V+ to V- 12V	(derate 20.2mW/°C above +70°C) 1620mW
Analog Input Voltage (V- - 0.3V) to (V+ + 0.3V)	24-Pin Wide SO (derate 19.3mW/°C above +70°C) 1590mW
Digital Input Voltage -0.3V to (V+ + 0.3V)	28-Pin Narrow Plastic DIP
Output Short-Circuit Duration (to GND) 1 Minute	(derate 20.2mW/°C above +70°C) 1620mW
Input Current into Any Pin, Power On or Off ±50mA	28-Pin Wide SO (derate 18.1mW/°C above +70°C) 1440mW
Continuous Power Dissipation (T _A = +70°C)	Operating Temperature Ranges
16-Pin Plastic DIP (derate 22.22mW/°C above +70°C) 1778mW	MAX4__C_ 0°C to +70°C
16-Pin Wide SO (derate 20.00mW/°C above +70°C) 1600mW	MAX4__E_ -40°C to +85°C
	Storage Temperature Range -65°C to +150°C
	Lead Temperature (soldering, 10sec) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, -2V ≤ V_{IN} ≤ +2V, R_{LOAD} = 75Ω, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T _A = +25°C			T _A = T _{MIN} to T _{MAX}		UNITS
			MIN	TYP	MAX	MIN	MAX	
Operating Supply Voltage	V _S		±4.75	±5	±5.25	±4.75	±5.25	V
Input Voltage Range	V _{IN}		-2		2	-2	2	V
Offset Voltage	V _{OS}			±3	±10		±15	mV
Power-Supply Rejection Ratio	PSRR		50	60		50		dB
On Input Bias Current	I _{BIAS}			±1	±3		±5	μA
On Input Resistance	R _{IN}		300	700		150		kΩ
Input Capacitance	C _{IN}	Channel off or on		5				pF
Voltage-Gain Accuracy		MAX463/MAX464, MAX467/MAX468 (Note 1)		0.2	0.5		1.0	%
		MAX465/MAX466, MAX469/MAX470, R _{LOAD} = 150Ω, (Note 2)		0.3	1.0		2.0	
Output Voltage Swing	V _{OUT}	R _{LOAD} = 150Ω	±2.5	±2.8		±2.5		V
		R _{LOAD} = 75Ω	±2.0	±2.4		-1.5/+2		
Output Impedance	R _{OUT}	f _{IN} = 10MHz		5				Ω
		f _{IN} = DC	MAX463/MAX464, MAX467/MAX468		0.05			
			MAX465/MAX466, MAX469/MAX470		0.1			
Output Resistance, Disabled Mode	R _{OUTD}	MAX463/MAX464	150	250		100		kΩ
		MAX465/MAX466	0.7	1		0.7		kΩ
Output Capacitance, Disabled Mode	C _{OUTD}	MAX463-MAX466		10				pF
Positive Supply Current	I+	MAX463/MAX465/MAX467/MAX469, V _{IN} = 0V		65	80		100	mA
		MAX464/MAX466/MAX468/MAX470, V _{IN} = 0V		85	100		120	
		MAX463/MAX465, disabled mode		35	45		50	
		MAX464/MAX466, disabled mode		40	50		55	

Two-Channel, Triple/Quad RGB Video Switches and Buffers

MAX463-MAX470

ELECTRICAL CHARACTERISTICS (continued)

(V₊ = 5V, V₋ = -5V, -2V ≤ V_{IN} ≤ +2V, R_{LOAD} = 75Ω, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T _A = +25°C			T _A = T _{MIN} to T _{MAX}		UNITS
			MIN	TYP	MAX	MIN	MAX	
Negative Supply Current	I ₋	MAX463/MAX465/MAX467/MAX469, V _{IN} = 0V	50	65		75	mA	
		MAX464/MAX466/MAX468/MAX470, V _{IN} = 0V	65	80		95		
		MAX463/MAX465, disabled mode	20	30		35		
		MAX464/MAX466, disabled mode	25	35		40		
Input Noise Density	en	f _{IN} = 10kHz	20				nV/√Hz	
Slew Rate	SR	MAX463/MAX464, MAX467/MAX468	200				V/μs	
		MAX465/MAX466, MAX469/MAX470	300					
-3dB Bandwidth	BW	MAX463/MAX464, MAX467/MAX468	100				MHz	
		MAX465/MAX466, MAX469/MAX470	90					
Differential Gain Error (Note 3)	DG	MAX463/MAX464, MAX467/MAX468	0.01				%	
		MAX465/MAX466, MAX469/MAX470	0.12					
Differential Phase Error (Note 3)	DP	MAX463/MAX464, MAX467/MAX468	0.03				deg.	
		MAX465/MAX466, MAX469/MAX470	0.14					
Settling Time to 0.1%	t _s	V _{IN} = 2V-to-0V step	50				ns	
Adjacent Channel Crosstalk (Note 4)	XTALK	f _{IN} = 10MHz	60				dB	
All-Hostile Crosstalk (Note 5)	XTALK	f _{IN} = 10MHz	50				dB	
All-Hostile Off Isolation (Note 6)	ISO	f _{IN} = 10MHz, MAX463-MAX466	70				dB	
Channel Switching Propagation Delay (Note 7)	t _{PD}	MAX463-MAX466	15				ns	
Channel Switching Time (Note 8)	t _{SW}	MAX463-MAX466	20				ns	
Switching Transient		V _{INA} = V _{INB} = 0V, MAX463-MAX466	300				mVp-p	
Amplifier Switching Off-Time (Note 9)	t _{OFF}	MAX463-MAX466	80				ns	
Amplifier Switching On-Time (Note 10)	t _{ON}	MAX463-MAX466	100				ns	
Logic Input High Threshold	V _{IH}	\overline{EN} , A0, \overline{CS} , LE; MAX463-MAX466		2		2	V	
Logic Input Low Threshold	V _{IL}	\overline{EN} , A0, \overline{CS} , LE; MAX463-MAX466	0.8			0.8	V	
Logic Input Current High	I _{INH}	\overline{EN} , A0, \overline{CS} , LE; MAX463-MAX466		200		200	μA	
Logic Input Current Low	I _{INLO}	\overline{EN} , A0, \overline{CS} , LE; MAX463-MAX466		200		200	μA	

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ELECTRICAL CHARACTERISTICS (continued)

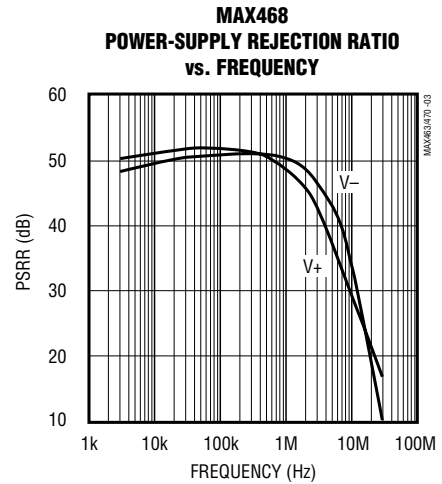
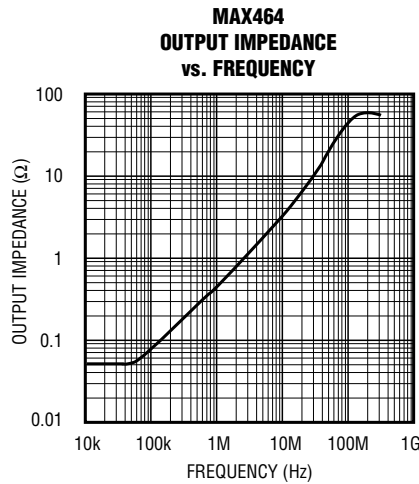
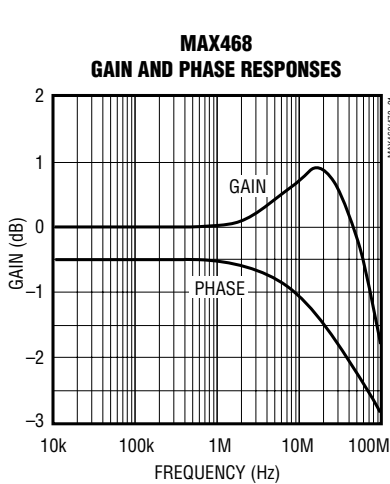
($V_+ = 5V$, $V_- = -5V$, $-2V \leq V_{IN} \leq +2V$, $R_{LOAD} = 75\Omega$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	$T_A = +25^\circ C$			$T_A = T_{MIN}$ to T_{MAX}		UNITS
			MIN	TYP	MAX	MIN	MAX	
Address Setup Time (Note 11)	t_{SU}	\overline{EN} , A0, \overline{CS} , LE; MAX463-MAX466	30			30		ns
Address Hold Time (Note 11)	t_H	\overline{EN} , A0, \overline{CS} , LE; MAX463-MAX466		0		0		ns
\overline{CS} Pulse Width Low (Note 11)	t_{CS}	\overline{EN} , A0, \overline{CS} , LE; MAX463-MAX466	15			15		ns

- Note 1:** Voltage gain accuracy for the unity-gain devices is defined as $[(V_{OUT} - V_{IN})$ at $V_{IN} = 1V - (V_{OUT} - V_{IN})$ at $V_{IN} = -1V]/2$.
- Note 2:** Voltage gain accuracy for the gain-of-two devices is defined as $[(V_{OUT}/2 - V_{IN})$ at $V_{IN} = 1V - (V_{OUT}/2 - V_{IN})$ at $V_{IN} = -1V]/2$.
- Note 3:** Tested with a 3.58MHz sine wave of amplitude 40IRE superimposed on a linear ramp (0IRE to 100IRE), $R_L = 150\Omega$ to ground.
- Note 4:** Tested with the selected input connected to ground through a 75Ω resistor, and a $4V_{P-P}$ sine wave at 10MHz driving adjacent input.
- Note 5:** Tested in the same manner as described in Note 4, but with all other inputs driven.
- Note 6:** Tested with $LE = 0V$, $EN = V_+$, and all inputs driven with a $4V_{P-P}$, 10MHz sine wave.
- Note 7:** Measured from a channel switch command to measurable activity at the output.
- Note 8:** Measured from where the output begins to move to the point where it is well defined.
- Note 9:** Measured from a disable command to amplifier in a non-driving state.
- Note 10:** Measured from an enable command to the point where the output reaches 90% current out.
- Note 11:** Guaranteed by design.

Typical Operating Characteristics

($T_A = +25^\circ C$, unless otherwise noted.)

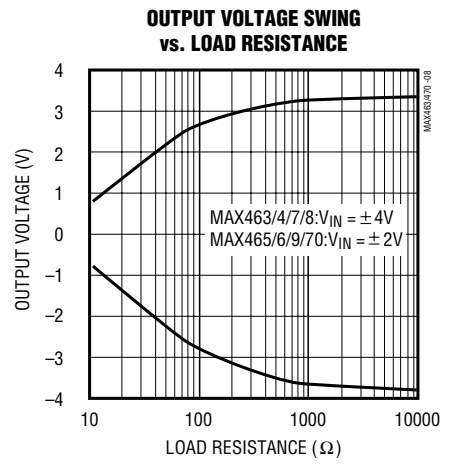
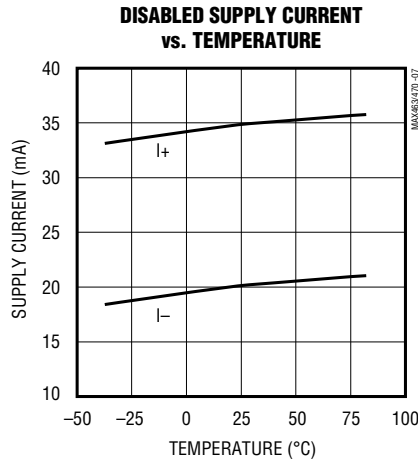
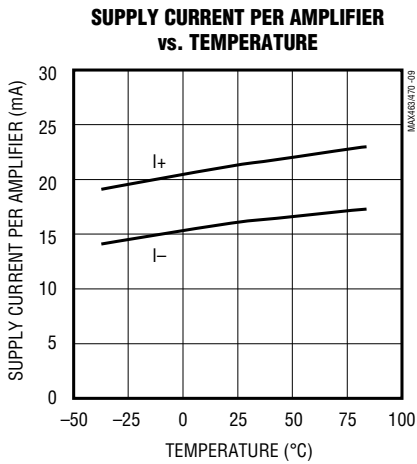
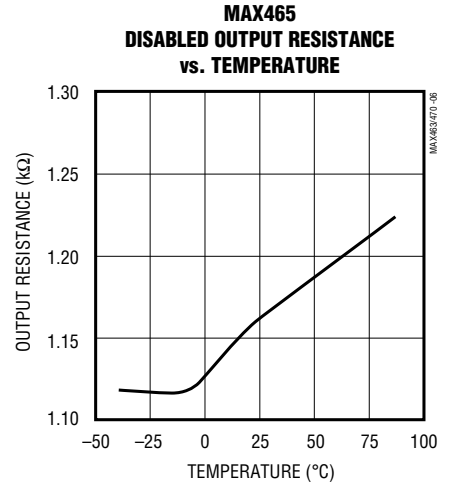
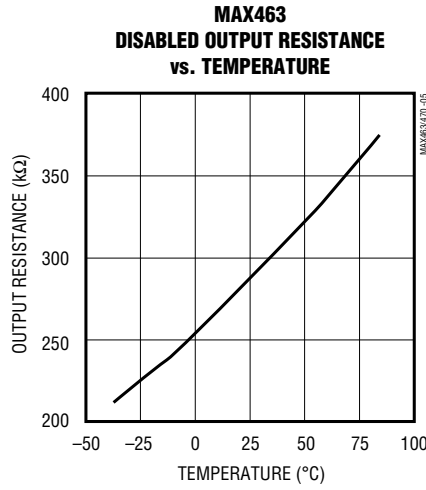
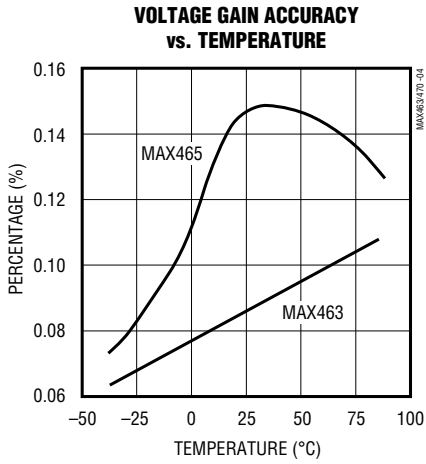


Two-Channel, Triple/Quad RGB Video Switches and Buffers

MAX463-MAX470

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

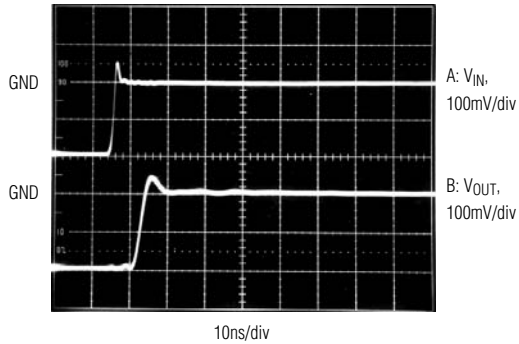


Two-Channel, Triple/Quad RGB Video Switches and Buffers

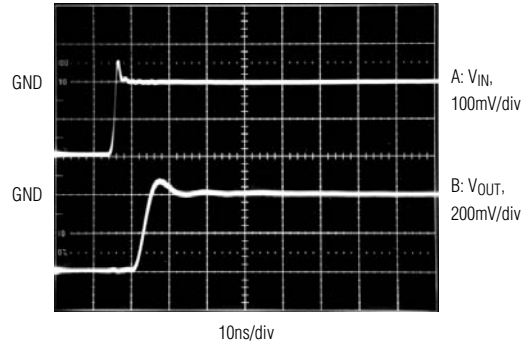
Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

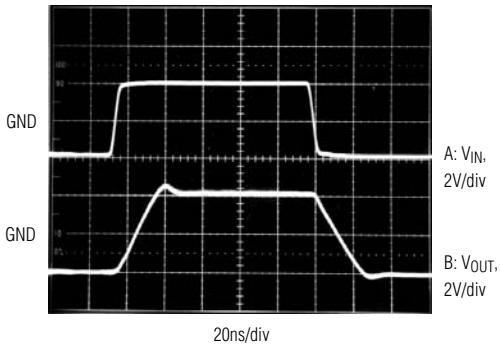
MAX464
SMALL-SIGNAL STEP RESPONSE



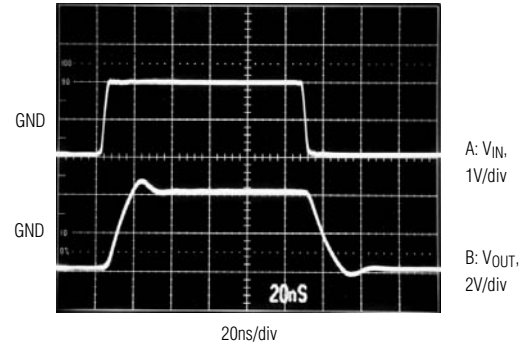
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SMALL-SIGNAL STEP RESPONSE



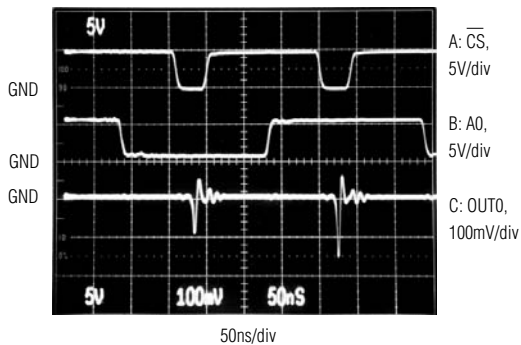
MAX464
LARGE-SIGNAL STEP RESPONSE



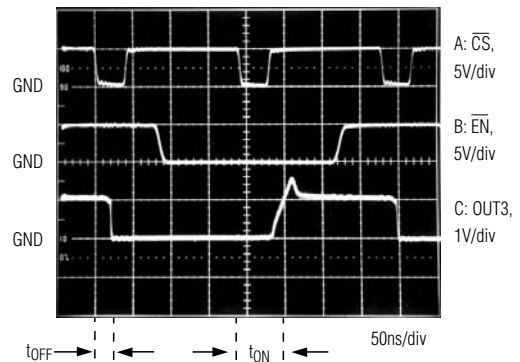
MAX466
LARGE-SIGNAL STEP RESPONSE



MAX464
OUTPUT TRANSIENT WHEN SWITCHING
BETWEEN TWO GROUNDED INPUTS



MAX464
 \overline{EN} RESPONSE TIME



Two-Channel, Triple/Quad RGB Video Switches and Buffers

Pin Descriptions

MAX463-MAX470

PIN		NAME	FUNCTION
MAX463/MAX465	MAX464/MAX466		
1	28	IN0A	Channel A, Analog Input 0
2, 4, 9, 11, 15, 24	1, 3, 5, 11, 13, 19	GND	Analog Ground
3	2	IN1A	Channel A, Analog Input 1
5	4	IN2A	Channel A, Analog Input 2
–	6	IN3A	Channel A, Analog Input 3
6, 7, 19	7, 9, 21, 23	V-	Negative Power-Supply Input. Connect to -5V. Thermal path.
8	8	IN0B	Channel B, Analog Input 0
10	10	IN1B	Channel B, Analog Input 1
12	12	IN2B	Channel B, Analog Input 2
–	14	IN3B	Channel B, Analog Input 3
–	15	OUT3	Buffered Analog Output 3
13	17	OUT2	Buffered Analog Output 2
14, 17	16, 18	V+	Positive Power-Supply Input. Connect to +5V.
16	20	OUT1	Buffered Analog Output 1
18	22	OUT0	Buffered Analog Output 0
20	24	\overline{CS}	Chip-Select—latch control for the digital inputs. When \overline{CS} is low, A0 and \overline{EN} input registers are transparent. When \overline{CS} goes high, the A0 input register latches. If LE is high, the \overline{EN} input register also latches when \overline{CS} goes high (see LE).
21	25	A0	Channel-Select Input. When \overline{CS} is low, driving A0 low selects channel A and driving A0 high selects channel B.
22	26	\overline{EN}	Buffer-Enable Input. When \overline{CS} is low or LE is low, driving \overline{EN} low enables all output buffers and driving \overline{EN} high disables all output buffers.
23	27	LE	Digital Latch-Enable Input. When LE is low, the \overline{EN} register is transparent; when LE is high, the \overline{EN} register is transparent only when \overline{CS} is low. Hard-wire to V+ or GND for best crosstalk performance.

PIN		NAME	FUNCTION
MAX467/MAX469	MAX468/MAX470		
1	1	IN0	Analog Input 0
2, 7, 8, 9, 15	2, 7, 15	GND	Analog Ground
3	3	IN1	Analog Input 1
4, 5, 12, 13	4, 5, 12, 13	V-	Negative Power-Supply Input. Connect to -5V. Thermal path.
6	6	IN2	Analog Input 2
–	8	IN3	Analog Input 3
–	9	OUT3	Buffered Analog Output 3
10	10	V+	Positive Power-Supply Input. Connect to +5V.
11	11	OUT2	Buffered Analog Output 2
14	14	OUT1	Buffered Analog Output 1
16	16	OUT0	Buffered Analog Output 0

Two-Channel, Triple/Quad RGB Video Switches and Buffers

Detailed Description

The MAX463-MAX470 have a bipolar construction, which results in a typical channel input capacitance of only 5pF, whether the channel is on or off. This low input capacitance allows the amplifiers to realize full AC performance, even with source impedances as great as 250 Ω . It also minimizes switching transients because the driving source sees the same load whether the channel is on or off. Low input capacitance is critical, because it forms a single-pole RC low-pass filter with the output impedance of the signal source, and this filter can limit the system's signal bandwidth if the RC product becomes too large.

The MAX465/MAX466/MAX469/MAX470's amplifiers are internally configured for a gain of two, resulting in an overall gain of one at the cable output when driving back-terminated coaxial cable (see the section *Driving Coaxial Cable*). The MAX463/MAX464/MAX467/MAX468 are internally configured for unity gain.

Power-Supply Bypassing and Board Layout

To realize the full AC performance of high-speed amplifiers, pay careful attention to power-supply bypassing and board layout, and use a large, low-impedance ground plane. With multi-layer boards, the ground plane should be located on the layer that is not dedicated to a specific signal trace.

To prevent unwanted signal coupling, minimize the trace area at the circuit's critical high-impedance nodes, and surround the analog inputs with an AC ground trace (analog ground, bypassed DC power supply, etc). The analog input pins to the MAX463-MAX470 have been separated with AC ground pins (GND, V+, V-, or a hard-wired logic input) to minimize parasitic coupling, which can degrade crosstalk and/or stability of the amplifier. Keep signal paths as short as possible to minimize inductance, and ensure that all input channel traces are of equal length to maintain the phase relationship between the R, G, and B signals. Connect the coaxial-cable shield to the ground side of the 75 Ω terminating resistor at the ground plane to further reduce crosstalk (see Figure 1).

Bypass all power-supply pins directly to the ground plane with 0.1 μ F ceramic capacitors, placed as close to the supply pins as possible. For high-current loads, it may be necessary to include 10 μ F tantalum or aluminum-electrolytic capacitors in parallel with the 0.1 μ F ceramics. Keep capacitor lead lengths as short as possible to minimize series inductance; surface-mount (chip) capacitors are ideal.

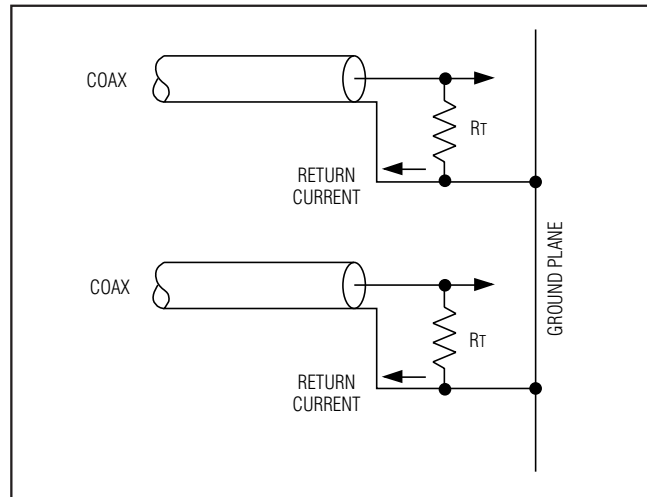


Figure 1. Low-Crosstalk Layout. Return current from the termination resistor does not flow through the ground plane.

Connect all V- pins to a large power plane. The V- pins conduct heat away from the internal die, aiding thermal dissipation.

Differential Gain and Phase Errors

Differential gain and phase errors are critical specifications for an amplifier/buffer in color video applications, because these errors correspond directly to changes in the color of the displayed picture in composite video systems. The MAX467-MAX470 have low differential gain and phase errors, making them ideal in broadcast-quality composite color applications, as well as in RGB video systems where these errors are less significant.

The MAX467-MAX470 differential gain and phase errors are measured with the Tektronix VM700 Video Measurement Set, with the input test signal provided by the Tektronix 1910 Digital Generator as shown in Figure 2.

Measuring the differential gain and phase of the MAX469/MAX470 (Figure 2a) is straightforward because the output amplifiers are configured for a gain of two, allowing connection to the VM700 through a back-terminated coaxial cable. Since the MAX467/MAX468 are unity-gain devices, driving a back-terminated coax would result in a gain of 1/2 at the VM700.

Figure 2b shows a test method to measure the differential gain and phase for the MAX467/MAX468. First, measure and store the video signal with the device under test (DUT) removed and replaced with a short circuit, and the 150 Ω load resistor omitted. Then do another measurement with the DUT and load resistor in the circuit, and calculate the differential gain and phase errors by subtracting the results.

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MAX463-MAX470

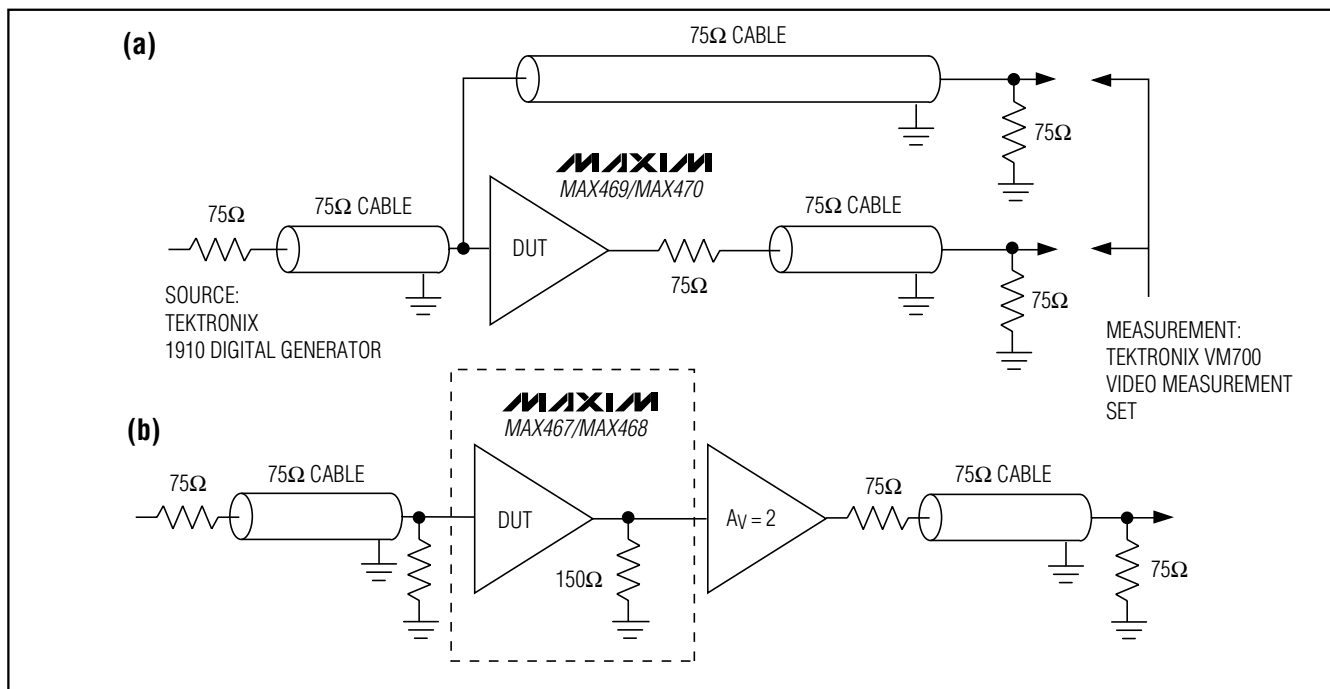


Figure 2. Differential Phase and Gain Error Test Circuits (a) for the MAX469/MAX470 Gain-of-Two Amplifiers, (b) for the MAX467/MAX468 Unity-Gain Amplifiers

Driving Coaxial Cable

High-speed performance, excellent output current capability, and an internally fixed gain of two make the MAX465/MAX466/MAX469/MAX470 ideal for driving 50Ω or 75Ω back-terminated coaxial cables. The MAX465/MAX466/MAX469/MAX470 will drive a 150Ω load (75Ω back-terminated cable) to $\pm 2.5\text{V}$.

The *Typical Operating Circuit* shows the MAX465/MAX466 driving four back-terminated 75Ω video cables. The back-termination resistor (at each amplifier output) provides impedance matching at the driven end of the cable to eliminate signal reflections. It forms a voltage divider with the load impedance, which attenuates the signal at the cable output by one-half. The amplifier operates with an internal 2V/V closed-loop gain to provide unity gain at the cable's output.

Driving Capacitive Loads

Driving large capacitive loads increases the likelihood of oscillation in most amplifier circuits. This is especially true for circuits with high loop-gains, like voltage followers. The amplifier's output impedance and the capacitive load form an RC filter that adds a pole to the loop response. If the pole frequency is low enough, as when driving a large capacitive load, the circuit phase margin is degraded and oscillation may occur.

The MAX463-MAX470 phase margin and capacitive-load driving performance are optimized by internal compensation. When driving capacitive loads greater than 50pF, connect an isolation resistor between the amplifier output and the capacitive load, as shown in Figure 3.

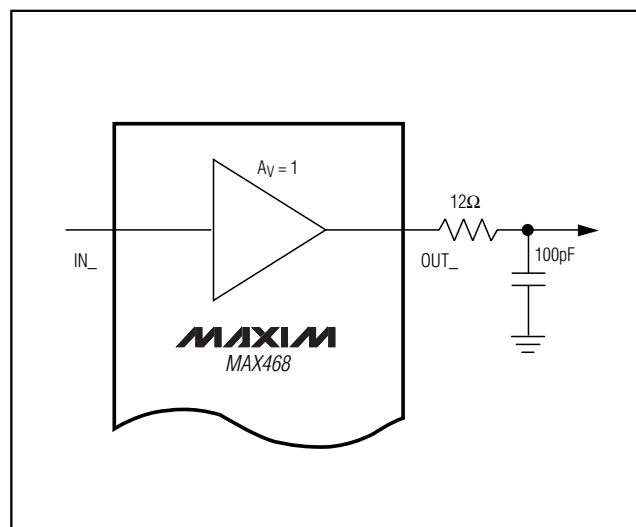


Figure 3a. Using an Isolation Resistor with a Capacitive Load

Two-Channel, Triple/Quad RGB Video Switches and Buffers

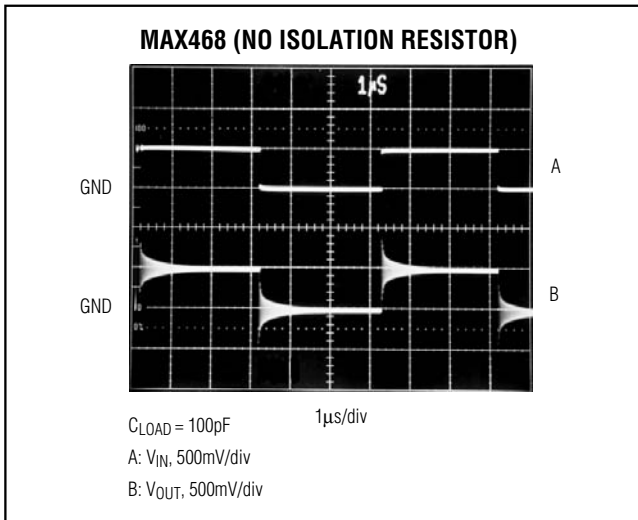


Figure 3b. Step Response without an Isolation Resistor

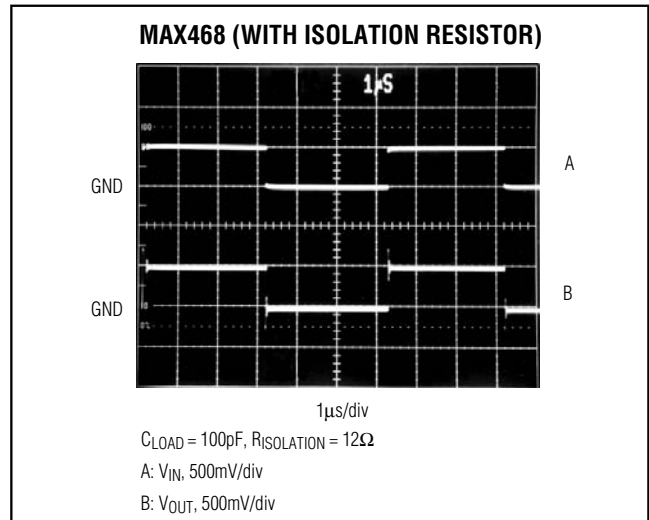


Figure 3c. Step Response with an Isolation Resistor

Digital Interface

The MAX463-MAX466 multiplexer architecture provides an input transistor buffer, ensuring that no input channels are ever connected together. Select a channel by changing A0's state (A0 = 0 for channel A, and A0 = 1 for channel B) and pulsing \overline{CS} low (see Tables 1a, 1b). Figure 4 shows the logic timing diagram.

Output Disable (MAX463-MAX466)

When the enable input (\overline{EN}) is driven to a TTL low state, it enables the MAX463-MAX466 amplifier outputs. When \overline{EN} is driven high, it disables the amplifier outputs. The

disabled MAX463/MAX464 outputs exhibit a 250k Ω typical resistance. Because their internal feedback resistors are required to produce a gain of two, the MAX465/MAX466 exhibit a 1k Ω disabled output resistance.

LE determines whether \overline{EN} is latched by \overline{CS} or operates independently. When the latch-enable input (LE) is connected to V+, \overline{CS} becomes the latch control for the \overline{EN} input register. If \overline{CS} is low, both the \overline{EN} and A0 registers are transparent; once \overline{CS} returns high, both registers are latched.

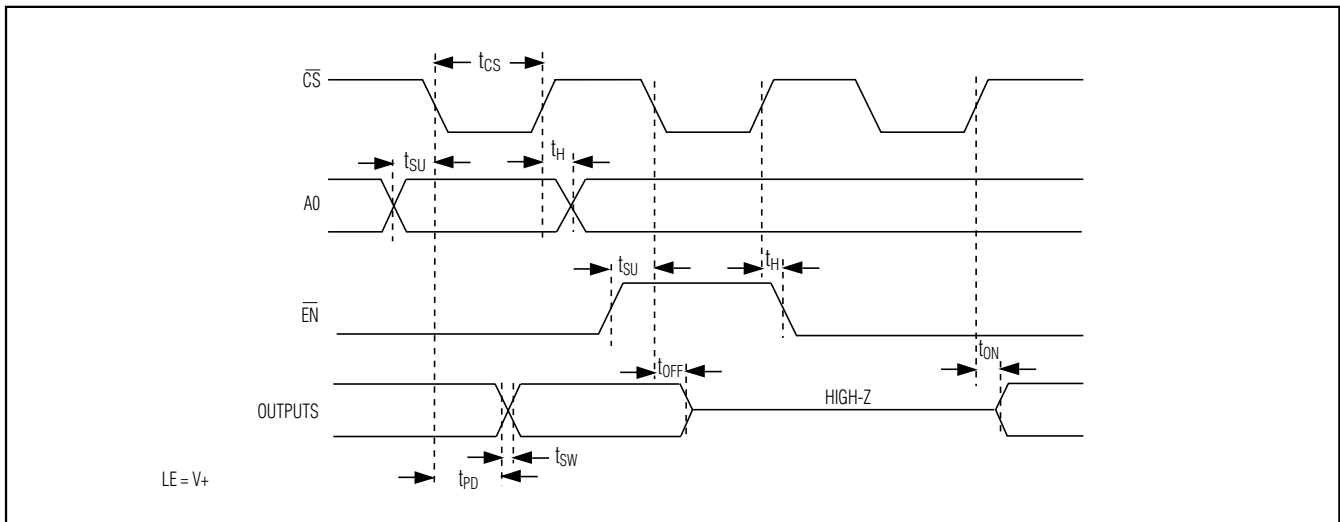


Figure 4. Logic Timing Diagram

Two-Channel, Triple/Quad RGB Video Switches and Buffers

Table 1a. Amplifier and Channel Selection with LE = V+

\overline{CS}	\overline{EN}	A0	FUNCTION
0	0	0	Enables amplifier outputs. Selects channel A.
0	0	1	Enables amplifier outputs. Selects channel B.
0	1	X	Disables amplifiers. Outputs high-Z.
1	X	X	Latches all input registers. Changes nothing.

Table 1b. Amplifier and Channel Selection with LE = GND

\overline{CS}	\overline{EN}	A0	FUNCTION
0	0	0	Enables amplifier outputs. Selects channel A.
0	0	1	Enables amplifier outputs. Selects channel B.
0	1	0	Disables amplifiers. Outputs high-Z. A0 register = channel A
0	1	1	Disables amplifiers. Outputs high-Z. A0 register = channel B
1	0	X	Enables amplifier outputs, latches A0 register, programs outputs to output A or B, according to the setting of A0 at \overline{CS} 's last edge.
1	1	X	Disables amplifiers. Outputs high-Z.

When LE is connected to ground, the \overline{EN} register is transparent and independent of \overline{CS} activity. This allows all MAX463–MAX466 devices to be simultaneously shut down, regardless of the \overline{CS} input state. Simply connect LE to ground and connect all \overline{EN} inputs together (Figure 5a). For the MAX464 and MAX466, LE must be hard-wired to either V+ or ground (rather than driving LE with a gate) to prevent crosstalk from the digital inputs to INOA.

Another option for output disable is to connect LE to V+, parallel the outputs of several MAX463–MAX466s, and use \overline{EN} to individually disable all devices but the one in use (Figure 5b).

When the outputs are disabled, the off isolation from the analog inputs to the amplifier outputs is typically 70dB at 10MHz, all inputs driven with a 4VP-P sine wave and a 150Ω load impedance. Figure 6 shows the test circuits used to measure isolation and crosstalk.

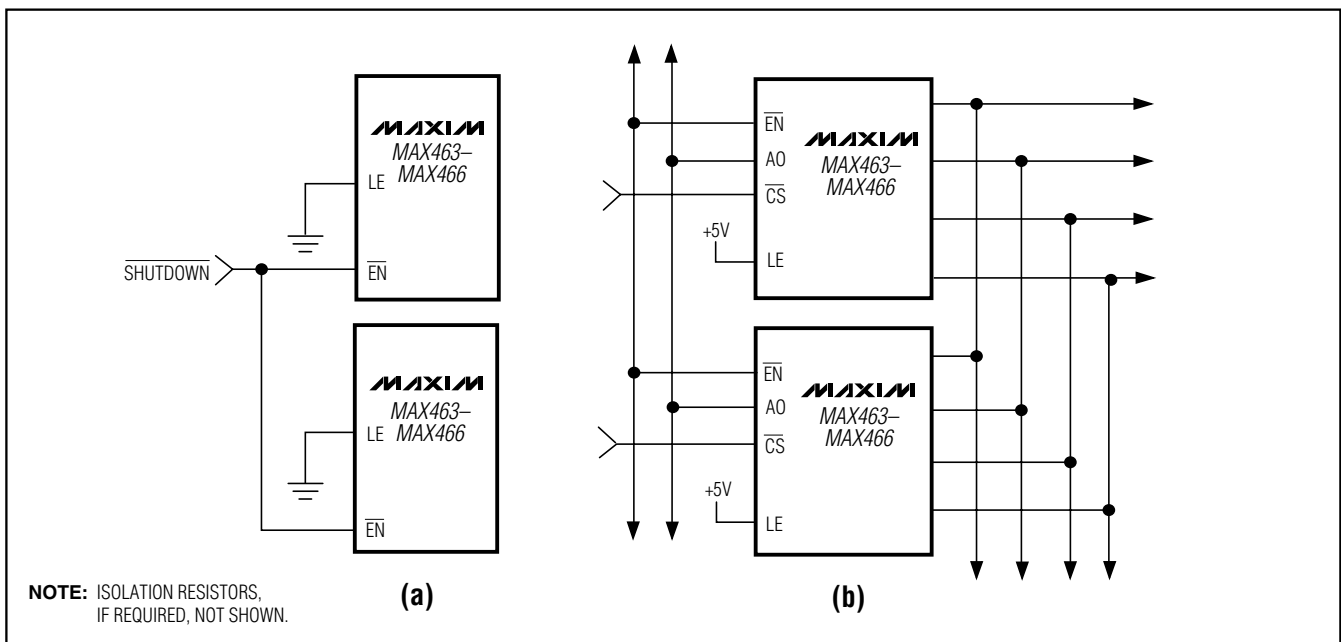


Figure 5. (a) Simultaneous Shutdown of all MAX463–MAX466, (b) Enable (\overline{EN}) Register Latched by \overline{CS}

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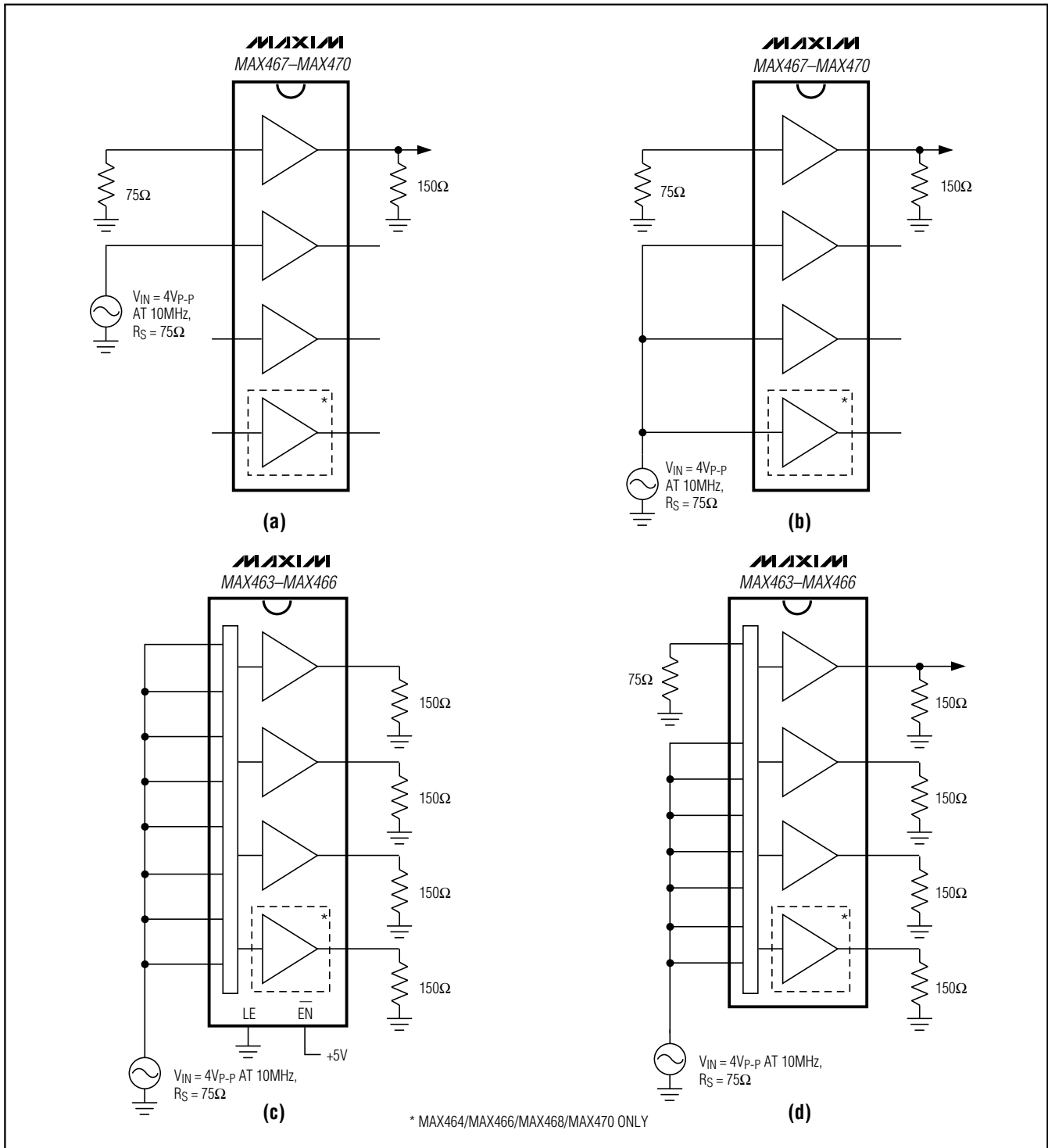


Figure 6. (a) MAX467-MAX470 Adjacent Channel Crosstalk, (b) MAX467-MAX470 All-Hostile Crosstalk, (c) MAX463-MAX466 All-Hostile Off Isolation, (d) MAX463-MAX466 All-Hostile Crosstalk

Two-Channel, Triple/Quad RGB Video Switches and Buffers

MAX463-MAX470

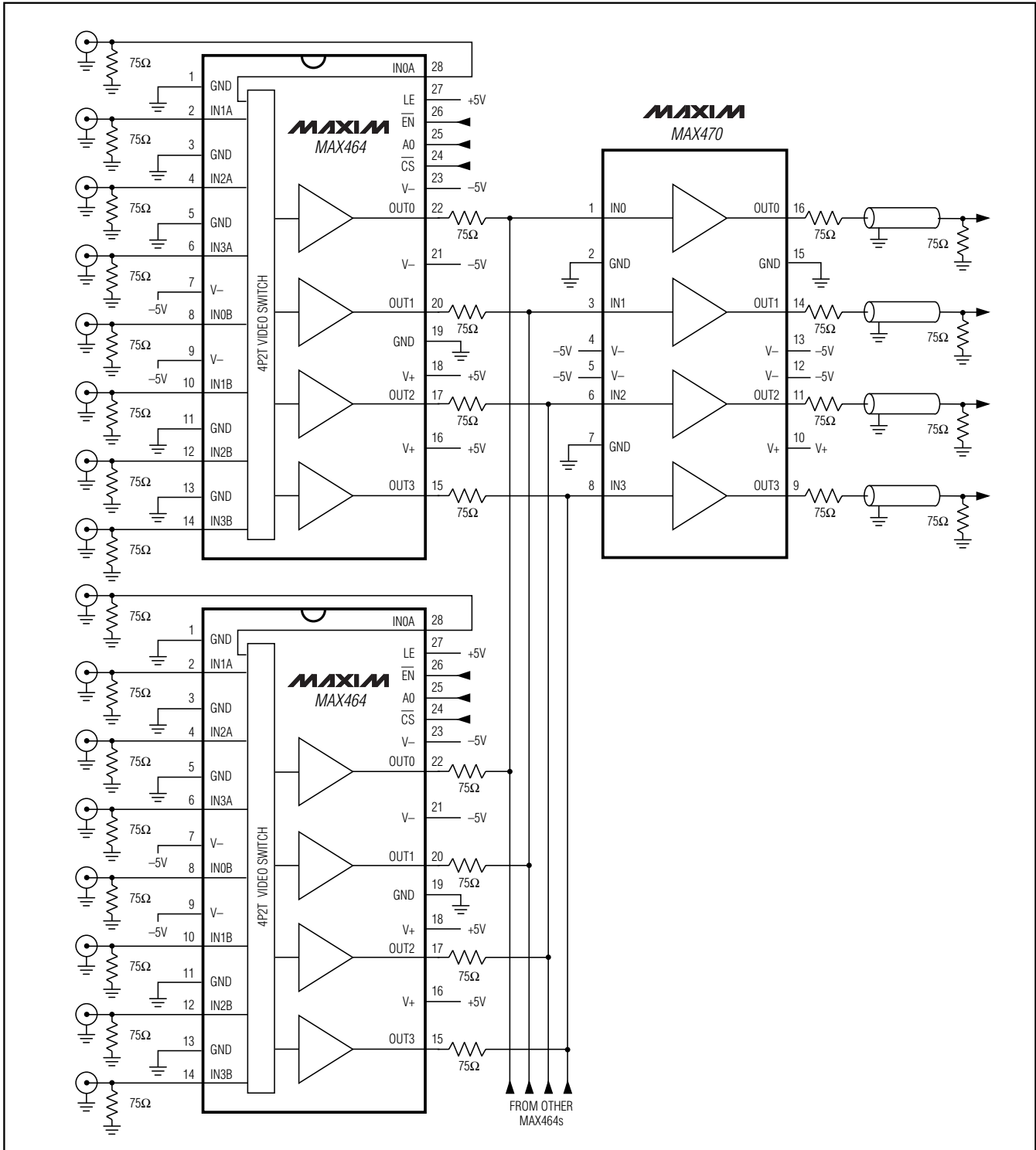


Figure 7. Higher-Order RGB + Sync Video Multiplexer

Two-Channel, Triple/Quad RGB Video Switches and Buffers

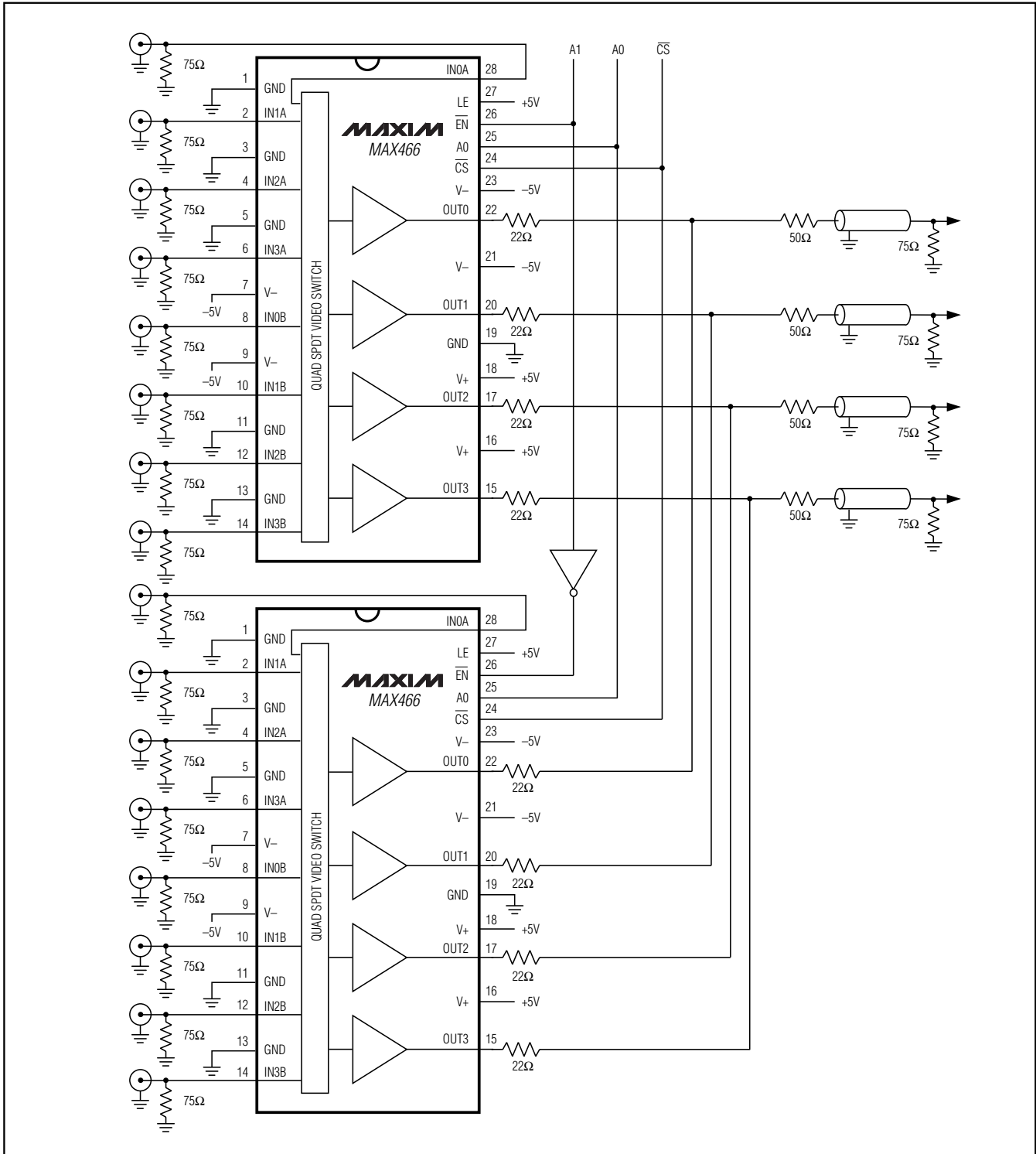


Figure 8. 1-of-4 RGB + Sync Video Multiplexer

Two-Channel, Triple/Quad RGB Video Switches and Buffers

Applications Information

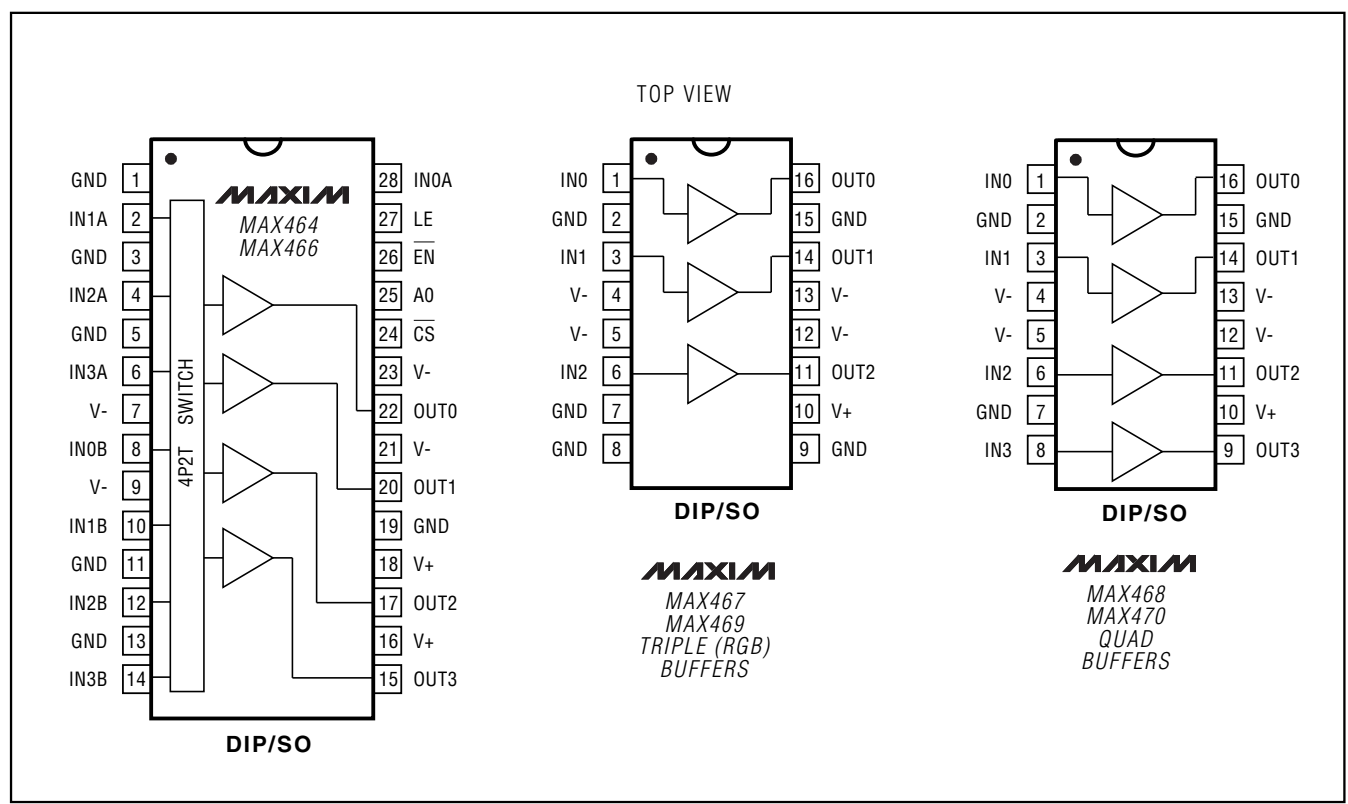
Higher-Order RGB + Sync Video Multiplexing

Higher-order RGB video multiplexers can be realized by paralleling several MAX463/MAX464s. Connect LE to V+ and use CS and EN to disable all devices but the one in use. Since the disabled output resistance of the MAX463/MAX464 is 250kΩ, several devices may be paralleled to form larger RGB video multiplexer arrays without signal degradation. Connect series resistors at each amplifier's output to isolate the disabled output capacitance of each paralleled device, and use a MAX469 or MAX470 to drive the output coaxial cables (see Figure 7).

Paralleling MAX466s to Switch 1-of-4 RGB + Sync Signal Inputs

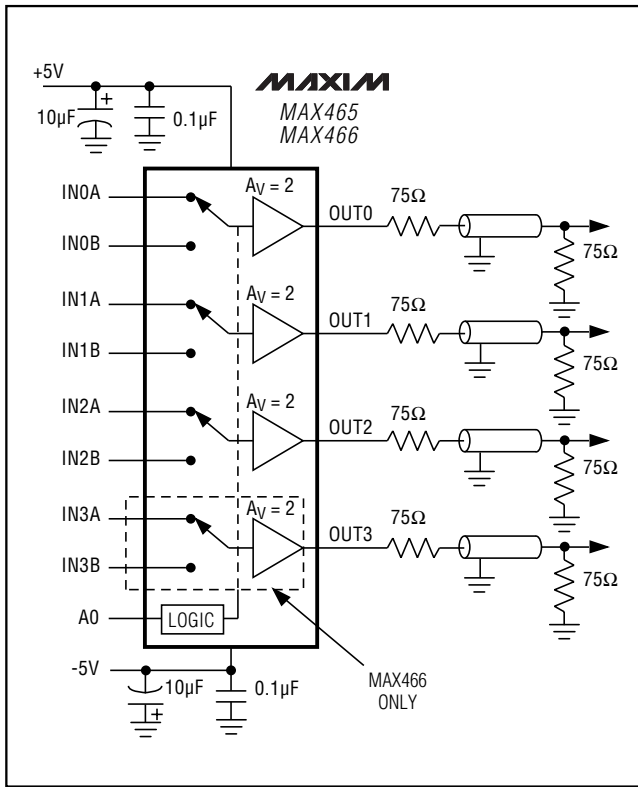
Figure 8 shows a 1-of-4 RGB + sync video mux/amp circuit. The 1kΩ disabled output resistance limits the number of paralleled MAX465/MAX466s to no more than two. The amplifier outputs are connected after a 22Ω isolation resistor and ahead of a 50Ω back-termination resistor, which isolates the active amplifier output from the capacitive load (5pF typ) presented by the inactive output of the second MAX466. Impedance mismatching is minimal, and the signal gain at the cable end is near 1. This minimizes ringing in the output signals. For multiplexing more than two devices, see the section *Higher Order RGB + Sync Video Multiplexing*, above.

Pin Configurations (continued)



Two-Channel, Triple/Quad RGB Video Switches and Buffers

Typical Operating Circuit



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX464 CNI	0°C to +70°C	28 Narrow Plastic DIP
MAX464CWI	0°C to +70°C	28 Wide SO
MAX464C/D	0°C to +70°C	Dice*
MAX464ENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX464EWI	-40°C to +85°C	28 Wide SO
MAX465 CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX465CWG	0°C to +70°C	24 Wide SO
MAX465C/D	0°C to +70°C	Dice*
MAX465ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX465EWG	-40°C to +85°C	24 Wide SO
MAX466 CNI	0°C to +70°C	28 Narrow Plastic DIP
MAX466CWI	0°C to +70°C	28 Wide SO
MAX466C/D	0°C to +70°C	Dice*
MAX466ENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX466EWI	-40°C to +85°C	28 Wide SO
MAX467 CPE	0°C to +70°C	16 Plastic DIP
MAX467CWE	0°C to +70°C	16 Wide SO
MAX467C/D	0°C to +70°C	Dice*
MAX467EPE	-40°C to +85°C	16 Plastic DIP
MAX467EWE	-40°C to +85°C	16 Wide SO
MAX468 CPE	0°C to +70°C	16 Plastic DIP
MAX468CWE	0°C to +70°C	16 Wide SO
MAX468C/D	0°C to +70°C	Dice*
MAX468EPE	-40°C to +85°C	16 Plastic DIP
MAX468EWE	-40°C to +85°C	16 Wide SO
MAX469 CPE	0°C to +70°C	16 Plastic DIP
MAX469CWE	0°C to +70°C	16 Wide SO
MAX469C/D	0°C to +70°C	Dice*
MAX469EPE	-40°C to +85°C	16 Plastic DIP
MAX469EWE	-40°C to +85°C	16 Wide SO
MAX470 CPE	0°C to +70°C	16 Plastic DIP
MAX470CWE	0°C to +70°C	16 Wide SO
MAX470C/D	0°C to +70°C	Dice*
MAX470EPE	-40°C to +85°C	16 Plastic DIP
MAX470EWE	-40°C to +85°C	16 Wide SO

* Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

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