THE DATASHEET OF

MAX4548EAX-T

www.win-source.net 0086-755-83957316

19-1496; Rev 0; 6/99

Serially Controlled, Triple 3x2 Audio/Video Crosspoint Switches

MAX4548/MAX4549

General Description

The MAX4548/MAX4549 serial-interface, programmable, triple 3x2 audio/video crosspoint switches are ideal for multimedia applications. The devices include three crosspoint switch matrices, each containing three inputs and two outputs. To improve off-isolation, each switch matrix has a shunt input and each output is selectively programmable for clickless or regular-mode operation. A selectable set of internal resistive voltage dividers supplies DC bias for each output when using AC-coupled inputs. To improve crosstalk, the voltage dividers include four externally accessible bypass points.

The MAX4548/MAX4549 feature 35Ω max on-resistance, 7Ω on-resistance matching between channels, 5Ω on-resistance flatness, and 0.07% total harmonic distortion (THD). Additionally, they feature off-isolation of -85dB at 20kHz and -72dB at 10MHz, with crosstalk of -85dB at 20kHz and -55dB at 10MHz. The MAX4548 uses a 2-wire I²C™-compatible serial interface, while the MAX4549 uses a 3-wire SPI™/QSPI™/MICROWIRE™-compatible serial interface. These parts are available in 36-pin SSOP packages and are specified for the extended (-40°C to +85°C) operating range.

Applications

Set-Top Boxes

PC Multimedia Boards

Video Conferencing Systems

High-End Audio Systems

Security Systems

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4548EAX	-40°C to +85°C	36 SSOP
MAX4549EAX	-40°C to +85°C	36 SSOP

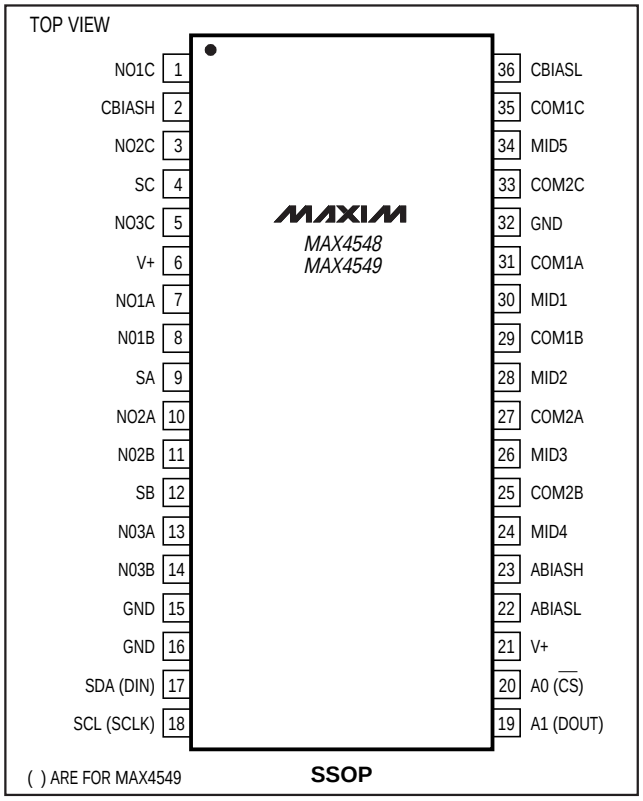
Functional Diagram appears at end of data sheet.

SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.
I²C is a trademark of Philips Corp.

Features

- **Selectable Soft-Switching Mode for "Clickless" Audio Operation**
- **22Ω Typical On-Resistance (+5V Supply)**
- **5Ω Typical On-Resistance Matching Between Channels**
- **2Ω Typical On-Resistance Flatness**
- **Audio Performance**
  - **-85dB Off-Isolation at 20kHz**
  - **-85dB Crosstalk at 20kHz**
  - **0.07% THD with 600Ω Load**
- **Video Performance**
  - **-72dB Off-Isolation at 10MHz**
  - **-55dB Crosstalk at 10MHz**
- **Serial Interface**
  - **2-Wire I²C-Compatible (MAX4548)**
  - **3-Wire SPI/QSPI/MICROWIRE-Compatible (MAX4549)**
- **Single-Supply Operation from +2.7V to +5.5V**

Pin Configuration



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For small orders, phone 1-800-835-8769.

Serially Controlled, Triple 3x2 Audio/Video Crosspoint Switches

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +6V
NO_ _, S_, MID_, BYP, COM_ _, CBIASL, ABIASL, CBIASH, ABIASH, DOUT to GND (Note 1).....-0.3V to (V+ + 0.3V)
$\overline{CS}$, A0, A1, SDA, SCL, DIN, SCLK to GND .....-0.3V to +6V
Continuous Current into Any Terminal.....±20mA
Peak Current, NO_ _, S_, COM_ _ (pulsed at 1ms, 10% duty cycle max).....±40mA
Continuous Power Dissipation (T_A = +70°C) 36-Pin SSOP (derate 11.8mW/°C above +70°C) 941mW
Operating Temperature Range .....-40°C to+85°C
Storage Temperature Range .....-65°C to+150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on NO_ _, S_, or COM_ _ exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCHES							
Analog Signal Range (Note 3)	$V_{NO__}$, $V_{COM__}$, $V_{S_}$			0		V+	V
On-Resistance	R_{ON}	$I_{COM__}$ = 4mA, $V_{NO__}$ or $V_{S_}$ = 3V, V+ = 4.75V	T_A = +25°C		22	35	Ω
			T_A = T_{MIN} to T_{MAX}			45	
COM_ _ to NO_ _ or S_ On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	$I_{COM__}$ = 4mA, $V_{NO__}$ or $V_{S_}$ = 3V, V+ = 4.75V	T_A = +25°C		5	7	Ω
			T_A = T_{MIN} to T_{MAX}			8	
COM_ _ to NO_ _ or S_ On-Resistance Flatness (Note 5)	R_{FLAT}	$I_{COM__}$ = 4mA; V+ = 4.75V; $V_{NO__}$ or $V_{S_}$ = 1V, 2V, 3V	T_A = +25°C		2	5	Ω
			T_A = T_{MIN} to T_{MAX}			7	
NO_ _ or S_ Off-Leakage Current (Note 6)	$I_{NO__(OFF)}$	$V_{NO__}$ or $V_{S_}$ = 4.5V, 1V; $V_{COM__}$ = 1V, 4.5V; V+ = 5.25V	T_A = +25°C	-2	0.04	2	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
COM_ _ Off-Leakage Current (Note 6)	$I_{COM__(OFF)}$	$V_{NO__}$ or $V_{S_}$ = 4.5V, 1V; $V_{COM__}$ = 1V, 4.5V; V+ = 5.25V	T_A = +25°C	-2	0.04	2	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
COM_ _On-Leakage Current (Note 6)	$I_{COM__(ON)}$	$V_{NO__}$ or $V_{S_}$ = 4.5V, 1V, or floating; $V_{COM__}$ = 4.5V, 1V; V+ = 5.25V	T_A = +25°C	-2	0.04	2	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
AUDIO PERFORMANCE							
Total Harmonic Distortion plus Noise	THD+N	f_{IN} = 1kHz, $V_{NO__}$ or $V_{S_}$ = $1V_{RMS}$ + $2.5V_{DC}$	R_L = 600Ω		0.07		%
			R_L =10kΩ		0.006		
Off-Isolation (Note 7)	$V_{ISO(A)}$	$V_{NO__}$ = $1V_{RMS}$, f_{IN} = 20kHz, R_L = 600Ω, S_ = GND, shunt switch on or off			-85		dB
Channel-to-Channel Crosstalk	$V_{CT(A)}$	$V_{NO__}$ = $1V_{RMS}$, f_{IN} = 20kHz, R_L = R_S = 600Ω			-85		dB

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VIDEO PERFORMANCE							
Off-Isolation (Note 7)	$V_{ISO(V)}$	$V_{NO__}$ or $V_{S_}$ = 1V_{RMS}, f_{IN} = 10MHz, R_L = 50Ω, R_S =50Ω, S_ = GND	Shunt switch on		-72		dB
			Shunt switch off		-62		
Channel-to-Channel Crosstalk	$V_{CT(V)}$	$V_{NO__}$ or $V_{S_}$ = 0.5V_{RMS}, R_S = 50Ω, f_{IN} = 10MHz, R_L = 50Ω,			-55		dB
-3dB Bandwidth	BW	R_S = 50Ω, R_L = 50Ω			250		MHz
Off-Capacitance	$C_{OFF(NO)}$	f = 1MHz			10		pF
DYNAMIC TIMING WITH CLICKLESS MODE DISABLED (Note 8, Figure 1)							
Turn-On Time	t_{ONSD}	$V_{NO__}$ or $V_{S_}$ = 2.5V, R_L = 5kΩ, C_L = 35pF	T_A = +25°C		200	400	ns
			T_A = T_{MIN} to T_{MAX}			500	
Turn-Off Time	t_{OFFSD}	$V_{NO__}$ or $V_{S_}$ = 2.5V, R_L = 300Ω, C_L = 35pF	T_A = +25°C		100	200	ns
			T_A = T_{MIN} to T_{MAX}			250	
Break-Before-Make Time	t_{BBM}	$V_{NO__}$ or $V_{S_}$ = 2.5V		10	50		ns
DYNAMIC TIMING WITH CLICKLESS MODE ENABLED (Note 8, Figure 1)							
Turn-On Time	t_{ONSE}	$V_{NO__}$ or $V_{S_}$ = 2.5V, R_L = 5kΩ, C_L = 35pF, T_A = +25°C			12		ms
Turn-Off Time	t_{OFFSE}	$V_{NO__}$ or $V_{S_}$ = 2.5V, R_L = 300Ω, C_L = 35pF, T_A = +25°C			3		ms
BIAS NETWORKS							
Bias Network Resistance	R_{BIAS}				110		kΩ
POWER SUPPLIES							
Supply Voltage Range	V+			2.7		5.5	V
Supply Current (Note 9)	I+	All logic inputs = GND or V+			6	10	µA

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCHES							
Analog Signal Range (Note 3)	$V_{NO__}$, $V_{COM__}$, $V_{S_}$			0		V+	V
On-Resistance	R_{ON}	$I_{COM__}$ = 4mA, $V_{NO__}$ or $V_{S_}$ = 1V, V+ = 2.7V	T_A = +25°C		40	60	Ω
			T_A = T_{MIN} to T_{MAX}			80	
COM_ _ to NO_ _ or S_ On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	$I_{COM__}$ = 4mA, $V_{NO__}$ or $V_{S_}$ = 1V, V+ = 2.7V	T_A = +25°C		5	7	Ω
			T_A = T_{MIN} to T_{MAX}			8	
COM_ _ to NO_ _ or S_ On-Resistance Flatness (Note 5)	R_{FLAT}	$I_{COM__}$ = 4mA; V+ = 2.7V; $V_{NO__}$ = 1V, 1.5V, 2V	T_A = +25°C		3	6	Ω
			T_A = T_{MIN} to T_{MAX}			8	

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ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

($V+$ = +3V ±10%, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
NO_ _ or S_ Off-Leakage Current (Notes 6, 10)	$I_{NO__(OFF)}$	$V_{NO__}$ or $V_{S_}$ = 3V, 0.5V; $V_{COM__}$ = 0.5V, 3V; V+ = 3.6V	T_A = +25°C	-2	0.04	2	nA
			$T_A = T_{MIN}$ to T_{MAX}	-10		10	
COM _ Off-Leakage Current (Notes 6, 10)	$I_{COM__(OFF)}$	$V_{NO__}$ or $V_{S_}$ = 3V, 0.5V; $V_{COM__}$ = 0.5V, 3V; V+ = 3.6V	T_A = +25°C	-2	0.04	2	nA
			$T_A = T_{MIN}$ to T_{MAX}	-10		10	
COM _ On-Leakage Current (Notes 6, 10)	$I_{COM__(ON)}$	$V_{NO__}$ or $V_{S_}$ = 0.5V, 3V, or floating; $V_{COM__}$ = 0.5V, 3V; V+ = 3.6V	T_A = +25°C	-2	0.04	2	nA
			$T_A = T_{MIN}$ to T_{MAX}	-10		10	
AUDIO PERFORMANCE							
Total Harmonic Distortion plus Noise	THD+N	f_{IN} = 1kHz, $V_{NO__}$ or $V_{S_}$ = 1.5V_{DC} + 0.5V_{RMS}	R_L = 600Ω		0.1		%
			R_L = 10Ω		0.01		
Off-Isolation (Note 7)	$V_{ISO(A)}$	$V_{NO__}$ = 0.5V_{RMS}, f_{IN} = 20kHz, R_L = 600Ω, S_ = GND, shunt switch on or off			-85		dB
Channel-to-Channel Crosstalk	$V_{CT(A)}$	$V_{NO__}$ = 0.5V_{RMS}, f_{IN} = 20kHz, R_L = 600kΩ, R_S = 600Ω			-85		dB
VIDEO PERFORMANCE							
Off-Isolation (Note 7)	$V_{ISO(V)}$	$V_{NO__}$ or $V_{S_}$ = 0.5V_{RMS}, f_{IN} = 10MHz, R_L = 50Ω, R_S = 50Ω	Shunt switch on		-72		dB
			Shunt switch off		-62		
Channel-to-Channel Crosstalk	$V_{CT(V)}$	$V_{NO__}$ or $V_{S_}$ = 0.5V_{RMS}, R_S = 50Ω, f_{IN} = 10MHz, R_L = 50Ω			-55		dB
-3dB Bandwidth	BW	R_S = 50Ω, R_L = 50Ω			200		MHz
Off-Capacitance	$C_{OFF(NO)}$	f = 1MHz			10		pF
DYNAMIC TIMING WITH CLICKLESS MODE DISABLED (Notes 8 and 12, Figure 1)							
Turn-On Time	t_{ONSD}	$V_{NO__}$ or $V_{S_}$ = 1.5V, R_L = 5kΩ, C_L = 35pF	T_A = +25°C		400	800	ns
			$T_A = T_{MIN}$ to T_{MAX}			1000	
Turn-Off Time	t_{OFFSD}	$V_{NO__}$ or $V_{S_}$ = 1.5V, R_L = 300Ω, C_L = 35pF	T_A = +25°C		200	350	ns
			$T_A = T_{MIN}$ to T_{MAX}			500	
Break-Before-Make Time	t_{BBM}	$V_{NO__}$ or $V_{S_}$ = 1.5V		10	100		ns
DYNAMIC TIMING WITH CLICKLESS MODE ENABLED (Notes 8 and 12, Figure 1)							
Turn-On Time	t_{ONSE}	$V_{NO__}$ or $V_{S_}$ = 1.5V, R_L = 5kΩ, C_L = 35pF			12		ms
Turn-Off Time	t_{OFFSE}	$V_{NO__}$ or $V_{S_}$ = 1.5V, R_L = 300Ω, C_L = 35pF			3		ms
BIAS NETWORK							
Bias Network Resistance	R_{BIAS}				110		kΩ

I/O INTERFACE CHARACTERISTICS

(V+ = +2.7V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, SCL, SDA, A0, A1)						
Input Low Voltage	V_{IL}	V+ = 5V			0.8	V
		V+ = 3V			0.6	
Input High Voltage	V_{IH}	V+ = 5V	3			V
		V+ = 3V	2			
Input Hysteresis	V_{HYST}			0.2		V
Input Leakage Current	I_{LEAK}	Digital inputs = GND or V+	-1	0.001	1	µA
Input Capacitance	C_{IN}	f = 1MHz		5		pF
DIGITAL OUTPUTS (DOUT, SDA)						
Output Low Voltage	V_{OL}	I_{SINK} = 6mA			0.4	V
DOUT Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA	V+ - 0.5			V

2-WIRE TIMING CHARACTERISTICS (Figure 3)

(V+ = +2.7V to +5.25V, f_{SCL} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	V+ = 4.75V to 5.25V	0		400	kHz
		V+ = 2.7V to 5.25V	0		100	
Bus-Free Time between Stop and Start Condition	t_{BUF}		4.7			µs
Hold Time After Start Condition	$t_{HD:STA}$		4			µs
Pulse Width of Suppressed Spike (Note 3)			0		50	ns
STOP Condition Setup Time	$t_{SU:STO}$		4			µs
Data Hold Time	$t_{HD:DAT}$		0			µs
Data Setup Time	$t_{SU:DAT}$		250			ns
Clock Low Period	t_{LOW}		4.7			µs
Clock High Period	t_{HIGH}		4			µs
SCL/SDA Rise Time (Note 11)	t_R		20 + $0.1C_b$		300	ns
SCL/SDA Fall Time (Note 11)	t_F		20 + $0.01C_b$		300	ns

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3-WIRE TIMING CHARACTERISTICS (Figure 5)

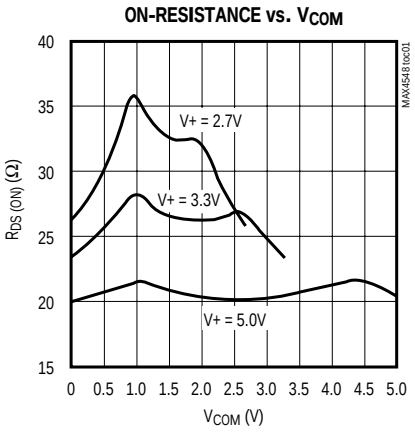
(V+ = +2.7V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

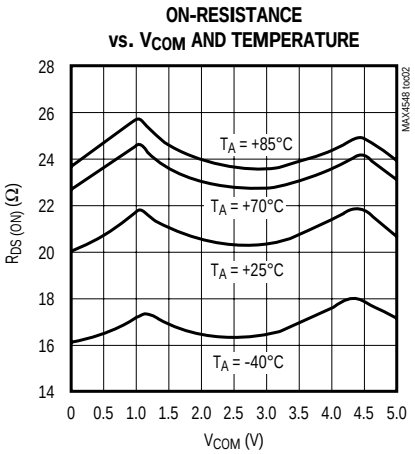
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	f_{OP}	V+ = 4.75V to 5.25V	0		10	MHz
		V+ = 2.7V to 5.25V	0		2.1	
DIN to SCLK Setup	t_{DS}		100			ns
DIN to SCLK Hold	t_{DH}		0			ns
SCLK Fall to Output Data Valid	t_{DO}	C_{LOAD} = 50pF			200	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		40			ns
SCLK Pulse Width High	t_{CH}		200			ns
SCLK Pulse Width Low	t_{CL}		200			ns
Rise Time (SCLK, DIN, $\overline{CS}$)	t_R				2	µs
Fall Time (SCLK, DIN, $\overline{CS}$)	t_F				2	µs

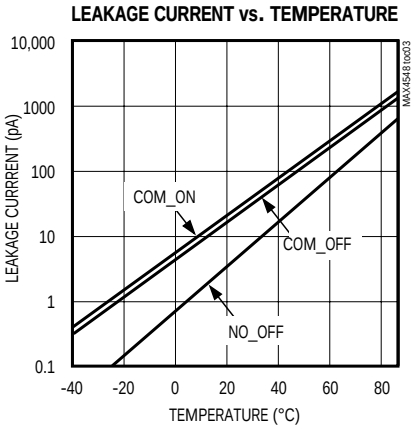
Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Guaranteed by design. Not subject to production testing.
Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
Note 5: Resistance flatness is defined as the difference between the maximum and minimum on-resistance values, as measured over the specified analog signal range.
Note 6: Leakage parameters are 100% tested at maximum rated temperature and guaranteed by correlation at T_A = +25°C.
Note 7: Off-isolation = 20log ($V_{COM_}$ / $V_{NO__}$), $V_{COM_}$ = output, $V_{NO__}$ = input to off switch.
Note 8: All timing is measured from the clock's falling edge preceding the ACK signal for 2-wire and from the rising edge of $\overline{CS}$ for 3-wire. Turn-off time is defined at the output of the switch for a 0.5V change, tested with a 300Ω load to ground. Turn-on time is defined at the output of the switch for a 0.5V change and measured with a 5kΩ load resistor to GND. All timing is shown with respect to 20% V+ and 70% V+, unless otherwise noted.
Note 9: Supply current can be as high as 2mA per switch during switch transitions in the clickless mode, corresponding to a 48mA total supply transient current requirement.
Note 10: Leakage testing is guaranteed by testing with a +5.25V supply.
Note 11: C_b = capacitance of one bus line in pF. Tested with C_b = 400pF.
Note 12: Typical values are for MAX4548 devices.

Typical Operating Characteristics

(V+ = +5V, T_A = +25°C, unless otherwise noted.)



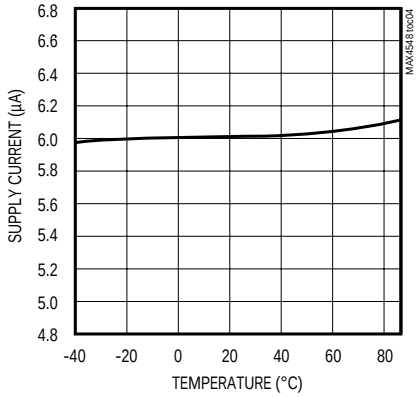




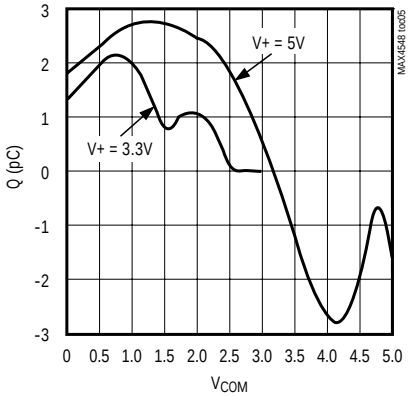
Typical Operating Characteristics (continued)

(V+ = +5V, T_A = +25°C, unless otherwise noted.)

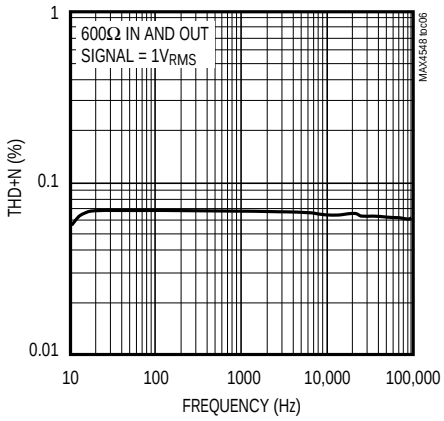
SUPPLY CURRENT vs. TEMPERATURE



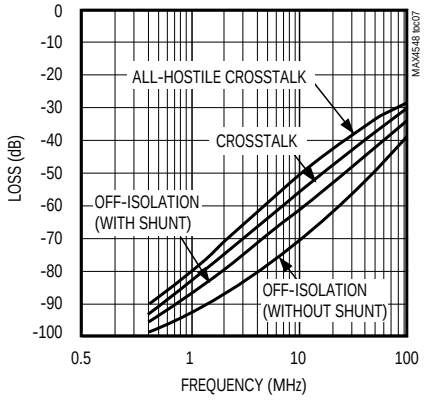
CHARGE INJECTION vs. V_{COM}



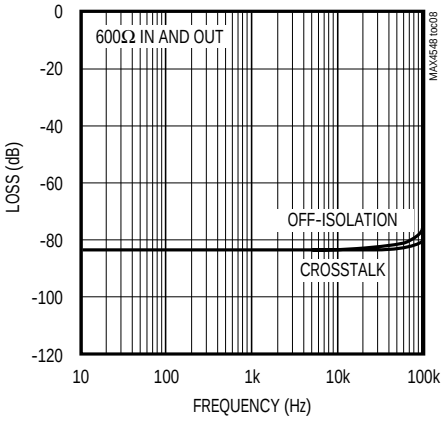
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



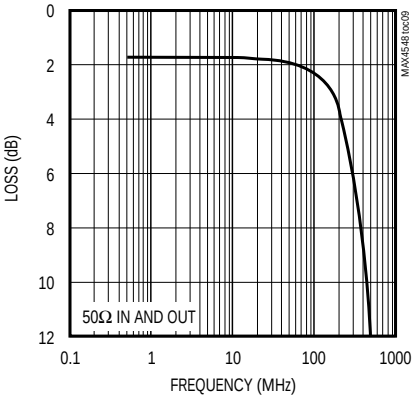
VIDEO FREQUENCY CHARACTERISTICS



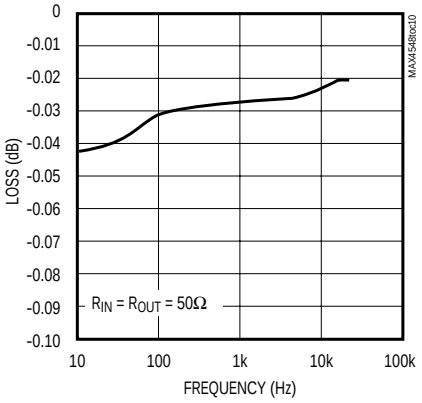
AUDIO FREQUENCY CHARACTERISTICS



VIDEO FREQUENCY RESPONSE



AUDIO FREQUENCY RESPONSE

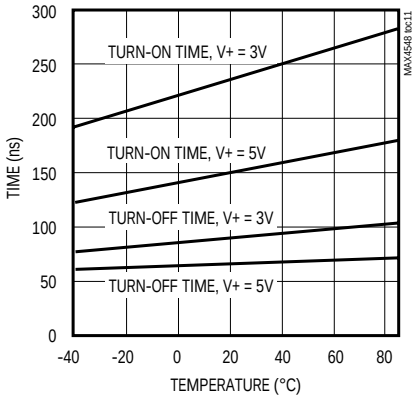


Serially Controlled, Triple 3x2 Audio/Video Crosspoint Switches

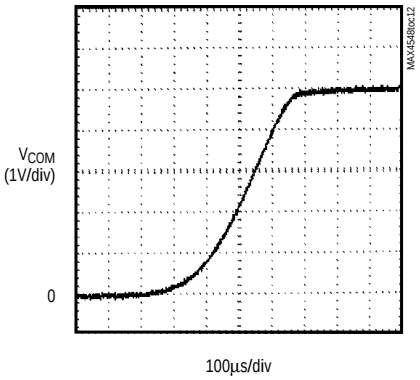
Typical Operating Characteristics (continued)

(V+ = +5V, T_A = +25°C, unless otherwise noted.)

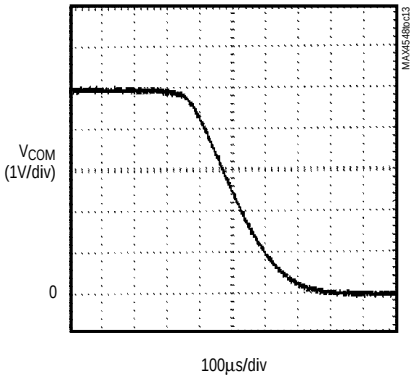
ON/OFF TIME vs. TEMPERATURE (HARD MODE)



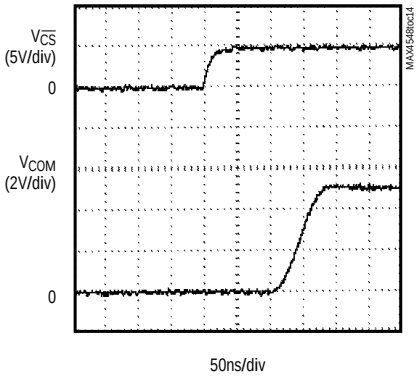
COM RISE TIME (SOFT MODE)



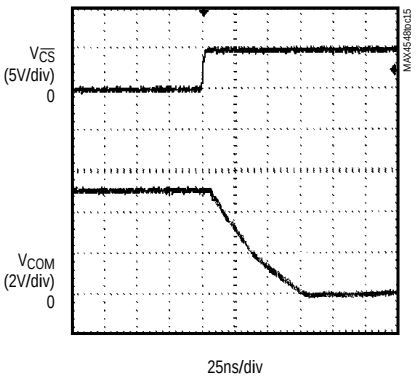
COM FALL TIME (SOFT MODE)



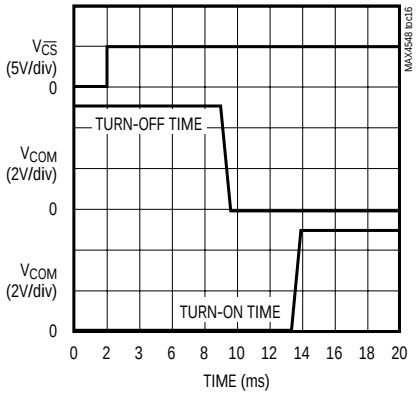
COM TURN-ON TIME (HARD MODE)



COM TURN-OFF TIME (HARD MODE)



COM ON/OFF TIMES (SOFT MODE)



Pin Description

PIN		NAME	FUNCTION
MAX4548	MAX4549		
1	1	NO1C	Input 1 to Crosspoint C
2	2	CBIASH	High Side of Bias Network for Crosspoint C. Use to give the C outputs a DC bias when inputs are AC-coupled (refer to the *Using the Internal Bias Resistors* section).
3	3	NO2C	Input 2 to Crosspoint C
4	4	SC	Shunt Input to Crosspoint C. Use for shunt capacitor of AC ground connection to improve off-isolation, or as an additional input to switch matrix C.
5	5	NO3C	Input 3 to Crosspoint C
6, 21	6, 21	V+	Positive Supply Voltage. Supply range is 2.7V to 5.5V.
7	7	NO1A	Input 1 to Crosspoint A
8	8	NO1B	Input 1 to Crosspoint B
9	9	SA	Shunt Input to Crosspoint A. Use for shunt capacitor of AC ground connection to improve off-isolation, or as an additional input to switch matrix A.
10	10	NO2A	Input 2 to Crosspoint A
11	11	NO2B	Input 2 to Crosspoint B
12	12	SB	Shunt Input to Crosspoint B. Use for shunt capacitor of AC ground connection to improve off-isolation, or as an additional input to switch matrix B.
13	13	NO3A	Input 3 to Crosspoint A
14	14	NO3B	Input 3 to Crosspoint B
15, 16, 32	15, 16, 32	GND	Ground
17	–	SDA	2-Wire Serial-Interface Data Input. Data is clocked in on SCL's rising edge.
–	17	DIN	3-Wire Serial-Interface Data Input. Data is clocked in on SCLK's rising edge.
18	–	SCL	2-Wire Serial-Interface Clock Input
–	18	SCLK	3-Wire Serial-Interface Clock Input
19	–	A1	LSB+1 of 2-Wire Serial-Interface Address Field
–	19	DOUT	Data Output of 3-Wire Serial-Interface. Input data is clocked on SCLK's falling edge delayed by 24 clock cycles. DOUT remains active when $\overline{CS}$ is high.
20	–	A0	LSB of 2-Wire Serial-Interface Address Field
–	20	$\overline{CS}$	Chip Select of 3-Wire Serial Interface. Logic low on $\overline{CS}$ enables serial data to be clocked in to device. Programming commands are executed on $\overline{CS}$'s rising edge.
22	22	ABIASL	Low Side of Bias Network for Crosspoint A and B. Use to give the A and B outputs a DC bias when inputs are AC-coupled (refer to the *Using the Internal Bias Resistors* section).
23	23	ABIASH	High Side of Bias Network for Crosspoint A and B. Use to give the A and B outputs a DC bias when inputs are AC-coupled (refer to the *Using the Internal Bias Resistors* section).
24	24	MID4	Audio Bypass for SA and SB Inputs
25	25	COM2B	Output 2 of Crosspoint B

Pin Description (continued)

PIN		NAME	FUNCTION
MAX4548	MAX4549		
26	26	MID3	Audio Bypass for IN3A and IN3B Inputs
27	27	COM2A	Output 2 of Crosspoint A
28	28	MID2	Audio Bypass for IN2A and IN2B Inputs
29	29	COM1B	Output 1 of Crosspoint B
30	30	MID1	Audio Bypass for IN1A and IN1B Inputs
31	31	COM1A	Output 1 of Crosspoint A
33	33	COM2C	Output 2 of Crosspoint C
34	34	MID5	Video Bypass for All Inputs to Crosspoint C
35	35	COM1C	Output 1 of Crosspoint C
36	36	CBIASL	High Side of Bias Network for Crosspoint C. Use to give the C outputs a DC bias when inputs are AC-coupled (refer to the *Using the Internal Bias Resistors* section).

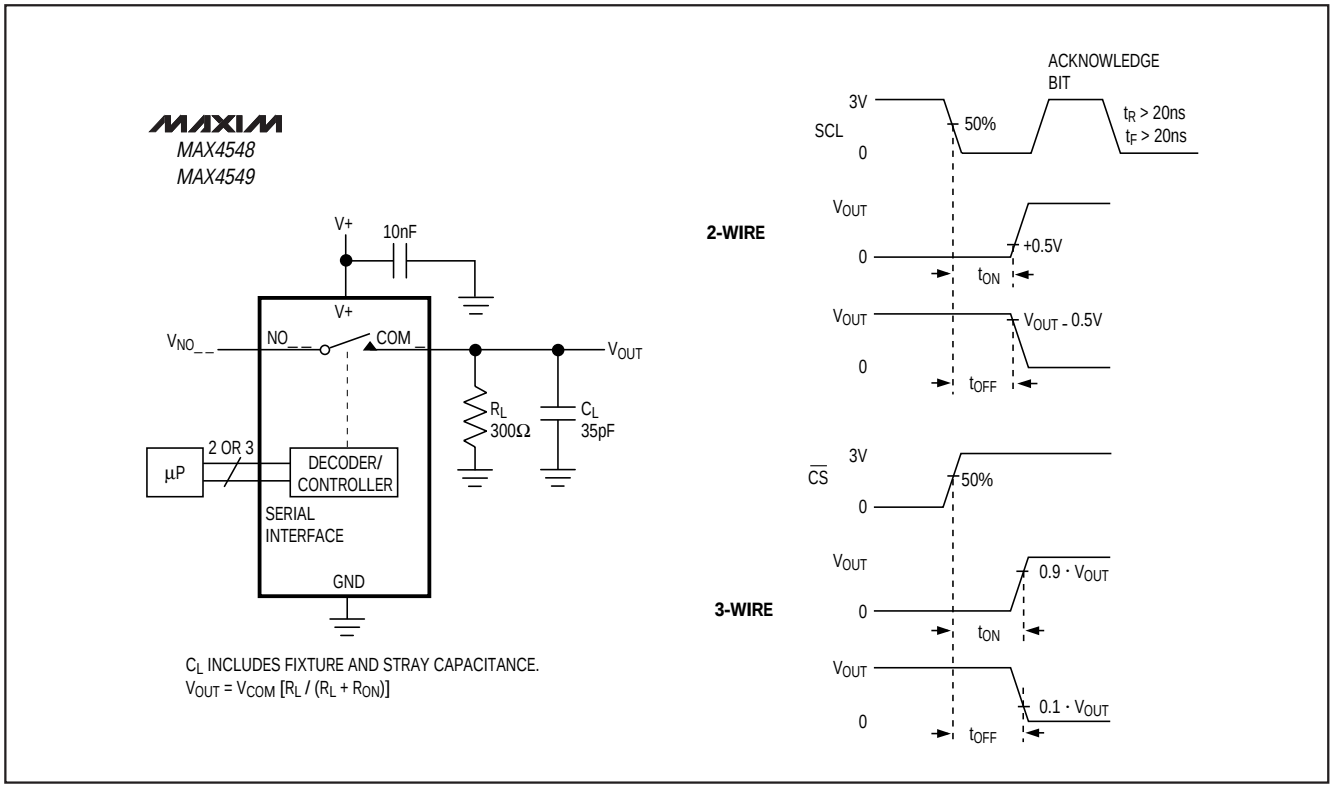


Figure 1. Switching Times

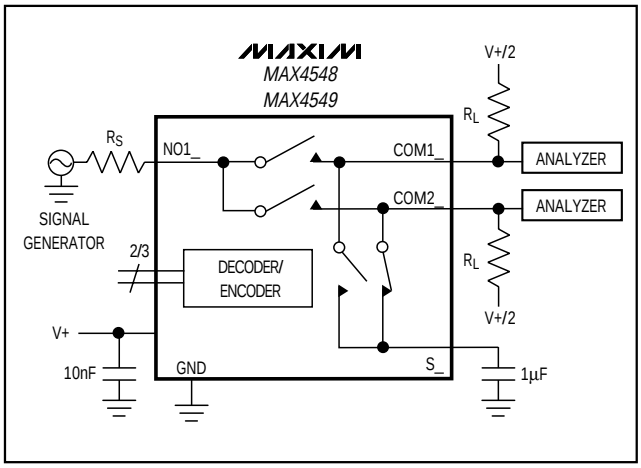


Figure 2a. Off-Isolation

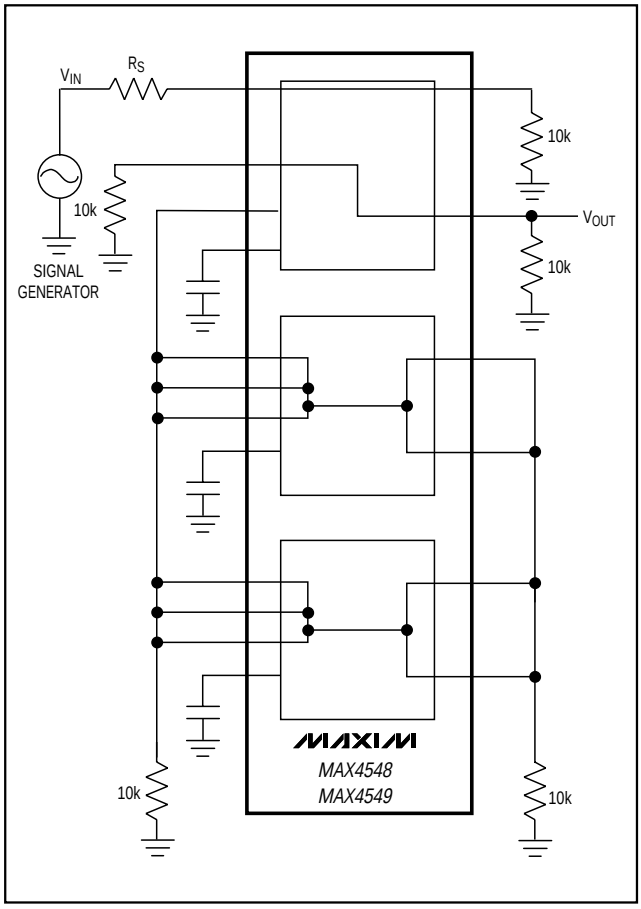


Figure 2b. Crosstalk

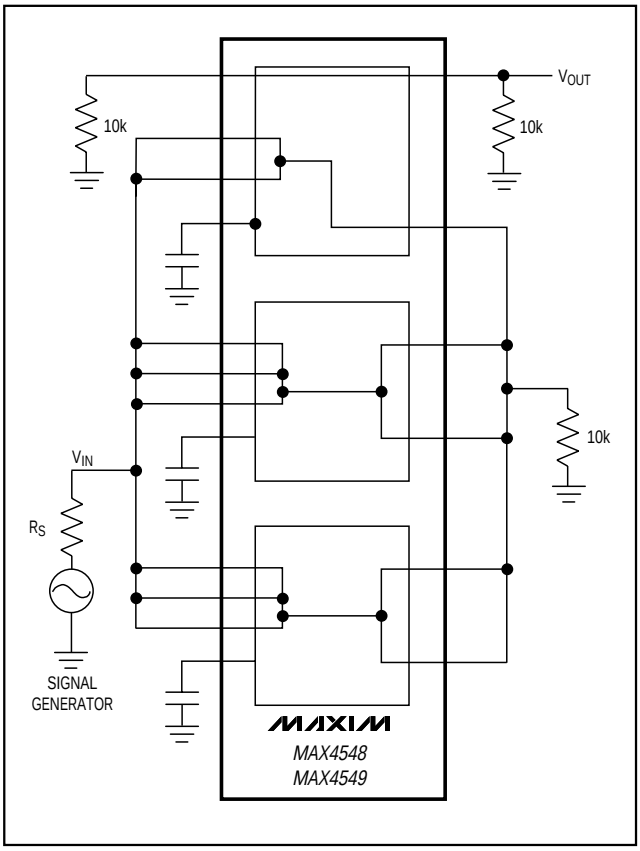


Figure 2c. All-Hostile Crosstalk

Detailed Description

The MAX4548/MAX4549 are serial-interface, programmable, triple 3x2 audio/video crosspoint switches. Each device contains two crosspoint switches with a common bypass network and another crosspoint switch with its own bypass network. The switches are independently controlled through the on-chip serial interface. The MAX4548 uses a 2-wire I^2C-compatible serial communications protocol, while the MAX4549 uses a 3-wire SPI/QSPI/MICROWIRE-compatible serial communications protocol.

These ICs include twelve selectable bias-resistor networks (one for each input) for use with AC-coupled input signals. They operate from a single supply of +2.7V to +5.5V and are optimized for use in the audio frequency range to 20kHz and at video frequencies to 10MHz. They feature 35Ω max on-resistance, 7Ω on-resistance matching between channels, 5Ω on-resistance flatness, and as low as 0.07% total harmonic distortion.

Serially Controlled, Triple 3x2 Audio/Video Crosspoint Switches

Table 1. Command-Byte Format

BIT	REGISTER
C7	Clickless Mode
C6	Bias
C5	COM2C
C4	COM1C
C3	COM2B
C2	COM1B
C1	COM2A
C0	COM1A

Audio off-isolation is -85dB at 20kHz, crosstalk is -85dB at 20kHz, and video off-isolation is -62dB at 10MHz. The SA, SB, and SC (shunt) inputs further improve off-isolation, allowing for the addition of external shunt capacitors to connect the outputs to AC grounds. When using the bias resistors, MID_ inputs improve crosstalk by providing an AC ground at the common bias points. Resistance from the bias points to the inputs allows AC signals to pass through the device and improve crosstalk performance (refer to the *Functional Diagram*). These devices feature a clickless operation mode for noiseless audio switching. Use the serial interface to select the clickless or standard-switching mode for each individual output.

Table 2. COM Data-Byte Format (C0, C1, C2, C3, C4, C5 = "1")

BIT	DESCRIPTION	POWER-UP DEFAULT STATE
D7	Don't care	—
D6	Don't care	—
D5	Don't care	—
D4	Don't care	—
D3	Controls the switch connected to S_; 1 = close switch, 0 = open switch.	1
D2	Controls the switch connected to NO3_; 1 = close switch, 0 = open switch.	0
D1	Controls the switch connected to NO2_; 1 = close switch, 0 = open switch.	0
D0	Controls the switch connected to NO1_; 1 = close switch, 0 = open switch.	0

Applications Information

The MAX4548/MAX4549 are divided into five functional blocks: the control-logic block, three switch-matrix blocks, and the bias-resistor block (see *Functional Diagram*). The control-logic block accepts commands through the serial interface and uses those commands to control the four remaining blocks.

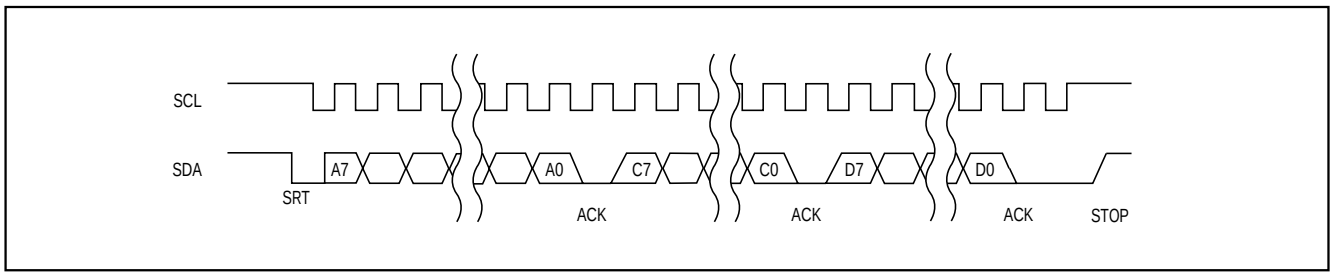


Figure 3. 2-Wire Serial-Interface Timing Diagram ("WriteByte")

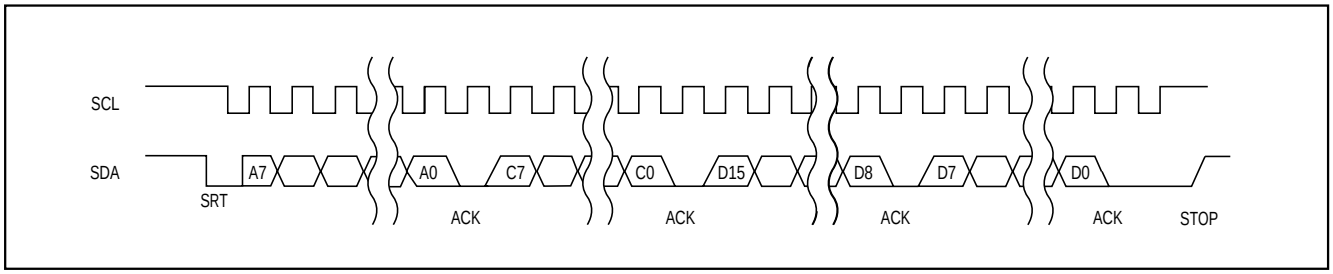


Figure 4. 2-Wire Serial-Interface Timing Diagram ("WriteWord")

Command-Byte and Data-Byte Programming

The devices are programmed with a command byte and a data byte or data word (2 bytes). Each bit of the command byte selects one of the functional blocks to be controlled by the subsequent data byte (word). The data byte (word) sets the state of the selected block(s). For the three switch-matrix blocks, the data byte sets the switch state. For the bias-resistor block, the data word controls which bias network is active (see *Functional Diagram*).

A logic "1" in any bit position of the data byte makes that function active, while a logic "0" makes it inactive. Tables 1–4 describe the command byte and the corresponding data byte. If more than one bit of the command byte is set, the data byte programs all of the corresponding blocks. This operation is useful, for instance, to simultaneously set all switch matrices to

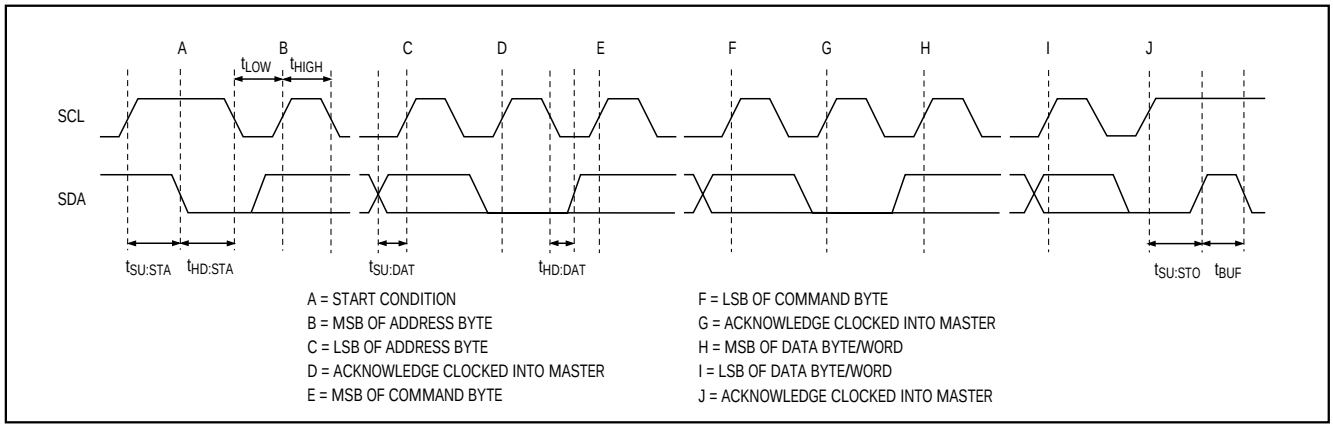


Figure 5. 2-Wire Serial-Interface Timing Details

Table 3. Bias Data-Byte (C6 = "1")

BIT	DESCRIPTION	POWER-UP DEFAULT STATE
D15	Don't care	–
D14	Don't care	–
D13	Don't care	–
D12	Don't care	–
D11	Controls SC bias resistors; 1 = connect bias resistors, 0 = disconnect bias resistors.	1
D10	Controls NO3C bias resistors; 1 = connect bias resistors, 0 = disconnect bias resistors.	1
D9	Controls NO2C bias resistors; 1 = connect bias resistors, 0 = disconnect bias resistors.	1
D8	Controls NO1C bias resistors; 1 = connect bias resistors, 0 = disconnect bias resistors.	1
D7	Controls SB bias resistors; 1 = connect bias resistors, 0 = disconnect bias resistors.	1
D6	Controls SA bias resistors; 1 = connect bias resistors, 0 = disconnect bias resistors.	1
D5	Controls NO3B bias resistors; 1 = connect bias resistors, 0 = disconnect bias resistors.	1
D4	Controls NO3A bias resistors; 1 = connect bias resistors, 0 = disconnect bias resistors.	1
D3	Controls NO2B bias resistors; 1 = connect bias resistors, 0 = disconnect bias resistors.	1
D2	Controls NO2A bias resistors; 1 = connect bias resistors, 0 = disconnect bias resistors.	1
D1	Controls NO1B bias resistors; 1 = connect bias resistors, 0 = disconnect bias resistors.	1
D0	Controls NO1A bias resistors; 1 = connect bias resistors, 0 = disconnect bias resistors.	1

Serially Controlled, Triple 3x2 Audio/Video Crosspoint Switches

Table 4. Clickless Mode Format (C7 = “1”)

BIT	DESCRIPTION	POWER-UP DEFAULT STATE
D7	Don’t care	—
D6	Don’t care	—
D5	Controls COM2C clickless mode; 1 = enables clickless mode, 0 = disables clickless mode.	1
D4	Controls COM1C clickless mode; 1 = enables clickless mode, 0 = disables clickless mode.	1
D3	Controls COM2B clickless mode; 1 = enables clickless mode, 0 = disables clickless mode.	1
D2	Controls COM1B clickless mode; 1 = enables clickless mode, 0 = disables clickless mode.	1
D1	Controls COM2A clickless mode; 1 = enables clickless mode, 0 = disables clickless mode.	1
D0	Controls COM1A clickless mode; 1 = enables clickless mode, 0 = disables clickless mode.	1

Table 5. “WriteByte” Protocol

	ADDRESS BYTE									COMMAND BYTE									DATA BYTE									
	A7	A6	A5	A4	A3	A2	A1	A0		C7	C6	C5	C4	C3	C2	C1	C0		D7	D6	D5	D4	D3	D2	D1	D0		
SRT	1	0	0	1	1	A1	A0	0	ACK	CLICK	BIAS	COM2C	COM1C	COM2B	COM1B	COM2A	COM1A	ACK									ACK	STOP

SRT = Start Condition
ACK = Acknowledge Condition
STOP = Stop Condition

Table 6. “WriteWord” Protocol

	ADDRESS BYTE									COMMAND BYTE									DATA WORD															
	A7	A6	A5	A4	A3	A2	A1	A0		C7	C6	C5	C4	C3	C2	C1	C0		D15	D14	D13	D12	D11	D10	D9	D8		D7	D6	D5	D4	D3	D2	D1	D0		
SRT	1	0	0	1	1	A1	A0	0	ACK	CLICK	BIAS	COM2C	COM1C	COM2B	COM1B	COM2A	COM1A	ACK									ACK									ACK	STOP

SRT = Start Condition
ACK = Acknowledge Condition
STOP = Stop Condition

Table 7. “SPI” Protocol

COMMAND BYTE									DATA WORD																
C7	C6	C5	C4	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CLICK	BIAS	COM2C	COM1C	COM2B	COM1B	COM2A	COM1A																

SRT = Start Condition
ACK = Acknowledge Condition
STOP = Stop Condition

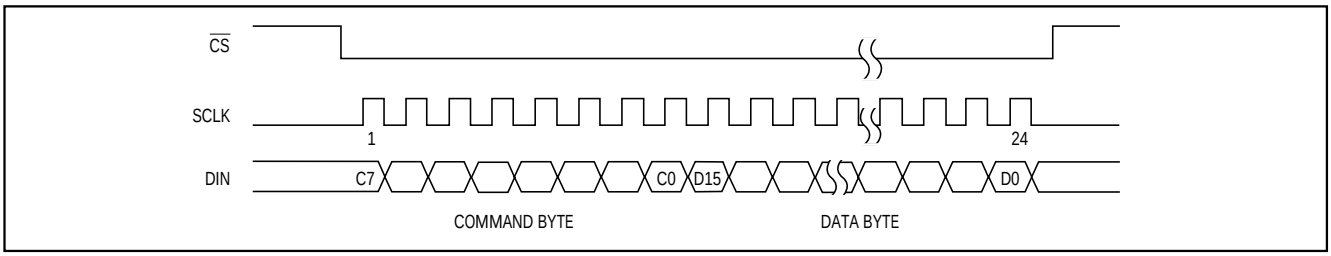


Figure 6. 3-Wire Serial-Interface Communication

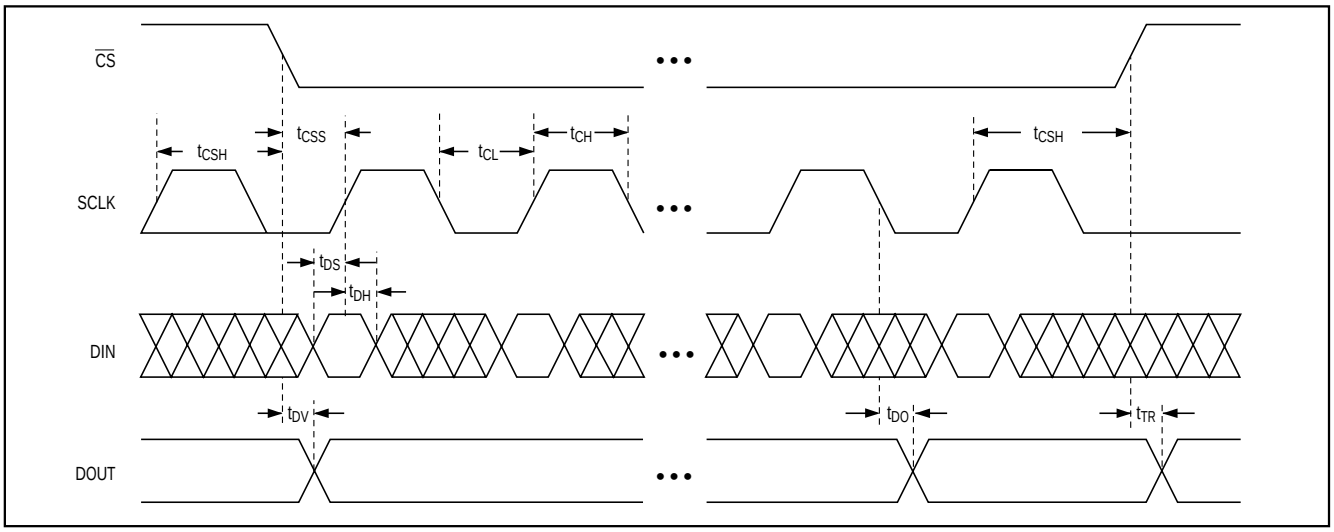


Figure 7. 3-Wire Serial-Interface Timing Details

the same configuration. Any block that is not selected in the command byte remains unchanged.

2-Wire Serial Interface

The MAX4548 uses a 2-wire I^{2}C-compatible serial interface. The COM_ _ registers and the Clickless Mode register use the "WriteByte" protocol, which consists of an address byte, followed by a command byte, followed by a data byte (Table 5). The Bias register uses the "WriteWord" protocol, which consists of an address byte, followed by a command byte, followed by a data word (Table 6).

To address a given chip, the A0 and A1 bits in the address byte must duplicate the values present at the A0 and A1 pins of that chip. The rest of the address bits must match those shown in Tables 5 and 6. The command and data-byte details are described in the *Command-Byte and Data-Byte Programming* section.

The 2-wire serial interface requires only two I/O lines of a standard microprocessor port. Figures 3, 4, and 5 detail the timing diagram for signals on the 2-wire bus, while Tables 5 and 6 detail the format of the signals. The MAX4548 is a receive-only device and must be controlled by the bus master device. A bus master device communicates by transmitting the address byte of the slave device over the bus and then transmitting the desired information. Each transmission consists of a start condition, a command byte, a data byte or word, and finally a stop condition. The slave device acknowledges the recognition of its address by pulling the SDA line low for one clock period after the address byte is transmitted. The slave device also issues a similar acknowledgment after the command byte and again after each data byte.

Start and Stop Conditions

The bus master signals the beginning of a transmission with a start condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a stop condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Serially Controlled, Triple 3x2 Audio/Video Crosspoint Switches

Slave Address (Address Byte)

The MAX4548 uses an 8-bit slave address. To select a slave address, connect A0 and A1 to V+ or GND. The MAX4548 has four possible slave addresses, thus a maximum of four of these devices may share the same 2-bit address bus. The slave devices on the MAX4548 monitor the serial bus continuously, waiting for a start condition followed by an address byte. When a slave device recognizes its address, it acknowledges that it is ready for further communication by pulling the SDA line low for one clock period.

3-Wire Serial Interface

The MAX4549 3-wire serial interface is SPI/QSPI/MICROWIRE-compatible. An active-low chip-select ($\overline{CS}$) input enables the device to receive data for the serial input (DIN). Data is clocked in on the rising edge of the serial-clock (SCLK) signal. A total of 24 bits is needed in each write cycle. Segmented write cycles are allowed (three 8-bit-wide transfers) if $\overline{CS}$ remains low. The first bit clock into the MAX4549 is the command byte's MSB, and the last bit clocked in is the data byte's LSB. When programming the COM_ _ registers and the Clickless Mode register, the last eight bits of the data word are "don't care." While shifting data, the device remains in its original configuration. After all 24 bits are clocked into the input shift register, a rising edge on $\overline{CS}$ latches the data into the MAX4549 internal registers, initiating the device's change of state. Figures 6 and 7 and Table 7 show the details of the 3-wire protocol, as it applies to the MAX4549.

DOUT is the shift register's output. Data at DOUT is simply the input data delayed by 24 clock cycles, with data appearing synchronous with SCLK's falling edge. Transitions at DIN and SCLK have no effect when $\overline{CS}$ is high, and DOUT holds the last bit in the shift register.

Daisy-Chaining

To program several MAX4549s, "daisy-chain" the devices by connecting DOUT of the first device to DIN of the second, and so on. The $\overline{CS}$ pins of all devices are connected together, and data is shifted through the MAX4549 in series. Twenty-four bits of data per device are required for proper programming of all devices. When $\overline{CS}$ is brought high, all devices are updated simultaneously.

Addressable Serial Interface

To program several MAX4549s individually using a single processor, connect the DIN pins of each MAX4549 together and control $\overline{CS}$ on each MAX4549 separately. To select a particular device, drive the corresponding $\overline{CS}$ low, clock in the 24-bit command, then drive $\overline{CS}$ high to execute the command. Typically only one MAX4549 is addressed at a time.

Improving Off-Isolation

To improve off-isolation, connect the S_ input to ground either directly (DC ground) or through capacitors (AC ground). Closing S_ then effectively grounds the unused outputs.

Using the Internal Bias Resistors

Use the internal bias-resistor networks to give the switch outputs a DC bias when the switch terminals are AC-coupled. Programming the switches that connect the bias resistors to the inputs is accomplished via bit C6 of the command byte. Connect _BIASH and _BIASL inputs to DC levels (for example, V+ and GND), and activate the switch connecting the appropriate outputs. This applies a voltage midway between _BIASH and _BIASL to the input (refer to Tables 1 and 4, and the *Functional Diagram*). To improve crosstalk when using the bias resistors, connect the MID_ inputs to ground through capacitors.

Clickless Switching

Audible switching transients ("clicks") are eliminated in this mode of operation. When an output is configured as "clickless," the gate signal of the switches connected to the output are controlled with slow-moving voltages. As a result, the output slew rates are significantly reduced. Program clickless operation via bit C7 of the command byte (refer to Tables 1 and 4, and the *Functional Diagram*). Each operating switch may draw 2mA during a transition. When another command is given while a switch is changing state in the soft mode, the MAX4548/MAX4549 will complete the previous command in the hard mode. To avoid this situation, do not issue a second command until the transition of the switch is complete.

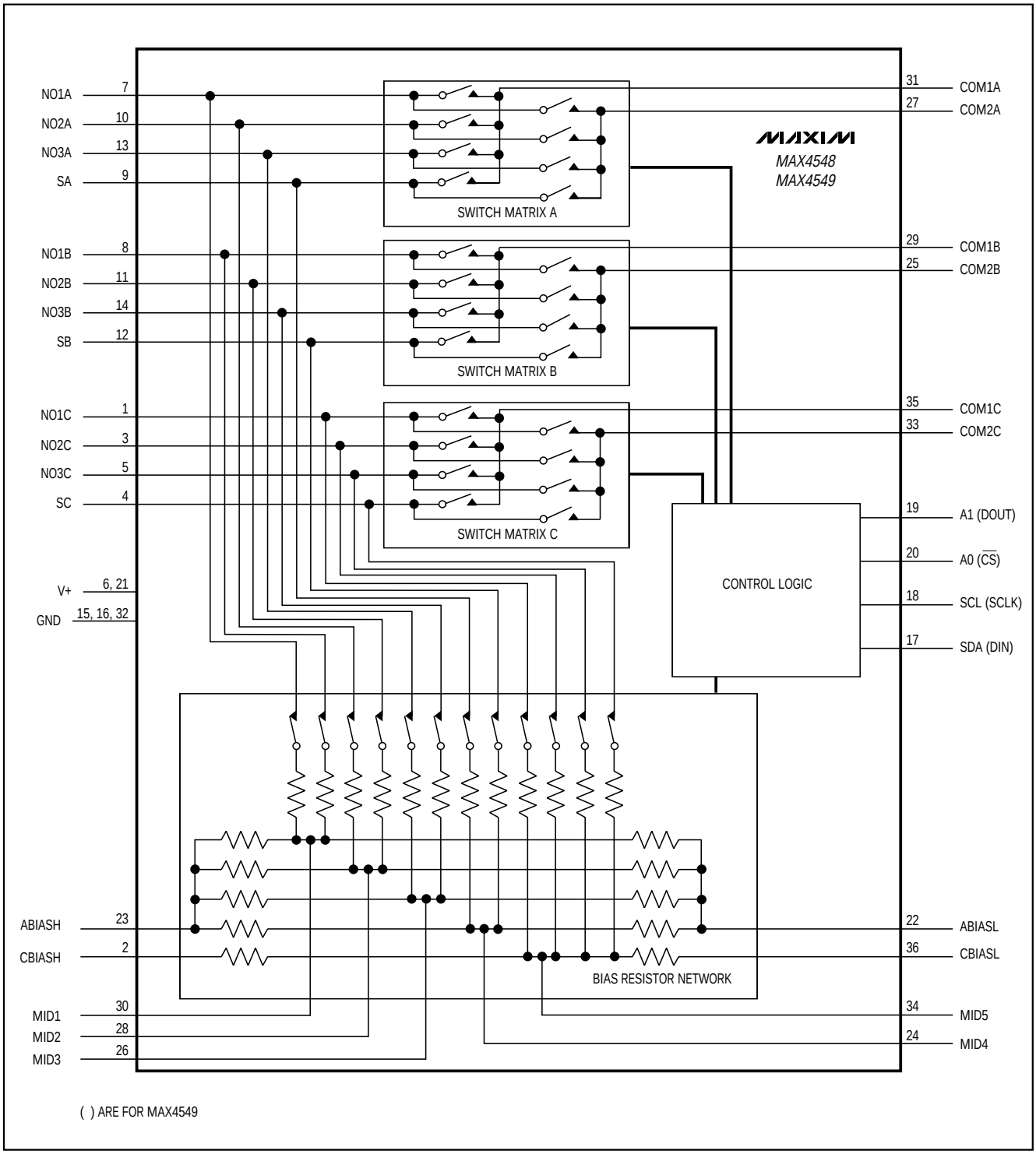
Power-Up State

The MAX4548/MAX4549 feature a preset power-up state. Refer to Tables 2, 3, and 4 to determine the power-up state of the devices.

Bypass Capacitors

The MAX4548/MAX4549 have five bypass pins for the internal bias resistor networks (MID_). The equivalent AC impedance at these pins is 10kΩ. To improve crosstalk performance, bypass MID_ pins with 10µF. For lowest cost, standard aluminum electrolytic capacitors in parallel with 0.1µF ceramic chip capacitors perform well in audio applications. For computer audio applications, a single 1µF capacitor is sufficient. For telecom voice applications, a 0.1µF capacitor is adequate. For video applications, bypass MID_ with 0.1µF in parallel with 1000pF. This provides a low impedance across the entire video bandwidth.

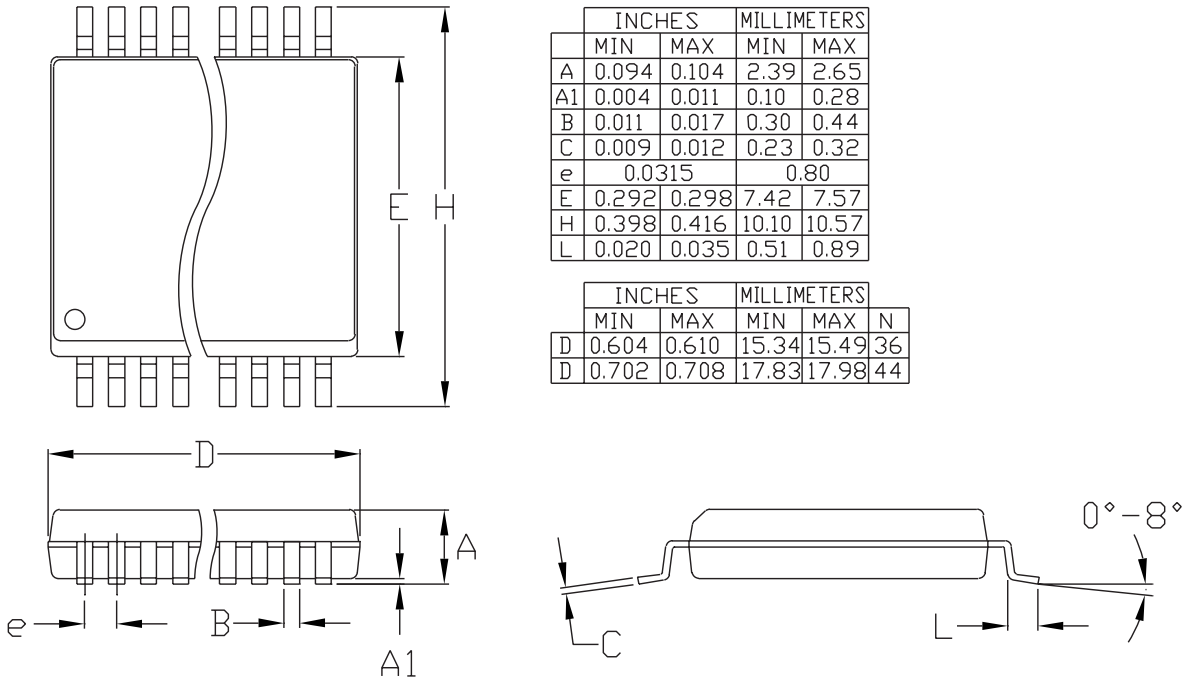
Functional Diagram



Serially Controlled, Triple 3x2 Audio/Video Crosspoint Switches

Package Information

SSOP.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.094	0.104	2.39	2.65
A1	0.004	0.011	0.10	0.28
B	0.011	0.017	0.30	0.44
C	0.009	0.012	0.23	0.32
e	0.0315		0.80	
E	0.292	0.298	7.42	7.57
H	0.398	0.416	10.10	10.57
L	0.020	0.035	0.51	0.89

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.604	0.610	15.34	15.49	36
D	0.702	0.708	17.83	17.98	44

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. N = NUMBER OF PINS

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, SSOP, 36/44L, .300X8mm

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0040	B	1/1

Chip Information

TRANSISTOR COUNT: 7700

SUBSTRATE IS INTERNALLY CONNECTED TO V+.

NOTES

NOTES

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