



**THE DATASHEET OF  
MAX4092ASA+T**





# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

## General Description

The single MAX4091, dual MAX4092, and quad MAX4094 operational amplifiers combine excellent DC accuracy with Rail-to-Rail® operation at the input and output. Since the common-mode voltage extends from V<sub>CC</sub> to V<sub>EE</sub>, the devices can operate from either a single supply (2.7V to 6V) or split supplies ( $\pm 1.35V$  to  $\pm 3V$ ). Each op amp requires less than 130 $\mu A$  of supply current. Even with this low current, the op amps are capable of driving a 1k $\Omega$  load, and the input-referred voltage noise is only 12nV/ $\sqrt{Hz}$ . In addition, these op amps can drive loads in excess of 2000pF.

The precision performance of the MAX4091/MAX4092/MAX4094 combined with their wide input and output dynamic range, low-voltage, single-supply operation, and very low supply current, make them an ideal choice for battery-operated equipment, industrial, and data acquisition and control applications. In addition, the MAX4091 is available in space-saving 5-pin SOT23, 8-pin  $\mu$ MAX, and 8-pin SO packages. The MAX4092 is available in 8-pin  $\mu$ MAX and SO packages, and the MAX4094 is available in 14-pin TSSOP and 14-pin SO packages.

## Applications

Portable Equipment  
 Battery-Powered Instruments  
 Data Acquisition and Control  
 Low-Voltage Signal Conditioning

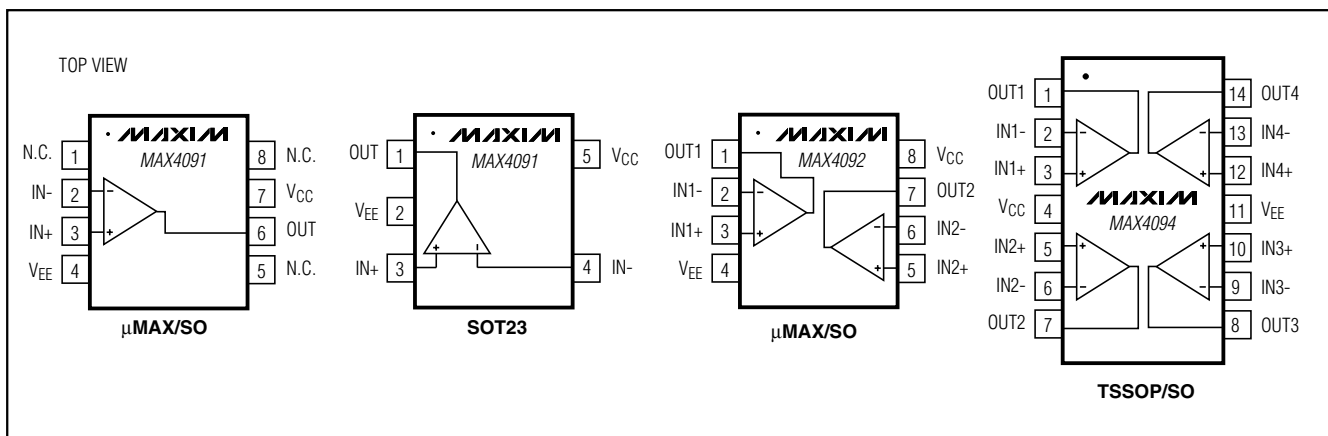
## Features

- ◆ Low-Voltage, Single-Supply Operation (2.7V to 6V)
- ◆ Beyond-the-Rails™ Inputs
- ◆ No Phase Reversal for Overdriven Inputs
- ◆ 30 $\mu V$  Offset Voltage
- ◆ Rail-to-Rail Output Swing with 1k $\Omega$  Load
- ◆ Unity-Gain Stable with 2000pF Load
- ◆ 165 $\mu A$  (max) Quiescent Current Per Op Amp
- ◆ 500kHz Gain-Bandwidth Product
- ◆ High Voltage Gain (115dB)
- ◆ High Common-Mode Rejection Ratio (90dB) and Power-Supply Rejection Ratio (100dB)
- ◆ Temperature Range (-40°C to +125°C)

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4091AUK-T	-40°C to +125°C	5 SOT23-5
MAX4091ASA	-40°C to +125°C	8 SO
MAX4091AUA	-40°C to +125°C	8 $\mu$ MAX
MAX4092ASA	-40°C to +125°C	8 SO
MAX4092AUA	-40°C to +125°C	8 $\mu$ MAX
MAX4094AUD	-40°C to +125°C	14 TSSOP
MAX4094ASD	-40°C to +125°C	14 SO

## Pin Configurations/Functional Diagrams



Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.  
 Beyond-the-Rails is a trademark of Maxim Integrated Products, Inc.



# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC to VEE).....7V	8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
Common-Mode Input Voltage.....(VCC + 0.3V) to (VEE - 0.3V)	8-Pin μMAX (derate 4.1mW/°C above +70°C) .....330mW
Differential Input Voltage.....±(VCC - VEE)	14-Pin SO (derate 8.33mW/°C above +70°C).....667mW
Input Current (IN+, IN-) .....±10mA	14-Pin TSSOP (derate 9.1mW/°C above +70°C) .....727mW
Output Short-Circuit Duration	Operating Temperature Range .....-40°C to +125°C
OUT shorted to GND or VCC.....Continuous	Storage Temperature Range .....-65°C to +150°C
Continuous Power Dissipation (TA = +70°C)	Junction Temperature .....+150°C
5-Pin SOT23 (derate 7.1mW/°C above +70°C).....571mW	Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(VCC = 2.7V to 6V, VEE = GND, VCM = 0, VOUT = VCC/2, TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>DC CHARACTERISTICS</b>							
Supply Voltage Range	VCC	Inferred from PSRR test	2.7		6.0	V	
Supply Current	ICC	VCM = VCC/2	VCC = 2.7V	115	165	μA	
			VCC = 5V	130	185		
Input Offset Voltage	VOS	VCM = VEE to VCC		0.03	1.4	mV	
Input Bias Current	IB	VCM = VEE to VCC		20	180	nA	
Input Offset Current	IOS	VCM = VEE to VCC		0.2	7	nA	
Input Common-Mode Range	VCM	Inferred from CMRR test	VEE - 0.05		VCC + 0.05	V	
Common-Mode Rejection Ratio	CMRR	(VEE - 0.05V) ≤ VCM ≤ (VCC + 0.05V)	71	90		dB	
Power-Supply Rejection Ratio	PSRR	2.7V ≤ VCC ≤ 6V	86	100		dB	
Large-Signal Voltage Gain (Note 1)	AVOL	VCC = 2.7V, RL = 100kΩ 0.25V ≤ VOUT ≤ 2.45V	Sourcing	83	105	dB	
			Sinking	81	105		
		VCC = 2.7V, RL = 1kΩ 0.5V ≤ VOUT ≤ 2.2V	Sourcing	91	105		
			Sinking	78	90		
		VCC = 5.0V, RL = 100kΩ 0.25V ≤ VOUT ≤ 4.75V	Sourcing	87	115		
			Sinking	83	115		
		VCC = 5.0V, RL = 1kΩ 0.5V ≤ VOUT ≤ 4.5V	Sourcing	97	110		
			Sinking	84	100		
Output Voltage Swing High (Note 1)	VOH	VCC - VOUT	RL = 100kΩ		15	69	mV
			RL = 1kΩ		130	210	
Output Voltage Swing Low (Note 1)	VOL	VOUT - VEE	RL = 100kΩ		15	70	mV
			RL = 1kΩ		80	220	
<b>AC CHARACTERISTICS</b>							
Gain-Bandwidth Product	GBWP	RL = 100kΩ, CL = 100pF		500		kHz	
Phase Margin	φM	RL = 100kΩ, CL = 100pF		60		degrees	
Gain Margin		RL = 100kΩ, CL = 100pF		10		dB	
Slew Rate	SR	RL = 100kΩ, CL = 15pF		0.20		V/μs	

# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

MAX4091/MAX4092/MAX4094

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = 2.7V$  to  $6V$ ,  $V_{EE} = GND$ ,  $V_{CM} = 0$ ,  $V_{OUT} = V_{CC}/2$ ,  $T_A = +25^{\circ}C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Noise Voltage Density	$e_N$	$f = 10kHz$		12		$nV/\sqrt{Hz}$
Input-Noise Current Density		$f = 10kHz$		1.5		$pA/\sqrt{Hz}$
Noise Voltage (0.1Hz to 10Hz)				16		$\mu V_{RMS}$
Total Harmonic Distortion Plus Noise	THD + N	$f = 1kHz$ , $R_L = 10k\Omega$ , $C_L = 15pF$ , $A_V = 1$ , $V_{OUT} = 2V_{P-P}$		0.003		%
Capacitive-Load Stability	$C_{LOAD}$	$A_V = 1$		2000		pF
Settling Time	$t_s$	To 0.1%, 2V step		12		$\mu s$
Power-On Time	$t_{ON}$	$V_{CC} = 0$ to 3V step, $V_{IN} = V_{CC}/2$ , $A_V = 1$		2		$\mu s$
Op-Amp Isolation		$f = 1kHz$ (MAX4092/MAX4094)		125		dB

## ELECTRICAL CHARACTERISTICS

( $V_{CC} = 2.7V$  to  $6V$ ,  $V_{EE} = GND$ ,  $V_{CM} = 0$ ,  $V_{OUT} = V_{CC}/2$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values specified at  $T_A = +25^{\circ}C$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC CHARACTERISTICS</b>						
Supply Voltage Range	$V_{CC}$	Inferred from PSRR test	2.7		6.0	V
Supply Current	$I_{CC}$	$V_{CM} = V_{CC}/2$	$V_{CC} = 2.7V$		200	$\mu A$
			$V_{CC} = 5V$		225	
Input Offset Voltage	$V_{OS}$	$V_{CM} = V_{EE}$ to $V_{CC}$			$\pm 3.5$	mV
Input Offset Voltage Tempco	$\Delta V_{OS}/\Delta T$			$\pm 2$		$\mu V/^{\circ}C$
Input Bias Current	$I_B$	$V_{CM} = V_{EE}$ to $V_{CC}$			$\pm 200$	nA
Input Offset Current	$I_{OS}$	$V_{CM} = V_{EE}$ to $V_{CC}$			$\pm 20$	nA
Input Common-Mode Range	$V_{CM}$	Inferred from CMRR test	$V_{EE} - 0.05$		$V_{CC} + 0.05$	V
Common-Mode Rejection Ratio	CMRR	$(V_{EE} - 0.05V) \leq V_{CM} \leq (V_{CC} + 0.05V)$	62			dB
Power-Supply Rejection Ratio	PSRR	$2.7V \leq V_{CC} \leq 6V$	80			dB
Large-Signal Voltage Gain (Note 1)	$A_{VOL}$	$V_{CC} = 2.7V$ , $R_L = 100k\Omega$ , $0.25V \leq V_{OUT} \leq 2.45V$	Sourcing	82		dB
			Sinking	80		
		$V_{CC} = 2.7V$ , $R_L = 1k\Omega$ , $0.5V \leq V_{OUT} \leq 2.2V$	Sourcing	90		
			Sinking	76		
		$V_{CC} = 5V$ , $R_L = 100k\Omega$ , $0.25V \leq V_{OUT} \leq 4.75V$	Sourcing	86		
			Sinking	82		
$V_{CC} = 5V$ , $R_L = 1k\Omega$ , $0.5V \leq V_{OUT} \leq 4.5V$	Sourcing	94				
	Sinking	80				
Output Voltage Swing High (Note 1)	$V_{OH}$	$ V_{CC} - V_{OUT} $	$R_L = 100k\Omega$		75	mV
			$R_L = 1k\Omega$		250	
Output Voltage Swing Low (Note 1)	$V_{OL}$	$ V_{OUT} - V_{EE} $	$R_L = 100k\Omega$		75	mV
			$R_L = 1k\Omega$		250	

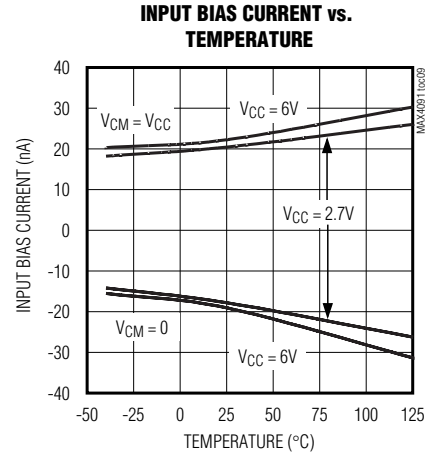
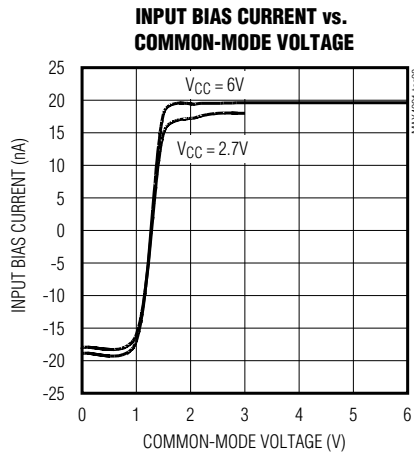
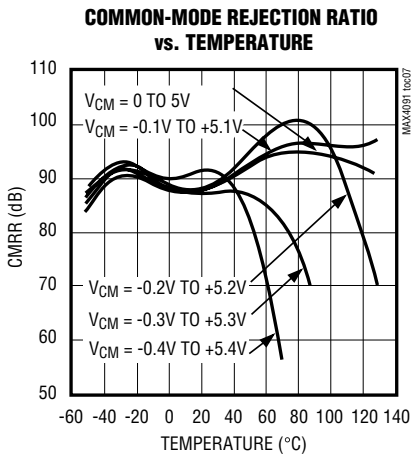
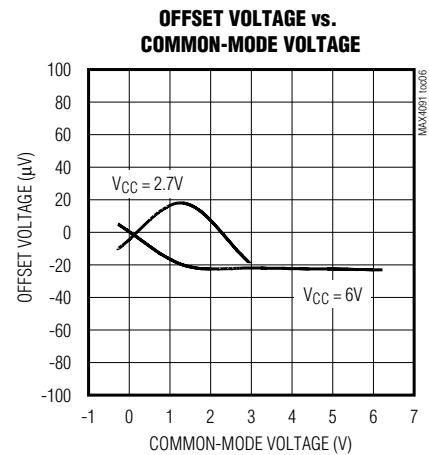
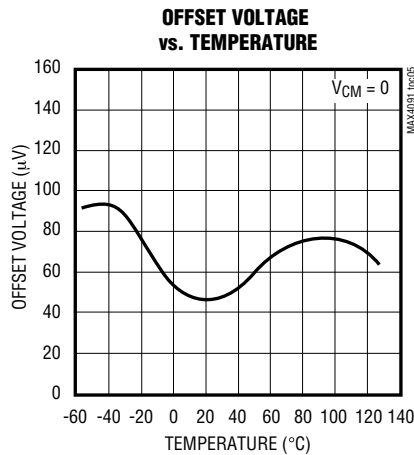
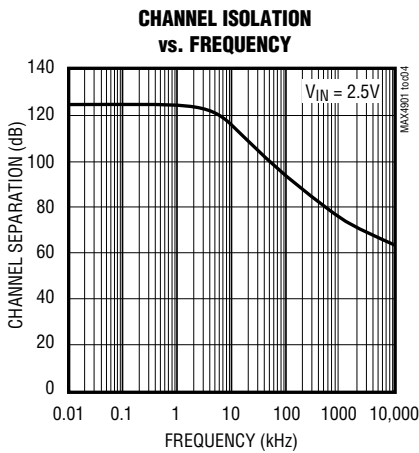
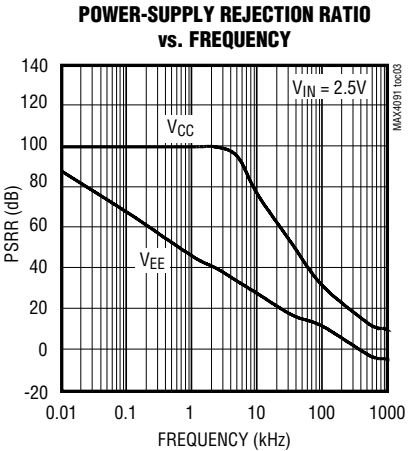
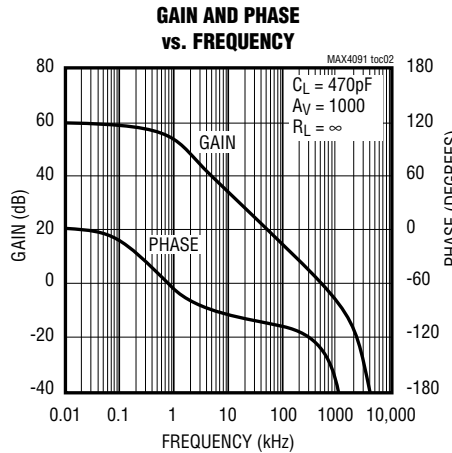
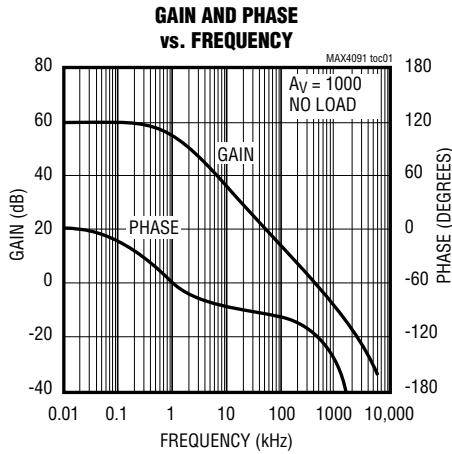
**Note 1:**  $R_L$  is connected to  $V_{EE}$  for  $A_{VOL}$  sourcing and  $V_{OH}$  tests.  $R_L$  is connected to  $V_{CC}$  for  $A_{VOL}$  sinking and  $V_{OL}$  tests.

**Note 2:** All specifications are 100% tested at  $T_A = +25^{\circ}C$ . Specification limits over temperature ( $T_A = T_{MIN}$  to  $T_{MAX}$ ) are guaranteed by design, not production tested.

# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

## Typical Operating Characteristics

( $V_{CC} = 5V$ ,  $V_{EE} = 0$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



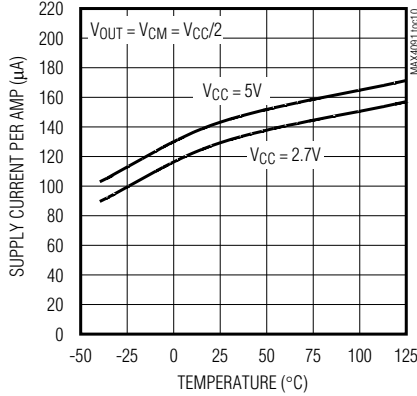
# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

## Typical Operating Characteristics (continued)

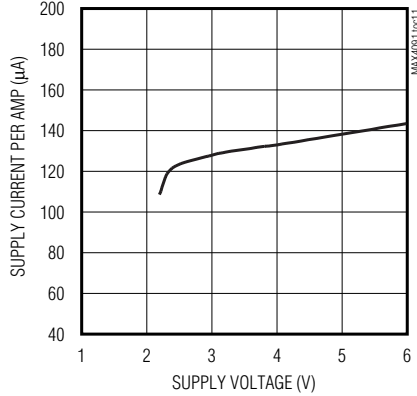
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MAX4091/MAX4092/MAX4094

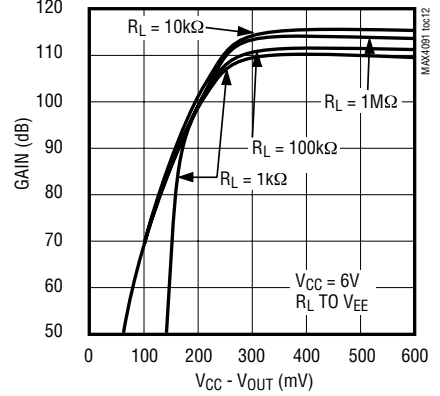
**SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE**



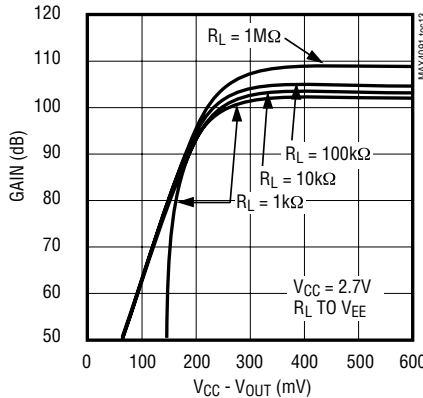
**SUPPLY CURRENT PER AMPLIFIER vs. SUPPLY VOLTAGE**



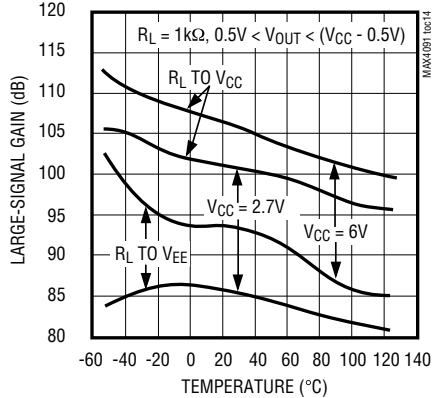
**LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE**



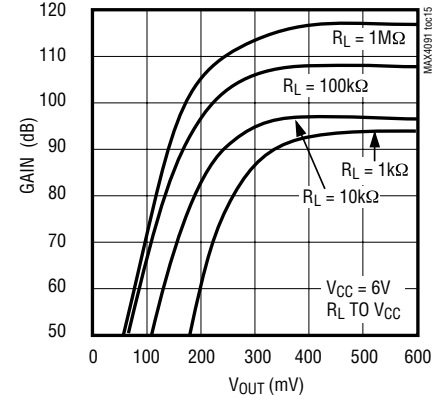
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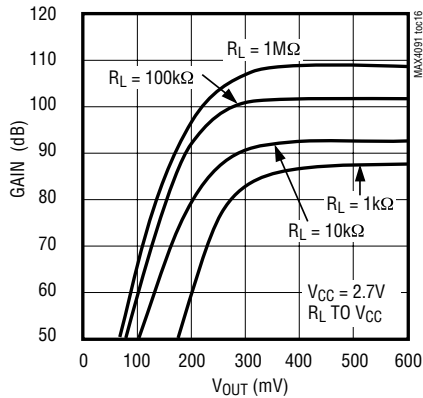
**LARGE-SIGNAL GAIN vs. TEMPERATURE**



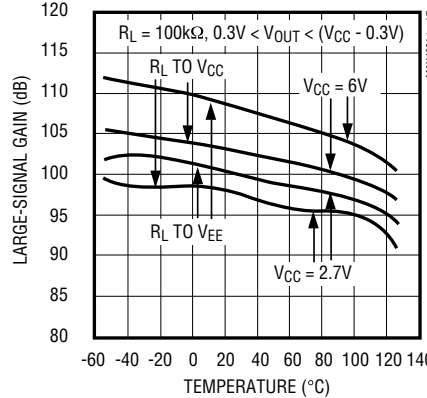
**LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE**



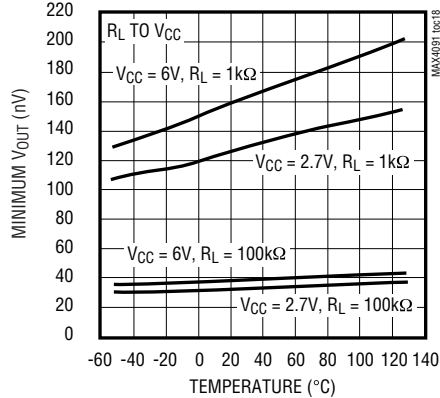
**LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE**



**LARGE-SIGNAL GAIN vs. TEMPERATURE**



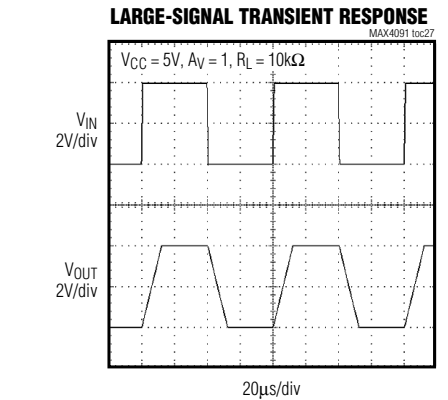
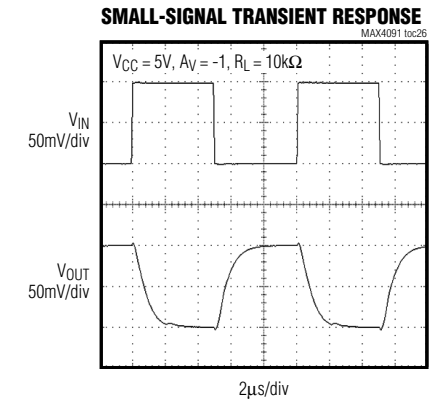
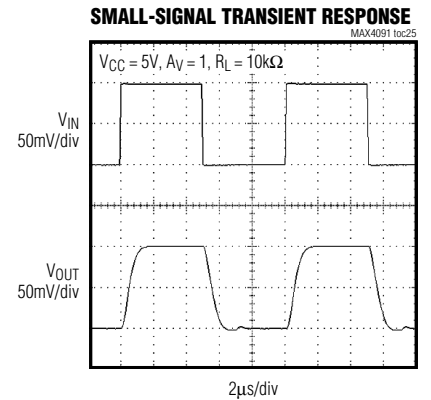
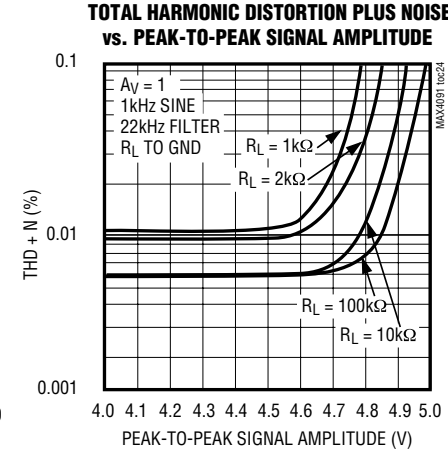
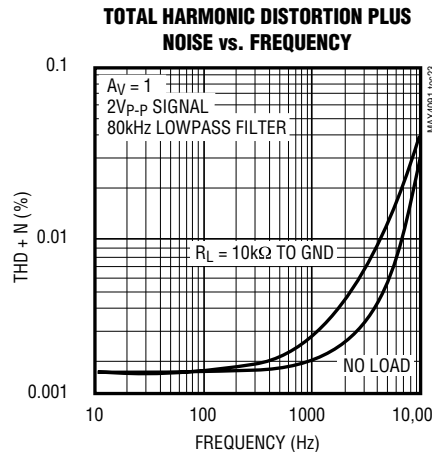
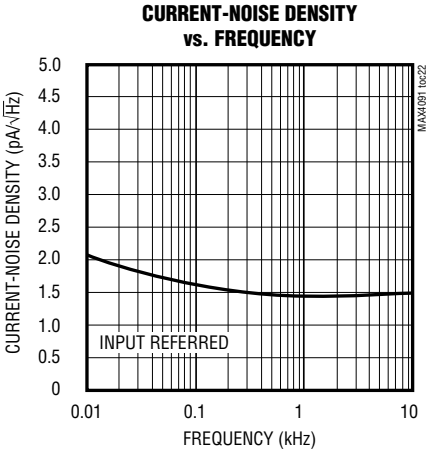
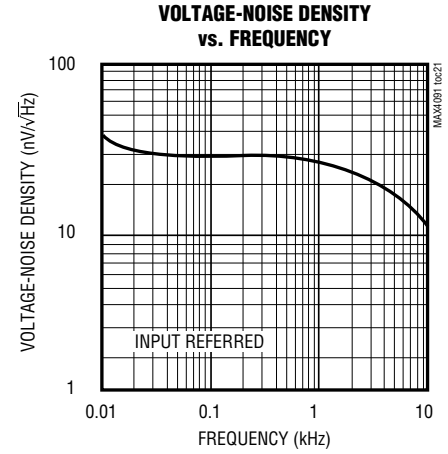
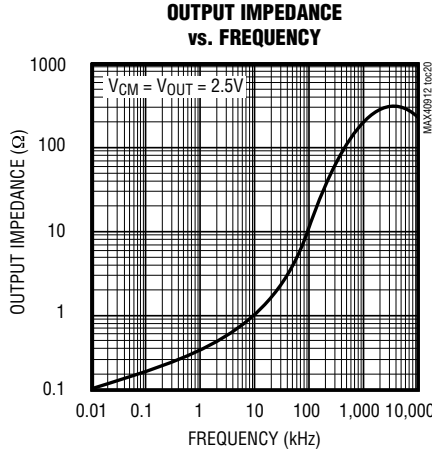
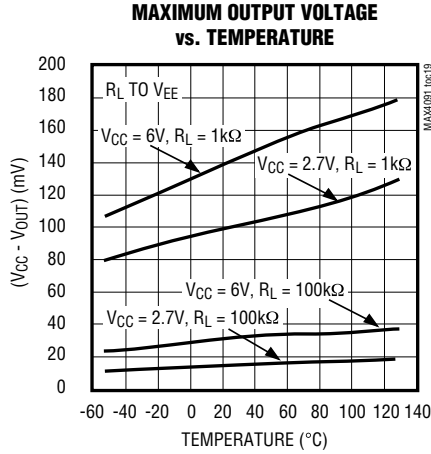
**MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE**



# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

## Typical Operating Characteristics (continued)

( $V_{CC} = 5V$ ,  $V_{EE} = 0$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

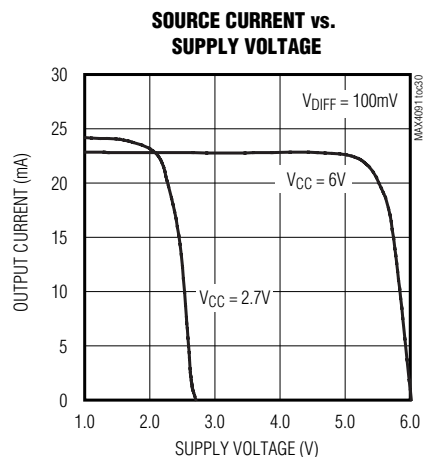
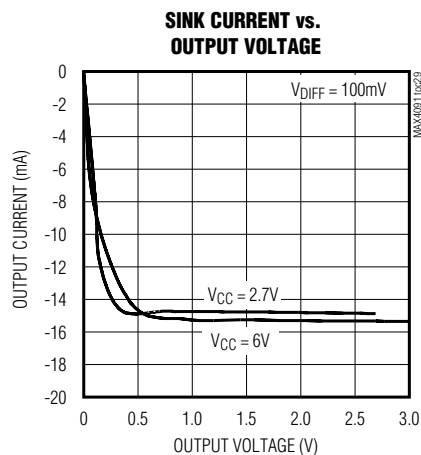
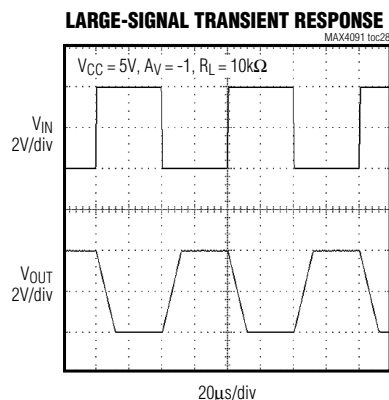


# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

## Typical Operating Characteristics (continued)

( $V_{CC} = 5V$ ,  $V_{EE} = 0$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

MAX4091/MAX4092/MAX4094



## Pin Description

PIN				NAME	FUNCTION
MAX4091 SOT23	MAX4091 SO/ $\mu$ MAX	MAX4092	MAX4094		
1	6	—	—	OUT	Amplifier Output
2	4	4	11	$V_{EE}$	Negative Supply
3	3	—	—	IN+	Noninverting Input
4	2	—	—	IN-	Inverting Input
5	7	8	4	$V_{CC}$	Positive Supply
—	1, 5, 8	—	—	N.C.	No Connection. Not internally connected.
—	—	1	1	OUT1	Amplifier 1 Output
—	—	2	2	IN1-	Amplifier 1 Inverting Input
—	—	3	3	IN1+	Amplifier 1 Noninverting Input
—	—	5	5	IN2+	Amplifier 2 Noninverting Input
—	—	6	6	IN2-	Amplifier 2 Inverting Input
—	—	7	7	OUT2	Amplifier 2 Output
—	—	—	8	OUT3	Amplifier 3 Output
—	—	—	9	IN3-	Amplifier 3 Inverting Input
—	—	—	10	IN3+	Amplifier 3 Noninverting Input
—	—	—	12	IN4+	Amplifier 4 Noninverting Input
—	—	—	13	IN4-	Amplifier 4 Inverting Input
—	—	—	14	OUT4	Amplifier 4 Output

# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

## Detailed Description

The single MAX4091, dual MAX4092 and quad MAX4094 op amps combine excellent DC accuracy with rail-to-rail operation at both input and output. With their precision performance, wide dynamic range at low supply voltages, and very low supply current, these op amps are ideal for battery-operated equipment, industrial, and data acquisition and control applications.

## Applications Information

### Rail-to-Rail Inputs and Outputs

The MAX4091/MAX4092/MAX4094's input common-mode range extends 50mV beyond the positive and negative supply rails, with excellent common-mode rejection. Beyond the specified common-mode range, the outputs are guaranteed not to undergo phase reversal or latchup. Therefore, the MAX4091/MAX4092/MAX4094 can be used in applications with common-mode signals, at or even beyond the supplies, without the problems associated with typical op amps.

The MAX4091/MAX4092/MAX4094's output voltage swings to within 15mV of the supplies with a 100k $\Omega$  load. This rail-to-rail swing at the input and the output substantially increases the dynamic range, especially in low-supply-voltage applications. Figure 1 shows the input and output waveforms for the MAX4092, configured as a unity-gain noninverting buffer operating from a single 3V supply. The input signal is 3.0V<sub>p-p</sub>, a 1kHz sinusoid centered at 1.5V. The output amplitude is approximately 2.98V<sub>p-p</sub>.

### Input Offset Voltage

Rail-to-rail common-mode swing at the input is obtained by two complementary input stages in parallel, which feed a folded cascaded stage. The PNP stage is active for input voltages close to the negative rail, and the NPN stage is active for input voltages close to the positive rail.

The offsets of the two pairs are trimmed. However, there is some residual mismatch between them. This mismatch results in a two-level input offset characteristic, with a transition region between the levels occurring at a common-mode voltage of approximately 1.3V above  $V_{EE}$ . Unlike other rail-to-rail op amps, the transition region has been widened to approximately 600mV in order to minimize the slight degradation in CMRR caused by this mismatch.

The input bias currents of the MAX4091/MAX4092/MAX4094 are typically less than 20nA. The bias current flows into the device when the NPN input stage is active, and it flows out when the PNP input stage is active. To reduce the offset error caused by input bias current flowing through external source resistances,

match the effective resistance seen at each input. Connect resistor R3 between the noninverting input and ground when using the op amp in an inverting configuration (Figure 2a); connect resistor R3 between the noninverting input and the input signal when using the op amp in a noninverting configuration (Figure 2b). Select R3 to equal the parallel combination of R1 and R2. High source resistances will degrade noise performance, due to the the input current noise (which is multiplied by the source resistance).

### Input Stage Protection Circuitry

The MAX4091/MAX4092/MAX4094 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of back-to-back diodes between IN+ and IN- with two 1.7k $\Omega$  resistors in series (Figure 3). The diodes limit the differential voltage applied to the amplifiers' internal circuitry to no more than  $V_F$ , where  $V_F$  is the diodes' forward-voltage drop (about 0.7V at +25°C).

Input bias current for the ICs ( $\pm 20$ nA) is specified for small differential input voltages. For large differential input voltages (exceeding  $V_F$ ), this protection circuitry increases the input current at IN+ and IN-:

$$\text{INPUT CURRENT} = \frac{[(V_{IN+}) - (V_{IN-})] - V_F}{2 \times 1.7\text{k}\Omega}$$

### Output Loading and Stability

Even with their low quiescent current of less than 130 $\mu$ A per op amp, the MAX4091/MAX4092/MAX4094 are well suited for driving loads up to 1k $\Omega$  while maintaining DC accuracy. Stability while driving heavy capacitive loads is another key advantage over comparable CMOS rail-to-rail op amps.

In op amp circuits, driving large capacitive loads increases the likelihood of oscillation. This is especially true for circuits with high-loop gains, such as a unity-gain voltage follower. The output impedance and a capacitive load form an RC network that adds a pole to the loop response and induces phase lag. If the pole frequency is low enough—as when driving a large capacitive load—the circuit phase margin is degraded, leading to either an under-damped pulse response or oscillation.

The MAX4091/MAX4092/MAX4094 can drive capacitive loads in excess of 2000pF under certain conditions (Figure 4). When driving capacitive loads, the greatest potential for instability occurs when the op amp is sourcing approximately 200 $\mu$ A. Even in this case, stability is maintained with up to 400pF of output capaci-

# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

MAX4091/MAX4092/MAX4094

tance. If the output sources either more or less current, stability is increased. These devices perform well with a 1000pF pure capacitive load (Figure 5). Figures 6a, 6b, and 6c show the performance with a 500pF load in parallel with various load resistors.

To increase stability while driving large-capacitive loads, connect a pullup resistor to  $V_{CC}$  at the output to decrease the current the amplifier must source. If the amplifier is made to sink current rather than source, stability is further increased.

Frequency stability can be improved by adding an output isolation resistor ( $R_S$ ) to the voltage-follower circuit (Figure 7). This resistor improves the phase margin of the circuit by isolating the load capacitor from the op amp's output. Figure 8a shows the MAX4092 driving 5000pF ( $R_L \geq 100k\Omega$ ), while Figure 8b adds a 47 $\Omega$  isolation resistor.

Because the MAX4091/MAX4092/MAX4094 have excellent stability, no isolation resistor is required, except in the most demanding applications. This is beneficial because an isolation resistor would degrade the low-frequency performance of the circuit.

## Power-Up Settling Time

The MAX4091/MAX4092/MAX4094 have a typical supply current of 130 $\mu$ A per op amp. Although supply current is already low, it is sometimes desirable to reduce it further by powering down the op amp and associated ICs for periods of time. For example, when using a MAX4092 to buffer the inputs of a multi-channel analog-to-digital converter (ADC), much of the circuitry could be powered down between data samples to increase battery life. If samples are taken infrequently, the op amps, along with the ADC, may be powered down most of the time.

When power is reapplied to the MAX4091/MAX4092/

MAX4094, it takes some time for the voltages on the supply pin and the output pin of the op amp to settle. Supply settling time depends on the supply voltage, the value of the bypass capacitor, the output impedance of the incoming supply, and any lead resistance or inductance between components. Op amp settling time depends primarily on the output voltage and is slew-rate limited. With the noninverting input to a voltage follower held at midsupply (Figure 9), when the supply steps from 0 to  $V_{CC}$ , the output settles in approximately 2 $\mu$ s for  $V_{CC} = 3V$  (Figure 10a) and 8 $\mu$ s for  $V_{CC} = 5V$  (Figure 10b).

## Power Supplies and Layout

The MAX4091/MAX4092/MAX4094 operate from a single 2.7V to 6V power supply, or from dual supplies of  $\pm 1.35V$  to  $\pm 3V$ . For single-supply operation, bypass the power supply with a 0.1 $\mu$ F capacitor. If operating from dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize both trace lengths and resistor leads and place external components close to the op amp's pins.

## Chip Information

MAX4091 TRANSISTOR COUNT: 168

MAX4092 TRANSISTOR COUNT: 336

MAX4094 TRANSISTOR COUNT: 670

PROCESS: Bipolar

# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

## Test Circuits/Timing Diagrams

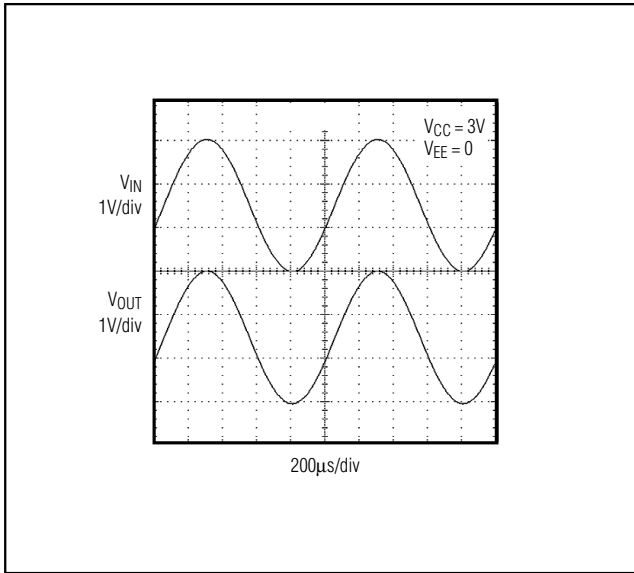


Figure 1. Rail-to-Rail Input and Output Operation

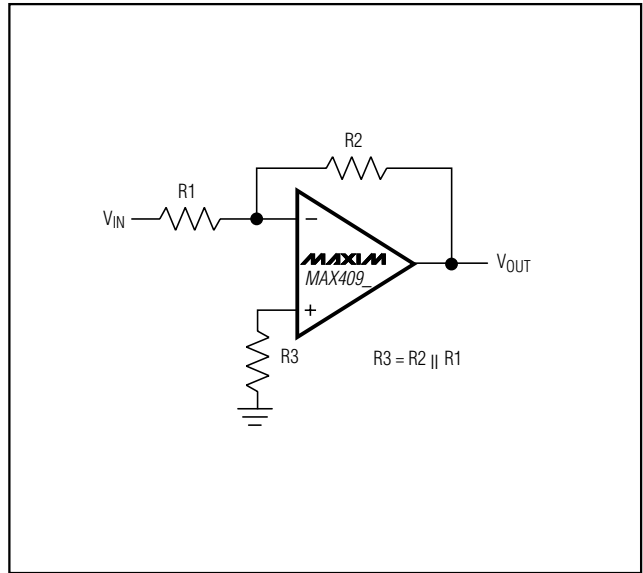


Figure 2a. Reducing Offset Error Due to Bias Current: Inverting Configuration

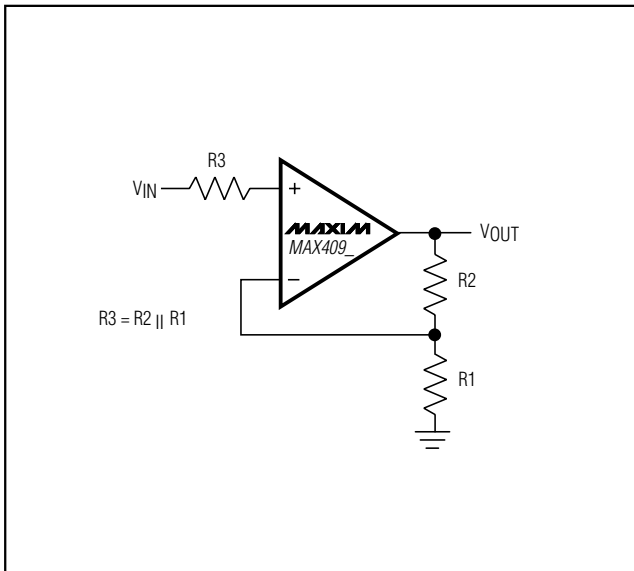


Figure 2b. Reducing Offset Error Due to Bias Current: Noninverting Configuration

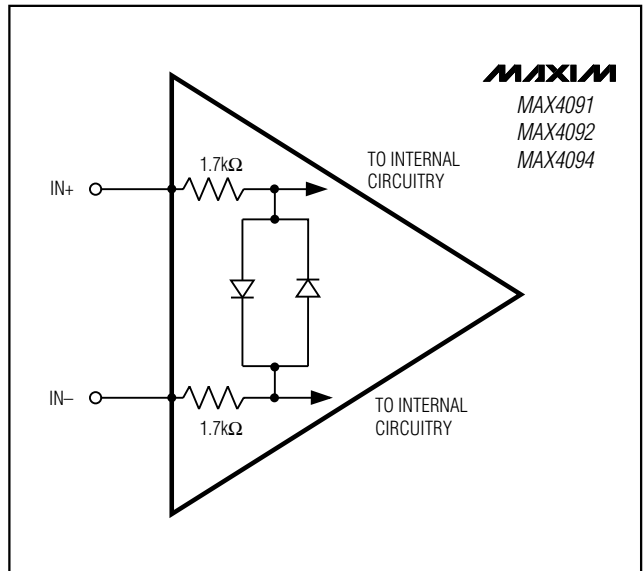


Figure 3. Input Stage Protection Circuitry

# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

## Test Circuits/Timing Diagrams (continued)

MAX4091/MAX4092/MAX4094

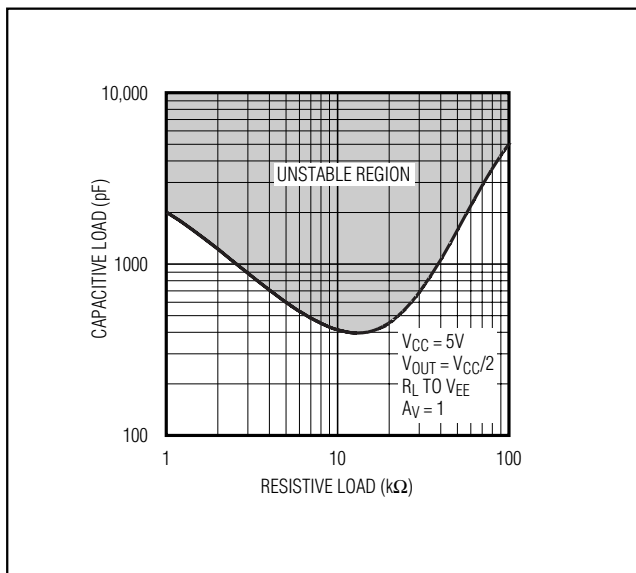


Figure 4. Capacitive-Load Stable Region Sourcing Current

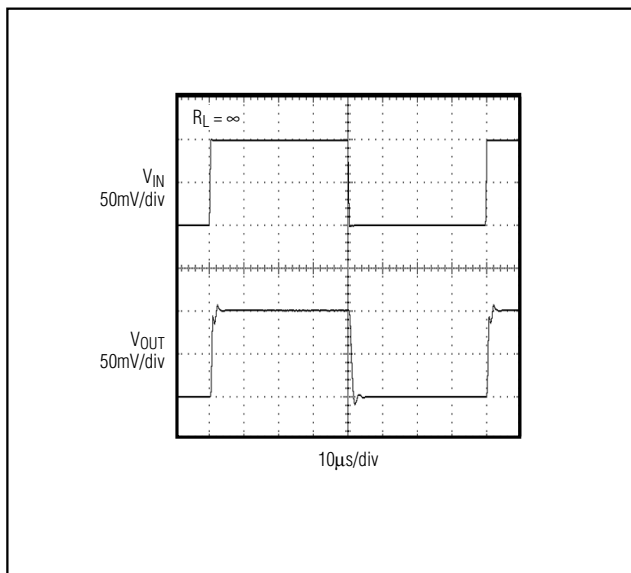


Figure 5. MAX4092 Voltage Follower with 1000pF Load

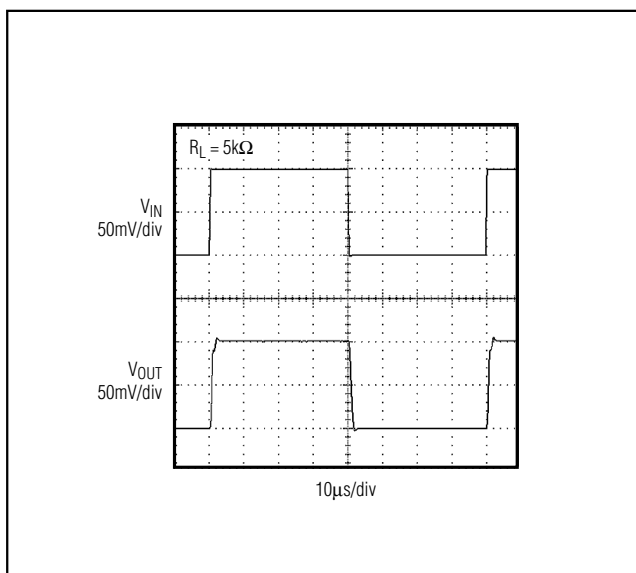


Figure 6a. MAX4092 Voltage Follower with 500pF Load ( $R_L = 5k\Omega$ )

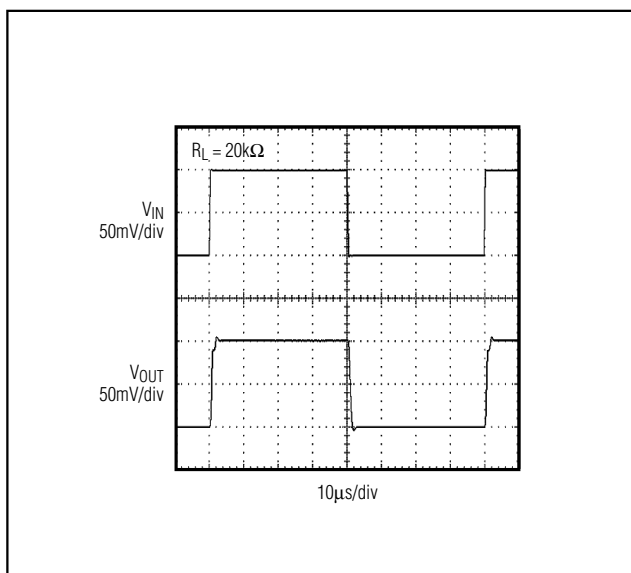


Figure 6b. MAX4092 Voltage Follower with 500pF Load ( $R_L = 20k\Omega$ )

# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

## Test Circuits/Timing Diagrams (continued)

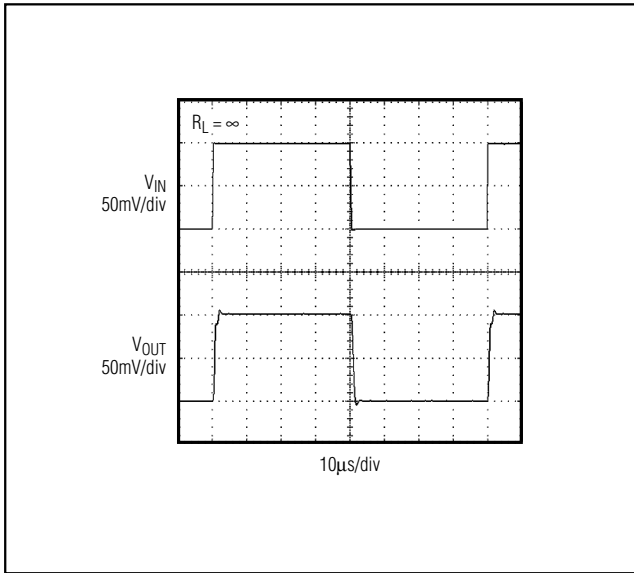


Figure 6c. MAX4092 Voltage Follower with 500pF Load ( $R_L = \infty$ )

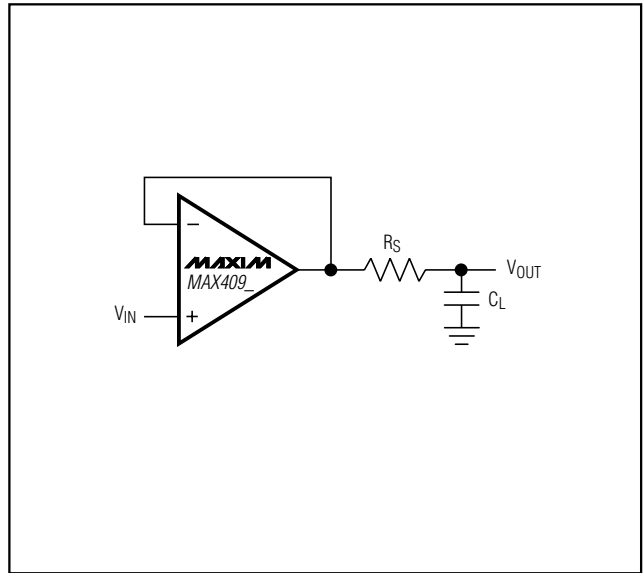


Figure 7. Capacitive-Load Driving Circuit

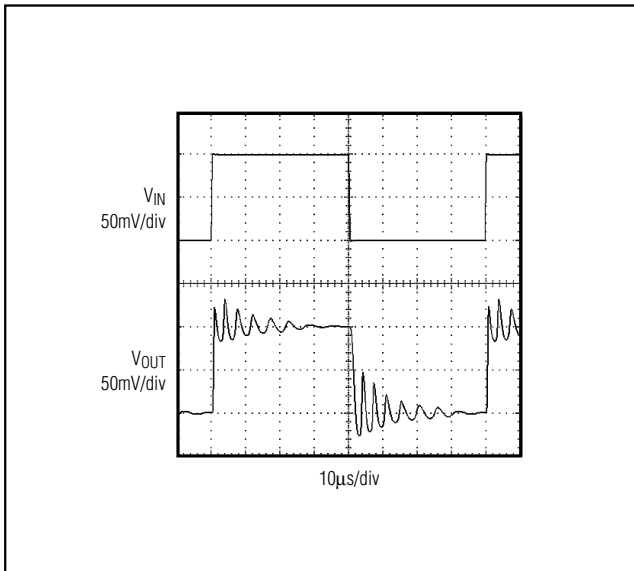


Figure 8a. Driving a 5000pF Capacitive Load

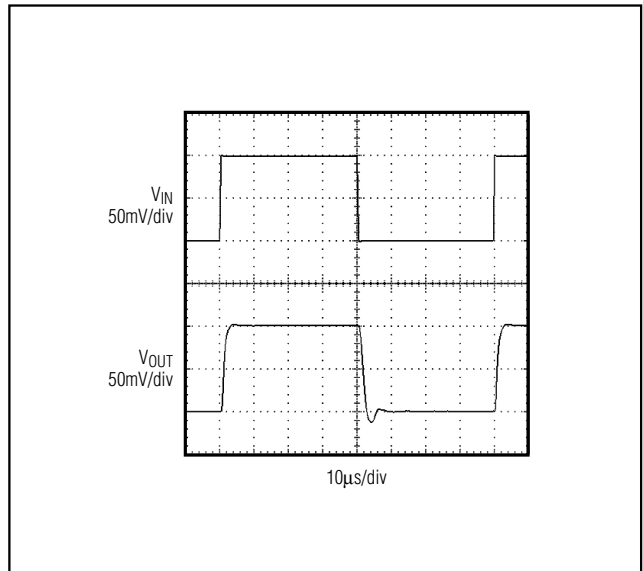


Figure 8b. Driving a 5000pF Capacitive Load with a 47Ω Isolation Resistor

# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

## Test Circuits/Timing Diagrams (continued)

MAX4091/MAX4092/MAX4094

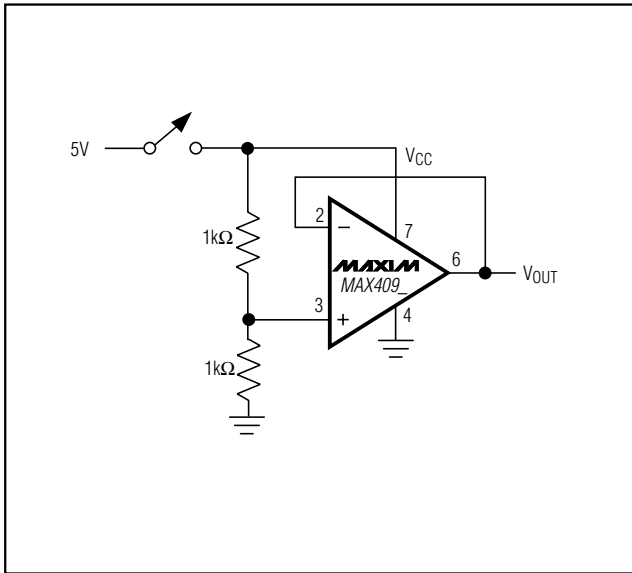


Figure 9. Power-Up Test Configuration

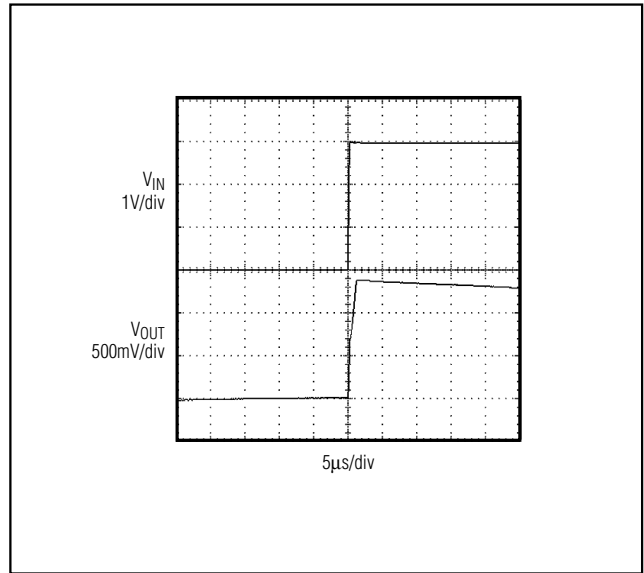


Figure 10a. Power-Up Settling Time ( $V_{CC} = +3V$ )

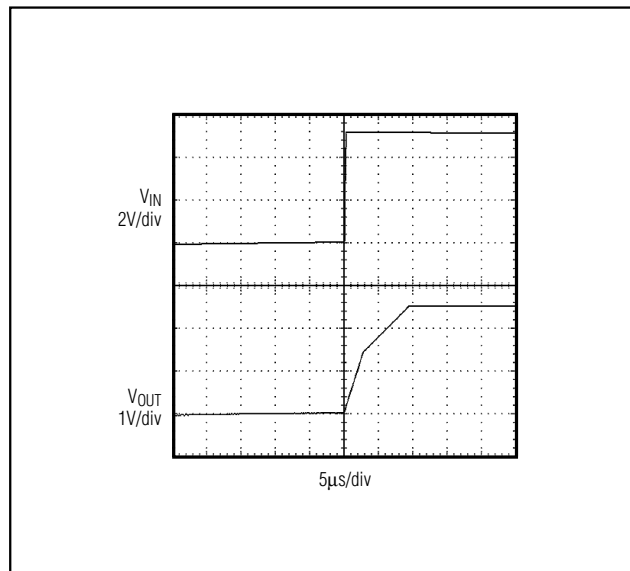


Figure 10b. Power-Up Settling Time ( $V_{CC} = +5V$ )

# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

## Package Information

SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95	REF
e1	1.90	REF
α	0°	10°

NOTES:  
 1. ALL DIMENSIONS ARE IN MILLIMETERS.  
 2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.  
 3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.  
 4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.  
 5. MEETS JEDEC MO178.

MAXIM  
 PROPRIETARY INFORMATION  
 TITLE: PACKAGE OUTLINE, SOT-23, 5L  
 APPROVAL: DOCUMENT CONTROL NO: 21-0057 REV: C 1/1

SOT23EFS

		JEDEC			
		MILLIMETERS		MILLIMETERS	
INCHES	MILLIMETERS	MIN	MAX	MIN	MAX
A	0.037 0.043	0.94	1.10	---	0.043
A1	0.002 0.006	0.05	0.15	0.002	0.006
B	0.010 0.014	0.25	0.36	0.010	0.016
C	0.005 0.007	0.13	0.18	0.005	0.009
D	0.116 0.120	2.95	3.05	0.114	0.122
e	0.0256 BSC	0.65 BSC	0.0256 BSC	0.64 BSC	3.1
E	0.116 0.120	2.95	3.05	0.114	0.122
H	0.188 0.198	4.78	5.03	0.193 BSC	4.9 BSC
L	0.016 0.026	0.41	0.66	0.016	0.027
α	0° 6°	0° 6°	0° 6°	0° 6°	0° 6°
S	0.0207 BSC	0.5250 BSC			

NOTES:  
 1. D&E DO NOT INCLUDE MOLD FLASH.  
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").  
 3. CONTROLLING DIMENSION: MILLIMETERS.  
 4. MEETS JEDEC MO-187.

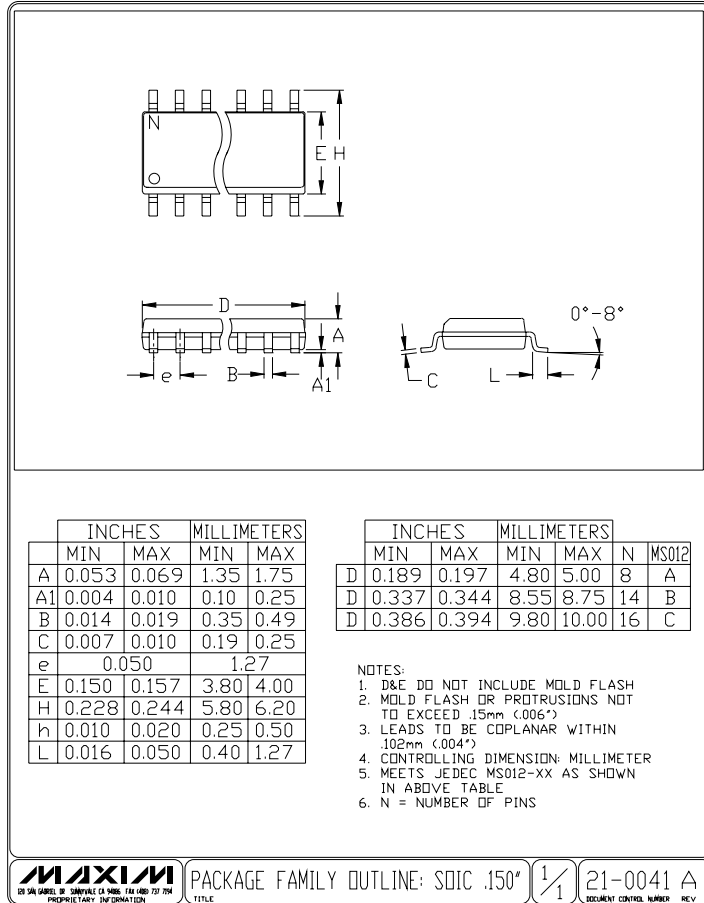
MAXIM  
 PROPRIETARY INFORMATION  
 TITLE: PACKAGE OUTLINE, 8L uMAX  
 APPROVAL: DOCUMENT CONTROL NO: 21-0036 REV: 1 1/1

8LUMAXD.EFS

# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

## Package Information (continued)

MAX4091/MAX4092/MAX4094



# Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

## Package Information (continued)

**COMMON DIMENSIONS**

	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10	—	.043
A <sub>1</sub>	0.05	0.15	.002	.006
A <sub>2</sub>	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b <sub>1</sub>	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c <sub>1</sub>	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC	N	VARIATIONS			
		MILLIMETERS		INCHES	
		MIN.	MAX.	MIN.	MAX.
AB-1	14 D	4.90	5.10	.193	.201
AB	16 D	4.90	5.10	.193	.201
AC	20 D	6.40	6.60	.252	.260
AD	24 D	7.70	7.90	.303	.311
AE	28 D	9.60	9.80	.378	.386

**NOTES:**

- DIMENSIONS D AND E DO NOT INCLUDE FLASH
- MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
- CONTROLLING DIMENSION: MILLIMETER
- MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
- 'N' REFERS TO NUMBER OF LEADS

⚠ THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

**MAXIM**

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY

APPROVAL	DOCUMENT CONTROL NO.	REV	1/1
	21-0066	E	

TSSOP, NO PADS, EPS

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