# THE DATASHEET OF

# MAX3634ETM+T

19-3818; Rev 0; 9/05

EVALUATION KIT AVAILABLE

# 622Mbps/1244Mbps Burst-Mode Clock Phase Aligner for GPON OLT Applications



## General Description

The MAX3634 burst-mode clock phase aligner (CPA) is designed specifically for 622Mbps or 1244Mbps GPON (ITU G.984) optical line terminal (OLT) receiver applications. The MAX3634 provides clock and clock-aligned resynchronized upstream data through differential LVPECL outputs. Using the OLT system clock as a reference, the MAX3634 aligns to the input data and acquires within the first 13 bits of the burst. The CPA operates with received data that is frequency locked to the OLT reference. The acquisition time, bit-error ratio, and jitter tolerance all support GPON PMD specifications. LVPECL high-speed clock and data outputs provide compatibility with FPGAs at 622Mbps and with the MAX3885 deserializer at 1244Mbps.

The MAX3634 is available in a low-profile, 7mm x 7mm, 48-lead TQFN package. The MAX3634 operates from a single +3.3V supply, over the -40°C to +85°C temperature range.

## Applications

622Mbps GPON OLT Receivers

1244Mbps GPON OLT Receivers

## Features

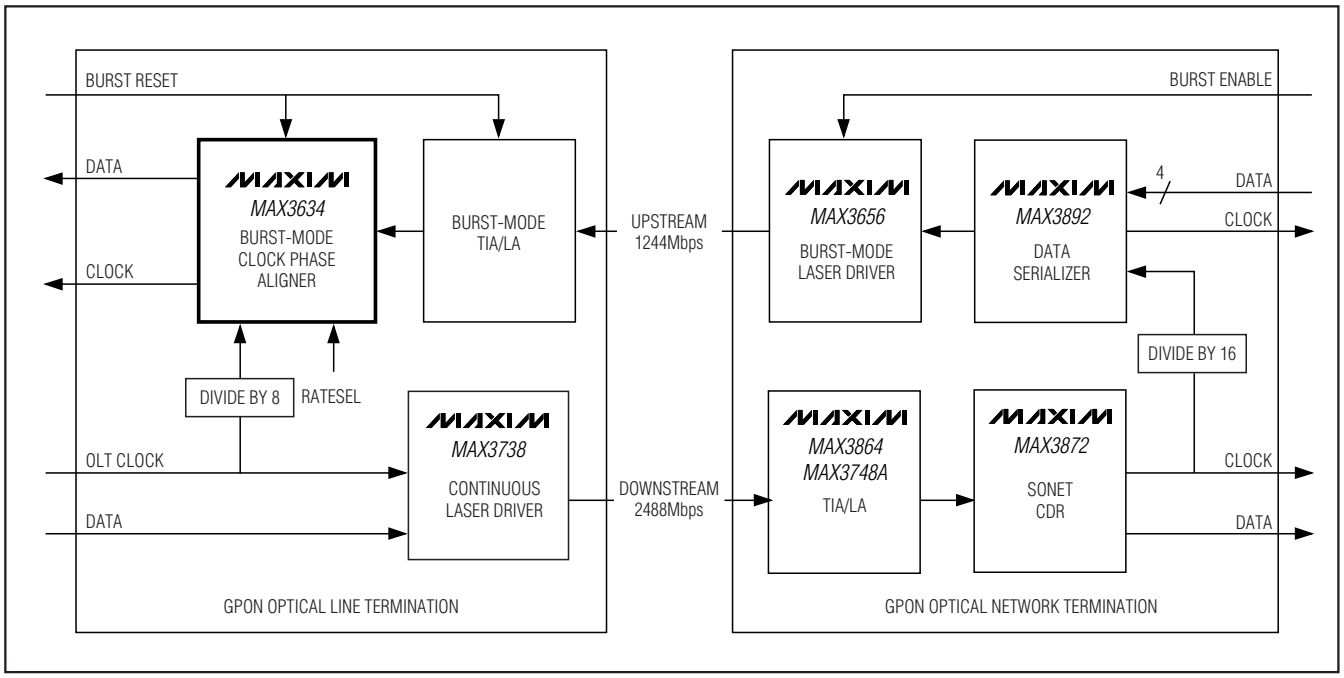
- **DC-Coupled Clock Phase Aligner for Burst-Mode GPON Applications**
- **13-Bit Burst Acquisition Time**
- **0.85UI High-Frequency Jitter Tolerance**
- **Continuous Clock Output**
- **Byte Rate (1/8th Data Rate) Reference Clock Input**
- **Lock Detect Output**
- **LVPECL Serial Data Input and Output**
- **LVPECL Reset Input**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | PKG CODE |
|---|---|---|---|
| MAX3634ETM | -40°C to +85°C | 48 TQFN (7mm x 7mm) | T4877-6 |

***Pin Configuration appears at end of data sheet.***

## Typical Application Circuit



# 622Mbps/1244Mbps Burst-Mode Clock Phase Aligner for GPON OLT Applications

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$, $V_{CC}I$, $V_{CC}O$, $V_{CC}V$ .....-0.5V to +4.0V
SDI±, RST±, REFCLK±,
RATESEL, FILT, TEST.....-0.5V to ($V_{CC}$ + 0.5V)
LVPECL Output Current (SDO±, SCLK±, LOCK±).....50mA

Continuous Power Dissipation ($T_A$ = +85°C)
48-Lead TQFN package
(derate 27.8mW/°C above +85°C).....1800mW
Storage Temperature Range .....-55°C to +150°C
Operating Ambient Temperature Range .....-40°C to +85°C
Lead Temperature (soldering, 10s) .....+400°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +3.0V to +3.6V, $T_A$ = -40°C to +85°C. Typical values are at $V_{CC}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Current | $I_{CC}$ | Not including LVPECL output current | | 315 | 390 | mA |
| Data Rate | | RATESEL = low | | 1244.16 | | Mbps |
| | | RATESEL = high | | 622.08 | | |
| Reference Clock Input Frequency | | RATESEL = low | | 155.52 | | MHz |
| | | RATESEL = high | | 77.76 | | |
| SDI, RST, REFCLK Differential Input | $V_{IN}$ | | 200 | | 1600 | $mV_{P-P}$ |
| SDI±, RST±, REFCLK± Input Current | | | -180 | | +180 | µA |
| RST Input Rise/Fall Times | $t_r$, $t_f$ | Rate = 1244Mbps | | | 200 | ps |
| | | Rate = 622Mbps | | | 200 | |
| SDI±, RST±, REFCLK± Common-Mode Input | | | $V_{CC}$ - 1.49 | | $V_{CC}$ - $V_{IN}$/4 | V |
| SDO±, SCLK±, LOCK± Output Voltage Low | $V_{OL}$ | $T_A$ = 0°C to +85°C (Note 1) | $V_{CC}$ - 1.81 | | $V_{CC}$ - 1.62 | V |
| | | $T_A$ = -40°C to 0°C (Note 1) | $V_{CC}$ - 1.83 | | $V_{CC}$ - 1.555 | |
| SDO±, SCLK±, LOCK± Output Voltage High | $V_{OH}$ | $T_A$ = 0°C to +85°C (Note 1) | $V_{CC}$ - 1.025 | | $V_{CC}$ - 0.88 | V |
| | | $T_A$ = -40°C to 0°C (Note 1) | $V_{CC}$ - 1.085 | | $V_{CC}$ - 0.88 | |
| Jitter Tolerance | | 622Mbps (Notes 2, 5, 6) | 0.73 | 0.83 | | $UI_{P-P}$ |
| | | 1244Mbps (Notes 2, 5, 6) | 0.73 | 0.81 | | |
| Acquisition Time | | (Notes 2, 3) | | | 13 | Bits |
| Bit-Error Ratio | | After acquisition (Notes 2, 4) | | | $10^{-10}$ | |
| SDO±, LOCK± Transition Time | $t_r$, $t_f$ | 20% to 80% (Note 1) | | | 265 | ps |
| SCLK± Transition Time | $t_r$, $t_f$ | 20% to 80% (Note 1) | | | 200 | ps |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +3.0V to +3.6V, $T_A$ = -40°C to +85°C. Typical values are at $V_{CC}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Serial Data Output Clock-to-Q Delay (Figure 1) | $t_{CLK-Q}$ | 622Mbps (Notes 1, 2) | 500 | | | ps |
| | | 1244Mbps (Notes 1, 2) | 250 | | | |
| Serial Data Output Q-to-Clock Delay (Figure 1) | $t_{Q-CLK}$ | 622Mbps (Notes 1, 2) | 500 | | | ps |
| | | 1244Mbps (Notes 1, 2) | 250 | | | |
| RATESEL Input High | $V_{IH}$ | | 2 | | | V |
| RATESEL Input Low | $V_{IL}$ | | | | 0.8 | V |
| RATESEL Input Current | | $V_{IN}$ = 0V or $V_{CC}$ | -100 | | +100 | µA |

**Note 1:** PECL output must have external termination of 50Ω to $V_{CC}$ - 2V (Thevenin equivalent).
**Note 2:** AC parameters are guaranteed by design and characterization.
**Note 3:** From start of PON burst, 101010101010 preamble sequence.
**Note 4:** BER, acquisition time requirements are met with 100m$V_{P-P}$ sinusoidal noise on $V_{CC}$, 0 < $f_{NOISE}$ ≤ 10MHz.
**Note 5:** Measured with 20ps$_{RMS}$ input random jitter (1.244Mbps), 30ps$_{RMS}$ (622Mbps)
**Note 6:** Jitter tolerance refers to the variation in phase between REFCLK and SDI after acquisition.

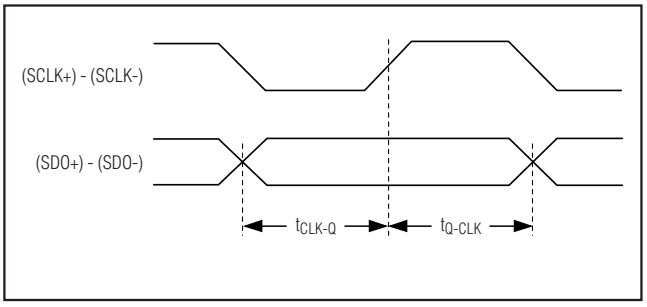
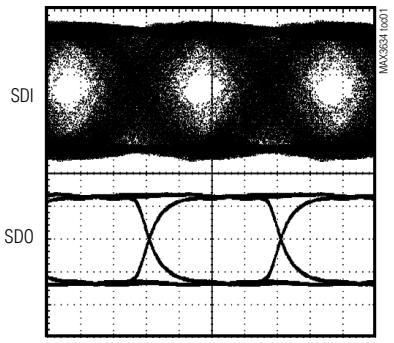



*Figure 1. Definition of Clock-to-Q and Q-to-Clock Delay*

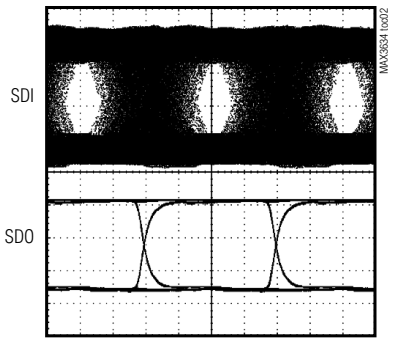
## Typical Operating Characteristics

($V_{CC}$ = +3.3V and $T_A$ = +25°C, unless otherwise noted)

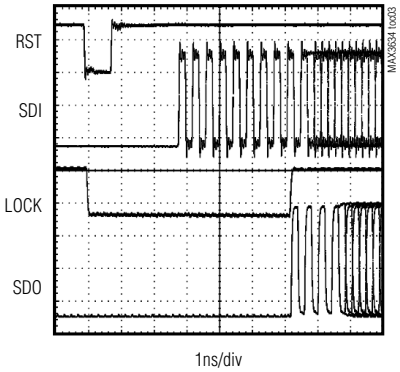
**1.244Gbps INPUT AND OUTPUT EYE DIAGRAMS**




**622Mbps INPUT AND OUTPUT EYE DIAGRAMS**




**BURST CAPTURE AT 1.244Gbps**

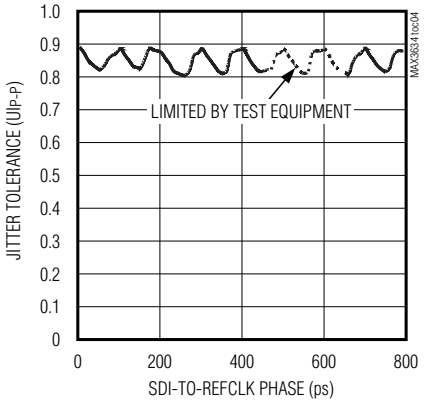


# 622Mbps/1244Mbps Burst-Mode Clock Phase Aligner for GPON OLT Applications

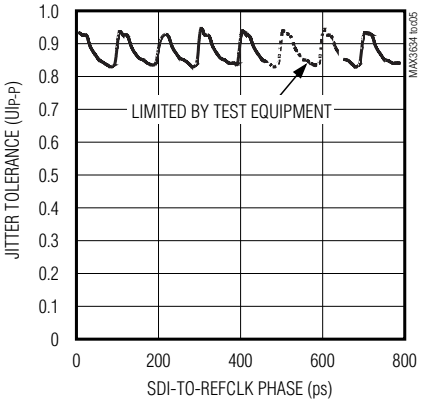
## Typical Operating Characteristics (continued)

($V_{CC}$ = +3.3V and $T_A$ = +25°C, unless otherwise noted)

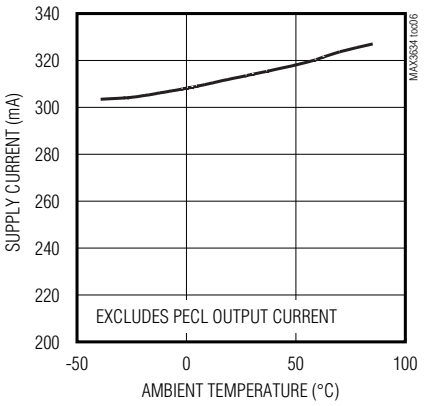
**JITTER TOLERANCE vs. SDI-TO-REFCLK PHASE (1.244Gbps)**




**JITTER TOLERANCE vs. SDI-TO-REFCLK PHASE (622Mbps)**




**SUPPLY CURRENT vs. TEMPERATURE**




## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1, 2, 12, 25, 36, 37, 48 | GND | Supply Ground |
| 3, 6, 7, 10 | $V_{CC}I$ | +3.3V Supply for Input Buffers |
| 4 | SDI+ | Positive Serial Data Input, LVPECL |
| 5 | SDI- | Negative Serial Data Input, LVPECL |
| 8 | RST+ | Positive Reset Input, LVPECL. Reset (= RST+ - RST-) is falling edge triggered. |
| 9 | RST- | Negative Reset Input, LVPECL |
| 11, 38, 39, 44, 47 | $V_{CC}$ | +3.3V Supply for Digital Circuitry |
| 13–20, 22, 23 | TEST | Production Test Pins, Reserved. Leave open for normal operation. |
| 21, 24, 26, 29, 32, 35 | $V_{CC}O$ | +3.3V Supply for Output Buffers |
| 27 | LOCK- | Negative Lock Status Output, LVPECL |
| 28 | LOCK+ | Positive Lock Status Output, LVPECL. Lock (= (LOCK+) - (LOCK-)) high indicates that the MAX3634 has acquired the correct phase. |
| 30 | SDO- | Negative Serial Data Output, LVPECL |
| 31 | SDO+ | Positive Serial Data Output, LVPECL |
| 33 | SCLK- | Negative Serial Clock Output, LVPECL |
| 34 | SCLK+ | Positive Serial Clock Output, LVPECL |
| 40 | RATESEL | Rate Select Input, TTL. High selects 622.08Mbps operation. |
| 41, 43 | $V_{CC}V$ | +3.3V Supply for VCO |
| 42 | FILT | PLL Filter Capacitor. Connect a 0.1µF X7R capacitor from pin 42 to $V_{CC}V$. |
| 45 | REFCLK- | Negative Reference Clock Input, LVPECL (1/8th data rate) |
| 46 | REFCLK+ | Positive Reference Clock Input, LVPECL |
| EP | Exposed Pad | The exposed pad must be connected to the ground plane for proper thermal performance. |

# 622Mbps/1244Mbps Burst-Mode Clock Phase Aligner for GPON OLT Applications

## General Description

### Theory of Operation

The MAX3634 CPA provides serial clock and data outputs for GPON upstream bursts.

The burst-mode CPA operates on the principle that the recovered clock from the ONT CDR is used at each ONT to clock upstream data bursts out of the ONT controller. The burst-mode CPA has logic that determines the correct phase relationship between the upstream data and the OLT reference clock at the beginning of each ONT's burst, and resamples the upstream data at each bit using that clock.

The burst-mode CPA contains a phase-locked loop (PLL) that synchronizes its oscillator to the reference clock input. This oscillator drives a phase splitter, which generates eight evenly spaced phases of the serial clock, which are used to sample the input data at 1/8th bit intervals in eight flip-flops. Combinatorial and sequential logic measures the preamble, and based on the phase of the preamble, determines which one of the eight clock phases is at the center of the input data bits. The data from the flip-flop associated with this phase is then steered through a multiplexer to the CPA output, which requires four or five additional clock periods until valid data is output. The CPA serial output clock is continuous, without any phase jumps or discontinuities from burst to burst.

The burst-mode CPA requires a preamble sequence of 1010101010101 (13 bits) for correct phase alignment. Typically, output begins after the 12th bit, although for certain data/phase relationships, 13 bits are required. An LVPECL-compatible lock status output is provided, which indicates when the correct phase has been acquired and valid serial output data is available. This output remains low until reset by the burst reset input (RST). The output data is disabled (held low) during the period between reset and lock.

### Reference Clock Input

The MAX3634 includes a PLL, which multiplies the reference clock by eight for use in the retiming circuitry. For correct operation, the REFCLK input must be connected to the OLT byte-rate reference clock, which must be equal to 1/8th the serial data rate, and must have a 40% to 60% duty cycle. This must be the same clock source used to time the downstream data, and the upstream data must be frequency locked to this source.

The RATESEL input is used to configure 622Mbps or 1244Mbps operation; when RATESEL is high, the MAX3634 operates at 622Mbps.

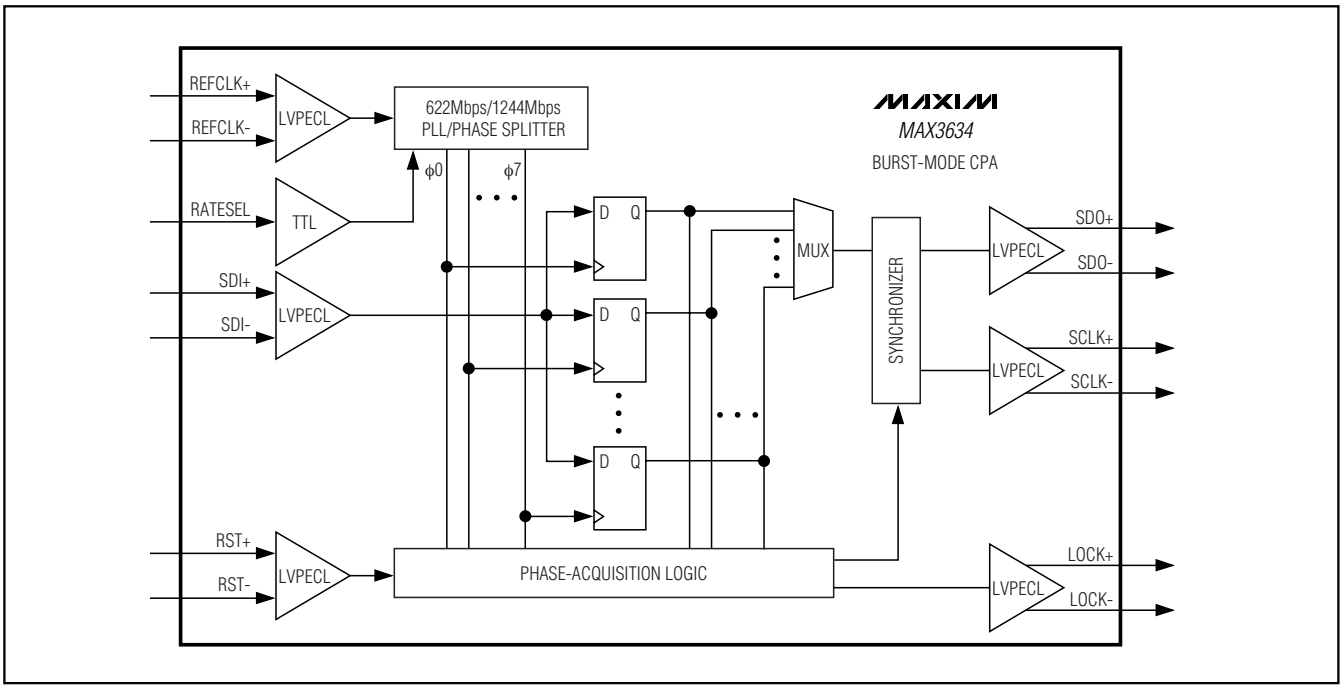



*Figure 2. Functional Block Diagram*

# 622Mbps/1244Mbps Burst-Mode Clock Phase Aligner for GPON OLT Applications

### Input Stage

The LVPECL serial data input, SDI±, and burst-mode reset input, RST±, provide 200mV$_{P-P}$ sensitivity. The RST± input rise and fall times (20% to 80%) must not exceed 200ps. LVPECL inputs must be DC-coupled with external termination for correct operation with burst data (see *Maxim Application Note HFAN 1.0* for termination configuration).

### Lock Detect

After the first 12 or 13 bits of the preamble, plus 4 or 5 bits of synchronizer delay, LOCK asserts to indicate the beginning of valid data output.

## Applications Information

### GPON Burst-Mode Timing

Internally, the MAX3634 requires five internal clock cycles (8x REFCLK) to initialize itself after receiving the rest (BRST) signal. It then uses the next 8 bits of preamble (10101010) to measure the phase relationship between the reference clock and upstream data (after the internal logic has been reset), and 3 to 5 bits later begins outputting data. The time interval from BRST to the end of the preamble must be no less than 18 bits long. If the 8 bits of preamble that it uses to measure phase have been excessive pulse-width distortion, the phase measurement is in error.

The active edge of the reset input (BRST) must arrive at the MAX3634 after the TIA has finished its level recovery, but no sooner than 18 bits prior to the end of the (repeating 10 pattern) preamble, in order to provide adequate time for the MAX3634 to initialize, measure the phase, and load the output pipelines. This timing is shown in Figure 3.

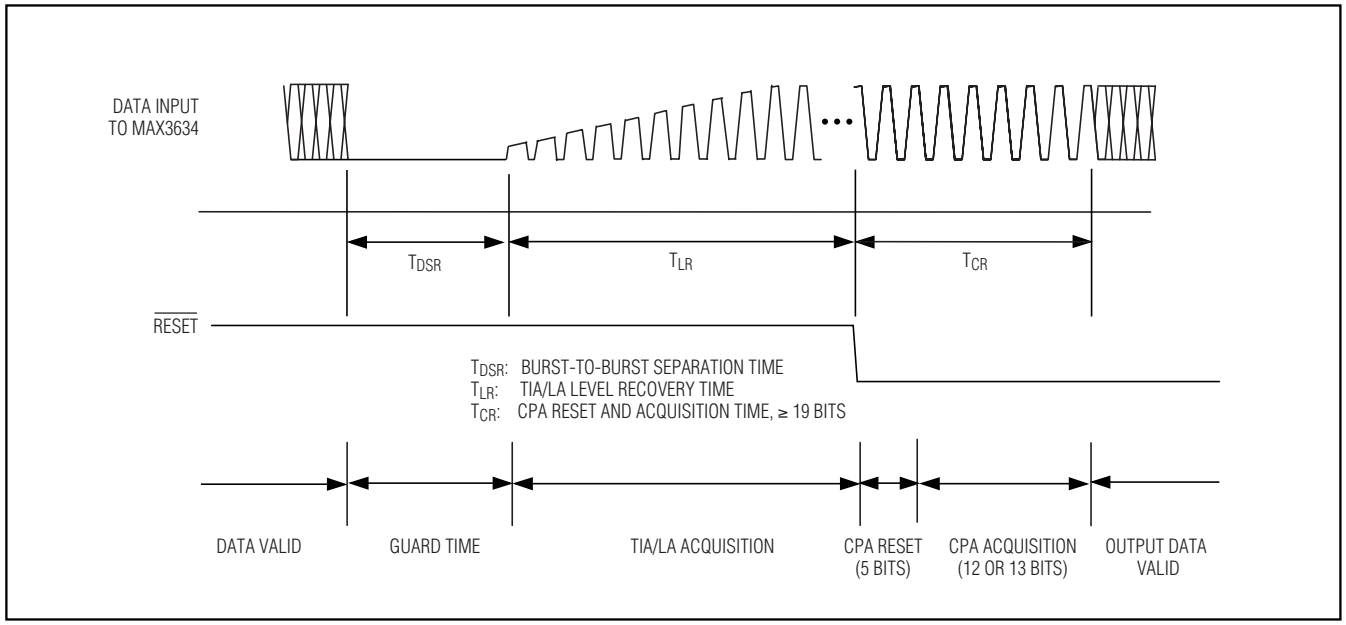
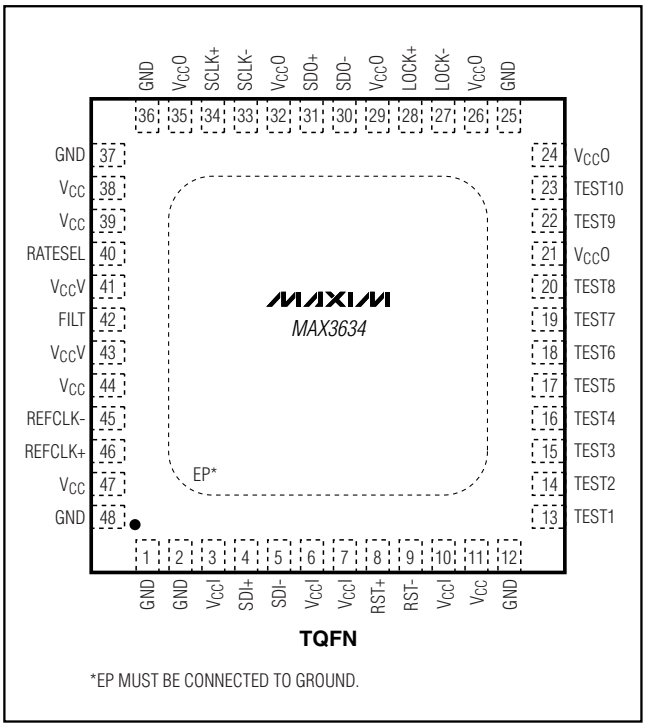



*Figure 3. Clock Phase Aligner Operation Timing Diagram*

# 622Mbps/1244Mbps Burst-Mode Clock Phase Aligner for GPON OLT Applications

## Pin Configuration




**TQFN**

*EP MUST BE CONNECTED TO GROUND.

## Chip Information

TRANSISTOR COUNT: 10,805

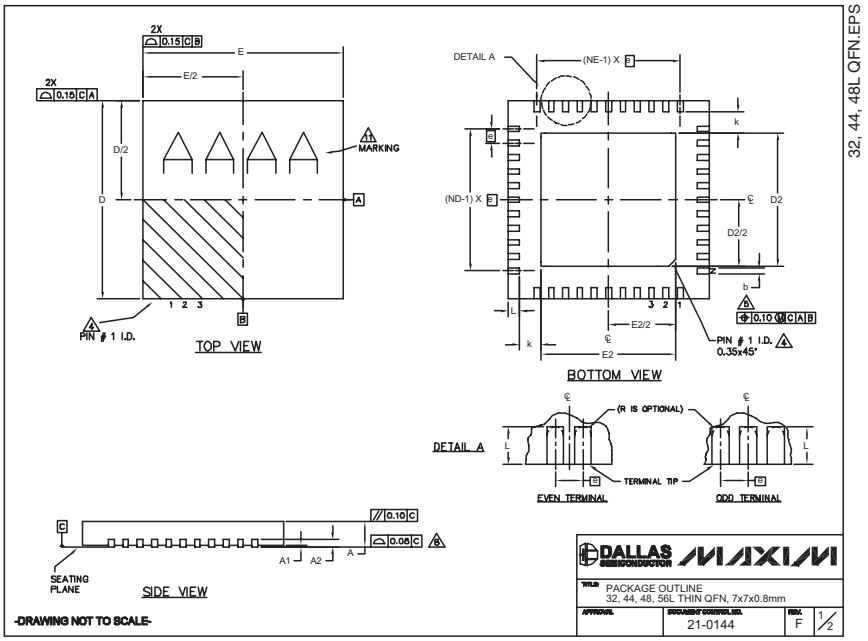
PROCESS: Silicon Germanium BiCMOS

# 622Mbps/1244Mbps Burst-Mode Clock Phase Aligner for GPON OLT Applications

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32, 44, 48L QFN.EPS




**COMMON DIMENSIONS**

| PKG | 32L 7x7 | | | 44L 7x7 | | | 48L 7x7 | | | CUSTOM PKG. (T4877-1) 48L 7x7 | | | 56L 7x7 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SYMBOL | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | – | 0.05 |
| A2 | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | |
| b | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 | 0.15 | 0.20 | 0.25 |
| D | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 |
| E | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 |
| e | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | | 0.40 BSC. | | |
| k | 0.25 | – | – | 0.25 | – | – | 0.25 | – | – | 0.25 | – | – | 0.25 | – | – |
| L | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 |
| N | 32 | | | 44 | | | 48 | | | 44 | | | 56 | | |
| ND | 8 | | | 11 | | | 12 | | | 10 | | | 14 | | |
| NE | 8 | | | 11 | | | 12 | | | 12 | | | 14 | | |

**EXPOSED PAD VARIATIONS**

| PKG. CODES | DEPOPULATED LEADS | D2 | | | E2 | | | JEDEC MO220 REV. C |
|---|---|---|---|---|---|---|---|---|
| | | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | |
| T3277-2 | – | 4.55 | 4.70 | 4.85 | 4.55 | 4.70 | 4.85 | – |
| T3277-3 | – | 4.55 | 4.70 | 4.85 | 4.55 | 4.70 | 4.85 | – |
| T4477-2 | – | 4.55 | 4.70 | 4.85 | 4.55 | 4.70 | 4.85 | WKKD-1 |
| T4477-3 | – | 4.55 | 4.70 | 4.85 | 4.55 | 4.70 | 4.85 | WKKD-1 |
| T4877-1** | 13,24,37,48 | 4.20 | 4.30 | 4.40 | 4.20 | 4.30 | 4.40 | – |
| T4877-3 | – | 4.95 | 5.10 | 5.25 | 4.95 | 5.10 | 5.25 | – |
| T4877-4 | – | 5.40 | 5.50 | 5.60 | 5.40 | 5.50 | 5.60 | – |
| T4877-5 | – | 2.40 | 2.50 | 2.60 | 2.40 | 2.50 | 2.60 | – |
| T4877-6 | – | 5.40 | 5.50 | 5.60 | 5.40 | 5.50 | 5.60 | – |
| T4877-7 | – | 4.95 | 5.10 | 5.25 | 4.95 | 5.10 | 5.25 | – |
| T4877M-1 | – | 5.40 | 5.50 | 5.60 | 5.40 | 5.50 | 5.60 | – |
| T4877M-6 | – | 5.40 | 5.50 | 5.60 | 5.40 | 5.50 | 5.60 | – |
| T4877MN-8 | – | 5.40 | 5.50 | 5.60 | 5.40 | 5.50 | 5.60 | – |
| T5677-1 | – | 5.40 | 5.50 | 5.60 | 5.40 | 5.50 | 5.60 | – |
| T5677-2 | – | 5.40 | 5.50 | 5.60 | 5.40 | 5.50 | 5.60 | – |

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T4877-1/-3/-4/-5/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

PACKAGE OUTLINE
32, 44, 48, 56L THIN QFN, 7x7x0.8mm
21-0144
F
2/2

*Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.*

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- Shortage Management
- Alternative Solution
- Excess Inventory Management