



# THE DATASHEET OF MAX3232ECDR



# MAX3232E 3-V to 5.5-V Multichannel RS-232 Line Driver and Receiver

## With $\pm 15$ -kV IEC ESD Protection

### 1 Features

- ESD protection for RS-232 bus pins
  - $\pm 15$  kV (HBM)
  - $\pm 8$  kV (IEC61000-4-2, Contact discharge)
  - $\pm 15$  kV (IEC61000-4-2, Air-gap discharge)
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU V.28 standards
- Operates with 3-V to 5.5-V  $V_{CC}$  supply
- Operates up to 250 kbit/s
- Two drivers and two receivers
- Low supply current: 300  $\mu$ A (typical)
- External capacitors:  $4 \times 0.1 \mu$ F
- Accepts 5-V logic input with 3.3-V supply
- Pin compatible to alternative high-speed devices (1 Mbit/s)
  - SN65C3232E ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
  - SN75C3232E ( $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ )

### 2 Applications

- [Industrial PCs](#)
- [Wired networking](#)
- [Data center and enterprise computing](#)
- [Battery-powered systems](#)
- [Notebooks](#)
- [Palm-top PCs](#)
- [Hand-held equipment](#)

### 3 Description

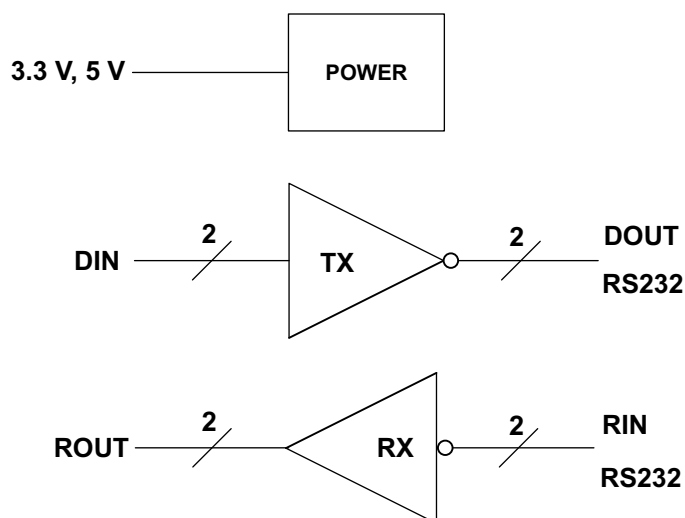
The MAX3232E device consists of two line drivers, two-line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV IEC ESD protection pin to pin (serial-port connection pins, including GND).

The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/ $\mu$ s driver output slew rate.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MAX3232E	SOIC (D) (16)	9.90 mm $\times$ 3.91 mm
	SSOP (DB) (16)	6.20 mm $\times$ 5.30 mm
	SOIC (DW) (16)	10.30 mm $\times$ 7.50 mm
	TSSOP (PW) (16)	5.00 mm $\times$ 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Diagram



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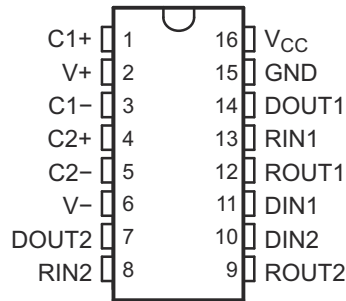
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (May 2017) to Revision E (June 2021)</b>	<b>Page</b>
• Added <i>Applications</i> : Industrial PCs, Wired networking, and Data center and enterprise computing.....	1
• Added the <i>ESD Ratings - IEC Specifications</i> table. Added a table note about 1-uF capacitor requirement between V <sub>CC</sub> and GND for D, DB and PW packages.....	4
• Changed the thermal parameter values for D, DB and PW packages in the <i>Thermal Information</i> table.....	5
<b>Changes from Revision C (June 2015) to Revision D (May 2017)</b>	<b>Page</b>
• Changed 3 V ± 5.5 V to 3 V to 5.5 V in the V <sub>CC</sub> column of <a href="#">Table 9-1</a> .....	11
<b>Changes from Revision B (December 2013) to Revision C (May 2015)</b>	<b>Page</b>
• Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
<b>Changes from Revision A (April 2007) to Revision B (December 2013)</b>	<b>Page</b>
• Updated document to new TI data sheet format.....	1
• Deleted <i>Ordering Information</i> table.....	1
• Added <i>Thermal Information</i> table.....	5

## 5 Pin Configuration and Functions



**Figure 5-1. D, DW, DB and PW Package, 16-Pin SOIC, SSOP and TSSOP, Top View**

**Table 5-1. Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
V+	2	O	Positive charge pump output for storage capacitor only
C1-	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2-	5	—	Negative lead of C2 capacitor
V-	6	O	Negative charge pump output for storage capacitor only
DOUT2	7	O	RS232 line data output (to remote RS232 system)
RIN2	8	I	RS232 line data input (from remote RS232 system)
ROUT2	9	O	Logic data output (to UART)
DIN2	10	I	Logic data input (from UART)
DIN1	11	I	Logic data input (from UART)
ROUT1	12	O	Logic data output (to UART)
RIN1	13	I	RS232 line data input (from remote RS232 system)
DOUT1	14	O	RS232 line data output (to remote RS232 system)
GND	15	—	Ground
V <sub>CC</sub>	16	—	Supply Voltage, Connect to external 3-V to 5.5-V power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>	-0.3	6	V	
V+	Positive output supply voltage <sup>(2)</sup>	-0.3	7	V	
V-	Negative output supply voltage <sup>(2)</sup>	0.3	-7	V	
V+ – V-	Supply voltage difference <sup>(2)</sup>		13	V	
V <sub>I</sub>	Input voltage	Drivers	-0.3	6	V
		Receivers	-25	25	V
V <sub>O</sub>	Output voltage	Drivers	-13.2	13.2	V
		Receivers	-0.3	V <sub>CC</sub> + 0.3	V
T <sub>J</sub>	Operating virtual junction temperature		150	°C	
T <sub>stg</sub>	Storage temperature	-65	150	°C	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
- (2) All voltages are with respect to network GND.

### 6.2 ESD Ratings

		VALUE	UNIT		
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	All pins except RIN and DOUT	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	RIN and DOUT Pins	±15,000	
			All pins	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 ESD Ratings - IEC Specifications

		VALUE	UNIT		
V <sub>(ESD)</sub>	Electrostatic discharge	IEC61000-4-2, Contact Discharge <sup>(1)</sup>	RS232 port pins (RIN, DOUT)	±8000	V
		IEC61000-4-2, Air-Gap Discharge <sup>(1)</sup>	RS232 port pins (RIN, DOUT)	±15,000	

- (1) For D, DB and PW packages only: Minimum of 1-μF capacitor is required between V<sub>CC</sub> and GND to meet the specified IEC 16000-4-2 rating.

### 6.4 Recommended Operating Conditions<sup>(1)</sup>

See [Typical Operating Circuit and Capacitor Values](#).

		MIN	NOM	MAX	UNIT	
Supply voltage		V <sub>CC</sub> = 3.3 V	3	3.3	3.6	V
		V <sub>CC</sub> = 5 V	4.5	5	5.5	
V <sub>IH</sub>	Driver high-level input voltage	DIN	V <sub>CC</sub> = 3.3 V	2	5.5	V
			V <sub>CC</sub> = 5 V	2.4	5.5	
V <sub>IL</sub>	Driver low-level input voltage	DIN	0	0.8	V	
V <sub>I</sub>	Receiver input voltage	RIN	-25	25	V	

## 6.4 Recommended Operating Conditions<sup>(1)</sup> (continued)

See [Typical Operating Circuit and Capacitor Values](#).

		MIN	NOM	MAX	UNIT
T <sub>A</sub>	Operating free-air temperature	MAX3232EC	0	70	°C
		MAX3232EI	-40	85	

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>	MAX3232E				UNIT	
	PW (TSSOP)	D (SOIC)	DW (SOIC)	DB (SSOP)		
	16 PINS	16 PINS	16 PINS	16 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	108.2	85.9	72.3	103.1	°C/W
R <sub>θJctop</sub>	Junction-to-case (top) thermal resistance	39.0	43.1	33.5	49.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	54.4	44.5	37.1	54.8	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	3.3	10.1	7.5	12	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	53.8	44.1	37.1	54.1	°C/W
R <sub>θJcbot</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Electrical Characteristics — Device<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Typical Operating Circuit and Capacitor Values](#)).

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
I <sub>CC</sub>	Supply current	No load, V <sub>CC</sub> = 3.3 V or 5 V		0.3	1	mA

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 6.7 Electrical Characteristics — Driver<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted) (see [Typical Operating Circuit and Capacitor Values](#)).

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT		
V <sub>OH</sub>	High-level output voltage	DOUT at R <sub>L</sub> = 3 kΩ to GND, DIN = GND		5	5.4	V	
V <sub>OL</sub>	Low-level output voltage	DOUT at R <sub>L</sub> = 3 kΩ to GND, DIN = V <sub>CC</sub>		-5	-5.4	V	
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = V <sub>CC</sub>		±0.01	±1	μA	
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> at GND		±0.01	±1	μA	
I <sub>OS</sub> <sup>(3)</sup>	Short-circuit output current	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0 V		±35	±60	mA
		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0 V				
r <sub>O</sub>	Output resistance	V <sub>CC</sub> , V+, and V- = 0 V, V <sub>O</sub> = ±2 V		300	10M	Ω	

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

(3) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 6.8 Electrical Characteristics — Receiver<sup>(2)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Typical Operating Circuit and Capacitor Values](#)).

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1 mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.1	V	
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1.6 mA		0.4	V	
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 3.3 V		1.5	2.4	V
		V <sub>CC</sub> = 5 V		1.8	2.4	
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 3.3 V	0.6	1.2	V	
		V <sub>CC</sub> = 5 V	0.8	1.5		
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )		0.3		V	
r <sub>i</sub>	Input resistance	V <sub>I</sub> = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(2) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.9 Switching Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Typical Operating Circuit and Capacitor Values](#)).

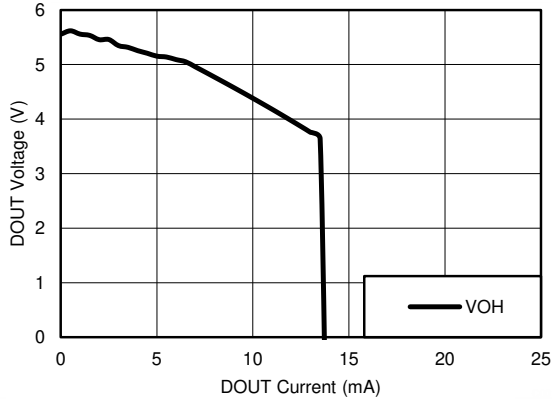
PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
Maximum data rate	R <sub>L</sub> = 3 kΩ, One DOUT switching, C <sub>L</sub> = 1000 pF, see <a href="#">Driver Slew Rate</a>	150	250		kbit/s
t <sub>sk(p)</sub>	R <sub>L</sub> = 3 kΩ to 7 kΩ, see <a href="#">Driver Pulse Skew</a>		300		ns
SR(tr)	R <sub>L</sub> = 3 kΩ to 7 kΩ, V <sub>CC</sub> = 3.3 V	C <sub>L</sub> = 150 pF to 1000 pF	6	30	V/μs
		C <sub>L</sub> = 150 pF to 2500 pF	4	30	
t <sub>PLH</sub>	C <sub>L</sub> = 150 pF, see <a href="#">Receiver Propagation Delay Times</a>		300		ns
t <sub>PHL</sub>			300		ns
t <sub>sk(p)</sub>			300		ns

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

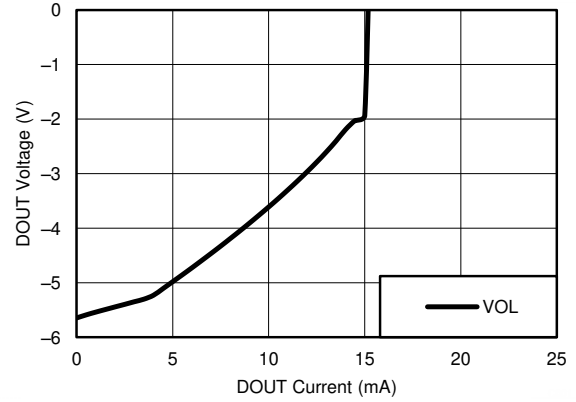
(3) Pulse skew is defined as |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

## 6.10 Typical Characteristics



$V_{CC} = 3.3\text{ V}$

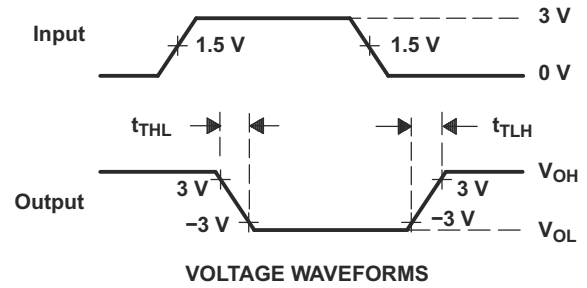
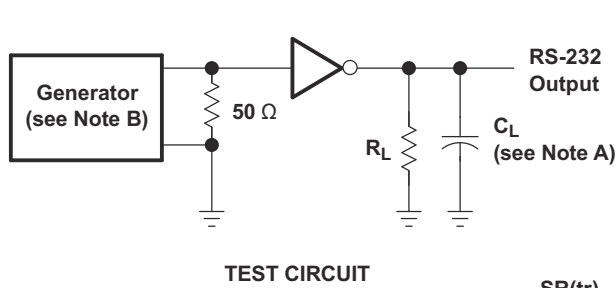
**Figure 6-1. DOUT  $V_{OH}$  vs Load Current, Both Drivers Loaded**



$V_{CC} = 3.3\text{ V}$

**Figure 6-2. DOUT  $V_{OL}$  vs Load Current, Both Drivers Loaded**

## 7 Parameter Measurement Information

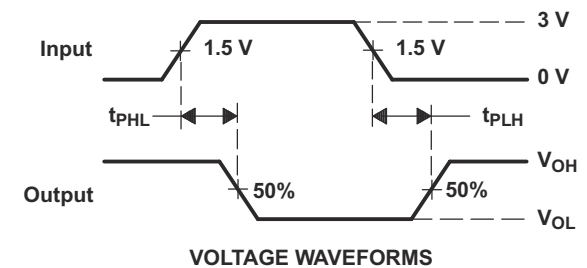
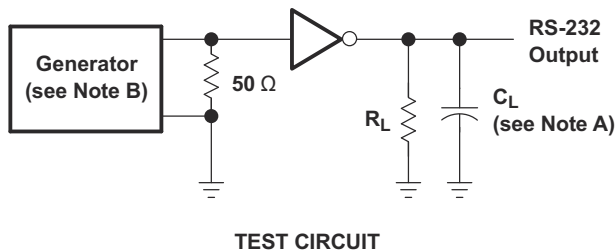


$$SR(tr) = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$

A.  $C_L$  includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$

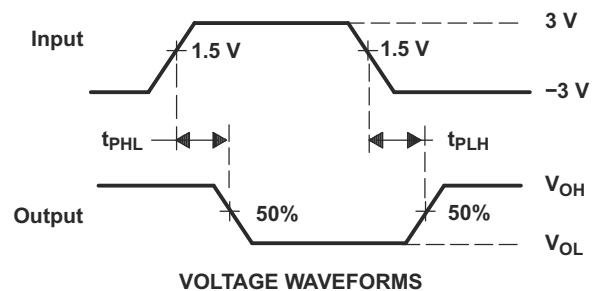
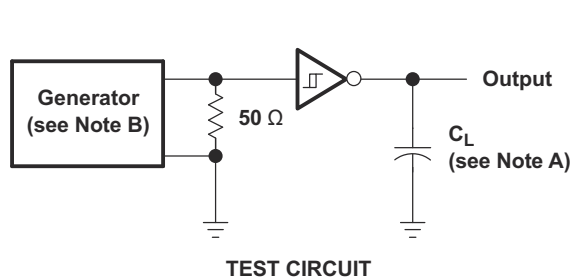
Figure 7-1. Driver Slew Rate



A.  $C_L$  includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$

Figure 7-2. Driver Pulse Skew



A.  $C_L$  includes probe and jig capacitance

B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$

Figure 7-3. Receiver Propagation Delay Times

## 8 Detailed Description

### 8.1 Overview

The MAX3232E device consists of two line drivers, two-line receivers, and a dual charge-pump circuit with IEC61000-4-2 ESD protection terminal to terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/ $\mu$ s driver output slew rate. Outputs are protected against shorts to ground.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V– pins using a charge pump that requires four external capacitors.

#### 8.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

#### 8.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

## 8.4 Device Functional Modes

Table 8-1 and Table 8-2 list the functional modes of the drivers and receivers of MAX3232E.

**Table 8-1. Each Driver<sup>(1)</sup>**

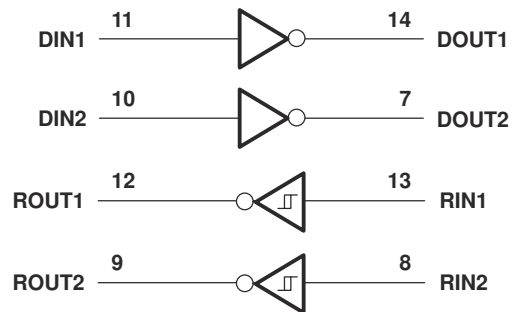
INPUT DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

**Table 8-2. Each Receiver<sup>(1)</sup>**

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,  
Open = input disconnected or connected driver off



**Figure 8-1. Logic Diagram**

### 8.4.1 $V_{CC}$ Powered by 3 V to 5.5 V

The device is in normal operation.

### 8.4.2 $V_{CC}$ Unpowered, $V_{CC} = 0$ V

When MAX3232E is unpowered, it can be safely connected to an active remote RS232 device.

## 9 Application and Implementation

### Note

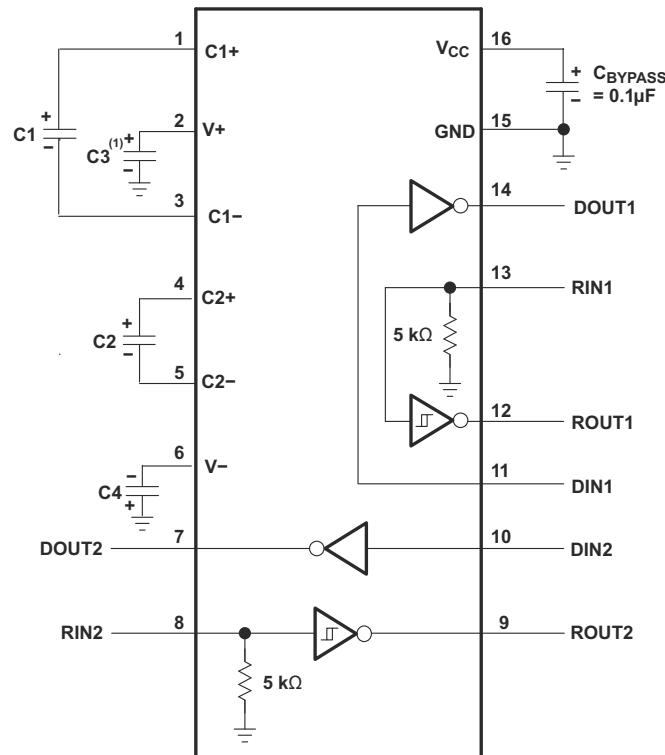
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

For proper operation, add capacitors as shown in [Table 9-1](#).

### 9.2 Typical Application

ROUT and DIN connect to UART or general-purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable.



- A. C3 can be connected to  $V_{CC}$  or GND
- A. Resistor values shown are nominal.
- B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

**Figure 9-1. Typical Operating Circuit and Capacitor Values**

**Table 9-1. VCC vs Capacitor Values**

VCC	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

### 9.2.1 Design Requirements

The recommended  $V_{CC}$  is 3.3 V or 5 V. 3 V to 5.5 V is also possible

The maximum recommended bit rate is 250 kbit/s.

### 9.2.2 Detailed Design Procedure

All DIN inputs must be connected to valid low or high logic levels.

Select capacitor values based on  $V_{CC}$  level for best performance.

### 9.2.3 Application Curve

Figure 9-2 curves are for 3.3-V  $V_{CC}$  and 250-kbit/s alternative bit data stream.

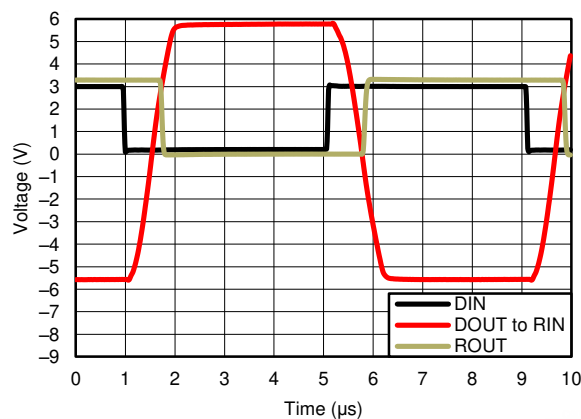


Figure 9-2. 250 kbit/s Driver to Receiver Loopback Timing Waveform,  $V_{CC} = 3.3$  V

## 10 Power Supply Recommendations

The supply voltage,  $V_{CC}$ , should be between 3 V and 5.5 V. Select the values of the charge-pump capacitors using Table 9-1.

## 11 Layout

### 11.1 Layout Guidelines

Keep the external capacitor traces short, specifically on the C1 and C2 nodes that have the fastest rise and fall times.

### 11.2 Layout Example

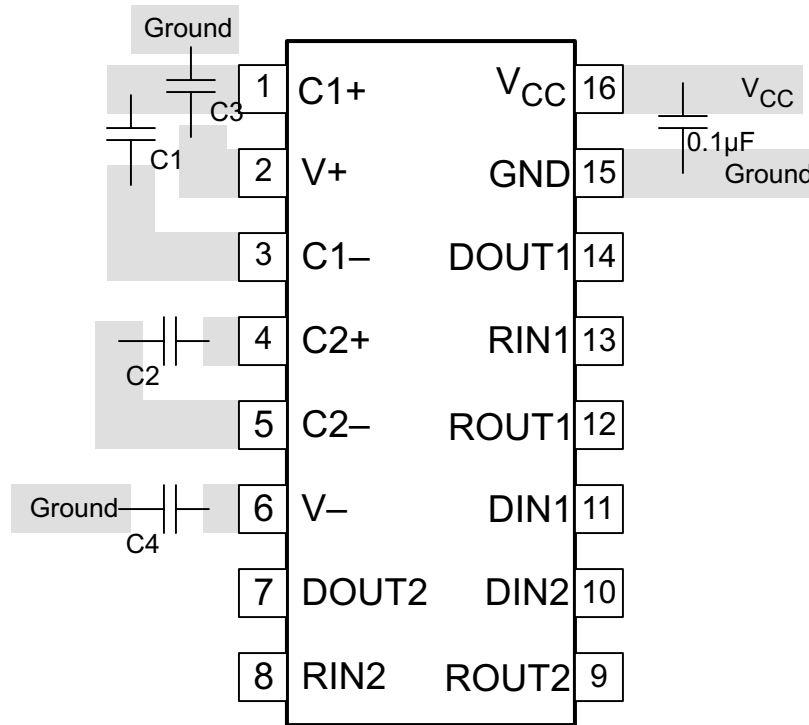


Figure 11-1. Layout Diagram

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

### Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3232ECDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC	<a href="#">Samples</a>
MAX3232ECDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC	<a href="#">Samples</a>
MAX3232ECDRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC	<a href="#">Samples</a>
MAX3232ECDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3232EC	<a href="#">Samples</a>
MAX3232ECPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP232EC	<a href="#">Samples</a>
MAX3232EIDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	<a href="#">Samples</a>
MAX3232EIDBRE4	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	<a href="#">Samples</a>
MAX3232EIDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI	<a href="#">Samples</a>
MAX3232EIDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3232EI	<a href="#">Samples</a>
MAX3232EIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	<a href="#">Samples</a>
MAX3232EIPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP232EI	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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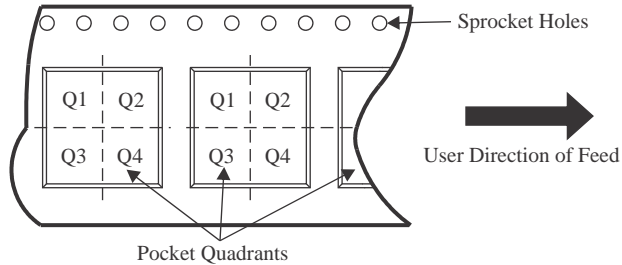
**OTHER QUALIFIED VERSIONS OF MAX3232E :**

- Automotive : [MAX3232E-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3232ECDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX3232ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX3232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3232EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX3232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX3232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3232ECDBR	SSOP	DB	16	2000	356.0	356.0	35.0
MAX3232ECDR	SOIC	D	16	2500	356.0	356.0	35.0
MAX3232ECDWR	SOIC	DW	16	2000	350.0	350.0	43.0
MAX3232ECPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
MAX3232ECPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
MAX3232EIDBR	SSOP	DB	16	2000	356.0	356.0	35.0
MAX3232EIDR	SOIC	D	16	2500	356.0	356.0	35.0
MAX3232EIDWR	SOIC	DW	16	2000	350.0	350.0	43.0
MAX3232EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0016A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

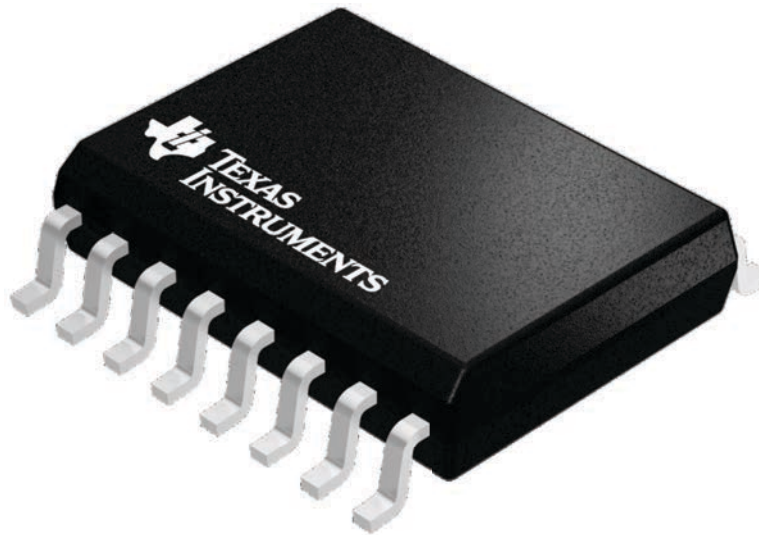
**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

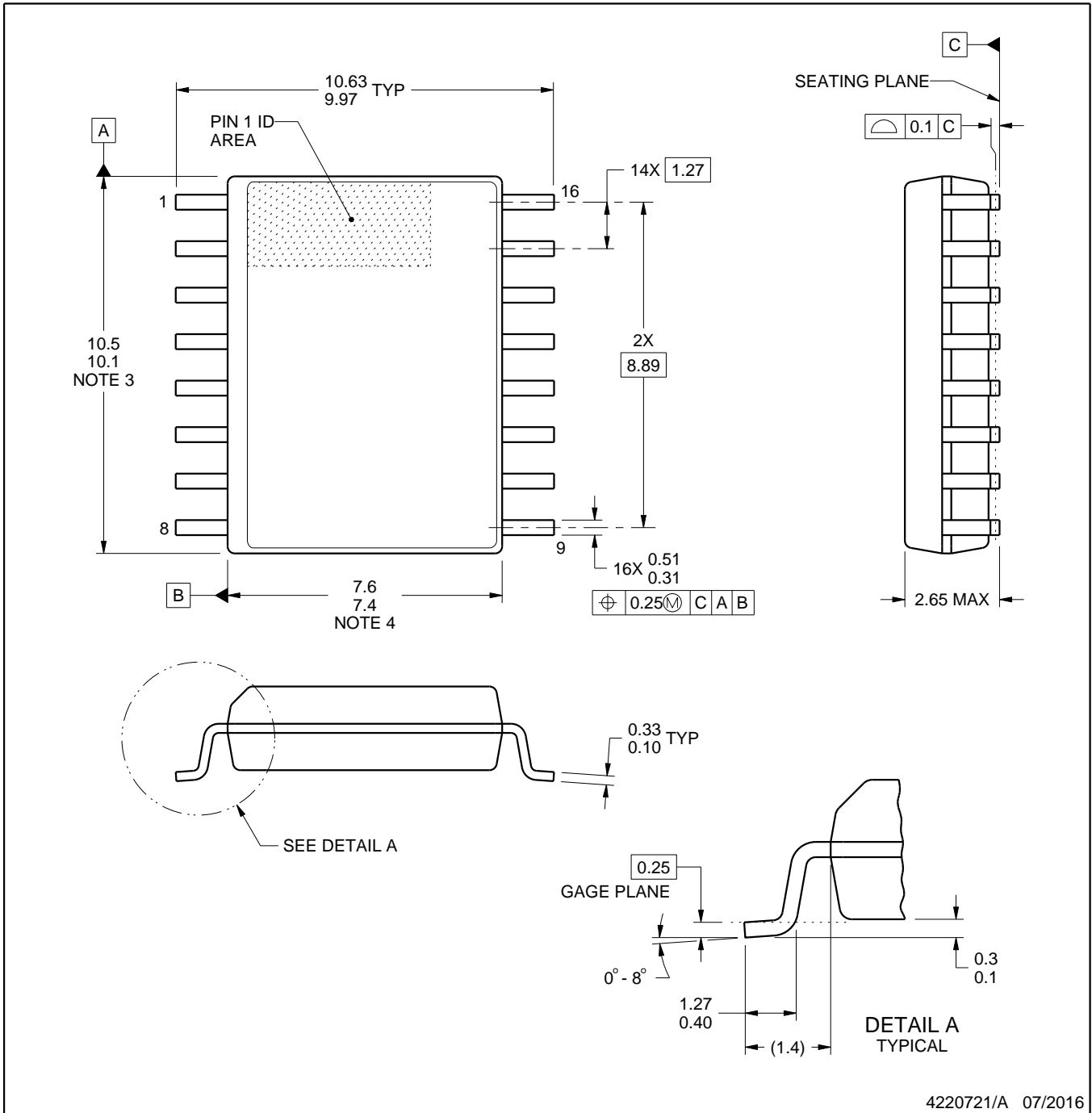


# DW0016A

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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