THE DATASHEET OF

MAX24001TL+

MAX24001

2.5Gbps Tx Burst-Mode Laser Transceiver

General Description

The MAX24001 is a complete burst-mode laser driver transmitter and limiting amplifier receiver for use within fiber optic modules for FTTx applications. A fully compliant GPON/GEPON module with digital diagnostics can be realized when used with a 2KB EEPROM and suitable optics. Alternatively, a microcontroller can be used in conjunction with the MAX24001; however, this is not a necessity in order to achieve SFF-8472 compliance.

The 2.5Gbps limiting receive path features programmable output swing control, rate selection, and OMA-based loss-of-signal detection. Functions are also provided which facilitate the implementation of APD biasing without the need for an external DC-DC converter.

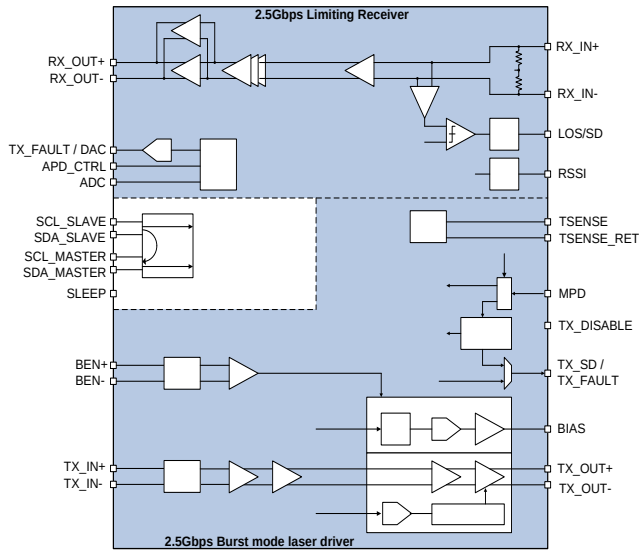
The burst-mode laser driver has temperature compensated modulation control using a lookup table. Closed-loop control of laser power incorporates tracking error compensation and has multiple options for rapidly settling the laser power thus enabling fast registration and shutdown on the network. Diagnostics are enhanced with the inclusion of programmable transmit signal detection during bursts, and rogue ONU detection between bursts. This is linked to a laser safety system which allows the modulation and bias currents to be shut off in response to a range of different fault conditions detected on-chip.

The transmit and receive systems are independently powered and can respond separately to the SLEEP pin. The MAX24001 is highly configurable from either EEPROM or low-cost MCU using a two-wire interface.

Applications

GPON, GEPON, Gigabit Ethernet

Functional Diagram



Features

- **2.5Gbps Limiting Receiver**
- **Integrated APD Bias Loop With Overvoltage And Overcurrent Protection**
- **OMA-Based LOS Detection**
- **1.25Gbps to 2.5Gbps Laser Driver**
- **CML, LVPECL, HSTL, SSTL-Compatible Inputs**
- **Open and Closed-Loop Bias Control**
- **Temperature-Compensated I_{MOD} Control**
- **Highly Configurable Laser Safety System**
- **Transmit TX_SD and Rogue ONU Detection**
- **SFP MSA and SFF-8472 Digital Diagnostics**
- **Integrated Temperature Sensor**
- **Power-Saving SLEEP Modes**
- **External DAC, ADC, and PWM Interfaces**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX24001TL+	-40°C to +95°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

19-6460; Rev 2; 2/14

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{DD_TX}, V_{DD_TXO}, V_{DD_RX}, V_{DD_RXO} ..... -0.3V to +3.65V
Voltage Range on Any Pin Not Otherwise Specified (with respect to V_{SS_*}) ..... -0.5V to (V_{DD_*} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 35.7mW/°C above +70°C) 2857.1mW
Operating Temperature Range ..... -40°C to +95°C
Junction Temperature ..... +150°C
Storage Temperature ..... -70°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V_{DD}		3.0	3.3	3.6	V
RSSI Pin Compliance		ROSA sourcing to RSSI pin			V_{DD} - 0.75	V
		ROSA sinking from RSSI pin	0.75			V
BIAS Pin Compliance			0.8			V
TX_OUT Pin Compliance			0.8			V
MPD Input Current		For correct APC loop operation	40		2000	µA
MPD Input Capacitance		For correct APC loop operation	4		20	pF
Junction Temperature			-40		+120	°C
Case Temperature			-40		+95	°C

Device not guaranteed to meet parametric specifications when operated beyond these conditions. Permanent damage may be incurred by operating beyond these limits.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.97V to 3.63V, T_A = -40°C to +95°C.) (Note 1)

Note 1: Electrical specifications are production tested at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization. Typical specifications are at T_A = +25°C, 3.3V.

CONTINUOUS RATINGS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{DD}	Excluding laser bias and modulation currents, 20mA bias and modulation current, Rx CML output 400mV_{P-P}		136		mA

RECEIVER CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Impedance			80	100	120	Ω
Maximum Input Data Rate				2.5		Gbps
Minimum Input Data Rate				1.25		Gbps
Input Sensitivity		Differential, BER = 1E-10, 2.5Gbps, PRBS 2^{23}-1 pattern		6.5	13	mV_{P-P}
Deterministic Jitter		2.5Gbps, V_{OUT} = $800mV_{P-P}$, V_{IN} between $25mV_{P-P}$ differential and $1000mV_{P-P}$		40		ps_{P-P}
Random Jitter		2.5Gbps, V_{OUT} = $800mV_{P-P}$, V_{IN} between $25mV_{P-P}$ differential and $1000mV_{P-P}$		2.7		ps_{RMS}
Output Rise/Fall Times		2.5Gbps, V_{OUT} = $800mV_{P-P}$, V_{IN} = $25mV_{P-P}$ differential and $1000mV_{P-P}$		60		ps
Low-Frequency Cutoff				30		kHz
Output Impedance		1MHz differential	80	100	120	Ω
Minimum Output Swing		Differential, 4-bit programmable (Note 2)		200	240	mV_{P-P}
Maximum Output Swing		Differential, 4-bit programmable (Note 2)	800	880		mV_{P-P}

Note 2: Measured with 1111111100000000 pattern.

LOSS OF SIGNAL AND RSSI CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum OMA LOS Assert Time				11		µs
Maximum OMA LOS Deassert Time				11		µs
Maximum LOS Threshold Setting				400		mV_{P-P}
LOS Assert/Deassert Level		LOS DAC = 50 (Note 3)		67		mV_{P-P}
		LOS DAC = 105 (Note 3)		143		mV_{P-P}
Maximum RSSI Current Level		Sourced or sunk from RSSI pin		1200		µA

Note 3: LOS assert and deassert levels can be set independently to define hysteresis.

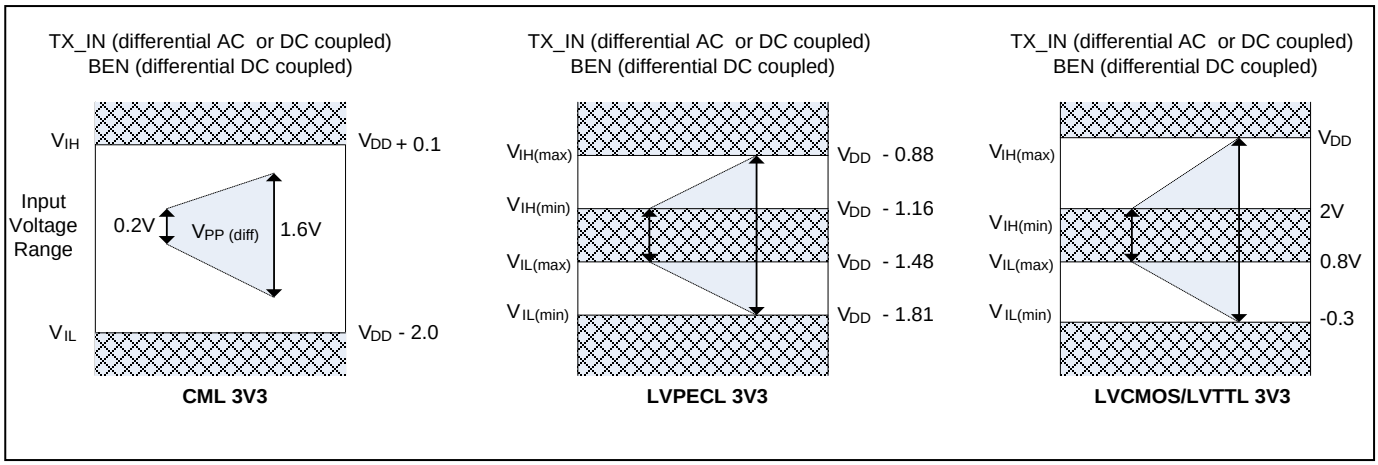
TRANSMITTER CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Input Data Rate		PRBS23		2.488		Gbps
Minimum Input Data Rate		PRBS23		1.25		Gbps
Maximum Modulation Current			80			mA_{P-P}
Minimum Modulation Current				8		mA_{P-P}
Maximum Electrical Rise/Fall Time (20% to 80%)		Measured using 15Ω effective termination, I_{MOD} = $8mA_{P-P}$ to $80mA_{P-P}$		96		ps
Total Jitter		PRBS15, 2.488Gbps, I_{MOD} = $8mA_{P-P}$ to $80mA_{P-P}$, differential electrical measurement		65	175	mUI_{P-P}
Deterministic Jitter		PRBS15, 2.488Gbps, I_{MOD} = $8mA_{P-P}$ to $80mA_{P-P}$, differential electrical measurement		45		mUI_{P-P}
Random Jitter		PRBS15, 2.488Gbps, I_{MOD} = $8mA_{P-P}$ to $80mA_{P-P}$, differential electrical measurement		1.11		mUI_{RMS}
Maximum Bias Current				90		mA

BURST TIMINGS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Burst Enable/Disable Time (Electrical)		Disable: Bias current reduced to 20% of its maximum value. Enable: Bias current increased to 90% of desired bias plus modulation current Target bias current > 3mA		7	12	ns
Minimum Burst Length to Update APC Loop		During closed-loop operation		90		ns
Minimum Burst Gap		During closed-loop operation		75		ns
Maximum Initial Mean Power Control Settling Time (APC Loop)		From power-on, negation of TX_DISABLE, or negation of SLEEP to 90% of desired optical power. Fast settling algorithm enabled, no fast start LUT. Bias current overshoot < 10% Bias current > 4mA		1.2		ms

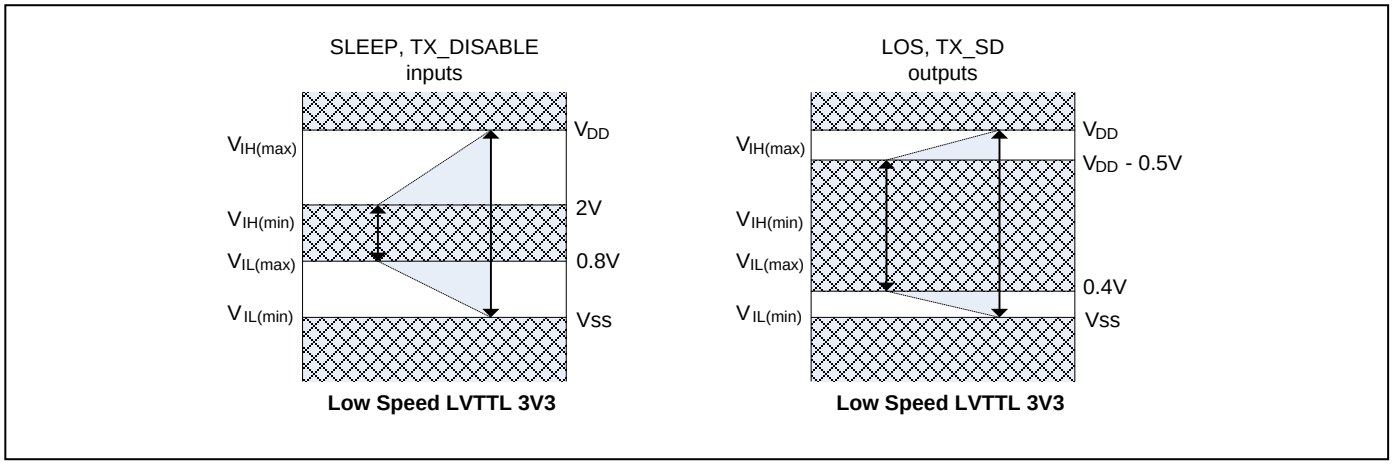
TRANSMITTER INPUT CHARACTERISTICS



Typical I/O ranges for TX_IN and BEN are shown. TX_IN and BEN inputs are also compatible with HSTL and SSTL for low-voltage operation.

DIGITAL I/O CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time To Initialise		From power-up or hot plug		71		ms
TX_DISABLE Assert		TX_DISABLE assert to optical disable		0.3		µs
TX_DISABLE Negate		TX_DISABLE negate to optical enable		0.5		ms
TX_DISABLE to Reset		Time TX_DISABLE must be held high to reset TX_FAULT		0.155		µs
Maximum Delay BEN Change to TX_SD Response		Rising or falling edge		100		ns
Light During Gap to Laser Shutdown		Rogue ONU		100		µs



Typical I/O Ranges for SLEEP, TX_DISABLE, LOS and TX_SD

PERIPHERAL FUNCTIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-On-Reset (POR) Voltage		Module 3V3 supply voltage above which reset will not be asserted			2.5	V
		Module 3V3 supply voltage below which reset is guaranteed	2.2			V

APD Control

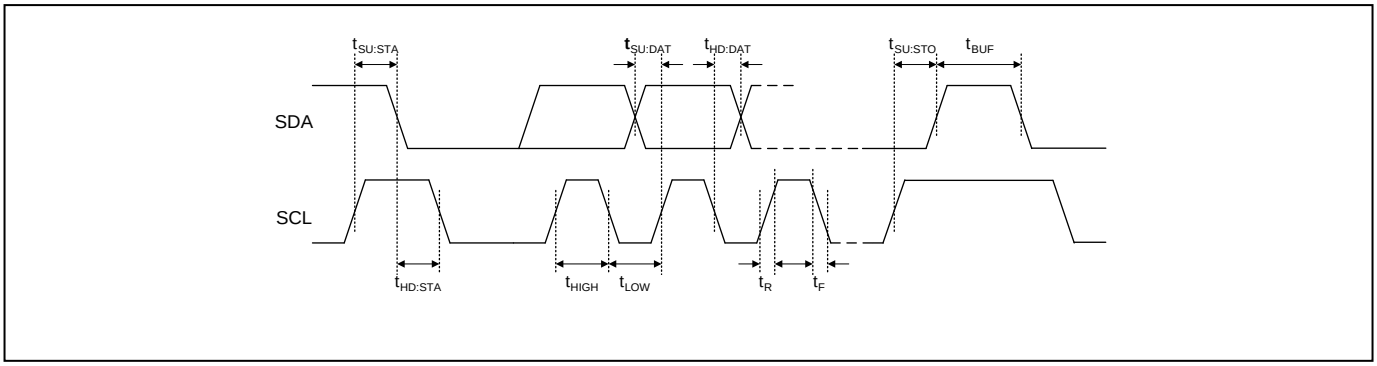
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Pin Minimum Voltage					1.30	V
ADC Pin Maximum Voltage			2.25			V
DAC Pin Minimum Current				0		mA
DAC Pin Maximum Current				0.45		mA
DAC Pin Compliance				1.5		V
PWM Frequency		Minimum PWM frequency		250		kHz
		Maximum PWM frequency		2		MHz
Step Response Settling Time		Load current change from 20µA to 1mA		2		ms

SLEEP

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sleep Assert/Deassert		Time to allow first operation or enter sleep from deassertion of sleep pin		100		ns

TWO-WIRE INTERFACE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum SCL Clock Frequency				400		kHz
Minimum SCL Clock LOW Period	t_{LOW}			1200		ns
Minimum SCL Clock HIGH Period	t_{HIGH}			600		ns
Minimum Setup Time For A Repeated START Condition	$t_{SU:STA}$			600		ns
Minimum Hold Time (Repeated) START Condition	$t_{HD:STA}$			600		ns
Minimum Data Hold Time	$t_{HD:DAT}$			0		ns
Minimum Data Setup Time	$t_{SU:DAT}$			100		ns
Minimum Setup Time for STOP Condition	$t_{SU:STO}$			600		ns
Minimum Bus Free Time Between a STOP and START Condition	t_{BUF}			1200		ns
Maximum Rise and Fall Times of Both SDA and SCL Signals	t_R, t_F			300		ns
Minimum Rise and Fall Times of Both SDA and SCL Signals	t_R, t_F	C_b = capacitance of a single bus line C_x = 20 + 0.1 x Cb		Cx		ns
Maximum Capacitance for Each I/O Pin				10		pF

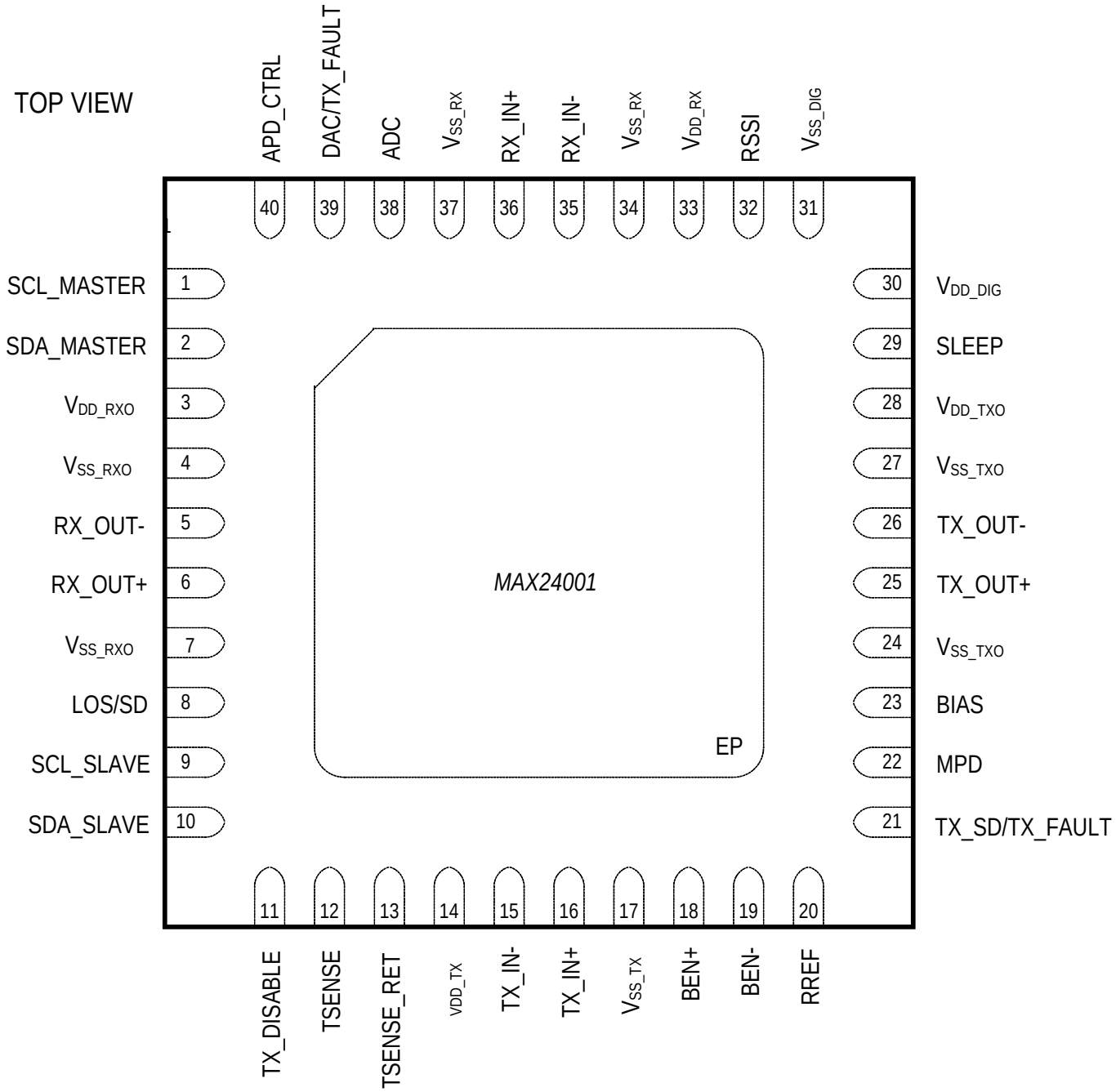


DIGITAL DIAGNOSTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TEMPERATURE						
Reporting Resolution		-40°C to +95°C range		0.85		°C/LSB
Maximum Inaccuracy		Single-point calibration, external mode		±2		°C
POWER SUPPLY						
Reporting Resolution		3.0V to 3.6V range		10		mV/LSB
Maximum Inaccuracy		Calibrated, within the supply reporting range		±3		%
TX BIAS						
Reporting Resolution		5mA to 90mA range		0.392		mA/LSB
Maximum Inaccuracy		Calibrated, within the Tx bias reporting range		±10		%
TX POWER						
MPD Current Reporting Resolution		**mpd_range** = 00, 40µA to 200µA		0.78		µA/LSB
		mpd_range = 01, 100µA to 800µA		3.125		µA/LSB
		mpd_range = 10, 400µA to 2000µA		12.5		µA/LSB
Maximum Inaccuracy		Calibrated, within the MPD operating range		±20		%
RX POWER						
RSSI Current Reporting Resolution		0 to 16µA (Note 4)		0.5		µA/LSB
		16µA to 206µA (Note 4)		2.0		µA/LSB
		206µA to 1000µA (Note 4)		8.0		µA/LSB
Maximum Inaccuracy		3µA to 25µA, calibrated (Note 4)		±25		%
		25µA to 1000µA, calibrated (Note 4)		±10		%

Note 4: rx_rssi_scale = 00 (x1 gain) range and resolution settings can be changed to improve accuracy.

Pin Configuration



TQFN
(5mm x 5mm)

Pin Description

PIN	NAME	DIR	TYPE	FUNCTION
1	SCL_MASTER	O/P	LVTTL	Two-Wire Interface Clock Connection To EEPROM, with Internal 10kΩ Pullup Resistor
2	SDA_MASTER	I/O	LVTTL	Two-Wire Interface Data Connection To EEPROM, with Internal 10kΩ Pullup Resistor
3	V_{DD_RXO}	Analog	+3.3V	Receiver Output Power Supply
4	V_{SS_RXO}	Analog	GND	Receiver Output Ground Connection
5	RX_OUT-	O/P	High Speed	Limiting Receiver Inverted Output. 100Ω differential to RX_OUT+.
6	RX_OUT+	O/P	High Speed	Limiting Receiver Noninverted Output. 100Ω differential to RX_OUT-.
7	V_{SS_RXO}	Analog	GND	Receiver Output Ground Connection
8	LOS/SD	O/P	LVTTL	Loss-Of-Signal Indication. Open drain with external 4.7kΩ to 10kΩ resistor.
9	SCL_SLAVE	I/P	LVTTL	Two-Wire Interface Clock Connection To Host. with external 10kΩ pullup resistor
10	SDA_SLAVE	I/O	LVTTL	Two-Wire Interface Data Connection To Host. with external 10kΩ pullup resistor
11	TX_DISABLE	I/P	LVTTL	Internally pulled high to V_{DD_DIG} with a 7.5kΩ resistor
12	TSENSE	Analog	Analog	Temperature Sensor Current Force
13	TSENSE_RET	Analog	Analog	Temperature Sensor Current Return
14	V_{DD_TX}	Analog	+3.3V	Transmitter Power Supply
15	TX_IN-	I/P	High Speed	Transmitter Input Signal Inverted
16	TX_IN+	I/P	High Speed	Transmitter Input Signal Noninverted
17	V_{SS_TX}	Analog	GND	Transmitter Ground Connection
18	BEN+	I/P	High Speed	Burst-Enable Noninverted
19	BEN-	I/P	High Speed	Burst-Enable Inverted
20	RREF	Analog	Analog	Connects to External Precision Resistor
21	TX_SD/ TX_FAULT	O/P	LVTTL	Push-Pull Signal Detect Indication. Can be configured as open-drain TX_FAULT output, pulled high externally using a 4.7kΩ to 10kΩ resistor.
22	MPD	I/P	Analog	Monitor Photodiode Input
23	BIAS	Analog	Analog	Bias Current Sink
24	V_{SS_TXO}	Analog	GND	Transmitter Output Ground Connection
25	TX_OUT+	O/P	High Speed	Laser Data Differential Drive Output
26	TX_OUT-	O/P	High Speed	Laser Data Differential Drive Output
27	V_{SS_TXO}	Analog	GND	Transmitter Output Ground Connection
28	V_{DD_TXO}	Analog	+3.3V	Transmitter Output Power Supply
29	SLEEP	I/P	LVTTL	Sleep Mode Select
30	V_{DD_DIG}	Analog	+3.3V	Digital Power Supply
31	V_{SS_DIG}	Analog	GND	Digital Ground Connection
32	RSSI	I/P	Analog	Rx Photodiode Monitor (RSSI)
33	V_{DD_RX}	Analog	+3.3V	Receiver Power Supply
34	V_{SS_RX}	Analog	GND	Receiver Ground Connection
35	RX_IN-	I/P	CML	Receiver Input Signal. Differential 100Ω with RX_IN+.
36	RX_IN+	I/P	CML	Receiver Input Signal. Differential 100Ω with RX_IN-.
37	V_{SS_RX}	Analog	GND	Receiver Ground Connection
38	ADC	I/P	Analog	Voltage Input to On-Chip ADC
39	DAC/TX_FAULT	O/P	Analog	Current Output For APD Loop Control. Can be configured as open-drain TX_FAULT output, pulled high externally using a 4.7kΩ to 10kΩ resistor.
40	APD_CTRL	O/P	LVTTL	3V3 Push-Pull APD Bias PWM Output. Can be configured as open-drain APD bias shutdown pin, pulled high externally using a 4.7kΩ to 10kΩ resistor.
—	EP	Analog	GND	Exposed Pad. Solder to board to provide effective thermal connection to circuit board

Detailed Description

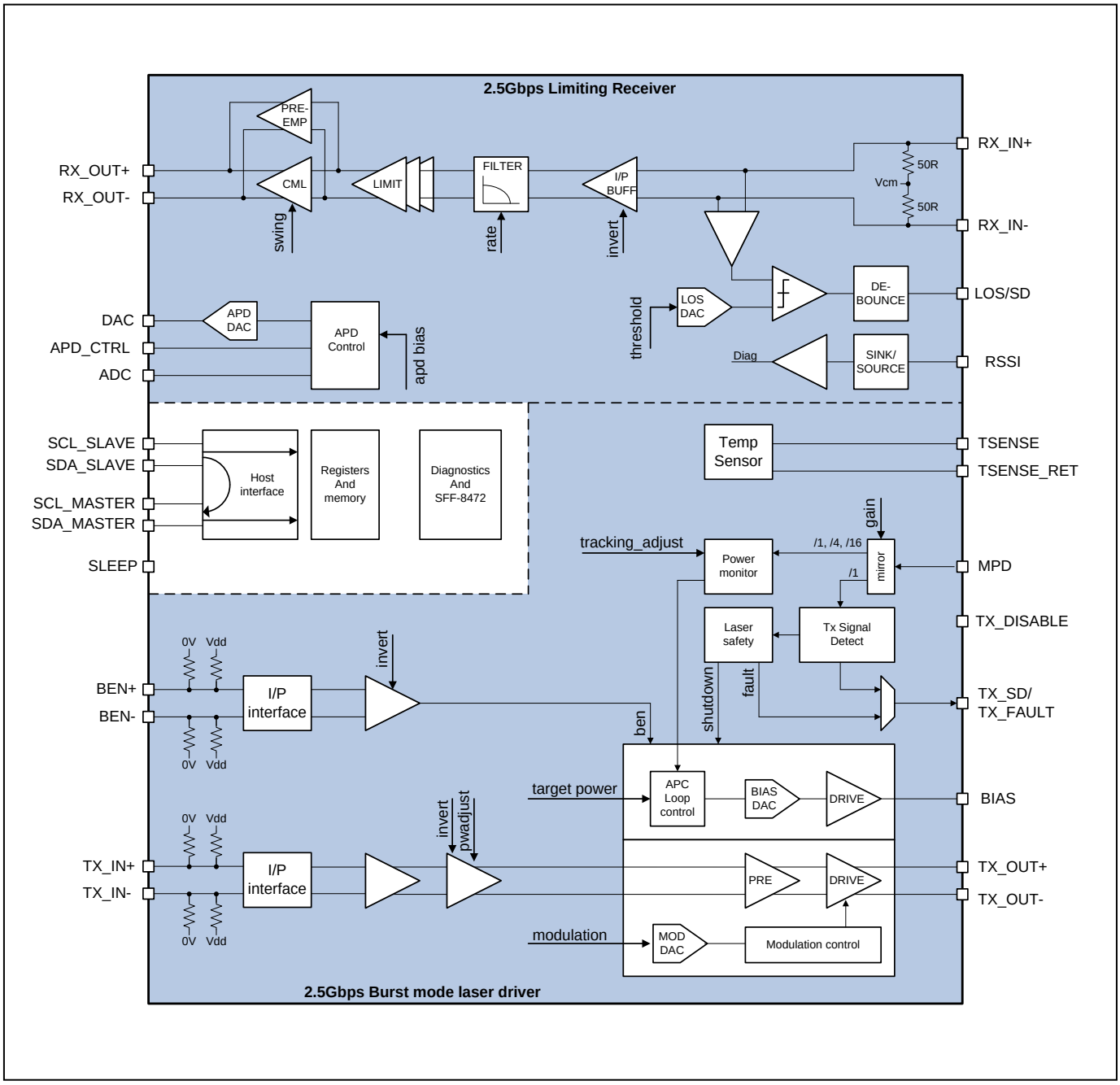


Figure 1. MAX24001 Block Diagram

Receiver Signal Path

[Control Register Address Range A4h: 90h to 93h]

The signal arriving at RX_IN is terminated with a 100Ω load to minimise return loss. An input buffer adds peaking to compensate for up to 10mm of FR4. The level of peaking is controlled by the **rx_input_peak** register. The signal can also be inverted using **rx_invert**.

rx_ratesel0 or rx_ratesel1	BANDWIDTH (GHz)	BIT RATE (Gbps)
00	1	1.25
01	1.8	2.488

The received signal is then band limited to one of two rates selected by the **soft_rate_select** bit of the **system_control** register (A2h: 7Bh). If **soft_rate_select** = '0' then select **rx_ratesel0** else select **rx_ratesel1**. Filter bandwidths are nominally designed to be 0.7x the available data rates.

The CML output stage is a high-current driver that delivers a 200mV to 880mV signal from a low-impedance 50Ω output. The **rx_output_swing** register is used to control the signal at RX_OUT with 45mV resolution. Pre-emphasis may also be applied to the output signal using **rx_preemphasis**. The pre-emphasis (defined as ((B-A)/B) x 100) can be set to 0%, 2%, 6% or 10%. The pre-emphasis ratio remains relatively constant when A is adjusted.

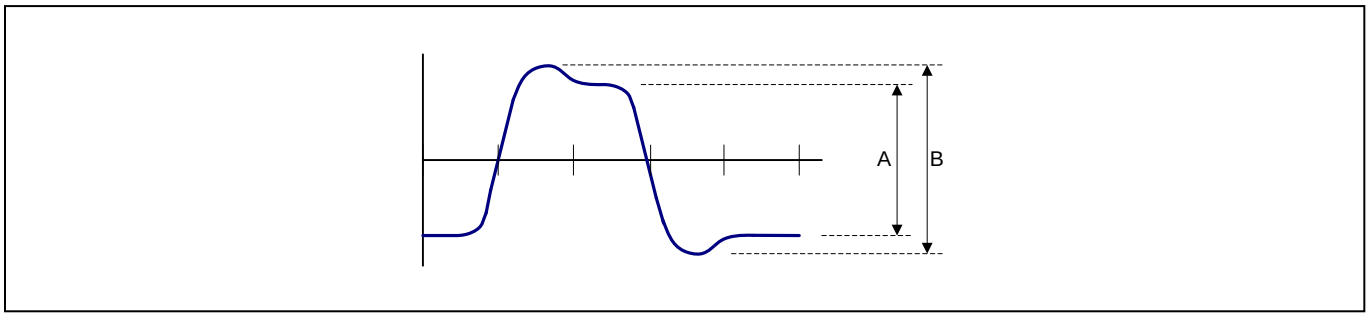


Figure 2. Rx Pre-Emphasis Control

The CML, pre-emphasis and limiting stages may be automatically powered down under loss-of-signal conditions (LOS = '1') by setting the **los_squelch** register. This feature uses the debounced LOS signal prior to any inversion caused by setting **los_invert**. Alternatively, the CML, pre-emphasis and limiting stages may be directly powered down by setting the **squelch** register.

Receiver Loss of Signal (LOS)

[Control Register Address Range A4h: 9Bh to 9Dh]

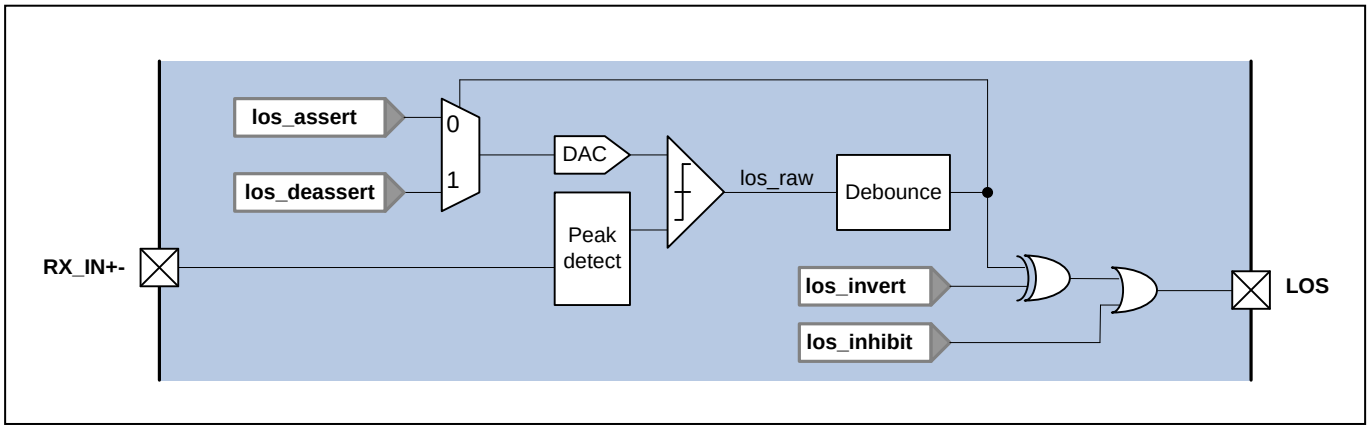


Figure 3. LOS Detection System

When the peak signal amplitude detected at RX_IN drops below the threshold level set by **los_assert** then a loss-of-signal condition is reported on the LOS pin and the **los_deassert** threshold is selected. The signal amplitude must then rise back above the threshold set by **los_deassert** before the loss-of-signal condition is removed and the **los_assert** threshold is re-selected. The two thresholds can be used to introduce a wide range of hysteresis into LOS detection. The deassert threshold level should be higher than the assert threshold for correct operation.

When the comparator output (`los_raw`) changes, the los debounce circuit holds the new value at its output for a programmable period of time controlled by **los_debounce**. Longer debounce timeout periods may be required to accommodate the much longer timeframe pulses caused by the response of the TIA AGC when the signal is suddenly interrupted. The decay of the differential signal is characterized by an unwanted signal crossover as shown in the diagram below. The unwanted pulse on `los_raw` is rejected by setting the debounce period to > 50µs.

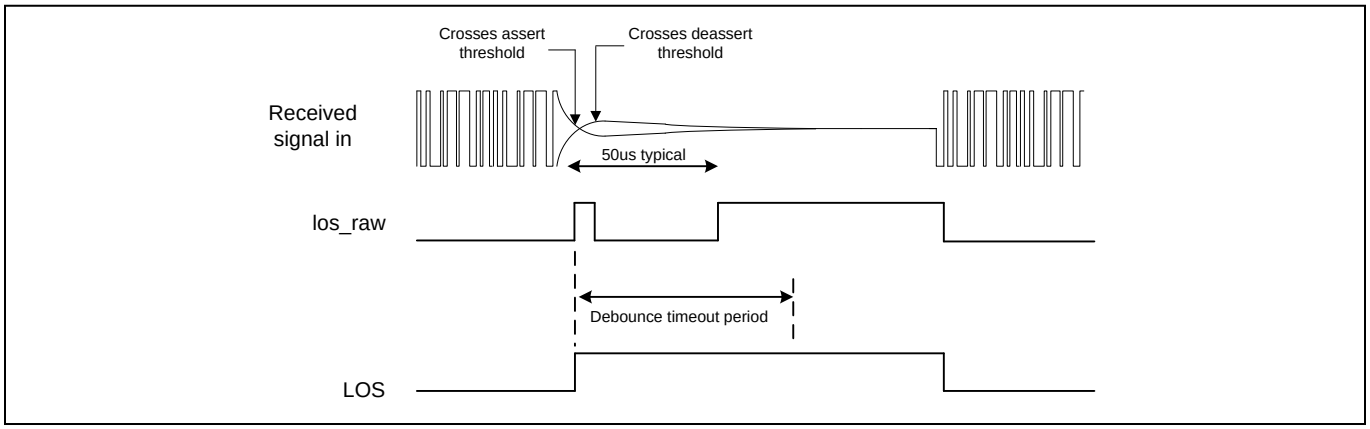


Figure 4. LOS Debounce Operation

The **los_invert** register is used to configure the pin for Signal Detect (SD) instead of LOS. An output mask (**los_inhibit**) holds the output to the LOS pin high after power-on reset until the configuration register load from EEPROM or microcontroller is complete. This avoids multiple transitions on the LOS pin during initialization, which can cause fault conditions to occur at the system level.

Transmitter Signal Path
[Control Register Address Range A4h: 9Eh to A1h]

The input to the transmitter signal path supports CML, LVPECL, HSTL, and SSTL electrical signalling schemes with a minimum of external components. The input may be either DC or AC coupled. An external 100Ω resistor provides differential termination. The internal potential dividers set the common mode level at 2.0V when the input is AC-coupled.

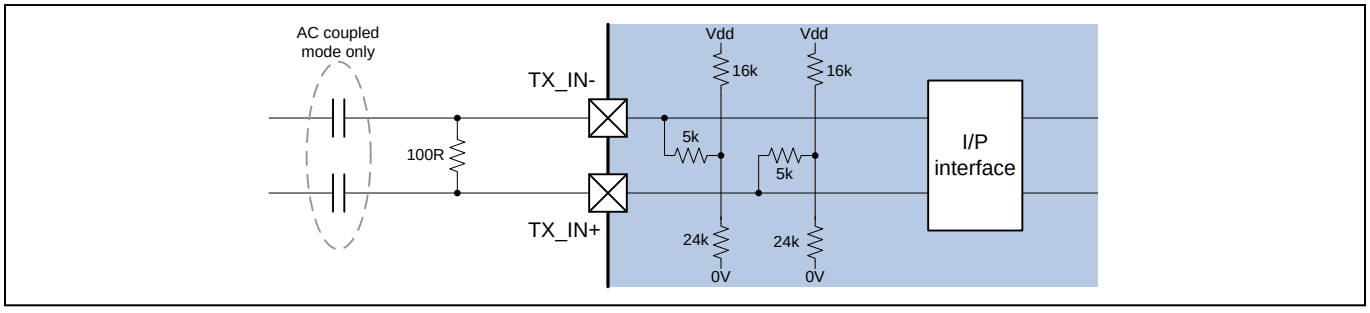


Figure 5. TX_IN and BEN Input Termination and Signal Conditioning

The laser modulation current is controlled by the **tx_moddac** register with a resolution of 375µA per LSB (nominally). This register may be set by the host, or alternatively set the **modlut_en** bit to cause the **tx_moddac** register to be automatically refreshed from the modulation lookup table (LUT) every 10ms. The modulation LUT is stored in external EEPROM at TWI slave address A6h, register address range 80h to FFh. It is indexed using the upper 7 bits of **temperature_uncal**.

If the **modramp_en** register is set then the value in **tx_moddac** ramps progressively from the old value to the new value by 1 LSB every cycle of the internal 64MHz clock. This prevents glitches from occurring in the DAC. If ramping is disabled then updates to **tx_moddac** are effective immediately. The modulation current is switched off between bursts and when the laser safety system asserts a shutdown. **burst_invert** is used to invert the differential signal on BEN±. **tx_invert** is used to invert the polarity of the transmit signal path.

Eye Optimization

The pulse width of the transmitted signal is adjusted by moving the crossing point of the eye up or down using **tx_pwadjust_dir**. Use the **tx_pwadjust_size** to control the amount of adjustment, in the direction set by **tx_pwadjust_dir**. At maximum adjustment, the zero crossing point (a) is moved by 40% of the 0-pk eye opening (b). The **tx_pwadjust_hires** register can be used to halve the adjustment step size and thus increase resolution (at the expense of halving the range).

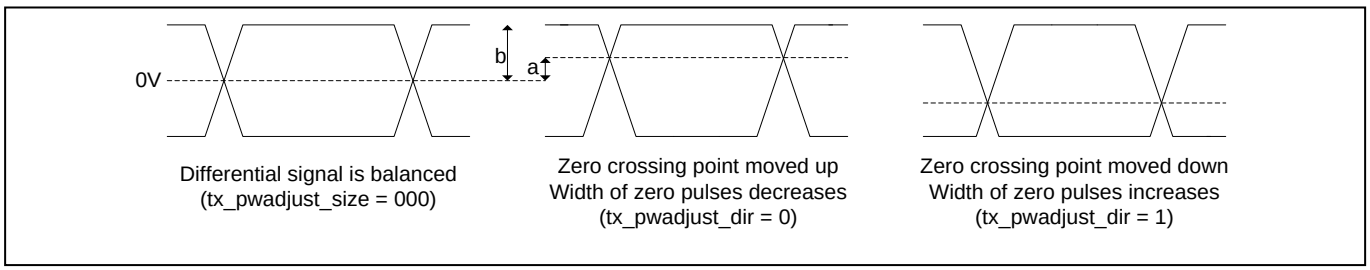


Figure 6. Crossing Point Adjustment

The **tx_snubber** register is used to snub out overshoot or undershoot in the output eye.

Tx Signal Detect
[Control Register Address Range A4h: ADh to AEh, BEh to BFh]

The Tx Signal Detect feature comprises two related areas of functionality:

For external signal and rogue ONU fault detect by the host, the MAX24001 controls the TX_SD pin as follows: TX_SD = '1' when there is light; TX_SD = '0' when there is no light from the laser.

For on-chip "Rogue ONU fault detect", the MAX24001 detects the presence of light during the burst gap. This fault condition is input to the laser safety system which can then optionally shut down the laser within 100µs of light being detected.

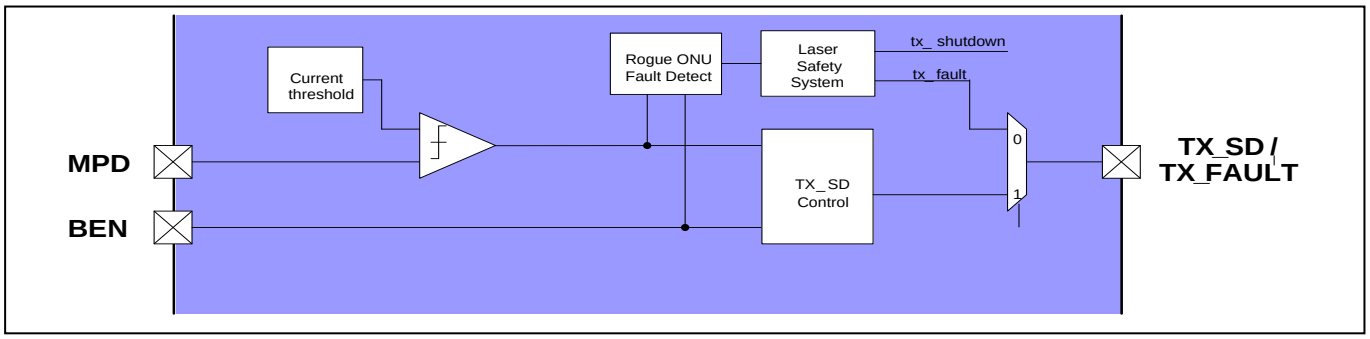


Figure 7. TX_SD Pin Signal Generation

The MPD current is compared with a threshold current set by the **txsd_threshold** register. This determines the MPD current level at which both TX_SD and rogue ONU are detected.

When BEN = '0' the TX_SD logic transfers the comparator output directly through to `tx_sd`. In addition, the Rogue ONU Fault Detect logic transfers the comparator output through to the laser safety system. The **txsd_rogueonu_delay** register specifies the delay (in cycles of the internal 64MHz clock) between the falling edge of BEN and testing for rogue ONU. The rogue_onu_fault condition is not generated during this time.

When BEN = '1' the TX_SD logic output goes high when the input from the comparator goes high. This state is latched. The `tx_sd` signal will then remain high until either the end of the burst, or until the comparator output remains low for a period of time exceeding the time defined by the **txsd_deglitch_period** register. This prevents `tx_sd` from toggling during a burst due to the pattern sensitivity of the MPD current. (During bias loop fast-start, `tx_sd` is held at '1')

Selection between TX_SD and TX_FAULT functionality is governed by the **txsd_select** register. The **txsd_allow** register holds the pin high until the configuration register load from EEPROM (or microcontroller) is complete. This avoids multiple transitions on the TX_SD pin during initialization.

Rogue ONU Behavior

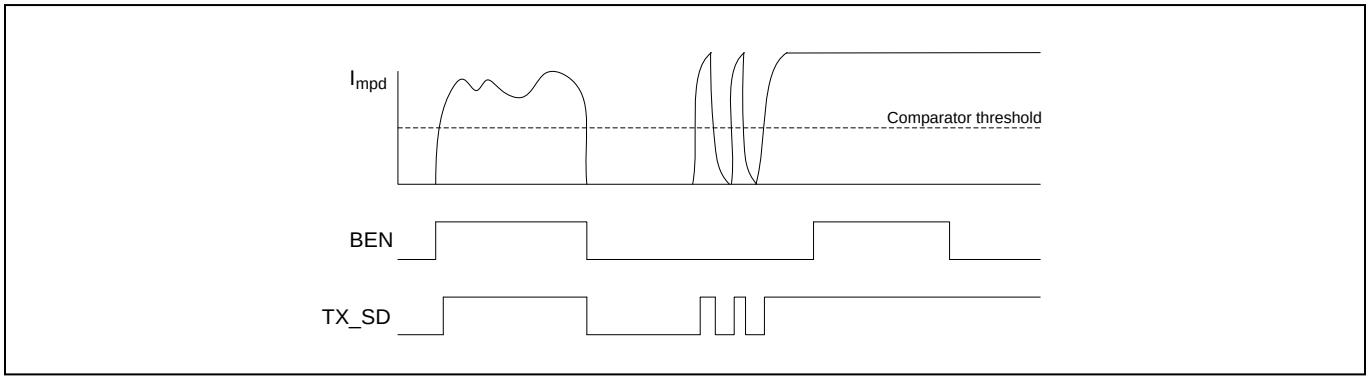


Figure 8. Rogue ONU Timing

TX_SD Behavior

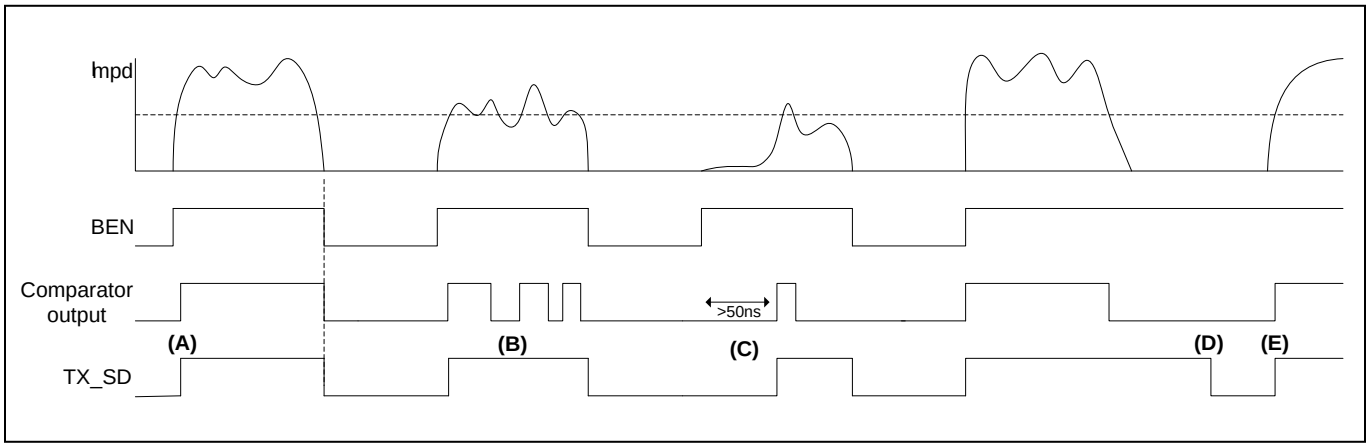


Figure 9. TX Signal Detect Timing

During the gaps the TX_SD logic is transparent and the comparator output is routed directly through to the TX_SD pin.

During the bursts:

(A) The TX_SD pin is asserted high when the MPD current first exceeds the threshold.
(B) The TX_SD pin will not toggle in response to short term fluctuations of the MPD current above and below the threshold (due to the pattern sensitivity of the MPD current).
(C) There is a requirement that the TX_SD pin responds within 50ns of the assertion of BEN. The MPD current is settled and the TX_SD circuitry can respond well within 50ns of the start of a burst. However, the MAX24001 will assert TX_SD high whenever a signal is detected during a long burst—even if the signal does not appear until well after the initial 50ns.
(D) If the laser stops outputting light during a burst, then there is a delay before TX_SD goes low. This is necessary in order to distinguish between the MPD current dipping below threshold due to a run of zeros, and the MPD current dropping below threshold due to a legitimate loss of signal. The delay is programmable using **txsd_deglitch_period**.
(E) If the signal is restored during a burst then TX_SD is asserted high again.

Laser Biasing

[Control Register Address Range A4h: A2h to A9h]

The bias current is controlled by the **tx_biasdac** register in one of six operating modes:

OPERATING MODE	DESCRIPTION	tx_biasmode <2:0>
Open loop, static	tx_biasdac only changes when it is written by the host	000
Open loop, LUT	tx_biasdac is constantly refreshed from values read from a temperature indexed lookup table (the bias LUT)	001
Closed loop, natural start	An automatic power control (APC) loop constantly adjusts tx_biasdac in order to maintain a target laser output power level. tx_biasdac defaults to near-zero after power-up and then converges naturally on the target level over a duration of time dictated by the loop bandwidth.	100
Closed loop, LUT start	The APC loop controls tx_biasdac, and tx_biasdac is preloaded from the bias LUT at power-up.	101
Closed loop, fast start	The APC loop controls tx_biasdac, and a fast-start algorithm is invoked at power-up to rapidly converge the loop on the target power level.	110
Closed loop, LUT fast start	The APC loop controls tx_biasdac. tx_biasdac is preloaded from the bias LUT at power up, and then a fast-start algorithm is invoked to rapidly converge the loop on the target power level.	111

Operational Overview

The **tx_biasmode<2:0>** register is a grouping of three individual controls registers:

tx_biasmode<0>: bias_lut_enable
tx_biasmode<1>: faststart_enable
tx_biasmode<2>: apc_enable

Open-Loop Operation

Clear the **apc_enable** register for open-loop operation.

The laser bias current is controlled by the **tx_biasdac** register with a resolution of 92.5µA per LSB (nominal). This register may be set by the host, or alternatively set the **bias_lut_enable** bit to cause the **tx_biasdac** register to be automatically refreshed from the bias lookup table (LUT) every 10ms. The bias LUT is stored in external EEPROM at TWI slave address A6h, register address range 00h to 7Fh. It is indexed using the upper 7 bits of **temperature_uncal**.

If the **biasramp_en** register is set then the value in **tx_biasdac** ramps progressively from the old value to the new by 1 LSB every cycle of the internal 64MHz clock. This prevents glitches from occurring in the DAC. If ramping is disabled then updates to **tx_biasdac** are effective immediately.

Closed-Loop Operation

Set the **apc_enable** register for closed-loop operation.

The automatic power control (APC) loop compares a value of laser output power produced by the power monitoring circuits with a target level set by **tx_apc_target**. This proportional error value is scaled using the **apc_loop_gain** and is then used to adjust the value of **tx_biasdac** (which has a number of internal precision extension bits). The **apc_loop_gain** register thus controls the bandwidth of the APC loop.

Since the bandwidth of the loop is not very high, it is desirable to set the **tx_biasdac** register to a point as close as possible to the target laser power level before the APC loop takes over. This is achieved by preloading the **tx_biasdac** register with a value from the bias LUT and/or running a search algorithm (referred to as fast-start). These actions are both triggered by the **bias_lut_enable** and **faststart_enable** bits. When these bits are set, then a table lookup or fast-start will occur at the next available opportunity. Once the lookup or fast-start has occurred then these bits are cleared. The host may therefore re-trigger fast/lut start by resetting **bias_lut_enable** and **faststart_enable** at any time. The bits are also set automatically as follows:

On power-up: **tx_biasmode** is configured from EEPROM

During SLEEP: The value in **faststart_after_sleep** is transferred to **faststart_enable**
The value in **bias_lut_after_sleep** is transferred to **bias_lut_enable**

During TX_DISABLE: The value in **faststart_after_txdisable** is transferred to **faststart_enable**
The value in **bias_lut_after_txdisable** is transferred to **bias_lut_enable**

Thus, the required loop behavior when the laser is enabled can be independently configured for reset, sleep mode and tx disable. This is further illustrated in the figure below:

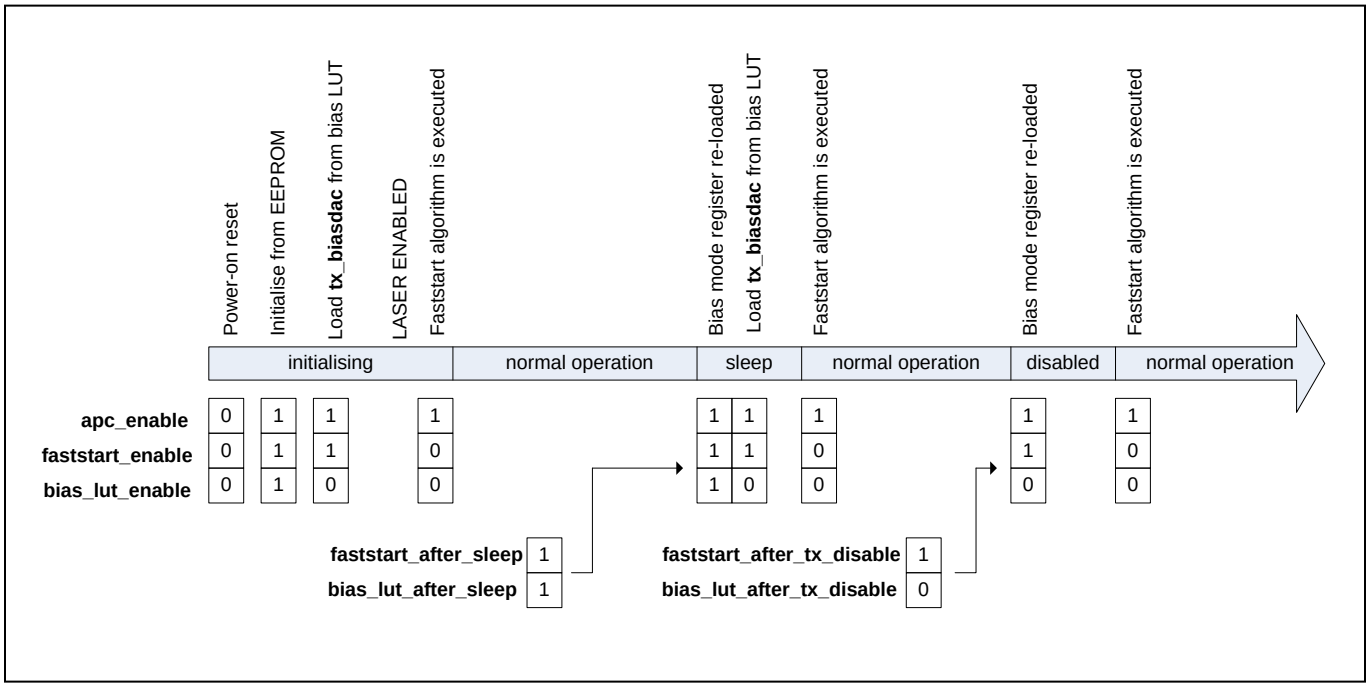


*Figure 10. Behavior of the **tx_biasmode** Register in Closed-Loop Mode*

Fast-Start Algorithm

[Control Register Address Range A4h: AAh to Ach]

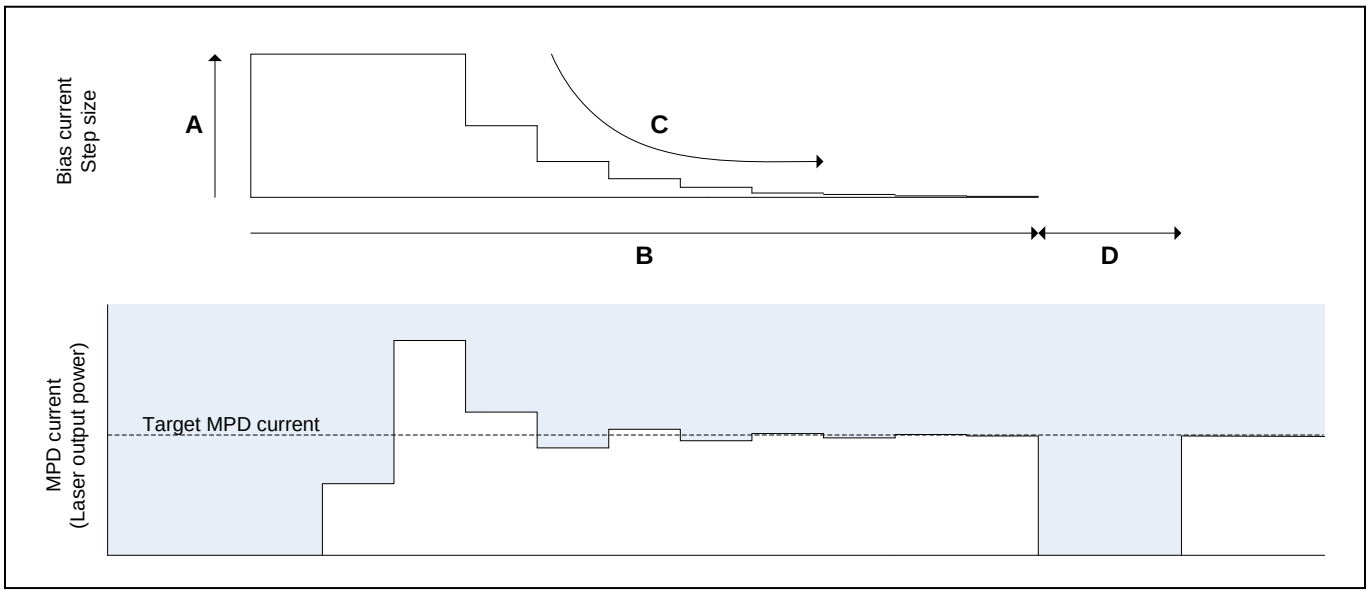


Figure 11. Fast-Start Algorithm Timing

During fast-start, the MAX24001 is temporarily reconfigured. The modulation driver sinks a constant current of $I_{MOD}/2$ on TX_OUT to represent the contribution made by the signal current to the average power. The power monitoring circuit is reconfigured to supply a direct comparison between the received MPD current and the target MPD current. The process of making a change to bias current and then a subsequent comparison of MPD current and target current is referred to as iteration. An iteration has a fixed duration (nominally 62ns).

Initially, the bias current is stepped up on every iteration until the MPD current exceeds the threshold. The initial bias current step size A is ideally ½ the modulation current, the rationale being that this is the largest step which can be taken whilst ensuring that the P1 power level is not exceeded. More generally, the initial step size is defined as A = (**tx_fstart_initial**/256) x I_{MOD}.

When the target level is exceeded the step size then decays (C). Halving the step size every iteration amounts to a binary search. In practice, incomplete settling of the loop can result in a small overshoot of the target current level. It is therefore recommended that each step is slightly more than 0.5x the previous step. This is configurable using the **fstart_decay** register. The **fstart_decay** register determines the multiplication factor applied to the step size on each subsequent iteration of the fast-start algorithm.

f_{start_decay}	STEP DECAY MULTIPLIER
100000	32/64 = 0.5
100001	33/64 = 0.516
100010	34/64 = 0.531
100011	35/64 = 0.547
100100	36/64 = 0.563
100101	37/64 = 0.5785
..	..
101110	46/64 = 0.719
101111	47/64 = 0.734

The direction of each current step depends on whether the measured MPD current is above or below the target level. The number of iterations B is controlled by the **fstart_duration** register. The maximum number of iterations which can be guaranteed to complete within 3 x 400ns bursts is 15.

At the end of the fast-start algorithm, the laser output stage switches from sinking DC $I_{MON}/2$ on TX_OUT to full amplitude signal. This may result in a brief current spike. A facility is provided to optionally shut down the modulation current through the laser during this transition period (D). Use the **fstart_recovery_en** and **fstart_recovery_time** registers to shut down the modulation current for 0, 1, or 2 iterations.

APC Loop Bandwidth

The **apc_loop_gain** register adjusts the gain of the APC control loop. Loop bandwidth (Hz) is calculated as a function of **apc_loop_gain**:

$$\text{Bandwidth (Hz)} = \frac{2^{\text{apc\_loop\_gain - 15}} \times k_{elec} \times k_{mpd} \times (\text{biasdac\_lsb} \times 4) \times f_{CLOCK}}{2 \times p \times 16 \times \text{mondac\_lsb}}$$

$$= 2^{\text{apc\_loop\_gain - 15}} \times k_{elec} \times k_{mpd} \times 3.02 \times 10^{8}$$

Where: mondac_lsb = 0.78µA
biasdac_lsb = 92.5µA
f_{CLOCK} = 64MHz (typical)
kmpd = 0.0625 when **mpd_range** = 10
0.25 when **mpd_range** = 01
1 when **mpd_range** = 00
k_{elec} = (MPD current)/(laser current)

apc_loop_gain	GAIN
0000	2^{-15}
0001	2^{-14}
0010	2^{-13}
:	:
1100	2^{-3}
1101	2^{-2}
1110	2^{-1}
1111	1

Power Monitoring

A power monitoring circuit generates a digital measure of MPD current (laser power) based on time-averaged samples taken during bursts when the laser is enabled. It has three settings in order to accommodate the wide range of monitor photodiode currents. The range setting (**mpd_range**) is chosen at the time that the module is calibrated, and does not change during normal operation of the APC loop. The unfiltered, 8-bit digital measure of MPD current is used internally by the APC loop.

mpd_range	PD MIRROR GAIN	I_{MON} OPERATING RANGE (µA)
00	1	40 to 200
01	1/4	100 to 800
10	1/16	400 to 2000

Tracking error in the TOSA means that the MPD current may vary over temperature in a nonlinear way for a given laser optical power. If the temperature-indexed tracking error lookup table (LUT) is enabled then the digital measure of MPD current is multiplied by the values read from the LUT. Each entry in the LUT represents a number in the range 0.5 (00h) to 1.5 (FFh), and 80h represents unity gain.

Set the **trackinglut_en** bit to enable this feature. A correction factor is retrieved from the tracking error LUT every 10ms. This LUT is stored in external EEPROM at TWI slave address A8h, register address range 80h to FFh. It is indexed using the upper 7 bits of **temperature_uncal**.

The digital measure of MPD current (including tracking error compensation) is used by the APC loop to control bias current.

Power Reporting

For power reporting purposes, the power monitor output is low-pass filtered to suppress the pattern sensitivity of the MPD current. This filter bandwidth is programmable using the mon_bandwidth register. Bandwidth = $64/(2\pi \times 2^{(15-n)})$ where n is the 4-bit integer mon_bandwidth value up to a maximum of 14. The filtered measure of laser power can be read from the txpower_uncal register.

mon_bandwidth	BANDWIDTH at f_{CLOCK} = 64MHz
0000	311Hz
0001	622Hz
..	..
1000	80kHz
..	..
1110	5.1MHz
1111	No filtering

The ***mpd_range*** should be set at a level which accommodates the expected range of MPD current. The MAX24001 is not designed to automatically range switch during normal APC loop operation. However, if the APC loop fails and the power monitor saturates then the ***mpd_range*** will temporarily switch so that power reporting can cover the full 0 to 2mA range of photodiode current. The range then recovers back to the original setting if the power monitor value drops back below 64.

Power Leveling

The power_levelling register implements GPON power levelling. Set to 00, 01, or 1x to reduce the modulation amplitude set by tx_moddac by x1, x0.5 and x0.25, respectively. This register will also reduce the power level by having the same effect on the output of the tx_apc_target register. Power levelling does not affect the bias current in open-loop mode.

Laser Safety

[Control Register Address Range A4h: AFh to B3h]

The laser safety system generates two signals, `tx_fault_int` and `tx_shutdown_int`. `Tx_fault_int` is pure status. It reports via both register and TX_FAULT pin whether one or more enabled fault conditions have occurred. The TX_FAULT pin can be configured to appear at pin 21 or 39 using **pin_config0**. `Tx_shutdown_int` is a control signal. It disables the bias and modulation currents to the laser when one or more enabled fault conditions have occurred.

Fault Conditions

The fault conditions which affect `tx_fault_int` and `tx_shutdown_int` are:

Bias Fault	This occurs when the BIAS pin is shorted to ground.
APC Fault	This occurs when the MPD pin is shorted to ground.
VREF Fault	This occurs when the RREF pin is shorted to ground.
VDD Fault	This occurs when brownouts are detected on TX or TXO.
Tx Disable Fault	Is given by: (TX_DISABLE XOR **tx_disable_invert**) OR **soft_tx_disable** where TX_DISABLE is the pin value and **soft_tx_disable** is in SFF-8472 **status_control**.
Soft Tx Fault	This occurs when the **soft_tx_fault** bit in **software_faults** register is set.
RogueOnu Fault	If the laser is on during a gap between bursts then this fault condition is generated.
Alarm Fault	This occurs when one or more of the SFF-8472 DDM alarm flags are set to '1'. The flags which contribute to Alarm Fault are programmable via **ls_alarmflag_en**.

When the laser is in shutdown then the bias fault condition is ignored by the laser safety system. When `tx_shutdown` is deasserted there is a 250µs delay before the bias fault condition is used. This allows the circuit which detect a ground short on the bias pin time to settle before the bias fault condition is seen by the laser safety system.

Architecture

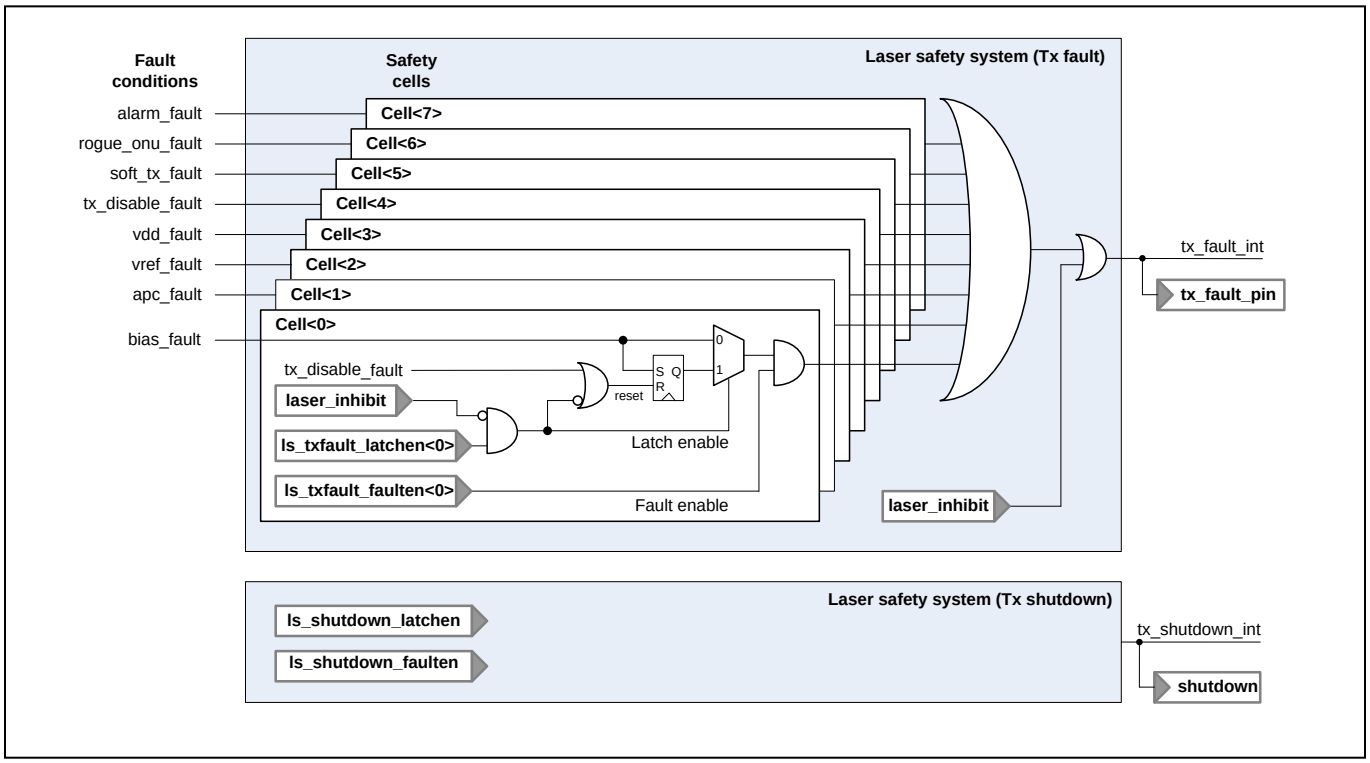


Figure 12. Laser Safety System

The laser safety system (Tx fault) generates the `tx_fault_int` signal. The status of this signal can be accessed in the SFF-8472 **status_control** register. The signal is also multiplexed onto the TX_FAULT/TX_SD pin.

Every safety cell has its own pair of latch enable and fault enable control register bits. The fault condition can only propagate through to the output when **_faulten** = '1'. When **_latchen** = '1' a latched version of the fault condition is used. The latch is held in reset when latching is disabled or when the `tx_disable_fault` signal is asserted. Note that `tx_disable_fault` is also a fault condition signal.

When it is asserted, the **laser_inhibit** signal holds all latches in reset and forces the `tx_fault_int` signal to '1'. Note that after the power-on reset, **laser_inhibit** is enabled. During initialization **pin_config** is the last configuration register to be loaded from EEPROM and therefore has the effect of clearing **laser_inhibit** and thus enabling the laser.

ls_fault_status reports the status of the fault conditions at the inputs to the safety cells.

The laser safety system is fully replicated for controlling laser shutdown. The system uses the **ls_shutdown_faulten** and **ls_shutdown_latchen** registers and produces the `tx_shutdown_int` signal for disabling the modulation and bias currents. The internal architecture is otherwise the same as the system for Tx Fault. The **shutdown** register can be found in **hardware_status**.

The module Tx supply (V_{CC_TX}) can be used in some applications to shut down the laser. This is supported in MAX24001 by detecting the removal of V_{CC_TX} on the V_{DD_TXO} pin. V_{CC_TX} is connected to V_{DD_TXO} as shown in Figure 13. A shutdown is then asserted if the voltage falls below 2.7V. If the connection between V_{CC_TX} and V_{DD_TXO} is not used, V_{DD_TXO} must be connected to another supply.

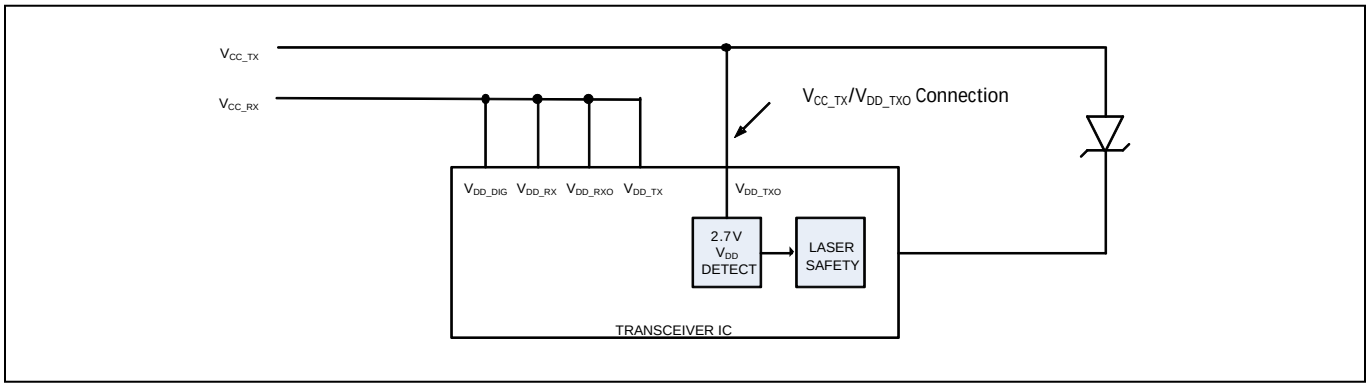


Figure 13. VDD_TXO Configured to Assert Laser Shutdown

Temperature Sensor

[Control Register Address Range A4h: B6h, B9h, C1h]

The MAX24001 includes an integrated temperature sensor that reports the module temperature at the sensor transistor. The **temp_ext_sensor** register selects between an internal transistor or an external PNP transistor connected to the TSENSE and TSENSE_RET pins. If an external transistor is used then the PCB tracks connecting an external PNP transistor to the chip each have resistance << 1Ω. i.e. the tracks must be kept as short as possible. The temperature sensor reports a value in **temperature_uncal** once every 65ms. Resolution is approximately 0.8C per LSB of **temperature_uncal**. Part-to-part accuracy is optimized by adjusting **temp_calibrate** until each part reports the same value of **temperature_uncal** at a common temperature.

Setting **leave_pu** and **tempsense_pu** enables the temperature sensor to be in a power-saving mode by powering down between reads.

APD Controller

[Control register address range A4h: 94h]

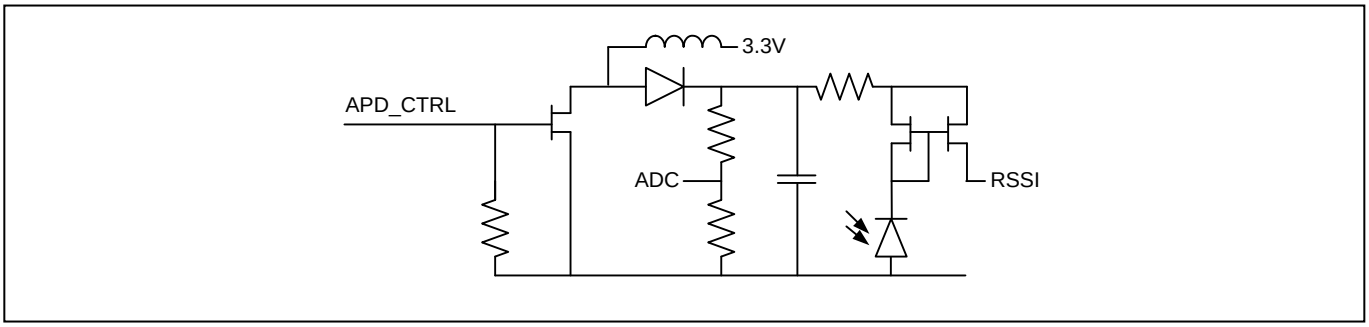


Figure 14. APD Biasing Application

Figure 14 shows a simplified arrangement for controlling the APD bias voltage, whereby the FET is switched by a pulse width modulated signal. The duty cycle can be used to control the voltage across the capacitor. This voltage can be sampled at the tap point of the potential divider. The MAX24001 provides functions which support this approach.

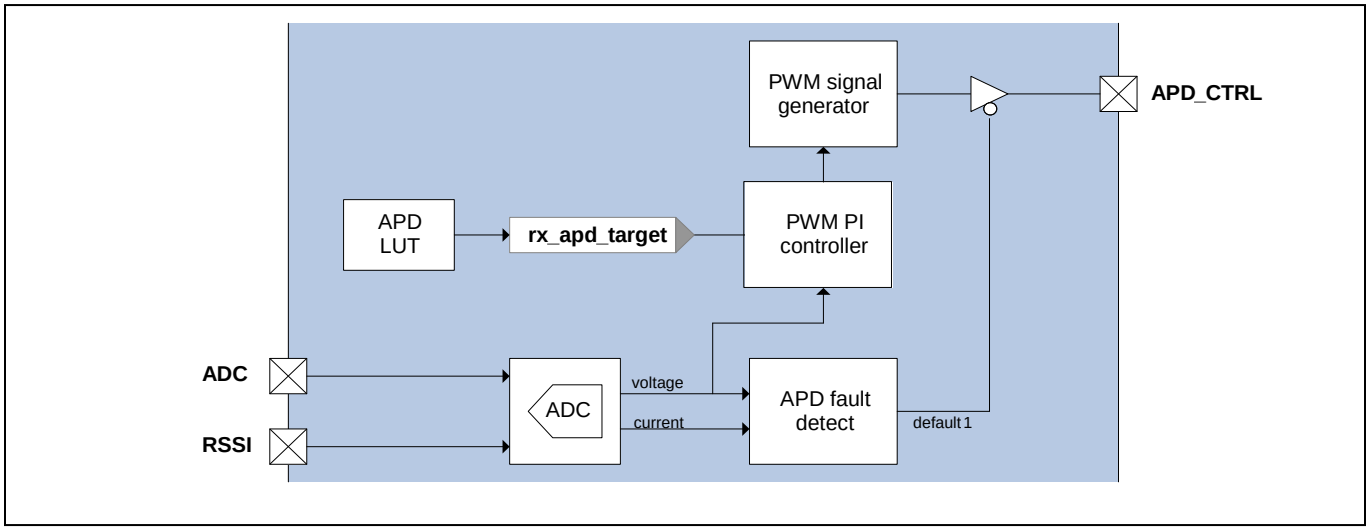


Figure 15. APD Biasing Control Loop Components

The PWM frequency can be configured to be 250kHz, 500kHz, 1MHz or 2MHz by **pwm_frequency**. The 8-bit value of **rx_apdpwm** adjusts the duty cycle from 0/256 to 255/256.

The APD controller adjusts the value of **rx_apdpwm** according to the proportional and integral gain setting of the loop in registers **k_proportional** and **k_integral** such that the voltage level sampled on the ADC pin converges on the target value **rx_apd_target**. The target value apdlut_en may be fixed, or it may be actively refreshed from the temperature indexed APD lookup table (LUT) when **target_lut_enable** is set. This LUT is stored in EEPROM at two-wire slave address A8h, register address range 00h to 7Fh. The LUT is indexed by **temperature_uncal**.

When the APD controller is active, a limit may be imposed on the maximum PWM duty using **max_duty**.

APD Controller—Additional features

APD safety features are also implemented. If the sampled value of RSSI current exceeds **rx_apd_i_threshold**, or the sampled voltage on the ADC pin exceeds **rx_apd_v_threshold** then the APC_CTRL pin driver is disabled (Hi-Z). Set the thresholds to FFh to disable this feature.

The APD controller is disabled when **k_proportional** and **k_integral** are both zero. The value in **rx_apdpwm** can be written directly, or will be periodically refreshed from the APD LUT if **pwm_lut_enable** is set. The polarity of the output on APD_CTRL can be inverted by setting **pwm_invert** to '1'.

If an external control loop is used (for example, using an external DC-DC converter) then this loop could be controlled by the DAC pin. The DAC is controlled from the **rx_apddac** register. This will be periodically refreshed from the APD LUT if **dac_lut_enable** is set. In this arrangement, the APD_CTRL pin can be used to control the shutdown input pin of the DC-DC converter.

Digital Diagnostics

Data Generation

[Control Register Address Range A4h: B4h to B5h, E6h to EAh]

Temperature, supply voltage, laser bias current, transmit power, and received power are all periodically sampled.

Temperature

The uncalibrated temperature can be read from the **temperature_uncal** register.

Supply Voltage

Select between Tx and Rx supply voltages using **adc_supplysel**, and adjust the sampling rate using **supply_bandwidth**. The uncalibrated supply voltage can be read from the **supply_uncal** register.

Tx Bias Current

The bias current measured during a burst will continue to be reported between bursts, irrespective of the length of the gap. If the laser is deliberately shutdown by the laser safety system or by asserting TX_DISABLE then Bias Current reports zero and the low alarm/warning flags are set. The uncalibrated bias current is read from the **bias_uncal** register.

Tx Power

The Tx Power measured during a burst will continue to be reported between bursts, irrespective of the length of the gap. If the laser is deliberately shutdown by the laser safety system or by asserting TX_DISABLE then Tx Power reports zero and the low alarm/warning flags are set. The uncalibrated Tx Power is read from the **txpower_uncal** register.

Rx Power

The RSSI pin can both source and sink a current (**rx_rssi_sink**) which is proportional to the optical power incident on the receiver. Resolution can be enhanced by applying additional gain (x1, x1.5 or x2) to the current at the RSSI pin using the **rx_rssi_scale** register (see **los_rssi_config**).

For Rx power measurement, the ADC is used in nonlinear "3-slope" mode. This provides both wide dynamic range and high resolution at low powers. The uncalibrated, 3-slope encoded value of Rx Power is read from the **rxpower_uncal** register.

RSSI CURRENT RANGE (µA)			**rxpower_uncal**
GAIN x1	**GAIN x1.5**	**GAIN x2**	
0 to 16	0 to 11	0 to 8	0 to 32
16 to 208	11 to 139	8 to 104	32 to 128
208 to 1232	139 to 821	104 to 616	128 to 255

Adjust the Rx Power sampling bandwidth using **rxpower_bandwidth**.

Digital Diagnostic Monitors

The raw digital measures of: temperature, supply voltage, bias current, Tx Power, and Rx power are converted into calibrated SFF-8472 Digital Diagnostic Monitor (DDM) values once every 10ms when sff_en is set and the main loop is active (mainloop_en is set). These registers are located in main_config. The following calibration constants are used:

METRIC	REFERENCE	SLOPE (SLA: A4h)	OFFSET (SLA: A4h)	DDM (SLA: A2h)
Temperature	temp	00h–01h	02h–03h	60h–61h
Supply Voltage	vcc	04h–05h	06h–07h	62h–63h
Tx Bias Current	bias	08h–09h	0Ah–0Bh	64h–65h
Tx Power	txpower	0Ch–0Dh	0Eh–0Fh	66h–67h
Rx Power	rxpower	10h–11h (slope 0) 14h–15h (slope 1)	12h–13h (offset 0) 16h–17h (offset 1)	68h–69h

All slope values (including Rx power) are stored as 16-bit fixed point (unsigned) as per SFF-8472 external calibration constants. The slope is calculated as DDM LSB's per ADC increment, e.g. for supply voltage the slope unit (bit 8) represents units of 100µA per ADC increment (hence the >>8 operation after multiplication).

All offset values (including Rx power) are stored as 16-bit fixed point (signed two's complement) as per SFF-8472 external calibration constants. In all cases, the upper byte of the 16-bit word is stored at the lower address.

Rx power has an additional pair of constants to support a rough piecewise linear approximation of the nonlinear characteristic of received optical power vs. RSSI current. This occurs when a series resistor is used between the APD and the APD bias voltage generation circuit. It provides a form of compression, protecting the APD by reducing avalanche gain if current gets too high.

Temperature

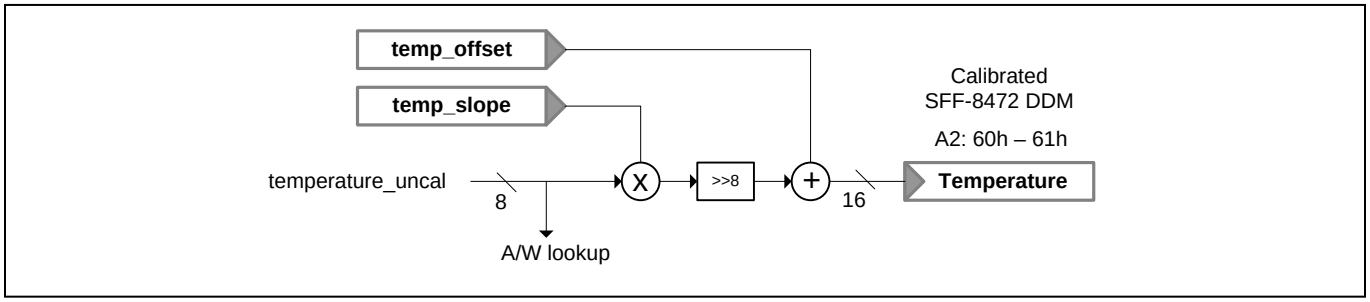


Figure 16. Calculating the Temperature DDM

Supply Voltage

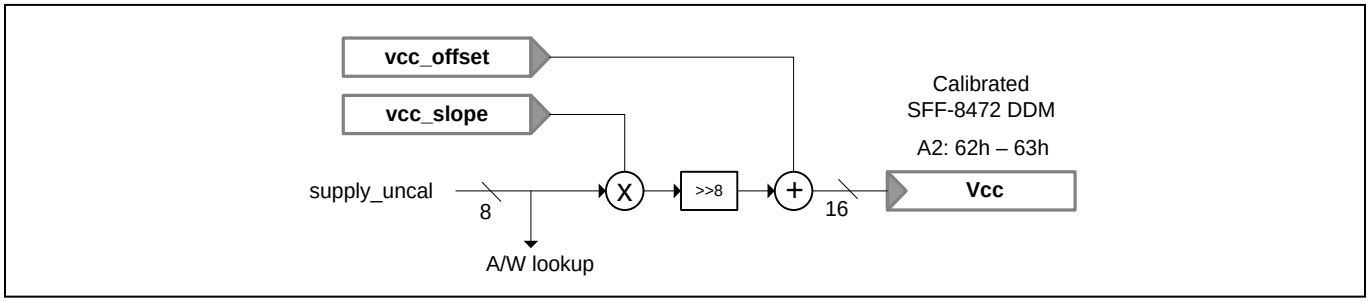


Figure 17. Calculating the Supply Voltage DDM

Tx Bias Current

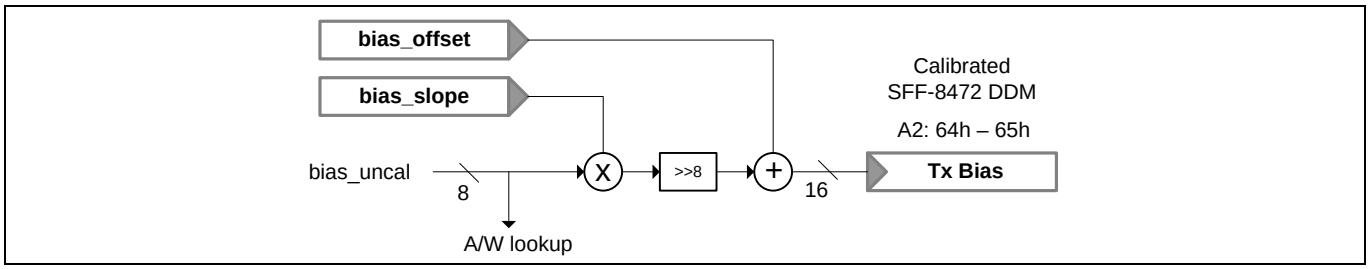


Figure 18. Calculating the Bias Current DDM

Tx Power

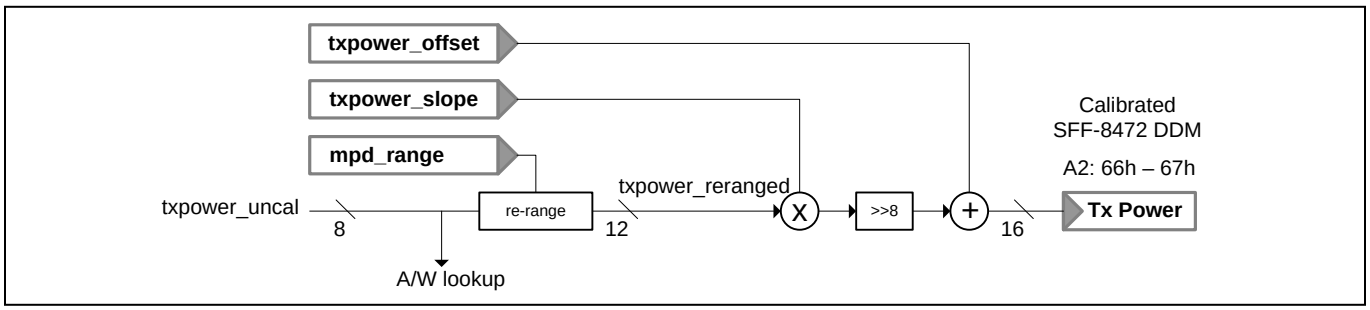


Figure 19. Calculating the Tx Power DDM

The power monitor generates an 8-bit measure of MPD current after a gain of 1, 1/4, or 1/16 has been applied. Re-ranging increases the Tx Power value when gains < 1 have been applied to the MPD current.

txpower_reranged = txpower_uncal << 4 when **mpd_range** = '10' else
txpower_uncal << 2 when **mpd_range** = '01' else
txpower_uncal

Rx Power

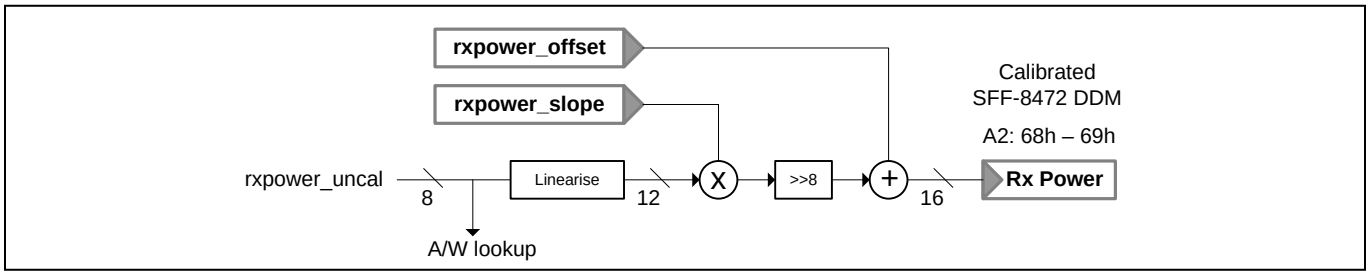


Figure 20. Calculating the Rx Power DDM

The following formulae are used to convert the 3-slope **rxpower_uncal** value into a linear pseudo 12-bit (0 to 2448) value:

0 < rxpower_uncal ≤ 32 linearized_rx_power = rxpower_uncal
32 ≤ rxpower_uncal ≤ 128 linearized_rx_power = ((rxpower_uncal – 32) x 4) + 32
128 ≤ rxpower_uncal ≤ 255 linearized_rx_power = ((rxpower_uncal – 128) x16) + 416

The selected pair of slope and offset values depend on the value of **linearized_rx_power**. If **linearized_rx_power** is greater than **rxpower_threshold,** then use the slope and offset pair from the address range 14h to 17h. Otherwise use the slope and offset pair from address range 10h to 13h. This coarsely accommodates the nonlinearity of the curve of received optical power vs. RSSI current.

Alarm and Warning Flags

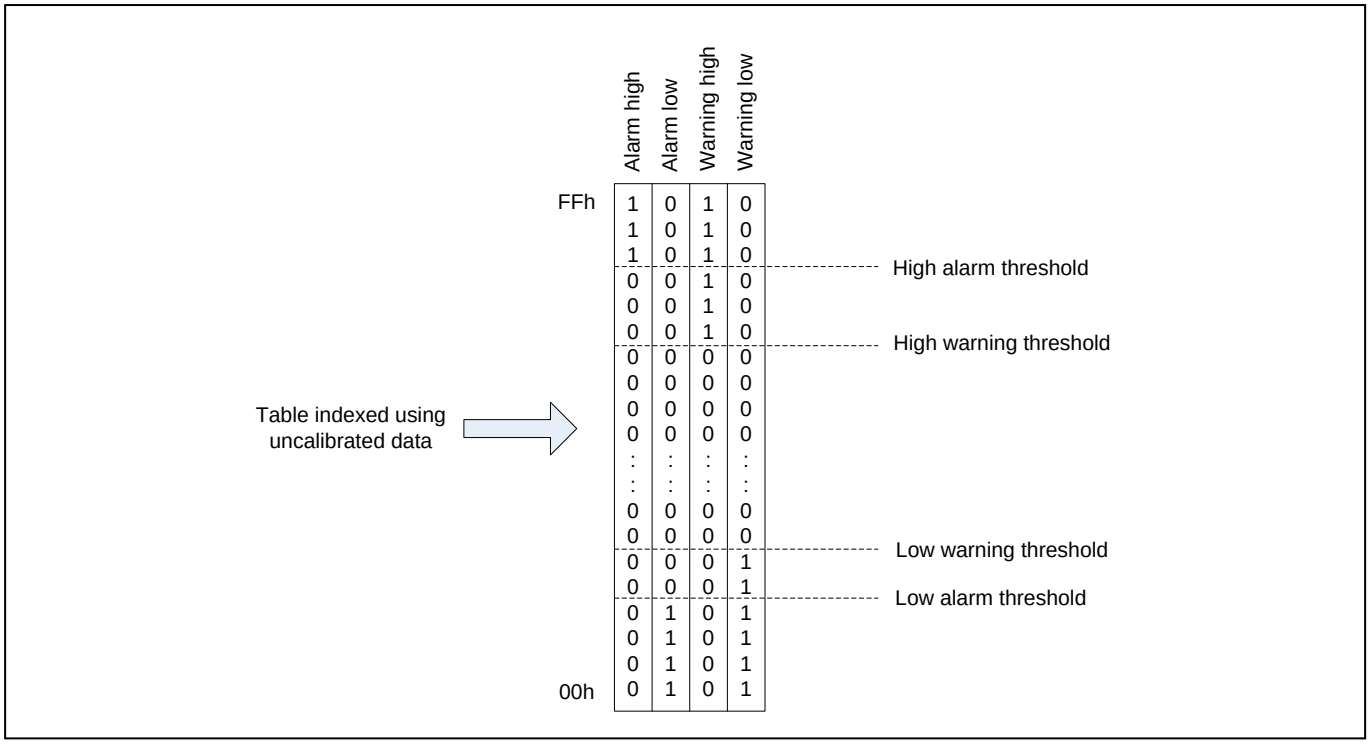


Figure 21. Using 8-Bit Calibrated Data to Look Up Alarm and Warning Flags

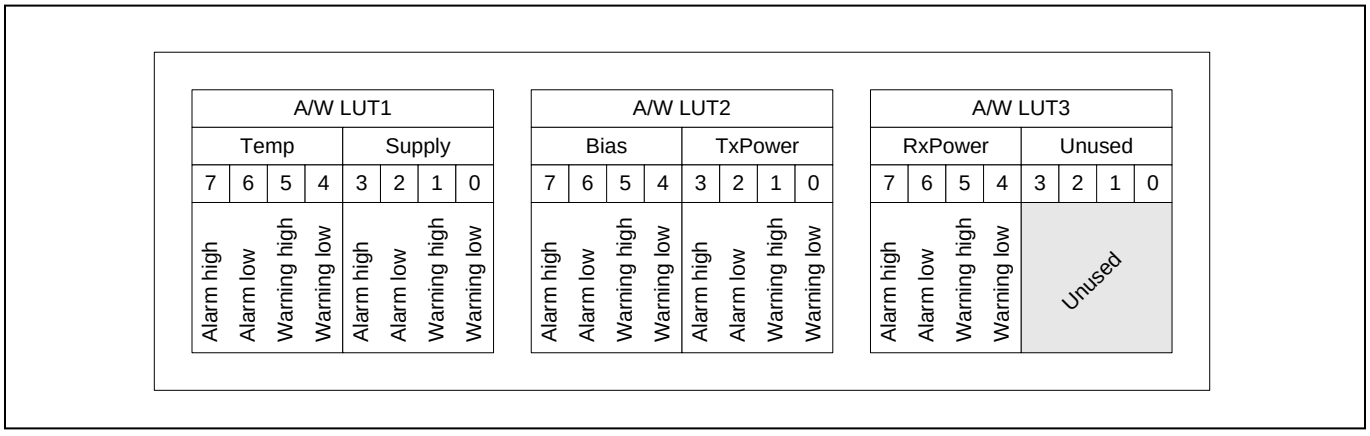


Figure 22. Alarm and Warning LUT Mapping

The uncalibrated 8-bit diagnostic data values are used to index the alarm and warning LUTs. Construct a LUT by identifying the required threshold levels in absolute units (V, C, mA, µW) and then reverse the calculations shown by the figures in the previous section to yield corresponding uncalibrated threshold levels. For Tx and Rx power, these should incorporate the range and 3-slope encoding, respectively.

The **ls_alarmflag_en** register controls which of the DDM alarm flags contribute to the laser safety alarm_fault fault condition.

Power-Up and Sleep Mode

[Control Register Address Range A4h:8Ch, B8h]

The MAX24001 can be put into a low-power mode of operation when the SLEEP pin is asserted. This is achieved by combining the sleep function with the chip-power sequencing, SLEEP can be configured to independently affect the Rx and Tx signal paths.

Rx Signal path: The response to the SLEEP pin is controlled by the **rx_respond_to_sleeppin** register.

Tx Signal path: The response to the SLEEP pin is controlled by the **tx_respond_to_sleeppin** register.

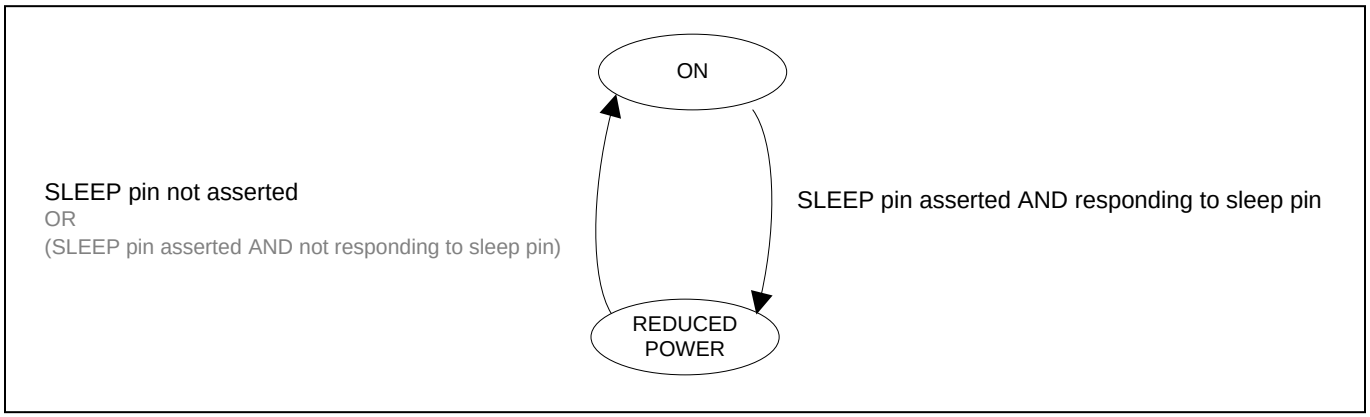


Figure 23. Conditions for Moving In and Out of Sleep Mode

The device will only move between these states when power sequencing is enabled (**tx_powerup_en** and **rx_powerup_en** are set).

The host can alternatively put the MAX24001 to sleep using the **tx_force_sleep** and **rx_force_sleep** registers.

Initialization and Control

Overview

The MAX24001 is normally used in conjunction with a 2k byte EEPROM.

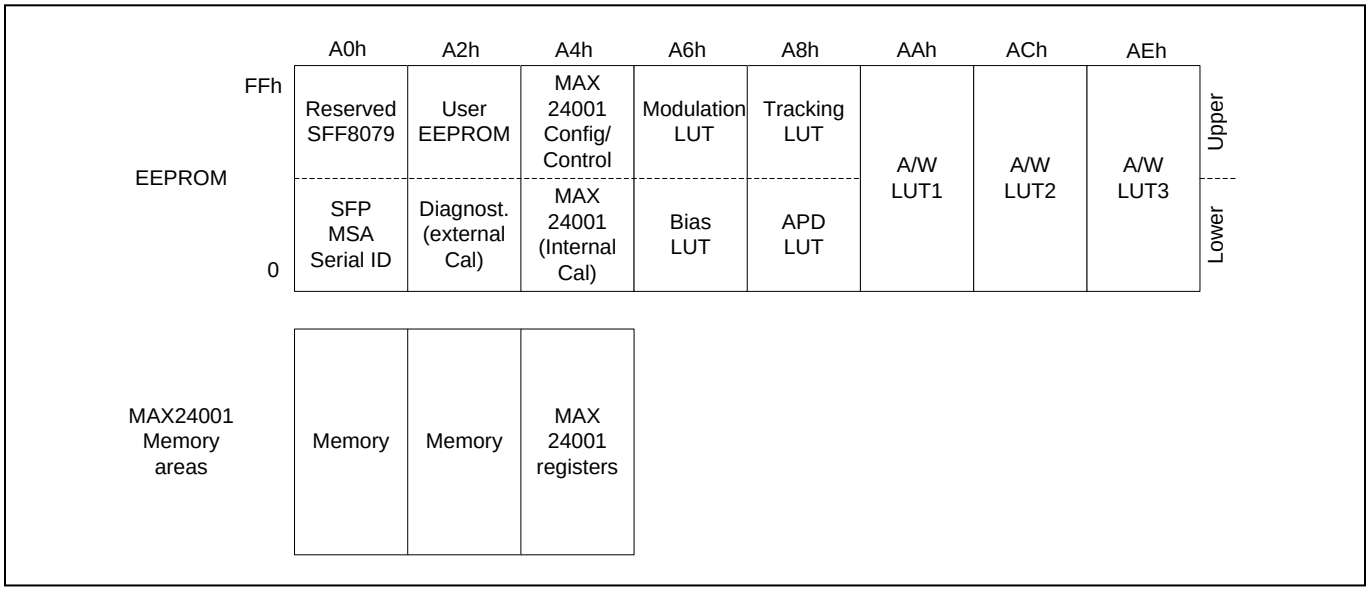


Figure 24. Address Map

Normal Operation

During initialization, data is transferred from EEPROM areas with TWI slave addresses A0h and A2h into shadow areas of memory on the MAX24001. Device configuration data is transferred from area A4h into MAX24001 registers.

During normal operation, the MAX24001 has exclusive access to the lookup tables held in EEPROM using the TWI master interface. The MAX24001 TWI slave interface only decodes slave addresses A0h and A2h, and when the host accesses these areas it is accessing the shadowed memory on the MAX24001. The diagnostic data in the memory is regularly refreshed.

Using a Microcontroller

If the initialization fails, then the MAX24001 defaults to a state whereby the Tx and Rx paths are not enabled, the main loop is off, and all memory areas are accessible. A microcontroller may then upload data to registers and control the operation of the MAX24001.

Module Setup

To access EEPROM (cf **initialisation_status** and **system_control** registers)

- Clear **mainloop_en**. This stops the main loop.
- Wait until **eeprom_dma_idle** is set. Accesses to EEPROM have then ceased.
- Set **external_access** to direct accesses via the TWI slave interface to EEPROM.

All regions of the EEPROM may then be accessed as long as the chip is in security level 2.

Access Control

[Control register address range A2h: 7Ch to 7Fh, and A4h: 82h to 8Bh]

Three levels of security are defined. The security level determines which areas of EEPROM and register space may be accessed via the two-wire interface. The security level is selected by the **password_entry** register and can be read from the **security_level** register in **system_status**.

Level2 – (**password_entry** value matches **password2**). The host has full read and write access to all address spaces. (password2 has priority over password1).

Level1 – (**password_entry** value matches **password1**). The host has read and write access to A0h and A2h only, as defined by the upper nibbles of the **password_configA0** and **password_configA2** registers.

Level0 – (**password_entry** value matches neither **password1** nor **password2**). The host has read and write access to A0h and A2h only, as defined by the lower nibbles of the **password_configA0** and **password_configA2** registers.

Password1 and **password2** can only be written in level2. The security level will not change when writing a new value to **password2**. Typically access in level 0 is more restrictive than access in level1. Read and write access to A2h:78h to 7Fh is always permitted. If access is denied then the transaction is discarded in the case of a write, and returns FFh in the case of a read. During burst-mode accesses, access permission and destination are tested on a byte-by-byte basis.

Initialization Sequence

[Control register addresses A4h: 80h, 81h, 8Ch, E0h]

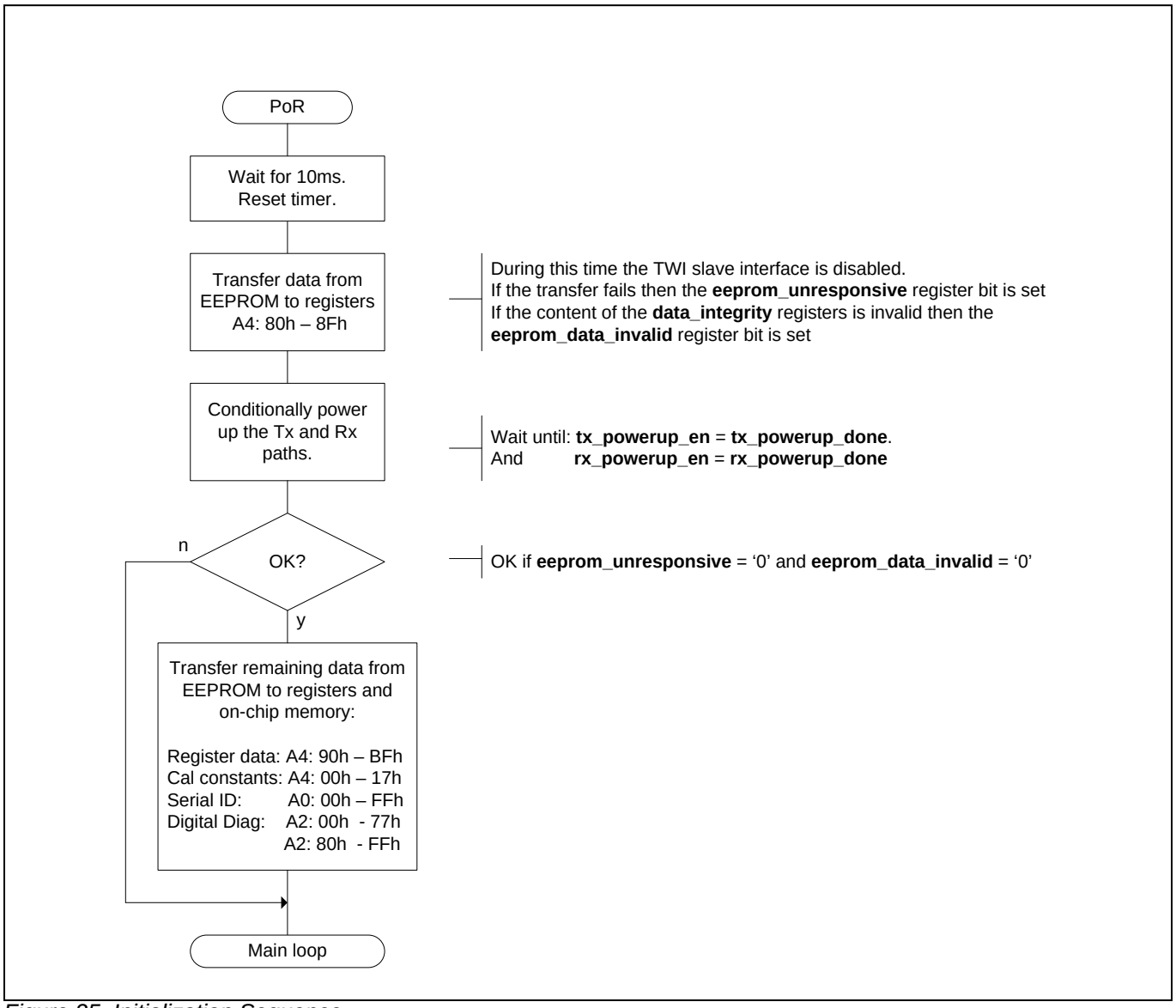


Figure 25. Initialization Sequence

The data integrity bytes are the first two bytes to be read from EEPROM (addresses A4: 80h to 81h). If **data_integrity0** = C3h and **data_integrity1** = 5Ah then it is inferred that the EEPROM is correctly programmed and initialization continues.

If the read access fails (no EEPROM) then **eeprom_unresponsive** is set. If the read access succeeds but the data integrity values are incorrect then **eeprom_data_invalid** is set. In both cases the transfer from EEPROM is aborted to prevent MAX24001 defaults from being overwritten with random data. The Tx and Rx paths will not power up and the MAX24001 will remain in the wait state at the start of the main loop.

The data integrity values only exist in EEPROM. They have no corresponding registers.

Main Operating Loop

[Control register address A4h: B7h]

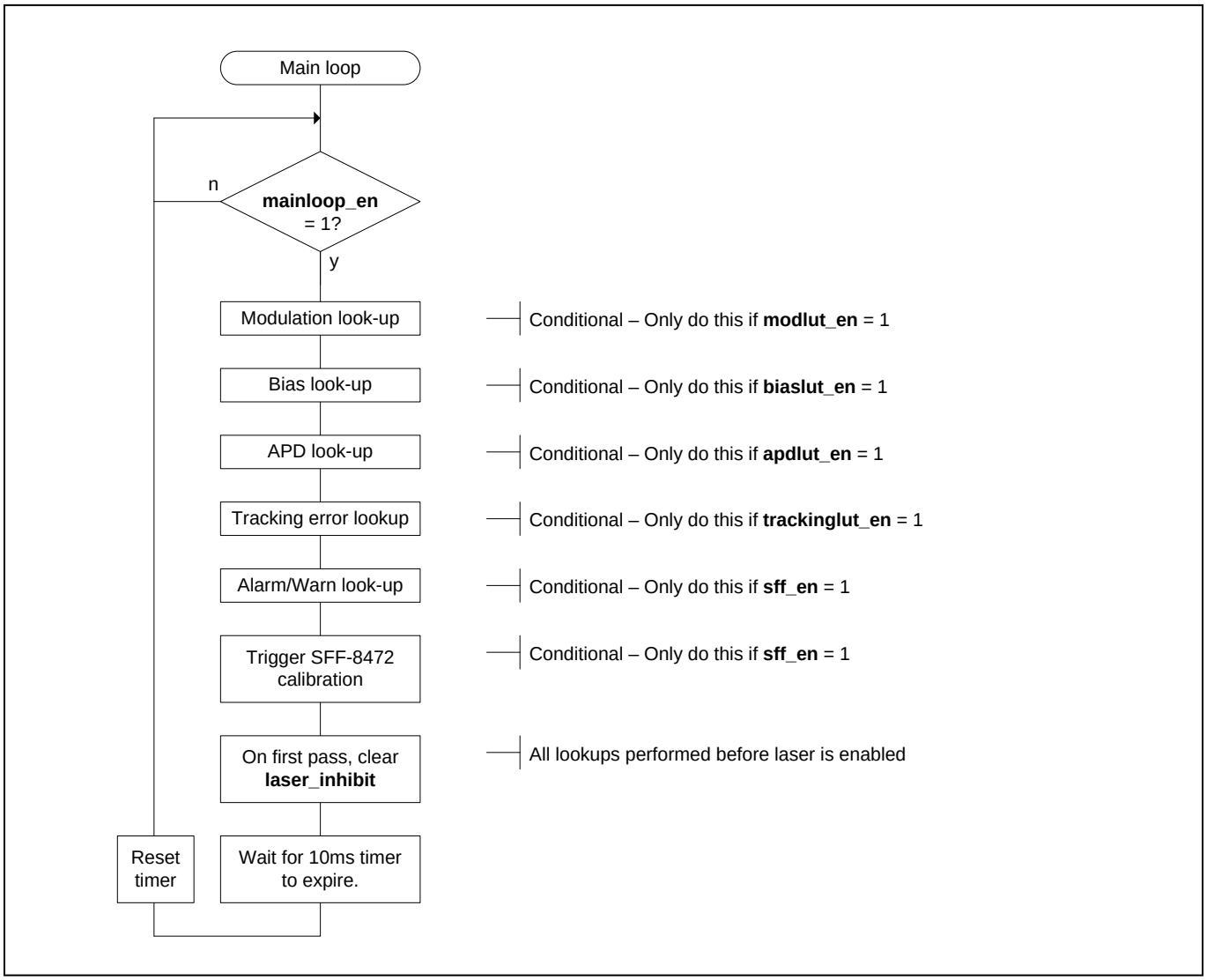


Figure 26. Main Operating Loop

The modulation, bias, APD, and tracking error LUTs are all 128 bytes and indexed by the upper 7 bits of the uncalibrated temperature sensor output (**temperature_uncal**). Typically, LUT entry 14h corresponds with a temperature of -40°C. LUT resolution is then 1.6°C between consecutive table entries. These values are approximate and may vary slightly from batch to batch.

Two-Wire Interface (TWI) Protocol

The SDA_SLAVE and SCL_SLAVE pins are referred to as the slave two-wire interface (slave TWI). The slave TWI provides external access to both registers within the MAX24001 and to any device connected to the SCL_MASTER and SDA_MASTER pins (the master TWI). Typically, an EEPROM is connected to the master TWI.

Framing and Data Transfer

The two-wire interface comprises a clock line (SCL) and a data line (SDA).

An individual transaction is framed by a START condition and a STOP condition. A START condition occurs when a bus master pulls SDA low while SCL is high. A STOP condition occurs when the bus master allows SDA to transition low-to-high when SCL is high. Within the frame the master has exclusive control of the bus. The MAX24001 supports Repeated START conditions whereby the master may simultaneously end one frame and start another without releasing the bus by replacing the STOP condition with a START condition.

Within a frame the state of SDA only changes when SCL is low. A data bit is transferred on a low-to-high transition of SCL. Data is arranged in packets of 9 bits. The first 8 bits represent data to be transferred (most significant bit first). The last bit is an acknowledge bit. The recipient of the data holds SDA low during the ninth clock cycle of a data packet to acknowledge (ACK) the byte. Leaving SDA to be pulled high on the ninth bit signals a not-acknowledged (NACK) condition. The interpretation of the acknowledge bit by the sender depends on the type of transaction and the nature of the byte being received. SDA is bidirectional so that the master may send data bytes during write transactions and the slave may send data bytes during reads.

Device Addressing

The first byte to be sent after a START condition is a slave address byte. The first seven bits of the byte contain the target slave address (MSB first). The eighth bit indicates the transaction type – ‘0’ = write, ‘1’ = read. Each slave interface on the bus is assigned a 7-bit slave address. If no slave matches the address broadcast by the master then SDA will be left to be pulled high during the acknowledge bit and the master receives a NACK. The master must then assert a STOP condition. If a slave identifies the address then it acknowledges it by pulling SDA low. The master then proceeds with the transaction identified by the type bit.

The two-wire interface of the MAX24001 decodes slave addresses A0h to AFh.

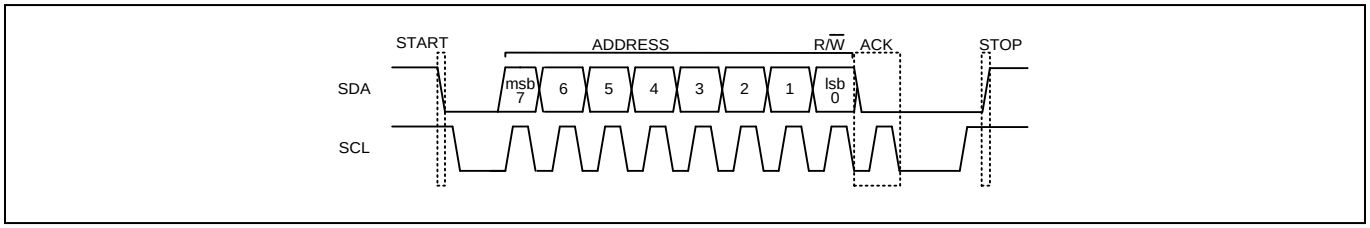


Figure 27. Address Decoding Example

Write Transaction

Figure 28 shows an example of a write transaction. The address byte is successfully acknowledged by the slave, and the type bit is set low to signify a write transaction. After the first acknowledge the master sends a single data byte. All signalling is controlled by the master except for the SDA line during the acknowledge bits. During the acknowledge cycle the direction of the SDA line is reversed and the slave pulls SDA low to return a ‘0’ (ACK) to the master.

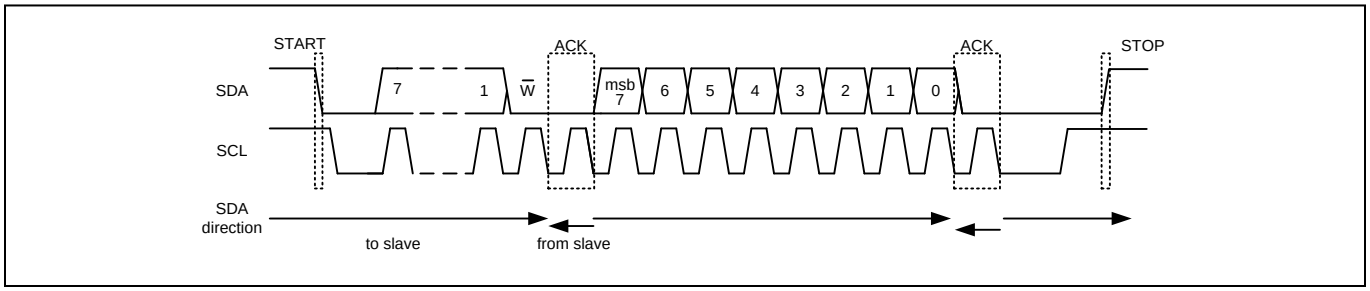


Figure 25. Write Transaction

The MAX24001 interprets the first data byte as a register address. This is used to set an internal memory pointer. Subsequent data bytes within the same transaction will then be written to the memory location addressed by the pointer. The pointer is autoincremented after each byte. There is no limit to the number of bytes which may be written in a single burst to the internal registers of the MAX24001.

Read Transaction

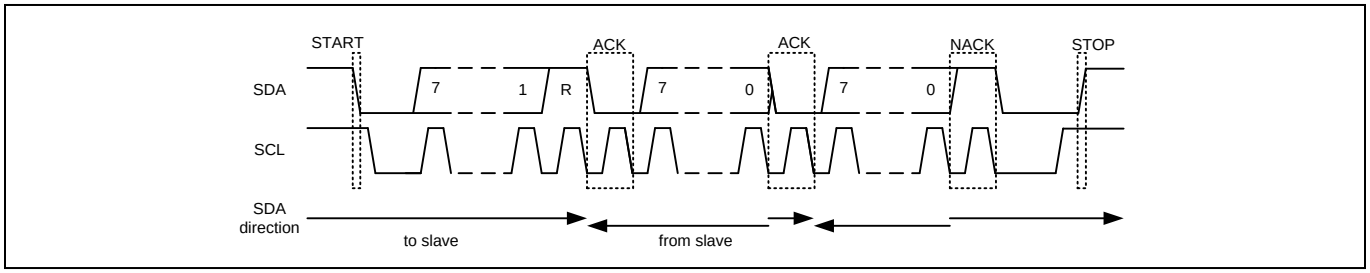


Figure 26. Read Transaction

Figure 29 shows an example of a 2-byte read transaction. The slave address byte is successfully acknowledged by the slave, and the type bit is set high to signify a read. After the ACK the slave returns a byte from the location identified by the internal memory pointer. This pointer is then auto-incremented. The slave then releases SDA so that the master can ACK the byte. If the slave receives an ACK then it will send another byte. The master identifies the last byte by sending a NACK to the slave. The master then issues a STOP to terminate the transaction.

Thus, to implement a random access read transaction, a write must first be issued by the master containing a slave address byte and a single data byte (the register address) as shown in Figure 28. This sets up the memory pointer. A read is then sent to retrieve data from this address (see Figure 29).

Register Descriptions

For registers containing a single 8-bit field, the MSB of the field is stored in bit 7 of the register byte. Note that 'reserved' register bits are specified as read only. These registers should not be changed from their power-on reset (POR) default settings. Register types are:

R Bit is read only via the slave TWI. Writing to this bit will have no effect. The value may be changed by the MAX24001 to communicate operating status to the host.

R/W Bit is readable and writable via the slave TWI. The value will not be changed by the device itself except under a device reset.

E Event bit. This bit is set to '1' by the MAX24001 when a specified event occurs. It is only cleared to '0' when the host writes '1' to it via the slave TWI. Writing a zero to this register has no effect. This bit is also readable.

Slave Address: A2h

6Eh	**status_control**			Status and control information (cf. sff-8472 specification)
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	tx_disable_state	R/W	0	State of the TX_DISABLE pin
6	soft_tx_disable	R/W	0	1: Disable the laser
5	—	—	—	—
4	p_down_status	R	—	State of the SLEEP pin
3	P_down_control	R/W	0	1: Assert SLEEP
2	tx_fault_state	R	—	State of the TX_FAULT pin
1	rx_los_state	R	—	State of the LOS/SD pin
0	data_ready_bar	R	1	Changes to '0' when the transceiver is powered up and data is ready

7Ah	**system_status**			Additional vendor specific status made available to the user irrespective of security level
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	—	—	—	—
6	rogue_onu	E	0	1: Rogue_onu condition is detected
5	excessive_bias	R	0	1: Bias DAC exceeds tx_bias_threshold
4	eeprom_dma_idle	R	0	1: EEPROM is idle and may be accessed
3	eeprom_data_invalid	R	0	1: Data integrity check failed during initialization
2	eeprom_unresponsive	R	0	1: EEPROM failed to ACK the slave address during initialization
1–0	security_level	R	10	00h = level0, 01h = level1, 10h = level2

7Bh	system_control			Additional vendor specific control bits made available to the user irrespective of security level
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–6	—	—	—	Undefined
5-4	power_levelling	R/W	00	GPON power levelling: 00: x1, 01: x0.5, 1x: x0.25
3	soft_rate_select	R/W	0	0: **ratesel0** control rx filter, 1: **ratesel1** controls rx filter
2	tx_force_sleep	R/W	0	1: Force Tx system into low-power SLEEP mode (if **respond_to_sleep** pin set)
1	rx_force_sleep	R/W	0	1: Force Rx system into low-power SLEEP mode
0	external_access	R/W	0	Host access routing: 1: EEPROM, 0: internal registers/memory

7Ch	**password_entry0**	R/W	00h	Write to this register to select the security level. Level 2 if **password_entry** = password2 else Level 1 if **password_entry** = password1 else Level 0
7Dh	**password_entry1**	R/W	00h	
7Eh	**password_entry2**	R/W	00h	
7Fh	**password_entry3**	R/W	00h	

Slave Address: A4h

82h	**password1_0**	R/W	00h	Holds the security level 1 password.
83h	**password1_1**	R/W	00h	
84h	**password1_2**	R/W	00h	
85h	**password1_3**	R/W	00h	

86h	**password2_0**	R/W	00h	Holds the security level 2 password
87h	**password2_1**	R/W	00h	
88h	**password2_2**	R/W	00h	
89h	**password2_3**	R/W	00h	

8Ah	password_configA0			Enables the access to the upper and lower halves of the A0h address space to be configured for security levels 0 and 1
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	level1_write_upper	R/W	1	1: Write access to upper half of A0h permitted in security level 1
6	level1_read_upper	R/W	1	1: Read access to upper half of A0h permitted in security level 1
5	level1_write_lower	R/W	1	1: Write access to lower half of A0h permitted in security level 1
4	level1_read_lower	R/W	1	1: Read access to lower half of A0h permitted in security level 1
3	level0_write_upper	R/W	0	1: Write access to upper half of A0h permitted in security level 0
2	level0_read_upper	R/W	0	1: Read access to upper half of A0h permitted in security level 0
1	level0_write_lower	R/W	0	1: Write access to lower half of A0h permitted in security level 0
0	level0_read_lower	R/W	1	1: Read access to lower half of A0h permitted in security level 0

8Bh	password_configA2			Enables the access to the upper and lower halves of the A2h address space to be configured for security levels 0 and 1
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	level1_write_upper	R/W	1	1: Write access to upper half of A2h permitted in security level 1
6	level1_read_upper	R/W	1	1: Read access to upper half of A2h permitted in security level 1
5	level1_write_lower	R/W	1	1: Write access to lower half of A2h permitted in security level 1
4	level1_read_lower	R/W	1	1: Read access to lower half of A2h permitted in security level 1
3	level0_write_upper	R/W	0	1: Write access to upper half of A2h permitted in security level 0
2	level0_read_upper	R/W	0	1: Read access to upper half of A2h permitted in security level 0
1	level0_write_lower	R/W	0	1: Write access to lower half of A2h permitted in security level 0
0	level0_read_lower	R/W	1	1: Read access to lower half of A2h permitted in security level 0

8Ch	initialization_config			Early stage chip configuration at the start of the initialisation process
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	—	—	—	Undefined
6	—	R/W	0	Reserved
5	tx_powerup_en	R/W	0	1: Enable automatic power-up sequencing for the Tx system
4	rx_powerup_en	R/W	0	1: Enable automatic power-up sequencing for the Rx system
3–0	—	R/W	0111	Reserved

90h	rx_input			Configures the input buffer of the receive path and sets the receiver bandwidth
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–4	rx_input_peak	R/W	0000	0000: no peaking, increasing to 1111 for maximum peaking
3–2	rx_ratesel1	R/W	11	Sets the receiver bandwidth: 00: 1.25Gbps 01: 2.488Gbps
1–0	rx_ratesel0	R/W	00	Register is selected by **soft_rate_select**.

92h	rx_output			Configures the output stage of the receive path
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	—	—	—	Undefined
6	los_squelch	R/W	1	1: Power down RX_OUT when LOS = 1
5	Squelch	R/W	0	1: Power down RX_OUT (but only if **los_squelch** = ‘0’)
4	rx_invert	R/W	0	1: Invert signal on RX_OUT
3–0	—	R/W	0000	Reserved

93h	rx_driver			Controls the output amplitude and pre emphasis on RX_OUT
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–6	—	—	—	Undefined
5–4	rx_preemphasis	R/W	00	Sets pre-emphasis ratio: 00: 0% 01: 2% 10: 6% 11: 10%
3–0	rx_output_swing	R/W	1010	Sets output voltage swing: 0000: 200mV$_{P-P}$ 1111: 880mV$_{P-P}$ Step size is 45mV

94h	rx_apd_control			Configuration of the APD system and specifically the APD_CTRL and DAC outputs
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–6	pwm_frequency	R/W	00	0: 250kHz, 1: 500kHz, 2: 1MHz, 3: 2MHz
5	pwm_invert	R/W	0	1: invert, 0: normal
4	high_v	R/W	0	APD_CTRL output, 0: open, 1: 3.3V driver
3	—	R/W	1	Reserved
2	target_lut_enable	R/W	0	1: Load the **rx_apd_target** register periodically from the APD LUT
1	pwm_lut_enable	R/W	0	1: Load the **rx_apdpwm** register periodically from the APD LUT
0	dac_lut_enable	R/W	0	1: Load the **rx_apddac** register periodically from the APD LUT

95h	rx_apd_pi			Gain values for APD proportional-integral controller
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–6	max_duty	R/W	00	Duty-cycle limit (maximum): 0: 207/256 1: 223/256 2: 239/256 3: 255/256
5–3	k_integral	R/W	000	Integral gain of PI controller (**rx_apdpwm** LSBs/LSB of error value). 0: 0 4: 2^{-5} 1: 2^{-8} 5: 2^{-4} 2: 2^{-7} 6: 2^{-3} 3: 2^{-6} 7: 2^{-2} The error value is the difference between the sampled APD voltage and the **rx_apd_target** value. Eg. If **k_integral** = 6 and error value = +2 then the **rx_apdpwm** register will be incremented by 2 x 2^{-3} = 0.25. (Note that the **rx_apdpwm** register is the integer part of a fixed point register with 8 additional bits of precision.)
2–0	k_proportional	R/W	000	Proportional gain of PI controller (**rx_apdpwm** LSBs / LSB of error value): 0: 0 4: 2^{3} 1: 2^{0} 5: 2^{4} 2: 2^{1} 6: 2^{5} 3: 2^{2} 7: 2^{6}

96h	rx_apd_v_threshold	TYPE	POR	While the APD voltage exceeds this threshold, APD_CTRL is three-stated. Note that a threshold of FFh amounts to turning off this feature.
		R/W	FFh	

97h	rx_apd_i_threshold	TYPE	POR	While the APD current exceeds this threshold, APD_CTRL is three-stated. Note that a threshold of FFh amounts to turning off this feature.
		R/W	FFh	

98h	rx_apddac	TYPE	POR	Sets the APD DAC output current from 0 to 500µA.
		R/W	00h	

99h	rx_apdpwm	TYPE	POR	Sets the PWM duty cycle in the range 0/256 to 255/256
		R/W	00h	

9Ah	rx_apd_target	TYPE	POR	Sets the target voltage of the APD controller.
		R/W	00h	

9Bh	los_rssi_config			Sets the los debounce period and LOS polarity. This register also contains bits used to control current on RSSI pin
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	—	—	—	Undefined
6–4	los_debounce	R/W	000	000 = 0µs 100 = 64µs 001 = 16µs 101 = 80µs 010 = 32µs 110 = 96µs 011 = 48µs 111 = 112µs
3–2	rx_rssi_scale	R/W	11	Sets gain applied to current flowing through RSSI pin. 00: x1 : RSSI current range 0 to 1275µA 01: x1.5: RSSI current range 0 to 850µA 10: x1.5: RSSI current range 0 to 850µA 11: x2: RSSI current range 0 to 638µA
1	rx_rssi_sink	R/W	1	1: Current flows into RSSI pin, 0: Current flows out of RSSI pin
0	—	—	—	—

9Ch	los_assert	TYPE	POR	Sets threshold at which LOS is asserted
		R/W	00h	

9Dh	los_deassert	TYPE	POR	Sets threshold at which LOS is deasserted
		R/W	FFh	

9Eh	tx_input			Configures the input circuitry of the transmit path. Pulse width of the transmitted signal is adjusted by moving the crossing point of the eye up or down.
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	burst_invert	R/W	0	1: Invert differential signal on BEN
6	tx_invert	R/W	0	1: Invert differential signal on TX_IN
5	—	—	—	Undefined
4	tx_pwadjust_hires	R/W	0	1: Reduce step size of pulse width adjust by half
3	tx_pwadjust_dir	R/W	0	0: Move crossing point of eye up, 1: Move crossing point down
2–0	tx_pwadjust_size	R/W	000	000: No adjustment, 111: Maximum adjustment. At maximum adjustment the zero-crossing point moved by 40% of 0-pk eye opening.

A0h	tx_output			This register is used for managing the quality of the output eye
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	modramp_en	R/W	1	1: DAC ramps from old value to new, 0: immediate step change
6–4	tx_snubber	R/W	000	Adjust this to improve rise time and pulse width distortion
3–0	—	R/W	0000	Reserved

A1h	tx_moddac	TYPE	POR	Sets the CML output current for the laser driver (modulation current)
		R/W	00h	

A2h	tx_bias			The mpd_gain register applies gain to the MPD current. It does not change during normal operation and therefore the range must be selected to accommodate all expected values of MPD current.
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	—	R/W	0	Reserved
6	—	—	—	Undefined
5–4	mpd_range	R/W	10	10: 400µA to 2000µA 01: 100µA to 800µA 00: 40µA to 200µA
3	biasramp_en	R/W	1	1: Bias DAC ramps from old to new, 0: Immediate step change
2–0	—	—	—	Undefined

A3h	tx_biasmode			
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	faststart_after_sleep	R/W	0	1: Trigger the fast-start algorithm when emerging from sleep mode
6	bias_lut_after_sleep	R/W	0	1: Do single bias LUT lookup when emerging from sleep mode
5	faststart_after_txdisable	R/W	0	1: Trigger the fast-start algorithm when tx_disable deasserted
4	bias_lut_after_txdisable	R/W	0	1: Do single bias LUT lookup when tx_disable deasserted
3	—	—	—	—
2	apc_enable	R/W	0	1: Closed-loop operation. 0 => open-loop operation
1	faststart_enable	R/W	0	1: Trigger the fast-start algorithm after power-on reset
0	bias_lut_enable	R/W	0	1: Do single bias LUT lookup after power-on reset (apc_enable = 1) 1: Periodic lookups (apc_enable = 0). 0: No lookups from bias LUT

A4h	tx_apc			The APC delay register controls the delay between the deassertion of laser shutdown and the activation of the APC loop counter. The APC loop gain sets the gain (and thus the bandwidth) of the APC control loop.
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–4	apc_delay	R/W	0000	0000: 0µs 0001: 128µs 0010: 256µs 0011: 384µs : 1110: 1792µs 1111: 1920µs
3–0	apc_loop_gain	R/W	1000	0000: 2^{-15} 0001: 2^{-14} 0010: 2^{-13} : 1101: 2^{-2} 1110: 2^{-1} 1111: 1

A5h	tx_apc_target	TYPE	POR	This is the MPD current target level for both the APC loop and the fast-start algorithm.
		R/W	00h	

A6h	tx_biasdac0	TYPE	POR	Bits 7-0 of the 10-bit value which controls the bias current. The default is non-zero so that there is sufficient current for the loop fault detect circuits to operate correctly.
		R/W	28h	

A7h	tx_biasdac1			
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–2	—	—	—	Undefined
1–0	tx_biasdac	R/W	00	Bits 9-8 of the 10-bit value which controls the bias current

A8h	tx_bias_threshold	TYPE	POR	If tx_biasdac<9-2> exceeds **tx_bias_threshold** then the excessive_bias bit is set in **system_status**.
		R/W	FFh	

A9h	tx_mon_bandwidth			Determines the bandwidth of the first order digital lowpass filter which is applied by the power monitoring circuit to the measured value of MPD current.
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–4	—	—	—	Undefined
3–0	mon_bandwidth	R/W	1000	0000: 311Hz 0001: 622Hz … 1000: 80kHz … 1110: 5.1MHz 1111: No filtering

AAh	tx_fstart_initial	TYPE	POR	Determines the initial step size of the fast-start algorithm.
		R/W	80h	

ABh	tx_fstart_decay			Determines the multiplication factor applied to the step size on each step of the fast-start algorithm after the MPD current first exceeds the target threshold.
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–2	fstart_decay	R/W	100101	100000: 32/64 = 0.5 100001: 33/64 = 0.516 100010: 34/64 = 0.531 100011: 35/64 = 0.547 100100: 36/64 = 0.563 100101: 37/64 = 0.5785 .. 101110: 46/64 = 0.719 101111: 47/64 = 0.734
1–0	—	—	—	Undefined

ACh	tx_fstart_duration			Determines the duration of the fast-start algorithm (an iteration is 4 cycles of the 64 MHz system clock) and whether the laser is shut down for one or two cycles afterwards while the modulation control circuits settle.
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	fstart_recovery_en	R/W	1	1: Briefly shut down bias and modulation after the fast-start algorithm
6	fstart_recovery_time	R/W	0	0: Shut down for single iteration, 1: Shut down for 2 iterations
5–0	fstart_duration	R/W	001111	The fast-start algorithm runs for a number of iterations specified by this register.

ADh	txsd_config			Configures the TX signal detect feature.
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–4	txsd_rogueonu_delay	R/W	0011	The delay (in 64MHz clock cycles) between the falling edge of BEN and the testing for rogue ONU.
3–2	txsd_threshold	R/W	00	MPD current level above which signal is detected during bursts and rogue ONU is detected during gaps. 00: 20µA 01: 40µA 10: 60µA 11: 80mA
1	—	—	—	Undefined
0	—	—	—	Undefined

AEh	txsd_deglitch_period	TYPE	POR	The approximate time between the loss of transmitted signal and the deassertion of TX_SD during a burst: 00h: 16ns to 31ns 01h: 31ns to 62ns 02h: 46ns to 92ns a: b to c b = (a + 1) x 15.625ns c = 2b
		R/W	02h	

AFh	ls_txfault_faulten			Enables the fault conditions associated with the tx_fault laser safety system
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	Alarm	R/W	1	1: Enable this fault condition for the tx_fault laser safety system
6	rogue_onu	R/W	1	1: Enable this fault condition for the tx_fault laser safety system
5	soft_tx_fault	R/W	1	1: Enable this fault condition for the tx_fault laser safety system
4	tx_disable	R/W	0	1: Enable this fault condition for the tx_fault laser safety system
3	Vdd	R/W	1	1: Enable this fault condition for the tx_fault laser safety system
2	Vref	R/W	1	1: Enable this fault condition for the tx_fault laser safety system
1	Apc	R/W	1	1: Enable this fault condition for the tx_fault laser safety system
0	Bias	R/W	1	1: Enable this fault condition for the tx_fault laser safety system

B0h	ls_txfault_latchen			Latches the fault conditions associated with the tx_fault laser safety system
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	Alarm	R/W	1	1: Enable latching for this fault condition
6	rogue_onu	R/W	1	1: Enable latching for this fault condition
5	soft_tx_fault	R/W	0	1: Enable latching for this fault condition
4	tx_disable	R/W	0	1: Enable latching for this fault condition
3	Vdd	R/W	1	1: Enable latching for this fault condition
2	Vref	R/W	1	1: Enable latching for this fault condition
1	Apc	R/W	1	1: Enable latching for this fault condition
0	Bias	R/W	1	1: Enable latching for this fault condition

B1h	ls_shutdown_faulten			Enables the fault conditions associated with the shutdown laser safety system
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	Alarm	R/W	1	1: Enable this fault condition for the shutdown laser safety system
6	rogue_onu	R/W	1	1: Enable this fault condition for the shutdown laser safety system
5	soft_tx_fault	R/W	0	1: Enable this fault condition for the shutdown laser safety system
4	tx_disable	R/W	1	1: Enable this fault condition for the shutdown laser safety system
3	Vdd	R/W	1	1: Enable this fault condition for the shutdown laser safety system
2	Vref	R/W	1	1: Enable this fault condition for the shutdown laser safety system
1	Apc	R/W	1	1: Enable this fault condition for the shutdown laser safety system
0	Bias	R/W	1	1: Enable this fault condition for the shutdown laser safety system

B2h	ls_shutdown_latchen			Latches the fault conditions associated with the shutdown laser safety system
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	Alarm	R/W	1	1: Enable latching for this fault condition
6	rogue_onu	R/W	1	1: Enable latching for this fault condition
5	soft_tx_fault	R/W	0	1: Enable latching for this fault condition
4	tx_disable	R/W	0	1: Enable latching for this fault condition
3	Vdd	R/W	1	1: Enable latching for this fault condition
2	Vref	R/W	1	1: Enable latching for this fault condition
1	Apc	R/W	1	1: Enable latching for this fault condition
0	Bias	R/W	1	1: Enable latching for this fault condition

B3h	ls_alarmflag_en			Controls which of the DDM alarm flags contribute to the laser safety alarm_fault fault condition.
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	temp_hifault_en	R/W	0	1: Alarm fault occurs when temp exceeds high temp threshold
6	temp_lofault_en	R/W	0	1: Alarm fault occurs when temp below low temp threshold
5	supply_hifault_en	R/W	0	1: Alarm fault occurs when supply exceeds high supply threshold
4	supply_lofault_en	R/W	0	1: Alarm fault occurs when supply below low supply threshold
3	bias_hifault_en	R/W	0	1: Alarm fault occurs when bias exceeds high bias threshold
2	bias_lofault_en	R/W	0	1: Alarm fault occurs when bias below low bias threshold
1	txpower_hifault_en	R/W	0	1: Alarm fault occurs when txpower exceeds high txpower threshold
0	txpower_lofault_en	R/W	0	1: Alarm fault occurs when txpower below low txpower threshold

B4h	adc_filter			The samples of supply and rxpower may be lowpass filtered using a filter with programmable bandwidth. 00: fs/(2 x pi x 64) = 0.25Hz 01: fs/(2 x pi x32) = 0.5Hz 10: fs/(2 x pi x16) = 1Hz 11: fs/(2 x pi x 8) = 2Hz f_S = 100Hz based on measurements every 10ms.
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–6	—	—	—	Undefined
5–4	rxpower_bandwidth	R/W	00	Selects rxpower filter bandwidth
3–2	supply_bandwidth	R/W	00	Selects supply filter bandwidth
1–0	—	—	—	Undefined

B5h	adc_config			Configure the ADC
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–6	—	—	—	Undefined
5–4	adc_supplysel	R/W	00	00: V_{DD_TX} 10: V_{DD_RX} 01: V_{DD_TXO} 11: V_{DD_RXO}
3–0	—	—	—	Undefined

B6h	temp_config			Configures the temperature sensor
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	temp_ext_sensor	R/W	0	1: Use external sensor, 0: Use internal sensor
6	—	R/W	11	Reserved
5	leave_PU	R/W	1	0: Enable **tempsense_pu**
4–0	—	—	—	Undefined

B7h	main_config			Selects the operations performed when the main loop is enabled. Operations are performed once per iteration of the loop.
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	biaslut_en	R/W	1	1: Load **tx_biasdac** register form the bias LUT
6	sff_en	R/W	1	1: Recalculate sff-8472 DDMs
5	—	—	—	Undefined
4	trackinglut_en	R/W	1	Power monitor uses values from the tracking LUT
3	apdlut_en	R/W	1	1: Load the **rx_apddac**, **rx_apdpwm** or **rx_apd_target** register from the APD LUT
2	modlut_en	R/W	1	1: Load the **tx_moddac** register from the modulation LUT
1	—	—	—	Undefined
0	mainloop_en	R/W	0	1: Enable the main loop

B8h	sleep_config			Configures Sleep mode
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–6	—	—	—	Undefined
5	—	—	—	Reserved
4	rx_respond_to_sleeppin	R/W	0	1: Power down Rx when SLEEP pin asserted, 0: Ignore SLEEP pin
3–2	—	—	—	Undefined
1	—	—	—	Reserved
0	tx_respond_to_sleeppin	R/W	0	1: Power down Tx when SLEEP pin asserted, 0: Ignore SLEEP pin

B9h	temp_calibrate			Used during calibration of temperature sensor
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–6	—	—	—	Undefined
5–0	temp_calibrate	R/W	011111	Calibration trim register

BAh	rx_power_threshold	TYPE	POR	The threshold that defines which pair of Rx Power calibration constants is used. If the 3-slope encoded sample of rx power is above this threshold then select **rxpower_slope1** and **rxpower_offset1**. Otherwise select **rxpower_slope0** and **rxpower_offset0**.
		R/W	FFh	

BEh	pin_config0			Pin function and polarity configuration
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	—	—	—	Undefined
6	dac_select	R/W	1	1: DAC pin 39, 0: TX_FAULT pin 39
5	txsd_select	R/W	0	1: TX_SD pin 21, 0: TX_FAULT pin 21
4	txfault_invert	R/W	0	1: Invert the signal to TX_FAULT pin, 0: No inversion
3	los_invert	R/W	0	1: LOS pin = 1 when signal detected and LOS pin = 0 when no signal 0: LOS pin = 1 when no signal detected and LOS = 0 when signal
2	—	R/W	0	Reserved
1	—	R/W	0	Reserved
0	tx_disable_invert	R/W	0	1: Signal from TX_DISABLE pin is inverted, 0: No inversion

BFh	pin_config1			Masks outputs which should remain quiet during initialization
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–4	—	—	—	Undefined
3	apd_inhibit	R/W	1	1: APD_CTRL disabled (= Hi-Z), 0: Normal function
2	txsd_allow	R/W	0	0: TX_SD disabled (= 1), 1: Normal function
1	los_inhibit	R/W	1	1: LOS disabled (= 1), 0: Normal function
0	laser_inhibit	R/W	1	1: TX_OUT and BIAS are shutdown, 0: Normal function

C0h	software_faults			This register is used to set fault conditions via the TWI
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–1	—	—	—	Undefined
0	soft_tx_fault	R/W	0	1: Asserts the soft_tx_fault laser safety fault condition

C1h	temp_control			Configures the temperature sensor
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–6	—	—	—	Undefined
5	tempsense_pu	R/W	1	0: temperature sensor powers down between reads
4–0	—	—	—	Undefined

E0h	initialization_status			Reports status associated with device initialization
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	—	E	0	Reserved
6	—	—	—	Undefined
5	eeprom_dma_idle	R	0	1: EEPROM is idle and may be accessed
4	—	R	1	Reserved
3	tx_powerup_done	R	0	1: Tx path power up during initialization is complete
2	rx_powerup_done	R	0	1: Rx path power up during initialization is complete
1	eeprom_data_invalids	R	0	1: Data integrity check failed during initialization
0	eeprom_unresponsive	R	0	1: EEPROM failed to ACK the slave address during initialization

E1h	ls_fault_status			Reports real time status of fault conditions at input to the laser safety system
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	Alarm	R	—	1: Fault condition currently exists
6	rogue_onu	R	—	1: Fault condition currently exists
5	soft_tx_fault	R	—	1: Fault condition currently exists
4	tx_disable	R	—	1: Fault condition currently exists
3	Vdd	R	—	1: Fault condition currently exists
2	Vref	R	—	1: Fault condition currently exists
1	Apc	R	—	1: Fault condition currently exists
0	Bias	R	—	1: Fault condition currently exists

E2h	ls_fault_events			Records when the fault conditions at the input to the laser safety system have been asserted. Write ‘1’ to these bits to clear back to ‘0’
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7	Alarm	E	—	1: Fault condition has occurred
6	rogue_onu	E	—	1: Fault condition has occurred
5	soft_tx_fault	E	—	1: Fault condition has occurred
4	tx_disable	E	—	1: Fault condition has occurred
3	Vdd	E	—	1: Fault condition has occurred
2	Vref	E	—	1: Fault condition has occurred
1	Apc	E	—	1: Fault condition has occurred
0	Bias	E	—	1: Fault condition has occurred

E4h	hardware_status			Reports the real-time status of selected digital pins
BIT	**FIELD NAME**	**TYPE**	**POR**	**DESCRIPTION**
7–5	—	—	—	Undefined
4	txsd_pin	R	—	Indicates the status of the TXSD pin
3	tx_fault_pin	R	—	Indicates the status of the TX_FAULT pin
2	Shutdown	R	—	Indicates the status of the internal shutdown signal
1	sleep_pin	R	—	Indicates the status of the SLEEP pin
0	tx_disable_pin	R	—	Indicates the status of the TX_DISABLE pin

E6h	temperature_uncal	TYPE	POR	The temperature sample value before calibration
		R	—	

E7h	**supply_uncal**	**TYPE**	**POR**	The supply sample value before calibration
		R	—	

E8h	**bias_uncal**	**TYPE**	**POR**	The bias sample value before calibration
		R	—	

E9h	**txpower_uncal**	**TYPE**	**POR**	The tx_power value before re-ranging and calibration
		R	—	

EAh	**rxpower_uncal**	**TYPE**	**POR**	The rxpower sample value before calibration
		R	—	

EBh	**apdadc_uncal**	**TYPE**	**POR**	The uncalibrated measure of APD voltage
		R	—	

Simplified Interface Models

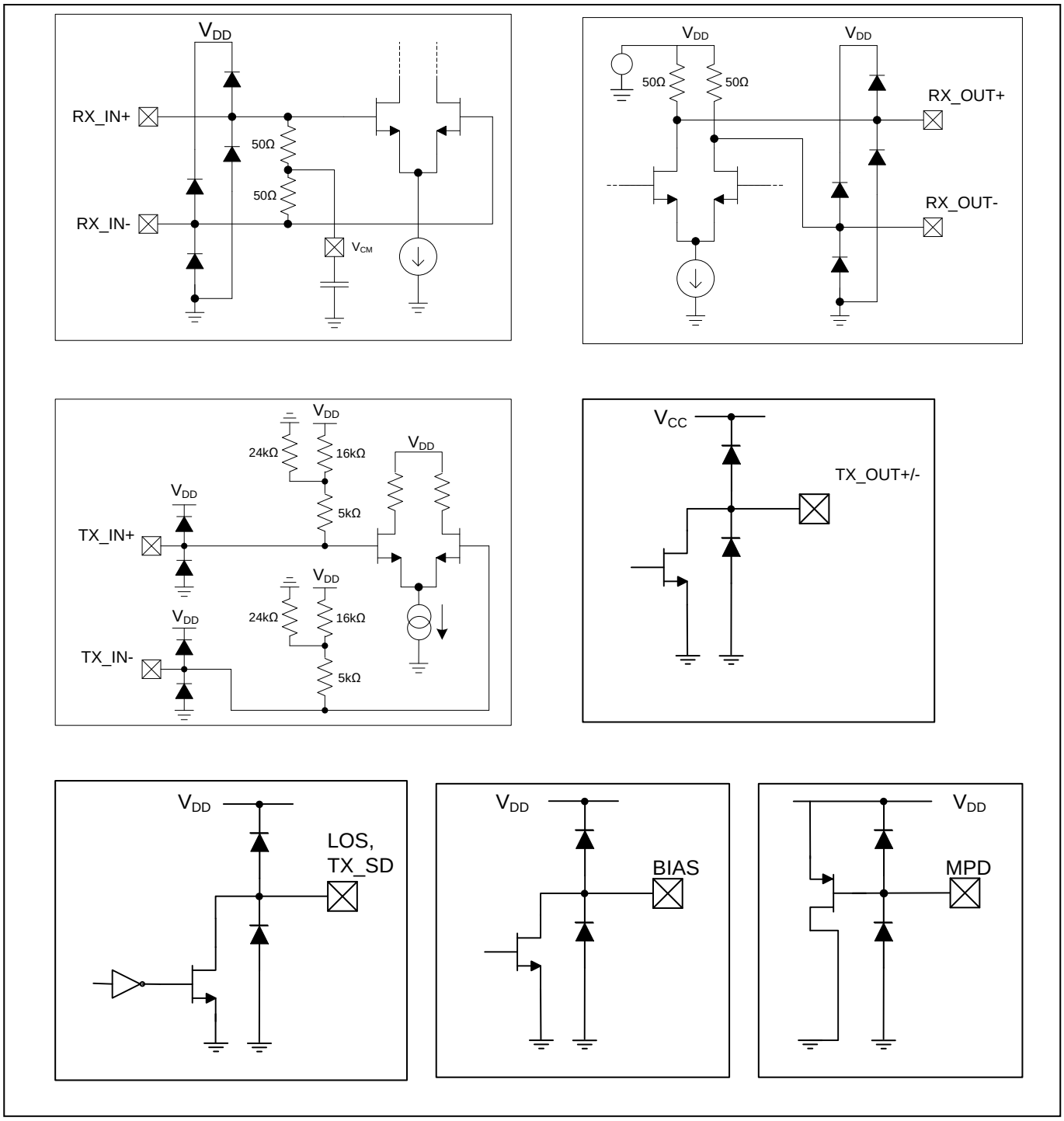


Figure 27. Interface Diagrams

ONU Application Diagrams

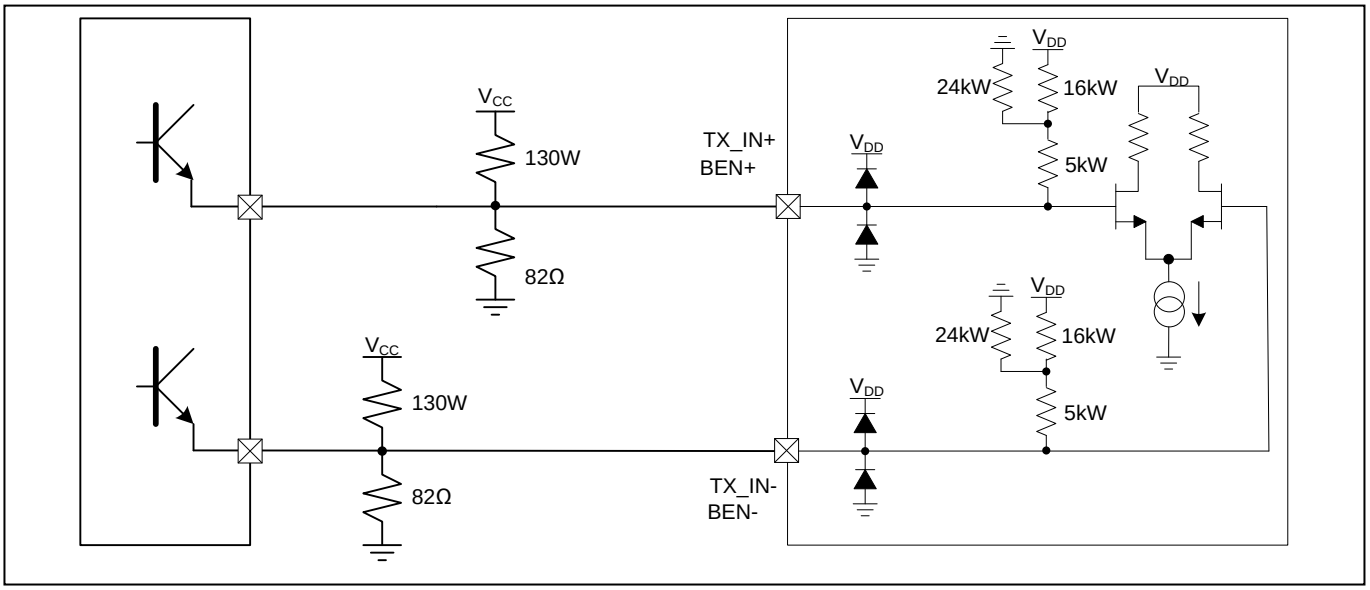


Figure 28. LVPECL External Terminations

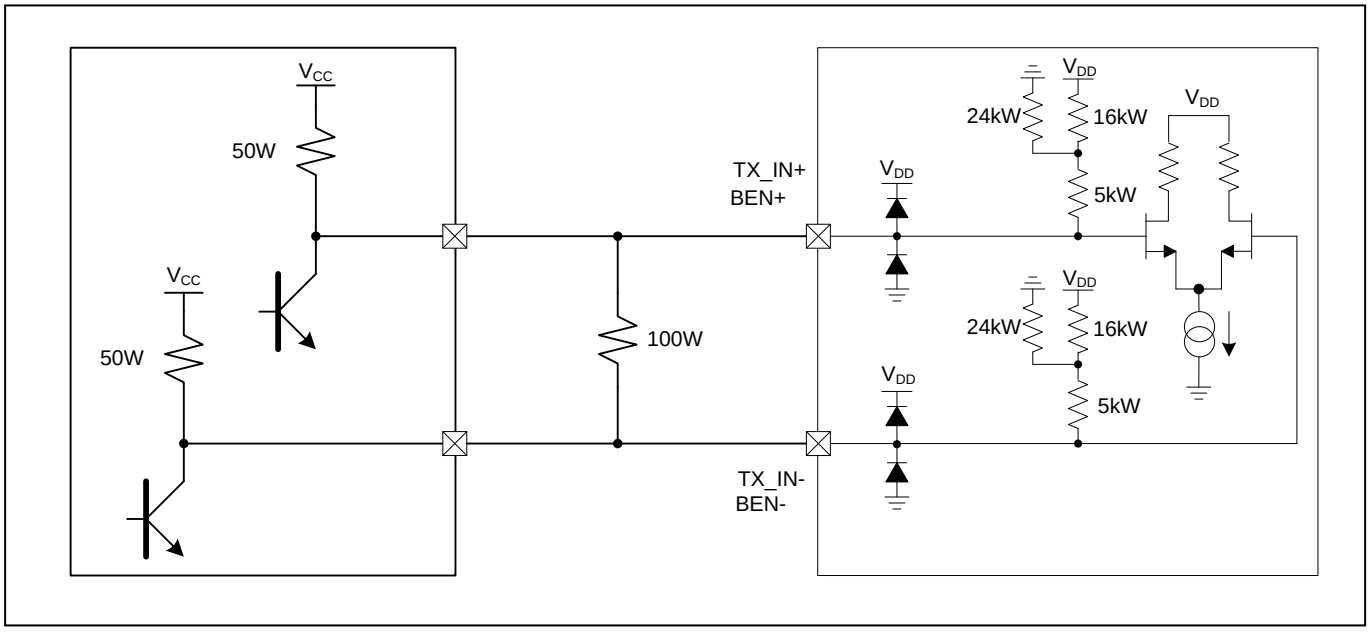


Figure 29. CML External Terminations

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN-EP	T4055+2	21-0140	90-0002

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/12	Initial release	—
1	7/13	Made corrections to *Pin Description*, Figure 15, 94h register table	10, 24, 39
2	2/14	Made corrections to *Pin Description*, *apc loop bandwidth* section, Figure 15, mismatch font, *mpd_range* section, *Register Map* section, Figure 29, and bold typeface for register table headings	10, 12, 20, 21, 25–29, 36–49, 50, 52

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