THE DATASHEET OF

MAX1168BEEG+

www.win-source.net 0086-755-83957316

19-2956; Rev 1; 10/09

EVALUATION KIT AVAILABLE

Multichannel, 16-Bit, 200ksps Analog-to-Digital Converters

General Description

The MAX1167/MAX1168 low-power, multichannel, 16-bit analog-to-digital converters (ADCs) feature a successive-approximation ADC, integrated +4.096V reference, a reference buffer, an internal oscillator, automatic power-down, and a high-speed SPI™/QSPI™/MICROWIRE™-compatible interface. The MAX1167/MAX1168 operate with a single +5V analog supply and feature a separate digital supply, allowing direct interfacing with +2.7V to +5.5V digital logic.

The MAX1167/MAX1168 consume only 3.6mA (AV_{DD} = DV_{DD} = +5V) at 200ksps when using an external reference. AutoShutdown™ reduces the supply current to 185µA at 10ksps and to less than 10µA at reduced sampling rates.

The MAX1167 includes a 4-channel input multiplexer, and the MAX1168 accepts up to eight analog inputs. In addition, digital signal processor (DSP)-initiated conversions are simplified with the DSP frame-sync input and output featured in the MAX1168. The MAX1168 includes a data-bit transfer input to select between 8-bit-wide or 16-bit-wide data-transfer modes. Both devices feature a scan mode that converts each channel sequentially or one channel continuously.

Excellent dynamic performance and low power, combined with ease of use and an integrated reference, make the MAX1167/MAX1168 ideal for control and data-acquisition operations or for other applications with demanding power consumption and space requirements. The MAX1167 is available in a 16-pin QSOP package and the MAX1168 is available in a 24-pin QSOP package. Both devices are guaranteed over the commercial (0°C to +70°C) and extended (-40°C to +85°C) temperature ranges. Use the MAX1168 evaluation kit to evaluate the MAX1168.

Applications

Motor Control

Industrial Process Control

Industrial I/O Modules

Data-Acquisition Systems

Thermocouple Measurements

Accelerometer Measurements

Features

- **16-Bit Resolution, No Missing Codes**
- **+5V Single-Supply Operation**
- **Adjustable Logic Level (+2.7V to +5.25V)**
- **Input Voltage Range: 0 to V_{REF}**
- **Internal (+4.096V) or External (+3.8V to AV_{DD}) Reference**
- **Internal Track/Hold, 4MHz Input Bandwidth**
- **Internal or External Clock**
- **SPI/QSPI/MICROWIRE-Compatible Serial Interface, MAX1168 Performs DSP-Initiated Conversions**
- **8-Bit-Wide or 16-Bit-Wide Data-Transfer Mode (MAX1168 Only)**
- **4-Channel (MAX1167) or 8-Channel (MAX1168) Input Mux**
  - **Scan Mode Sequentially Converts Multiple Channels or One Channel Continuously**
- **Low Power**
  - **3.6mA at 200ksps**
  - **1.85mA at 100ksps**
  - **185µA at 10ksps**
  - **0.6µA in Full Power-Down Mode**
- **Small Package Size**
  - **16-Pin QSOP (MAX1167)**
  - **24-Pin QSOP (MAX1168)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX1167BCEE	0°C to +70°C	16 QSOP	±3
MAX1167BEEE	-40°C to +85°C	16 QSOP	±3
MAX1168BCEG	0°C to +70°C	24 QSOP	±3
MAX1168BEEG	-40°C to +85°C	24 QSOP	±3

Pin Configurations appear at end of data sheet.

SPI/QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

AutoShutdown is a trademark of Maxim Integrated Products, Inc.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Multichannel, 16-Bit, 200ksps Analog-to-Digital Converters

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +6V
DV_{DD} to DGND.....-0.3V to +6V
DGND to AGND.....-0.3V to +0.3V
AIN_, REF, REFCAP to AGND.....-0.3V to (AV_{DD} + 0.3V)
SCLK, $\overline{CS}$, DSEL, DSPR, DIN to DGND .....-0.3V to +6V
DOUT, DSPX, $\overline{EOC}$ to DGND.....-0.3V to (DV_{DD} + 0.3V)
Maximum Current into Any Pin.....50mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
24-Pin QSOP (derate 9.5mW/°C above +70°C).....762mW
Operating Temperature Ranges
MAX116_ _ CE_ .....0°C to +70°C
MAX116_ _ EE_ .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = +4.75V to +5.25V, f_{SCLK} = 4.8MHz external clock (50% duty cycle), 24 clocks/conversion (200ksps), external V_{REF} = +4.096V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				16			Bits
Relative Accuracy (Note 2)	INL	MAX116_B			±1.8	±3	LSB
Differential Nonlinearity	DNL	MAX116_B (16 bit, no missing codes over temperature)		16-bit NMC	+0.7	+1.75	LSB
Transition Noise		RMS noise	External reference		0.7		LSB_{RMS}
			Internal reference		0.8		
Offset Error					±0.1	±10	mV
Gain Error		(Note 3)			±0.01	±0.2	%FSR
Offset Drift					1		ppm/°C
Gain Drift		(Note 3)			±1.2		ppm/°C
DYNAMIC SPECIFICATIONS (1kHz sine wave, 4.096V_{P-P}) (Note 1)							
Signal-to-Noise Plus Distortion	SINAD			85	88.5		dB
Signal-to-Noise Ratio	SNR			86	88.5		dB
Total Harmonic Distortion	THD				-100	-88	dB
Spurious-Free Dynamic Range	SFDR			88	101		dB
Full-Power Bandwidth		-3dB point			4		MHz
Full-Linear Bandwidth		SINAD > 85dB			10		kHz
Channel-to-Channel Isolation		(Note 4)			96		dB
CONVERSION RATE							
Conversion Time	t_{CONV}	Internal clock, no data transfer, single conversion (Note 5)			5.52	7.07	µs
		External clock			3.75		
Acquisition Time	t_{ACQ}	(Note 6)		729			ns
Serial Clock Frequency	f_{SCLK}	External clock, data transfer and conversion		0.1		4.8	MHz
		External clock, data transfer only				9	

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +4.75V to +5.25V, f_{SCLK} = 4.8MHz external clock (50% duty cycle), 24 clocks/conversion (200ksps), external V_{REF} = +4.096V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Clock Frequency	f_{INTCLK}	Internal clock	3.2	4.0		MHz
Aperture Delay	t_{AD}			15		ns
Aperture Jitter	t_{AJ}			<50		ps
Sample Rate (Note 7)	f_S	8-bit-wide data-transfer mode	4.17		200.00	ksps
		16-bit-wide data-transfer mode	3.125		150.00	
		Internal clock, single conversion, 8-bit-wide data-transfer mode		89		
		Internal clock, single conversion, 16-bit-wide data-transfer mode		68		
		Internal clock, scan mode, 8-bit-wide data-transfer mode (four conversions)		103		
		External clock, scan mode, 16-bit-wide data-transfer mode (four conversions)		82		
Duty Cycle			45		55	%
ANALOG INPUT (AIN_)						
Input Range	$V_{AIN_}$		0		V_{REF}	V
Input Capacitance	$C_{AIN_}$			45		pF
EXTERNAL REFERENCE						
Input Voltage Range	V_{REF}	(Note 8)	3.8		AV_{DD} - 0.2	V
Input Current	I_{REF}	$V_{AIN_}$ = 0		34		µA
		SCLK idle		0.1		
		$\overline{CS}$ = DV_{DD}, SCLK idle		0.1		
INTERNAL REFERENCE						
Reference Voltage	V_{REFIN}		4.042	4.096	4.136	V
Reference Short-Circuit Current	I_{REFSC}			13		mA
Reference Temperature Coefficient				±25		ppm/°C
Reference Wake-Up Time	t_{RWAKE}	V_{REF} = 0		5		ms
DIGITAL INPUTS (SCLK, $\overline{CS}$, DSEL, DSPR, DIN) (DV_{DD} = +2.7V to +5.25V)						
Input High Voltage	V_{IH}		0.7 × DV_{DD}			V
Input Low Voltage	V_{IL}				0.3 × DV_{DD}	V
Input Leakage Current	I_{IN}	Digital inputs = 0 to DV_{DD}		±0.1	±1	µA
Input Hysteresis	V_{HYST}			0.2		V
Input Capacitance	C_{IN}			15		pF

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ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +4.75V to +5.25V, f_{SCLK} = 4.8MHz external clock (50% duty cycle), 24 clocks/conversion (200ksps), external V_{REF} = +4.096V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL OUTPUT (DOUT, DSPX, $\overline{EOC}$) (DV_{DD} = +2.7V to +5.25V)							
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA		DV_{DD} - 0.4			V
Output Low Voltage	V_{OL}	I_{SINK} = 10mA, DV_{DD} = +4.75V to +5.25V				0.8	V
		I_{SINK} = 1.6mA, DV_{DD} = +2.7V to +5.25V				0.4	
Three-State Output Leakage Current	I_L	$\overline{CS}$ = DV_{DD}			±0.1	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = DV_{DD}			15		pF
POWER SUPPLIES							
Analog Supply	AV_{DD}			4.75		5.25	V
Digital Supply	DV_{DD}			2.70		5.25	V
Analog Supply Current (Note 9)	I_{AVDD}	200ksps	External reference		2.7	3.3	mA
			Internal reference		3.6	4.2	
		100ksps	External reference		1.4		
			Internal reference		2.7		
		10ksps	External reference		0.14		
			Internal reference		1.8		
		1ksps	External reference		0.014		
			Internal reference		1.7		
Digital Supply Current	I_{DVDD}	DOUT = all zeros	200ksps		0.87	1.3	mA
			100ksps		0.45		
			10ksps		0.045		
			1ksps		0.005		
Power-Down Supply Current	I_{AVDD} + I_{DVDD}	$\overline{CS}$ = DV_{DD}, SCLK = 0, DIN = 0, DSPR = DV_{DD}	Internal reference and reference buffer on between conversions		0.66		mA
			Internal reference on, reference buffer off between conversions		0.20		
Shutdown Supply Current	I_{AVDD} + I_{DVDD}	$\overline{CS}$ = DV_{DD}, SCLK = 0, DIN = 0, DSPR = DV_{DD}, full power-down			0.6	10	µA
Power-Supply Rejection Ratio	PSRR	AV_{DD} = DV_{DD} = 4.75V to 5.25V, full-scale input (Note 10)			63		dB

TIMING CHARACTERISTICS (Figures 1, 2, 8, and 16)

(**AV_{DD} = DV_{DD} = +4.75V to +5.25V**, f_{SCLK} = 4.8MHz external clock (50% duty cycle), 24 clocks/conversion (200ksps), external V_{REF} = +4.096V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}	External clock (Note 6)		729			ns
SCLK to DOUT Valid	t_{DO}	C_{DOUT} = 30pF				50	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DV}	C_{DOUT} = 30pF				80	ns
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_{DOUT} = 30pF				80	ns
$\overline{CS}$ Pulse Width	t_{CSW}			100			ns
$\overline{CS}$ to SCLK Setup	t_{CSS}	SCLK rise		100			ns
		SCLK fall (DSP)					
$\overline{CS}$ to SCLK Hold	t_{CSH}	SCLK rise		0			ns
		SCLK fall (DSP)					
SCLK High Pulse Width	t_{CH}	Duty cycle 45% to 55%	Conversion	93			ns
			Data transfer	50			
SCLK Low Pulse Width	t_{CL}	Duty cycle 45% to 55%	Conversion	93			ns
			Data transfer	50			
SCLK Period	t_{CP}			209			ns
DIN to SCLK Setup	t_{DS}	SCLK rise		50			ns
		SCLK fall (DSP)					
DIN to SCLK Hold	t_{DH}	SCLK rise		0			ns
		SCLK fall (DSP)					
$\overline{CS}$ Falling to DSPR Rising	t_{DF}			100			ns
DSPR to SCLK Falling Setup	t_{FSS}			100			ns
DSPR to SCLK Falling Hold	t_{FSH}			0			ns

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TIMING CHARACTERISTICS (Figures 1, 2, 8, and 16)

(AV_{DD} = +4.75V to +5.25V, **DV_{DD} = +2.7V to +5.25V**, f_{SCLK} = 4.8MHz external clock (50% duty cycle), 24 clocks/conversion (200ksps), external V_{REF} = +4.096V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

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SCLK to DOUT Valid	t_{DO}	C_{DOUT} = 30pF				100	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DV}	C_{DOUT} = 30pF				100	ns
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_{DOUT} = 30pF				80	ns
$\overline{CS}$ Pulse Width	t_{CSW}			100			ns
$\overline{CS}$ to SCLK Setup	t_{CSS}	SCLK rise		100			ns
		SCLK fall (DSP)					
$\overline{CS}$ to SCLK Hold	t_{CSH}	SCLK rise		0			ns
		SCLK fall (DSP)					
SCLK High Pulse Width	t_{CH}	Duty cycle 45% to 55%	Conversion	93			ns
			Data transfer	93			
SCLK Low Pulse Width	t_{CL}	Duty cycle 45% to 55%	Conversion	93			ns
			Data transfer	93			
SCLK Period	t_{CP}			209			ns
DIN to SCLK Setup	t_{DS}	SCLK rise		100			ns
		SCLK fall (DSP)					
DIN to SCLK Hold	t_{DH}	SCLK rise		0			ns
		SCLK fall (DSP)					
$\overline{CS}$ Falling to DSPR Rising	t_{DF}			100			ns
DSPR to SCLK Falling Setup	t_{FSS}			100			ns
DSPR to SCLK Falling Hold	t_{FSH}			0			ns

Note 1: AV_{DD} = DV_{DD} = +5.0V.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after full-scale range has been calibrated.

Note 3: Offset and reference errors nulled.

Note 4: DC voltage applied to on channel, and a full-scale 1kHz sine wave applied to off channels.

Note 5: Conversion time is measured from the rising edge of the 8th external SCLK pulse to $\overline{EOC}$ transition minus t_{ACQ} in 8-bit data-transfer mode.

Note 6: See Figures 10 and 17.

Note 7: f_{SCLK} = 4.8MHz, f_{INTCLK} = 4.0MHz. Sample rate is calculated with the formula $f_S = n_1 (n_2 / f_{SCLK} + n_3 / f_{INTCLK})^{-1}$ where: n_1 = number of scans, n_2 = number of SCLK cycles, and n_3 = number of internal clock cycles (see Figures 11–14).

Note 8: Guaranteed by design; not production tested.

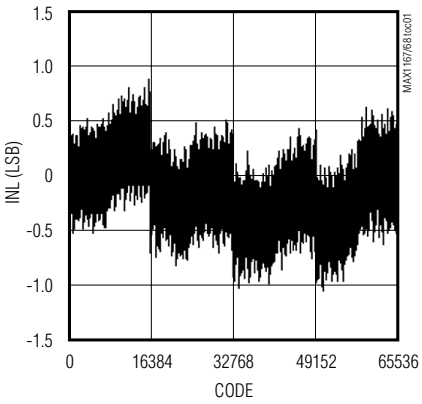
Note 9: Internal reference and buffer are left on between conversions.

Note 10: Defined as the change in the positive full scale caused by a ±5% variation in the nominal supply voltage.

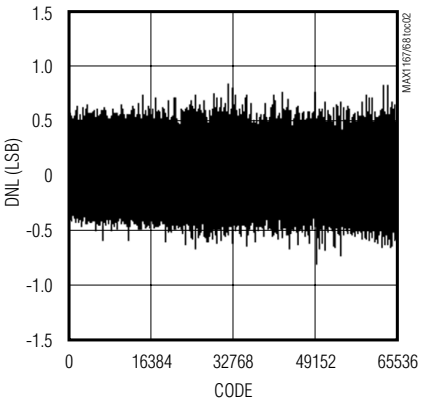
Typical Operating Characteristics

(AV_{DD} = DV_{DD} = +5V, f_{SCLK} = 4.8MHz, C_{DOUT} = 30pF, external V_{REF} = +4.096V, T_A = +25°C, unless otherwise noted.)

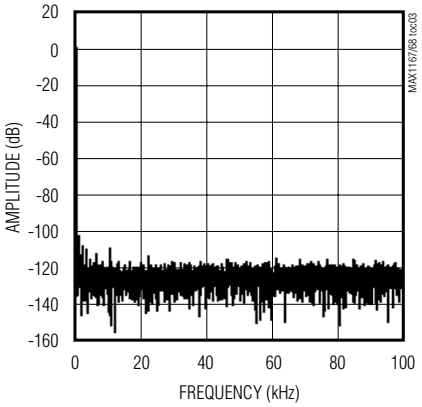
INL vs. CODE



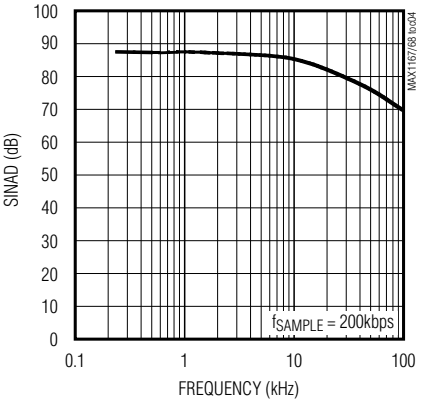
DNL vs. CODE



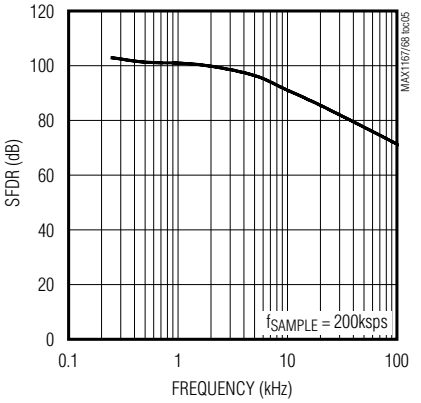
FFT AT f_{AIN} = 1kHz



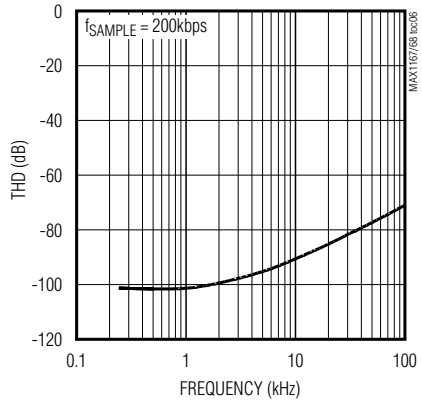
SINAD vs. FREQUENCY



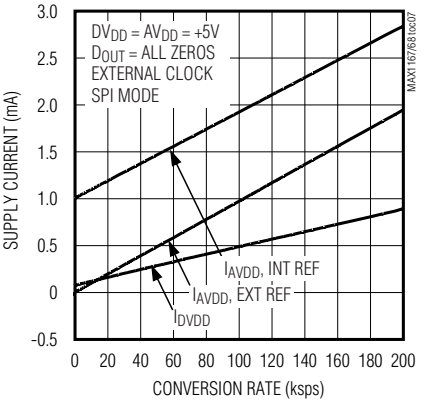
SFDR vs. FREQUENCY



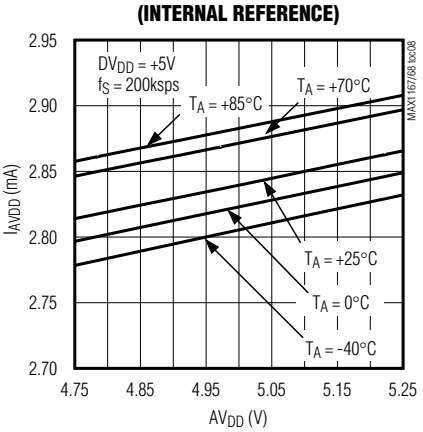
THD vs. FREQUENCY



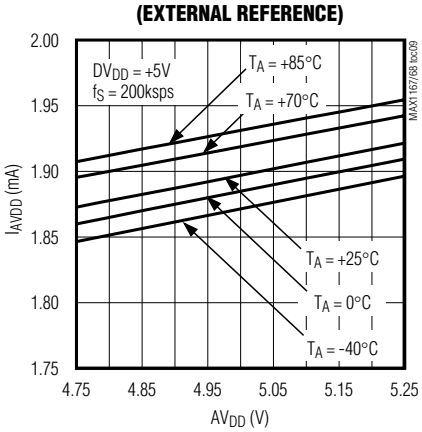
SUPPLY CURRENT vs. CONVERSION RATE (EXTERNAL CLOCK)



ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE (INTERNAL REFERENCE)



ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE (EXTERNAL REFERENCE)

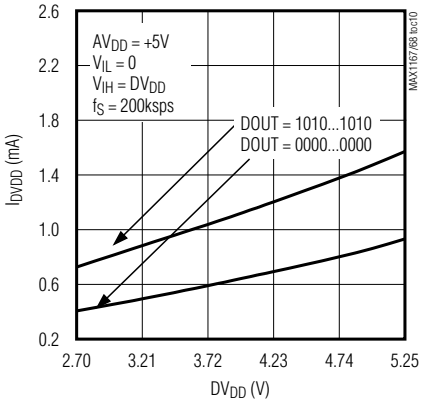


Multichannel, 16-Bit, 200ksps Analog-to-Digital Converters

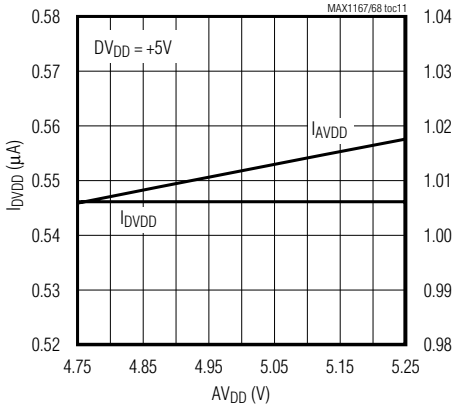
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = +5V, f_{SCLK} = 4.8MHz, C_{DOUT} = 30pF, external V_{REF} = +4.096V, T_A = +25°C, unless otherwise noted.)

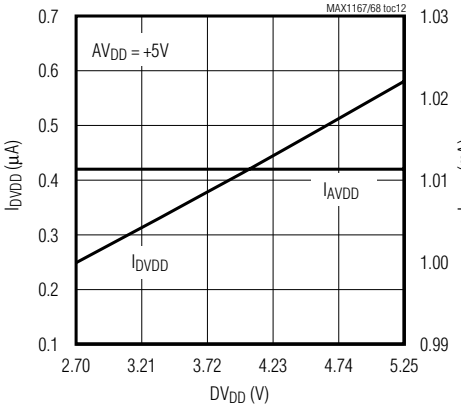
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



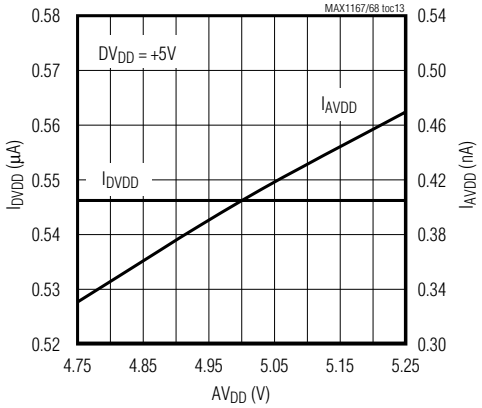
POWER-DOWN SUPPLY CURRENT vs. AV_{DD} SUPPLY VOLTAGE (INTERNAL REFERENCE)



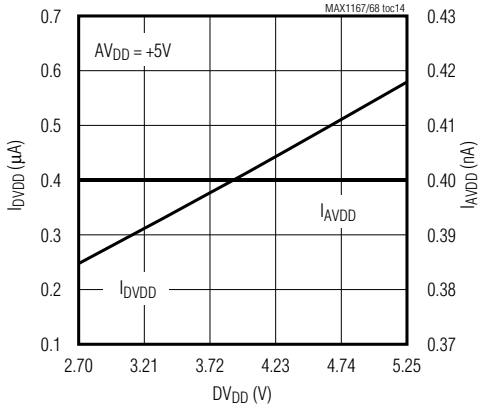
POWER-DOWN SUPPLY CURRENT vs. DV_{DD} SUPPLY VOLTAGE (INTERNAL REFERENCE)



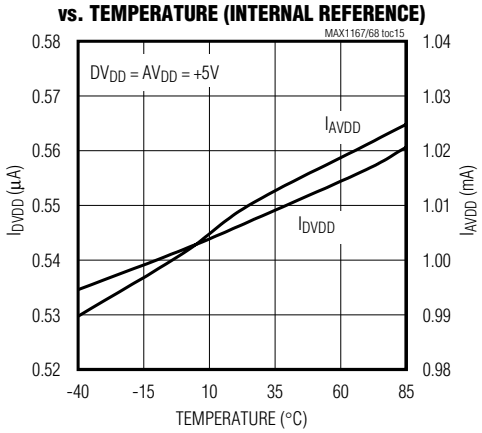
SHUTDOWN SUPPLY CURRENT vs. AV_{DD} SUPPLY VOLTAGE (EXTERNAL REFERENCE)



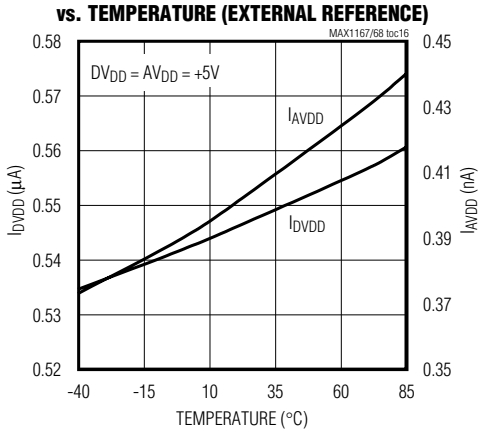
SHUTDOWN SUPPLY CURRENT vs. DV_{DD} SUPPLY VOLTAGE (EXTERNAL REFERENCE)



POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE (INTERNAL REFERENCE)



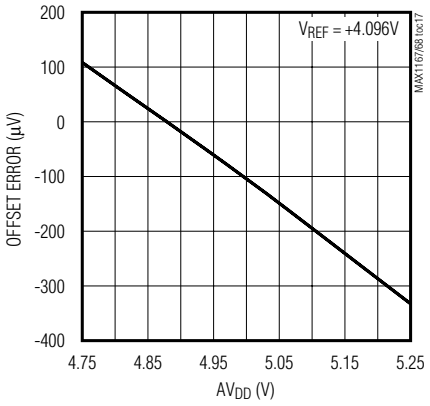
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE (EXTERNAL REFERENCE)



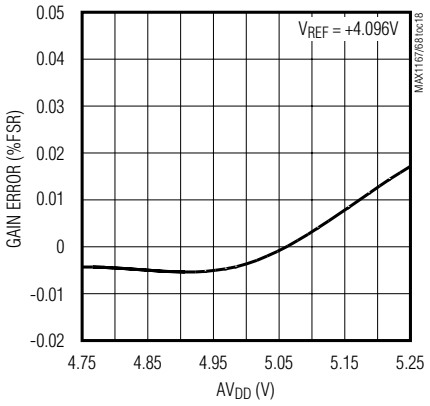
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = +5V, f_{SCLK} = 4.8MHz, C_{DOUT} = 30pF, external V_{REF} = +4.096V, T_A = +25°C, unless otherwise noted.)

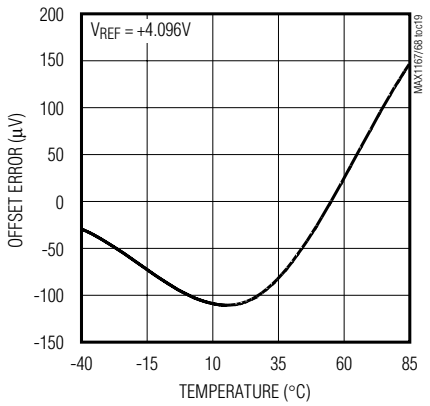
OFFSET ERROR vs. SUPPLY VOLTAGE



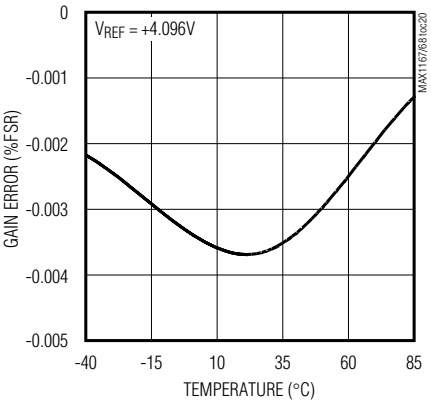
GAIN ERROR vs. SUPPLY VOLTAGE



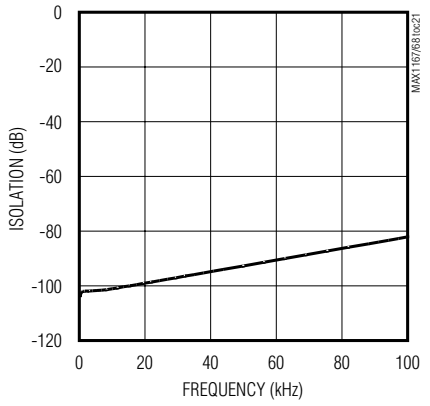
OFFSET ERROR vs. TEMPERATURE



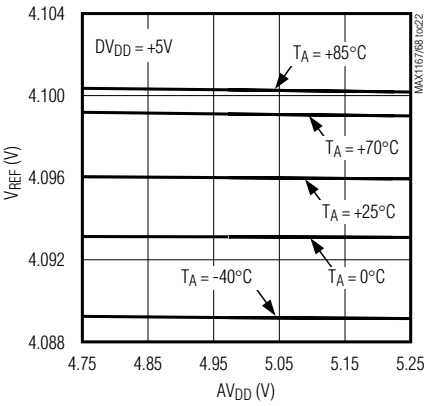
GAIN ERROR vs. TEMPERATURE



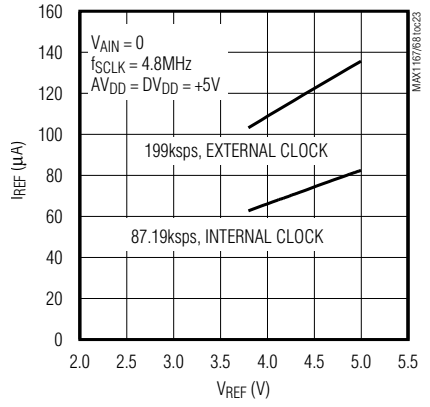
CHANNEL-TO-CHANNEL ISOLATION vs. FREQUENCY



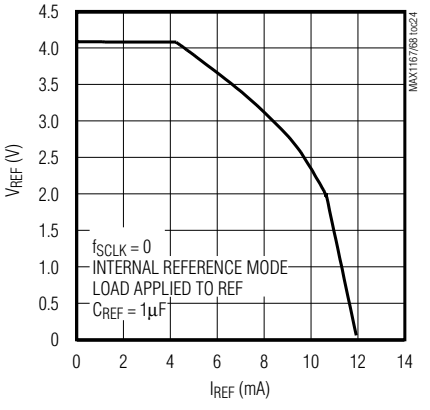
INTERNAL +4.096V REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



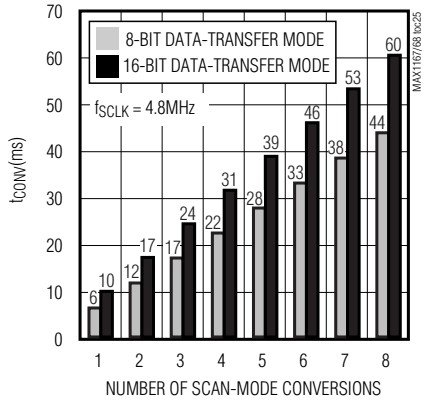
EXTERNAL REFERENCE INPUT CURRENT vs. EXTERNAL REFERENCE VOLTAGE



INTERNAL REFERENCE VOLTAGE vs. REF LOAD



INTERNAL CLOCK CONVERSION TIME (8th RISING SCLK TO FALLING $\overline{EOC}$)



Multichannel, 16-Bit, 200ksps Analog-to-Digital Converters

Pin Description

PIN		NAME	FUNCTION
MAX1167	MAX1168		
1	3	DOUT	Serial Data Output. Data changes state on SCLK's falling edge in SPI/QSPI/MICROWIRE mode and on SCLK's rising edge in DSP mode (MAX1168 only). DOUT is high impedance when $\overline{CS}$ is high.
2	4	SCLK	Serial Clock Input. SCLK drives the conversion process in external clock mode and clocks data out.
3	5	DIN	Serial Data Input. Use DIN to communicate with the command/configuration/control register. In SPI/QSPI/MICROWIRE mode, the rising edge of SCLK clocks in data at DIN. In DSP mode, the falling edge of SCLK clocks in data at DIN.
4	6	$\overline{EOC}$	End-of-Conversion Output. In internal clock mode, a logic low at $\overline{EOC}$ signals the end of a conversion with the result available at DOUT. In external clock mode, $\overline{EOC}$ remains high.
5	7	AIN0	Analog Input 0
6	8	AIN1	Analog Input 1
7	9	AIN2	Analog Input 2
8	10	AIN3	Analog Input 3
9	15	REF	Reference Voltage Input/Output. V_{REF} sets the analog voltage range. Bypass to AGND with a 10µF capacitor. Bypass with a 1µF (min) capacitor when using internal reference.
10	16	REFCAP	Reference Bypass Capacitor Connection. Bypass to AGND with a 0.1µF capacitor when using internal reference. Internal reference and buffer shut down in external reference mode.
11	17	AGND	Analog Ground. Connect to pin 18 (MAX1168) or pin 12 (MAX1167).
12	18	AGND	Primary Analog Ground (Star Ground). Power return for AV_{DD}.
13	19	AV_{DD}	Analog Supply Voltage. Bypass to AGND with a 0.1µF capacitor.
14	20	$\overline{CS}$	Active-Low Chip-Select Input. Forcing $\overline{CS}$ high places the MAX1167/MAX1168 in shutdown with a typical supply current of 0.6µA. In SPI/QSPI/MICROWIRE mode, a high-to-low transition on $\overline{CS}$ activates normal operating mode. In DSP mode, after the initial $\overline{CS}$ transition from high to low, $\overline{CS}$ can remain low for the entire conversion process (see the *Operating Modes* section).
15	21	DGND	Digital Ground
16	22	DV_{DD}	Digital Supply Voltage. Bypass to DGND with a 0.1µF capacitor.
—	1	DSPR	DSP Frame-Sync Receive Input. A frame-sync pulse received at DSPR initiates a conversion. Connect to logic high when using SPI/QSPI/MICROWIRE mode.
—	2	DSEL	Data-Bit Transfer-Select Input. Logic low on DSEL places the device in 8-bit-wide data-transfer mode. Logic high places the device in 16-bit-wide data-transfer mode. Do not leave DSEL unconnected.
—	11	AIN4	Analog Input 4
—	12	AIN5	Analog Input 5

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1167	MAX1168		
—	13	AIN6	Analog Input 6
—	14	AIN7	Analog Input 7
—	23	DSPX	DSP Frame-Sync Transmit Output. A frame-sync pulse at DSPX notifies the DSP that the MSB data is available at DOUT. Leave DSPX unconnected when not in DSP mode.
—	24	N.C.	No Connection. Not internally connected.

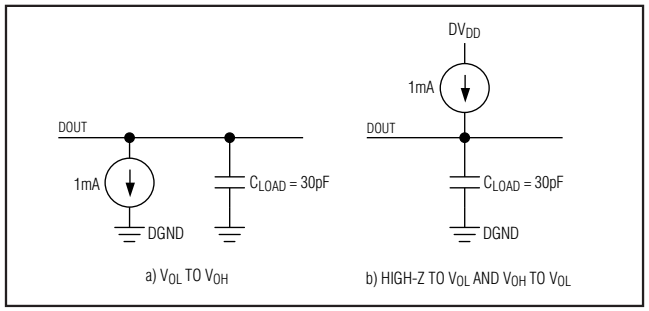


Figure 1. Load Circuits for DOUT Enable Time and SCLK-to-DOUT Delay Time

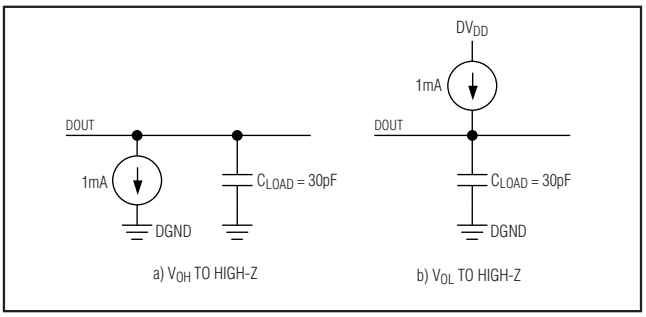


Figure 2. Load Circuits for DOUT Disable Time

Detailed Description

The MAX1167/MAX1168 low-power, multichannel, 16-bit ADCs feature a successive-approximation ADC, automatic power-down, integrated +4.096V reference, and a high-speed SPI/QSPI/MICROWIRE-compatible interface. A DSPR input and DSPX output allow the MAX1168 to communicate with digital signal processors (DSPs) with no external glue logic. The MAX1167/MAX1168 operate with a single +5V analog supply and feature a separate digital supply, allowing direct interfacing with +2.7V to +5.5V digital logic.

Figures 3 and 4 show the functional diagrams of the MAX1167/MAX1168, and Figures 5 and 6 show the MAX1167/MAX1168 in a typical operating circuit. The serial interface simplifies communication with microprocessors (µPs).

In external reference mode, the MAX1167/MAX1168 have two power modes: normal mode and shutdown mode. Driving $\overline{CS}$ high places the MAX1167/MAX1168 in shutdown mode, reducing the supply current to 0.6µA (typ). Pull $\overline{CS}$ low to place the MAX1167/MAX1168 in normal operating mode. The internal reference mode offers software-programmable, power-down options as shown in Table 5.

In SPI/QSPI/MICROWIRE mode, a falling edge on $\overline{CS}$ wakes the analog circuitry and allows SCLK to clock in data. Acquisition and conversion are initiated by SCLK. The conversion result is available at DOUT in unipolar serial format. DOUT is held low until data becomes available (MSB first) on the 8th falling edge of SCLK when in 8-bit transfer mode, and on the 16th falling edge when in 16-bit transfer mode (see the *Operating Modes* section). Figure 8 shows the detailed SPI/QSPI/MICROWIRE serial-interface timing diagram.

In external clock mode, the MAX1168 also interfaces with DSPs. In DSP mode, a frame-sync pulse from the DSP initiates a conversion that is driven by SCLK. The MAX1168 formats a frame-sync pulse to notify the DSP that the conversion results are available at DOUT in MSB-first, unipolar, serial-data format. Figure 16 shows the detailed DSP serial-interface timing diagram (see the *Operating Modes* section).

Analog Input

Figure 7 illustrates the input-sampling architecture of the ADC. The voltage applied at REF or the internal +4.096V reference sets the full-scale input voltage.

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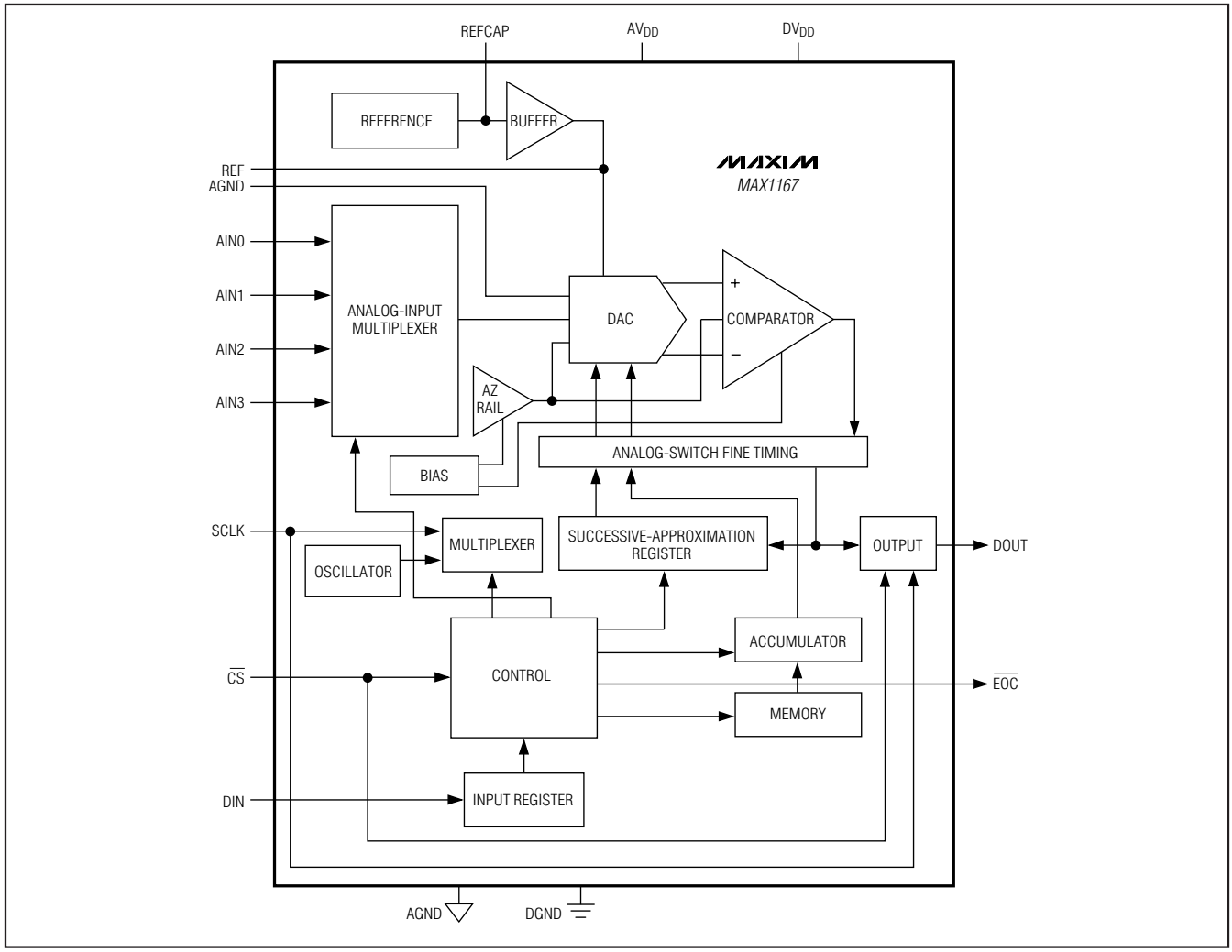

Figure 3. MAX1167 Functional Diagram

Track/Hold (T/H)

In track mode, the analog signal is acquired on the internal hold capacitor. In hold mode, the T/H switches open and the capacitive digital-to-analog converter (DAC) samples the analog input.

During the acquisition, the analog input (AIN_) charges capacitor C_{DAC}. At the end of the acquisition interval the T/H switches open. The retained charge on C_{DAC} represents a sample of the input.

In hold mode, the capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to zero within the limits of 16-bit resolution. At the end of the conversion, force $\overline{CS}$ high and then low to reset the T/H switches back to track mode (AIN_), where C_{DAC} charges to the input signal again.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. The acquisition time (t_{ACQ}) is the maximum time the device takes to acquire the signal. Use the following formula to calculate acquisition time:

$$t_{ACQ} = 11(R_S + R_{IN} + R_{DS(ON)}) \times 45pF + 0.3\mu s$$

where $R_{IN} = 340\Omega$, R_S = the input signal's source impedance, $R_{DS(ON)} = 60\Omega$, and t_{ACQ} is never less than 729ns. A source impedance of less than 200Ω does not significantly affect the ADC's performance.

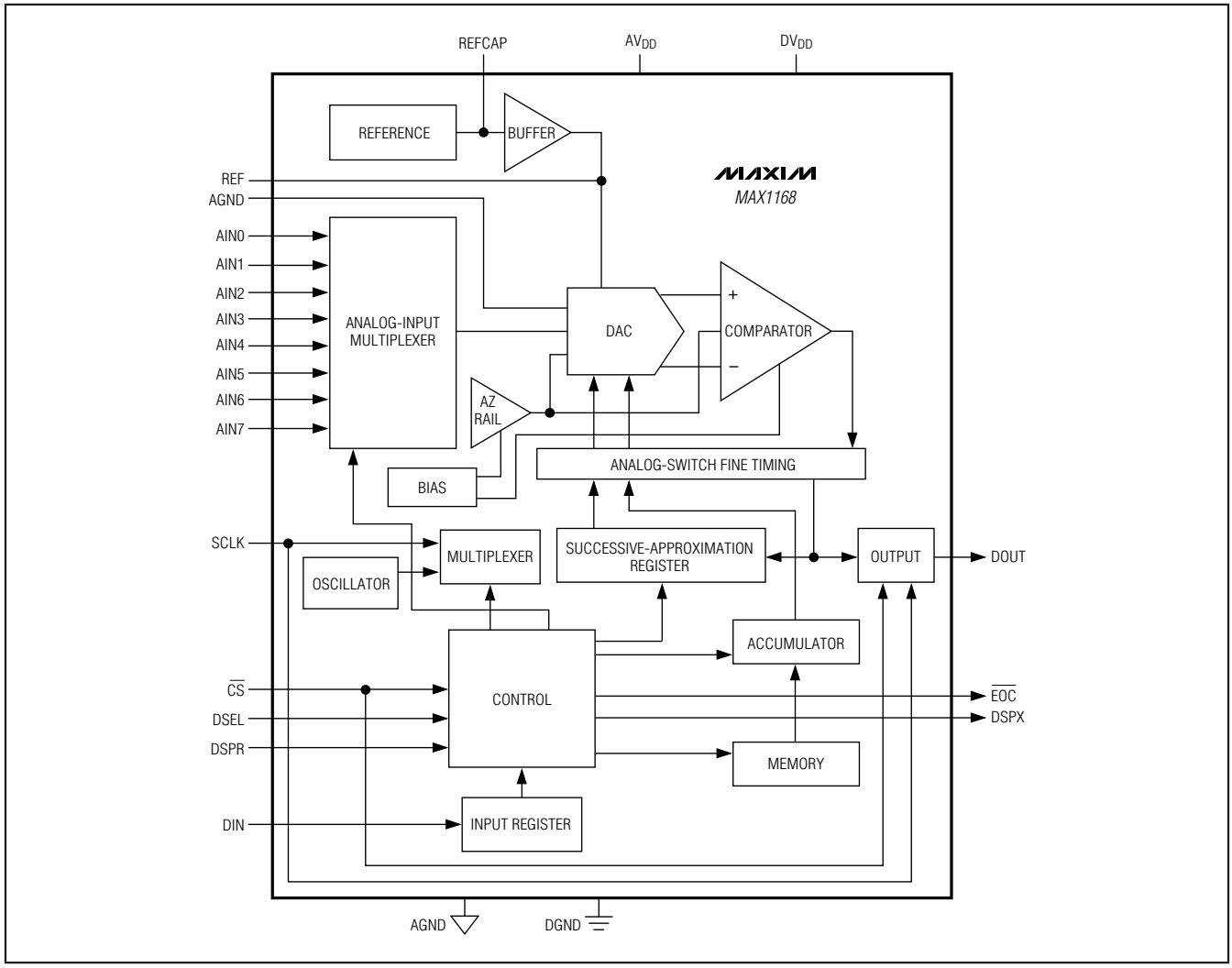

Figure 4. MAX1168 Functional Diagram

The MAX1168 features a 16-bit-wide data-transfer mode that includes a longer acquisition time (11.5 clock cycles). Longer acquisition times are useful in applications with input source resistances greater than 1kΩ. Noise increases when using large source resistances. To improve the input signal bandwidth under AC conditions, drive AIN_ with a wideband buffer (>10MHz) that can drive the ADC's input capacitance and settle quickly.

Input Bandwidth

The ADC's input-tracking circuitry has a 4MHz small-signal bandwidth, making possible the digitization of high-speed transient events and the measurement of periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing of unwanted, high-frequency signals into the frequency band of interest, use anti-alias filtering.

Analog Input Protection

Internal protection diodes, which clamp the analog input to AV_{DD} or AGND, allow the input to swing from (AGND - 0.3V) to (AV_{DD} + 0.3V) without damaging the device. If the analog input exceeds 300mV beyond the supplies, limit the input current to 10mA.

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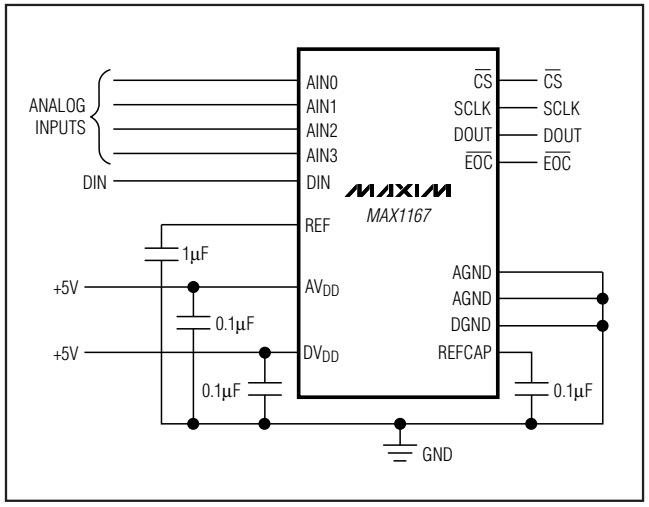

Figure 5. MAX1167 Typical Operating Circuit

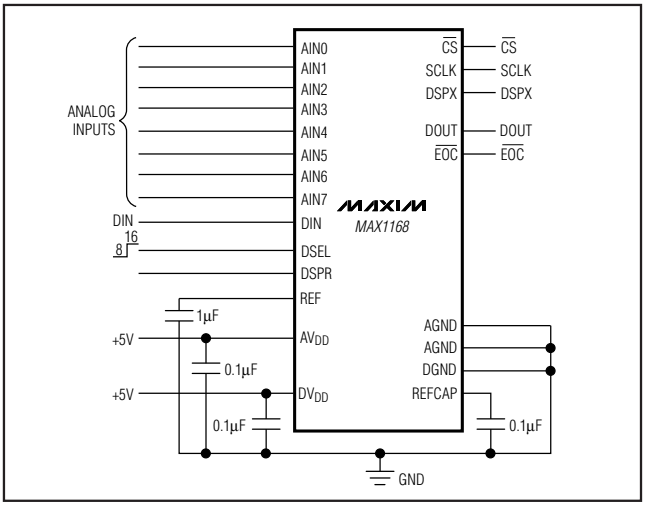

Figure 6. MAX1168 T ypical Operating Circuit

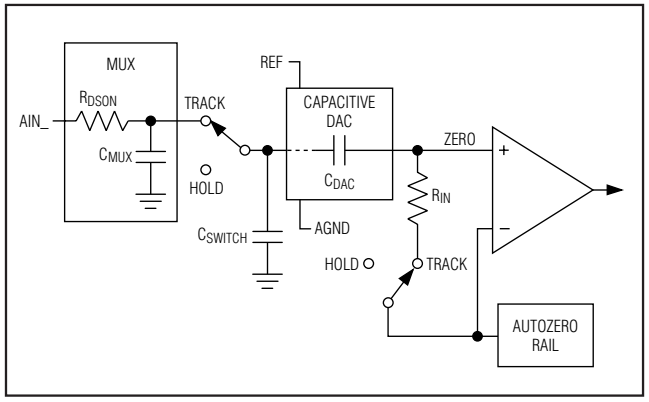

Figure 7. Equivalent Input Circuit

Digital Interface

The MAX1167/MAX1168 feature an SPI/QSPI/MICROWIRE-compatible, 3-wire serial interface. The MAX1167 digital interface consists of digital inputs $\overline{CS}$, SCLK, and DIN and outputs DOUT and $\overline{EOC}$. The MAX1167 operates in the following modes:

- SPI interface with external clock
- SPI interface with internal clock
- SPI interface with internal clock and scan mode

In addition to the standard 3-wire serial interface modes, the MAX1168 includes a DSPR input and a DSPX output for communicating with DSPs in external clock mode and a DSEL input to determine 8-bit-wide or 16-bit-wide data-transfer mode. When not using the MAX1168 in the DSP interface mode, connect DSPR to DV_{DD} and leave DSPX unconnected.

Command/Configuration/Control Register

Table 1 shows the contents of the command/configuration/control register and the state of each bit after initial power-up. Tables 2–6 define the control and configuration of the device for each bit. Cycling the power supplies resets the command/configuration/control register to the power-on-reset default state.

Initialization After Power-Up

A logic high on $\overline{CS}$ places the MAX1167/MAX1168 in the shutdown mode chosen by the power-down bits, and places DOUT in a high-impedance state. Drive $\overline{CS}$ low to power up and enable the MAX1167/MAX1168 before starting a conversion. In internal reference mode, allow 5ms for the shutdown internal reference and/or buffer to wake and stabilize before starting a conversion. In external reference mode (or if the internal reference is already on), no reference settling time is needed after power-up.

Table 1. Command/Configuration/Control Register

COMMAND	BIT7 (MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0 (LSB)
	CH SEL2	CH SEL1	CH SEL0	SCAN1	SCAN0	REF/PD_SEL1	REF/PD SEL0	INT/EXT CLK
POWER-UP STATE	0	0	0	0	0	1	1	0

Table 2. Channel Select

BIT7	BIT6	BIT5	CHANNEL AIN_
CH SEL2	CH SEL1	CH SEL0	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 3. MAX1167 Scan Mode, Internal Clock Only

ACTION	BIT4	BIT3
	SCAN1	SCAN0
Single channel, no scan	0	0
Sequentially scan channels 0 through N (N ≤ 3)	0	1
Sequentially scan channels 2 through N (2 ≤ N ≤ 3)	1	0
Scan channel N four times	1	1

Table 4. MAX1168 Scan Mode, Internal Clock Only (Not for DSP Mode)

ACTION	BIT4	BIT3
	SCAN1	SCAN0
Single channel, no scan	0	0
Sequentially scan channels 0 through N (N ≤ 7)	0	1
Sequentially scan channels 4 through N (4 ≤ N ≤ 7)	1	0
Scan channel N eight times	1	1

Table 5. Power-Down Modes

BIT2	BIT1	REFERENCE	REFERENCE MODE (INTERNAL REFERENCE)	TYPICAL SUPPLY CURRENT	TYPICAL WAKE-UP TIME (C_{REF} = 1µF)
REF/PD_ SEL1	REF/PD SEL0				
0	0	Internal	Internal reference and reference buffer on between conversions	1mA	NA
0	1	Internal	Internal reference and reference buffer off between conversions	0.6µA	5ms
1	0	Internal	Internal reference on, reference buffer off between conversions	0.43mA	5ms
1	1	External	Internal reference and buffer always off	0.6µA	NA

Table 6. Clock Modes

BIT0	CLOCK MODE
INT/EXT CLK	
0	External clock
1	Internal clock

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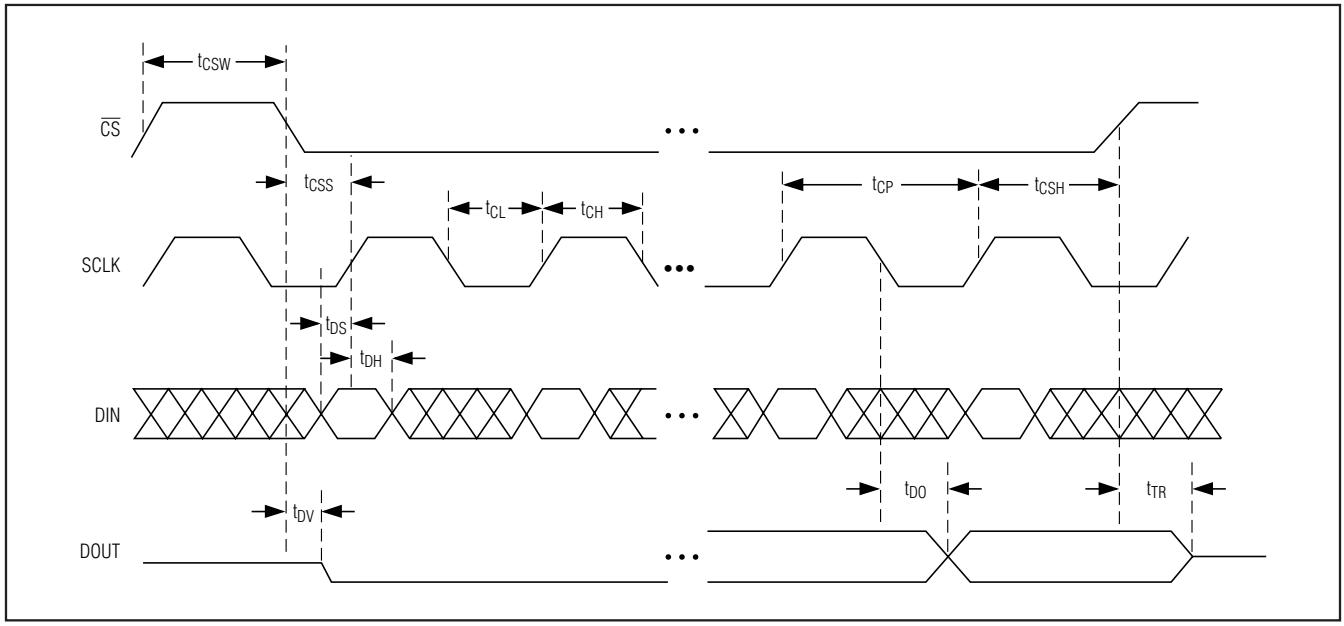

Figure 8. Detailed SPI Interface Timing

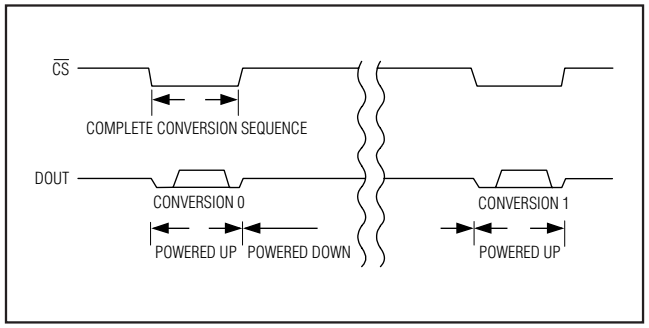

Figure 9. Shutdown Sequence

Power-Down Modes

Table 5 shows the MAX1167/MAX1168 power-down modes. Three internal reference modes and one external reference mode are available. Select power-down modes by writing to bits 2 and 1 in the command/configuration/control register. The MAX1167/MAX1168 enter the selected power-down mode on the rising edge of $\overline{CS}$.

The internal reference stays on when $\overline{CS}$ is pulled high, if bits 2 and 1 are set to zero. This mode allows for the fastest turn-on time.

Setting bit 2 = 0 and bit 1 = 1 turns both the reference and reference buffer off when $\overline{CS}$ is brought high. This mode achieves the lowest supply current. The reference and buffer wake up on the falling edge of $\overline{CS}$ when in SPI/QSPI/MICROWIRE mode and on the falling edge of DSPR when in DSP mode. Allow 5ms for the internal reference to rise and settle when powering up from a complete shutdown (V_{REF} = 0, C_{REF} = 1µF).

The internal reference stays on and the buffer is shut off on the rising edge of $\overline{CS}$ when bit 2 = 1 and bit 1 = 0. The MAX1167/MAX1168 enter this mode on the rising edge of $\overline{CS}$. The buffer wakes up on the falling edge of $\overline{CS}$ when in SPI/QSPI/MICROWIRE mode and on the rising edge of DSPR when in DSP mode. Allow 5ms for V_{REF} to settle when powering up from a complete shutdown (V_{REF} = 0, C_{REF} = 1µF). V_{REFCAP} is always equal to +4.096V in this mode.

Set both bit 2 and bit 1 to 1 to turn off the reference and reference buffer to allow connection of an external reference. Using an external reference requires no extra wake-up time.

Operating Modes

External Clock 8-Bit-Wide Data-Transfer Mode (MAX1167 and MAX1168)

Force DSPR high and DSEL low (MAX1168) for SPI/QSPI/MICROWIRE interface mode. The falling edge of $\overline{CS}$ wakes the analog circuitry and allows SCLK to clock in data. Ensure the duty cycle on SCLK is between 45% and 55% when operating at 4.8MHz (the maximum clock frequency). For lower clock frequencies, ensure the minimum high and low times are at least 93ns. External-clock-mode conversions with

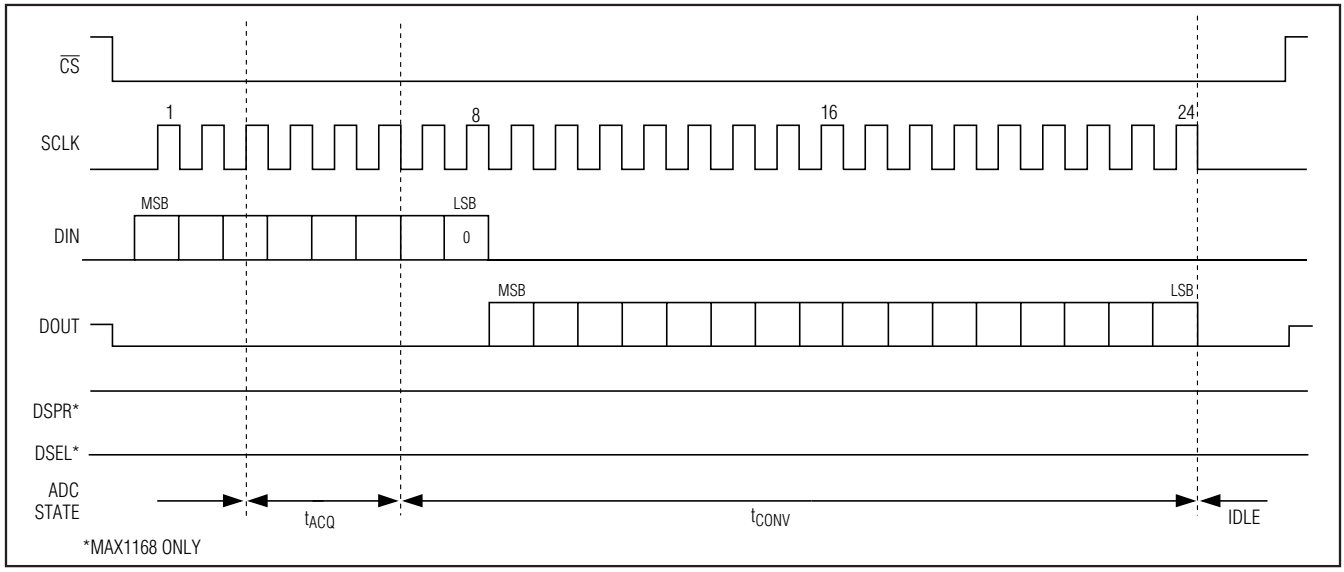

Figure 10. SPI External Clock Mode, 8-Bit Data-Transfer Mode, Conversion Timing

SCLK rates less than 125kHz can reduce accuracy due to leakage of the sampling capacitor. DOUT changes from high-Z to logic low after $\overline{CS}$ is brought low. Input data latches on the rising edge of SCLK. The first SCLK rising edge begins loading data into the command/configuration/control register from DIN. The devices select the proper channel for conversion on the rising edge of the 3rd SCLK cycle. Acquisition begins immediately thereafter and ends on the falling edge of the 6th clock cycle. The MAX1167/MAX1168 sample the input and begin conversion on the falling edge of the 6th clock cycle. Setup and configuration of the MAX1167/MAX1168 complete on the rising edge of the 8th clock cycle. The conversion result is available (MSB first) at DOUT on the falling edge of the 8th SCLK cycle. To read the entire conversion result, 16 SCLK cycles are needed. Extra clock pulses, occurring after the conversion result has been clocked out and prior to the rising edge of $\overline{CS}$, cause zeros to be clocked out of DOUT. The MAX1167/ MAX1168 external clock 8-bit-wide data-transfer mode requires 24 SCLK cycles for completion (Figure 10).

Force $\overline{CS}$ high after the conversion result is read. For maximum throughput, force $\overline{CS}$ low again to initiate the next conversion immediately after the specified minimum time (t_{CSW}). Forcing $\overline{CS}$ high in the middle of a conversion immediately aborts the conversion and places the MAX1167/MAX1168 in shutdown.

External Clock 16-Bit-Wide Data-Transfer Mode (MAX1168 Only)

Force DSPR high and DSEL high for SPI/QSPI/MICROWIRE interface mode. Logic high at DSEL allows the MAX1168 to transfer data in 16-bit-wide words. The acquisition time is extended an extra eight SCLK cycles in the 16-bit-wide data-transfer mode. The falling edge of $\overline{CS}$ wakes the analog circuitry and allows SCLK to clock in data. Ensure the duty cycle on SCLK is between 45% and 55% when operating at 4.8MHz (the maximum clock frequency). For lower clock frequencies, ensure that the minimum high and low times are at least 93ns. External-clock-mode conversions with SCLK rates less than 125kHz can reduce accuracy due to leakage of the sampling capacitor. DOUT changes from high-Z to logic low after $\overline{CS}$ is brought low. Input data latches on the rising edge of SCLK. The first SCLK rising edge begins loading data into the command/configuration/control register from DIN. The devices select the proper channel for conversion and begin acquisition on the rising edge of the 3rd SCLK cycle. Setup and configuration of the MAX1168 completes on the rising edge of the 8th clock cycle. Acquisition ends on the falling edge of the 14th SCLK cycle. The MAX1168 samples the input and begins conversion on the falling edge of the 14th clock cycle. The conversion result is available (MSB first) at DOUT on the falling edge of the 16th SCLK cycle. To read the entire conversion result, 16 SCLK cycles are needed. Extra clock pulses, occurring after the conversion result has been clocked out and prior to the rising edge of $\overline{CS}$, cause zeros to be clocked out of DOUT.

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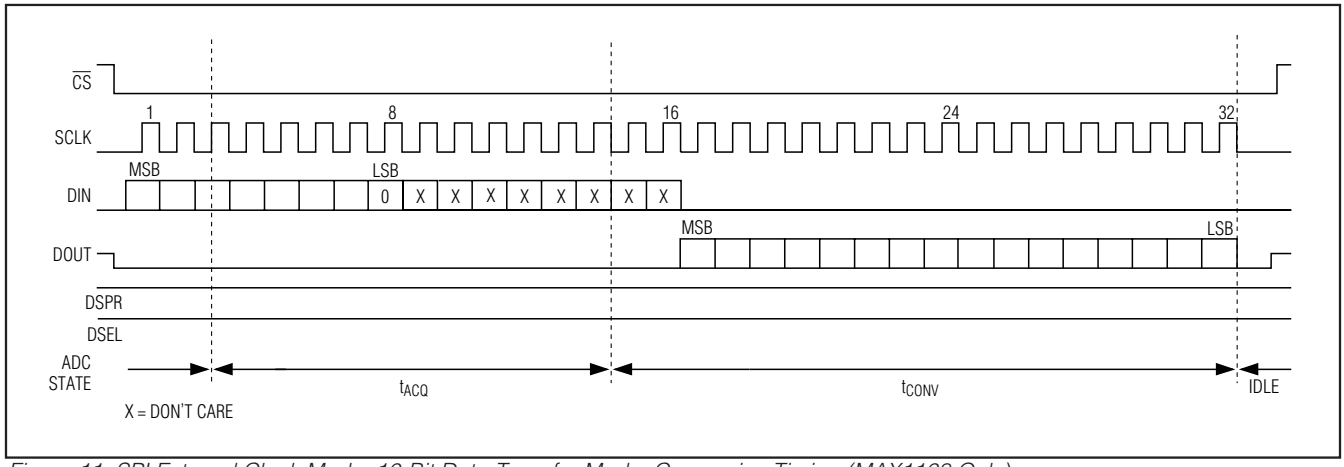

Figure 11. SPI External Clock Mode, 16-Bit Data-Transfer Mode, Conversion Timing (MAX1168 Only)

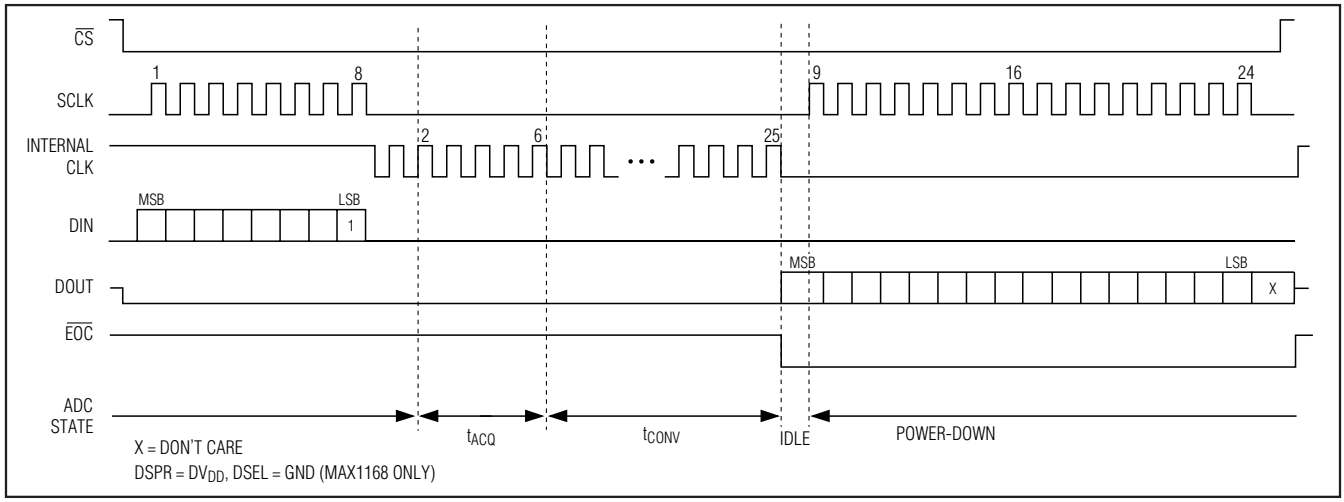

Figure 12. SPI Internal Clock Mode, 8-Bit Data-Transfer Mode, Conversion Timing

The MAX1168 external clock 16-bit-wide data-transfer mode requires 32 SCLK cycles for completion (Figure 11).

Force $\overline{CS}$ high after the conversion result is read. For maximum throughput, force $\overline{CS}$ low again to initiate the next conversion immediately after the specified minimum time (t_{CSW}). Forcing $\overline{CS}$ high in the middle of a conversion immediately aborts the conversion and places the MAX1168 in shutdown.

Internal Clock 8-Bit-Wide Data-Transfer and Scan Mode (MAX1167 and MAX1168)

Force DSPR high and DSEL low (MAX1168) for the SPI/QSPI/MICROWIRE interface mode. The falling edge of $\overline{CS}$ wakes the analog circuitry and allows SCLK to clock in data (Figure 12). DOUT changes from high-Z to logic low after $\overline{CS}$ is brought low. Input data latches on the rising edge of SCLK. The command/configuration/control register begins reading DIN on the first SCLK rising edge and ends on the rising edge of the 8th SCLK cycle. The MAX1167/MAX1168 select the proper channel for conversion on the rising edge of the 3rd SCLK cycle. The internal oscillator activates 125ns after the rising edge of the 8th SCLK cycle. Turn off the external clock while the internal clock is on. Turning off SCLK ensures the lowest noise performance during acquisition. Acquisition begins on the 2nd rising edge of the internal clock and ends on the falling edge of the 6th internal clock cycle. Each bit of the conversion result shifts into memory as it becomes available. The conversion result is available (MSB first) at DOUT on the falling edge of $\overline{EOC}$. The internal oscillator and analog circuitry are shut down on the high-to-low $\overline{EOC}$ transition. Use the $\overline{EOC}$ high-to-low transition as the

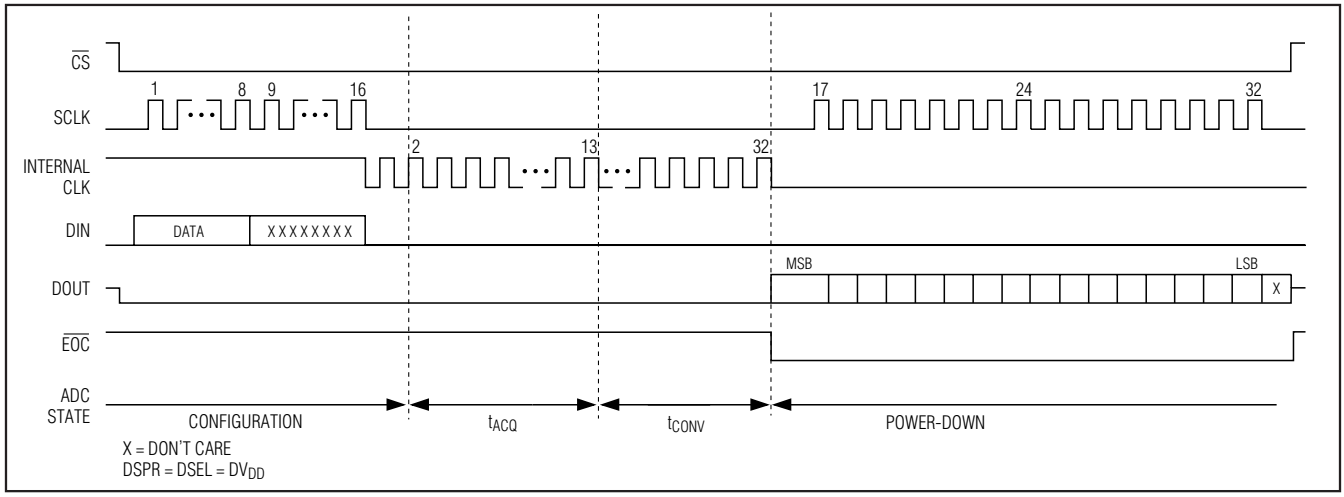

Figure 13. SPI Internal Clock Mode,16-Bit Data-Transfer Mode, Conversion Timing (MAX1168 Only)

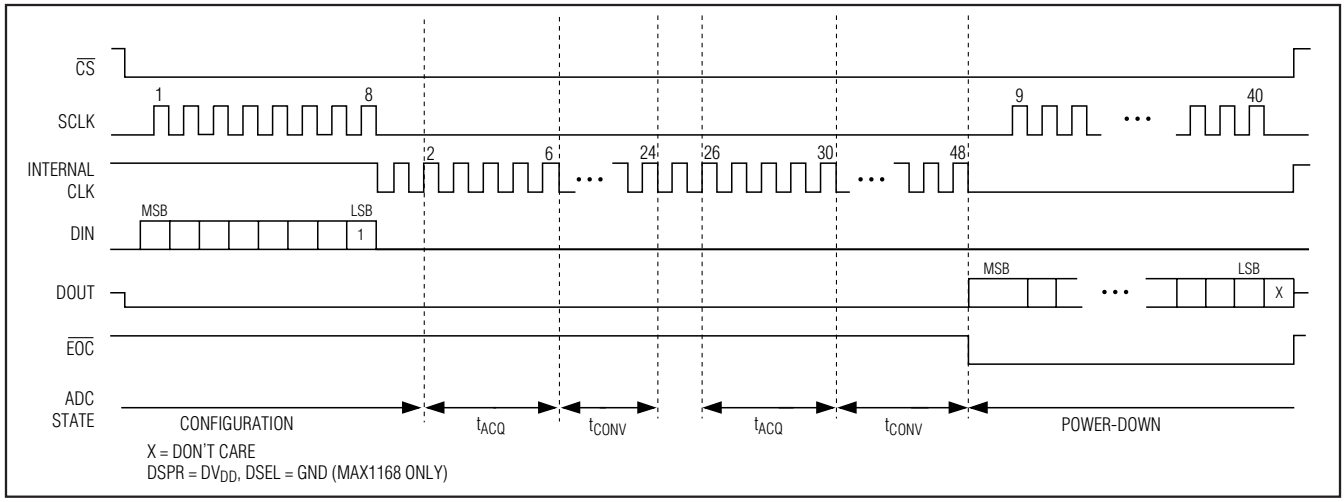

Figure 14. SPI Internal Clock Mode, 8-Bit Data-Transfer Mode, Scan Mode for Two Conversions, Conversion Timing

signal to restart the external clock (SCLK). To read the entire conversion result, 16 SCLK cycles are needed. Extra clock pulses, occurring after the conversion result has been clocked out and prior to the rising edge of $\overline{CS}$, cause the conversion result to be shifted out again. The MAX1167/MAX1168 internal clock 8-bit-wide data-transfer mode requires 24 external clock cycles and 25 internal clock cycles for completion.

Force $\overline{CS}$ high after the conversion result is read. For maximum throughput, force $\overline{CS}$ low again to initiate the next conversion immediately after the specified minimum time (t_{CSW}). Forcing $\overline{CS}$ high in the middle of a conversion immediately aborts the conversion and places the MAX1167/MAX1168 in shutdown.

Scan mode allows multiple channels to be scanned consecutively or one channel to be scanned eight times. Scan mode can only be enabled when using the MAX1167/MAX1168 in the internal clock mode. Enable scanning by setting bits 4 and 3 in the command/configuration/control register (see Tables 3 and 4). In scan mode, conversion results are stored in memory until the completion of the last conversion in the sequence. Upon completion of the last conversion in the sequence, $\overline{EOC}$ transitions from high to low to indicate the end of the conversion and shuts down the internal oscillator. Use the $\overline{EOC}$ high-to-low transition as the signal to restart the external clock (SCLK). DOUT provides the conversion results in the same order as the channel conversion process. The MSB of the first conversion is available at DOUT on the falling edge of $\overline{EOC}$ (Figure 14).

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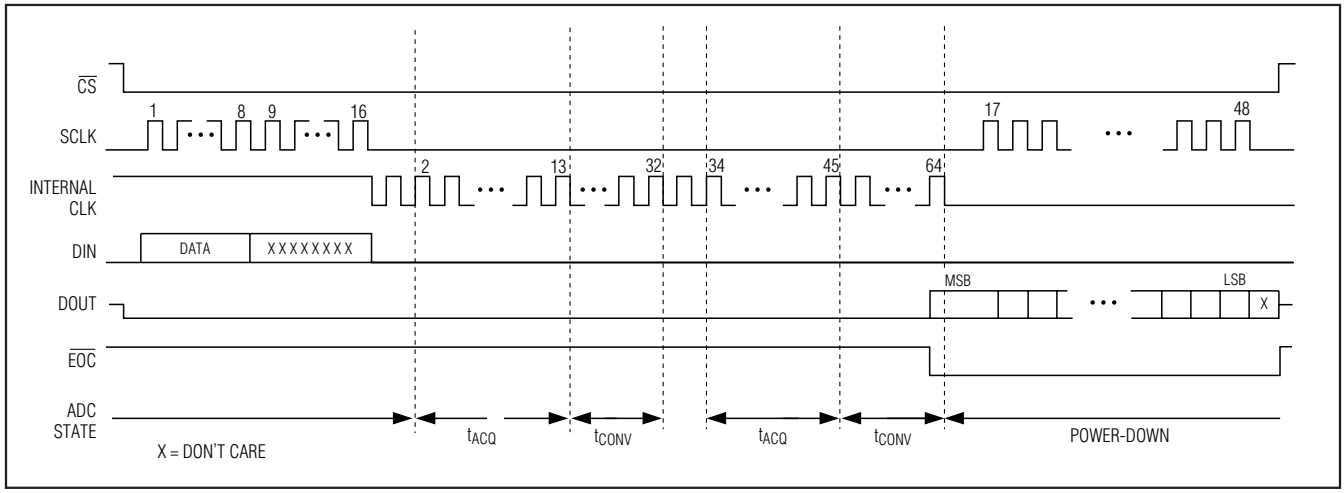

Figure 15. SPI Internal Clock Mode, 16-Bit Data-Transfer Mode, Scan Mode for Two Conversions, Conversion Timing (MAX1168 Only)

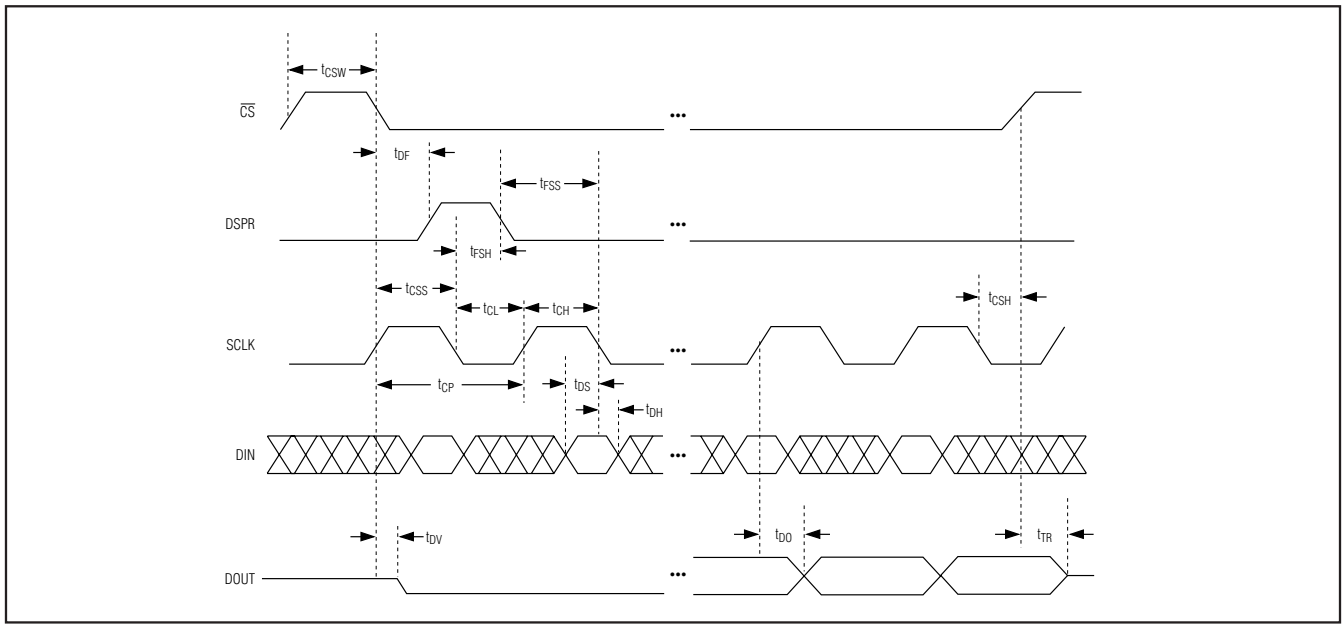

Figure 16. Detailed DSP-Interface Timing (MAX1168 Only)

Internal Clock 16-Bit-Wide Data-Transfer and Scan Mode (MAX1168 Only)

Force DSPR high and DSEL low for the SPI/QSPI/MICROWIRE interface mode. The falling edge of $\overline{CS}$ wakes the analog circuitry and allows SCLK to clock in data (Figure 13). DOUT changes from high-Z to logic low after $\overline{CS}$ is brought low. Input data latches on the rising edge of SCLK. The command/configuration/control register begins reading DIN on the first SCLK rising edge and ends on the rising edge of the 8th SCLK cycle. The MAX1168 selects the proper channel for conversion on the rising edge of the 3rd SCLK cycle. The internal oscillator activates 125ns after the rising edge of the 16th SCLK cycle. Turn off the external clock while the internal clock is on. Turning off SCLK ensures lowest noise performance during acquisition. Acquisition begins on the 2nd rising edge of the internal clock and ends on the falling edge of the 18th internal clock cycle. Each bit of the conversion result shifts into memory as it becomes available. The conversion result is available (MSB first) at DOUT on the falling edge of $\overline{EOC}$. The internal oscillator and analog circuitry

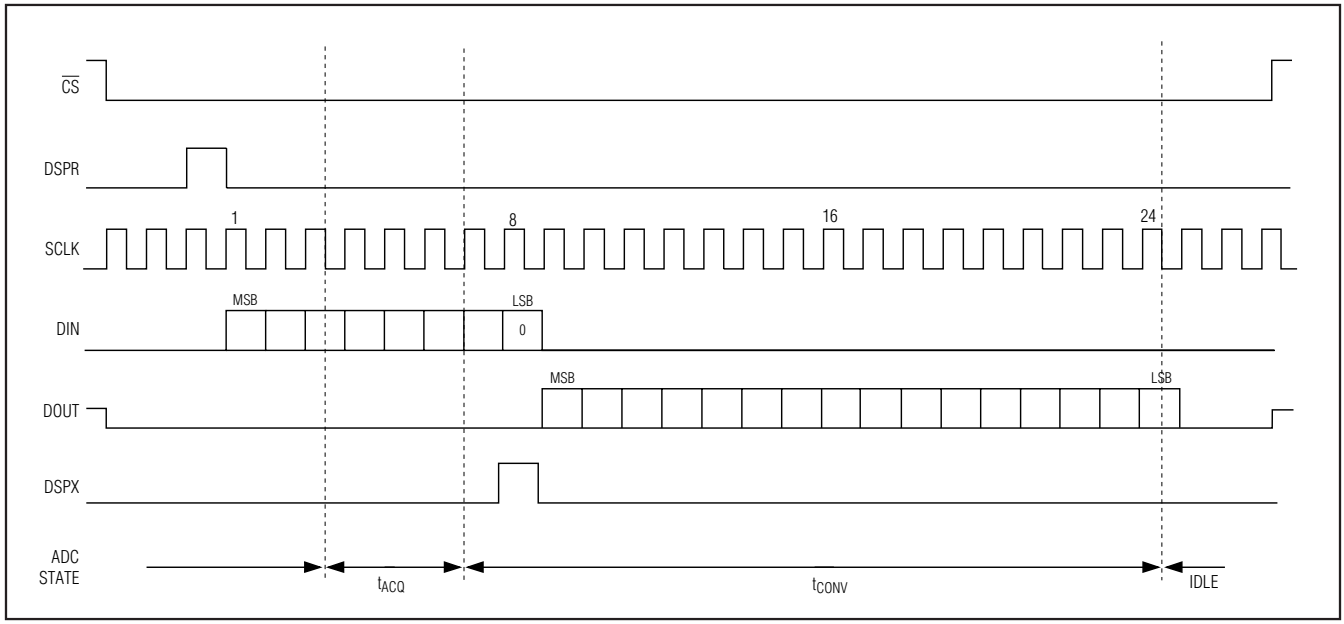

Figure 17. DSP External Clock Mode, 8-Bit Data-Transfer Mode, Conversion Timing (MAX1168 Only)

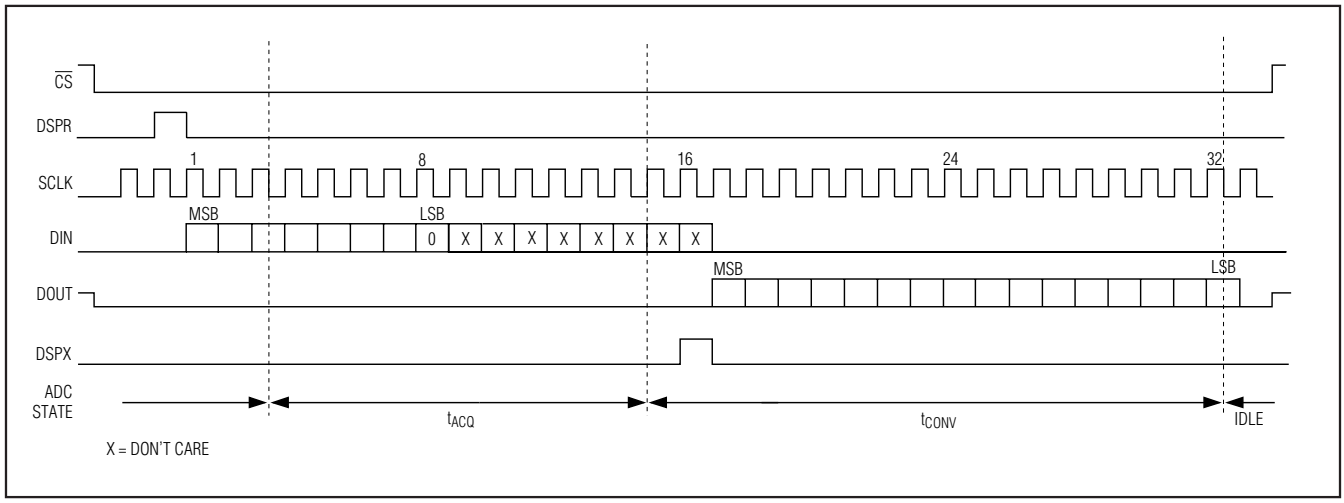

Figure 18. DSP External Clock Mode, 16-Bit Data-Transfer Mode, Conversion Timing (MAX1168 Only)

are shut down on the $\overline{EOC}$ high-to-low transition. Use the $\overline{EOC}$ high-to-low transition as the signal to restart the external clock (SCLK). To read the entire conversion result, 16 SCLK cycles are needed. Extra clock pulses, occurring after the conversion result has been clocked out and prior to the rising edge of $\overline{CS}$, cause the conversion result to be shifted out again. The MAX1168 internal-clock 16-bit-wide data-transfer mode requires 32 external clock cycles and 32 internal clock cycles for completion.

Force $\overline{CS}$ high after the conversion result is read. For maximum throughput, force $\overline{CS}$ low again to initiate the next conversion immediately after the specified minimum time (t_{CSW}). Forcing $\overline{CS}$ high in the middle of a conversion immediately aborts the conversion and places the MAX1168 in shutdown.

Scan mode allows multiple channels to be scanned consecutively or one channel to be scanned eight times. Scan mode can only be enabled when using the MAX1168 in internal clock mode. Enable scanning by

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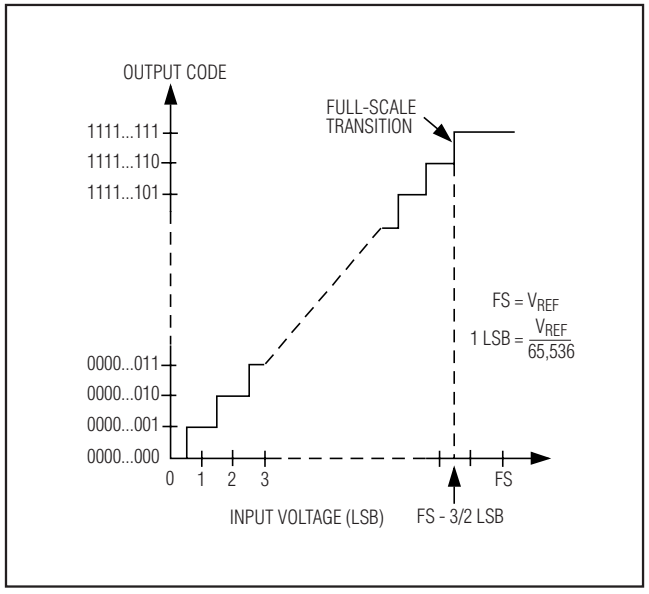

Figure 19. Unipolar Transfer Function, Full Scale (FS) = V_{REF}, Zero Scale (ZS) = GND

setting bits 4 and 3 in the command/configuration/control register (see Tables 3 and 4). In scan mode, conversion results are stored in memory until the completion of the last conversion in the sequence. Upon completion of the last conversion in the sequence, $\overline{EOC}$ transitions from high to low to indicate the end of the conversion and shuts down the internal oscillator. Use the $\overline{EOC}$ high-to-low transition as the signal to restart the external clock (SCLK). DOUT provides the conversion results in the same order as the channel conversion process. The MSB of the first conversion is available at DOUT on the falling edge of $\overline{EOC}$. Figure 15 shows the timing diagram for 16-bit-wide data transfer in scan mode.

DSP 8-Bit-Wide Data-Transfer Mode (External Clock Mode, MAX1168 Only)

Figure 16 shows the DSP-interface timing diagram. Logic low at DSPR on the falling edge of $\overline{CS}$ enables DSP interface mode. After the MAX1168 enters DSP mode, $\overline{CS}$ can remain low for the duration of the conversion process and each subsequent conversion. Drive DSEL low to select the 8-bit data-transfer mode. A sync pulse from the DSP at DSPR wakes the analog circuitry and allows SCLK to clock in data (Figure 17). The frame sync pulse alerts the MAX1168 that incoming data is about to be sent to DIN. Ensure the duty cycle on SCLK is between 45% and 55% when operating at 4.8MHz (the maximum clock frequency). For lower clock frequencies, ensure the minimum high and low times are at least 93ns. External clock mode conversions with SCLK rates less than 125kHz can reduce accuracy due to leakage of the sampling capacitor. The input data latches on the falling edge of SCLK. The command/configuration/control register starts reading data in on the falling edge of the first SCLK cycle immediately following the falling edge of the frame sync pulse and ends on the falling edge of the 8th SCLK cycle. The MAX1168 selects the proper channel for conversion on the falling edge of the 3rd clock cycle and begins acquisition. Acquisition continues until the rising edge of the 7th clock cycle. The MAX1168 samples the input on the rising edge of the 7th clock cycle. On the rising edge of the 8th clock cycle, the MAX1168 outputs a frame sync pulse at DSPX. The frame sync pulse alerts the DSP that the conversion results are about to be output at DOUT (MSB first) starting on the rising edge of the 9th clock pulse. To read the entire conversion result, 16 SCLK cycles are needed. Extra clock pulses, occurring after the conversion result has been clocked out and prior to the next rising edge of DSPR, cause zeros to be clocked out of DOUT. The MAX1168 external clock, DSP 8-bit-wide data-transfer mode requires 24 clock cycles to complete.

Begin a new conversion by sending a new frame sync pulse to DSPR followed by new configuration data. Send the new DSPR pulse immediately after reading the conversion result to realize maximum throughput. Sending a new frame sync pulse in the middle of a conversion immediately aborts the current conversion and begins a new one. A rising edge on $\overline{CS}$ in the middle of a conversion aborts the current conversion and places the MAX1168 in shutdown.

DSP 16-Bit-Wide Data-Transfer Mode (External Clock Mode, MAX1168 Only)

Figure 16 shows the DSP-interface timing diagram. Logic low at DSPR on the falling edge of $\overline{CS}$ enables DSP interface mode. After the MAX1168 enters DSP mode, $\overline{CS}$ can remain low for the duration of the conversion process and each subsequent conversion. The acquisition time is extended an extra eight SCLK cycles in the 16-bit-wide data-transfer mode. Drive DSEL high to select the 16-bit-wide data-transfer mode. A sync pulse from the DSP at DSPR wakes the analog circuitry and allows SCLK to clock in data (Figure 18). The frame sync pulse also alerts the MAX1168 that incoming data is about to be sent to DIN. Ensure the duty cycle on SCLK is between 45% and 55% when operating at 4.8MHz (the maximum clock frequency). For lower clock frequencies, ensure the minimum high and low times are at least 93ns. External-clock-mode conversions with SCLK rates less than 125kHz can reduce accuracy due to leakage of the sampling capacitor.

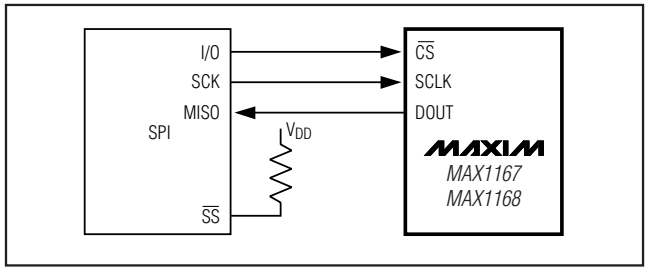

Figure 20a. SPI Connections

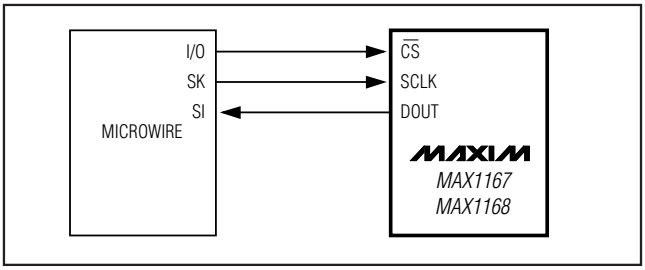

Figure 20b. MICROWIRE Connections

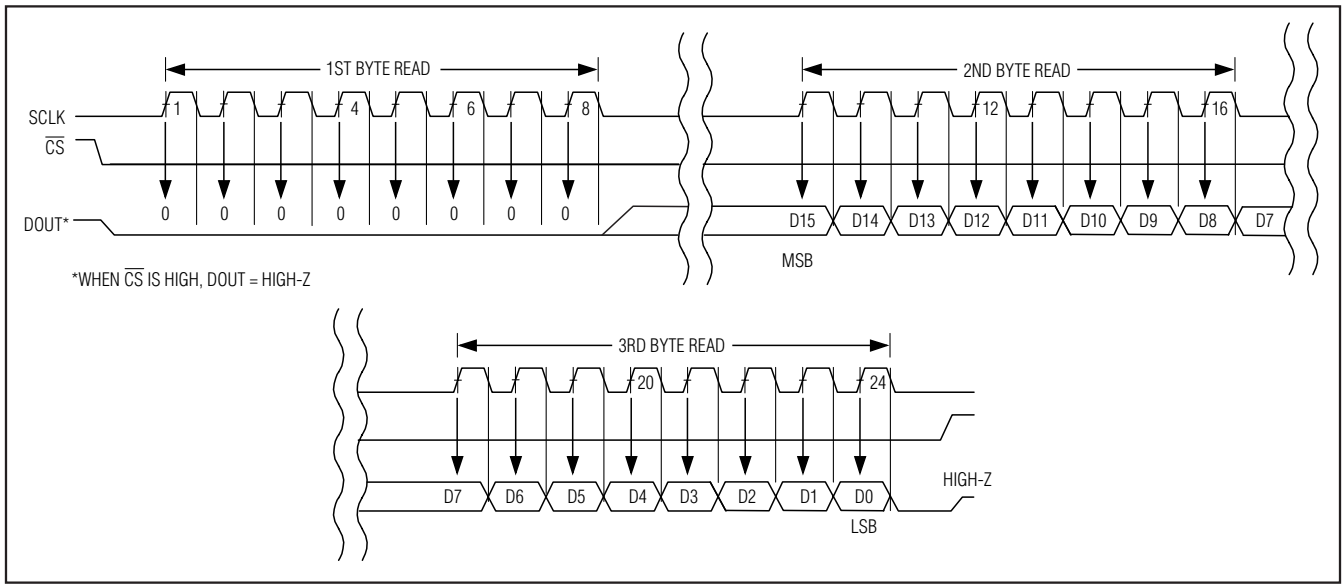

Figure 20c. SPI/MICROWIRE Interface Timing Sequence (CPOL = CPHA = 0)

The input data latches on the falling edge of SCLK. The command/configuration/control register starts reading data in on the falling edge of the first SCLK cycle immediately following the falling edge of the frame sync pulse and ends on the falling edge of the 16th SCLK cycle. The MAX1168 selects the proper channel for conversion on the falling edge of the 3rd clock cycle and begins acquisition. Acquisition continues until the rising edge of the 15th clock cycle. The MAX1168 samples the input on the rising edge of the 15th clock cycle. On the rising edge of the 16th clock cycle, the MAX1168 outputs a frame sync pulse at DSPX. The frame sync pulse alerts the DSP that the conversion results are about to be output at DOUT (MSB first) starting on the rising edge of the 17th clock pulse. To read the entire conversion result, 16 SCLK cycles are needed. Extra clock pulses, occurring after the conversion result has been clocked out and prior to the next rising edge of DSPR, cause zeros to be clocked out of DOUT. The MAX1168 external clock, DSP 16-bit-wide data-transfer mode requires 32 clock cycles to complete.

Begin a new conversion by sending a new frame sync pulse to DSPR followed by new configuration data. Send the new DSPR pulse immediately after reading the conversion result to realize maximum throughput. Sending a new frame sync pulse in the middle of a conversion immediately aborts the current conversion and begins a new one. A rising edge on $\overline{CS}$ in the middle of a conversion aborts the current conversion and places the MAX1168 in shutdown.

Output Coding and Transfer Function

The data output from the MAX1167/MAX1168 is straight binary. Figure 19 shows the nominal transfer function. Code transitions occur halfway between successive integer LSB values (V_{REF} = +4.096V, and 1 LSB = +62.5µV or 4.096V / 65,536V).

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Table 7. Detailed SSPCON Register Contents

CONTROL BIT		SETTINGS	SYNCHRONOUS SERIAL-PORT CONTROL REGISTER (SSPCON)
WCOL	BIT7	X	Write Collision Detection Bit
SSPOV	BIT6	X	Receive Overflow Detection Bit
SSPEN	BIT5	1	Synchronous Serial-Port Enable Bit: 0: Disables serial port and configures these pins as I/O port pins. 1: Enables serial port and configures SCK, SDO, and SCI pins as serial port pins.
CKP	BIT4	0	Clock Polarity Select Bit. CKP = 0 for SPI master-mode selection.
SSPM3	BIT3	0	Synchronous Serial-Port Mode Select Bit. Sets SPI master mode and selects $f_{CLK} = f_{OSC} / 16$.
SSPM2	BIT2	0	
SSPM1	BIT1	0	
SSPM0	BIT0	1	

X = Don't care.

Applications Information

Internal Reference

The internal bandgap reference provides a buffered +4.096V. Bypass REFCAP with a 0.1µF capacitor to AGND and REF with a 1µF capacitor to AGND. For best results, use low-ESR, X5R/X7R ceramic capacitors. Allow 5ms for the reference and buffer to wake up from full power-down (see Table 5).

External Reference

The MAX1167/MAX1168 accept an external reference with a voltage range between +3.8V and AV_{DD}. Connect the external reference directly to REF. Bypass REF to AGND with a 10µF capacitor. When not using a low-ESR bypass capacitor, use a 0.1µF ceramic capacitor in parallel with the 10µF capacitor. Noise on the reference degrades conversion accuracy.

The input impedance at REF is 37kΩ for DC currents. During a conversion, the external reference at REF must deliver 118µA of DC load current and have an output impedance of 10Ω or less.

For optimal performance, buffer the reference through an op amp and bypass the REF input. Consider the equivalent input noise ($40\mu V_{RMS}$) of the MAX1167/MAX1168 when choosing a reference.

Internal/External Oscillator

Select either an external (0.1MHz to 4.8MHz) or the internal 4MHz (typ) clock to perform conversions (Table 6). The external clock shifts data in and out of the MAX1167/MAX1168 in either clock mode.

When using the internal clock mode, the internal oscillator controls the acquisition and conversion processes, while the external oscillator shifts data in and out of the MAX1167/MAX1168. Turn off the external clock (SCLK) when the internal clock is on to realize lowest noise performance. The internal clock remains off in external clock mode.

Input Buffer

Most applications require an input-buffer amplifier to achieve 16-bit accuracy. The input amplifier must have a slew rate of at least 2V/µs and a unity-gain bandwidth of at least 10MHz to complete the required output-voltage change before the end of the acquisition time.

At the beginning of the acquisition, the internal sampling capacitor array connects to AIN_ (the amplifier input), causing some disturbance on the output of the buffer. Ensure the sampled voltage has settled before the end of the acquisition time.

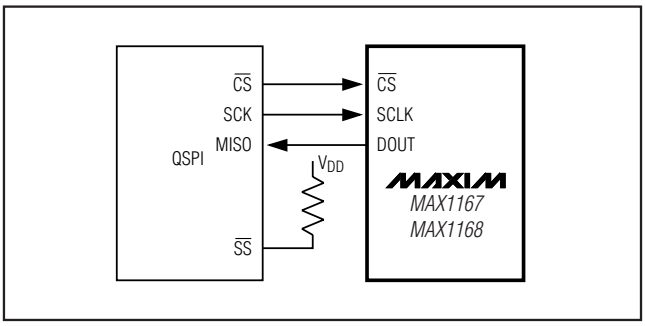

Figure 21a. QSPI Connections

Table 8. Detailed SSPSTAT Register Contents

CONTROL BIT		SETTINGS	SYNCHRONOUS SERIAL-PORT STATUS REGISTER (SSPSTAT)
SMP	BIT7	0	SPI Data-Input Sample Phase. Input data is sampled at the middle of the data output time.
CKE	BIT6	1	SPI Clock Edge-Select Bit. Data is transmitted on the rising edge of the serial clock.
D/A	BIT5	X	Data Address Bit
P	BIT4	X	Stop Bit
S	BIT3	X	Start Bit
R/W	BIT2	X	Read/Write Bit Information
UA	BIT1	X	Update Address
BF	BIT0	X	Buffer-Full Status Bit

X = Don't care.

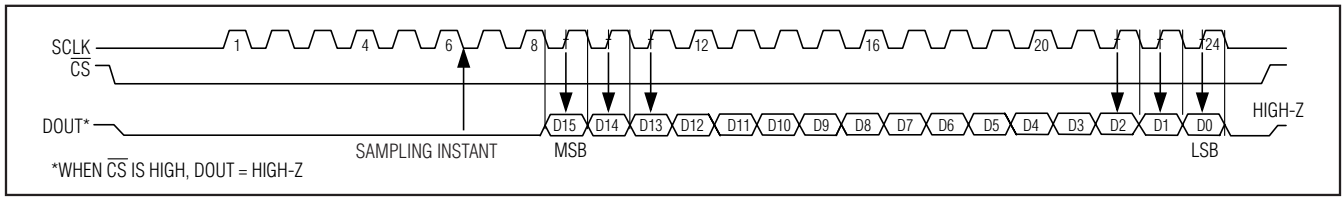

Figure 21b. QSPI Interface Timing Sequence (External Clock, 8-Bit Data Transfer, CPOL = CPHA = 0)

Digital Noise

Digital noise can couple to AIN_ and REF. The conversion clock (SCLK) and other digital signals active during input acquisition contribute noise to the conversion result. Noise signals, synchronous with the sampling interval, result in an effective input offset. Asynchronous signals produce random noise on the input, whose high-frequency components can be aliased into the frequency band of interest. Minimize noise by presenting a low impedance (at the frequencies contained in the noise signal) at the inputs. This requires bypassing AIN_ to AGND, or buffering the input with an amplifier that has a small-signal bandwidth of several megahertz (doing both is preferable). AIN has a typical bandwidth of 4MHz.

Distortion

Avoid degrading dynamic performance by choosing an amplifier with distortion much less than the total harmonic distortion of the MAX1167/MAX1168 at the frequencies of interest (THD = -100dB at 1kHz). If the chosen amplifier has insufficient common-mode rejection, which results in degraded THD performance, use the inverting configuration (positive input grounded) to eliminate errors from this source. Low-temperature-coefficient, gain-setting resistors reduce linearity errors caused by resistance changes due to self-heating. To reduce linearity errors due to finite amplifier gain, use amplifier circuits with sufficient loop gain at the frequencies of interest.

DC Accuracy

To improve DC accuracy, choose a buffer with an offset much less than the MAX1167/MAX1168s' offset (±10mV max for +5V supply), or whose offset can be trimmed while maintaining stability over the required temperature range.

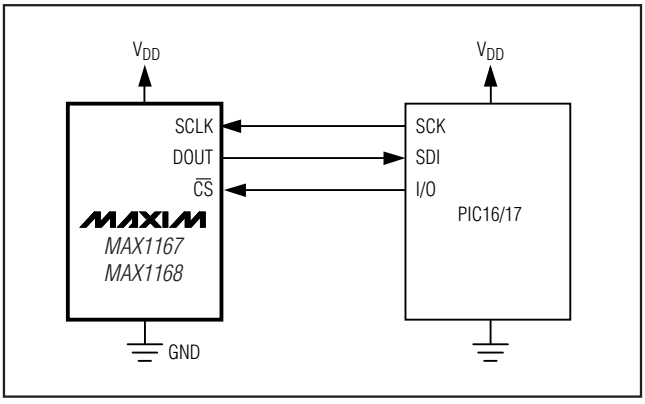

Figure 22a. SPI-Interface Connection for a PIC16/PIC17

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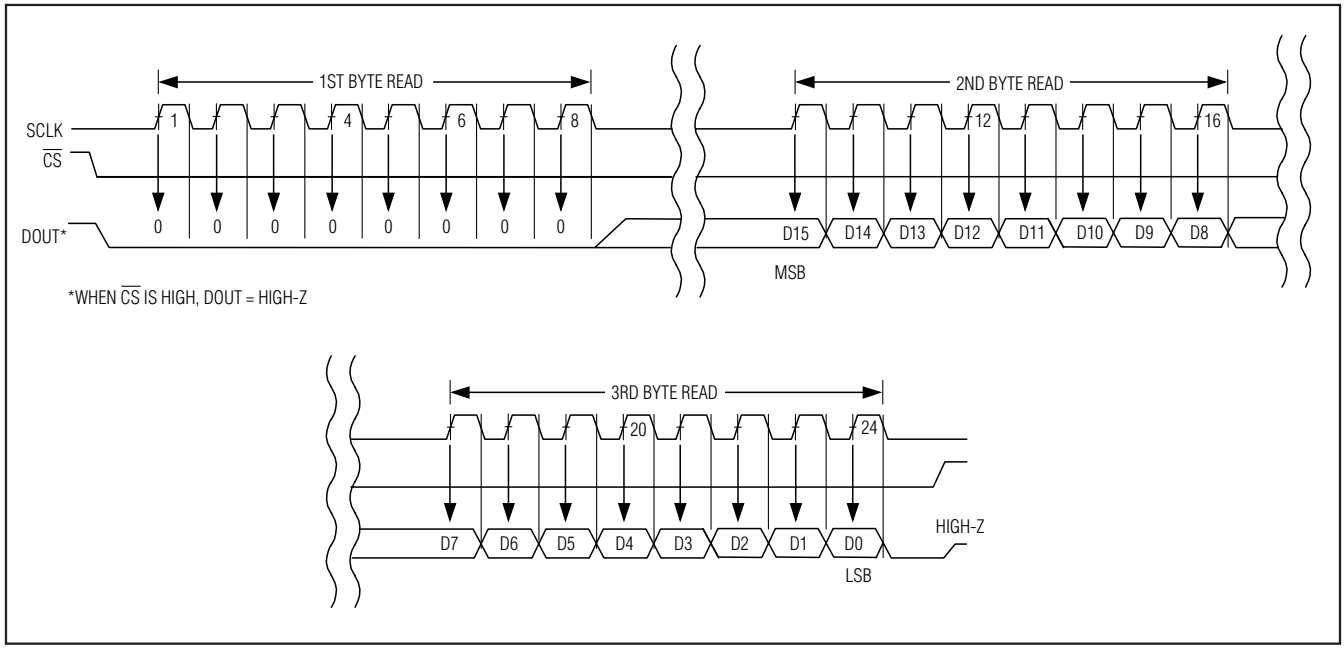

Figure 22b. SPI Interface Timing with PIC16/PIC17 in Master Mode (CKE = 1, CKP = 0, SMP = 0, SSPM3 - SSPM0 = 0001)

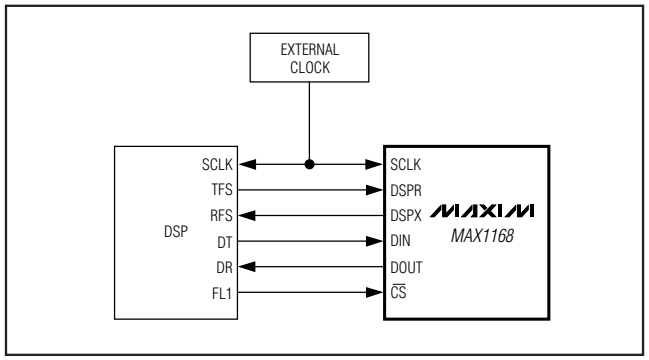

Figure 23. DSP Interface Connection

Serial Interfaces

SPI and MICROWIRE Interfaces

When using the SPI (Figure 20a) or MICROWIRE (Figure 20b) interfaces, set CPOL = 0 and CPHA = 0. Drive $\overline{CS}$ low to power on the MAX1167/MAX1168 before starting a conversion (Figure 20c). Three consecutive 8-bit-wide readings are necessary to obtain the entire 16-bit result from the ADC. DOUT data transitions on the serial clock's falling edge. The first 8-bit-wide data stream contains all leading zeros. The 2nd 8-bit-wide data stream contains the MSB through D6. The 3rd 8-bit-wide data stream contains D5 through D0 followed by S1 and S0.

QSPI Interface

Using the high-speed QSPI interface with CPOL = 0 and CPHA = 0, the MAX1167/MAX1168 support a maximum f_{SCLK} of 4.8MHz. Figure 21a shows the MAX1167/MAX1168 connected to a QSPI master, and Figure 21b shows the associated interface timing.

PIC16 with SSP Module and PIC17 Interface

The MAX1167/MAX1168 are compatible with a PIC16/PIC17 controller (µC), using the synchronous serial-port (SSP) module.

To establish SPI communication, connect the controller as shown in Figure 22a and configure the PIC16/PIC17 as system master by initializing its synchronous serial-port control register (SSPCON) and synchronous serial-port status register (SSPSTAT) to the bit patterns shown in Tables 7 and 8.

In SPI mode, the PIC16/PIC17 µCs allow 8 bits of data to be synchronously transmitted and received simultaneously. Three consecutive 8-bit-wide readings (Figure 22b) are necessary to obtain the entire 16-bit result from the ADC. DOUT data transitions on the serial clock's falling edge and is clocked into the µC on SCLK's rising edge. The first 8-bit-wide data stream contains all zeros. The 2nd 8-bit-wide data stream contains the MSB through D6. The 3rd 8-bit-wide data stream contains bits D5 through D0 followed by S1 and S0.

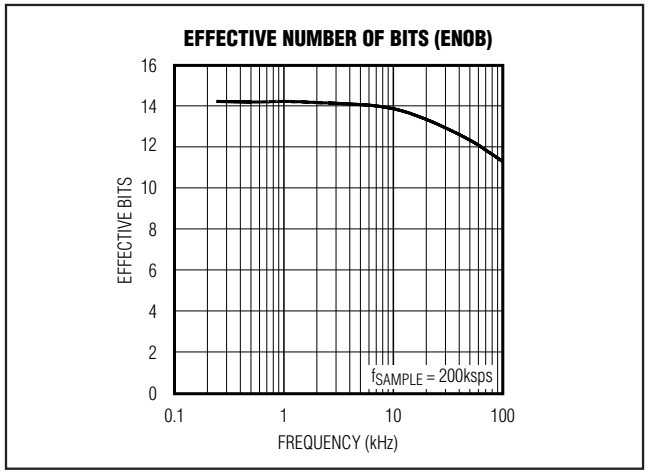

Figure 24. Effective Bits vs. Frequency

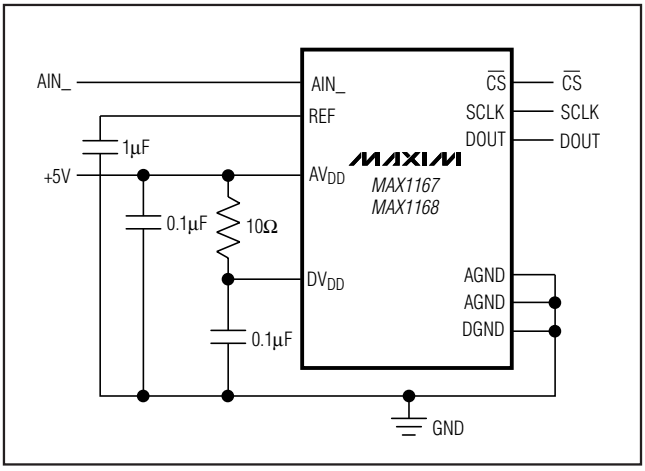

Figure 25. Powering AV_{DD} and DV_{DD} from a Single Supply

DSP Interface

The DSP mode of the MAX1168 only operates in external clock mode. Figure 23 shows a typical DSP interface connection to the MAX1168. Use the same oscillator as the DSP to provide the clock signal for the MAX1168. The DSP provides the falling edge at $\overline{CS}$ to wake the MAX1168. The MAX1168 detects the state of DSPR on the falling edge of $\overline{CS}$ (Figure 17). Logic low at DSPR places the MAX1168 in DSP mode. After the MAX1168 enters DSP mode, $\overline{CS}$ can be left low. A frame sync pulse from the DSP to DSPR initiates a conversion. The MAX1168 sends a frame sync pulse from DSPX to the DSP signaling that the MSB is available at DOUT. Send another frame sync pulse from the DSP to DSPR to begin the next conversion. The MAX1168 does not operate in scan mode when using DSP mode.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1167/MAX1168 are measured using the end-point method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step-width and the ideal value of ±1 LSB. A DNL error specification of ±1 LSB guarantees no missing codes and a monotonic transfer function.

Aperture Definitions

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between samples. Aperture delay (t_{AD}) is the time between the falling edge of the sampling clock and the instant when the actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals:

$$SINAD\ (dB) = 20 \times \log [Signal_{RMS} / (Noise + Distortion)_{RMS}]$$

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Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$ENOB = (SINAD - 1.76) / 6.02$$

Figure 24 shows the ENOB as a function of the MAX1167/MAX1168s' input frequency.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left[\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2)}}{V_1}\right]$$

where V_1 is the fundamental amplitude and V_2 through V_5 are the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest frequency component.

Supplies, Layout, Grounding, and Bypassing

Use printed circuit (PC) boards with separate analog and digital ground planes. Do not use wire-wrap boards. Connect the two ground planes together at the MAX1167/MAX1168 AGND terminal. Isolate the digital supply from the analog with a low-value resistor (10Ω) or ferrite bead when the analog and digital supplies come from the same source (Figure 25).

Constraints on sequencing the power supplies and inputs are as follows:

- Apply AGND before DGND.
- Apply AIN_ and REF after AV_{DD} and AGND are present.
- DV_{DD} is independent of the supply sequencing.

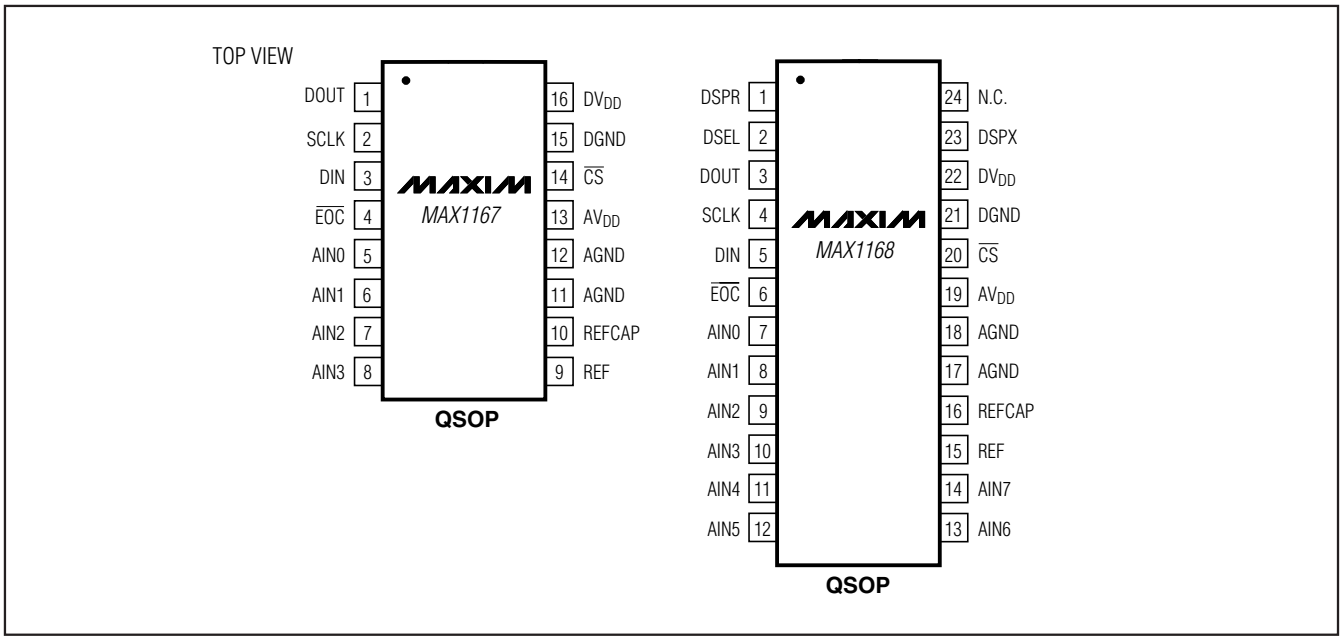
Ensure that digital return currents do not pass through the analog ground and that return-current paths are low impedance. A 5mA current flowing through a PC board ground trace impedance of only 0.05Ω creates an error voltage of about 250µV and a 4 LSB error with a +4.096V full-scale system.

The board layout should ensure that digital and analog signal lines are kept separate. Do not run analog and digital lines (especially the SCLK and DOUT) parallel to one another. If one must cross another, do so at right angles.

The ADC's high-speed comparator is sensitive to high-frequency noise on the AV_{DD} power supply. Bypass an excessively noisy supply to the analog ground plane with a 0.1µF capacitor in parallel with a 1µF to 10µF low-ESR capacitor. Keep capacitor leads short for best supply-noise rejection.

Multichannel, 16-Bit, 200ksps Analog-to-Digital Converters

Pin Configurations



Chip Information

TRANSISTOR COUNT: 20,760

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 QSOP	E16-1	21-0055
24 QSOP	E24-1	

Multichannel, 16-Bit, 200ksps Analog-to-Digital Converters

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/03	Initial release.	—
1	10/09	Changed 2.9mA at 200ksps to 3.6mA at 200ksps, 1.45mA at 100ksps to 1.85mA at 100ksps, and 145µA at 10ksps to 185µA to 10ksps in the *General Description* and *Features* sections.	1
		Removed the ±1.2 INL LSB and ±2 INL LSB packages from the *Ordering Information* table.	1, 29
		Updated the *Electrical Characteristics* table to include the reference buffer and GBD at -40°C.	2–6

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