



**THE DATASHEET OF
MAX11047ETN+T**



EVALUATION KIT
AVAILABLE

MAXIM

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

General Description

The MAX11047/MAX11048/MAX11049 and MAX11057/MAX11058/MAX11059 16-bit/14-bit ADCs offer 4, 6, or 8 independent input channels. Featuring independent track and hold (T/H) and SAR circuitry, these parts provide simultaneous sampling at 250ksps for each channel.

The devices accept a 0 to +5V input. All inputs are overrange protected with internal $\pm 20\text{mA}$ input clamps providing overrange protection with a simple external resistor. Other features include a 4MHz T/H input bandwidth, internal clock, and internal or external reference. A 20MHz, bidirectional, parallel interface provides the conversion results and accepts digital configuration inputs.

The devices operate with a 4.75V to 5.25V analog supply and a separate flexible 2.7V to 5.25V digital supply for interfacing with the host without a level shifter. The MAX11047/MAX11048/MAX11049 are available in a 56-pin TQFN and 64-pin TQFP packages while the MAX11057/MAX11058/MAX11059 are available in TQFP only. All devices operate over the extended -40°C to $+85^{\circ}\text{C}$ temperature range.

Applications

Automatic Test Equipment
Power-Factor Monitoring and Correction
Power-Grid Protection
Multiphase Motor Control
Vibration and Waveform Analysis

Ordering Information

| PART | PIN-PACKAGE | CHANNELS |
|--------------|-------------|----------|
| MAX11047ETN+ | 56 TQFN-EP* | 4 |
| MAX11047ECB+ | 64 TQFP-EP* | 4 |
| MAX11048ETN+ | 56 TQFN-EP* | 6 |
| MAX11048ECB+ | 64 TQFP-EP* | 6 |
| MAX11049ETN+ | 56 TQFN-EP* | 8 |
| MAX11049ECB+ | 64 TQFP-EP* | 8 |
| MAX11057ECB+ | 64 TQFP-EP* | 4 |
| MAX11058ECB+ | 64 TQFP-EP* | 6 |
| MAX11059ECB+ | 64 TQFP-EP* | 8 |

Note: All devices are specified over the -40°C to $+85^{\circ}\text{C}$ operating temperature range.

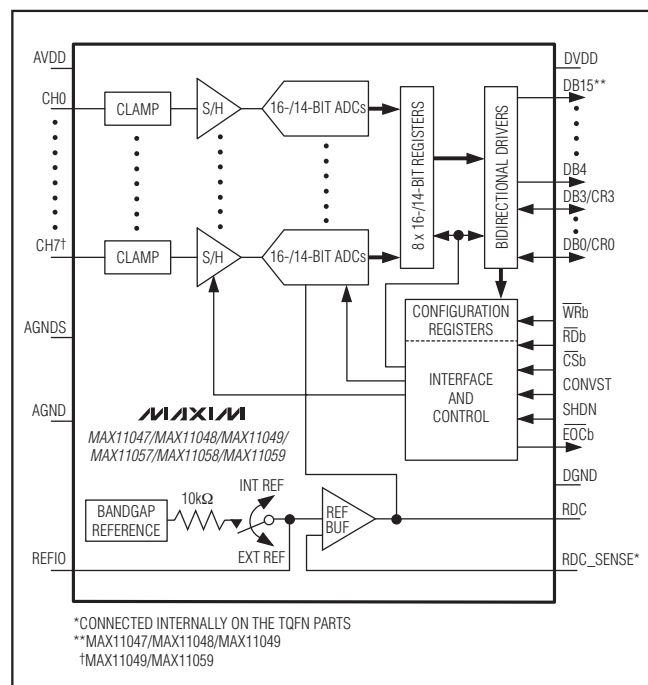
+ Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Features

- ◆ 16-Bit ADC (MAX11047/MAX11048/MAX11049)
- ◆ 14-Bit ADC (MAX11057/MAX11058/MAX11059)
- ◆ 4-Channel ADC (MAX11047/MAX11057)
- ◆ 6-Channel ADC (MAX11048/MAX11058)
- ◆ 8-Channel ADC (MAX11049/MAX11059)
- ◆ Single Analog and Digital Supply
- ◆ High-Impedance Inputs Up to $1\text{G}\Omega$
- ◆ On-Chip T/H Circuit for Each Channel
- ◆ Fast $3\mu\text{s}$ Conversion Time
- ◆ High Throughput: 250ksps for Each Channel
- ◆ 16-/14-Bit, High-Speed, Parallel Interface
- ◆ Internal Clocked Conversions
- ◆ 10ns Aperture Delay
- ◆ 100ps Channel-to-Channel T/H Matching
- ◆ Low Drift, Accurate 4.096V Internal Reference Providing an Input Range of 0 to 5V
- ◆ External Reference Range of 3.0V to 4.25V, Allowing Full-Scale Input Ranges of +3.7V to +5.2V
- ◆ 56-Pin TQFN (8mm x 8mm) and 64-Pin TQFP (10mm x 10mm) Packages
- ◆ Evaluation Kit Available (MAX11046EVKIT+)

Functional Diagram



MAX11047-MAX11049/MAX11057-MAX11059

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

ABSOLUTE MAXIMUM RATINGS

| | |
|---|--|
| AVDD to AGND | -0.3V to +6V |
| DVDD to AGND and DGND | -0.3V to +6V |
| DGND to AGND | -0.3V to +0.3V |
| AGNDS to AGND | -0.3V to +0.3V |
| CHO-CH7 to AGND | -2.5V to +7.5V |
| REFIO, RDC to AGND | -0.3V to the lower of (AVDD + 0.3V) and +6V |
| \overline{EOC} , \overline{WR} , \overline{RD} , \overline{CS} , CONVST to AGND | -0.3V to the lower of (DVDD + 0.3V) and +6V |
| DB0-DB15 to AGND | -0.3V to the lower of (DVDD + 0.3V) and +6V |

| | |
|--|-----------------|
| Maximum Current into Any Pin Except AVDD, DVDD, AGND, DGND | ±50mA |
| Continuous Power Dissipation (T _A = +70°C) | |
| 56-Pin TQFN (derated 47.6mW/°C above +70°C) | 3809.5mW |
| 64-Pin TQFP (derate 43.5mW/°C above +70°C) | 3478mW |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Soldering Temperature (reflow) | +260°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = +2.7V to 5.25V, V_{AGNDS} = V_{AGND} = V_{DGND} = 0V, V_{REFIO} = internal reference, C_{RDC} = 4 x 33µF, C_{REFIO} = 0.1µF, C_{AVDD} = 4 x 0.1µF || 10µF, C_{DVDD} = 3 x 0.1µF || 10µF; all digital inputs at DVDD or DGND, unless otherwise noted. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------------|--------|--|------|--------|--------|--------|
| STATIC PERFORMANCE (Note 1) | | | | | | |
| Resolution | N | MAX11047/MAX11048/MAX11049 | 16 | | | Bits |
| | | MAX11057/MAX11058/MAX11059 | 14 | | | |
| Integral Nonlinearity | INL | MAX11047/MAX11048/MAX11049 | -2 | ±0.65 | +2 | LSB |
| | | MAX11057/MAX11058/MAX11059 | -0.9 | ±0.2 | +0.9 | |
| Differential Nonlinearity | DNL | MAX11047/MAX11048/MAX11049 | > -1 | ±0.7 | < +1.2 | LSB |
| | | MAX11057/MAX11058/MAX11059 | -0.6 | ±0.2 | +0.7 | |
| No Missing Codes | | MAX11047/MAX11048/MAX11049 | 16 | | | Bits |
| | | MAX11057/MAX11058/MAX11059 | 14 | | | |
| Offset Error | | | | ±0.001 | ±0.012 | %FSR |
| Offset Temperature Coefficient | | | | ±0.8 | | µV/°C |
| Channel Offset Matching | | | | | ±0.01 | %FSR |
| Gain Error | | | | | ±0.012 | %FSR |
| Positive Full-Scale Error | | | | | ±0.017 | %FSR |
| Positive Full-Scale Error Matching | | | | | ±0.01 | %FSR |
| Channel Gain-Error Matching | | Between all channels | | | ±0.01 | %FSR |
| Gain Temperature Coefficient | | | | ±0.6 | | ppm/°C |
| DYNAMIC PERFORMANCE | | | | | | |
| Signal-to-Noise Ratio | SNR | MAX11047/MAX11048/MAX11049, f _{IN} = 10kHz, full-scale input | 90.7 | 92.3 | | dB |
| | | MAX11057/MAX11058/MAX11059, f _{IN} = 10kHz, full-scale input | 84.5 | 85.3 | | |

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

MAX11047-MAX11049/MAX11057-MAX11059

ELECTRICAL CHARACTERISTICS (continued)

V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = +2.7V to 5.25V, V_{AGNDS} = V_{AGND} = V_{DGND} = 0V, V_{REFIO} = internal reference, C_{RD} = 4 x 33μF, C_{REFIO} = 0.1μF, C_{AVDD} = 4 x 0.1μF || 10μF, C_{DVDD} = 3 x 0.1μF || 10μF; all digital inputs at DVDD or DGND, unless otherwise noted. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------|--|-------|-------|---------------------------|--------|
| Signal-to-Noise and Distortion Ratio | SINAD | MAX11047/MAX11048/MAX11049, f _{IN} = 10kHz, full-scale input | 90.5 | 92 | | dB |
| | | MAX11057/MAX11058/MAX11059, f _{IN} = 10kHz, full-scale input | 84.5 | 85.2 | | |
| Spurious-Free Dynamic Range | SFDR | f _{IN} = 10kHz, full-scale input | 98 | 108 | | dB |
| | | | 95 | 108 | | |
| Total Harmonic Distortion | THD | f _{IN} = 10kHz, full-scale input | | -108 | -98 | dB |
| | | | | -108 | -95 | |
| Channel-to-Channel Crosstalk | | f _{IN} = 60Hz, full scale and ground on adjacent channel (Note 2) | | -126 | -100 | dB |
| ANALOG INPUTS (CH0-CH7) | | | | | | |
| Input Voltage Range | | (Note 3) | 0 | | 1.22 x V _{REFIO} | V |
| Input Leakage Current | | | -1 | | +1 | μA |
| Input Capacitance | | | | 15 | | pF |
| Input-Clamp Protection Current | | Each input simultaneously | -20 | | +20 | mA |
| TRACK AND HOLD | | | | | | |
| Throughput Rate | | Per channel | | | 250 | ksps |
| Acquisition Time | t _{ACQ} | | 1 | | | μs |
| Full-Power Bandwidth | | -3dB point | | 4 | | MHz |
| | | -0.1dB point | | > 0.2 | | |
| Aperture Delay | | | | 10 | | ns |
| Aperture-Delay Matching | | | | 100 | | ps |
| Aperture Jitter | | | | 50 | | psRMS |
| INTERNAL REFERENCE | | | | | | |
| REFIO Voltage | V _{REF} | | 4.080 | 4.096 | 4.112 | V |
| REFIO Temperature Coefficient | | | | ±4 | | ppm/°C |
| EXTERNAL REFERENCE | | | | | | |
| Input Current | | | -10 | | +10 | μA |
| REF Voltage Input Range | V _{REF} | | 3.00 | | 4.25 | V |
| REF Input Capacitance | | | | 15 | | pF |
| DIGITAL INPUTS (CR0-CR3, RD, WR, CS, CONVST) | | | | | | |
| Input-Voltage High | V _{IH} | V _{DVDD} = 2.7V to 5.25V | 2 | | | V |
| Input-Voltage Low | V _{IL} | V _{DVDD} = 2.7V to 5.25V | | | 0.8 | V |
| Input Capacitance | C _{IN} | | | 10 | | pF |
| Input Current | I _{IN} | V _{IN} = 0 or V _{DVDD} | | | ±10 | μA |

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

ELECTRICAL CHARACTERISTICS (continued)

$V_{AVDD} = 4.75V$ to $5.25V$, $V_{DVDD} = +2.7V$ to $5.25V$, $V_{AGNDS} = V_{AGND} = V_{DGND} = 0V$, V_{REFIO} = internal reference, $C_{RDC} = 4 \times 33\mu F$, $C_{REFIO} = 0.1\mu F$, $C_{AVDD} = 4 \times 0.1\mu F$ || $10\mu F$, $C_{DVDD} = 3 \times 0.1\mu F$ || $10\mu F$; all digital inputs at DVDD or DGND, unless otherwise noted. $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------|--|------------------|-----------|------|---------|
| DIGITAL OUTPUTS (DB0–DB15, \overline{EOC}) | | | | | | |
| Output-Voltage High | V_{OH} | $I_{SOURCE} = 1.2mA$ | $V_{DVDD} - 0.4$ | | | V |
| Output-Voltage Low | V_{OL} | $I_{SINK} = 1mA$ | | | 0.4 | V |
| Three-State Leakage Current | | DB0–DB15, $V_{RD} \geq V_{IH}$ or $\overline{VCS} \geq V_{IH}$ | | | 10 | μA |
| Three-State Output Capacitance | | DB0–DB15, $V_{RD} \geq V_{IH}$ or $\overline{VCS} \geq V_{IH}$ | 15 | | | pF |
| POWER SUPPLIES (MAX11047/MAX11057) | | | | | | |
| Analog Supply Voltage | AVDD | | 4.75 | | 5.25 | V |
| Digital Supply Voltage | DVDD | | 2.70 | | 5.25 | V |
| Analog Supply Current | I_{AVDD} | | | | 25 | mA |
| Digital Supply Current | I_{DVDD} | $V_{DVDD} = 3.3V$ (Note 4) | | | 5.5 | mA |
| Shutdown Current | | For DVDD | | | 10 | μA |
| Shutdown Current | | For AVDD | | | 10 | μA |
| Power-Supply Rejection | PSR | $V_{AVDD} = 4.9V$ to $5.1V$ (Note 5) | MAX11047 | ± 1.2 | | LSB |
| | | | MAX11057 | ± 0.3 | | |
| POWER SUPPLIES (MAX11048/MAX11058) | | | | | | |
| Analog Supply Voltage | AVDD | | 4.75 | | 5.25 | V |
| Digital Supply Voltage | DVDD | | 2.70 | | 5.25 | V |
| Analog Supply Current | I_{AVDD} | | | | 32 | mA |
| Digital Supply Current | I_{DVDD} | $V_{DVDD} = 3.3V$ (Note 4) | | | 6.5 | mA |
| Shutdown Current | | For DVDD | | | 10 | μA |
| Shutdown Current | | For AVDD | | | 10 | μA |
| Power-Supply Rejection | PSR | $V_{AVDD} = 4.9V$ to $5.1V$ (Note 5) | MAX11048 | ± 1.2 | | LSB |
| | | | MAX11058 | ± 0.3 | | |
| POWER SUPPLIES (MAX11049/MAX11059) | | | | | | |
| Analog Supply Voltage | AVDD | | 4.75 | | 5.25 | V |
| Digital Supply Voltage | DVDD | | 2.70 | | 5.25 | V |
| Analog Supply Current | I_{AVDD} | | | | 39 | mA |
| Digital Supply Current | I_{DVDD} | $V_{DVDD} = 3.3V$ (Note 4) | | | 7 | mA |
| Shutdown Current | | For DVDD | | | 10 | μA |
| Shutdown Current | | For AVDD | | | 10 | μA |
| Power-Supply Rejection | PSR | $V_{AVDD} = 4.9V$ to $5.1V$ (Note 5) | MAX11049 | ± 1.2 | | LSB |
| | | | MAX11059 | ± 0.3 | | |
| TIMING CHARACTERISTICS (Note 4) | | | | | | |
| CONVST Rise to \overline{EOC} Fall | t_{CON} | Conversion time (Note 6) | | | 3 | μs |
| Acquisition Time | t_{ACQ} | | 1 | | | μs |
| \overline{CS} Rise to CONVST Rise | t_Q | Sample quiet time (Note 6) | 500 | | | ns |

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

MAX11047-MAX11049/MAX11057-MAX11059

ELECTRICAL CHARACTERISTICS (continued)

$V_{AVDD} = 4.75V$ to $5.25V$, $V_{DVDD} = +2.7V$ to $5.25V$, $V_{AGNDS} = V_{AGND} = V_{DGND} = 0V$, $V_{REFIO} =$ internal reference, $C_{RDC} = 4 \times 33\mu F$, $C_{REFIO} = 0.1\mu F$, $C_{AVDD} = 4 \times 0.1\mu F \parallel 10\mu F$, $C_{DVDD} = 3 \times 0.1\mu F \parallel 10\mu F$; all digital inputs at $DVDD$ or $DGND$, unless otherwise noted. $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|----------|----------------------------------|-----|-----|-----|-------|
| CONVST Rise to EOC Rise | t_0 | | | 65 | 140 | ns |
| EOC Fall to CONVST Fall | t_1 | CONVST mode B0 = 0 only (Note 7) | 0 | | | ns |
| CONVST Low Time | t_2 | CONVST mode B0 = 1 only | 20 | | | ns |
| CS Fall to WR Fall | t_3 | | 0 | | | ns |
| WR Low Time | t_4 | | 20 | | | ns |
| CS Rise to WR Rise | t_5 | | 0 | | | ns |
| Input Data Setup Time | t_6 | | 10 | | | ns |
| Input Data Hold Time | t_7 | | 0 | | | ns |
| CS Fall to RD Fall | t_8 | | 0 | | | ns |
| RD Low Time | t_9 | | 30 | | | ns |
| RD Rise to CS Rise | t_{10} | | 0 | | | ns |
| RD High Time | t_{11} | | 10 | | | ns |
| RD Fall to Data Valid | t_{12} | | | | 35 | ns |
| RD Rise to Data Hold Time | t_{13} | (Note 7) | 5 | | | ns |

Note 1: See the *Definitions* section at the end of the data sheet.

Note 2: Tested with alternating channels modulated at full scale and ground.

Note 3: See the *Input Range and Protection* section.

Note 4: $C_{LOAD} = 30pF$ on $DB0-DB15$ and \overline{EOC} . Inputs ($CH0-CH7$) alternate between full scale and zero scale. $f_{CONV} = 250ksps$. All data is read out.

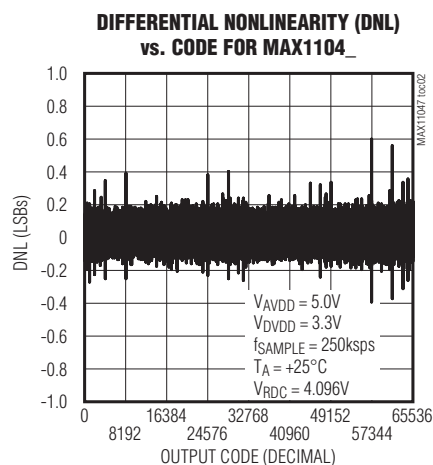
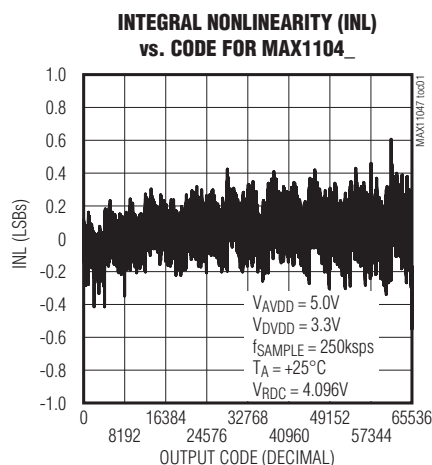
Note 5: Defined as the change in positive full scale caused by a $\pm 2\%$ variation in the nominal supply voltage.

Note 6: It is recommended that \overline{RD} , \overline{WR} , and \overline{CS} are kept high for the quiet time (t_Q) and conversion time (t_{CON}).

Note 7: Guaranteed by design.

Typical Operating Characteristics

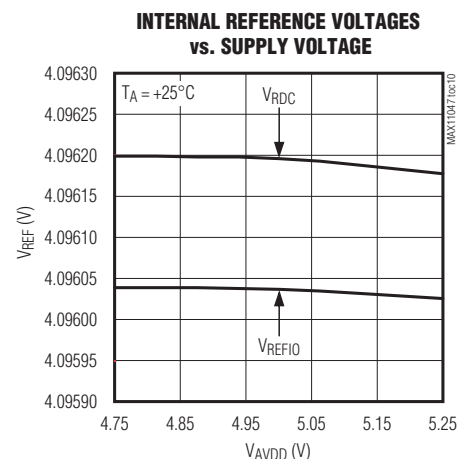
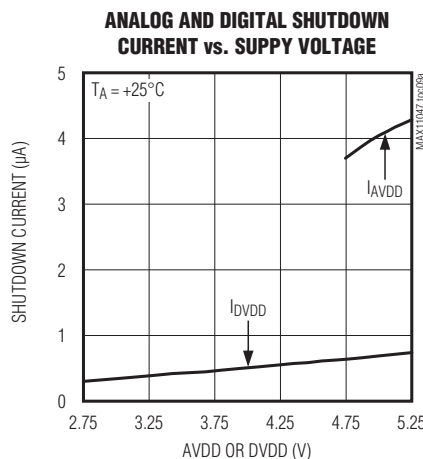
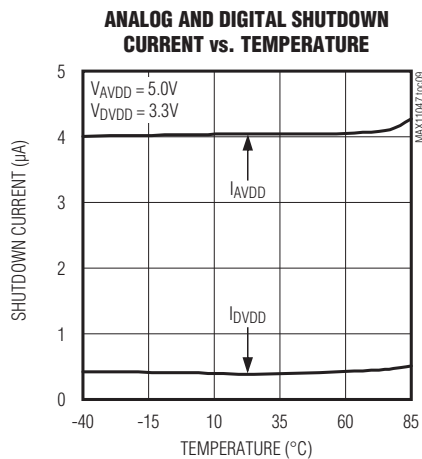
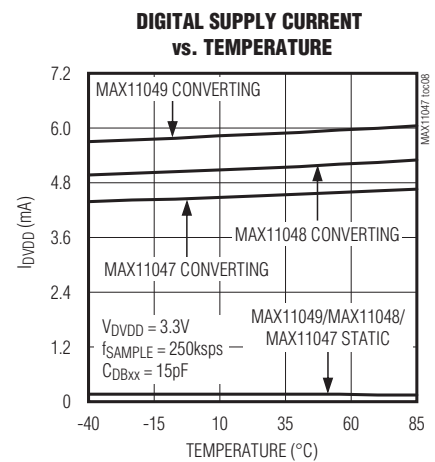
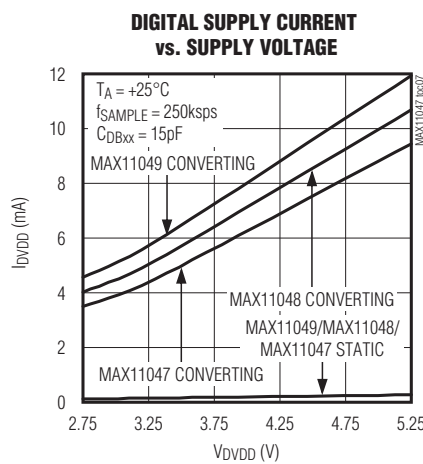
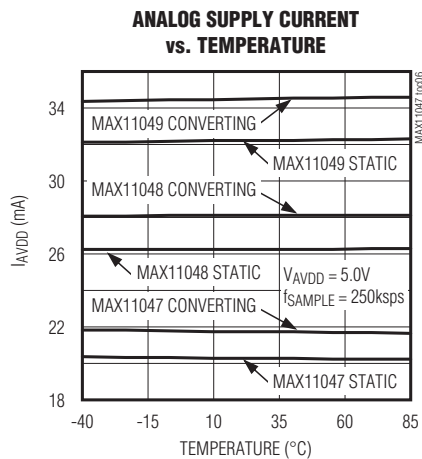
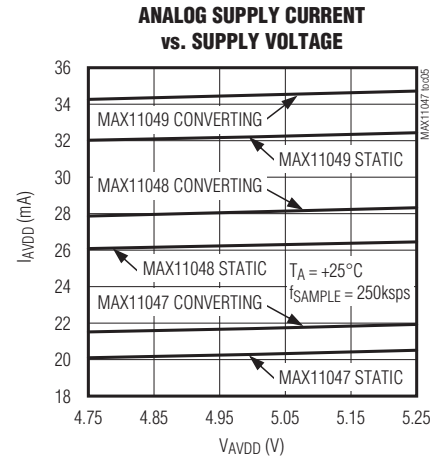
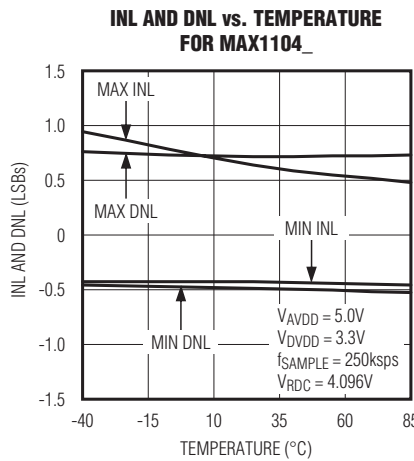
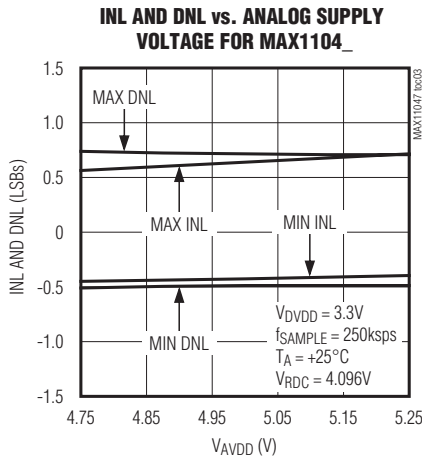
($V_{AVDD} = 5V$, $V_{DVDD} = 3.3V$, $T_A = +25^\circ C$, $f_{SAMPLE} = 250ksps$, internal reference, unless otherwise noted.)



4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

Typical Operating Characteristics (continued)

($V_{AVDD} = 5V$, $V_{DVDD} = 3.3V$, $T_A = +25^\circ C$, $f_{SAMPLE} = 250ksps$, internal reference, unless otherwise noted.)

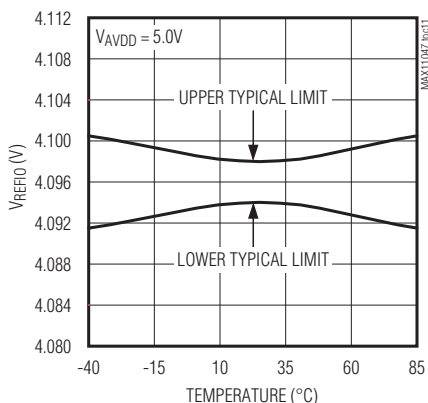


4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

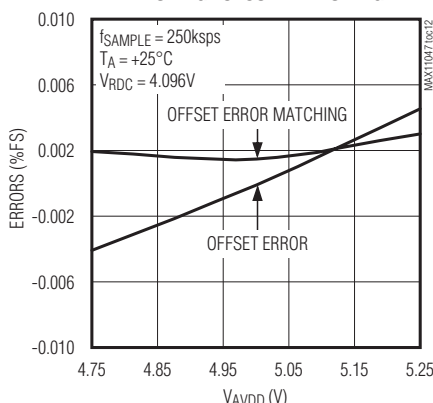
Typical Operating Characteristics (continued)

($V_{AVDD} = 5V$, $V_{DVDD} = 3.3V$, $T_A = +25^\circ C$, $f_{SAMPLE} = 250ksps$, internal reference, unless otherwise noted.)

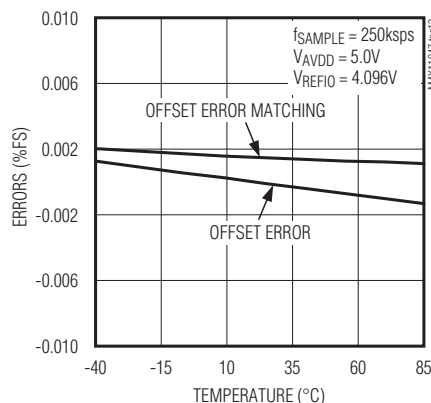
INTERNAL REFERENCE VOLTAGES vs. TEMPERATURE



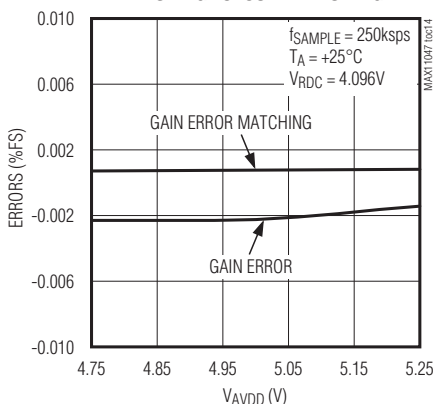
OFFSET ERROR AND OFFSET ERROR MATCHING vs. SUPPLY VOLTAGE



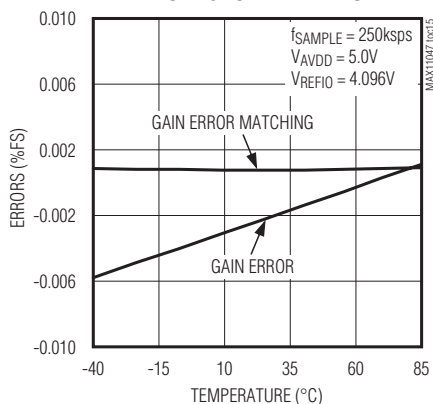
OFFSET ERROR AND OFFSET ERROR MATCHING vs. TEMPERATURE



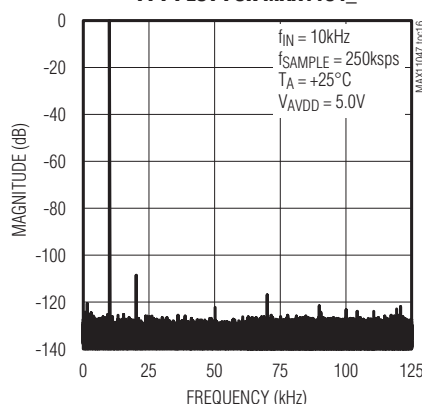
GAIN ERROR AND GAIN ERROR MATCHING vs. SUPPLY VOLTAGE



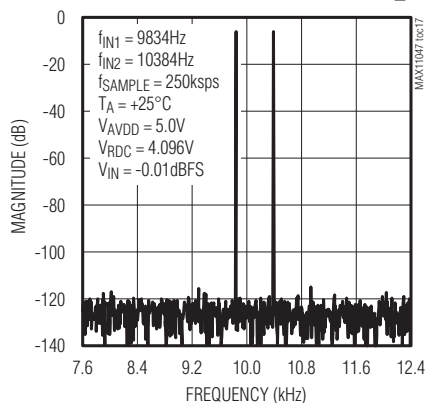
GAIN ERROR AND GAIN ERROR MATCHING vs. TEMPERATURE



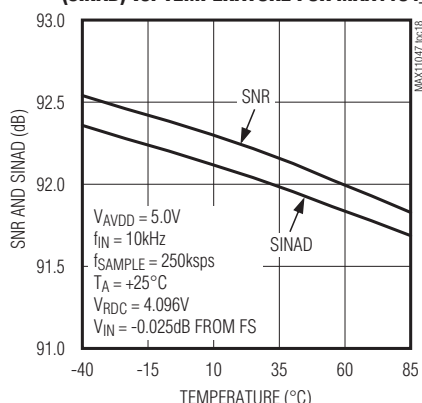
FFT PLOT FOR MAX1104_



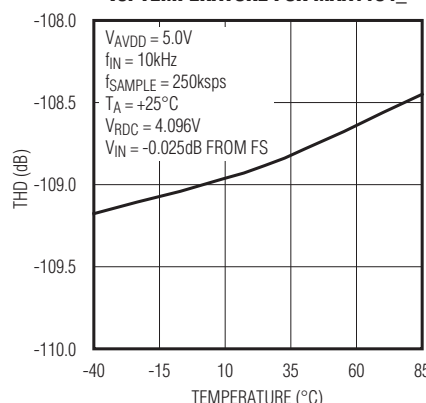
TWO-TONE IMD PLOT FOR MAX1104_



SIGNAL-TO-NOISE RATIO (SNR) AND SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD) vs. TEMPERATURE FOR MAX1104_



TOTAL HARMONIC DISTORTION (THD) vs. TEMPERATURE FOR MAX1104_



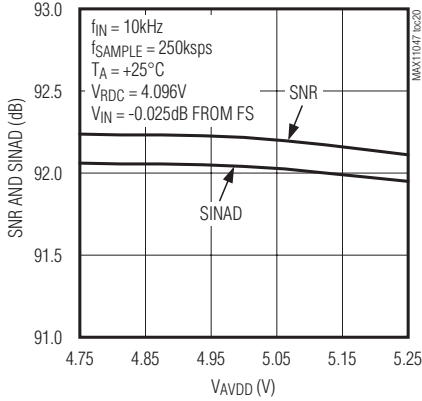
MAX11047-MAX11049/MAX11057-MAX11059

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

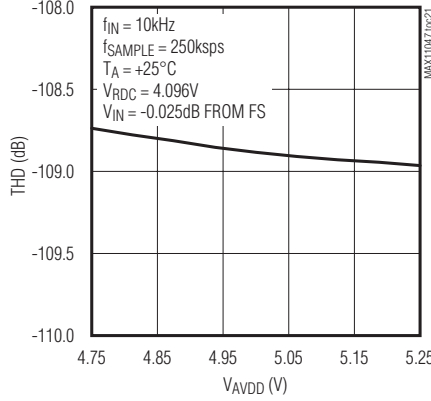
Typical Operating Characteristics (continued)

($V_{AVDD} = 5V$, $V_{DVDD} = 3.3V$, $T_A = +25^\circ C$, $f_{SAMPLE} = 250ksps$, internal reference, unless otherwise noted.)

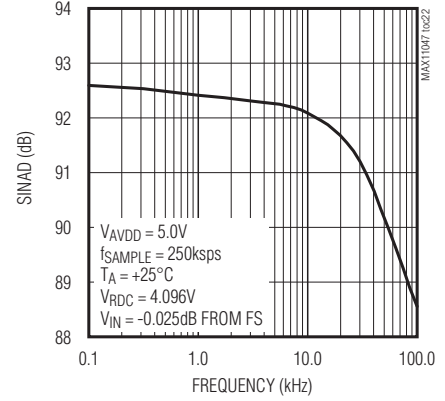
SNR AND SINAD vs. ANALOG SUPPLY VOLTAGE FOR MAX1104_



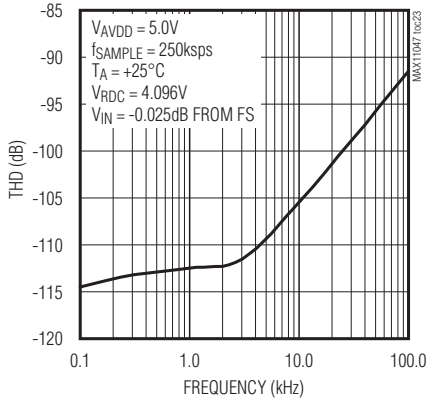
THD vs. ANALOG SUPPLY VOLTAGE FOR MAX1104_



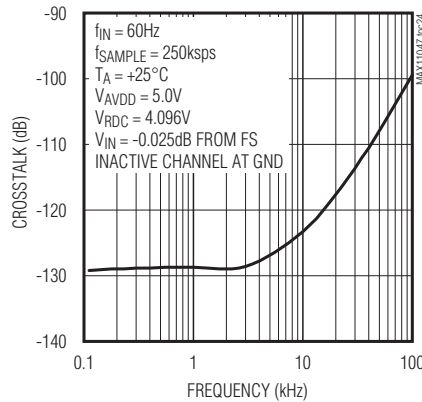
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD) vs. FREQUENCY FOR MAX1104_



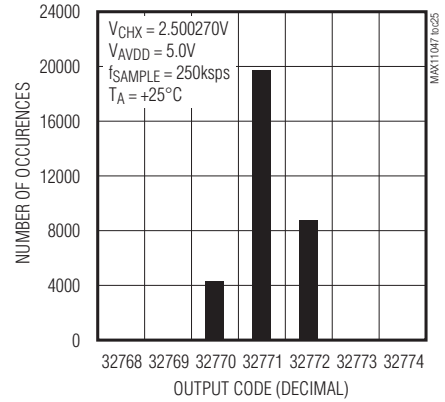
THD vs. INPUT FREQUENCY FOR MAX1104_



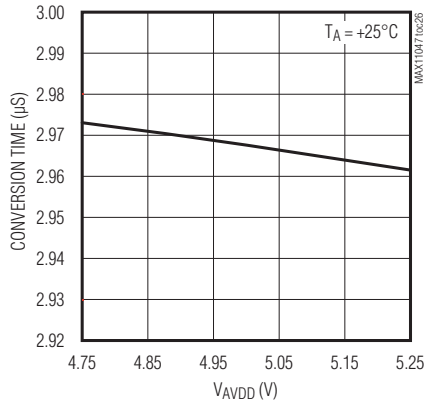
CROSSTALK vs. FREQUENCY



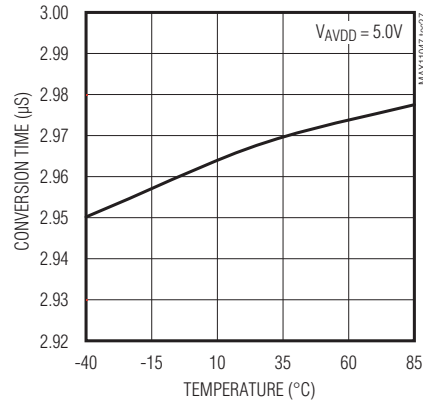
OUTPUT NOISE HISTOGRAM WITH INPUT CONNECTED TO 2.5V FOR MAX1104_



CONVERSION TIME vs. ANALOG SUPPLY VOLTAGE



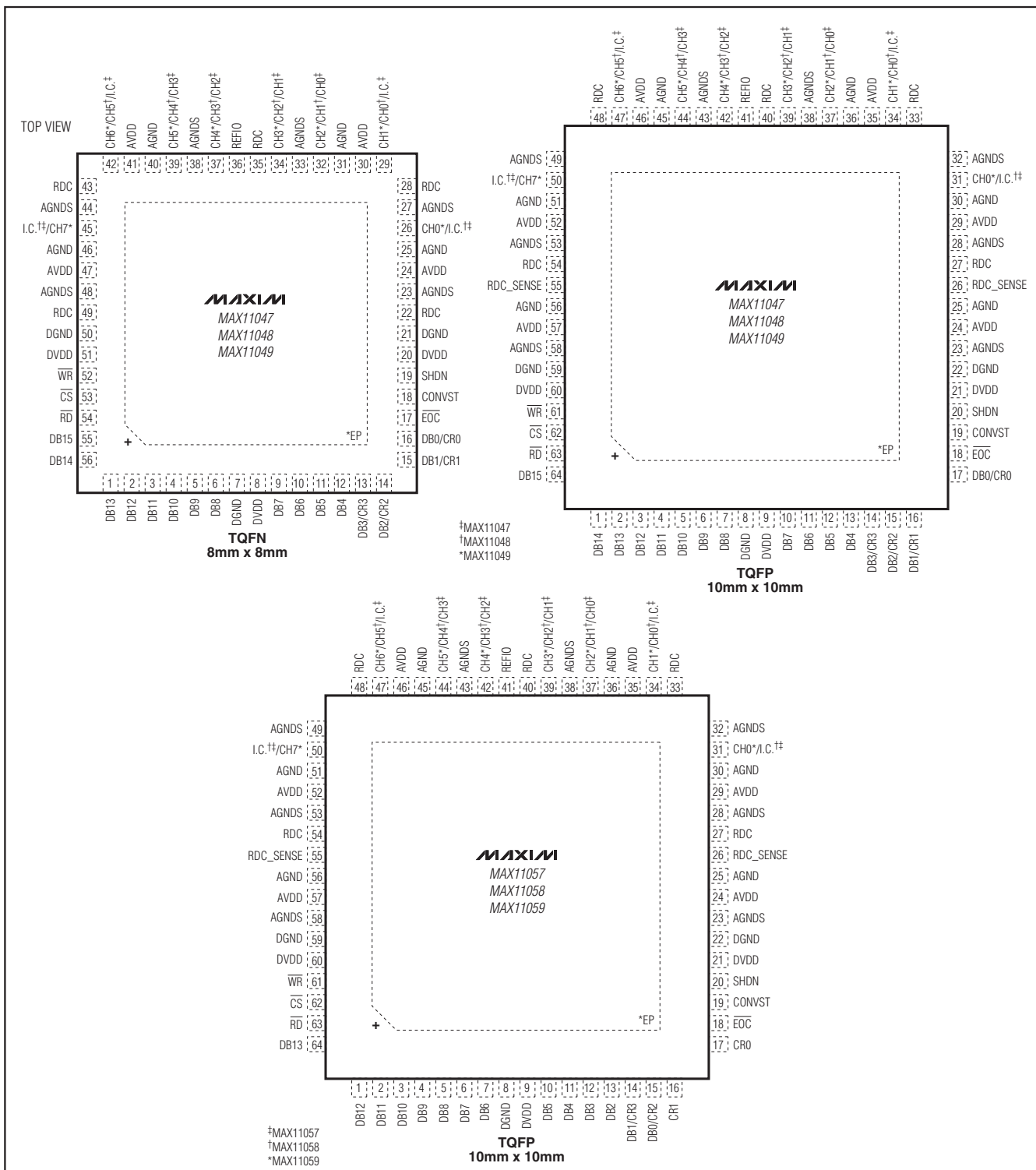
CONVERSION TIME vs. TEMPERATURE



4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

Pin Configurations

MAX11047-MAX11049/MAX11057-MAX11059



4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

Pin Description

| PIN | | | NAME | FUNCTION |
|---------------------------|---------------------------|---------------------------|------------------|--|
| MAX11047 (TQFN-EP) | MAX11048 (TQFN-EP) | MAX11049 (TQFN-EP) | | |
| 1 | 1 | 1 | DB13 | 16-Bit Parallel Data Bus Digital Output Bit 13 |
| 2 | 2 | 2 | DB12 | 16-Bit Parallel Data Bus Digital Output Bit 12 |
| 3 | 3 | 3 | DB11 | 16-Bit Parallel Data Bus Digital Output Bit 11 |
| 4 | 4 | 4 | DB10 | 16-Bit Parallel Data Bus Digital Output Bit 10 |
| 5 | 5 | 5 | DB9 | 16-Bit Parallel Data Bus Digital Output Bit 9 |
| 6 | 6 | 6 | DB8 | 16-Bit Parallel Data Bus Digital Output Bit 8 |
| 7, 21, 50 | 7, 21, 50 | 7, 21, 50 | DGND | Digital Ground |
| 8, 20, 51 | 8, 20, 51 | 8, 20, 51 | DVDD | Digital Supply. Bypass to DGND with a 0.1µF capacitor at each DVDD input. |
| 9 | 9 | 9 | DB7 | 16-Bit Parallel Data Bus Digital Output Bit 7 |
| 10 | 10 | 10 | DB6 | 16-Bit Parallel Data Bus Digital Output Bit 6 |
| 11 | 11 | 11 | DB5 | 16-Bit Parallel Data Bus Digital Output Bit 5 |
| 12 | 12 | 12 | DB4 | 16-Bit Parallel Data Bus Digital Output Bit 4 |
| 13 | 13 | 13 | DB3/CR3 | 16-Bit Parallel Data Bus Digital Output Bit 3/Configuration Register Input Bit 3 |
| 14 | 14 | 14 | DB2/CR2 | 16-Bit Parallel Data Bus Digital Output Bit 2/Configuration Register Input Bit 2 |
| 15 | 15 | 15 | DB1/CR1 | 16-Bit Parallel Data Bus Digital Output Bit 1/Configuration Register Input Bit 1 |
| 16 | 16 | 16 | DB0/CR0 | 16-Bit Parallel Data Bus Digital Output Bit 0/Configuration Register Input Bit 0 |
| 17 | 17 | 17 | \overline{EOC} | Active-Low End of Conversion Output. \overline{EOC} goes low when conversion is completed. \overline{EOC} goes high when a conversion is initiated. |
| 18 | 18 | 18 | CONVST | Convert Start Input. Rising edge of CONVST ends sample and starts a conversion on the captured sample. The ADC is in acquisition mode when CONVST is low and CONVST mode = 0. |
| 19 | 19 | 19 | SHDN | Shutdown Input. If SHDN is held high, the entire device enters and stays in a low-current state. Contents of the Configuration register are not lost when in the shutdown state. |
| 22, 28, 35, 43, 49 | 22, 28, 35, 43, 49 | 22, 28, 35, 43, 49 | RDC | Reference Buffer Decoupling. Connect all RDC outputs together. Bypass to AGND with at least an 80µF total capacitance. See the <i>Layout, Grounding, and Bypassing</i> section. |
| 23, 27, 33, 38, 44, 48 | 23, 27, 33, 38, 44, 48 | 23, 27, 33, 38, 44, 48 | AGNDS | Signal Ground. Connect all AGND and AGNDS inputs together on PWB. |
| 24, 30, 41, 47 | 24, 30, 41, 47 | 24, 30, 41, 47 | AVDD | Analog Supply Input. Bypass AVDD to AGND with a 0.1µF capacitor at each AVDD input. |
| 25, 31, 40, 46 | 25, 31, 40, 46 | 25, 31, 40, 46 | AGND | Analog Ground. Connect all AGND inputs together. |
| 26, 29, 42, 45 | 26, 45 | — | I.C. | Internally Connected. Connect to AGND |
| 32 | 29 | 26 | CH0 | Channel 0 Analog Input |
| 34 | 32 | 29 | CH1 | Channel 1 Analog Input |
| 36 | 36 | 36 | REFIO | External Reference Input/Internal Reference Output. Place a 0.1µF capacitor from REFIO to AGND. |

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

Pin Description (continued)

| PIN | | | NAME | FUNCTION |
|-----------------------|-----------------------|-----------------------|-----------------|---|
| MAX11047 (TQFN-EP) | MAX11048 (TQFN-EP) | MAX11049 (TQFN-EP) | | |
| 37 | 34 | 32 | CH2 | Channel 2 Analog Input |
| 39 | 37 | 34 | CH3 | Channel 3 Analog Input |
| — | 39 | 37 | CH4 | Channel 4 Analog Input |
| — | 42 | 39 | CH5 | Channel 5 Analog Input |
| — | — | 42 | CH6 | Channel 6 Analog Input |
| — | — | 45 | CH7 | Channel 7 Analog Input |
| 52 | 52 | 52 | \overline{WR} | Active-Low Write Input. Drive \overline{WR} low to write to the ADC. Configuration registers are loaded on the rising edge of \overline{WR} . |
| 53 | 53 | 53 | \overline{CS} | Active Low-Chip Select Input. Drive \overline{CS} low when reading from or writing to the ADC. |
| 54 | 54 | 54 | \overline{RD} | Active-Low Read Input. Drive \overline{RD} low to read from the ADC. Each rising edge of \overline{RD} advances the channel output on the data bus. |
| 55 | 55 | 55 | DB15 | 16-Bit Parallel Data Bus Digital Output Bit 15 |
| 56 | 56 | 56 | DB14 | 16-Bit Parallel Data Bus Digital Output Bit 14 |
| — | — | — | EP | Exposed Pad. Internally connected to AGND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point. |

| PIN | | | NAME | FUNCTION |
|-----------------------|-----------------------|-----------------------|---------|--|
| MAX11047 (TQFP-EP) | MAX11048 (TQFP-EP) | MAX11049 (TQFP-EP) | | |
| 1 | 1 | 1 | DB14 | 16-Bit Parallel Data Bus Digital Output Bit 14 |
| 2 | 2 | 2 | DB13 | 16-Bit Parallel Data Bus Digital Output Bit 13 |
| 3 | 3 | 3 | DB12 | 16-Bit Parallel Data Bus Digital Output Bit 12 |
| 4 | 4 | 4 | DB11 | 16-Bit Parallel Data Bus Digital Output Bit 11 |
| 5 | 5 | 5 | DB10 | 16-Bit Parallel Data Bus Digital Output Bit 10 |
| 6 | 6 | 6 | DB9 | 16-Bit Parallel Data Bus Digital Output Bit 9 |
| 7 | 7 | 7 | DB8 | 16-Bit Parallel Data Bus Digital Output Bit 8 |
| 8, 22, 59 | 8, 22, 59 | 8, 22, 59 | DGND | Digital Ground |
| 9, 21, 60 | 9, 21, 60 | 9, 21, 60 | DVDD | Digital Supply. Bypass to DGND with a 0.μF capacitor at each DVDD input. |
| 10 | 10 | 10 | DB7 | 16-Bit Parallel Data Bus Digital Output Bit 7 |
| 11 | 11 | 11 | DB6 | 16-Bit Parallel Data Bus Digital Output Bit 6 |
| 12 | 12 | 12 | DB5 | 16-Bit Parallel Data Bus Digital Output Bit 5 |
| 13 | 13 | 13 | DB4 | 16-Bit Parallel Data Bus Digital Output Bit 4 |
| 14 | 14 | 14 | DB3/CR3 | 16-Bit Parallel Data Bus Digital Output Bit 3/Configuration Register Input Bit 3 |
| 15 | 15 | 15 | DB2/CR2 | 16-Bit Parallel Data Bus Digital Output Bit 2/Configuration Register Input Bit 2 |
| 16 | 16 | 16 | DB1/CR1 | 16-Bit Parallel Data Bus Digital Output Bit 1/Configuration Register Input Bit 1 |
| 17 | 17 | 17 | DB0/CR0 | 16-Bit Parallel Data Bus Digital Output Bit 0/Configuration Register Input Bit 0 |

MAX11047-MAX11049/MAX11057-MAX11059

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

Pin Description (continued)

| PIN | | | NAME | FUNCTION |
|--------------------------------------|--------------------------------------|--------------------------------------|-------------------------|---|
| MAX11047 (TQFP-EP) | MAX11048 (TQFP-EP) | MAX11049 (TQFP-EP) | | |
| 18 | 18 | 18 | $\overline{\text{EOC}}$ | Active-Low, End-of-Conversion Output. EOC goes low when a conversion is completed. EOC goes high when a conversion is initiated. |
| 19 | 19 | 19 | CONVST | Convert Start Input. The rising edge of CONVST ends sample and starts a conversion on the captured sample. The ADC is in acquisition mode when CONVST is low and CONVST mode = 0. |
| 20 | 20 | 20 | SHDN | Shutdown Input. If SHDN is held high, the entire device enters and stays in a low-current state. Contents of the Configuration register are not lost when in the shutdown state. |
| 23, 28, 32, 38, 43, 49, 53, 58 | 23, 28, 32, 38, 43, 49, 53, 58 | 23, 28, 32, 38, 43, 49, 53, 58 | AGNDS | Signal Ground. Connect all AGND and AGNDS inputs together. |
| 24, 29, 35, 46, 52, 57 | 24, 29, 35, 46, 52, 57 | 24, 29, 35, 46, 52, 57 | AVDD | Analog Supply Input. Bypass AVDD to AGND with a 0.1μF capacitor at each AVDD input. |
| 25, 30, 36, 45, 51, 56 | 25, 30, 36, 45, 51, 56 | 25, 30, 36, 45, 51, 56 | AGND | Analog Ground. Connect all AGND inputs together. |
| 26, 55 | 26, 55 | 26, 55 | RDC_SENSE | Reference Buffer Sense Feedback. Connect to RDC plane. |
| 27, 33, 40, 48, 54 | 27, 33, 40, 48, 54 | 27, 33, 40, 48, 54 | RDC | Reference Buffer Decoupling. Connect all RDC outputs together. Bypass to AGND with at least an 80μF total capacitance. See the <i>Layout, Grounding, and Bypassing</i> section. |
| 31, 34, 47, 50 | 31, 50 | — | I.C. | Internally Connected. Connect to AGND. |
| 37 | 34 | 31 | CH0 | Channel 0 Analog Input |
| 39 | 37 | 34 | CH1 | Channel 1 Analog Input |
| 41 | 41 | 41 | REFIO | External Reference Input/Internal Reference Output. Place a 0.1μF capacitor from REFIO to AGND. |
| 42 | 39 | 37 | CH2 | Channel 2 Analog Input |
| 44 | 42 | 39 | CH3 | Channel 3 Analog Input |
| — | 44 | 42 | CH4 | Channel 4 Analog Input |
| — | 47 | 44 | CH5 | Channel 5 Analog Input |
| — | — | 47 | CH6 | Channel 6 Analog Input |
| — | — | 50 | CH7 | Channel 7 Analog Input |
| 61 | 61 | 61 | $\overline{\text{WR}}$ | Active-Low Write Input. Drive WR low to write to the ADC. Configuration registers are loaded on the rising edge of WR. |
| 62 | 62 | 62 | $\overline{\text{CS}}$ | Active-Low Chip-Select Input. Drive CS low when reading from or writing to the ADC. |
| 63 | 63 | 63 | $\overline{\text{RD}}$ | Active-Low Read Input. Drive RD low to read from the ADC. Each rising edge of RD advances the channel output on the data bus. |
| 64 | 64 | 64 | DB15 | 16-Bit Parallel Data Bus Digital Out Bit 15 |
| — | — | — | EP | Exposed Pad. Internally connected to AGND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point. |

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

Pin Description (continued)

| PIN | | | NAME | FUNCTION |
|--------------------------------------|--------------------------------------|--------------------------------------|-------------------------|---|
| MAX11057 (TQFP-EP) | MAX11058 (TQFP-EP) | MAX11059 (TQFP-EP) | | |
| 1 | 1 | 1 | DB12 | 14-Bit Parallel Data Bus Digital Output Bit 12 |
| 2 | 2 | 2 | DB11 | 14-Bit Parallel Data Bus Digital Output Bit 11 |
| 3 | 3 | 3 | DB10 | 14-Bit Parallel Data Bus Digital Output Bit 10 |
| 4 | 4 | 4 | DB9 | 14-Bit Parallel Data Bus Digital Output Bit 9 |
| 5 | 5 | 5 | DB8 | 14-Bit Parallel Data Bus Digital Output Bit 8 |
| 6 | 6 | 6 | DB7 | 14-Bit Parallel Data Bus Digital Output Bit 7 |
| 7 | 7 | 7 | DB6 | 14-Bit Parallel Data Bus Digital Output Bit 6 |
| 8, 22, 59 | 8, 22, 59 | 8, 22, 59 | DGND | Digital Ground |
| 9, 21, 60 | 9, 21, 60 | 9, 21, 60 | DVDD | Digital Supply. Bypass to DGND with a 0.1 μ F capacitor at each DVDD input. |
| 10 | 10 | 10 | DB5 | 14-Bit Parallel Data Bus Digital Output Bit 5 |
| 11 | 11 | 11 | DB4 | 14-Bit Parallel Data Bus Digital Output Bit 4 |
| 12 | 12 | 12 | DB3 | 14-Bit Parallel Data Bus Digital Output Bit 3 |
| 13 | 13 | 13 | DB2 | 14-Bit Parallel Data Bus Digital Output Bit 2 |
| 14 | 14 | 14 | DB1/CR3 | 14-Bit Parallel Data Bus Digital Output Bit 1/Configuration Register Input Bit 3 |
| 15 | 15 | 15 | DB0/CR2 | 14-Bit Parallel Data Bus Digital Output Bit 0/Configuration Register Input Bit 2 |
| 16 | 16 | 16 | CR1 | Configuration Register Input Bit 1 |
| 17 | 17 | 17 | CR0 | Configuration Register Input Bit 0 |
| 18 | 18 | 18 | $\overline{\text{EOC}}$ | Active-Low, End-of-Conversion Output. EOC goes low when a conversion is completed. EOC goes high when a conversion is initiated. |
| 19 | 19 | 19 | CONVST | Convert Start Input. The rising edge of CONVST ends sample and starts a conversion on the captured sample. The ADC is in acquisition mode when CONVST is low and CONVST mode = 0. |
| 20 | 20 | 20 | SHDN | Shutdown Input. If SHDN is held high, the entire device enters and stays in a low-current state. Contents of the Configuration register are not lost when in the shutdown state. |
| 23, 28, 32, 38, 43, 49, 53, 58 | 23, 28, 32, 38, 43, 49, 53, 58 | 23, 28, 32, 38, 43, 49, 53, 58 | AGNDS | Signal Ground. Connect all AGND and AGNDS inputs together. |
| 24, 29, 35, 46, 52, 57 | 24, 29, 35, 46, 52, 57 | 24, 29, 35, 46, 52, 57 | AVDD | Analog Supply Input. Bypass AVDD to AGND with a 0.1 μ F capacitor at each AVDD input. |
| 25, 30, 36, 45, 51, 56 | 25, 30, 36, 45, 51, 56 | 25, 30, 36, 45, 51, 56 | AGND | Analog Ground. Connect all AGND inputs together. |
| 26, 55 | 26, 55 | 26, 55 | RDC_SENSE | Reference Buffer Sense Feedback. Connect to RDC plane. |
| 27, 33, 40,48, 54 | 27, 33, 40,48, 54 | 27, 33, 40,48, 54 | RDC | Reference Buffer Decoupling. Connect all RDC outputs together. Bypass to AGND with at least an 80 μ F total capacitance. See the <i>Layout, Grounding, and Bypassing</i> section. |
| 31, 34, 47, 50 | 31, 50 | — | I.C. | Internally Connected. Connect to AGND. |
| 37 | 34 | 31 | CH0 | Channel 0 Analog Input |
| 39 | 37 | 34 | CH1 | Channel 1 Analog Input |

MAX11047-MAX11049/MAX11057-MAX11059

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

Pin Description (continued)

| PIN | | | NAME | FUNCTION |
|--------------------|--------------------|--------------------|------------------------|---|
| MAX11057 (TQFP-EP) | MAX11058 (TQFP-EP) | MAX11059 (TQFP-EP) | | |
| 41 | 41 | 41 | REFIO | External Reference Input/Internal Reference Output. Place a 0.1 μ F capacitor from REFIO to AGND. |
| 42 | 39 | 37 | CH2 | Channel 2 Analog Input |
| 44 | 42 | 39 | CH3 | Channel 3 Analog Input |
| — | 44 | 42 | CH4 | Channel 4 Analog Input |
| — | 47 | 44 | CH5 | Channel 5 Analog Input |
| — | — | 47 | CH6 | Channel 6 Analog Input |
| — | — | 50 | CH7 | Channel 7 Analog Input |
| 61 | 61 | 61 | $\overline{\text{WR}}$ | Active-Low Write Input. Drive WR low to write to the ADC. Configuration registers are loaded on the rising edge of WR. |
| 62 | 62 | 62 | $\overline{\text{CS}}$ | Active-Low Chip-Select Input. Drive CS low when reading from or writing to the ADC. |
| 63 | 63 | 63 | $\overline{\text{RD}}$ | Active-Low Read Input. Drive RD low to read from the ADC. Each rising edge of RD advances the channel output on the data bus. |
| 64 | 64 | 64 | DB13 | 14-Bit Parallel Data Bus Digital Out Bit 13 |
| — | — | — | EP | Exposed Pad. Internally connected to AGND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point. |

Detailed Description

The MAX11047/MAX11048/MAX11049 and MAX11057/MAX11058/MAX11059 are fast, low-power ADCs that combine 4, 6, or 8 independent ADC channels in a single IC. Each channel includes simultaneously sampling independent T/H circuitry that preserves relative phase information between inputs making the devices ideal for motor control and power monitoring. The devices are available with a 0 to 5V input range that features $\pm 20\text{mA}$ overrange, fault-tolerant inputs. The devices operate with a single 4.75V to 5.25V supply. A separate 2.7V to 5.25V supply for digital circuitry makes the devices compatible with low-voltage processors.

The devices perform conversions for all channels in parallel by activating independent ADCs. Results are available through a high-speed, 20MHz, parallel data bus after a conversion time of 3 μ s following the end of a sample. The

data bus is bidirectional and allows for easy programming of the configuration register. The devices feature a reference buffer, which is driven by an internal bandgap reference circuit ($V_{\text{REFIO}} = 4.096\text{V}$). Drive REFIO with an external reference or bypass with a 0.1 μ F capacitor to ground when using the internal reference.

Analog Inputs

Track and Hold (T/H)

To preserve phase information across all channels, each input includes a dedicated T/H circuitry. The input tracking circuitry provides a 4MHz small-signal bandwidth, enabling the device to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. Use anti-alias filtering to avoid high-frequency signals being aliased into the frequency band of interest.

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

Input Range and Protection

The full-scale analog input voltage is a product of the reference voltage. For the devices, the input is unipolar in the range of:

$$0 \text{ to } +V_{\text{REFIO}} \times \frac{5.0}{4.096}$$

In external reference mode, drive V_{REFIO} with a 3.0V to 4.25V source, resulting in a full-scale input range of 3.662V to 5.188V, respectively.

All analog inputs are fault-protected up to $\pm 20\text{mA}$. The devices include an input clamping circuit that activates when the input voltage at the analog input is above ($V_{\text{AVDD}} + 300\text{mV}$) or below -300mV . The clamp circuit remains high impedance while the input signal is within the range of 0V to $+V_{\text{AVDD}}$ and draws little to no current. However, when the input signal exceeds the range

of 0V to $+V_{\text{AVDD}}$, the clamps begin to turn on. Consequently, to obtain the highest accuracy, ensure that the input voltage does not exceed the range of 0V to $+V_{\text{AVDD}}$.

To make use of the input clamps, connect a resistor (R_s) between the analog input and the voltage source to limit the voltage at the analog input so that the fault current into the devices does not exceed $\pm 20\text{mA}$. Note that the voltage at the analog input pin limits to approximately 7V during a fault condition so the following equation can be used to calculate the value of R_s :

$$R_s = \frac{V_{\text{FAULT_MAX}} - 7\text{V}}{20\text{mA}}$$

where $V_{\text{FAULT_MAX}}$ is the maximum voltage that the source produces during a fault condition.

MAX11047-MAX11049/MAX11057-MAX11059

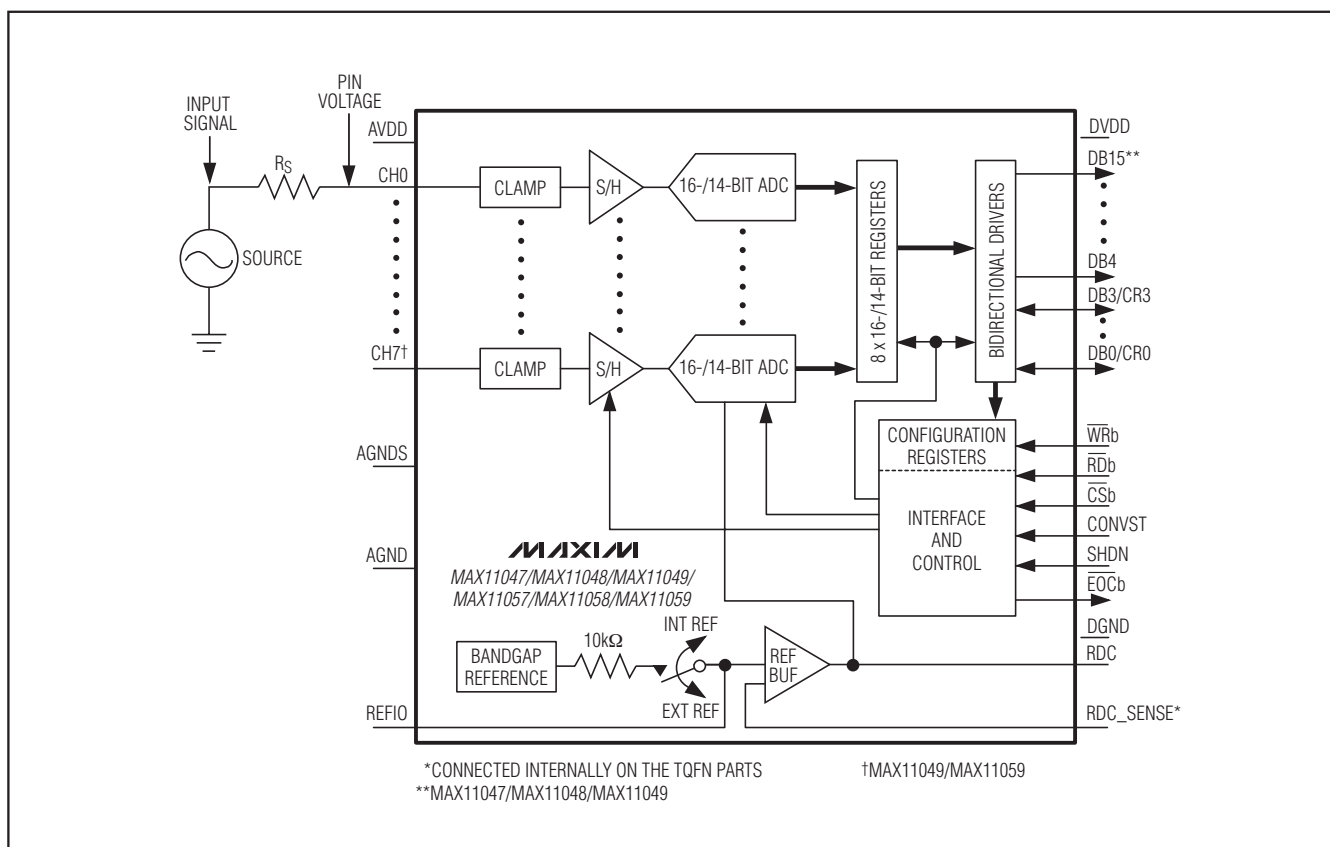


Figure 1. Required Setup for Clamp Circuit

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

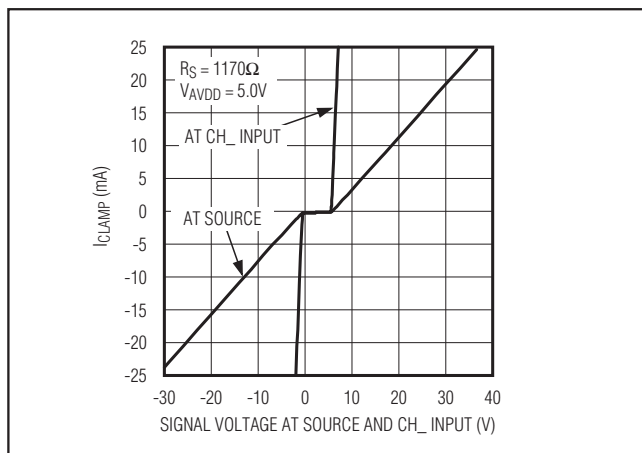


Figure 2. Input Clamp Characteristics

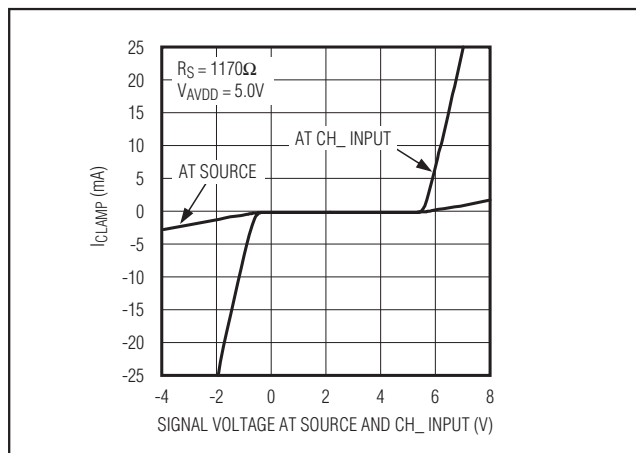


Figure 3. Input Clamp Characteristics (Zoom In)

Figures 2 and 3 illustrate the clamp circuit voltage-current characteristics for a source impedance $R_S = 1280\Omega$. While the input voltage is within the -300mV to $+(V_{AVDD} + 300\text{mV})$ range, no current flows in the input clamps. Once the input voltage goes beyond this voltage range, the clamps turn on and limit the voltage at the input pin.

Applications Information

Digital Interface

The bidirectional, parallel, digital interface, CR0–CR3, sets the 4-bit configuration register. This interface configures the following control signals: chip select (\overline{CS}), read (\overline{RD}), write (\overline{WR}), end of conversion (\overline{EOC}), and convert start (CONVST). Figures 6 and 7 and the Timing Characteristics in the *Electrical Characteristics* table show the operation of the interface.

DB0–DB15/13, output the 16-/14-bit conversion result. All bits are high impedance when $\overline{RD} = 1$ or $\overline{CS} = 1$.

CR3 (Int/Ext Reference)

CR3 selects the internal or external reference. The POR default = 0.

0 = internal reference, REFIO internally driven through a $10\text{k}\Omega$ resistor, bypass with $0.1\mu\text{F}$ capacitor to AGND.

1 = external reference, drive REFIO with a high quality reference.

CR2 (Output Data Format)

CR2 selects the output data format. The POR default = 0.

0 = offset binary.

1 = two's complement.

CR1 (Reserved)

CR1 must be set to 0.

CR0 (CONVST Mode)

CR0 selects the acquisition mode. The POR default = 0.

0 = CONVST controls the acquisition and conversion. Drive CONVST low to start acquisition. The rising edge of CONVST begins the conversion.

1 = acquisition mode starts as soon as previous conversion is complete. The rising edge of CONVST begins the conversion.

Programming the Configuration Register

To program the configuration register, bring the \overline{CS} and \overline{WR} low and apply the required configuration data on CR3–CR0 of the bus and then raise \overline{WR} once to save changes.

CAUTION: The host driving CR3–CR0 must relinquish the bus when the conversion results of the ADC are being read.

Starting a Conversion

CONVST initiates conversions. The devices provide two acquisition modes set through the configuration register. Allow a quiet time (t_Q) of 500ns prior to the start of conversion to avoid any noise interference during read-out or write operations from corrupting a sample.

Table 1. Configuration Register

| CR3 | CR2 | CR1 | CR0 |
|-------------------|--------------------|------------------|-------------|
| Int/Ext Reference | Output Data Format | Must be set to 0 | CONVST Mode |

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

MAX11047-MAX11049/MAX11057-MAX11059

In default mode (CR0 = 0), drive CONVST low to place the devices into acquisition mode. All the input switches are closed and the internal T/H circuits track the respective input voltage. Keep the CONVST signal low for at least 1 μ s (t_{ACQ}) to enable proper settling of the sampled voltages. On the rising edge of CONVST, the switches are opened and the devices begin the conversion on all the samples in parallel. $\overline{\text{EOC}}$ remains high until the conversion is completed.

In the second mode (CR0 = 1), the devices enter acquisition mode as soon as the previous conversion is completed. CONVST rising edge initiates the next sample and conversion sequence. Drive CONVST low for at least 20ns to be valid.

Provide adequate time for acquisition and the requisite quiet time in both modes to achieve accurate sampling and maximum performance of the devices.

Reading Conversion Results

The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are active-low, digital inputs that control the readout through the 16-/14-bit, parallel, 20MHz data bus (D0–D15/13). After $\overline{\text{EOC}}$ transitions low, read the conversion data by driving $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low. Each low period of $\overline{\text{RD}}$ presents the next channel's result. When $\overline{\text{CS}}$ or $\overline{\text{RD}}$ are high, the data bus is high impedance. $\overline{\text{CS}}$ may be driven high between individual channel readouts or left low during the entire 8-channel readout.

Reference

Internal Reference

The devices feature a precision, low-drift, internal bandgap reference. Bypass REFIO with a 0.1 μ F capacitor to AGND to reduce noise. The REFIO output voltage may be used as a reference for other circuits. The output impedance of REFIO is 10k Ω . Drive only high-impedance circuits or buffer externally when using REFIO to drive external circuitry.

External Reference

Set the configuration register to disable the internal reference and drive REFIO with a high-quality external reference. To avoid signal degradation, ensure that the integrated reference noise applied to REFIO is less than 10 μ V in the bandwidth of up to 50kHz.

Reference Buffer

The devices have a built-in reference buffer to provide a low-impedance reference source to the SAR converters. This buffer is used in both internal and external reference modes. The internal reference buffer output feeds five RDC outputs. Connect all RDC outputs

together. The reference buffer is externally compensated and requires at least 10 μ F on the RDC node for stability. For best performance, provide a total of at least 80 μ F on the RDC outputs.

Transfer Functions

Figures 8 and 9 show the transfer functions for all the formats and devices. Code transitions occur halfway between successive-integer LSB values.

Layout, Grounding, and Bypassing

For best performance, use PCBs with ground planes. Ensure that digital and analog signal lines are separated from each other. Do not run analog and digital lines parallel to one another (especially clock lines), and avoid running digital lines underneath the ADC package. A single solid GND plane configuration with digital signals routed from one direction and analog signals from the other provides the best performance. Connect DGND, AGND, and AGNDS pins on the devices to this ground plane. Keep the ground return to the power supply for this ground low impedance and as short as possible for noise-free operation.

To achieve the highest performance, connect all the RDC pins 22, 28, 35, 43, and 49 for the TQFN package or pins 27, 33, 40, 48, and 54 for the TQFP package to a local RDC plane on the PCB. In addition, on the TQFP package, the RDC_SENSE pins 26 and 55 should be directly connected to this RDC plane as well. Bypass the RDC outputs with a total of at least 80 μ F of capacitance. For example, if two capacitors are used, place two 47 μ F, 10V X5R capacitors in 1210 case size as close as possible to pins 22 and 49 (TQFN), or pins 27 and 54 (TQFP). Alternatively, if four capacitors are used, place four 22 μ F, 10V X5R capacitors in 1210 case size as close as possible to pins 22, 28, 43, and 49 (TQFN), or pins 27, 33, 48, and 54 (TQFP). Ensure that each capacitor is connected directly into the GND plane with an independent via.

In cases where Y5U or Z5U ceramics are used, select higher voltage rating capacitors to compensate for the high-voltage coefficient of these ceramic capacitors, thus ensuring that at least 80 μ F of capacitance is on the RDC plane when the plane is driven to 4.096V by the internal reference buffer. For example, at 4.096V, a 22 μ F X5R ceramic capacitor with a 10V rating diminishes to only 20 μ F, whereas the same capacitor in Y5U ceramic at 4.096V decreases to about 13 μ F. However, a 22 μ F Y5U ceramic capacitor with a 25V rating capacitor is approximately 20 μ F at 4.096V.

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

Bypass AVDD and DVDD to the ground plane with 0.1 μ F ceramic chip capacitors on each pin as close as possible to the device to minimize parasitic inductance. Add at least one bulk 10 μ F decoupling capacitor to AVDD and DVDD per PCB. Interconnect all of the AVDD inputs and DVDD inputs using two solid power planes. For best performance, bring the AVDD power plane in on the analog interface side of the devices and the DVDD power plane from the digital interface side of the devices.

For sampling periods near minimum (1 μ s) use a 1nF C0G ceramic chip capacitor between each of the channel inputs to the ground plane as close as possible to the devices. This capacitor reduces the inductance seen by the sampling circuitry and reduces the voltage transient seen by the input source circuit.

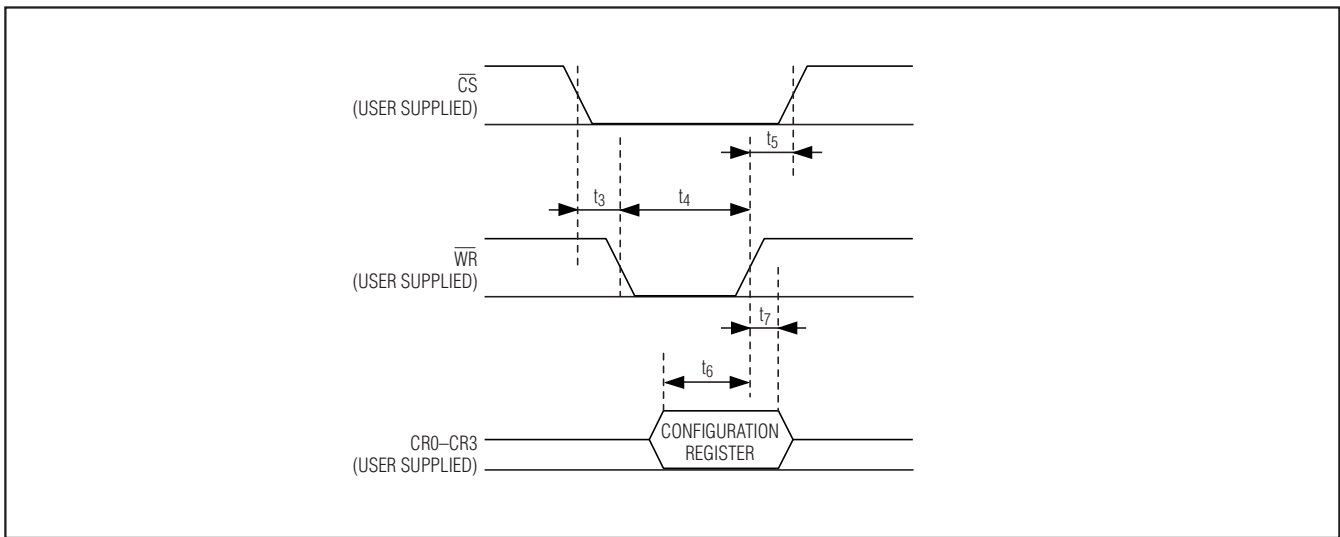


Figure 4. Programming Configuration-Register Timing Requirements

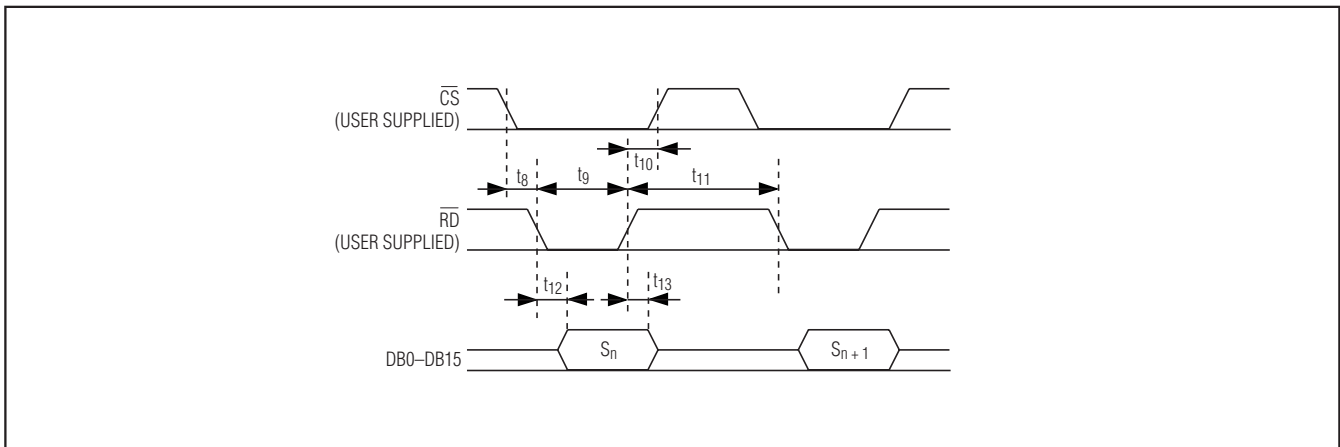


Figure 5. Readout Timing Requirements

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

MAX11047-MAX11049/MAX11057-MAX11059

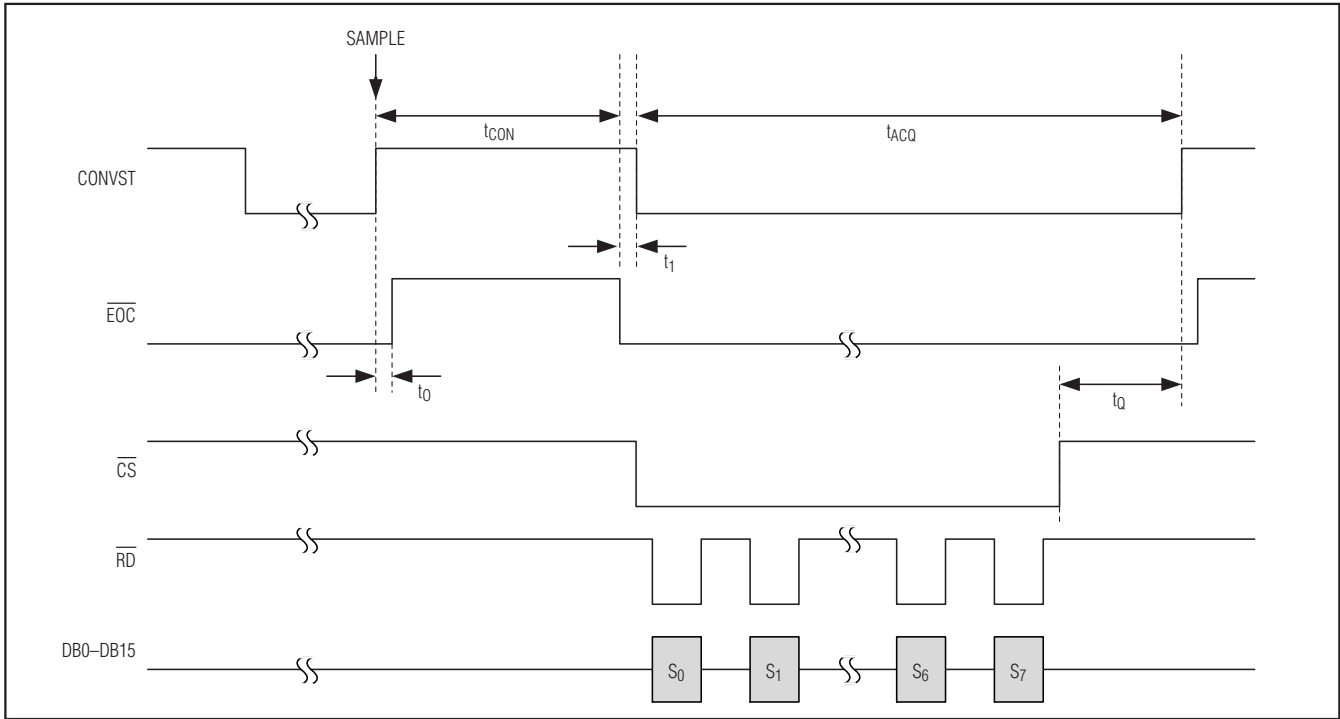


Figure 6. Conversion Timing Diagram (CR0 = 0)

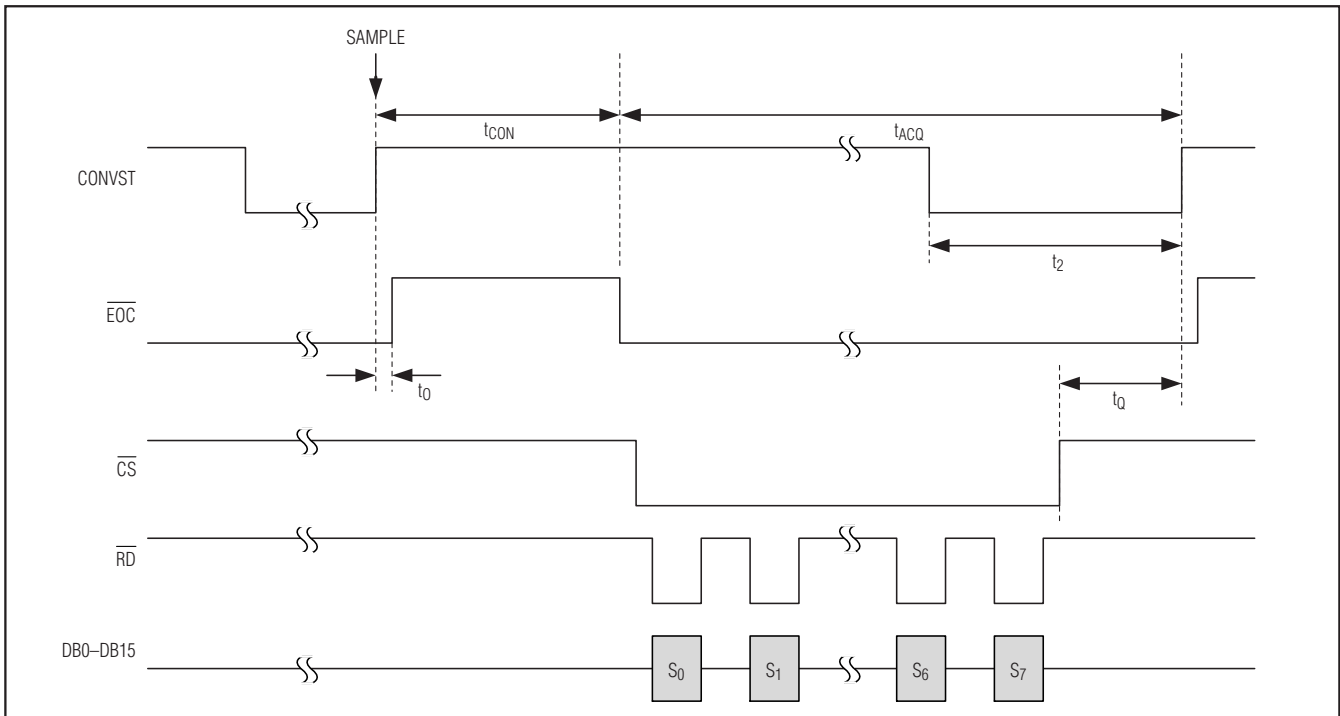


Figure 7. Conversion Timing Diagram (CR0 = 1)

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

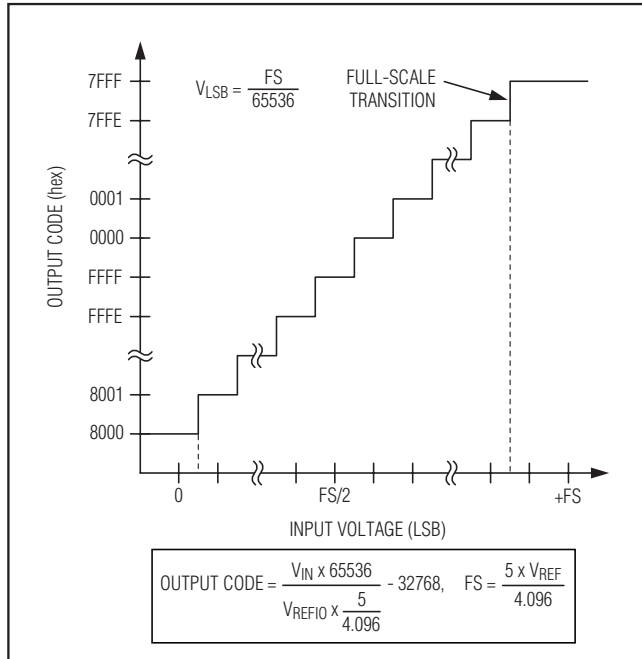


Figure 8a. Two's Complement Transfer Function for 16-Bit Devices

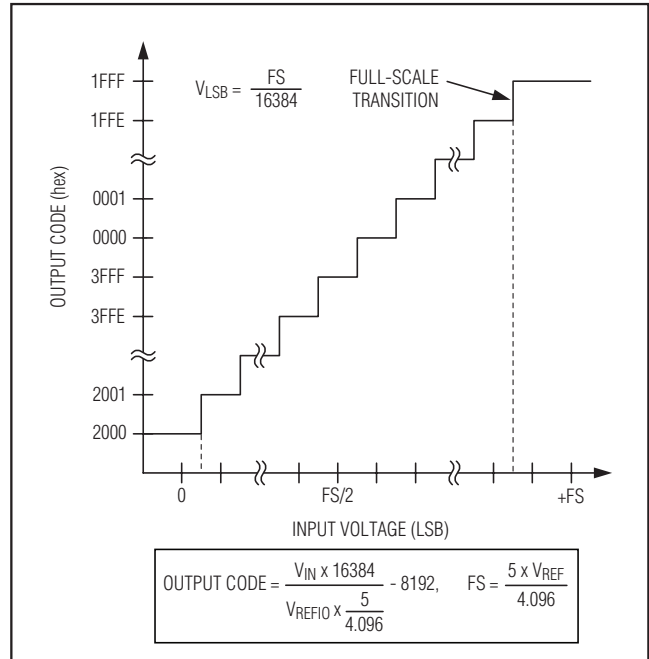


Figure 8b. Two's Complement Transfer Function for 14-Bit Devices

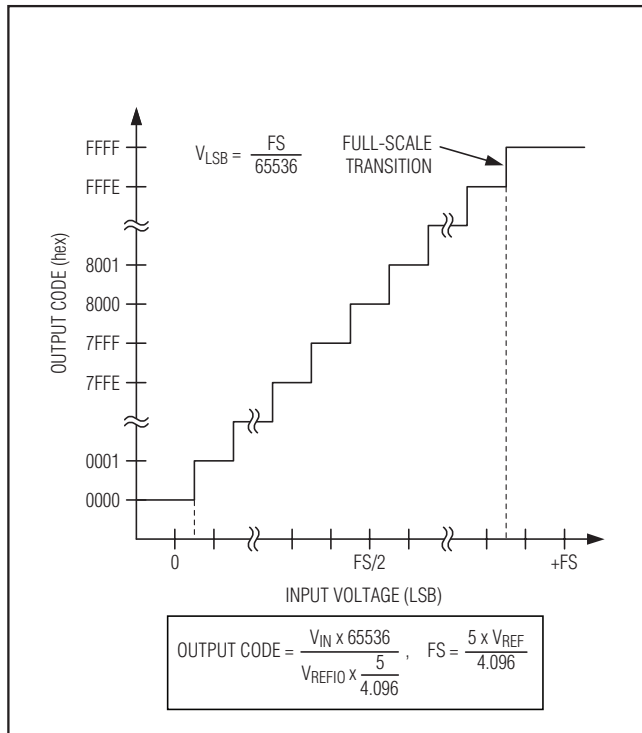


Figure 9a. Offset-Binary Transfer Function for 16-Bit Devices

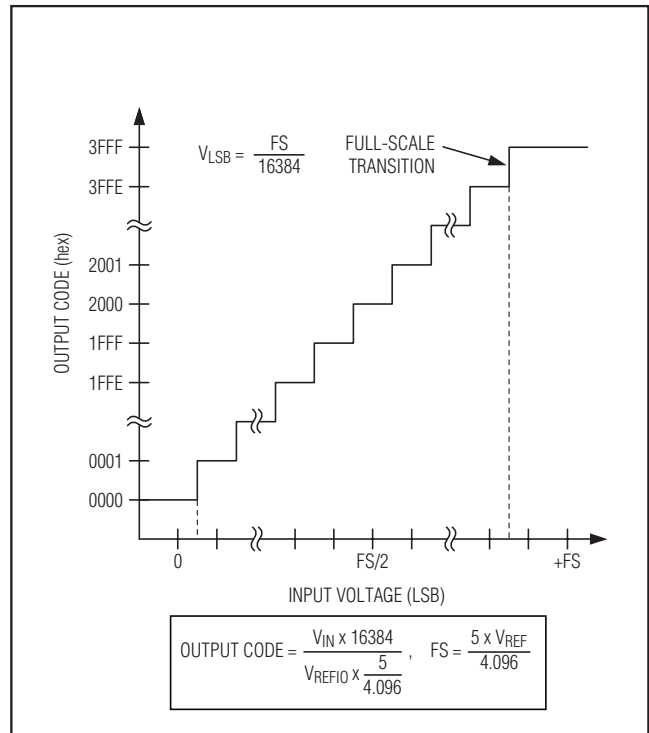


Figure 9b. Offset-Binary Transfer Function for 14-Bit Devices

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

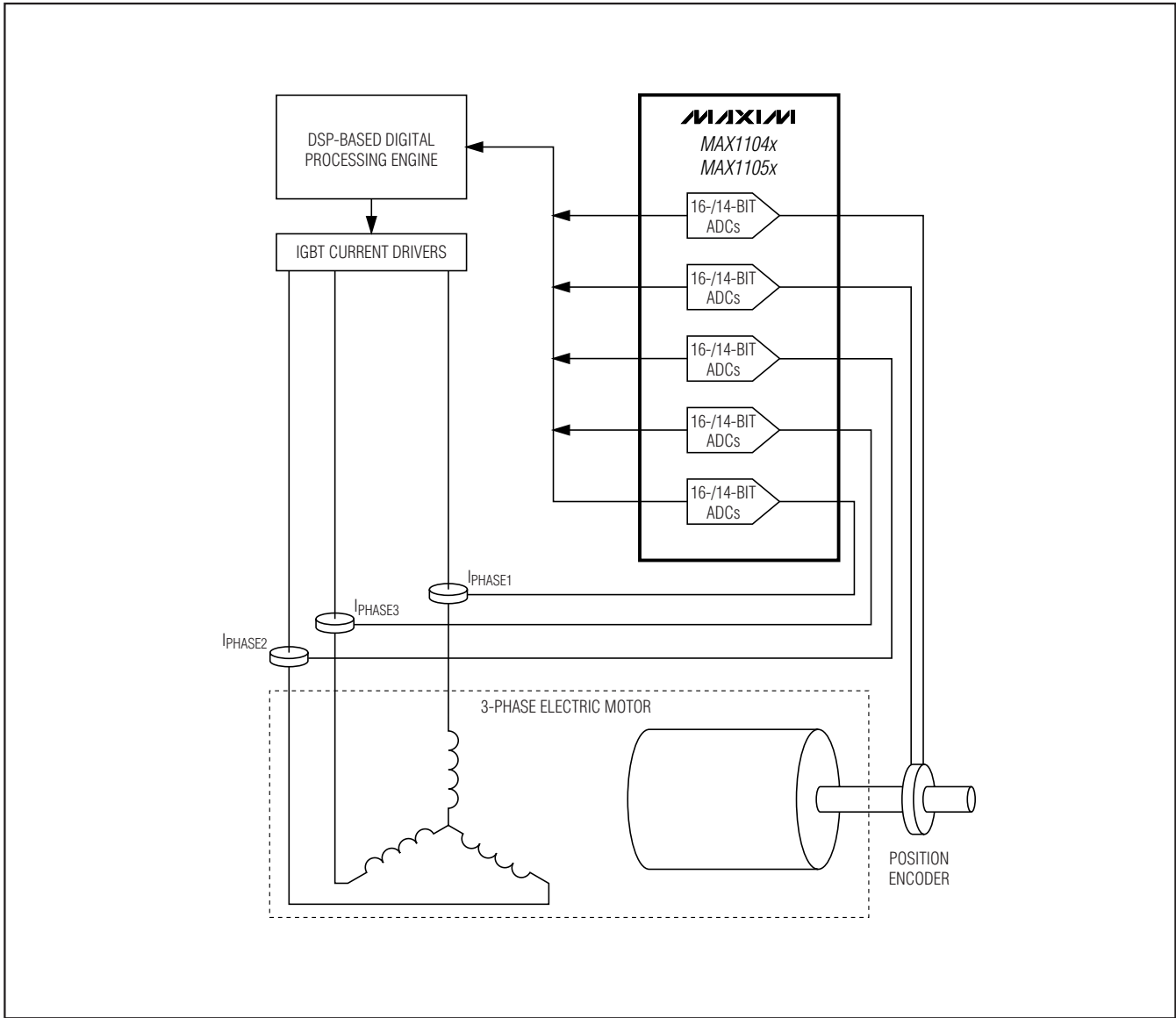


Figure 11. DSP Motor Control

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

MAX11047-MAX11049/MAX11057-MAX11059

Definitions

Integral Nonlinearity (INL)

INL is the deviation of the values on an actual transfer function from a straight line. For these devices, this straight line is a line drawn between the end points of the transfer function, once offset and gain errors have been nullified.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step width and the ideal value of 1 LSB. For these devices, the DNL of each digital output code is measured and the worst-case value is reported in the *Electrical Characteristics* table. A DNL error specification of greater than -1 LSB guarantees no missing codes and a monotonic transfer function for an SAR ADC. For example, -0.9 LSB guarantees no missing code while -1.1 LSB results in missing code.

Offset Error

For the MAX11047/MAX11048/MAX11049, the offset error is defined at code transition 0x0000 to 0x0001 in offset binary encoding and 0x8000 to 0x8001 for two's complement encoding. For the MAX11057/MAX11058/MAX11059, the offset error is defined at code transition 0x0000 to 0x0001 in offset binary encoding and 0x2000 to 0x2001 for two's complement encoding. The offset code transitions should occur with an analog input voltage of exactly $0.5 \times (5/4.096) \times V_{REF}/65,536$ above GND for 16-bit devices or $0.5 \times (5/4.096) \times V_{REF}/16384$ above GND for 14-bit devices. The offset error is defined as the deviation between the actual analog input voltage required to produce the offset code transition and the ideal analog input of $0.5 \times (5/4.096) \times V_{REF}/65,536$ above GND for 16-bit devices or $0.5 \times (5/4.096) \times V_{REF}/16384$ above GND for 14-bit devices, expressed in LSBs.

Gain Error

Gain error is defined as the difference between the change in analog input voltage required to produce a top code transition minus a bottom code transition, subtracted from the ideal change in analog input voltage on $(5/4.096) \times V_{REF} \times (65,534/65,536)$ for 16-bit or $(5/4.096) \times V_{REF} \times (16382/16384)$ for 14-bit devices. For the devices, top code transition is 0x7FFE to 0x7FFF in two's complement mode and 0xFFFE to 0xFFFF in offset binary mode. The bottom code transition is 0x8000 and 0x8001 in two's complement mode and 0x0000 and 0x0001 in offset binary mode. For the MAX11057/MAX11058/MAX11059, top code transition is 0x1FFE to 0x1FFF in two's complement mode and 0x3FFE to 0x3FFF in offset binary mode. The bottom code transition is 0x2000 and 0x2001 in two's

complement mode and 0x0000 to 0x0001 in offset binary mode. For the devices, the analog input voltage to produce these code transitions is measured and the gain error is computed by subtracting $(5/4.096) \times V_{REF} \times (65,534/65,536)$ or $(5/4.096) \times V_{REF} \times (16382/16384)$, respectively, from this measurement.

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$\text{SNR} = (6.02 \times N + 1.76) \text{dB}$$

where N = 16/14 bits. In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components not including the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals:

$$\text{SINAD(dB)} = 10 \times \log \left[\frac{\text{Signal}_{\text{RMS}}}{(\text{Noise} + \text{Distortion})_{\text{RMS}}} \right]$$

Effective Number of Bits (ENOB)

The ENOB indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}$$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$\text{THD} = 20 \times \log \left[\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1} \right]$$

where V_1 is the fundamental amplitude and V_2 through V_5 are the 2nd- through 5th-order harmonics.

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest frequency component.

Aperture Delay

Aperture delay (t_{AD}) is the time delay from the sampling clock edge to the instant when an actual sample is taken.

Aperture Jitter

Aperture Jitter (t_{AJ}) is the sample-to-sample variation in aperture delay.

Channel-to-Channel Isolation

Channel-to-channel isolation indicates how well each analog input is isolated from the other channels. Channel-to-channel isolation is measured by applying DC to channels 1 to 7, while a -0.4dBFS sine wave at 60Hz is applied to channel 0. A 10ksps FFT is taken for channel 0 and channel 1. Channel-to-channel isolation is expressed in dB as the power ratio of the two 60Hz magnitudes.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC in a manner that ensures that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased 3dB.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. This point is defined as full-power input bandwidth frequency.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 56 TQFN-EP | T5688+2 | 21-0135 | 90-0046 |
| 64 TQFP-EP | C64E+6 | 21-0084 | 90-0328 |

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|---|---------------|
| 0 | 12/09 | Initial release | — |
| 1 | 6/10 | Released MAX11047, MAX11048, and MAX11049 in TQFP packages | 1–20 |
| 2 | 1/11 | Released MAX11057, MAX11058, and MAX11059. Updated <i>Electrical Characteristics</i> and <i>Typical Operating Characteristics</i> . | 1–8 |

MAX11047-MAX11049/MAX11057-MAX11059

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