



**THE DATASHEET OF
M74HC109RM13TR**

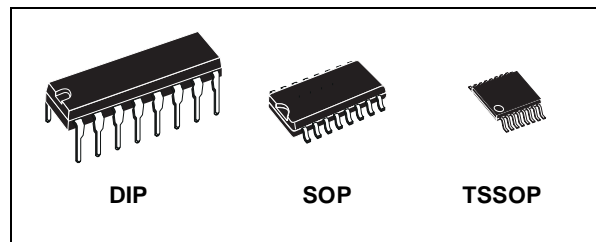




M74HC109

DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED :
 $f_{MAX} = 67\text{MHz}$ (TYP.) at $V_{CC} = 6\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 2\mu\text{A}$ (MAX.) at $T_A=25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4\text{mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH
 74 SERIES 109



ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC109B1R	
SOP	M74HC109M1R	M74HC109RM13TR
TSSOP		M74HC109TTR

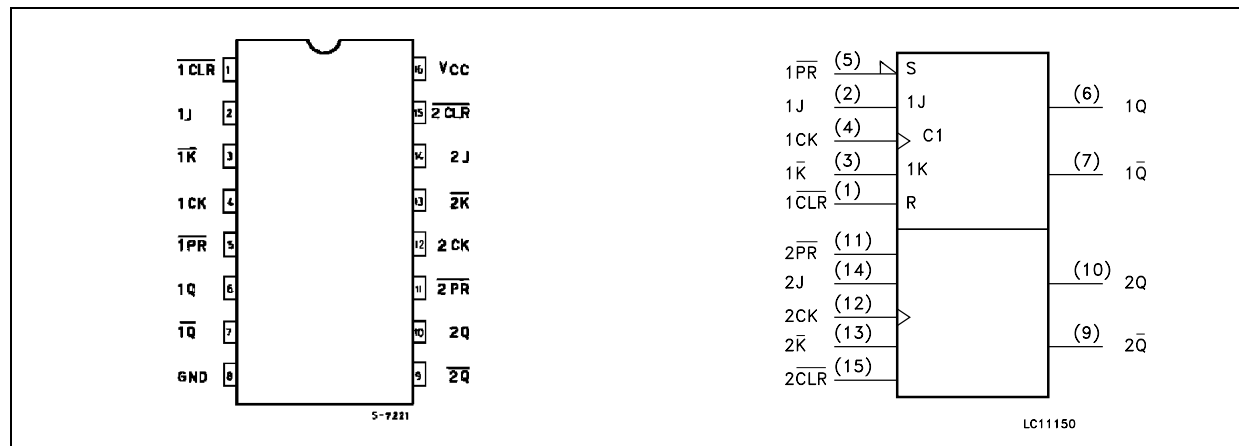
DESCRIPTION

The M74HC109 is an high speed CMOS DUAL J-K FLIP FLOP WITH PRESET AND CLEAR fabricated with silicon gate C²MOS technology. In accordance with the logic level on the J and \bar{K} input this device changes state on positive going transition of the clock pulse. CLEAR and PRESET

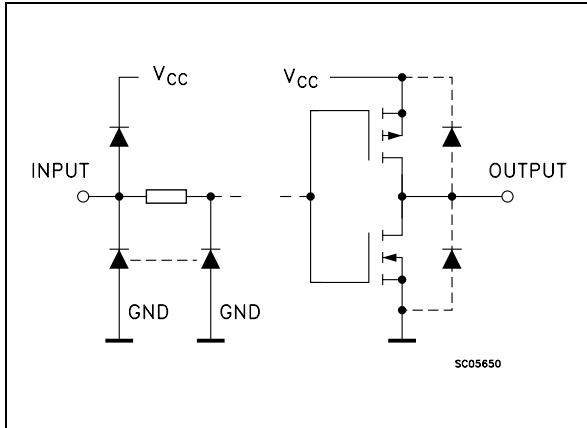
are independent of the clock and are accomplished by a logic low on the corresponding input.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

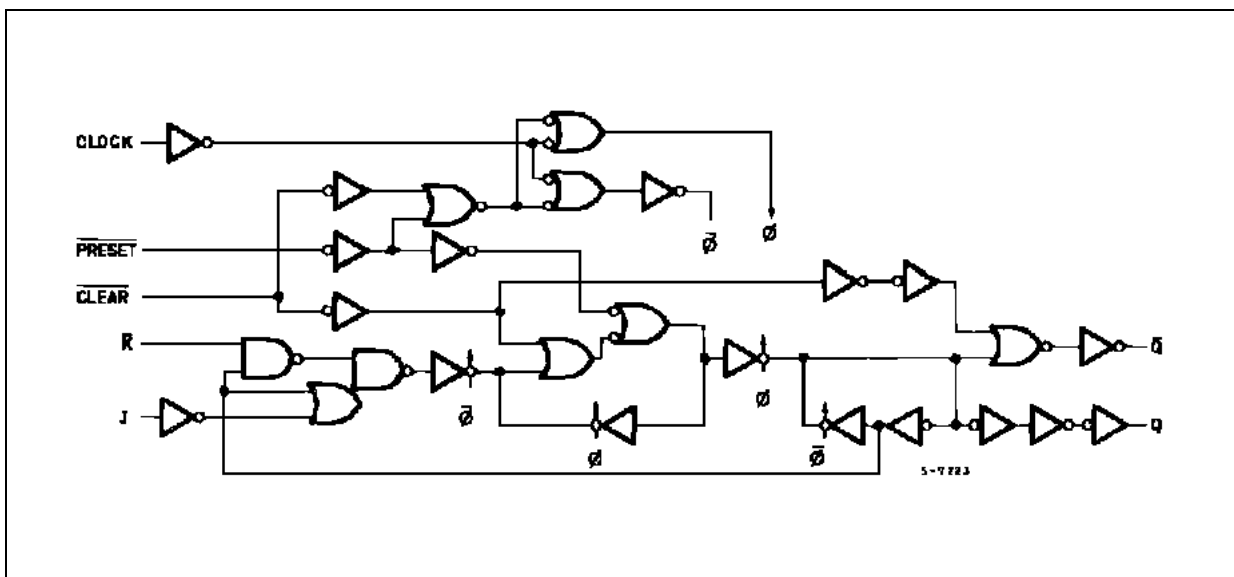
PIN No	SYMBOL	NAME AND FUNCTION
1,15	$\overline{1CLR}, \overline{2CLR}$	Asynchronous Reset Direct Input
2, 14, 3, 13	1J, 2J, 1K, 2K	Synchronous Inputs; Flip-Flops 1 and 2
4, 12	1CK, 2CK	Clock Input
5, 11	$\overline{1PR}, \overline{2PR}$	Asynchronous Set Direct Input (Active Low)
6, 10	1Q, 2Q	True Flip-Flop Outputs
7, 9	$\overline{1Q}, \overline{2Q}$	Complement Flip-Flop Outputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
\overline{CLR}	\overline{PR}	J	\overline{K}	CK	Q	\overline{Q}	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	----
H	H	L	H		Qn	\overline{Qn}	NO CHANGE
H	H	L	L		L	H	----
H	H	H	H		H	L	----
H	H	H	L		\overline{Qn}	Qn	TOGGLE
H	H	X	X		Qn	\overline{Qn}	NO CHANGE

X : Don't Care

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V_{CC}	Supply Voltage	2 to 6	V	
V_I	Input Voltage	0 to V_{CC}	V	
V_O	Output Voltage	0 to V_{CC}	V	
T_{op}	Operating Temperature	-55 to 125	°C	
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V _{OH}	High Level Output Voltage	2.0	I _O =-20 μA	1.9	2.0		1.9		1.9		V
		4.5	I _O =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I _O =-20 μA	5.9	6.0		5.9		5.9		
		4.5	I _O =-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I _O =-5.2 mA	5.68	5.8		5.63		5.60		
V _{OL}	Low Level Output Voltage	2.0	I _O =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I _O =20 μA		0.0	0.1		0.1		0.1	
		6.0	I _O =20 μA		0.0	0.1		0.1		0.1	
		4.5	I _O =4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I _O =5.2 mA		0.18	0.26		0.33		0.40	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			2		20		40	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

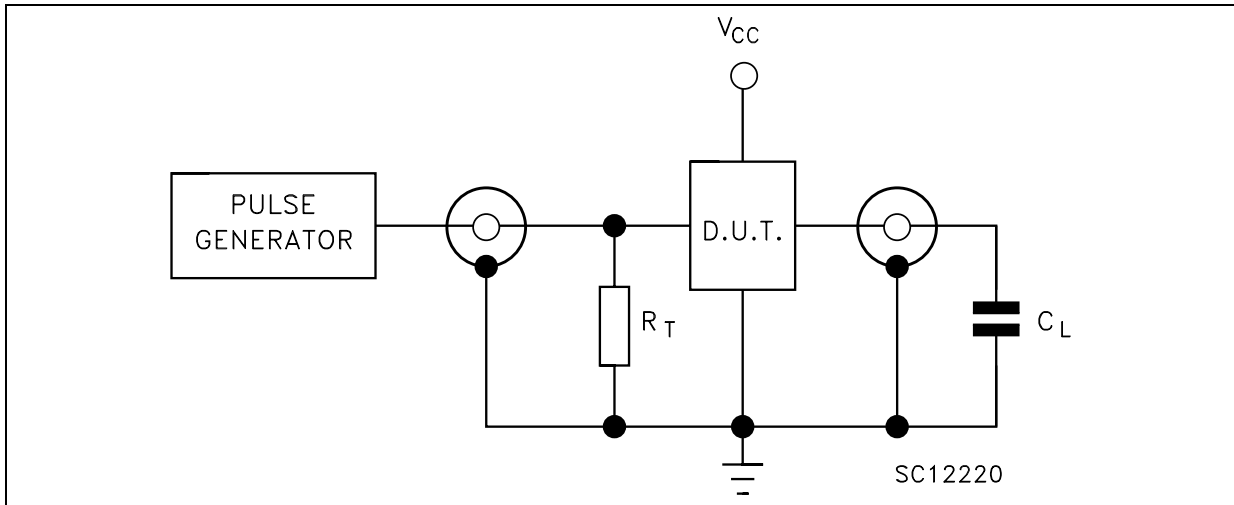
Symbol	Parameter	Test Condition		Value						Unit	
				$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{TLH} \ t_{THL}$	Output Transition Time	V_{CC} (V)			30	75		95		110	ns
				4.5	8	15		19		22	
				6.0	7	13		16		19	
$t_{PLH} \ t_{PHL}$	Propagation Delay Time (CK - Q, \bar{Q})	V_{CC} (V)			50	150		190		225	ns
				4.5	16	30		38		45	
				6.0	13	26		32		38	
$t_{PLH} \ t_{PHL}$	Propagation Delay Time (CLR, PR - Q, \bar{Q})	V_{CC} (V)			50	150		190		225	ns
				4.5	16	30		38		45	
				6.0	13	26		32		38	
f_{MAX}	Maximum Clock Frequency	V_{CC} (V)		6.2	17		5		4.2		MHz
				4.5	31	59		25		21	
				6.0	37	67		30		25	
$t_{W(H)} \ t_{W(L)}$	Minimum Pulse Width (CK)	V_{CC} (V)			15	75		95		110	ns
				4.5	6	15		19		22	
				6.0	6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CLR, PR)	V_{CC} (V)			15	75		95		110	ns
				4.5	6	15		19		22	
				6.0	6	13		16		19	
t_s	Minimum Set-Up Time	V_{CC} (V)			17	75		95		110	ns
				4.5	5	15		19		22	
				6.0	4	13		16		19	
t_h	Minimum Hold Time	V_{CC} (V)				0		0		0	ns
				4.5		0		0		0	
				6.0		0		0		0	
t_{REM}	Minimum Removal Time (CLR, PR)	V_{CC} (V)			13	50		65		75	ns
				4.5	4	10		13		15	
				6.0	3	9		11		13	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
				$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C_{IN}	Input Capacitance	V_{CC} (V)			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	V_{CC} (V)	5.0		41						pF

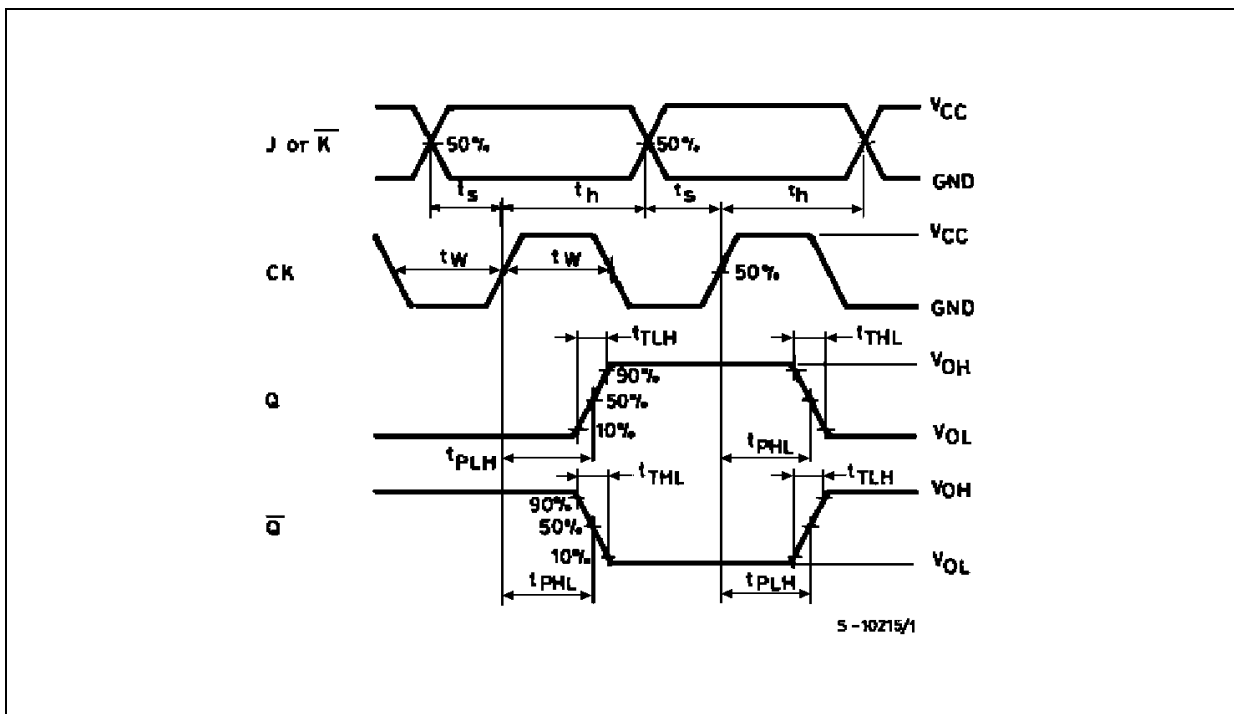
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

TEST CIRCUIT

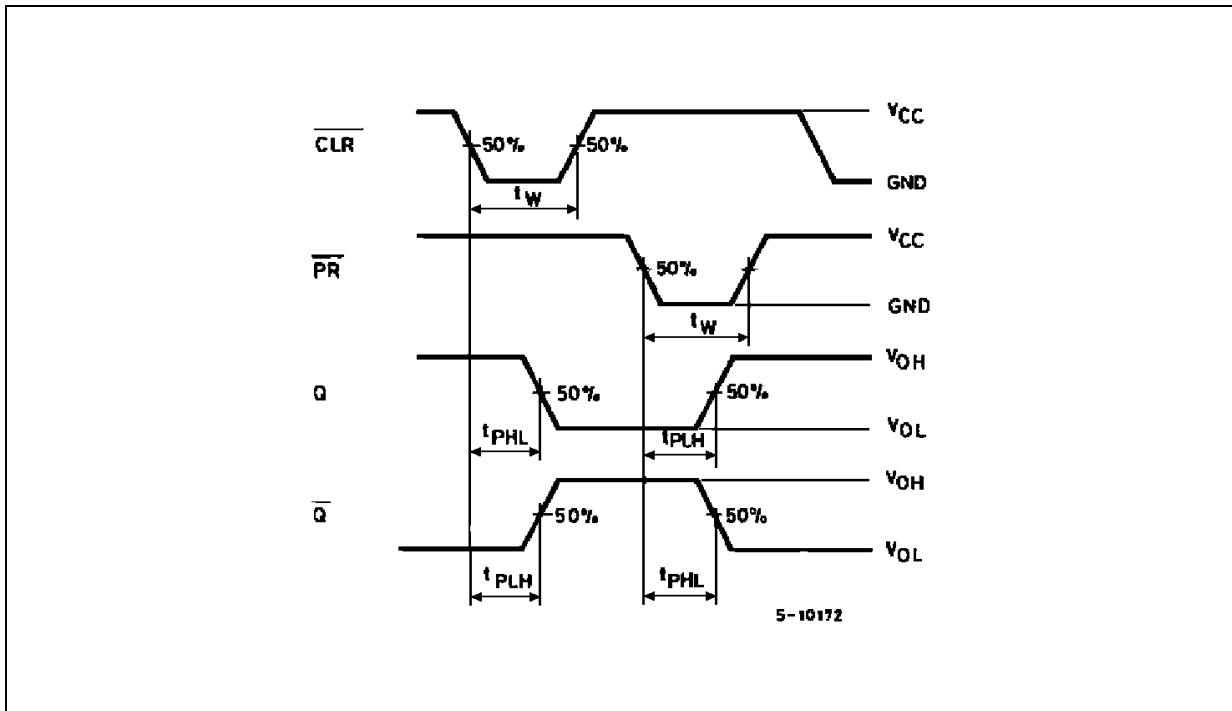


$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

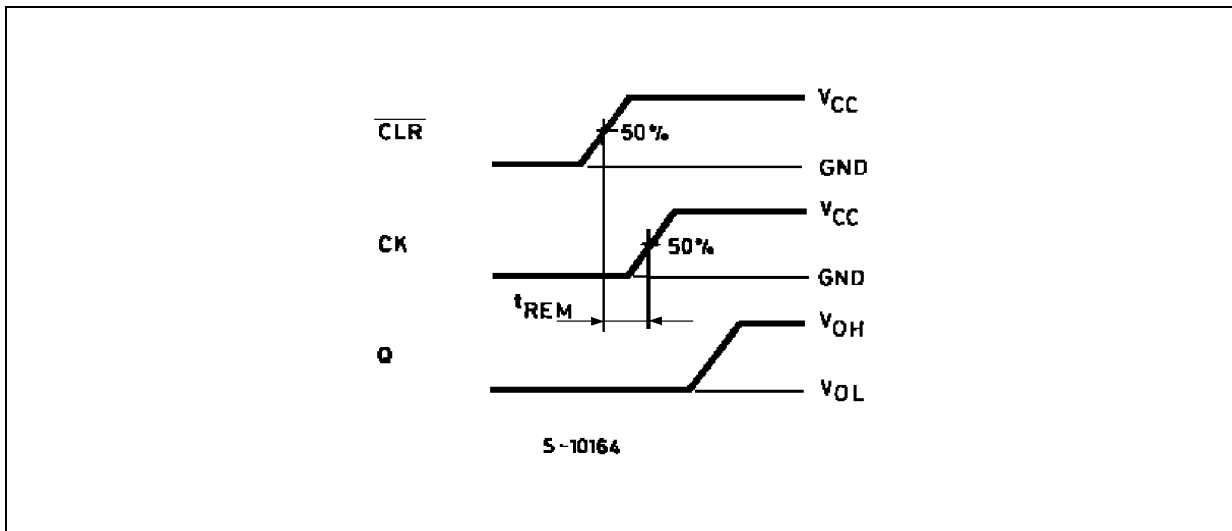
WAVEFORM 1: PROPAGATION DELAY TIMES, SETUP AND HOLD TIMES, MINIMUM PULSE WIDTH (CK) ($f=1\text{MHz}$; 50% duty cycle)



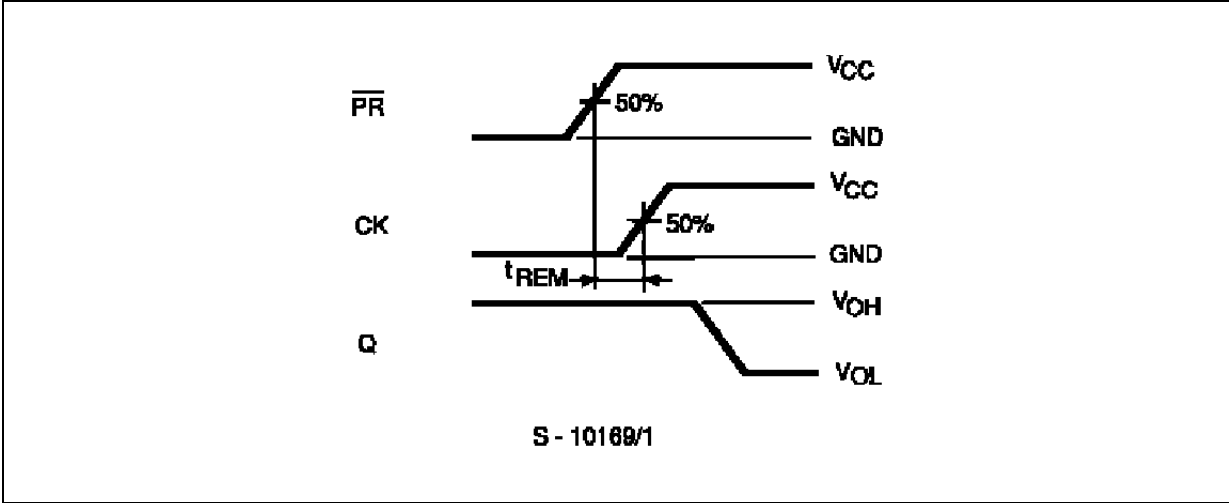
WAVEFORM 2 : PROPAGATION DELAY TIMES , MINIMUM PULSE WITDTH ($\overline{\text{CLR}}$), ($\overline{\text{PR}}$)
 (f=1MHz; 50% duty cycle)



WAVEFORM 3 : MINIMUM REMOVAL TIME ($\overline{\text{CLR}}$ to CK) (f=1MHz; 50% duty cycle)

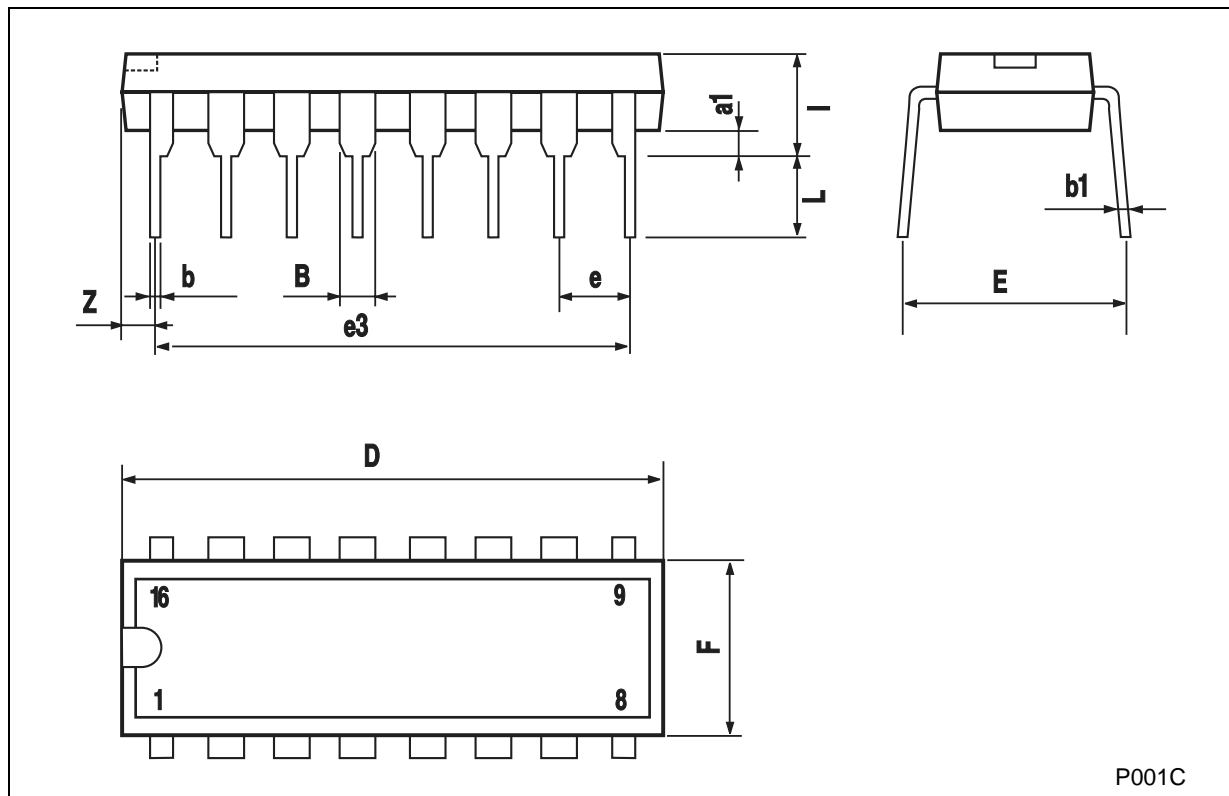


WAVEFORM 4 : MINIMUM REMOVAL TIME ($\overline{\text{PR}}$ to CK) (f=1MHz; 50% duty cycle)



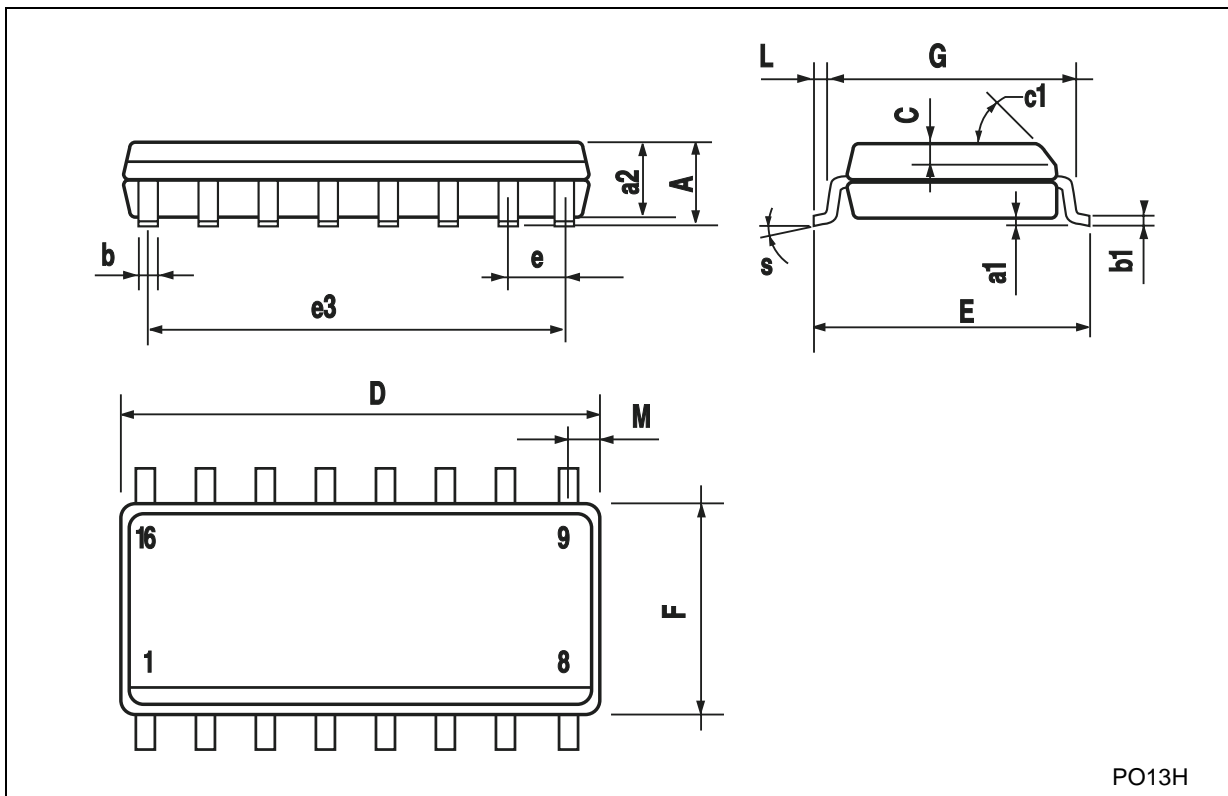
Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO-16 MECHANICAL DATA

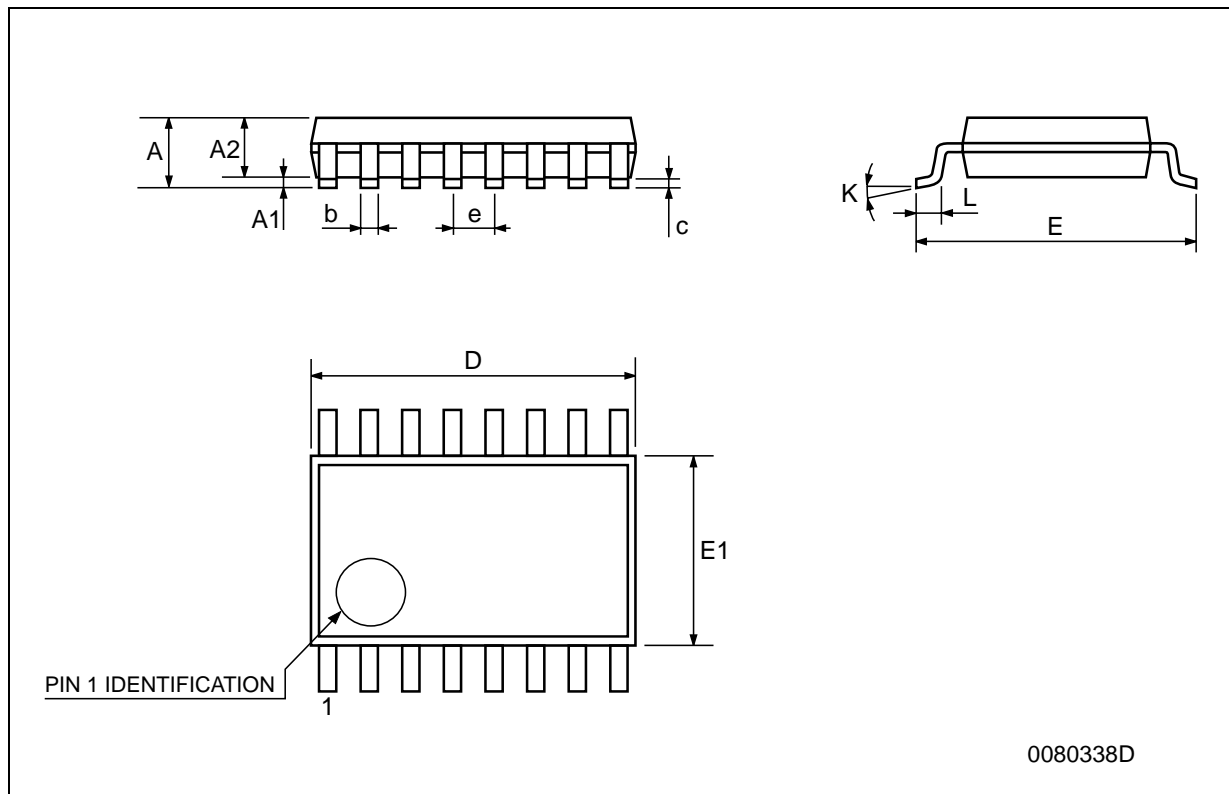
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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