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M66291GP/HP

ASSP (USB2.0 Device Controller)

REJ03F0125-0101Z
Rev1.01
2004.11.01

1 Overview

The M66291 is a general purpose USB (Universal Serial Bus) device controller compliant with the USB Specification Revision 2.0 and supports full speed transfer. The USB transceiver circuit is included, and the M66291 meets all transfer types which are defined in the USB specification. The M66291 has FIFO of 3 Kbytes for data transfer and can set 7 endpoints (maximum). Each endpoint can be set programmable of its transfer condition, so can correspond to each device class transfer system of USB.

1.1 Features

- USB Specification Revision 2.0 compliant
- Supports Full Speed (12 Mbps) transfer
- Built-in USB transceiver circuit
- Built-in oscillation buffer (Supports 6M/12M/24 MHz of oscillator) and PLL at 48 MHz
- Supports Vbus direct connection (5 V withstand voltage input), D+ pin pullup output
- Supports all transfer type which is defined in the USB specification.(Control transfer / Bulk transfer / Interrupt transfer / Isochronous transfer)
- Low power consumption operation (Average 15 mA at operation)
- Robust against signal distortion on USB transfer line due to SIE/DPLL(Digital Phase Lock Loop) of the original design
- Easy making enumeration program and timing design because hardware manages the device state / control transfer state (transition timing)
- Reduction of CPU load due to continuous transmit/receive mode (the mode for buffering several transaction data into FIFO) This enables high performance and throughput improvement.
- Up to 7 endpoints (EP0 to EP6) selectable
- Data transfer condition selectable for each endpoint (EP1 to EP6)
  Compatible to various applications (device class)
  - Data transfer type (Bulk transfer / Isochronous transfer / Interrupt transfer)
  - Transfer direction (IN, OUT)
  - Packet size
- Built-in FIFO buffer (3 Kbytes) for endpoints
- Buffering conditions of FIFO memory settable per endpoint (EP1 to EP6)
  - FIFO buffer size (up to 1Kbyte)
  - Presence/Absence of double buffer configuration (setting of buffer size x 2)
- Four pieces of configurable FIFO ports
  - Endpoint number allocation
  - Access method switching (CPU, DMAC)
  - Bit width (8-bit / 16-bit)
  - Endian switching
- ”Interrupt queuing function” that eliminates the need of complicated factor analysis
- Connectable to various CPU/DMAC
  - Bus width(8-bit / 16-bit)
  - Interface voltage(2.7V to 5.5V)
  - Interrupt signal and DMA control signal polarities settable
  - Supports multi-word DMA (burst)
- FIFO access cycle of maximum 24 Mbytes/sec

Applications
Support all PC peripheral built-in USB

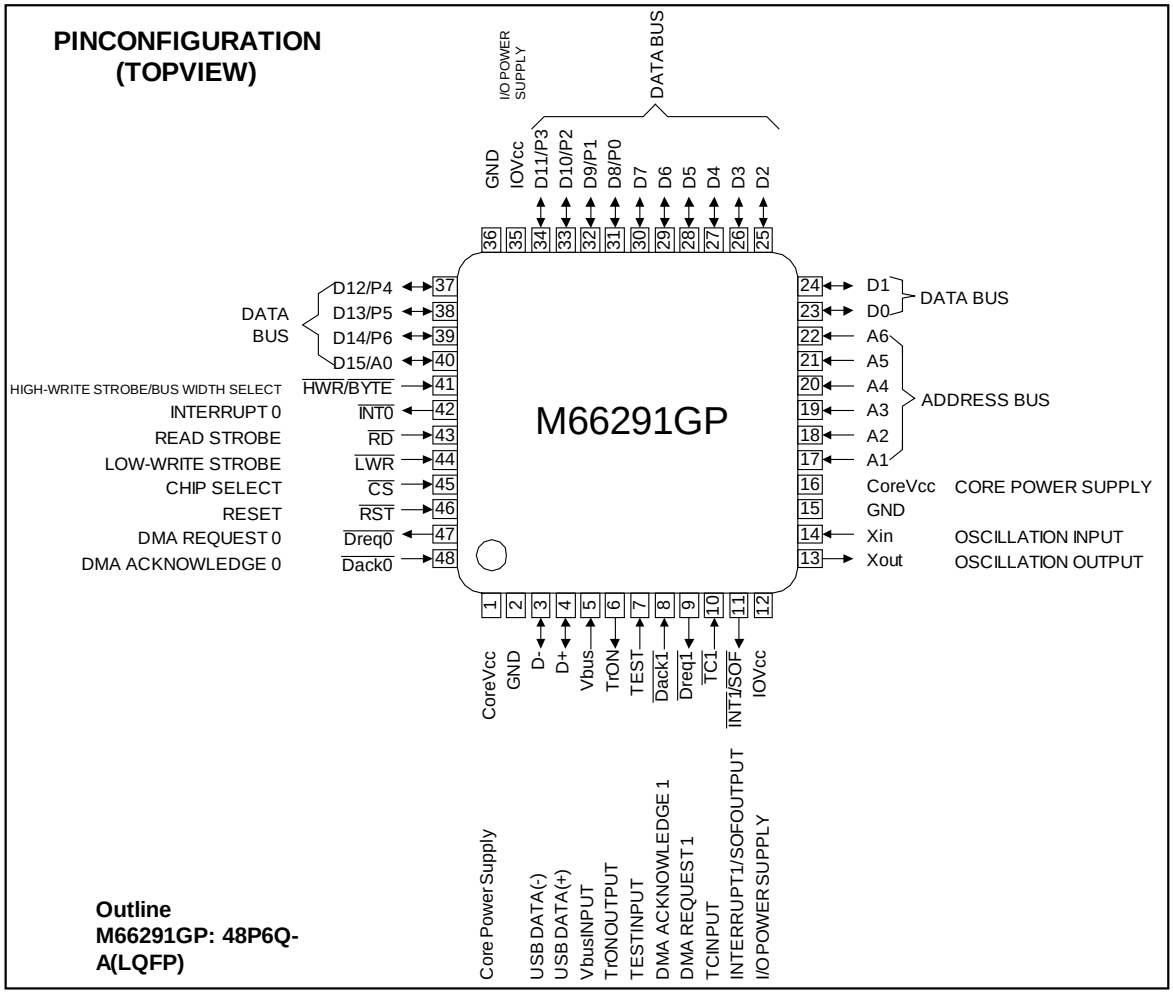


Figure 1.1-1 M66291GP Pin Configuration

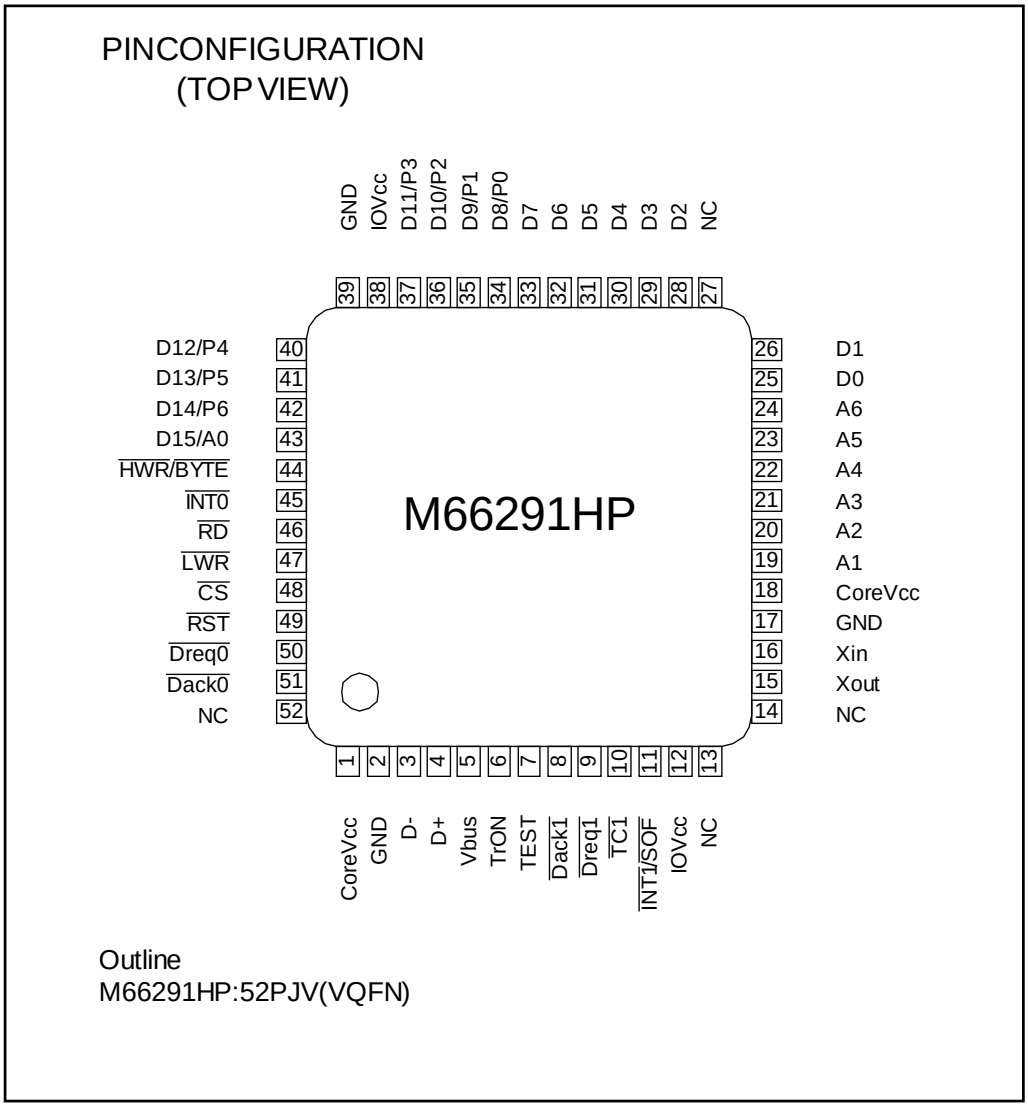


Figure1.1-2 M66291HP Pin Configuration

1.2 Block Diagram

The M66291 contains an USB-IP block, an I/O block, a bus interface unit (BIU), and a FIFO memory.

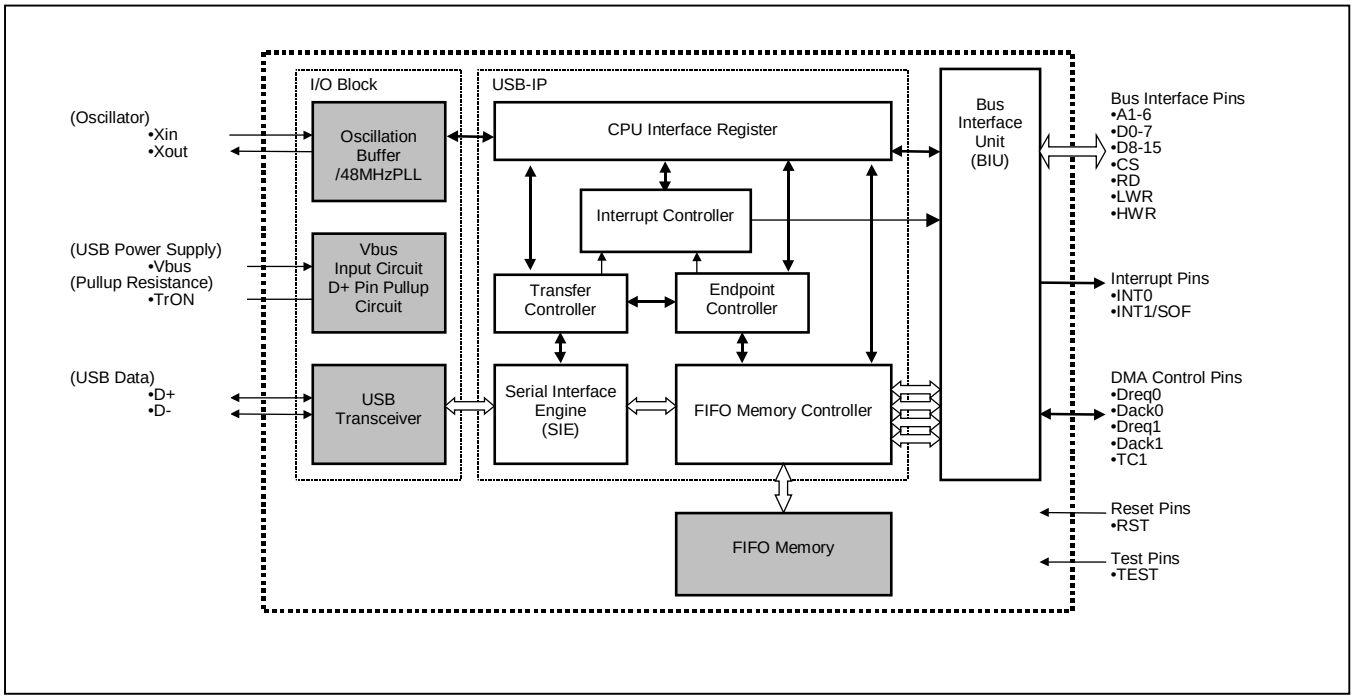


Figure 1.2 M66291 Block Diagram

1.2.1 USB-IP

The USB-IP block contains a serial interface engine, a transfer controller, an endpoint controller, a FIFO memory controller, an interrupt controller, and a CPU interface register.

(1) Serial Interface Engine (SIE)

The serial interface engine (SIE) executes low-order protocols processing of USB as follows:

- Extracts receive data/clock and generates transmit clock
- Serial - parallel conversion of transmit/receive data
- NRZI (Non Return Zero Invert) encoding and decoding
- Bit stuffing and destuffing
- SYNC (Synchronization pattern) and EOP (End Of Packet) detection
- USB address and endpoint detection
- CRC (Cyclic Redundancy Check) generation and checking

(2) Transfer Controller

The transfer controller executes device state transition control and control transfer sequence control.

(3) Endpoint Controller

The endpoint controller executes status control per endpoint.

(4) FIFO Memory Controller

The FIFO memory controller controls the write/read of the transmit/receive data at SIE (USB bus) side and internal bus (CPU bus) side under state control by the endpoint controller.

(5) Interrupt Controller

The interrupt controller outputs the status signals outputted by transfer controller and endpoint controller to INT0, INT1/SOF interrupt pins according to the CPU interface register setting.

(6) CPU Interface Register

The CPU interface register block is composed of the registers for mode setting, command setting and status reading.

1.2.2 Bus Interface Unit (BIU)

The bus interface unit (BIU) is a circuit to conform USB-IP to LSI external bus.

1.2.3 FIFO Memory

The FIFO memory is a FIFO for endpoint transmit/receive. It is possible to set 6 endpoints EP1 to EP6 in addition to EP0, the endpoint for control transfer.

1.2.4 I/O Block

The I/O block is composed of USB transceiver, oscillation buffer, 48 MHz PLL, Vbus input circuit and D+ pin pullup control circuit.

(1) USB Transceiver

The USB transceiver, conforming to the USB Specification Revision 2.0, is composed of a pair of 2 pieces of drivers D+/D- complying with full speed transfer mode, a pair of 2 pieces of single end receivers and a differential input receiver. A serial resistance for impedance matching is needed external to the chip.

(2) Oscillation Buffer, 48 MHz PLL

The 48 MHz clock with accuracy ± 0.25% is needed at the USB-IP block. The M66291 has a built-in oscillation buffer and a 48 MHz PLL. The PLL is capable of setting the multiplication number depending on the program and can therefore be connected with an external oscillation of 6, 12 or 24 MHz. Further, it can also be operated by the external 48 MHz clock without using the PLL function.

(3) Vbus Input Circuit, D+ Pin Pullup Control Circuit

The M66291 is capable of learning the connection status with host/hub by means of Vbus pin, and can inform the state of preparation at device side to host/hub by turning on/off the 1.5 KΩ D+ pin pullup.

The Vbus input buffer which is 5 V tolerant can be directly connected to the Vbus pin on the USB bus.

The current from TrON pin is supplied by Vbus input. Since the D+/D- pins of USB bus are operated at 0 V to 3.3 V, the TrON pin reduces the voltage to 3.3 V before output.

Since the USB is constantly pulled down by 15 KΩ at host/hub side when connected electrically, a current of 0.2 mA continuously flows into the D+ pin through the pullup resistance.

1.3 Pin Functions

Item	Pin name	Input/ Output	Function	Pin Count
Bus interface	D7~D0	Input/ Output	**Data Bus** This is a data bus to access the register from the system bus.	8
	D14/P6~ D8/P0	Input/ Output	**Data Bus / Port Signal** P6 to P0 are used as port signals when selected to 8-bit bus interface. D14 to D8 are used as data signals when selected to 16-bit bus interface.	7
	D15/A0	Input/ Output	**D15 Signal / A0 Signal** A0 (LSB) is used as an address signal when selected to 8-bit bus interface. D15 (MSB) is used as an data signal when selected to 16-bit bus interface.	1
	A6~A1	Input	**Address Bus** This is an address bus to access the register from the system bus.	6
	*CS	Input	**Chip Select** "L" level enables communication with the M66291.	1
	*LWR	Input	**Low-write Strobe** The lower data (D7 to D0) is written to the register at “L” level.	1
	*HWR/*BYTE	Input	**High-write Strobe / Bus Width Select** With the reset signal set to “H” level, the 8-bit bus interface is selected if this pin is at “L” level. Further, if this pin is at “H” level, the 16-bit bus interface is selected. When the 16-bit bus interface is selected, the upper data (D15 to D8) is written to the register at “L” level. Fix to “L” level when set to 8-bit bus interface.	1
	*RD	Input	**Read Strobe** Data are read from registers at "L" level	1
Interrupt interface	*INT0 (Note 1)	Output	**Interrupt 0** Interrupts are requested to the system at "L" level.	1
	*INT1/*SOF (Note 1)	Output	**Interrupt 1 / SOF Output** This pin is used as an interrupt 1 or as a SOF output pin to transmit USB SOF signal according to register setting.	1
DMA interface	*Dreq0 (Note 1)	Output	**DMA Request 0** This pin is used to request DMA transfer to endpoint FIFO for DMA channel 0.	1
	*Dack0 (Note 1)	Input	**DMA Acknowledge 0** This pin enables access of FIFO by DMA transfer for DMA channel 0.	1
	*Dreq1 (Note 1)	Output	**DMA Request 1** This pin is used to request DMA transfer to endpoint FIFO for DMA channel 1.	1

Item	Pin Name	Input/ Output	Function	Pin Count
DMA interface	*Dack1 (Note1)	Input	**DMA Acknowledge 1** This pin enables access of FIFO by DMA transfer for DMA channel 1.	1
	*TC1	Input	**Terminal Count 1** This pin indicates the final transfer cycle at “L” level for DMA channel 1. This is valid only in write cycle. Set to “H” level when not used.	1
USB interface	D+	Input/ Output	**USB Data (+)** D+ of USB. Connect an external resistance in series.	1
	D-	Input/ Output	**USB Data (-)** D- of USB. Connect an external resistance in series.	1
	Vbus	Input	**Vbus Input (with built-in pulldown resistance)** Connect to the Vbus of USB bus or to the 5V power supply. Connection or shutdown of the Vbus can be detected.	1
	TrON	Output	**TrON Output** This pin is connected to the D+ pullup resistance of 1.5 KΩ. This pin is used to control ON/OFF of the pullup resistance.	1
Others	*RST	Input	**Reset** This pin is used to initialize the values of the internal register or the counter at "L" level.	1
	Xin	Input	**Oscillator Input** These pins are used to input/output the signals of internal clock oscillation circuits. Connect a crystal unit between Xin and Xout pins. If an external clock signal is used, connect it to the Xin pin and leave the Xout pin open.	1
	Xout	Output	**Oscillator Output**	1
	TEST	Input	**TEST Input (with built-in pulldown resistance)** This pin is input for the test. Set to "L" level or keep open.	1
	CoreVcc (Note 2)	—	**Core Power Supply** These pins are used as the power source for internal logic, FIFO memory, PLL circuit, USB transceiver and oscillation buffer.	2
	IOVcc (Note 3)	—	**I/O Power Supply**	2
	GND	—	**Ground**	3

A pin preceded by an asterisk "*" is an active low pin.
(Example: *CS pin is an active low, $\overline{CS}$)

Note 1: The polarities of *Dreq, *Dack, *INT, and *SOF pins can be changed by the internal registers.

Note 2: The Xin, Xout, Vbus, D+ and D- pins are all driven by CoreVcc.

Note 3: The pins for bus interface, interrupt, DMA control, reset and test are all driven by IOVcc. See Figure 1.2.

2 Registers

How to Read Register Tables

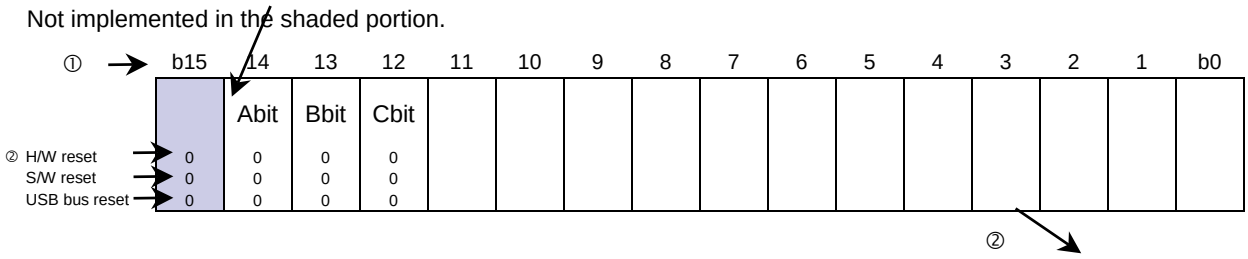
① Bit Numbers : Each register is connected with an internal bus of 16-bit wide, so the bit numbers of the registers located at odd addresses are b15-b8, and those at even addresses are b7-b0.

② State of Register at Reset :
Represents the initial state of each register immediately after reset with hexadecimal numbers. The "H/W reset" is the reset by an external reset signal; the "S/W reset" is the reset by the USBE bit of the USB Operation Enable Register.

③ At Read:
○ ... Read enabled
? ... Read disabled (Read value invalid)
0 ... Read always as 0
1 ... Read always as 1

④ At Write:
○ ... Write enabled
Δ ... Write enable conditionally (includes some conditions at write)
— ... Write disabled (Don't care "0" and "1" at write)
X ··· Write disabled

<Example of representation>
Not implemented in the shaded portion.



b	Bit name	Function	R	W
15	Reserved.		0	-
14	A bit (----------)	0: ---------- 1: ----------	0	0
13	B bit (----------)	0: ---------- 1: ----------	0	0
12	C bit (----------)	0: ---------- 1: ----------	0 ③	0 ④

The M66291 register mapping is shown in Figure 2.1 and Figure 2.2, and each register is described below.

Address	+1 address		+0 address		Reset state		
	b15	b8	b7	b0	H/W	S/W	USB bus
H'00	USB Operation Enable Register				H'0000	-	-
H'02	Remote Wakeup Register				H'0000	H'0000	-
H'04	Sequence Bit Clear Register				H'0000	H'0000	-
H'06	(Reserved)						
H'08	USB_Address Register				H'0000	H'0000	H'0000
H'0A	Isochronous Status Register				H'0000	H'0000	-
H'0C	SOF Control Register				H'0000	H'0000	-
H'0E	Polarity Set Register				H'0000	H'0000	-
H'10	Interrupt Enable Register 0				H'0000	H'0000	-
H'12	Interrupt Enable Register 1				H'0000	H'0000	-
H'14	Interrupt Enable Register 2				H'0000	H'0000	-
H'16	Interrupt Enable Register 3				H'0000	H'0000	-
H'18	Interrupt Status Register 0				H'0000	H'0000	Note
H'1A	Interrupt Status Register 1				H'0000	H'0000	-
H'1C	Interrupt Status Register 2				H'0000	H'0000	-
H'1E	Interrupt Status Register 3				H'0000	H'0000	-
H'20	Request Register				H'0000	H'0000	-
H'22	Value Register				H'0000	H'0000	-
H'24	Index Register				H'0000	H'0000	-
H'26	Length Register				H'0000	H'0000	-
H'28	Control Transfer Control Register				H'0000	-	-
H'2A	EP0 Packet Size Register				H'0008	-	-
H'2C	Automatic Response Control Register				H'0000	-	-
H'2E	(Reserved)						
H'30	EP0_FIFO Select Register				H'0000	-	-
H'32	EP0_FIFO Control Register				H'0800	-	-
H'34	EP0_FIFO Data Register				????	-	-
H'36	EP0_FIFO Continuous Transmit Data Length Register				H'0000	-	-

Note : Refer to each register described below.

Figure 2.1 Register Mapping (1)

Address	+1 address		+0 address		Reset state		
	b15	b8	b7	b0	H/W	S/W	USB bus
H'38	(Reserved)						
H'3A	(Reserved)						
H'3C	(Reserved)						
H'3E	(Reserved)						
H'40	CPU_FIFO Select Register				H'0000	-	-
H'42	CPU_FIFO Control Register				H'0800	-	-
H'44	CPU_FIFO Data Register				????	-	-
H'46	SIE_FIFO Status Register				H'0000	-	-
H'48	D0_FIFO Select Register				H'0000	-	-
H'4A	D0_FIFO Control Register				H'0800	-	-
H'4C	D0_FIFO Data Register				????	-	-
H'4E	DMA0_Transaction Count Register				H'0000	-	-
H'50	D1_FIFO Select Register				H'0000	-	-
H'52	D1_FIFO Control Register				H'0800	-	-
H'54	D1_FIFO Data Register				????	-	-
H'56	DMA1_Transaction Count Register				H'0000	-	-
H'58	FIFO Status Register				H'0000	H'0000	-
H'5A	Port Control Register				H'0000	-	-
H'5C	Port Data Register				H'0000	-	-
H'5E	Drive Current Adjust Register				H'0000	-	-
H'60	EP1 Configuration Register 0				H'0000	-	-
H'62	EP1 Configuration Register 1				H'0040	-	-
H'64	EP2 Configuration Register 0				H'0000	-	-
H'66	EP2 Configuration Register 1				H'0040	-	-
H'68	EP3 Configuration Register 0				H'0000	-	-
H'6A	EP3 Configuration Register 1				H'0040	-	-
H'6C	EP4 Configuration Register 0				H'0000	-	-
H'6E	EP4 Configuration Register 1				H'0040	-	-
H'70	EP5 Configuration Register 0				H'0000	-	-
H'72	EP5 Configuration Register 1				H'0040	-	-
H'74	EP6 Configuration Register 0				H'0000	-	-
H'76	EP6 Configuration Register 1				H'0040	-	-

Figure 2.2 Register Mapping (2)

2.1 USB Operation Enable Register

■ USB Operation Enable Register (USB_ENABLE) <Address : H'00>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
XCKE	PLLC	Xtal		SCKE	USBPC	Tr_on									USBE
0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -

<H/W reset : H'0000>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15	XCKE Oscillation Buffer Enable	0 : Disable oscillation buffer (Disable clock supply to inside PLL) 1 : Enable oscillation buffer (Enable clock supply to inside PLL)	○	○
14	PLLC PLL Operation Enable	0 : Disable PLL (PLL through) 1 : Enable PLL	○	○
13~12	Xtal Clock Select	00 : External clock frequency : 48 MHz (PLL through) 10 : External clock frequency : 24 MHz 01 : External clock frequency : 12 MHz 11 : External clock frequency : 6 MHz	○	○
11	SCKE Internal Clock Enable	0 : Disable Internal clock 1 : Enable Internal clock	○	○
10	USBPC USB Transceiver Power Control	0 : Disable USB transceiver 1 : Enable USB transceiver	○	○
9~8	Tr_on Tr_on Output Control	00 : TrON output ="Hi-Z" (SIE operate stop) 01 : TrON output ="L" 10 : Reserved 11 : TrON output ="H"	○	○
7~1	Reserved. Set it to "0".		0	0
0	USBE USB Module Operation Enable	0 : S/W reset state 1 : S/W reset state release	○	○

.

(1) XCKE (Oscillation Buffer Enable) Bit (b15)

This bit sets enable/disable of the oscillation buffer.
The output clock from the oscillation buffer is supplied to the PLL.
Refer to Figure 2.3.

(2) PLLC (PLL Operation Enable) Bit (b14)

This bit sets enable/disable of PLL.
When this bit is set to "1", the external clock into the PLL is multiplied according to the value set in the Xtal bits before being output to the core block. Set the XCKE bit to "1" and wait until the oscillation circuit starts and becomes stable before setting this bit to "1".
When this bit is set to "0", PLL stops operation and the external clock into the PLL is output to the core block without being multiplied. Hence, be sure to supply the 48 MHz clock to the oscillation buffer when setting this bit to "0".
Refer to Figure 2.3.

(3) Xtal (Clock Select) Bits (b13~b12)

These bits set the multiplication factor of the external clock into PLL.
Since it is necessary to supply 48 MHz to the core block, the setting values of these bits are determined by the clock frequency to be input into the PLL.
Refer to Figure 2.3.

(4) SCKE (Internal Clock Enable) Bit (b11)

This bit sets the clock supply into the core block.
Set the PLLC bit to "1" and wait until the oscillation of the PLL stabilizes before setting this bit to "1".
Refer to Figure 2.3.

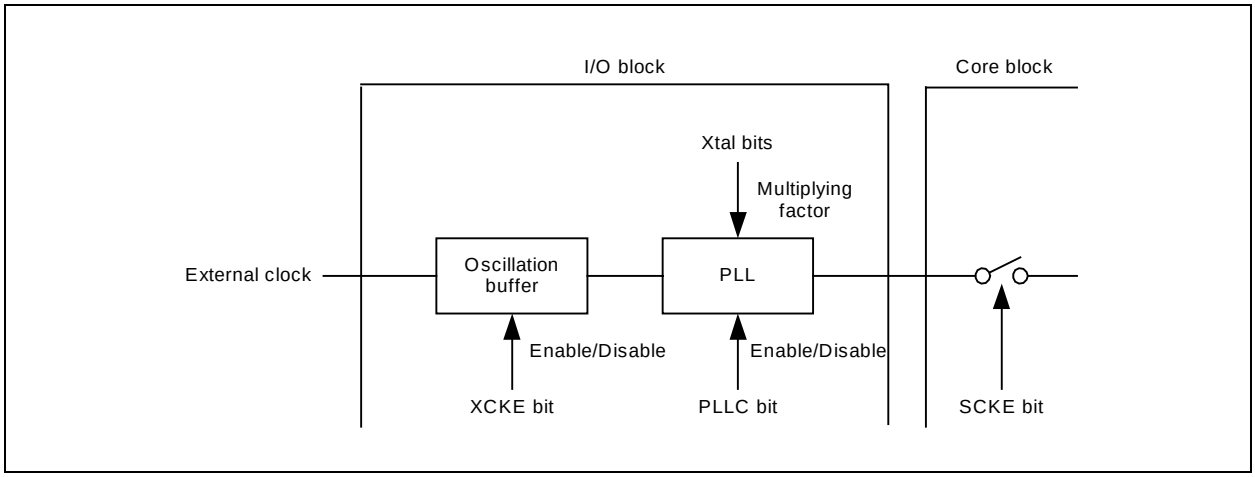


Figure 2.3 Clock Control

(5) USBPC (USB Transceiver Power Control) Bit (b10)

This bit sets the enable/disable of the USB transceiver block of I/O block.
Even if this bit is set to "0", it is possible to receive the resume signal during the Suspended state (DVSQ bits = "1xx"). It is necessary that the Tr_on bits be set to "x1" (during operation of SIE block).

(6) Tr_on (Tr_on Output Control) Bits (b9~b8)

These bits set the TrON signal output from I/O block and the enable/disable of SIE block in core block.

(7) USBE (USB Module Operation Enable) Bit (b0)

This bit sets S/W reset.
When this bit is set to "0", the M66291 enters the S/W reset state and the registers are set to their S/W reset state.
.

2.2 Remote Wakeup Register

■ Remote Wakeup Register (REMOTE_WAKEUP) <Address : H'02>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	WKUP 0 0 -

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15~1	Reserved. Set it to "0".		0	0
0	WKUP Remote Wakeup	■ Read 0 : Do not output the remote wakeup signal 1 : Output the remote wakeup signal ■ Write 0 : Invalid (Ignored when written) 1 : Output the remote wakeup signal	○	○

(1) WKUP (Remote Wakeup) Bit (b0)

This bit controls the output of the remote wakeup signal (K state output).
This bit is valid only when the device state is "suspend" (DVSQ bits = "1xx"). The writing of "1" to this bit is ignored when the device state is not suspend.
When "1" is written to this bit, the K state is output for 10 ms. The bit is automatically cleared to "0" after K state output.
The bus idle state continues (this WKUP bit = "1") for 2 ms after the Suspend state is detected when "1" is written to this bit before outputting the K state for 10 ms.
The 2 ms and 10 ms time intervals are counted using a clock. Make sure that the counting stops if the clock is not supplied (Note).

Note : SCKE bit = "0" when XCKE bit = "1 ", or XCKE bit = "0".

2.3 Sequence Bit Clear Register

■ Sequence Bit Clear Register (SEQUENCE_BIT) <Address : H'04>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
									SQCLR						
0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		0	0
6~0	SQCLR Sequence Bit Clear	■ Write 0 : Invalid (Ignored when written) 1 : Clear Sequence bit b6 corresponds to EP6, ---b1 corresponds to EP1 and b0 corresponds to EP0.	0	○

(1) SQCLR (Sequence Bit Clear) Bits (b6~b0)

These bits clear the sequence bit (the bit controlled by H/W) and turns the data PID into DATA 0 PID. This bit immediately returns to "0" after writing "1".
In the transfers after the sequence bit is cleared, the sequence bit is toggled through H/W control.
At S/W reset (USBE bit = "1") and USB bus reset, the sequence bit of each endpoint is not cleared.

Note : Be sure to set the response PID of the endpoint whose sequence bit is desired to be cleared to NAK (EP0_PID bits = "00"/EPi_PID bits = "00") before writing "1" to this bit.

2.4 USB_Address Register

■ USB_Address Register (USB_ADDRESS) <Address : H'08>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
									USB_Addr						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : H'0000>

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		0	0
6~0	USB_Addr USB_Address	■ Read USB address assigned by the host	○	×

(1) USB_Addr (USB_Address) Bits (b6~b0)

These bits store the USB address assigned by the host.
On receiving SET_ADDRESS request from the host at default state (DVSQ bits = "001"), the requested device address value is set to this register when the response is made through zero-length packet in status stage.
The device address value is set to these bits at the time of zero-length packet transmit even if the ASAD bit is set to "0" (automatic response is invalid).

2.5 Isochronous Status Register

■ Isochronous Status Register (ISOCHRONOUS_STATUS) <Address : H'0A>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
				FMOD	FRNM										
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15~12	Reserved. Set it to "0".		?	0
11	FMOD Frame Number Mode	0 : At SOF receive 1 : At Isochronous transfer complete	○	○
10~0	FRNM Frame Number	Stores the frame number	○	×

This register is valid only for isochronous transfer. In other words, the register is valid status for the endpoint that is set EPi_TYP bits to "11".

(1) FMOD (Frame Number Mode) Bit (b11)

This bit sets the storage timing of the frame number to be stored to the FRNM bits.
When this bit is set to "0", when the SOF packet is properly received, the frame number of the received SOF packet gets stored.
When this bit is set to "1", when the isochronous packet transfer completes, the frame number of the properly received SOF packet gets stored.

(2) FRNM (Frame Number) Bits (b10~b0)

The frame number is stored in the FRNM with the timing set by the FMOD bit of this register. Here, the SOFR bit is set to "1".

2.6 SOF Control Register

■ SOF Control Register (SOF_CNT) <Address : H'0C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
SOFOE	SOFA														
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15	SOFOE SOF Output Enable	0 : Disable SOF signal output 1 : Enable SOF signal output	○	○
14	SOFA SOF Polarity	0 : "L" active 1 : "H" active	○	○
13~0	Reserved. Set it to "0".		0	0

(1) SOFOE (SOF Output Enable) Bit (b15)

This bit sets the enable/disable of SOF signal output.
When this bit is set to "1", if SOF packet is received, the INT1/SOF pin outputs SOF signal. The output polarity is set by SOFA bit.
The SOF signal outputs the pulse (approx. 0.67 us) equivalent to 32 clocks of the 48 MHz clock after receiving the PID field. Refer to Figure 2.4.
Since the INT1 pin is double-function pin, do not allocate the interrupt signal to this pin when using the SOF signal (Set by the Polarity Set Register).

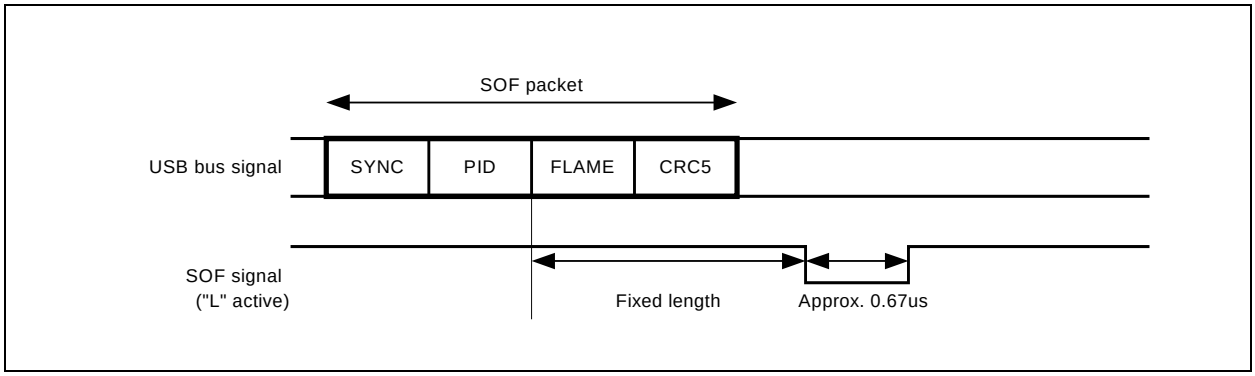


Figure 2.4 SOF Signal Output Timing

(2) SOFA (SOF Polarity) Bit (b14)

This bit sets the output polarity of SOF signal.

2.7 Polarity Set Register

■ Polarity Set Register (POLARITY_CNT) <Address : H'0E>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
VB01	RM01	SF01	DS01	CT01	BE01	NR01	RD01						RDYM	INTL	INTA
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15	VB01 Vbus Interrupt Assign	0 : Assigns to INT0 pin 1 : Assigns to INT1 pin (Note)	○	○
14	RM01 Resume Interrupt Assign	0 : Assigns to INT0 pin 1 : Assigns to INT1 pin (Note)	○	○
13	SF01 SOF Detect Interrupt Assign	0 : Assigns to INT0 pin 1 : Assigns to INT1 pin (Note)	○	○
12	DS01 Device State Transition Interrupt Assign	0 : Assigns to INT0 pin 1 : Assigns to INT1 pin (Note)	○	○
11	CT01 Control Transfer Transition Interrupt Assign	0 : Assigns to INT0 pin 1 : Assigns to INT1 pin (Note)	○	○
10	BE01 Buffer Empty/Size Over Error Interrupt Assign	0 : Assigns to INT0 pin 1 : Assigns to INT1 pin (Note)	○	○
9	NR01 Buffer Not Ready Interrupt Assign	0 : Assigns to INT0 pin 1 : Assigns to INT1 pin (Note)	○	○
8	RD01 Buffer Ready Interrupt Assign	0 : Assigns to INT0 pin 1 : Assigns to INT1 pin (Note)	○	○
7~3	Reserved. Set it to "0".		0	0
2	RDYM Buffer Ready Mode	0 : Clears the EPB_RDY bits by reading/writing all data of buffer 1 : Clears the EPB_RDY bits by writing "0" to EPB_RDY bit	○	○
1	INTL Interrupt Output Sense	0 : Edge sensitive output 1 : Level sensitive output	○	○
0	INTA Interrupt Polarity	0 : "L" active or change from "H" to "L" 1 : "H" active or change from "L" to "H"	○	○

Note : In order to allocate the interrupt output signal to the INT1/SOF pin, set the SOF signal output to "disable" (SOFOE bit = "0").

(1) VB01 (Vbus Interrupt Assign) Bit (b15)

This bit selects the pin to output the Vbus interrupt signal.

(2) RM01 (Resume Interrupt Assign) Bit (b14)

This bit selects the pin to output the resume interrupt signal.

(3) SF01 (SOF Detect Interrupt Assign) Bit (b13)

This bit selects the pin to output the SOF detect interrupt signal.

(4) DS01 (Device State Transition Interrupt Assign) Bit (b12)

This bit selects the pin to output device state transition interrupt signal.

(5) CT01 (Control Transfer Transition Interrupt Assign) Bit (b11)

This bit selects the pin to output the control transfer transition interrupt signal.

(6) BE01 (Buffer Empty/Size Over Error Interrupt Assign) Bit (b10)

This bit selects the pin to output the buffer empty/size over error interrupt signal.

(7) NR01 (Buffer Not Ready Interrupt Assign) Bit (b9)

This bit selects the pin to output the buffer not ready interrupt signal.

(8) RD01 (Buffer Ready Interrupt Assign) Bit (b8)

This bit selects the pin to output the buffer ready interrupt signal.

(9) RDYM (Buffer Ready Mode) Bit (b2)

This bit selects the method of clearing the buffer ready interrupt.
When this bit is set to "0", the EPB_RDY bit is cleared to "0" after the CPU side buffer data are all read out or after the writing of transmit data completes.
When this bit is set to "1", the EPB_RDY bit is cleared to "0" by writing "0" to the EPB_RDY bit.
For details, refer to "EPB_RDY bit".

Note : Refer to "3.2 FIFO Buffer" for CPU/SIE side.

(10) INTL (Interrupt Output Sense) Bit (b1)

This bit sets the sense mode for interrupt output from INT0 or INT1 pin.
When this bit is set to "0", the INT0 or INT1 pin notifies the occurrence of interrupt at the edge set by the INTA bit.
During edge sensitive output, when "0" is written to each interrupt factor bit to clear the interrupt, the output signal outputs the negate value one time. If the other interrupt factor bits are set to "1", the occurrence of interrupt again is notified at the edge. The negate period is equivalent to 32 clocks (approx. 667 ns) of the 48 MHz clock.
In case the clock is not supplied (Note), the negate period does not occur. Make sure not to miss the interrupt when Vbus interrupt or resume interrupt occurs.
When this bit is set to "1", the INT0 or INT1 pin notifies the occurrence of interrupt at the level set by the INTA bit.
During level sensitive output, the negate fails to work unless all interrupt factor bits are cleared even if "0" is written to clear the interrupt to the interrupt factor bits.
Refer to Figure 2.5 and "3.1 Interrupt Function".

Note : SCKE bit = "0" when XCKE bit = "1 " , or XCKE bit = "0".

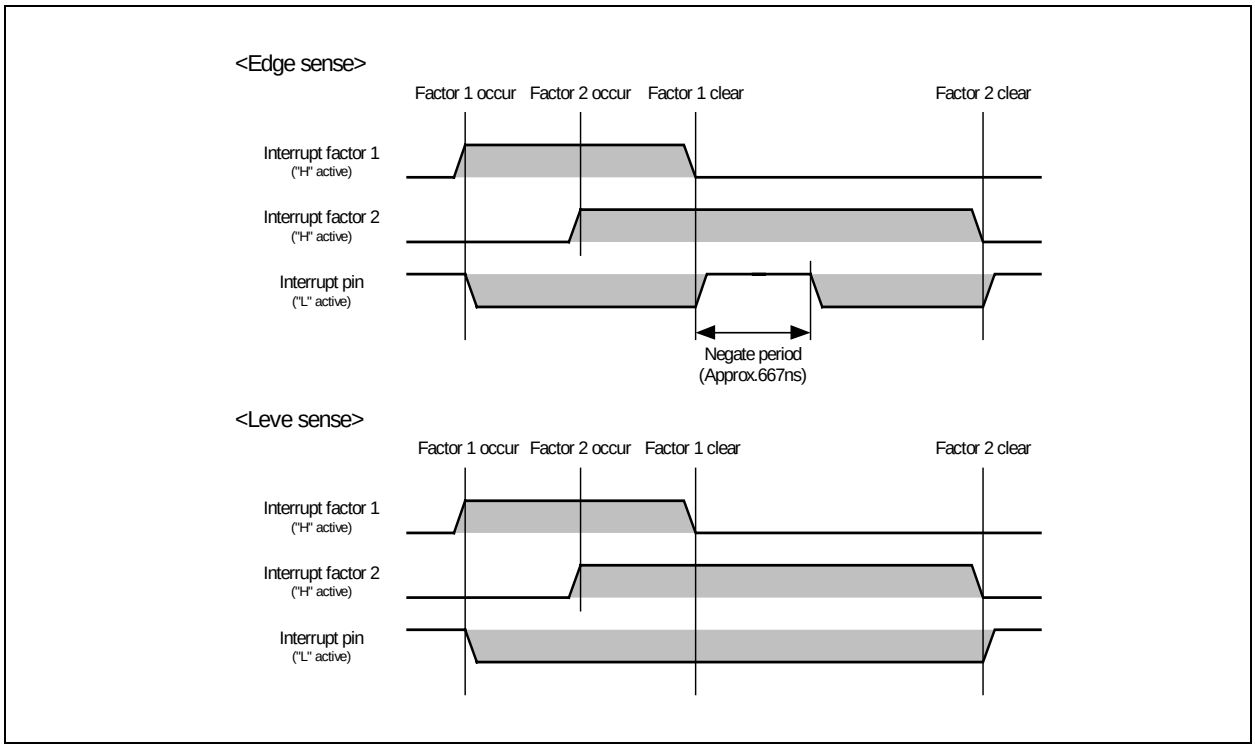


Figure 2.5 Interrupt Signal Output Timing

(11) INTA (Interrupt Polarity) Bit (b0)

This bit sets the interrupt signal output polarity.
When this bit is set to "0", the occurrence of interrupt is notified when;
In case of edge sense (INTL bit = "0") : Change from "H" to "L"
In case of level sense (INTL bit = "1") : "L" level

When this bit is set to "1", the occurrence of interrupt is notified when;
In case of edge sense (INTL bit = "0") : Change from "L" to "H"
In case of level sense (INTL bit = "1") : "H" level

2.8 Interrupt Enable Register 0

■ Interrupt Enable Register 0 (INT_ENABLE0) <Address : H'10>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	INTNE	INTRE	URST	SADR	SCFG	SUSP	WDST	RDST	CMPL	SERR
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15	VBSE Vbus Interrupt Enable	0 : Disable interrupt 1 : Enable interrupt (Interrupt occurs when VBUS bit is set to “1”)	○	○
14	RSME Resume Interrupt Enable	0 : Disable interrupt 1 : Enable interrupt (Interrupt occurs when RESM bit is set to "1")	○	○
13	SOFE SOF Detect Interrupt Enable	0 : Disable interrupt 1 : Enable interrupt (Interrupt occurs when SOFR bit is set to "1")	○	○
12	DVSE Device State Transition Interrupt Enable	0 : Disable interrupt 1 : Enable interrupt (Interrupt occurs when DVST bit is set to "1")	○	○
11	CTRE Control Transfer Transition Interrupt Enable	0 : Disable interrupt 1 : Enable interrupt (Interrupt is occurs when CTRT bit is set to "1")	○	○
10	BEMPE Buffer Empty/Size Over Error Interrupt Enable	0 : Disable interrupt 1 : Enable interrupt (Interrupt is occurs when BEMP bit is set to "1")	○	○
9	INTNE Buffer Not Ready Interrupt Enable	0 : Disable interrupt 1 : Enable interrupt (Interrupt occurs when INTN bit is set to "1")	○	○
8	INTRE Buffer Ready Interrupt Enable	0 : Disable interrupt 1 : Enable interrupt (Interrupt occurs when INTR bit is set to "1")	○	○
7	URST USB Reset Detect	0 : Disable DVST bit set 1 : Enable DVST bit set	○	○
6	SADR SET_ADDRESS Execute	0 : Disable DVST bit set 1 : Enable DVST bit set	○	○
5	SCFG SET_CONFIGURATION Execute	0 : Disable DVST bit set 1 : Enable DVST bit set	○	○
4	SUSP Suspend Detect	0 : Disable DVST bit set 1 : Enable DVST bit set	○	○
3	WDST Control Write Transfer Status Stage	0 : Disable CTRT bit set 1 : Enable CTRT bit set	○	○
2	RDST Control Read Transfer Status Stage	0 : Disable CTRT bit set 1 : Enable CTRT bit set	○	○
1	CMPL Control Transfer Complete	0 : Disable CTRT bit set 1 : Enable CTRT bit set	○	○
0	SERR Control Transfer Sequence Error	0 : Disable CTRT bit set 1 : Enable CTRT bit set	○	○

This register sets enable of interrupt and enable/disable of setting DVST and CTRT bits to “1”.
Also refer to “3.1 Interrupt Function”.

(1) VBSE (Vbus Interrupt Enable) Bit (b15)

This bit sets enable/disable of Vbus interrupt.
When this bit is set to "1", the interrupt occurs if VBUS bit is set to "1".
This bit is capable of writing/reading even if the clock is not supplied (Note).

Note : At SCKE bit = "0" when XCKE bit = "1 " or XCKE bit = "0".

(2) RSME (Resume Interrupt Enable) Bit (b14)

This bit sets enable/disable of resume interrupt.
When this bit is set to "1", the interrupt occurs if RESM bit is set to "1".
This bit is capable of writing/reading even if the clock is not supplied (Note).

Note : At SCKE bit = "0" when XCKE bit = "1 " or XCKE bit = "0".

(3) SOFE (SOF Detect Interrupt Enable) Bit (b13)

This bit sets enable/disable of SOF detect interrupt.
When this bit is set to "1", the interrupt occurs if SOFR bit is set to "1".

(4) DVSE (Device State Transition Interrupt Enable) Bit (b12)

This bit sets enable/disable of device state transition interrupt.
When this bit is set to "1", the interrupt occurs if DVST bit is set to "1".
The Conditions the DVST bit set are depend on the URST, SADR, SCFG or SUSP.

(5) CTRE (Control Transfer Transition Interrupt Enable) Bit (b11)

This bit sets enable/disable of control transfer transition interrupt.
When this bit is set to "1", the interrupt occurs if CTRT bit is set to "1".
The Conditions the DVST bit set are depend on the WDST, RDST, CMPL or SERR.
The complete of setup stage can not set enable/disable to set CTRT bit to "1".

(6) BEMPE (Buffer Empty/Size Over Error Interrupt Enable) Bit (b10)

This bit sets enable/disable of buffer empty/size over error interrupt.
When this bit is set to "1", the interrupt occurs if BEMP bit is set to "1".

(7) INTNE (Buffer Not Ready Interrupt Enable) Bit (b9)

This bit sets enable/disable of buffer not ready interrupt.
When this bit is set to "1", the interrupt occurs if INTN bit is set to "1".

(8) INTRE (Buffer Ready Interrupt Enable) Bit (b8)

This bit sets enable/disable of buffer ready interrupt.
When this bit is set to "1", the interrupt occurs if INTR bit is set to "1".

(9) URST (USB Reset Detect) Bit (b7)

This bit selects whether to set the DVST bit to "1" or not at the USB bus reset detection.
The register is initialized by the USB reset detection, irrespective of the value of this bit.

(10) SADR (SET_ADDRESS Execute) Bit (b6)

This bit selects whether to set the DVST bit to "1" or not at the SET_ADDRESS execution.
For details, refer to "DVST bit".

(11) SCFG (SET_CONFIGURATION Execute) Bit (b5)

This bit selects whether to set the DVST bit to "1" or not at the SET_ CONFIGURATION execution.
For details, refer to "DVST bit".

(12) SUSP (Suspend Detect) Bit (b4)

This bit selects whether to set the DVST bit to "1" or not at the suspend detection.

(13) WDST (Control Write Transfer Status Stage) Bit (b3)

This bit selects whether to set the CTRT bit to "1" or not when transited to status stage during control write transfer.

(14) RDST (Control Read Transfer Status Stage) Bit (b2)

This bit selects whether to set the CTRT bit to "1" or not when transited to status stage during control read transfer.

(15) CMPL (Control Transfer Complete) Bit (b1)

This bit selects whether to set the CTRT bit to "1" or not when the status stage completes during control transfer.

(16) SERR (Control Transfer Sequence Error) Bit (b0)

This bit selects whether to set the CTRT bit to "1" or not when the sequence error is detected at control transfer.

2.9 Interrupt Enable Register 1

■ Interrupt Enable Register 1 (INT_ENABLE1) <Address : H'12>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
									EPB_RE						
0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		0	0
6~0	EPB_RE Buffer Ready Interrupt Enable	0 : Disable INTR bit set 1 : Enable INTR bit set b6 corresponds to EP6, ---b1 corresponds to EP1 and b0 corresponds to EP0.	○	○

(1) EPB_RE (Buffer Ready Interrupt Enable) Bits (b6~b0)

These bits select whether to set the INTR bit to "1" or not when the EPB_RDY bit is set to "1". Also refer to "3.1 Interrupt Function".

2.10 Interrupt Enable Register 2

■ Interrupt Enable Register 2 (INT_ENABLE2) <Address : H'14>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
									EPB_NRE						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		0	0
6~0	EPB_NRE Buffer Not Ready Interrupt Enable	0 : Disable INTN bit set 1 : Enable INTN bit set b6 corresponds to EP6, ---b1 corresponds to EP1 and b0 corresponds to EP0.	○	○

(1) EPB_NRE (Buffer Not Ready Interrupt Enable) Bits (b6~b0)

These bits select whether to set the INTN bit to "1" or not when the EPB_NRDY bit is set to "1". Also refer to "3.1 Interrupt Function".

Note : Do not set the corresponding bit of this register to "1" when the endpoint is set to isochronous transfer (set by EPi _TYP bits).

2.11 Interrupt Enable Register 3

■ Interrupt Enable Register 3 (INT_ENABLE3) <Address : H'16>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
									EPB_EMPE						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		0	0
6~0	EPB_EMPE Buffer Empty/Size Over Error Interrupt Enable	0 : Disable BEMP bit set 1 : Enable BEMP bit set b6 corresponds to EP6, ---b1 corresponds to EP1 and b0 corresponds to EP0.	○	○

(1) EPB_EMPE (Buffer Empty/Size Over Error Interrupt Enable) Bits (b6~b0)

These bits select whether to set the BEMP bit to "1" or not when the EPB_EMP_OVR bit is set to "1". Also refer to "3.1 Interrupt Function".

2.12 Interrupt Status Register 0

■ Interrupt Status Register 0 (INT_STATUS0) <Address : H'18>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
VBUS	RESM	SOFR	DVST	CTRT	BEMP	INTN	INTR	Vbus	DVSQ			VALID	CTSQ		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	1	-	-	-	-	0	0	0	1	-	-	-	-

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : B'---1----0001---->

b	Bit name	Function	R	W
15	VBUS Vbus Interrupt	■ Read 0 : No occurrence of interrupt 1 : Occurrence of interrupt ■ Write 0 : Clear Interrupt 1 : Invalid (Ignored when written)	○	○
14	RESM Resume Interrupt	■ Read 0 : No occurrence of interrupt 1 : Occurrence of interrupt ■ Write 0 : Clear Interrupt 1 : Invalid (Ignored when written)	○	○
13	SOFR SOF Detect Interrupt	■ Read 0 : No occurrence of interrupt 1 : Occurrence of interrupt ■ Write 0 : Clear Interrupt 1 : Invalid (Ignored when written)	○	○
12	DVST Device State Transition Interrupt	■ Read 0 : No occurrence of interrupt 1 : Occurrence of interrupt ■ Write 0 : Clear Interrupt 1 : Invalid (Ignored when written)	○	○
11	CTRT Control Transfer Stage Transition Interrupt	■ Read 0 : No occurrence of interrupt 1 : Occurrence of interrupt ■ Write 0 : Clear Interrupt 1 : Invalid (Ignored when written)	○	○
10	BEMP Buffer Empty/Size Over Error Interrupt	■ Read 0 : No occurrence of interrupt 1 : Occurrence of interrupt ■ Write Invalid (Ignored when written)	○	×
9	INTN Buffer Not Ready Interrupt	■ Read 0 : No occurrence of interrupt 1 : Occurrence of interrupt ■ Write Invalid (Ignored when written)	○	×
8	INTR Buffer Ready Interrupt	■ Read 0 : No occurrence of interrupt 1 : Occurrence of interrupt ■ Write Invalid (Ignored when written)	○	×

b	Bit name	Function	R	W
7	Vbus Vbus Level	■ Read 0 : "L" 1 : "H" ■ Write Invalid (Ignored when written)	○	×
6~4	DVSQ Device State	■ Read 000 : Powered state 001 : Default state 010 : Address state 011 : Configured state 1xx : Suspended state (Note) ■ Write Invalid (Ignored when written)	○	×
3	VALID Setup Packet Detect	■ Read 0 : No detection 1 : Receiving the setup packet ■ Write 0 : This VALID bit clear 1 : Invalid (Ignored when written)	○	○
2~0	CTSQ Control Transfer Stage	■ Read 000 : Idle or setup stage 001 : Control read transfer data stage 010 : Control read transfer status stage 011 : Control write transfer data stage 100 : Control write transfer status stage 101 : Control write no data transfer status stage 110 : Control transfer sequence error 111 : Reserved ■ Write Invalid (Ignored when written)	○	×

Note : x is a optional value.

The b15 to b8 of this register are interrupt status bits. When the bit of the Interrupt Enable Register corresponding to these bits are set to “1” (interrupt enable), the interrupt occurs by setting these bits to “1”.

(1) VBUS (Vbus Interrupt) Bit (b15)

This bit indicates the change of Vbus input.
This bit is set to “1” (Vbus interrupt occurs) when the Vbus input changes (“L”->“H” or “H”->“L”).
This bit is cleared to “0” by writing “0” (interrupt is cleared).
This bit is set to “1” and can be read out even if the clock is not supplied (Note). This bit can also be cleared by writing “0”. In case the clock is not supplied, make sure to write “1” after writing “0” (no further interrupt will be accepted).

Note : SCKE bit = “0” when XCKE bit = “1 ”, or XCKE bit = “0”.

(2) RESM (Resume Interrupt) Bit (b14)

This bit indicates the change of USB bus state.
This bit is set to “1” when the USB bus state is changed from suspended (DVST bits = “1xx”) to “J”->“K” or “J”->“SE0” (resume interrupt occurs).
This bit is cleared to “0” by writing “0” (interrupt is cleared).
This bit is set to “1” and can be read out even if the clock is not supplied (Note). This bit can also be cleared by writing “0”. In case the clock is not supplied, make sure to write “1” after writing “0” (no further interrupt will be accepted).

Note : At SCKE bit = “0” when XCKE bit = “1 ” or XCKE bit = “0”.

(3) SOFR (SOF Detect Interrupt) Bit (b13)

This bit indicates that the SOF packet is received and the frame number is updated.
This bit is set to “1” when the SOF packet is received and the frame number is stored at the timing set by the FMOD bit of the Isochronous Status Register (SOF detect interrupt occurs).
This bit is cleared to “0” by writing “0” (interrupt is cleared).

(4) DVST (Device State Transition Interrupt) Bit (b12)

This bit indicates the transition of the device state.
This bit is set to “1” when the transition of device states takes place as follows (device state transition interrupt occurs):

(A) USB bus reset detect (Arbitrary state -> Default state):
When the SE0 state continues for 2.5 us or more in D+ and D- pins, the USB bus reset is detected, causing this bit to be set to “1”.

(B) “SET_ADDRESS” execute (Default state -> Address state):
This bit is set to “1” when the SET_ADDRESS request is detected as (a) and the response is made by zero-length packet in status stage.

(a) “SET_ADDRESS” request in case device address value in default state is not “0”:
In case the wValue in default state is “0”, this bit is not set to “1”. When this request is received, the device address value is set to the USB_Address Register, irrespective of the setting of this bit.

(C) “SET CONFIGURATION” execute (Address state -> Configured state):
This bit is set to “1” when the requests below are detected and ACK is received after the response is made through zero-length packet in status stage.
(a) “SET_CONFIGURATION” request in case configuration value in address state is not “0”
(b) “SET_CONFIGURATION” request in case configuration value in configured state is “0”

(D) Suspend detect (Powered/Default/Address/Configured state -> Suspended state):
The suspended state is detected and this bit is set to“1” when the idle state continues for 3 ms or more in D+ and D- pins.

The Conditions that this bit indicates "1" depend on the URST, SADR, SCFG or SUSP bits.
This bit is cleared to “0” by writing “0” (interrupt is cleared).
The present device state can be confirmed by the DVSQ bits.

(5) CTRT (Control Transfer Stage Transition Interrupt) Bit (b11)

This bit indicates the transition of stage in control transfers.
This bit is set to “1” when the stage transition of control transfer takes place as follows (control transfer stage transition interrupt occurs):
Refer to Figure 2.7.

- Setup Stage Complete (When transmitting ACK)
- Control Write Transfer Status Stage Transition (When receiving IN token)
- Control Read Transfer Status Stage Transition (When receiving OUT token)
- Control Transfer Complete (When transmitting or receiving ACK)
- Control Transfer Sequence Error (When error occurs)

The Conditions that this bit indicates "1" depend on the WDST, RDST, CMPL or SERR bits.
This bit is cleared to “0” by writing “0” (interrupt is cleared).
The present stage can be confirmed by the CTSQ bits.

(6) BEMP (Buffer Empty/Size Over Error Interrupt) Bit (b10)

This bit indicates the occurrence of “buffer empty” or “buffer size over error”.
This bit is set to “1” when the EPB_EMP_OVR bit is set to “1” (buffer empty/buffer size over error interrupt occurs).
This bit is cleared by setting all the bits of Interrupt Status Register 3 to “0”.
For details, refer to “Interrupt Status Register 3”.

(7) INTN (Buffer Not Ready Interrupt) Bit (b9)

This bit indicates the NAK has been sent to the host because of the “buffer not ready” state.
This bit is set to “1” when the EPB_NRDY bit is set to “1” (buffer not ready interrupt occurs).
This bit is cleared by setting all the bits of Interrupt Status Register 2 to “0”.
For details, refer to “Interrupt Status Register 2”.

(8) INTR (Buffer Ready Interrupt) Bit (b8)

This bit indicates the “buffer ready” state (that can be read/written).
This bit is set to “1” when the EPB_RDY bit is set to “1” (buffer ready interrupt occurs).
This bit is cleared by setting all the bits of Interrupt Status Register 1 to “0”.
For details, refer to “Interrupt Status Register 1”.

(9) Vbus (Vbus Level) Bit (b7)

This bit indicates the state of Vbus pin.
When this bit changes, the VBUS bit is set to “1”.
This bit is capable of reading the correct value even if the clock is not supplied (Note).

Note : SCKE bit = “0” when XCKE bit = “1 ”, or XCKE bit = “0”.

(10) DVSQ (Device State) Bits (b6~b4)

These bits indicate the present device states as follows:

000 :	Powered State	Power ON state
001 :	Default State	USB bus reset detected state
010 :	Address State	SET_ADDRESS request executed state
011 :	Configured State	SET_CONFIGURATION request executed state
1xx :	Suspended State	“suspended” detected state

Depending on the changes of these device states, the DVST bit and the RESM bit are set to “1” (set enable/disable by the URST, SADR, SCFG or SUSP bits). For details, refer to “DVST bit” and Figure 2.6.

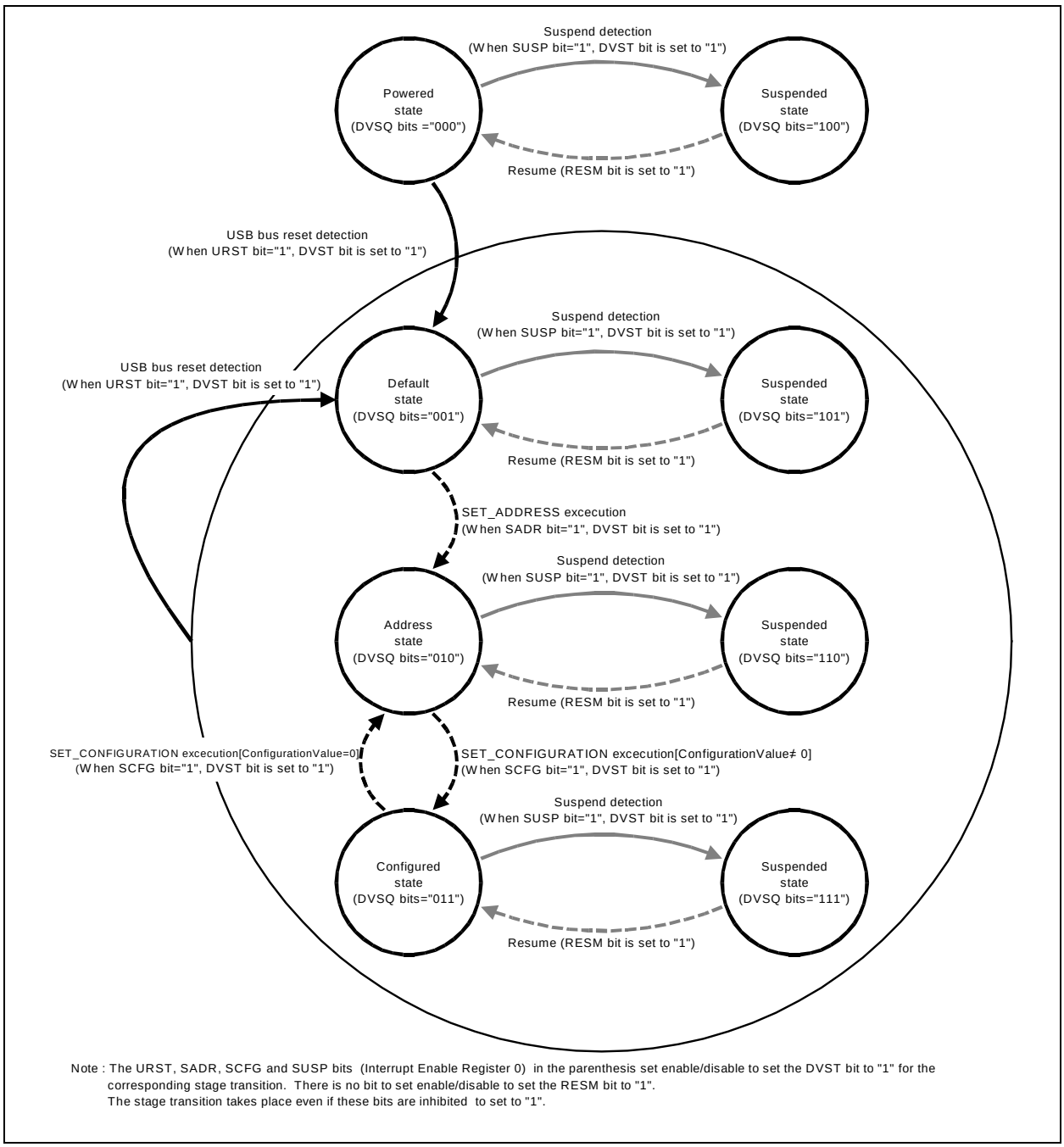


Figure 2.6 Device State Transition

(11) VALID (Setup Packet Detect) Bit (b3)

This bit indicates that the setup token has been received.
When the setup token is completely received, this bit is set to “1”.
When this bit is set to “1”, the writing to EP0_PID/CCPL bits of EP0_FIFO Control Register is ignored.
At the time of receiving the setup token, the interrupt has not occurred (the interrupt occurs only after the termination of setup stage).
This bit is cleared to “0” by writing “0”.

(12) CTSQ (Control Transfer Stage) Bits (b2~b0)

These bits indicate the present stage in the control transfer. Refer to Figure 2.7.

000 : Idle or Setup Stage
001 : Control Read Transfer Data Stage
010 : Control Read Transfer Status Stage
011 : Control Write Transfer Data Stage
100 : Control Write Transfer Status Stage
101 : Control Write No Data Transfer Status Stage
110 : Control Transfer Sequence Error (refer to below)
111 : Reserved

The control transfer sequence error is described below. When this error occurs, the EP0_PID bits are set to "1x" (stall state).

<At control read transfer>
- OUT token is received when data is never transferred against the IN token of the data stage.
- IN token is received at status stage.
- Data packet other than the zero-length packet is received at status stage.

<At control write transfer>
- IN token is received when ACK response is never made against the OUT token of the data stage.
- OUT token is received in status stage.

<At control write no data transfer>
- OUT token is received in status stage.

<Others>
- Data exceeding in size set by the EP0 Packet Size Register is received (the EPB_EMP_OVR bit of the Interrupt Status Register 3 is set to "1").

In case the amount of received data exceeds the wLength value in the request at the data stage of the control write transfer, it is not recognized as the control transfer sequence error.

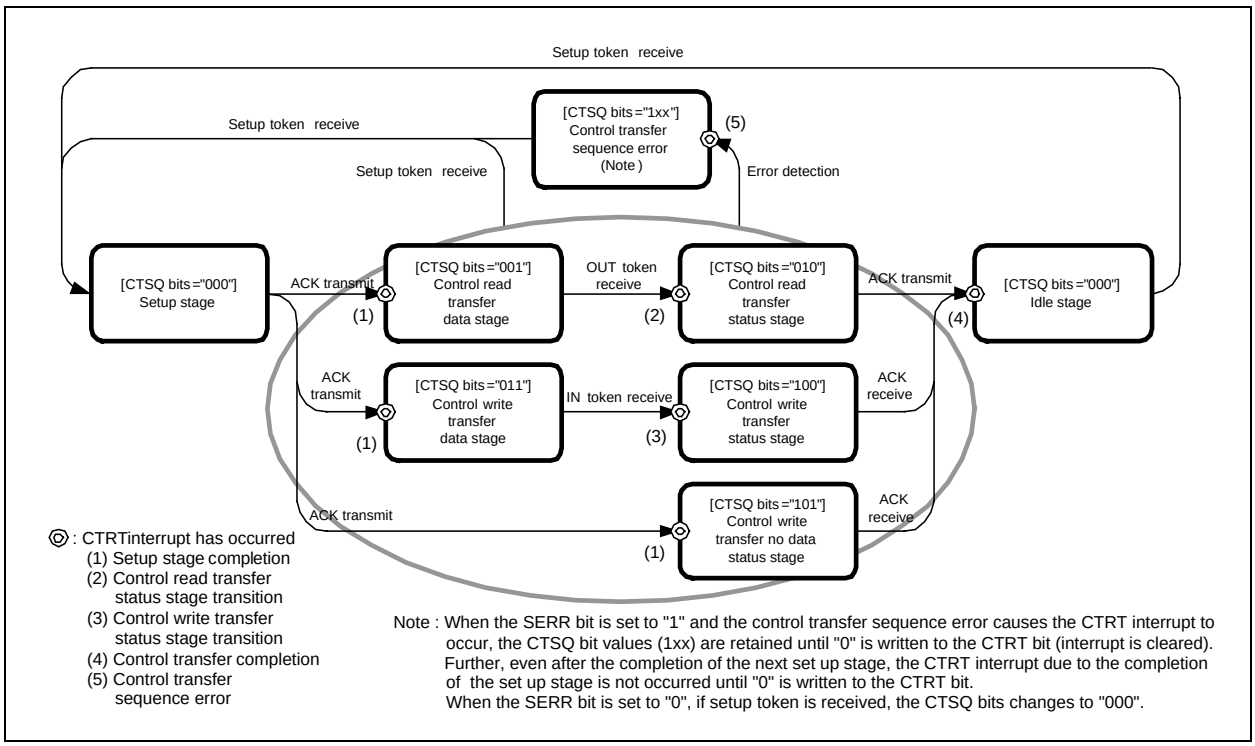


Figure 2.7 Control Transfer Transition

2.13 Interrupt Status Register 1

■ Interrupt Status Register 1 (INT_STATUS1) <Address : H'1A>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
									EPB_RDY						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset :H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		0	0
6~0	EPB_RDY Buffer Ready Interrupt	■ Read 0 : No occurrence of interrupt 1 : Occurrence of interrupt ■ Write <When RDYM bit is set to "0"> Invalid (Ignored when written) <When RDYM bit is set to "1"> 0 : Clear interrupt clear 1 : Invalid (Ignored when written) b6 corresponds to EP6, ---b1 corresponds to EP1 and b0 corresponds to EP0.	○	○

(1) EPB_RDY (Buffer Ready Interrupt) Bits (b6~b0)

The bit corresponding to each endpoint is set to "1" with the buffer at "ready" state.
The ready state refers to the state when CPU or DMAC can read or write the CPU side buffer. When the EPB_RE bit is set to "1", if this bit is set to "1", the INTR bit is set to "1", causing the buffer ready interrupt to occur.
Setting "1"/clearing to "0" to this bit differs according to the endpoint and transfer direction as shown below:

Note : Refer to "3.2 FIFO Buffer" for CPU/SIE side.

- Endpoint 0
  - ○ When set to control write transfer (ISEL bit = "0")
    The condition for this bit to be set to "1" is as follows:
    - When the IVAL bit of the EP0_FIFO Control Register changes from "0" to "1"

    The condition for this bit to be cleared to "0" differs according to the RDYM bit:
    - RDYM bit = "0" : When the IVAL bit of the EP0_FIFO Control Register changes from "1" to"0"
    - RDYM bit = "1" : Writes "0" to this bit

  - ○ When set to control read transfer (ISEL bit = "1")
    This bit is not set to "1" (Refer to "EPB_EMP_OVR bit").

- Endpoint 1~6
  - ○ When set to OUT buffer (EPi_DIR bit = "0")

    The condition for this bit to be set to "1" is as follows:

    <The endpoint not specified by DMA_EP bits>

    <The endpoint specified by DMA_EP bits with INTM bit set to "1">
    - When the IVAL bit of the endpoint changes from "0" to "1"

    <The endpoint specified in DMA_EP bits with INTM bit set to "0">
    - When the buffer data including the received short packet (including the zero-length packet) are all read out

    The condition for this bit to be cleared to "0" differs according to the RDYM bit (Note):
    - RDYM bit = "0" : When the IVAL bit of the endpoint changes from "1" to "0"
    - RDYM bit = "1" : Writes "0" to this bit

    Note : When the INTM bit at the endpoint specified by the DMA_EP bit is set to "0", the IVAL bit is retained to "1". Thus, it is necessary to write "1" to the BCLR bit and to clear the IVAL bit to "0" when RDYM bit is set to "0". Even when the RDYM bit is set to "1", this bit can be cleared by writing "0". It is necessary to write "1" to the BCLR bit and to clear the IVAL bit.

  - ○ When set to IN buffer (EPi_DIR bit = "1")

    The condition for this bit to be set to "1" is as follows:

    <The endpoint not specified by DMA_EP bits>

    <The endpoint specified by DMA_EP bits with INTM bit set to "1">
    - When the IVAL bit of the endpoint changes from "1" to "0"
    - Or when EPi_DER bit is changed from "0" to "1"

    <The endpoint specified by DMA_EP bits with INTM bit set to "0">

    This bit is not be set to "1".

    The condition for this bit to be cleared to "0" differs according to the RDYM bits:
    - RDYM bit = "0" : When the IVAL bit of the endpoint changes from "0" to "1"
    - RDYM bit = "1" : Writes "0" to this bit

Note : The IVAL bit is located per endpoint. For details, refer to "3.2.4 IVAL Bit and EPB_RDY Bit".

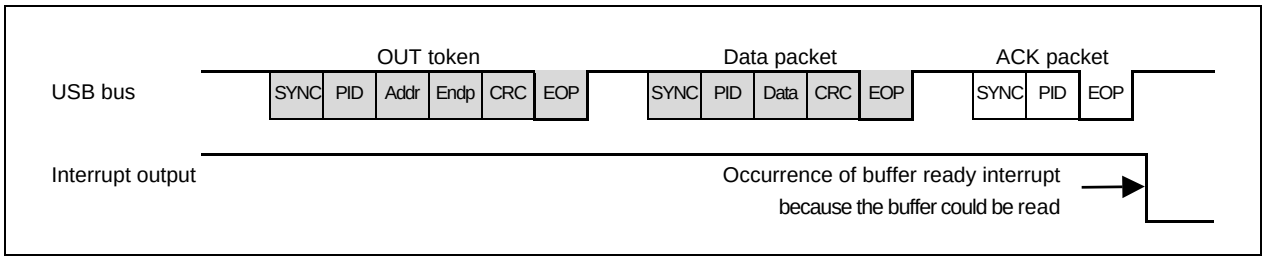


Figure 2.8 Examples of Buffer Ready Interrupt Occurrence Timing (OUT transfer)

2.14 Interrupt Status Register 2

■ Interrupt Status Register 2 (INT_STATUS2) <Address : H'1C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
									EPB_NRDY						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		0	0
6~0	EPB_NRDY Buffer Not Ready Interrupt	■ Read 0 : No occurrence of interrupt 1 : Occurrence of interrupt ■ Write 0 : Clear interrupt 1 : Invalid (Ignored when written) b6 corresponds to EP6, ---b1 corresponds to EP1 and b0 corresponds to EP0.	○	○

(1) EPB_NRDY (Buffer Not Ready Interrupt) Bits (b6~b0)

The bit corresponding to each endpoint is set to "1" when IN token/OUT token is received with the buffer at "not ready" state.
The "not ready" state refers to the state when EP0_PID bits and EPi_PID bits are set to BUF/STALL response and means that the buffer could not be received and transmitted.
When this bit is set to "1", if the EP0_PID and EPi_PID bits are set to BUF, NAK response is executed, and if they are set to STALL, STALL response is executed.
When the EPB_NRE bit is set to "1", if this bit is set to "1", the INTN bit is set to "1", causing the buffer not ready interrupt to occur.
This bit is cleared by writing "0".

Note: In case the endpoint is set to isochronous transfer (set by EPi_TYP bits), the corresponding bit of this register may be set to "1". Hence, do not set the corresponding bit of the Interrupt Enable Register 2 to "1".

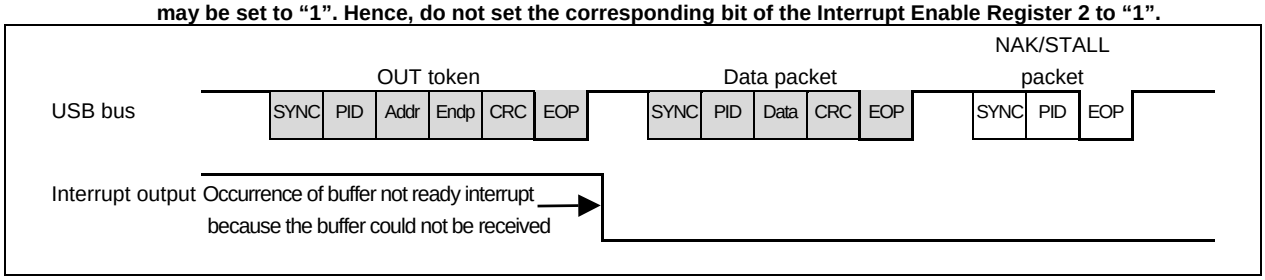


Figure 2.9 Examples of Buffer Not Ready Interrupt Occurrence Timing (OUT transfer)

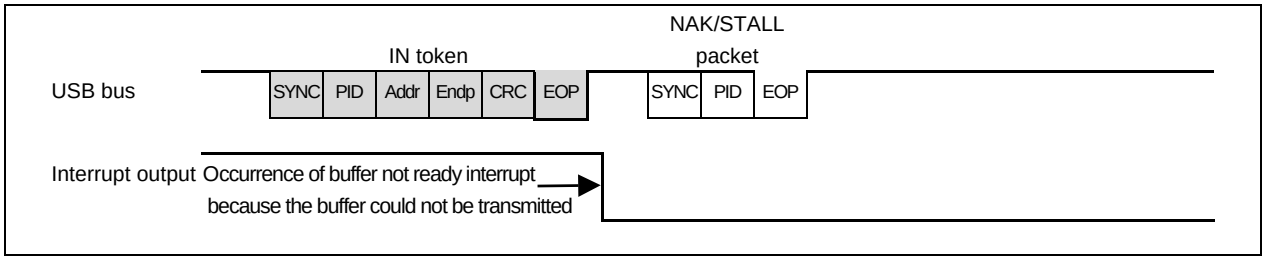


Figure 2.10 Examples of Buffer Not Ready Interrupt Occurrence Timing (IN transfer)

2.15 Interrupt Status Register 3

■ Interrupt Status Register 3 (INT_STATUS3) <Address : H'1E>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
									EPB_EMP_OVR						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		0	0
6~0	EPB_EMP_OVR Buffer Empty/Size Over Interrupt	■ Read 0 : No occurrence of interrupt 1 : Occurrence of interrupt ■ Write 0 : Clear interrupt 1 : Invalid (Ignored when written) b6 corresponds to EP6, ---b1 corresponds to EP1 and b0 corresponds to EP0.	○	○

(1) EPB_EMP_OVR (Buffer Empty/Size Over Interrupt) Bits (b6~b0)

These bits indicate that the received data size exceeds the maximum packet size or that the buffers of the endpoints 0 to 6 are empty.

- Endpoint 0
  - ○When set to control write transfer (ISEL bit = "0")
    The condition for this bit to be set to "1" is as follows:
    - Receives packet data with size exceeding the one set by the EP0 Packet Size Register (Size-over detection).

    In this case, the EP0_PID bits are set to STALL response.
    Further the CTRT bit sets to "1" if the SERR bit is set to "1".
    This bit is set to "1" when size-over is detected, irrespective of the EP0_PID bit setting.

  - ○When set to control read transfer (ISEL bit = "1")
    The condition for this bit to be set to "1" is as follows:
    - When the IVAL bit of the EP0_FIFO Control Register changes from "1" to "0".
    - When transmit data exist in the buffer for EP0_FIFO and "1" is written to the BCLR bit.
- Endpoint 1~6
  - ○When set to OUT buffer (EPi_DIR bit = "0")
    The condition for this bit to be set to "1" is as follows:
    - Receives packet data with size exceeding the one set by the EPi_MXPS bits (Size-over detection).

    The EPi_PID bits are set to STALL response.
    This bit isn't set to "1" at isochronous transfer.
    This bit is set to "1" when size-over is detected, irrespective of the EP0_PID bit setting.

  - ○When set to IN buffer (EPi_DIR bit = "1")
    The condition for this bit to be set to "1" is as follows:
    - When the data of SIE side buffer are all transmitted with the data not written to the CPU side buffer (Buffer empty).

The conditions for this bit to be cleared to "0" in all bits are as follows:
- Writes "0" to this bit.

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.

2.16 Request Register

■ Request Register (REQUEST_TYPE) <Address : H'20>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
bRequest								bmRequestType							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15~8	bRequest Request	■ Read Request received in the setup stage ■ Write Invalid (Ignored when written)	○	×
7~0	bmRequestType Request Type	■ Read Request type received in the setup stage ■ Write Invalid (Ignored when written)	○	×

(1) bRequest (Request) Bits (b15~b8)

These bits store the bRequest of the device request received in the setup stage of the control transfer.

(2) bmRequestType (Request Type) Bits (b7~b0)

These bits store the bmRequestType of the device request received in the setup stage of the control transfer.

2.17 Value Register

■ Value Register (REQUEST_VALUE) <Address : H'22>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
wValue															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15~0	wValue Value	■ Read Parameter of device request received in the setup stage ■ Write Invalid (Ignored when written)	○	×

(1) wValue (Value) Bits (b15~b0)

These bits store the wValue of the device request received at the setup stage of the control transfer.

2.18 Index Register

■ Index Register (REQUEST_INDEX) <Address : H'24>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
wIndex															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15~0	wIndex Index	■ Read Parameter of device request received in the setup stage ■ Write Invalid (Ignored when written)	○	×

(1) wIndex (Index) Bits (b15~b0)

These bits store wIndex of the device request received in the setup stage of the control transfer.

2.19 Length Register

■ Length Register (REQUEST_LENGTH) <Address : H'26>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
wlength															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15~0	wlength Length	■ Read Parameter of device request received in the setup stage ■ Write Invalid (Ignored when written)	○	×

(1) wlength (Length) Bits (b15~b0)

These bits store the wlength of the device request received at the setup stage of the control transfer.

2.20 Control Transfer Control Register

■ Control Transfer Control Register (CONTROL_TRANSFER) <Address : H'28>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
CTRR		Ctr_Rd_Buf_Nmb						CTRW		Ctr_Wr_Buf_Nmb					
0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -

<H/W reset : H'0000>
<S/W reset :->
<USB bus reset : ->

b	Bit name	Function	R	W
15	CTRR Control Read Transfer Continuous Transmit Mode	0 : Single transmit mode 1 : Continuous transmit mode	○	○
14	Reserved. Set it to "0".		0	0
13~8	Ctr_Rd_Buf_Nmb Control Read Buffer Start Number	The top block number for the Control Read buffer	○	○
7	CTRW Control Write Transfer Continuous Receive Mode	0 : Unit receive mode 1 : Continuous receive mode	○	○
6	Reserved. Set it to "0".		0	0
5~0	Ctr_Wr_Buf_Nmb Control Write Buffer Start Number	The top block number for the Control Write buffer	○	○

(1) CTRR (Control Read Transfer Continuous Transmit Mode) Bit (b15)

This bit sets the transmit mode at data stage of the control read transfer.
In case of single transmit mode, the transmit completes after transmitting one packet under the condition as follows:

- Transmits the data equivalent to the size set by the EP0 Packet Size Register or transmits a short packet by setting the IVAL bit to "1".

In case of continuous transmit mode, the transmit completes after transmitting several packets under the condition as follows:

- Transmits the data equivalent to the size set by the EP0_FIFO Continuous Transmit Data Length Register or transmits a short packet by setting the IVAL bit to "1".

In case of single transmit mode, the writing completes under the conditions as follows:

- Writes the data equivalent to the size set by the EP0 Packet Size Register to the buffer (The IVAL bit of the EP0_FIFO Control Register changed to "1").
- Writes "1" to the IVAL bit of the EP0_FIFO Control Register.

In case of continuous transmit mode, the writing completes under the conditions as follows:

- Writes the data equivalent to the size set by the EP0_FIFO Continuous Transmit Data Length Register (The IVAL bit of the EP0_FIFO Control Register changed to "1").
- Writes "1" to the IVAL bit of the EP0_FIFO Control Register.

The setting conditions of the IVAL bit of the EP0_FIFO Control Register change due to this bit.

(2) Ctr_Rd_Buf_Nmb (Control Read Buffer Start Number) Bits (b13~b8)

These bits set the beginning block number of the buffer to be used in control read transfer. The block number is a number by dividing the FIFO buffer into 64 byte sections (Note 1).
When the mode is set to single transmit (CTRR bit = "0"), the blocks set by these bits only are used and, from the following block, it is possible to set to the buffer of a different endpoint.
When the mode is set to continuous transmit (CTRR bit = "1"), the buffer equivalent to the size set by the EP0_FIFO Continuous Transmit Data Length Register (max. 256 bytes) is used from the block numbers set by these bits (Note 2).

Note 1: The M66291 is equipped with 3 Kbytes FIFO buffer and has blocks from H'0 to H'2F.
Note 2: Make sure that several endpoints do not get overlapped in the same buffer area.

(3) CTRW (Control Write Transfer Continuous Receive Mode) Bit (b7)

This bit sets the receive mode at data stage of the control write transfer.
In case of unit receive mode, the receive completes after receiving one packet under the condition as follows:

- Receives the data equivalent to the size set by the EP0 Packet Size Register.
- Receives a short packet.

In case of continuous receive mode, the receipt completes after receiving several packets under the condition as follows:

- Receives automatically the data equivalent to the size set by the EP0 Packet Size Register several times and receives the data equivalent to 256 bytes.
- Receives the short packet.

The setting conditions of the IVAL bit of the EP0_FIFO Control Register change due to this bit.

(4) Ctr_Wr_Buf_Nmb (Control Write Buffer Start Number) Bits (b5~b0)

These bits set the beginning? block number of the buffer to be used in control write transfer. The block number is a number for control by dividing the FIFO buffer into 64 byte sections (Note 1).
When the mode is set to unit receive (CTRW bit = "0"), the blocks set by these bits only are used and, from the following block, it is possible to set to the buffer of a different endpoint.
When the mode is set to continuous receive (CTRW bit = "1"), the buffer equivalent to 256 bytes is used from the block numbers set by these bits (Note 2).

Note 1: The M66291 is equipped with 3 Kbytes FIFO buffer and has blocks from H'0 to H'2F.
Note 2: Make sure that several endpoints do not get overlapped in the same buffer area.

2.21 EP0 Packet Size Register

■ EP0 Packet Size Register (EP0_PACKET_SIZE) <Address : H'2A>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
									EP0_MXPS						
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0008>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		0	0
6~0	EP0_MXPS Maximum Packet Size	Upper limit of the transmit/receive data for one packet transfer (Settable only 8,16,32 and 64)	○	○

(1) EP0_MXPS (Maximum Packet Size) Bits (b6~b0)

These bits set the upper limit (byte count) of the transmit/receive data for one packet transfer at data stage. Set the value of bMaxPacketSize0 transmitted to the host.
At the time of transmitting, the data equivalent to the size set by these bits is read from the buffer for transmission. In case the buffer does not have the data equivalent to the size set by these bits, the data is transmitted as the short packet.
At the time of receiving, the data equivalent to the size set by these bits is written to the buffer. If the received packet data is larger than the size set by these bits, the following bits are set to "1":

- The EPB_EMP_OVR bit.
  (buffer empty/Size over error interrupt occurs when the EPB_EMPE bit is set to "1".)
- The CTRT bit when the SERR bit is set to "1".
  (control transfer stage transition interrupt occurs.)

Note: Set these bits after setting the response PID to NAK (EP0_PID bits = "00").

2.22 Automatic Response Control Register

■ Automatic Response Control Register (AUTO_RESPONSE_CONTROL) <Address : H'2C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	ASCN 0 - -	ASAD 0 - -

<H/W reset : H'0000>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15~2	Reserved. Set it to "0".		0	0
1	ASCN SET_CONFIGURATION Automatic Response Mode	0 : Invalid of automatic response mode for SET_CONFIGURATION 1 : Valid of automatic response mode for SET_CONFIGURATION	○	○
0	ASAD SET_ADDRESS Automatic Response Mode	0 : Invalid of automatic response mode for SET_ADDRESS 1 : Valid of automatic response mode for SET_ADDRESS	○	○

(1) ASCN (SET_CONFIGURATION Automatic Response Mode) Bit (b1)

This bit sets the valid/invalid of automatic response mode for SET_CONFIGURATION request.
With the automatic response mode set to valid, zero-length packet is automatically transmitted against the requests below at the status stage before notifying the normal completion. Here, the CTRT bit is not set to "1" (control transfer stage transition interrupt does not occur).

- SET_CONFIGURATION request of Configuration Value ≠ 0 in Address state
- SET_CONFIGURATION request of Configuration Value = 0 in Configured state

No automatic response is executed when the SET_CONFIGURATION request other than the ones given above is received. In such case, the CTRT bit is set to "1" (control transfer stage transition interrupt occurs).
When the state gets changed after receiving the aforesaid requests, the DVST bit is set to "1" if the SCFG bit is set to "1", irrespective of the validity of this function (device state transition interrupt occurs).

(2) ASAD (SET_ADDRESS Automatic Response Mode) Bit (b0)

This bit sets the valid/invalid of automatic response mode for SET_ADDRESS request.
With the automatic response mode set to valid, zero-length packet is automatically transmitted against the requests below at the status stage before notifying the normal completion. Here, the CTRT bit is not set to "1" (control transfer stage transition interrupt does not occur).

- SET_ADDRESS request at Default state

No automatic response is executed when the SET_ADDRESS request other than the ones given above is received. In such case, the CTRT bit is set to "1" (control transfer stage transition interrupt occurs).
When the state gets changed after receiving the aforesaid requests, the DVST bit is set to "1" if the SADR bit is set to "1", irrespective of the validity of this function (device state transition interrupt occurs).

2.23 EP0_FIFO Select Register

■ EP0_FIFO Select Register (EP0_FIFO_SELECT) <Address : H'30>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
RCNT					Octl			BSWP							ISEL
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0000>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15	RCNT Read Count Mode	0: The ODLN bits are cleared by reading all receive data 1: The ODLN bits are counted down by reading receive data	○	○
14~11	Reserved. Set it to "0".		0	0
10	Octl Register 8-Bit Mode	0 : EP0_FIFO Data Register is 16-bit mode 1 : EP0_FIFO Data Register is 8-bit mode	○	○
9~8	Reserved. Set it to "0".		0	0
7	BSWP Byte Swap Mode	0 : Byte is treated as little ENDIAN 1 : Byte is treated as big ENDIAN	○	○
6~1	Reserved. Set it to "0".		0	0
0	ISEL Buffer Select	0 : Control write transfer 1 : Control read transfer	○	○

(1) RCNT (Read Count Mode) Bit (b15)

This bit sets the countdown methods of the ODLN bits at the time of reading the EP0_FIFO Data Register.
When this bit is set to "0", the ODLN bit value does not change in spite of reading the data from the EP0_FIFO Data Register, and is cleared to H'0 when all data is read out.
When this bit is set to "1", the ODLN bit values are counted down every time the data is read from the EP0_FIFO Data Register. Here, the down-count value differs as shown below depending on whether the EP0_FIFO Data Register is set to 8-bit mode or 16-bit mode:

- 8-bit mode : Down-count per "-1"
- 16-bit mode : Down-count per "-2"

Note : Use the *HWR/*BYTE pin or the Octl bit of this register for setting the 8-bit/16-bit mode.

(2) Octl (Register 8-Bit Mode) Bit (b10)

This bit sets the access mode of the EP0_FIFO Data Register.
When this bit is set to "0", the EP0_FIFO Data Register is set to 16-bit mode, and all bits of the EP0_FIFO Data Register are valid.
When this bit is set to "1", the EP0_FIFO Data Register is set to 8-bit mode, and the upper-order 8 bits of the EP0_FIFO Data Register (b15 to b8) are invalid.
Set this bit before receiving the data.
When set to control write transfer (ISEL bit = "0"), change this bit before receiving the data. When set to control read transfer (ISEL bit = "1"), if the E0req bit indicates "1", do not change this bit.
This bit becomes invalid (fixed to 8-bit mode) when the mode is set to 8-bit by *HWR/*BYTE pin.
In such case, this bit is read "0".

(3) BSWP (Byte Swap Mode) Bit (b7)

This bit sets the endian of the EP0_FIFO Data Register.
When this bit is set to "0", the EP0_FIFO Data Register gets such as little endian.
When this bit is set to "1", the EP0_FIFO Data Register gets such as big endian.

	b15~b8	b7~b0
Little Endian	odd number address	even number address
Big Endian	even number address	odd number address

Note: Don't set this bit to "1" when the mode is set to 8-bit (set by the Octl bit or *HWR/*BYTE pin).

(4) ISEL (Buffer Select) Bit (b0)

This bit selects the buffer transfer direction of the endpoint 0 used in the control transfer.
When "0" is written to this bit, the buffer for control write transfer is valid.
When "1" is written to this bit, the buffer for control read transfer is valid.

2.24 EP0_FIFO Control Register

■ EP0_FIFO Control Register (EP0_FIFO_CONTROL) <Address : H'32>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
EP0_PID		IVAL	BCLR	E0req	CCPL		ODLN								
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0800>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15~14	EP0_PID Response PID	00 : NAK 01 : BUF (Transmits response PID/data according to the state of buffer etc,) 1x : STALL	○	○
13	IVAL IN Buffer Set/OUT Buffer Status	<When set to control write transfer> ■ Read 0: Disables the reading of data from the buffer 1: Enables the reading of data from the buffer ■ Write Invalid (Ignored when written) <When set to control read transfer> ■ Read 0 : Incomplete to write the data to buffer 1 : Complete to write the data to buffer ■ Write 0 : Invalid (Ignored when written) 1 : Complete to write the data to buffer (Forced completion : Transmits the short packet)	○	○
12	BCLR Buffer Clear	<When set to control write transfer > ■ Write 0 : Invalid (Ignored when written) 1 : Buffer clear (When the IVAL bit is set to "1") <When set to control read transfer> ■ Write 0 : Invalid (Ignored when written) 1 : Buffer clear (**Note : When the IVAL bit is set to "1", make sure to set the EP0_PID bits to "00" before executing the aforesaid operations.**)	0	○
11	E0req EP0_FIFO Ready	0 : Enables to access EP0_FIFO Data Register etc, 1 : Disables to access EP0_FIFO Data Register etc,	○	×
10	CCPL Control Transfer Control	0 : NAK response at status stage 1 : Normal completion response at status stage (ACK response/zero-length packet transmit)	○	○
9	Reserved. Set it to "0".		0	0
8~0	ODLN Control Write Receive Data Length	Stores the receive data length in control write transfer	○	×

(1) EP0_PID (Response PID) Bits (b15~b14)

These bits set the PID for response to the host at data/status stage of the control transfer.
At setup stage, the ACK response is executed irrespective of these bits.
Writing these bits are ignored when the VALID bit is equal to“1”.

When these bits are set to “00”
- Data stage : NAK response
- Status stage : NAK response

When these bits are set to “01”
<When set to control write transfer (ISEL bit = “0”)>
- Data stage : ACK response after receiving the data if the SIE side buffer can be ready to receive
  : NAK response if the SIE side buffer is not ready to receive
  In case the SIE side buffer is not ready to receive, the EPB_NRD bit is set to “1” when OUT token is received.
- Status stage : Depends on CCPL bit

<When set to control read transfer (ISEL bit = “1”)>
- Data stage : Transmits the data if the SIE side buffer is not ready to transmit
  : NAK response if the SIE side buffer is not ready to transmit
  In case the SIE side buffer is not ready to transmit, the EPB_NRD bit is set to “1” when IN token is received.
- Status stage : Depends on CCPL bit

When these bits are set to “1x”
- Data stage : STALL response
  In case the SIE side buffer is not ready to receive/transmit, the EPB_NRD bit is set to “1” when OUT token is received.
- Status stage : STALL response

The NAK response is not executed even if these bits are set to “00” when the data is being received at data stage. The settings of these bits are reflected from the next transaction.
Similarly, the transmission is not interrupted even if these bits are set to “00” when the data is being transmitted at data stage.
Further, these bits are automatically set to the values below when the following states occur:

- When setup token is received
  - "00" (NAK)
- When the request set to automatic response (SET_ADDRESS or SET_CONFIGURATION) is received
  - "01" (BUF)

  The CCPL bit also is automatically set to “1” and transmits the zero-length packet at the succeeding status stage (IN transaction).
- When sequence error occurs (CTSQ bits are set to “110”)
  - "1x" (STALL)

(2) IVAL (IN Buffer Set/OUT Buffer Status) Bit (b13)

This bit indicates valid value when the E0req bit of this register is set to "0".

●When set to control write transfer (ISEL bit = "0")
When this bit is set to "1", the buffer is at CPU side and can be read.

This bit is set to "1" at completion of receiving data.
The conditions of receive completion depend on the CTRW bit.
When this bit is set to "1", the EPB_RDY bit is set to "1" (buffer ready interrupt occurs).

This bit is cleared to "0" due to one of the reasons as follows:
- Reads out all the data received in the CPU side buffer.
- Writes "1" to the BCLR bit.

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.

●When set to control read transfer (ISEL bit = "1")
When this bit is set to "0", the buffer is at CPU side and can be written.

This bit is cleared to "0" due to one of the reasons as follows:
- Transmits completely SIE side buffer.
- Writes "1" to the BCLR bit.

The transmit completion is changed by the CTRR bit.
When this bit is set to "0" if the EPB_EMPE bit is set to "1", the EPB_EMP_OVR bit is set to "1" (buffer empty/size over error interrupt occurs).

This bit is set to "1" due to one of the reasons as follows:
- Completely writes the transmit data to CPU side buffer.
- Writes "1" to this bit.

  When "1" is written to this bit, the write is forcibly completed. When some written data exists in the buffer, that data is transmitted as the short packet. Here, if the buffer is empty or cleared, the zero-length packet is transmitted. The buffer can be cleared using the BCLR bit. Further, the zero-length packet can be transmitted by writing "1" simultaneously to this bit and to the BCLR bit. In this case the buffer is cleared by setting "1" to BCLR bit, and this bit is cleared to "0" after the zero-length packet is transmitted.

The write completion also is changed by the CTRR bit.

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.

(3) BCLR (Buffer Clear) Bit (b12)

This bit clears the data written to the CPU side buffer.

●When set to control write transfer (ISEL bit = "0")
When the IVAL bit is set to "1", the following operations are executed by writing "1" to this bit:
- Clears CPU side buffer.
- Clears the IVAL bit of this register.
- Clears the ODLN bits of this register.

●When set to control read transfer (ISEL bit = "1")
When the IVAL bit is set to "0", the following operations are executed by writing "1" to this bit:
- Clears CPU side buffer.

Further, the zero-length packet can be transmitted by writing "1" simultaneously to this bit and to the IVAL bit. For details, refer to "IVAL bit".

When the IVAL bit is set to "1", the following operations are executed by writing "1" to this bit:
- Clears SIE side buffer (Unlike the other endpoints, the SIE side buffer can also be cleared by this bit).
- Clears the IVAL bit of this register.

Note: When the IVAL bit is set to "1", make sure to set the EP0_PID bits to "00" before executing the aforesaid operations.

This bit automatically returns to "0" after the buffer is cleared.

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.
Note: In case the transmit data exists in the buffer for EP0_FIFO, the buffer empty interrupt occurs in the concerned endpoint when "1" is written to the BCLR bit.

(4) E0req (EP0_FIFO Ready) Bit (b11)

When this bit is equal to "1", this bit indicates the states as follows:

- EP0_FIFO Data Register can not be accessed.
- The IVAL bit value of this register is invalid.
- The ODLN bit values of this register are invalid.

Make sure that this bit is equal to "0" before accessing the aforesaid registers/bits.

(5) CCPL (Control Transfer Control) Bit (b10)

This bit controls the status stage of the control transfer.
When this bit is set to "1", the operations below are executed at status stage of the control transfer and notifies the normal completion of the control transfer:

●When set to control write transfer (ISEL bit = "0")

- Transmits the zero-length packet after receiving IN token if the EP0_PID bits are set to "01".

●When set to control read transfer (ISEL bit = "1")

- ACK response to the host after receiving the zero-length packet following OUT token if the EP0_PID bits are set to "01".

When this bit is set to "0", NAK response is executed to the host after receiving the IN token/OUT token at status stage of the control transfer.
This bit is automatically cleared to "0" by receiving the setup token.

(6) ODLN (Control Write Receive Data Length) Bits (b8~b0)

These bits are valid for control write transfer and indicate the data number (byte count) received from the CPU side buffer.
Further, these bits are set to execute countdown when the EP0_FIFO Data Register is read out. This operation changes according to the RCNT bit. For details, refer to "RCNT bit".
These bits indicate the valid value when the E0req bit of this register is equal to "0".

2.25 EP0_FIFO Data Register

■ EP0_FIFO Data Register (EP0_FIFO_DATA) <Address : H'34>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
EP0_FIFO															
?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'????>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15~0	EP0_FIFO EP0_FIFO Data	<When set to control write transfer> ■ Read Reads receive data <When set to control read transfer> ■ Write Writes transmit data	○	○

Note:The upper 8 bits (b15 to b8) become invalid in the 8-bit-mode (using the Octl bit of the EP0_FIFO Select Register or *HWR/*BYTE pin).

(1) EP0_FIFO (EP0_FIFO Data) Bits (b15~b0)

The receive data from the CPU side buffer is read or the transmit data to the CPU side buffer is written through this register.
When set to control write transfer (ISEL bit = "0"), the receive data from the buffer is read through this register.
When set to control read transfer (ISEL bit = "1"), the transmit data to the buffer is written through this register.
Make sure that the E0req bit is set to "0" before reading/writing these bits.

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.

2.26 EP0 Continuous Transmit Data Length Register

■ EP0 Continuous Transmit Data Length Register (EP0_SEND_LEN) <Address : H'36>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
							SDLN								
0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -

<H/W reset : H'0000>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15~9	Reserved. Set it to "0".		0	0
8~0	SDLN Control Read Continuous Transmit Data Length	Control read continuous transmit data length	○	○

(1) SDLN (Control Read Continuous Transmit Data Length) Bits (b8~b0)

These bits are valid when the EP0 is set to continuous transmit mode (CTRR bit = "1") at the time of control read transfer (ISEL bit = "1").
These bits set the total byte count of the data transmitted (over multiple transactions) during data stage of control read transfer.
These bits can be set to maximum 256 bytes. When total byte count exceeds 256, set the 256 bytes and the excess byte in several cycles.
When the integral multiples of the value set by the EP0 Packet Size Register is set to these bits, the zero-length packet is automatically added after all data are transmitted. The zero-length packet is not automatically added if the SDLN are set to 256 to transmit 256 bytes data or more.
Write to the buffer after setting this bit. Set these bits before writing to the buffer.

2.27 CPU_FIFO Select Register

■ CPU_FIFO Select Register (CPU_FIFO_SELECT) <Address : H'40>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
RCNT			RWND					BSWP	Octl			CPU_EP			
0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -

<H/W reset : H'0000>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15	RCNT Read Count Mode	0: The CPU_DTLN bits are cleared by reading all receive data 1: The CPU_DTLN bits are counted down by reading receive data	○	○
14~13	Reserved. Set it to "0".		0	0
12	RWND Buffer Rewind	<When set to OUT buffer> ■ Write 0 : Invalid (Ignored when written) 1 : Clears the buffer reading pointer <When set to IN buffer> ■ Write 0 : Invalid (Ignored when written) 1 : Clears the buffer writing pointer	0	○
11~8	Reserved. Set it to "0".		0	0
7	BSWP Byte Swap Mode	0 : Byte is treated as little ENDIAN 1 : Byte is treated as big ENDIAN	○	○
6	Octl Register 8-Bit Mode	0 : CPU_FIFO Data Register is 16-bit mode 1 : CPU_FIFO Data Register is 8-bit mode	○	○
5~4	Reserved. Set it to "0".		0	0
3~0	CPU_EP CPU Access Endpoint Designate	0001 :EP1 (Endpoint 1) 0010 :EP2 (Endpoint 2) 0011 :EP3 (Endpoint 3) 0100 :EP4 (Endpoint 4) 0101 :EP5 (Endpoint 5) 0110 :EP6 (Endpoint 6) Other than those above : Invalid	○	○

(1) RCNT (Read Count Mode) Bit (b15)

This bit sets the countdown methods of the CPU_DTLN bits at the time of reading the CPU_FIFO Data Register.
When this bit is set to "0", the CPU_DTLN bit value does not change in spite of reading the data from the CPU_FIFO Data Register, and is cleared to H'0 when all data is read out.
When this bit is set to "1", the CPU_DTLN bit values are counted down every time the data is read from the CPU_FIFO Data Register. Here, the down-count value differs as shown below depending on whether the CPU_FIFO Data Register is set to 8-bit mode or 16-bit mode:

- 8-bit mode : Down-count per "-1"
- 16-bit mode : Down-count per "-2"

Note : Use the *HWR/*BYTE pin or the Octl bit of this register for setting the 8-bit/16-bit mode.

(2) RWND (Buffer Rewind) Bit (b12)

This bit rewinds (initializes) the buffer pointer.

- When set to OUT buffer (EPi_DIR bit = "0")
  When the IVAL bit of the CPU_FIFO Control Register is set to "1", the buffer reading pointer can be initialized by writing "1" to this bit. This enables reading of the receive data from the beginning.
- When set to IN buffer (EPi_DIR bit = "1")
  When the IVAL bit of the CPU_FIFO Control Register is set to "0", the buffer writing pointer can be initialized by writing "1" to this bit. This enables resetting of the transmit data from the beginning. The operation is equivalent to the case when "1" is set to the BCLR bit if set to IN buffer.

(3) BSWP (Byte Swap Mode) Bit (b7)

This bit sets the endian of the CPU_FIFO Data Register.
When this bit is set to "0", the CPU_FIFO Data Register gets such as little endian.
When this bit is set to "1", the CPU_FIFO Data Register gets such as big endian.

	b15~b8	b7~b0
Little Endian	odd number address	even number address
Big Endian	even number address	odd number address

Note: Do not set this bit to "1" when the mode is set to 8-bit (set by the Octl bit or *HWR/*BYTE pin).

(4) Octl (Register 8-Bit Mode) Bit (b6)

This bit sets the access mode of the CPU_FIFO Data Register.
When this bit is set to "0", the CPU_FIFO Data Register is set to 16-bit mode, and all bits of the CPU_FIFO Data Register are valid.
When this bit is set to "1", the CPU_FIFO Data Register is set to 8-bit mode, and the upper-order 8 bits of the CPU_FIFO Data Register (b15 to b8) are invalid.
When set to OUT buffer (EPi_DIR bit = "0"), change this bit before receiving the data. When set to IN buffer (EPi_DIR bit = "1"), if the Creq bit is equal to "1", do not change this bit.
This bit becomes invalid (fixed to 8-bit mode) when the mode is set to 8-bit by *HWR/*BYTE pin.
In such case, this bit is read "0".

Note: The access width of the CPU_FIFO Data Register is controlled by the logical sum of this bit and the EPi_Octl bits of the EPi Configuration Register 1 specified by the CPU_EP bits. Hence, the mode is set to 8-bit if "1" is set to either this bit or to the EPi_Octl bits of the EPi Configuration Register 1. Make sure that both bits must be set to "0" to change to 16-bit mode.

(5) CPU_EP (CPU Access Endpoint Designate) Bits (b3~b0)

These bits select the endpoint accessed by CPU.
Make sure that the endpoint selection does not get overlapped with the selection by the DMA_EP bits.
When making a change in these bits to select the other the endpoint, make sure that the source endpoint and the destination endpoint to be changed are not under the access by the CPU or during receiving/transmitting of SIE (under access to FIFO buffer).

2.28 CPU_FIFO Control Register

■ CPU_FIFO Control Register (CPU_FIFO_CONTROL) <Address : H'42>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
	IDLY	IVAL	BCLR	Creq	CPU_DTLN										
0 - -	0 - -	0 - -	0 - -	1 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -

<H/W reset : H'0800>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15	Reserved. Set it to "0".		0	0
14	IDLY Isochronous Transmit Delay Set	0 : Disable of IDLY function 1 : Enable of IDLY function	○	○
13	IVAL IN Buffer Set/OUT Buffer Status	<When set to OUT buffer> ■ Read 0: Disables reading data from the buffer 1: Enables reading data from the buffer ■ Write Invalid (Ignored when written) <When set to IN buffer> ■ Read 0 : Incomplete to write the data to buffer 1 : Complete to write the data to buffer ■ Write 0 : Invalid (Ignored when written) 1 : Complete to write the data to buffer (Forced completion : Transmits short packet)	○	○
12	BCLR Buffer Clear	<When set to OUT buffer> ■ Write 0 : Invalid (Ignored when written) 1 : Buffer clear (When the IVAL bit is set to "1") <When set to IN buffer> ■ Write 0 : Invalid (Ignored when written) 1 : Buffer clear (When the IVAL bit is set to "0")	0	○
11	Creq CPU_FIFO Ready	0 : Enables accessing CPU_FIFO Data Register etc, 1 : Disables accessing CPU_FIFO Data Register etc,	○	×
10~0	CPU_DTLN CPU_FIFO Receive Data Length Register	Stores the receive data length (byte count)	○	×

(1) IDLY (Isochronous Transmit Delay Set) Bit (b14)

In isochronous transfer, transmission can be started by writing "1" to this bit or to the IVAL bit after writing the transmit data to the buffer (Note).
When "1" is written to this bit, the data is transmitted by receiving the IN token after confirming the received SOF packet. After the data transmit starts, this is cleared to "0" (Refer to Figure 2.11).
When "1" is written to the IVAL bit of this register, the data is transmitted by receiving the next IN token (Refer to Figure 2.12).

Note: Set the transmit data size + 1 byte or more to the EPi_MXPS bits. When set to transmit data size, the IVAL bit is set to "1" when the writing to the buffer completes. Hence, this function is not applicable when set to 1023 bytes, the maximum value of the EPi_MXPS bits.

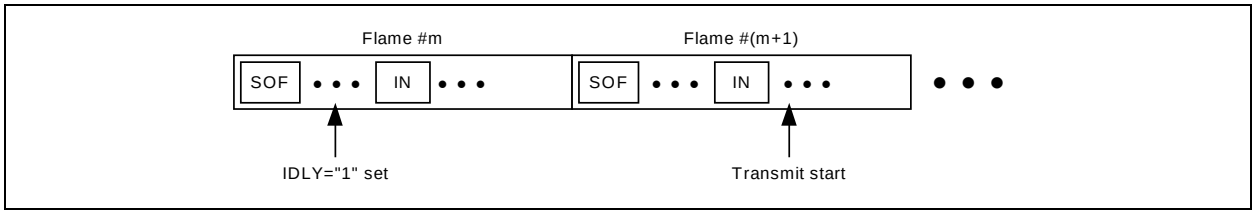


Figure 2.11 Transmit start timing at IDLY bit = "1"

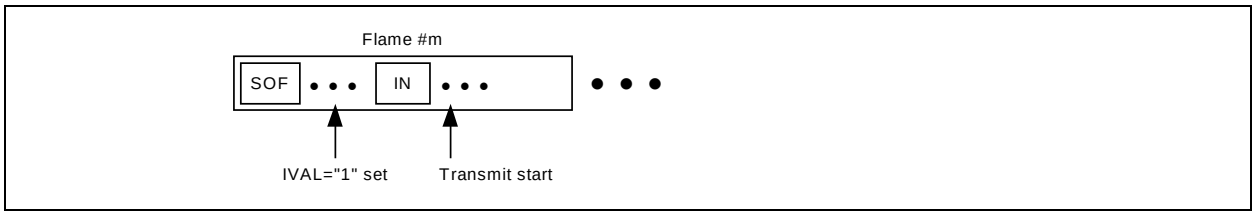


Figure 2.12 Transmit start timing at IVAL bit = "1"

(2) IVAL (IN Buffer Set/OUT Buffer Status) Bit (b13)

This bit indicates valid value when the Creq bit of this register is equal to "0".
This bit sets/clears the EPB_RDY bit to "1" (Refer to "EPB_RDY bit").

●When set to OUT buffer (EPi_DIR bit = "0")
When this bit is set to "1", the receive data in the CPU side buffer is ready to be read.

This bit is set to "1" due to one of the reasons as follows:
○When set to single buffer mode (EPi_DBLB bit = "0")
- Completes receiving (SIE side buffer).
- Writes "1" to the TGL bit.

○When set to double buffer mode (EPi_DBLB bit = "1")
- Completes receiving of SIE side buffer and reading of CPU side buffer.
- Writes "1" to the TGL bit.

The receive completion is changed by the EPi_RWMD bit.

This bit is cleared to "0" due to one of the reasons as follows:
- Reads out all the receive data in the CPU side buffer.
- Writes "1" to the BCLR bit.
- Writes "1" to the ACLR bit.

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.

●When set to IN buffer (EPi_DIR bit = "1")
When this bit is set to "0", the CPU side buffer is ready to write the transmit data.

This bit is cleared to "0" due to one of the reasons as follows:
○When set to single buffer mode (EPi_DBLB bit = "0")
- Completes transmitting of SIE side buffer.
- Writes "1" to the SCLR bit.
- Writes "1" to the ACLR bit.

○When set to double buffer mode (EPi_DBLB bit = "1")
- Completes transmitting of SIE side buffer and writing of CPU side buffer.
- Writes "1" to the SCLR bit.
- Writes "1" to the ACLR bit.
- Writes "1" to the BCLR bit.

The transmit completion is changed by the EPi_RWMD bit.

This bit is set to "1" due to one of the reasons as follows:
- Completes writing the transmit data to CPU side buffer.
- Writes "1" to this bit.

  When "1" is written to this bit, the write operation is forcibly completed. When some written data exists in the buffer, that data is solely transmitted as the short packet. Here, if the buffer is empty or cleared, the zero-length packet is transmitted. The buffer can be cleared using the BCLR bit. Further, the zero-length packet can be transmitted by writing "1" simultaneously to this bit and to the BCLR bit. In this case the buffer is cleared by setting "1" to BCLR bit, and this bit is cleared to "0" after the zero-length packet is transmitted.

The write completion also is changed by the EPi_RWMD bit.

(3) BCLR (Buffer Clear) Bit (b12)

This bit clears the data written to the CPU side buffer.

●When set to OUT buffer (EPi_DIR bit = "0")
When the IVAL bit is set to "1", the following operations are executed by writing "1" to this bit:
- Clears CPU side buffer.
- Clears the IVAL bit of this register.
- Clears the CPU_DTLN bits of this register.

●When set to IN buffer (EPi_DIR bit = "1")
When the IVAL bit is set to "0", the following operations are executed by writing "1" to this bit:
- Clears CPU side buffer.

Further, the zero-length packet can be transmitted by writing "1" simultaneously to this bit and to the IVAL bit. For details, refer to "IVAL bit".

This bit automatically returns to "0" after the buffer is cleared.

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.

(4) Creq (CPU_FIFO Ready) Bit (b11)

When this bit is equal to "1", this bit indicates the states as follows:
- CPU_FIFO Data Register can not be accessed.
- The IVAL bit value of this register is invalid.
- The CPU_DTLN bit values of this register are invalid.

Make sure that this bit is equal to "0" before accessing the aforesaid registers/bits.

(5) CPU_DTLN (CPU_FIFO Receive Data Length Register) Bits (b10~b0)

These bits are valid against the endpoint set to the OUT buffer (EPi_DIR bit = "0") and indicates the receive data number (byte count) in the CPU side buffer.
Further, these bits are set to execute countdown when the CPU_FIFO Data Register is read out. This operation changes according to the RCNT bit of the CPU_FIFO Select Register. For details, refer to "RCNT bit".
These bits indicate the valid value when the Creq bit of this register is equal to "0".

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.

2.29 CPU_FIFO Data Register

■ CPU_FIFO Data Register (CPU_FIFO_DATA) <Address : H'44>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
CPU_FIFO															
? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -

<H/W reset : H'????>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15~0	CPU_FIFO CPU_FIFO Data	<When set to OUT buffer> ■ Read Reads receive data <When set to IN buffer> ■ Write Writes transmit data	○	○

Note:The upper 8 bits (b15 to b8) become invalid in the 8-bit mode (using the Octl bits or *HWR/*BYTE pin).

(1) CPU_FIFO(CPU_FIFO Data) Bits (b15~b0)

The receive data from the CPU side buffer is read or the transmit data to the CPU side buffer is written through this register.
When set to OUT buffer (EPi_DIR bit = "0"), the receive data from the CPU side buffer is read through this register.
When set to IN buffer (EPi_DIR bit = "1"), the transmit data to the CPU side buffer is written through this register.
Make sure that the Creq bit is equal to "0" before reading/writing these bits.

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.
Note: When set to 16-bit mode, the M66291 is capable of recognizing the byte data written. Hence, it is possible to transmit the odd byte data by setting "1" to the IVAL bit after writing the byte data.

2.30 SIE_FIFO Status Register

■ SIE_FIFO Status Register (SIE_FIFO_STATUS) <Address : H'46>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
		TGL	SCLR	Sreq	SIE_DTLN										
0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -

<H/W reset : H'0000>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15~14	Reserved. Set it to "0".		0	0
13	TGL Buffer Toggle	<When set to OUT buffer> ■ Write 0 : Invalid (Ignored when written) 1 : Forces the buffer to toggle in receive ready state to read ready state <When set to IN buffer> ■ Write 0 : Invalid (Ignored when written) 1 : Inhibited	0	○
12	SCLR Buffer Clear	<When set to OUT buffer> ■ Write 0 : Invalid 1 : Inhibited <When set to IN buffer> 0 : Invalid (Ignored when written) 1 : Clears the buffer in transmit ready state	0	○
11	Sreq SIE_FIFO Ready	0 : Enables to be write to TGL bit/SCLR bit 1 : Disables to be write to TGL bit/SCLR bit	○	×
10~0	SIE_DTLN SIE_FIFO Receive Data Length	Receive data length of SIE internal FIFO	○	×

This register is valid against the endpoint set by the CPU_EP bits.

(1) TGL (Buffer Toggle) Bit (b13)

This bit is valid against the endpoint set to the OUT buffer (EPi_DIR bit = "0") and is used for continuous transmit/receive mode (EPi_RWMD = "1"). Do not write "1" when set to the IN buffer (EPi_DIR bit = "1") When "1" is written to this bit, the SIE side buffer is forced to complete receiving. The buffer is toggled, irrespective of the presence/absence of the CPU side buffer data (causing the SIE side buffer to complete receiving and to get toggled, and the IVAL bit to set to "1"). Make sure that the buffer data in the CPU side are not cleared.
Here, the EPB_RDY bit also is set to "1" (buffer ready interrupt occurs).

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.
Note: Make sure that the response PID is set to NAK (EPi_PID bits = "00") and the Sreq bit to "0" before writing "1" to this bit.

(2) SCLR (Buffer Clear) Bit (b12)

This bit is valid against the endpoint set to the IN buffer (EPi_DIR bit = "1"). Do not write "1" when set to the OUT buffer (EPi_DIR bit = "0")
The SIE side buffer is cleared by writing "1" to this bit.

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.
Note: Make sure that the response PID is set to NAK (EPi_PID bits = "00") and the Sreq bit to "0" before writing "1" to this bit.

(3) Sreq (SIE_FIFO Ready) Bit (b11)

This bit indicates to enable/disable of writing to the TGL bit and SCLR bit.
When this bit is set to "1", do not write to the TGL bit and SCLR bit.

(4) SIE_DTLN (SIE_FIFO Receive Data Length) Bits (b10~b0)

These bits are valid against the endpoint set to the OUT buffer (EPi_DIR bit = "0") and indicates the receive data number (byte count) in the SIE side buffer (renewed after every ACK transmit).

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.

2.31 Dn_FIFO Select Registers (n=0~1)

■ D0_FIFO Select Register (D0_FIFO_SELECT) <Address : H'48>
■ D1_FIFO Select Register (D1_FIFO_SELECT) <Address : H'50>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
BUST	DFORM		RWND	ACKA	REQA	INTM	DMAEN	BSWP	Octl			DMA_EP			
0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -

<H/W reset : H'0000>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15	BUST Burst Mode	0 : Cycle Steal Transfer 1 : Burst Transfer	○	○
13~14	DFORM Transfer Method	00 : Controls by DACK signal and read/write signal 01 : Controls by DACK signal only 10 : Controls by chip select/address signal and read/write signal 11 : Reserved	○	○
12	RWND Buffer Rewind	<When set to OUT buffer> ■ Write 0 : Invalid (Ignored when written) 1 : Clears the buffer reading pointer <When set to IN buffer> ■ Write 0 : Invalid (Ignored when written) 1 : Clears the buffer writing pointer	0	○
11	ACKA DACK Polarity	0 : "L" active 1 : "H" active	○	○
10	REQA DREQ Polarity	0 : "L" active 1 : "H" active	○	○
9	INTM DMA Interrupt Mode	0 : Sets "1" to EPB_RDY bit by completion of DMA transfer 1 : Sets "1" to EPB_RDY bit by completion of receiving	○	○
8	DMAEN DMA Enable	0 : Disable DMA transfer 1 : Enable DMA transfer (assertion of DREQ signal)	○	○
7	BSWP Byte Swap Mode	0 : Byte is treated as little ENDIAN 1 : Byte is treated as big ENDIAN	○	○
6	Octl Register 8-Bit Mode	0 : Dn_FIFO Data Register is 16-bit mode 1 : Dn_FIFO Data Register is 8-bit mode	○	○
5~4	Reserved. Set it to "0".		0	0
3~0	DMA_EP DMA Transfer Endpoint Designate	0001 :EP1 (Endpoint 1) 0010 :EP2 (Endpoint 2) 0011 :EP3 (Endpoint 3) 0100 :EP4 (Endpoint 4) 0101 :EP5 (Endpoint 5) 0110 :EP6 (Endpoint 6) Other than those above : Invalid	○	○

(1) BUST (Burst Mode) Bit (b15)

When set to cycle steal transfer, the assertion and negation of the DREQ signal are repeated every time the signal is subjected to DMA transfer (8-bit or 16-bit) when the CPU side buffer can be accessed. The negation is executed when the Dn_FIFO Data Register is accessed.
When set to burst transfer, it keeps on asserting the DREQ signal until the reading/writing of the CPU side buffer completes when the CPU side buffer can be accessed.
It is possible to forcibly complete the writing and then enabling transmit of short packet by asserting the TC signal at the time of writing.

(2) DFORM (Transfer Method) Bit (b14~b13)

These bits select the DMA transfer method.

- When set to "00"
  At the time of reading, the data of the Dn_FIFO Data Register is available while the DACK signal is at "L" and the read signal at "L".
  At the time of writing, the data is written to the Dn_FIFO Data Register when the DACK signal is at "L" and by the rising edge of write signal.
- When set to "01"
  Only the DACK signal is used and the Read/Write signal is not used (the Read/Write signal is ignored).
  At the time of reading, the data of the Dn_FIFO Data Register is available while the DACK signal is at "L".
  At the time of writing, the data is written to the Dn_FIFO Data Register by the rising edge of DACK signal.
- When set to "10"
  In place of the DACK signal (the DACK signal is ignored here), the address signal can be used to read/write the data of the Dn_FIFO Data Register.
  At the time of reading, the data of the Dn_FIFO Data Register is available when the read signal is at "L".
  At the time of writing, the data is written to the Dn_FIFO Data Register by the rising edge of write.

When the endpoint set to the OUT buffer (EPi_DIR bit = "0") is assigned to the DMA_EP, writing operation to the Dn_FIFO Data Register is ignored.
Similarly, when the endpoint set to the IN buffer (EPi_DIR bit = "1") is assigned to the DMA_EP, reading operation to the Dn_FIFO Data Register is ignored (undefined value is read).

(3) RWND (Buffer Rewind) Bit (b12)

This bit rewinds (clears) the buffer pointer.

- When set to OUT buffer (EPi_DIR bit = "0")
  When the IVAL bit of the Dn_FIFO Control Register is set to "1", the buffer reading pointer can be cleared by writing "1" to this bit. This enables reading of the receive data from the beginning.
- When set to IN buffer (EPi_DIR bit = "1")
  When the IVAL bit of the Dn_FIFO Control Register is set to "0", the buffer writing pointer can be cleared by writing "1" to this bit. This enables resetting of the transmit data from the beginning.

(4) ACKA (DACK Polarity) Bit (b11)

This bit sets the DACK signal polarity.

(5) REQA (DREQ Polarity) Bit (b10)

This bit sets the DREQ signal polarity.

(6) INTM (DMA Interrupt Mode) Bit (b9)

This bit sets the timing of setting "1" to the EPB_RDY bit.

<When set to OUT buffer (EPi_DIR bit = "0")>

When this bit is set to "0", the EPB_RDY bit is set to "1" after reading all buffer data including the received short packet (including the zero-length packet) <buffer ready interrupt occurs>.
In case of reading the buffer, the buffer state as well as the bits below are retained. This enables the reading of the received data length using the buffer ready interrupt.

- IVAL bit of the Dn_FIFO Control Register ("1" retained)
- DMA_DTLN bits of the Dn_FIFO Control Register

It is necessary to write "1" to the BCLR bit and to clean the buffer in order to receive the next data. Thus clears the IVAL bit to "0", and the EPB_RDY bits also are cleared if the RDYM bit is set to "0". If the RDYM bit is set to "1", the EPB_RDY bits are cleared to "0" by writing "0" to the EPB_RDY bit.

When this bit is set to "1", the EPB_RDY bit is set to "1" under the same conditions as the endpoint not specified by the DMA_EP bits (buffer ready interrupt occurs).

<When set to IN buffer (EPi_DIR bit = "1")>

When this bit is set to "0", the EPB_RDY bit cannot be set to "1".

When this bit is set to "1", the EPB_RDY bit is set to "1" under the same conditions as the endpoint not specified by the DMA_EP bits (buffer ready interrupt occurs).

Note: Do not use with DMAEN = "0" when this bit is set to "0".

(7) DMAEN (DMA Enable) Bit (b8)

This bit sets the enable/disable of the output of the DREQ signal for DMA transfer.
When this bit is set to "1", the DMA transfer is set to enable mode, making the DREQ signal ready for assertion.
When this bit is written to "0", the DMA transfer is disabled, allowing no output of DREQ signal.

Note: Do not use with INTM = "0" when this bit is set to "0".

(8) BSWP (Byte Swap Mode) Bit (b7)

This bit sets the endian of the Dn_FIFO Data Register.
When this bit is set to "0", the Dn_FIFO Data Register gets such as little endian.
When this bit is set to "1", the Dn_FIFO Data Register gets such as big endian.

	b15~b8	b7~b0
Little Endian	odd number address	even number address
Big Endian	even number address	odd number address

Note: Don't set this bit to "1" when the mode is set to 8-bit (set by the Octl bit or *HWR/*BYTE pin).

(9) Octl (Register 8-Bit Mode) Bit (b6)

This bit sets the access mode of the Dn_FIFO Data Register.
When this bit is set to "0", the Dn_FIFO Data Register is set to 16-bit mode, and all bits of the Dn_FIFO Data Register are valid.
When this bit is set to "1", the Dn_FIFO Data Register is set to 8-bit mode, and the upper-order 8 bits of the Dn_FIFO Data Register (b15 to b8) are invalid.
When set to OUT buffer (EPi_DIR bit = "0"), change this bit before receiving the data. When set to IN buffer (EPi_DIR bit = "1"), if the Dreq bit is equal to "1", do not change this bit.
This bit becomes invalid (fixed to 8-bit mode) when the mode is set to 8-bit by *HWR/*BYTE pin.
In such case, this bit is read "0".

Note: The access width of the Dn_FIFO Data Register is controlled by the logical sum of this bit and the EPi_Octl bits of the EPi Configuration Register 1 specified by the DMA_EP bits. Hence, the mode is set to 8-bit if "1" is set to either this bit or to the EPi_Octl bits of the EPi Configuration Register 1. Make sure that both bits must be set to "0" to change to 16-bit mode.

Note: Do not change this bit while accessing the Dn_FIFO Data Register.

(10) DMA_EP (DMA Transfer Endpoint Designate) Bits (b3~b0)

These bits select the endpoint of DMA transfer.
Make sure that the endpoint selection does not get overlapped with the selection by the CPU_EP bits.
When making a change in these bits to select the other endpoint, make sure that the source endpoint and the destination endpoint to be changed are not under the access by the CPU/DMA or during receiving/transmitting of SIE (under access to FIFO buffer).

2.32 Dn_FIFO Control Registers (n=0~1)

■ D0_FIFO Control Register (D0_FIFO_CONTROL) <Address : H'4A>
■ D1_FIFO Control Register (D1_FIFO_CONTROL) <Address : H'52>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
TRCLR	TREN	IVAL	BCLR	Dreq	DMA_DTLN										
0 - -	0 - -	0 - -	0 - -	1 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -

<H/W reset : H'0800>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15	TRCLR Transaction Count Clear	■ Write 0 : Invalid (Ignored when written) 1 : Clears the DMAn_Transaction Count Register	0	○
14	TREN Transaction Count Enable	0 : Disable of transaction count function 1 : Enable of transaction count function	○	○
13	IVAL IN Buffer Set/OUT Buffer Status	<When set to OUT buffer> ■ Read 0: Disables the reading of data from the buffer 1: Enables the reading of data from the buffer ■ Write Invalid (Ignored when written) <When set to IN buffer> ■ Read 0 : Incomplete to write the data to buffer 1 : Complete to write the data to buffer ■ Write 0 : Invalid (Ignored when written) 1 : Complete to write the data to buffer (Forced completion : Transmits short packet)	○	○
12	BCLR Buffer Clear	<When set to OUT buffer> ■ Write 0 : Invalid (Ignored when written) 1 : Buffer clear (When the IVAL bit is set to "1") <When set to IN buffer> ■ Write 0 : Invalid (Ignored when written) 1 : Buffer clear	0	○
11	Dreq D_FIFO Ready	0 : Enables to access Dn_FIFO Data Register 1 : Disables to access Dn_FIFO Data Register	○	×
10~0	DMA_DTLN D_FIFO Receive Data Length Register	Stores the receive data length (byte count)	○	×

(1) TRCLR (Transaction Count Clear) Bit (b15)

When written to "1", this bit clears the value of the DMAn_Transaction Count Register.
The writing of "1" to this bit is not retained and is automatically cleared to "0".

(2) TREN (Transaction Count Enable) Bit (b14)

This bit sets the enable/disable of transaction count function.
Refer to "2.34 DMAn_Transaction Count Registers (n=0~1)".

(3) IVAL (IN Buffer Set/OUT Buffer Status) Bit (b13)

This bit indicates valid value when the Dreq bit of this register is equal to "0".
The operation of this bit is the same as that of the IVAL bit of the CPU_FIFO Control Register.
Take care the setting of the EPB_RDY bit to "1" using this bit (buffer ready interrupt occurs) changes according to the INTM bit (Refer to "EPB_RDY/INTM bit").

(4) BCLR (Buffer Clear) Bit (b12)

This bit indicates valid value when the Dreq bit of this register is set to "0".
The operation of this bit is the same as that of the BCLR bit of the CPU_FIFO Control Register.

(5) Dreq (D_FIFO Ready) Bit (b11)

When this bit is equal to "1", this bit indicates the states as follows:

- Dn_FIFO Data Register can not be accessed.
- The IVAL bit value of this register is invalid.
- The DMA_DTLN bit values of this register are invalid.

Make sure that this bit is equal to "0" before making access to the aforesaid registers/bits.

(6) DMA_DTLN (D_FIFO Receive Data Length Register) Bits (b10~b0)

These bits are valid against the endpoint set to the OUT buffer (EPi_DIR bit = "0") and indicates the receive data number (byte count) in the CPU side buffer.

These bits indicate the valid value when the Dreq bit of this register is equal to "0".

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.

2.33 Dn_FIFO Data Registers (n=0~1)

■ D0_FIFO Data Register (D0_FIFO_DATA) <Address : H'4C>
■ D1_FIFO Data Register (D1_FIFO_DATA) <Address : H'54>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
D_FIFO															
? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -	? - -

<H/W reset : H'????>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15~0	D_FIFO D_FIFO Data	<When set to OUT buffer> ■ Read Reads receive data <When set to IN buffer> ■ Write Writes transmit data	○	○

Note:The upper 8 bits (b15 to b8) become invalid in the 8-bit mode (using the Octl bits or *HWR/*BYTE pin).

(1) D_FIFO(D_FIFO Data) Bits (b15~b0)

The receive data from the CPU side buffer is read or the transmit data to the CPU side buffer is written through this register.
When set to OUT buffer (EPi_DIR bit = "0"), the receive data from the CPU side buffer is read through this register.
When set to IN buffer (EPi_DIR bit = "1"), the transmit data to the CPU side buffer is written through this register.
Make sure that the Dreq bit is equal to "0" before reading/writing these bits when the DMAEN bit is set to "0".

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.
Note: When set to 16-bit mode, the M66291 is capable of recognizing the byte data written. Hence, it is possible to transmit the odd byte data by setting "1" to the IVAL bit or asserting the TC pin after writing the byte data.

2.34 DMAn_Transaction Count Registers (n=0~1)

■ DMA0_Transaction Count Register (DMA0_TRN_COUNT) <Address : H'4E>
■ DMA1_Transaction Count Register (DMA1_TRN_COUNT) <Address : H'56>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
TRNCNT															
0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -

<H/W reset : H'0000>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15~0	TRNCNT Transaction Count	<TREN bit = "0"> Packet count that completes the receiving (behaving as the compare register) <TREN bit = "1"> ■ Read The number of the received packets (behaving as the current register) ■ Write Packet count that completes the receiving (behaving as the compare register)	○	○

(1) TRNCNT (Transaction Count) Bits (b15~b0)

This register is used under the following conditions:

- When set to OUT buffer (EPi_DIR bit = "0").
- When set to continuous receive mode (EPi_RWMD bit = "1").
- When set to bulk transfer mode (EPi_TYP bits = " 01")
- When accessing using Dn_FIFO Data Register.

With the transaction count function set to be enabled (TREN bit = "1"), the following conditions are added to the buffer receive completion condition. In case of the receive completion, refer to the "EPi_RWMD bit of the EPi Configuration Register 0".

- When the value set by this register conforms to the packet receive count.
  (Conformity between current register and compare register; See below.)

This register is composed of two registers as follows:

- Current register :Counting of the received packet number (counts up at the TREN bit = "1")
- Compare register :The value that completes the receiving

It is necessary to clear the TNCNT bits as the current register to "0" by writing "1" to the TRCLR bit before the next transfer.

2.35 FIFO Status Register

■ FIFO Status Register (FIFO_STATUS) <Address : H'58>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
									EPB_STS						
0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -

<H/W reset : H'0000>
<S/W reset : H'0000>
<USB bus reset : ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		0	0
6~0	EPB_STS Endpoint 0~6 Buffer Status	■ Read 0: Disables the reading and writing of data to and from the buffer 1: Enables the reading and writing of data to and from the buffer	○	×

(1) EPB_STS (Endpoint 0~6 Buffer Status) Bits (b6~b0)

The condition for setting this bit to "1" is the same as that of the Interrupt Status Register 1. Make sure that the condition for clearing this bit to "0" differs as follows.

The condition for clearing this bit to "0" is always the same as in the case of the RDYM bit set to "0". Hence, the presence/absence of data in the buffer can be confirmed by reading these bits even after the interrupt is cleared by writing "0" to the Interrupt Status Register 1.

2.36 Port Control Register

■ Port Control Register (PORT_CNTL) <Address : H'5A>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
	PIEN								PDIR						
0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -

<H/W reset : H'0000>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15	Reserved. Set it to “0”.		0	0
14~8	PIEN Port Input Enable	0 : Disable Port Input 1 : Enable Port Input The port number corresponds to the bit number. b8 :P0 pin b9 :P1 pin b10 :P2 pin b11 :P3 pin b12 :P4 pin b13 :P5 pin b14 :P6 pin	○	○
7	Reserved. Set it to “0”.		0	0
6~0	PDIR Port Direction	0 : Input Port 1 : Output Port The port number corresponds to the bit number. b0 :P0 pin b1 :P1 pin b2 :P2 pin b3 :P3 pin b4 :P4 pin b5 :P5 pin b6 :P6 pin	○	○

The port pins, P0 ~ P6, automatically turn to input/output ports by setting to 8-bit bus interface mode (controlled by HWR/BYTE pin). When set to 16-bit bus interface mode, all functions of this register become invalid. Further, the writing into this register at 16-bit bus interface mode becomes invalid while the reading becomes H’0000.

(1) PIEN (Port Input Enable) Bits (b14~b8)

These bits set the enable/disable of port input.
When "0" is written to this bit, the related port pin does not work as the input pin even if the PDIR bit of this register is set to "0". In this case the related port pin is in the high-impedance state. In this state, the port data is read out as "0".
When the PDIR bit of this register is set to "0", the related port pin works as the input pin by writing "1" to this bit.
When the PDIR bit of this register is set to "1", these bits become invalid (and works as an output port).

(2) PDIR (Port Input/Output Select) Bits (b6~b0)

These bits select input/output direction of the port pin.

2.37 Port Data Register

■ Port Data Register (PORT_DATA) <Address : H'5C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
									PDAT						
0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -

<H/W reset : H'0000>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to “0”.		0	0
6~0	PDAT Port Data	0 : ”L” level 1 : ”H” level The port number corresponds to the bit number. b0 : P0 pin b1 : P1 pin b2 : P2 pin b3 : P3 pin b4 : P4 pin b5 : P5 pin b6 : P6 pin	○	○

The port pins, P0 ~ P6, automatically turn to input/output ports by setting to 8-bit bus interface mode (controlled by HWR/BYTE pin). When set to 16-bit bus interface mode, all functions of this register become invalid. Further, the writing into this register at 16-bit bus interface mode becomes invalid while the reading becomes H’0000.

(1) PDAT (Port Data) Bits (b6~b0)

These bits indicate the port pin state.
When the PIEN bit of the Port Control Register is set to “0”, this bit reads out “0”.

2.38 Drive Current Adjust Register

■ Drive Current Adjust Register (I_ADJ) <Address : H'5E>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	LDRV 0 - -

<H/W reset : H'0000>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15~1	Reserved. Set it to “0”.		0	0
0	LDRV Drive Current Adjust	0 : When IOVcc=2.7~3.6V 1 : When IOVcc=4.5~5.5V	○	○

(1) LDRV (Drive Current Adjust) Bit (b0)

This bit is used to adjust the drive current of the output pins.
The output pins here refer to D15/A0, D14/P6~D8/P0, D7~D0, *INT0, *INT1/*SOF, *Dreq0, and *Dreq1 pins.

2.39 EPi Configuration Registers 0 (i=1~6)

■ EP1 Configuration Register 0 (EP1_0CONFIG) <Address : H'60>
■ EP2 Configuration Register 0 (EP2_0CONFIG) <Address : H'64>
■ EP3 Configuration Register 0 (EP3_0CONFIG) <Address : H'68>
■ EP4 Configuration Register 0 (EP4_0CONFIG) <Address : H'6C>
■ EP5 Configuration Register 0 (EP5_0CONFIG) <Address : H'70>
■ EP6 Configuration Register 0 (EP6_0CONFIG) <Address : H'74>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
EPi_TYP		EPi_DIR	EPi_ITMD	EPi_Buf_siz				EPi_DBLB	EPi_RWMD	EPi_Buf_Nmb					
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0000>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15~14	EPi_TYP Transfer Type	00 : Invalid 01 : Bulk transfer 10 : Interrupt transfer 11 : Isochronous transfer	○	○
13	EPi_DIR Transfer Direction	0 : OUT buffer (Receives data from the host) 1 : IN buffer (Transmits data to the host)	○	○
12	EPi_ITMD Interrupt Toggle Mode	0 : Enable data resend function (normal toggle mode) 1 : Disable data resend function (forced toggle mode)	○	○
11~8	EPi_Buf_siz Buffer Size	Endpoint buffer size	○	○
7	EPi_DBLB Double Buffer Mode	0 : Single buffer mode 1 : Double buffer mode	○	○
6	EPi_RWMD Continuous Transmit/Receive Mode	0 : Single transmit /receive mode 1 : Continuous transmit/receive mode	○	○
5~0	EPi_Buf_Nmb Buffer Start Number	The top block number of buffer	○	○

(1) EPi_TYP (Transfer Type) Bits (b15~b14)

These bits are used to set the transfer type of the endpoint.

(2) EPi_DIR (Transfer Direction) Bit (b13)

This bit is used to set the transfer direction of the endpoint.
After switching the transfer direction, clear the buffer by the BCLR bit.

(3) EPi_ITMD (Interrupt Toggle Mode) Bit (b12)

This bit sets the enable/disable of data resend function at interrupt transfer.
This bit can be set to "1" only when the transfer type is set to interrupt transfer (EPi_TYP bits = "10"). Set this bit to "0" for other transfer modes.

When the data resend function is set to disable, the new data is transmitted at the next transmission by toggling the DATA PID and the buffer, even if the ACK is not received after transmitting the data at interrupt transfer. Here, the IVAL bit is cleared to "0" and the EPB_RDY bit is set to "1" (buffer ready interrupt has occurred).
When the data resend function is set to enable, the normal toggle sequence is executed. When the transmission completes normally, the DATA PID and the buffer got toggled to transmit the next data. In case ACK cannot be received after the data is transmitted, the DATA PID and the buffer do not get toggle, and the same data in the buffer is resent.

(4) EPi_Buf_siz (Buffer Size) Bits (b11~b8)

These bits set the buffer size in 64-byte unit (Note).
When set to double buffer mode (EPi_DBLB bit = "1"), the buffer double in size set by these bits is used.

Set the values to these bits as follows:

- Continuous transmit/receive mode : Value set by this register > Value set by the EPi_MXPS bits
- Single transmit/receive mode : Value set by this register ≥ Value set by the EPi_MXPS bits

Set in the manner as follows (single transmit/receive mode only) to write "1" to the IDLY bit at isochronous transfer mode (set by EPi_TYP bits):

- Single transmit/receive mode : Value set by this register > Value set by the EPi_MXPS bits

When set to IN buffer (EPi_DIR bit = "1"), if the integral multiples of the value set by the EPi_MXPS bits is set to these bits, the zero-length packet can be added after all data are transmitted. For details, refer to the setting of "1" to the EPi_NULMD bit.

Note: The M66291 is equipped with 3 Kbytes FIFO buffer. The Maximum buffer size is 1024Bytes for an endpoint, and the minimum one is 64Bytes.

(5) EPi_DBLB (Double Buffer Mode) Bit (b7)

This bit sets the single buffer mode/double buffer mode.
This bit is applicable to bulk/isochronous/interrupt transfers (set by the EPi_TYP bits).
When set to double buffer mode, 2 buffers of size set by the EPi_Buf_siz bits are secured and are allocated to SIE side buffer and CPU side buffer.

●Double buffer mode when set to OUT buffer (EPi_DIR bit = "0")

○SIE side buffer:

- The data received by SIE can be written.
- Can not be accessed by CPU/DMA.

○CPU side buffer:

- Can not be accessed by SIE.
- The received data can be read by CPU/DMA.

○Buffer toggle condition (switching of SIE side buffer and CPU side buffer)

- SIE side buffer receive completion and CPU side buffer read completion (empty)
  The receive completion changes according to the single/continuous transmit/receive mode.
  For details, refer to the "EPi_RWMD bit" and the "TGL bit".

●Double buffer mode when set to IN buffer (EPi_DIR bit = "1")

○SIE side buffer:

- SIE can transmit the written data.
- Can not be accessed by CPU/DMA.

○CPU side buffer:

- Can not be accessed by SIE.
- CPU/DMA can write the data for transmission.

○Buffer toggle condition (switching of SIE side buffer and CPU side buffer)

- CPU side buffer write completion and SIE side buffer transmit completion (empty)
  The write and transmit completion changes according to the single/continuous transmit/receive mode.
  For details, refer to the "EPi_RWMD bit".

Note: Refer to "3.2 FIFO Buffer" for CPU/SIE side.

(6) EPi_RWMD (Continuous Transmit/Receive Mode) Bit (b6)

This bit sets the transmit/receive mode at bulk transfer.
This bit can be set to "1" only when the transfer type is set to bulk transfer (EPi_TYP bits = "01").
Set to "0" for other transfer modes.

●When set to OUT buffer (EPi_DIR bit = "0")

In case of single transmit/receive mode, the receive completes after receiving one packet under the conditions as follows:

- Receives the data equivalent to the size set by the EPi_MXPS bits.
- Receives the short packet (including the zero-length packet).

In case of continuous transmit/receive mode, the receive completes after receiving several packets under the conditions as follows:

- Receives automatically the data equivalent to the size set by the EPi_MXPS bits several times and receives the data equivalent to the byte set by the EPi_Buf_siz bit.
- Receives the short packet (including the zero-length packet).
- When the value set by the DMAn_Transaction Count Register conforms to the packet receiving count.

●When set to IN buffer (EPi_DIR bit = "1")

In case of single transmit/receive mode, the transmit completes after transmitting one packet under the conditions as follows:

- Transmits the data equivalent to the size set by the EPi_MXPS bits or the zero-length packet.

In case of continuous transmit/receive mode, the transmit completes after transmitting several packets under the conditions as follows:

- Transmits automatically the data equivalent to the size set by the EPi_MXPS bits several times and transmits the data equivalent to the byte set by the EPi_Buf_siz bit.

In case of single transmit/receive mode, the write completes under the conditions as follows:

- Writes the data equivalent to the size set by the EPi_MXPS bits to the buffer (IVAL bit changed to "1").
- Writes "1" to the IVAL bit of the CPU_FIFO Control/Dn_FIFO Control Register.

In case of continuous transmit/receive mode, the write completes under the conditions as follows:

- Writes the data equivalent to the size set by the EPi_Buf_siz bit to the buffer (IVAL bit changed to "1").
- Writes "1" to the IVAL bit.

The set/clear conditions of the IVAL bit change according to this bit.

(7) EPi_Buf_Nmb (Buffer Start Number) Bits (b5~b0)

These bits set the beginning block number of the buffer.
The block number is a number by dividing the FIFO buffer into 64 byte sections (Note 1).
The domain set by the EPi_Buf_siz bit from the block set by these bits is secured as the buffer (Note 2).

Note 1: The M66291 is equipped with 3 Kbytes FIFO buffer and has the blocks from H'0 to H'2F.
Note 2: Make sure that several endpoints may not get overlapped in the same buffer area.

2.40 Epi Configuration Registers 1 (i=1~6)

■ EP1 Configuration Register 1 (EP1_1CONFIG) <Address : H'62>
■ EP2 Configuration Register 1 (EP2_1CONFIG) <Address : H'66>
■ EP3 Configuration Register 1 (EP3_1CONFIG) <Address : H'6A>
■ EP4 Configuration Register 1 (EP4_1CONFIG) <Address : H'6E>
■ EP5 Configuration Register 1 (EP5_1CONFIG) <Address : H'72>
■ EP6 Configuration Register 1 (EP6_1CONFIG) <Address : H'76>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
EPi_PID			EPi_NULMD	EPi_ACLR	EPi_Octl	EPi_MXPS									
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset : H'0040>
<S/W reset : ->
<USB bus reset : ->

b	Bit name	Function	R	W
15~14	EPi_PID Response PID	00 : NAK 01 : BUF (Transmits response PID/data according to the state of buffer etc,) 1x : STALL	○	○
13	Reserved. Set it to "0".		0	0
12	EPi_NULMD Zero-Length Packet Addtion Transmit Mode	0 : Disable to transmit zero-length packet automatically 1 : Enable to transmit zero-length packet automatically	○	○
11	EPi_ACLR OUT Buffer Automatic Clear Mode	0 : Exit buffer clear mode 1 : Buffer clear mode Make sure to set "0" after setting "1".	○	○
10	EPi_Octl Register 8-Bit Mode	0 : CPU/Dn_FIFO Data Register is 16-bit mode 1 : CPU/Dn_FIFO Data Register is 8-bit mode	○	○
9~0	EPi_MXPS Maximum Packet Size	Upper size limit of the data transmitted/received in one packet Interrupt transfer :0~64 Bulk transfer :only 8,16,32 and 64 Isochronous transfer :0~1023	○	○

(1) EPi_PID (Response PID) Bits (b15~b14)

These bits set the PID to be responded to the host.
These bits are valid only when the transfer type is set to bulk transfer mode or interrupt transfer mode (EPi_TYP bits = "01" or "10"). Set these bits to "01" at isochronous transfer mode (EPi_TYP bits = "11").
When these bits are set to "00", the NAK response is executed, regardless of the buffer state.

When these bits are set to "01";
<When set to OUT buffer (EPi_DIR bit = "0")>

- ACK response after receiving the data with the SIE side buffer in the receive ready state.
- NAK response with the SIE side buffer in the receive not ready state.
  When the SIE side buffer is not in receive ready state, if the OUT token is received, the EPB_NRD bit is set to "1".

<When set to IN buffer (EPi_DIR bit = "1")>

- Transmits the data with the SIE side buffer in transmit ready state.
- NAK response with the SIE side buffer not in the transmit ready state.
  When the SIE side buffer is in the transmit not ready state, if the IN token is received, the EPB_NRD bit is set to "1".

When these bits are set to "1x", the STALL response is executed, regardless of the buffer state.
When set to OUT buffer, if a data exceeding the maximum packet size is received, regardless of these bit values, these bits are set automatically to "1x" (STALL).

(2) EPi_NULMD (Zero-Length Packet Addtion Transmit Mode) Bit (b12)

This bit is valid at continuous transmit/receive mode (EPi_RWMD bit = "1") when set to IN buffer (EPi_DIR bit = "1"). Set to "0" for the other modes.

In case of the completion of SIE side buffer transmit, if the IVAL bit is set to "0", the zero-length packet automatically transmitted in the last under the condition as follows:

- When the buffer size set by the EPi_Buf_siz bit is the integral multiple of the size set by the EPi_MXPS bits.

In case of the continuous transmit/receive mode, the data equivalent to the size set by the EPi_MXPS bits is automatically transmitted several times before transmitting the data equivalent to the size set by the EPi_Buf_siz bit.

(3) EPi_ACLR (OUT Buffer Auto-Clear Mode) Bit (b11)

When set to OUT buffer (EPi_DIR bit = "0"), all buffers both of CPU and SIE sides are cleared by setting "1" to this bit.
This bit does not get automatically cleared to "0" even after the buffers are cleared.
When this bit is set to "1", if BUF is set to the EPi_PID bits, the NAK response is not executed against the received OUT token. Instead, the ACK response is sent to the host after receiving the data. The received data is not written to the buffer. Further, with the EPi_PID bits set to NAK/STALL, the NAK/STALL response is executed.

When set to IN buffer (EPi_DIR bit = "1"), only the SIE side buffer and the buffer with the writing completed (the buffer when IVAL bit = "1") are cleared by setting "1" to this bit.
When this bit is set to "1", if BUF is set to the EPi_PID bits, the NAK response is given against the received IN token. Further, with the EPi_PID bits set to NAK/STALL, the NAK/STALL response is executed.

Note: When set to IN buffer, make sure to set the response PID to NAK (EPi_PID bits = "00") before setting this bit to "1".

(5) EPi_Octl (Register 8-Bit Mode) Bit (b10)

This bit has the same function as the Octl bit of the CPU_FIFO Select Register or the Octl bit of the Dn_FIFO Select Register. Please refer to the items of these registers.

(6) EPi_MXPS (Maximum Packet Size) Bits (b9~b0)

These bits set the upper limit (byte count) of the data transmitted and received in one packet transfer.
Set the wMaxPacketSize value transmitted to the host.
In case of transmitting, the data equivalent to the size set by these bits is read out from the buffer for transmit. If the buffer does not have the data equivalent to the set by these bits, the data is transmitted as the short packet.
In case of receiving, the received data equivalent to the size set by these bits is written to the buffer. In case the received data exceeds the size set by these bits, the following bit is set to "1":

- The EPB_EMP_OVR bit
  (buffer empty/size-over error interrupt occurs when the EPB_EMPE bit is set to "1").

Note: Set this bit after setting the response PID to NAK (EPi_PID bits = "00").

3 M66291 OPERATIONS

3.1 Interrupt Function

There are 8 factors of interrupts in the M66291.
For details, refer to the “Interrupt Status Registers 0 to 3”.
The enable/disable of interrupt can be set by the Interrupt Enable Registers 0 to 3.
Each bit of the Interrupt Status Register is set to “1” according to the factor even if the Interrupt Enable Registers 0 to 3 are set to interrupt inhibit mode.
The list of interrupts in M66291 is given in Table 3.1 and the diagrams related to the interrupt in Figure 3.1.

Table 3.1 List of Interrupts

Status Bit (Interrupt Name)	Interrupt Factor	Related Item
VBUS (Vbus Interrupt)	Change of Vbus input level (change of "L"->"H", "H"->"L")	Confirmation of Vbus pin input state by the Vbus bit of the Interrupt Status Register 0
RESM (Resume Interrupt)	Change of USB bus state in suspend state ("J"->"K" or "SE0")	Confirmation of current device state by the DVSQ bits of the Interrupt Status Register 0
SOFR (SOF Detect Interrupt)	Receive of SOF packet	—
DVST (Device State Transition Interrupt)	• Detection of USB bus reset • Detection of suspend state • Execution of "SET_ADDRESS" • Execution of "SET_CONFIGURATION"	Confirmation of current device state by the DVSQ bits of the Interrupt Status Register 0
CTRT (Control Transfer Stage Transition Interrupt)	• Transition of control write transfer status stage • Transition of control read transfer status stage • Completion of control transfer • Occurrence of control transfer sequence error • Completion of setup stage	Confirmation of current control transfer stage state by the CTSQ bits of the Interrupt Status Register 0
BEMP (Buffer Empty / Size Over Interrupt)	• Transmit of all the data stored in the buffers at each endpoint • Receive of packet exceeding the maximum packet size during receiving data packet	Confirmation of endpoint number occurred the interrupt by the EPB_EMP_OVR bits of the Interrupt Status Register 3
INTN (Buffer Not Ready Interrupt)	When NAK response is automatically executed because of the buffer not ready state in the IN/OUT token of each endpoint	Confirmation of endpoint number occurred the interrupt by the EPB_NRDY bits of the Interrupt Status Register 2.
INTR (Buffer Ready Interrupt)	When each endpoint is buffer ready state (read /write enable state)	Confirmation of endpoint number of the occurred interrupt by the EPB_RDY bits of the Interrupt Status Register 1.

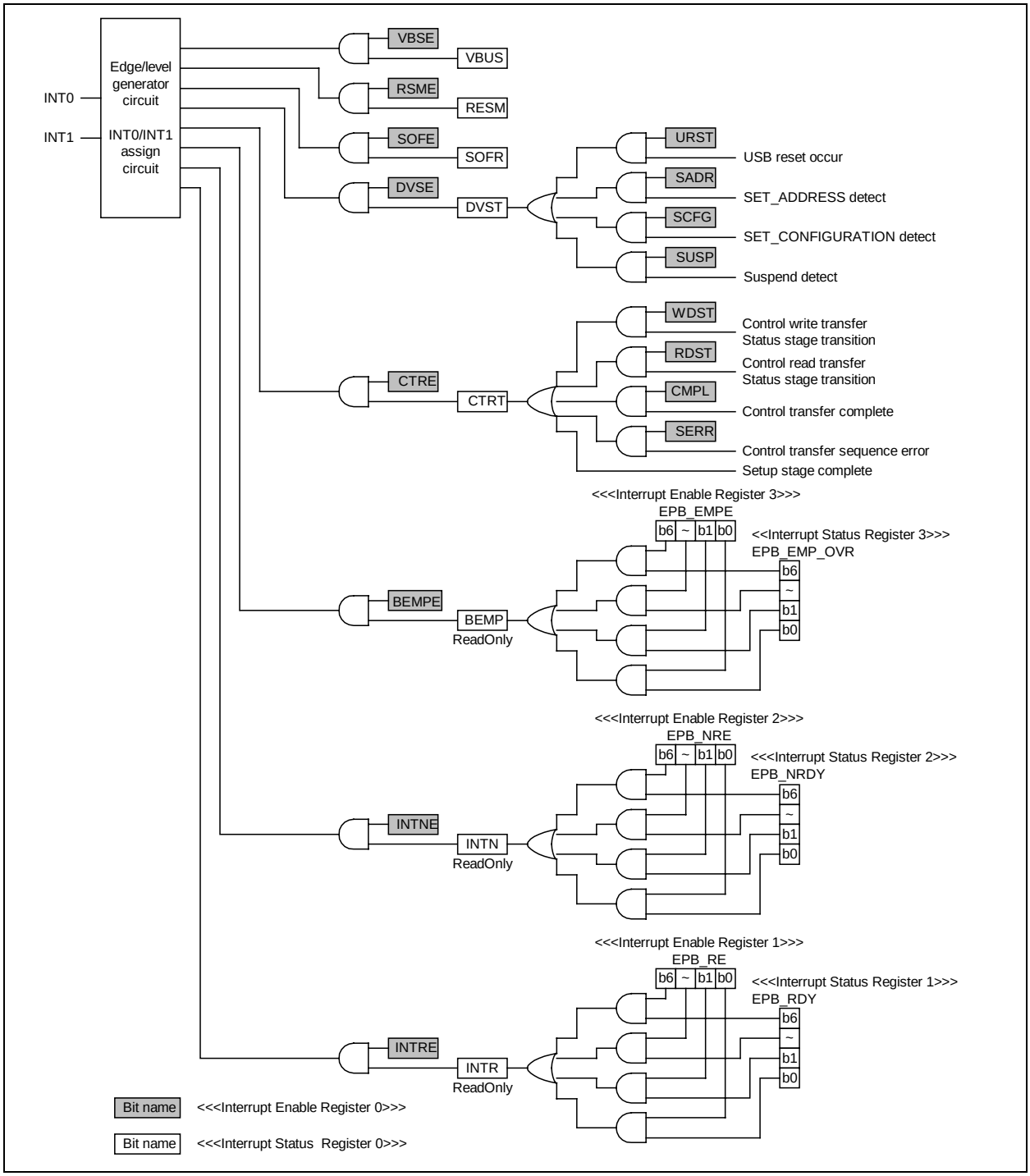


Figure 3.1 Interrupt Related Diagram

3.2 FIFO Buffer

The M66291 has 6 endpoints available for bulk/interrupt/isochronous transfers in addition to endpoint 0 for control transfer.

The M66291 is equipped with a total of 3 Kbytes FIFO that can be used as the buffer of the endpoint and can be assigned arbitrary byte count in 64-byte unit against each endpoint.

3.2.1 FIFO Buffer Configuration

The endpoint buffer can be set for double buffer configuration and continuous transmit/receive mode. Each buffer configuration is set by the registers as follows:

Endpoint 0:

- Control Transfer Control Register
- EP0 Packet Size Register
- EP0_FIFO Continuous Transmit Data Length Register

Endpoint 1~6:

- EPi Configuration Register 0
- EPi Configuration Register 1

3.2.2 Buffer Access

The buffers of endpoints 0 to 6 can be accessed by the four data registers as follows:

<EP0_FIFO Data Register>

- Quantity : 1 piece
- Exclusively used for endpoint 0

<CPU_FIFO Data Register >

- Quantity : 1 piece
- Shared with endpoints 1 to 6 (specified by the CPU_EP bits)

<Dn_FIFO Data Register >

- Quantity : 2 pieces
- Shared with endpoints 1 to 6 (specified by the DMA_EP bits)
- Can be accessed by DMAC

These four data registers can be set independently to 8-bit/16-bit mode by the Octl bit.

3.2.3 Buffer State and IVAL Bit

(1) Buffer state and IVAL bit of the OUT buffer

The relation between buffer state and IVAL bit is shown in Figure 3.2 when the buffer is set to OUT (set by the EPi_DIR bit/ISEL bit).
The single/double buffer mode is set by the EPi_DBLB bit. The double buffer mode cannot be set at endpoint 0.

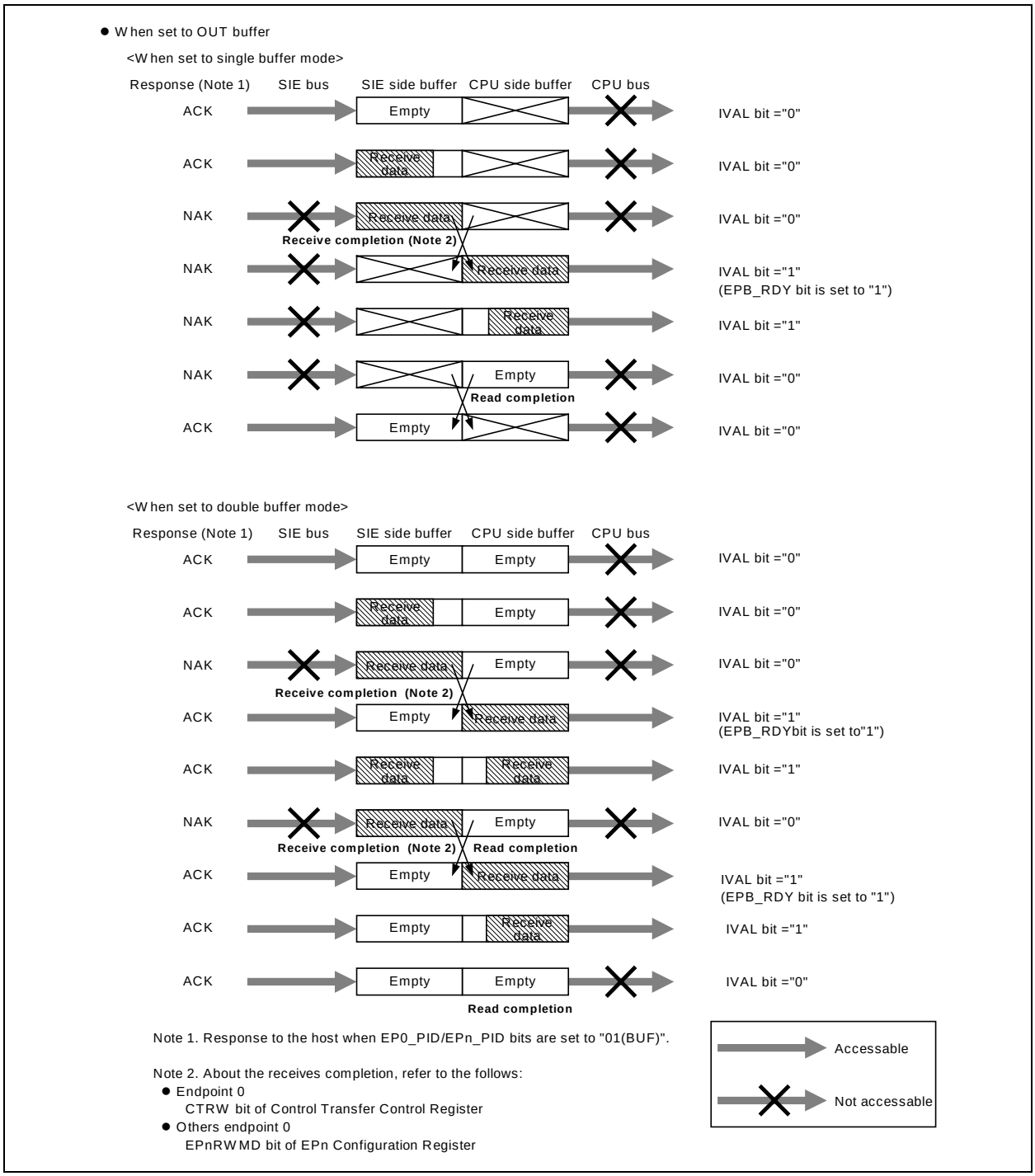


Figure 3.2 Relation between Buffer State and IVAL Bit (when set to OUT buffer)

(2) Buffer state and IVAL bit of the IN buffer

The relation between buffer state and IVAL bit is shown in Figure 3.3 when the buffer is set to IN (set by the EPi_DIR bit/ISEL bit).
The single/double buffer mode is set by the EPi_DBLB bit. The double buffer mode cannot be set at endpoint 0.

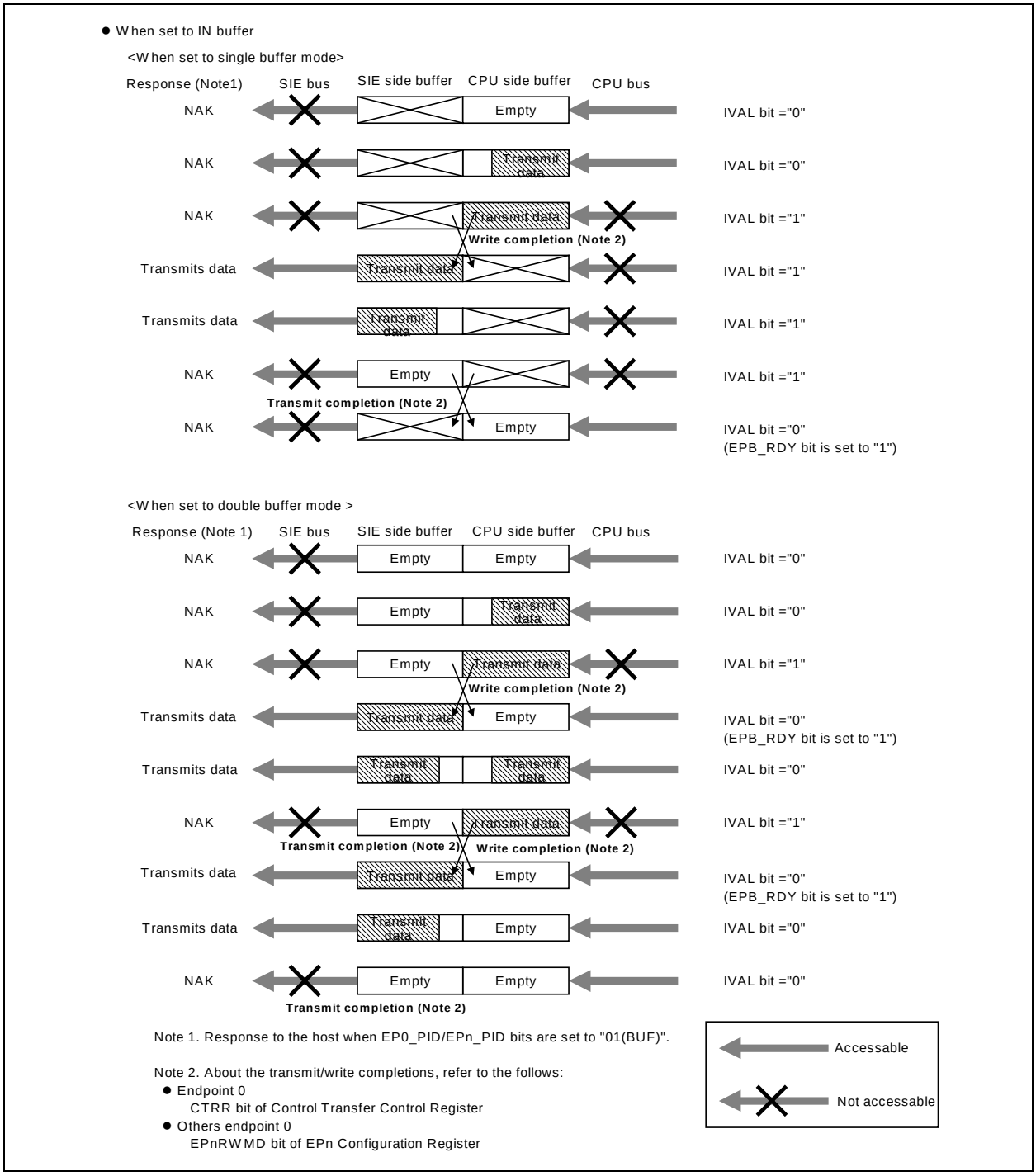


Figure 3.3 Relation between Buffer State and IVAL Bit (when set to IN buffer)

3.2.4 IVAL Bit and EPB_RDY Bit

The IVAL bit is available per endpoint.
These IVAL bits can be specified by the CPU_EP bits and the DMA_EP bits, and the read/write is possible by the IVAL bit of the CPU_FIFO Control Register and the IVAL bit of the Dn_FIFO Control Register.
The EPB_RDY bit can be set/cleared by the IVAL bit at each endpoint, irrespective of the aforesaid setting. Similarly, the EPB_NRDY bit and EPB_EMP_OVR bit can be set/cleared regardless of the CPU_EP bit/DMA_EP bit.
Make sure that the "1" setting to the EPB_RDY bit of the endpoint specified by the DMA_EP bit changes according to the setting of the INTM bit.

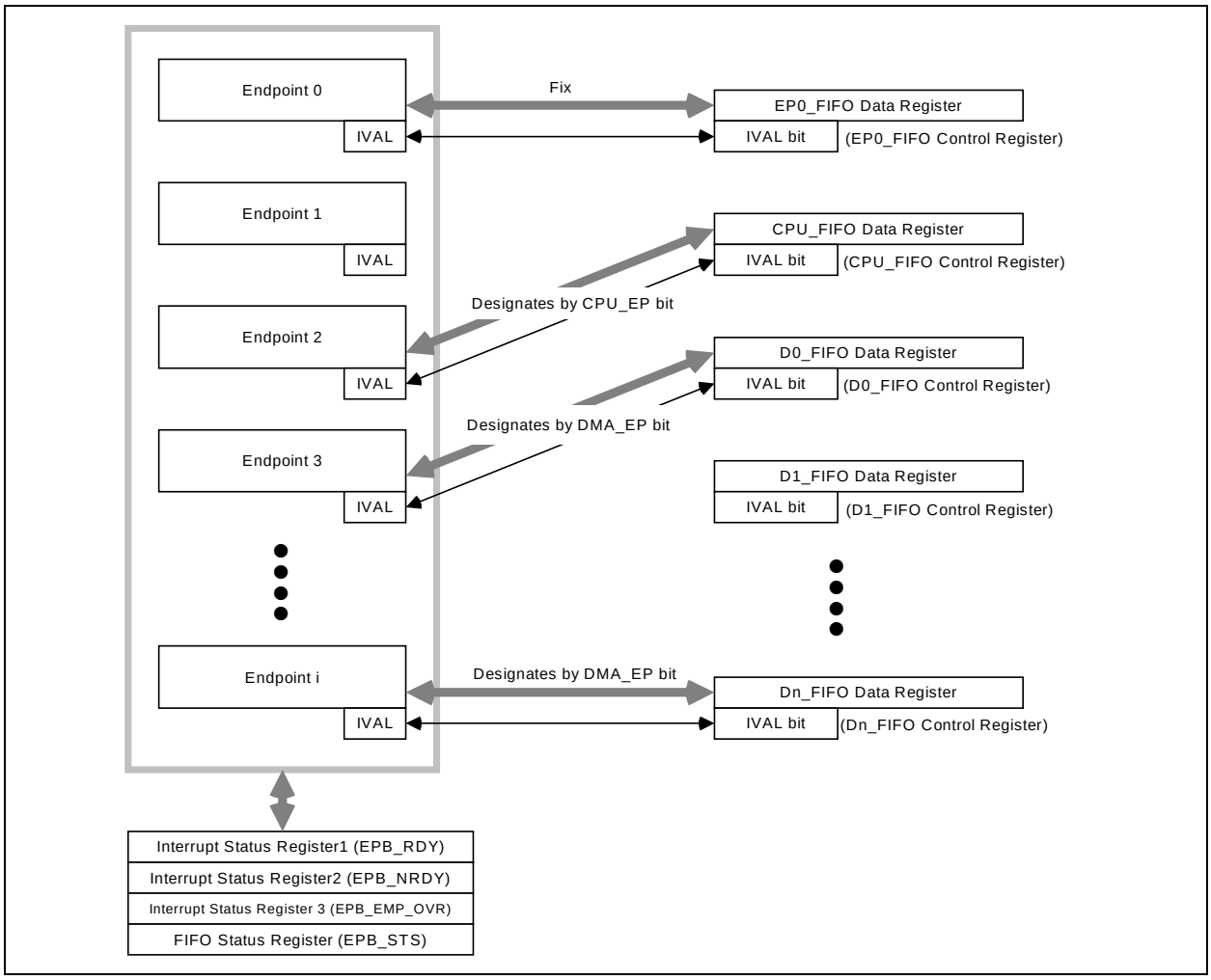


Figure 3.4 IVAL Bit and EPB_RDY Bit

3.3 USB Data Transfer Function Overview

The M66291 is capable of executing the USB transfer by processing the operations as follows:

(1) Response against the control transfer request
(2) Enable of transmitting after storing the transmit data to the buffer
Enable of receiving and reading the receive data from the buffer
(3) Stall processing
(4) Suspend/resume processing

3.3.1 Data Receive Function

The data receiving operation of the setup transaction and the OUT transaction differs as follows.

●Setup transaction (control transfer setup stage)
The device request data received from the host (8 bytes) are stored to 4 different registers.
Here, ACK response is executed to the host and the control transfer stage transition interrupt has occurred.

●OUT transaction
In the data packet after receiving OUT token from the host, when the buffer receives the packet of maximum size or the short packet, the ACK response is executed to the host and the buffer ready interrupt has occurred (ready for reading the receive data).
When the buffer is not in the receive ready state, the buffer not ready interrupt has occurred.

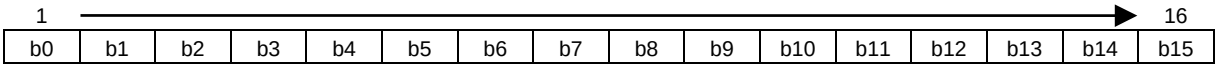
3.3.2 Data Transmit Function

The data transmit is executed on receiving the request for data transmit by the IN token packet.

●IN transaction
After the IN token is received from the host, the buffer data is transmitted. On completion of the buffer data transmit, the buffer ready interrupt has occurred (ready for writing the transmit data).
When the buffer is not in transmit ready state, the buffer not ready interrupt has occurred.

3.3.3 Data Transfer Sequence

The data written to the FIFO Data Register are transmitted to the USB bus in the order of LSB first. The same is true when the data received from the USB bus is stored to the FIFO Data Register.



3.3.4 DMA Transfer Overview

The M66291 is capable of DMA transfer in 16-bit/8-bit width (specified by the Octl bit) against the endpoint 1 to 6.
The DREQ pin is asserted when the endpoint buffer set to the Dn_FIFO Select Register is in read/write ready state. The output of DREQ pin is enabled by the DMAEN bit.
In order to write the data to transmit the short packet by the DMA_FIFO, assert the TC pin or set the IVAL bit to “1” after writing last data.
Further, when read by using DMA, the timing of the buffer ready interrupt occurrence can be changed by the INTM bit.

3.3.5 DMA Transfer Method

The DMA transfer method is set by the DFORM bit of the Dn_FIFO Control Register.

(1) Cycle Steal Mode (BUST bit = "0")

At cycle steal mode, the DREQ pin is asserted at every transfer (8-bit/16-bit).

(A-1) DMA transfer control by the DACK pin and read/write pins (DFORM bits = “00”):
At this mode, the DACK pin and read/write pins are used to access to the Dn_FIFO Data Register of the M66291.

(A-2) DMA transfer control solely by the DACK pin (DFORM bits = “01”):
At this mode, only the DACK pin is used to access to the Dn_FIFO Data Register of the M66291. The read/write pins are not used in this mode (are ignored).

(A-3) DMA transfer control by the chip select pin and the address pins (DFORM bits = “10”):
In this mode, the address pins and read/write pins are used to access the Dn_FIFO Data Register of the M66291. The DACK pin is not used in this mode (is ignored).

(2) Burst Mode (BUST bit = "1")

At burst mode, the DREQ pin is asserted until all data in the buffer has been transferred , and is negated when the transfer completes.

(B-1) DMA transfer control by the DACK pin and read/write pins (DEFORM bits = “00”):
This mode operates with the same timing as (A-1).

(B-2) DMA transfer control by the chip select pin and address pins (DEFORM bits = “10”):
This mode operates with the same timing as (A-3).

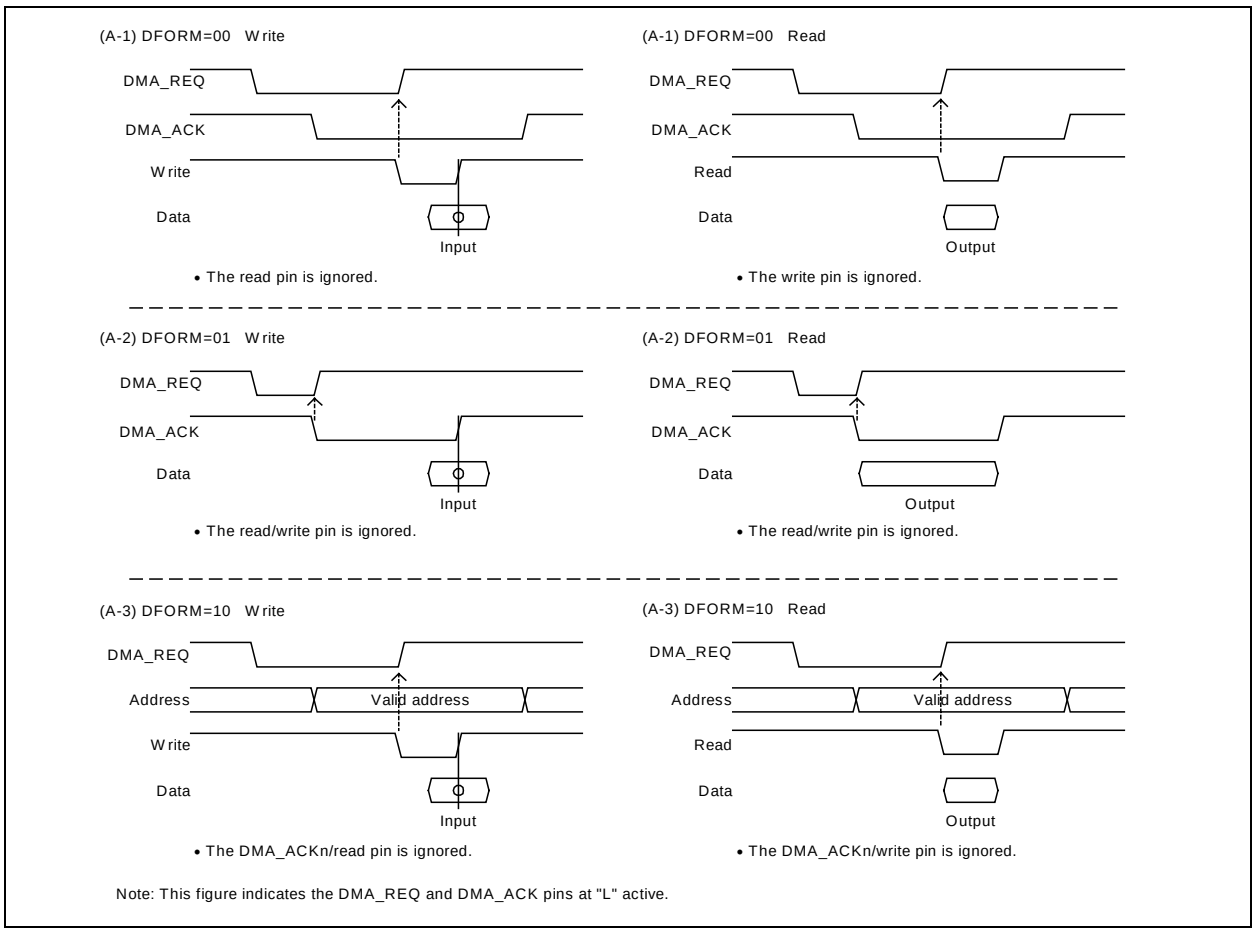


Figure 3.5 Access Timing at Cycle Steal Transfer

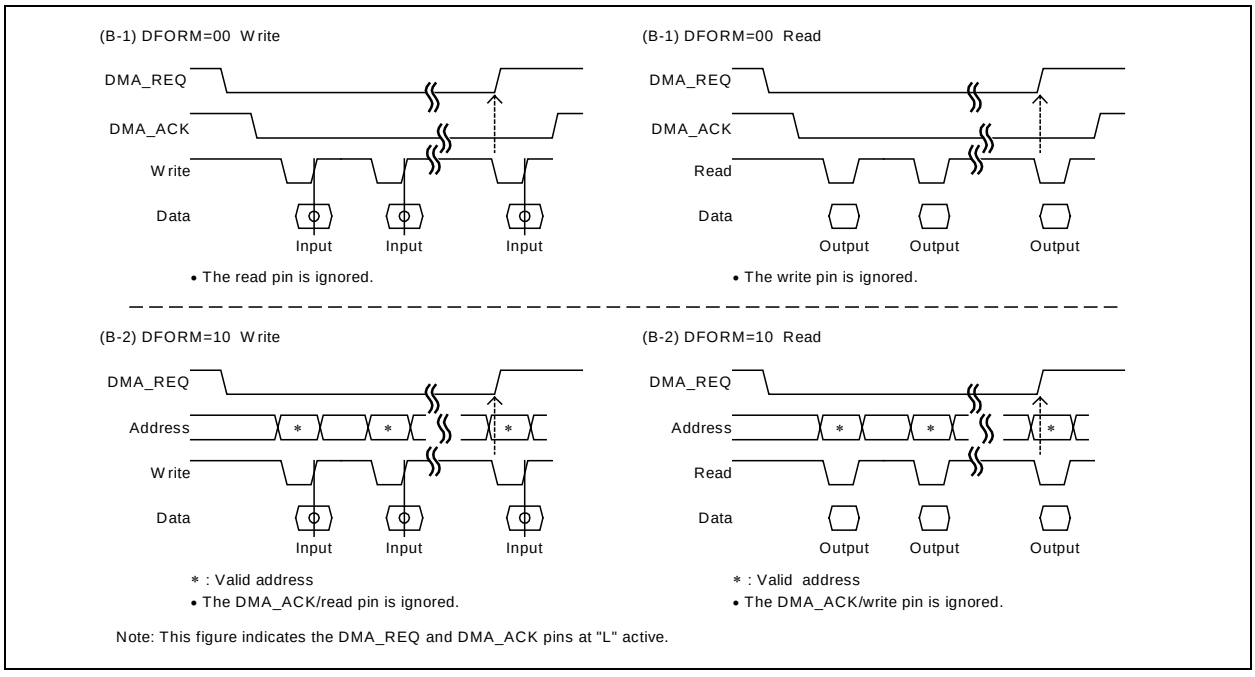


Figure 3.6 Access Timing at Burst Transfer

3.4 Control Transfer Overview

The control transfer is composed of three stages as follows:

(1) Setup stage
(2) Data stage (some control transfers don't include)
(3) Status stage

The M66291 automatically controls the stages of the control transfers by the hardware and is capable of generating interrupt against the aforesaid stage transition.

The control transfers are executed by the endpoint 0.

The examples of control write transfer, control read transfer, control write no data transfer, control transfer error and continuous setup operations are shown in Figure 3.7 to Figure 3.12.

(1) Setup stage

The transition to the setup stage occurs when the setup token is received.
The request data received at the setup stage (8 bytes) is automatically stored to four registers (Request, Value, Index and Length) before the ACK response is executed.
For SET_ADDRESS request and SET_CONFIGURATION request, the M66291 can respond automatically to the host. As for the other requests, execute data analysis (decoding) and processing by the software after the setup stage complete interrupt has occurred.

When the setup token is received, the VALID bit is set to “1”, the EP0_PID and CCPL bits are changed as shown below, then these bits are protected until the VALID bit is cleared:

- EP0_PID bits “00” : NAK response (response at data stage)
- CCPL bit “0” : NAK response (response at status stage)

(2) Data stage

The transition to the data stage occurs when the IN token/OUT token is received after the setup stage. In case of the request with no data stage, the transition to the status stage executes by receiving the OUT token after the setup stage.

- Control write transfer (OUT transaction)
  With the buffer set to receive ready state (buffer empty), the EP0_PID bits are set to “01” to make ACK response to the host after receiving the data.
  When the buffer is ready for data reading, the buffer ready interrupt occurs to enable reading of the receive data by the EP0_FIFO Data Register.
- Control read transfer (IN transaction)
  With the buffer set to transmit ready state (buffer contains transmit data), the data is transmitted to the host by setting the EP0_PID bits to “01”.
  When the buffer is ready to accept new transmit data, the buffer ready interrupt occurs.

(3) Status stage

The transition to the status stage occurs when IN token and OUT token are received after the data stage, causing the control write/read transfer status transition interrupt to occur. In this case, setting the EP0_PID bits to “01” and the CCPL bit to “1” enables to notify the normal completion to the host.
In the case of the request with no data stage, this interrupt works as the setup stage complete interrupt.

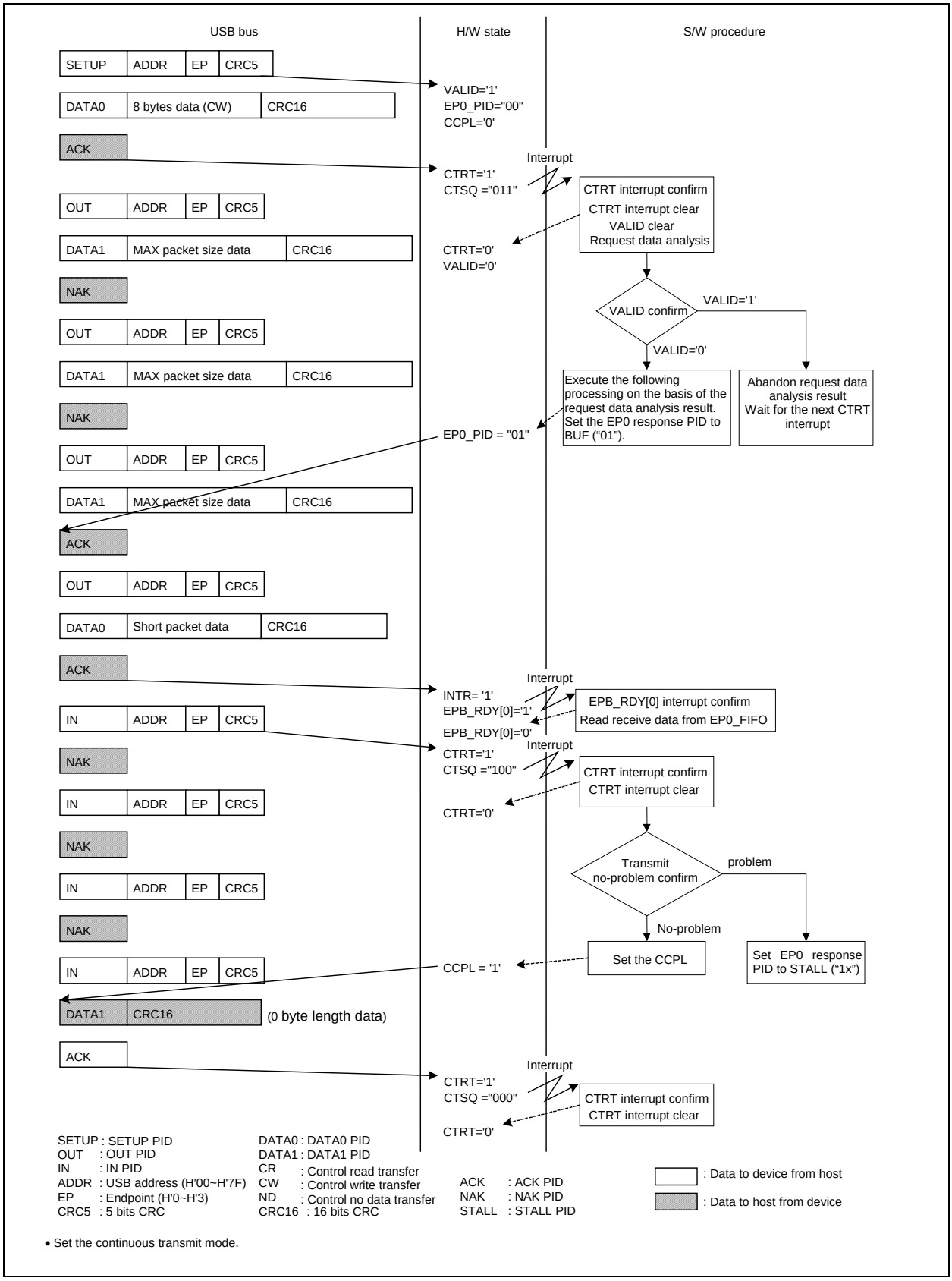


Figure 3.7 Examples of Control Write Transition Operations

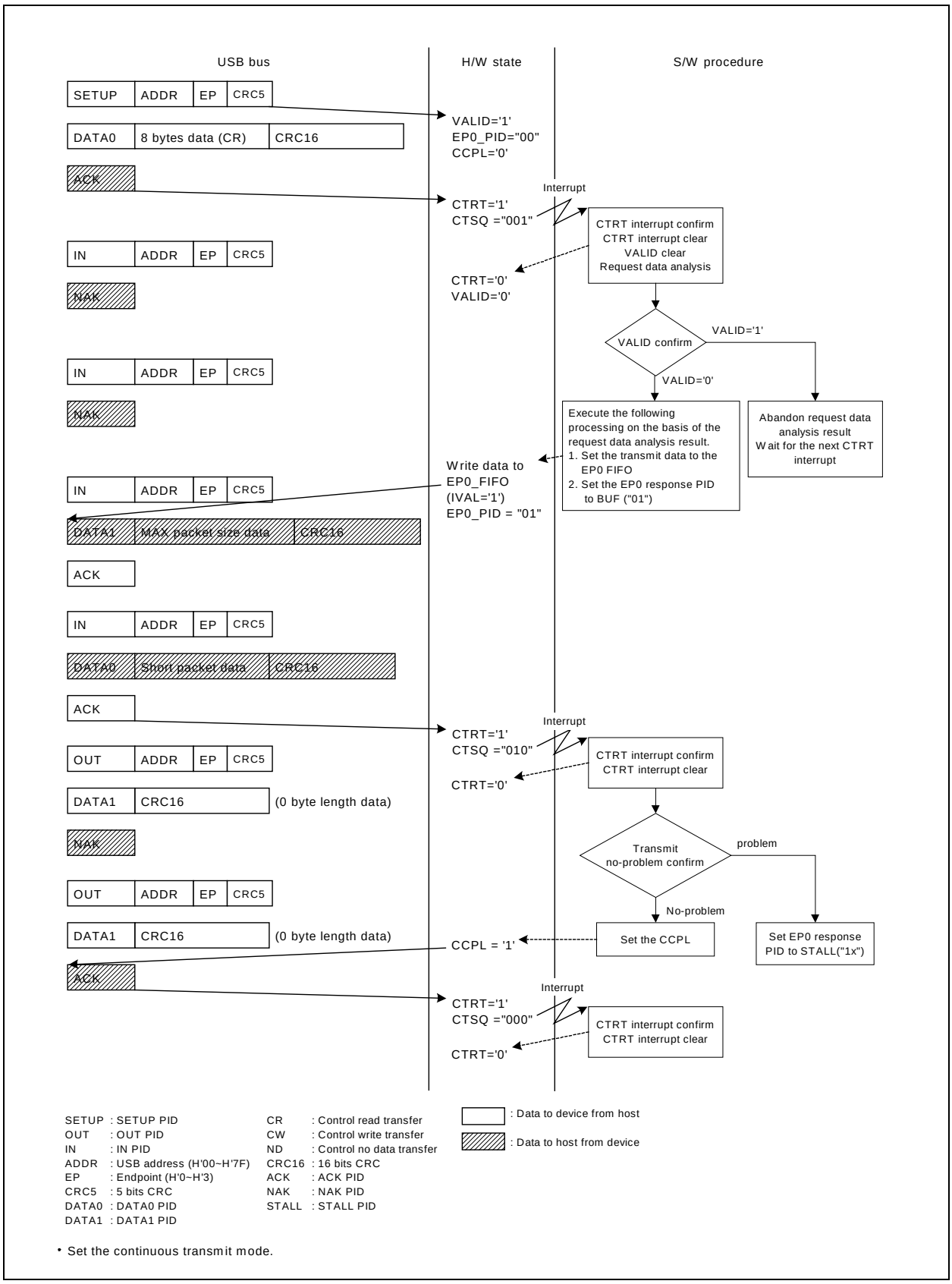


Figure 3.8 Examples of Control Read Transition Operations

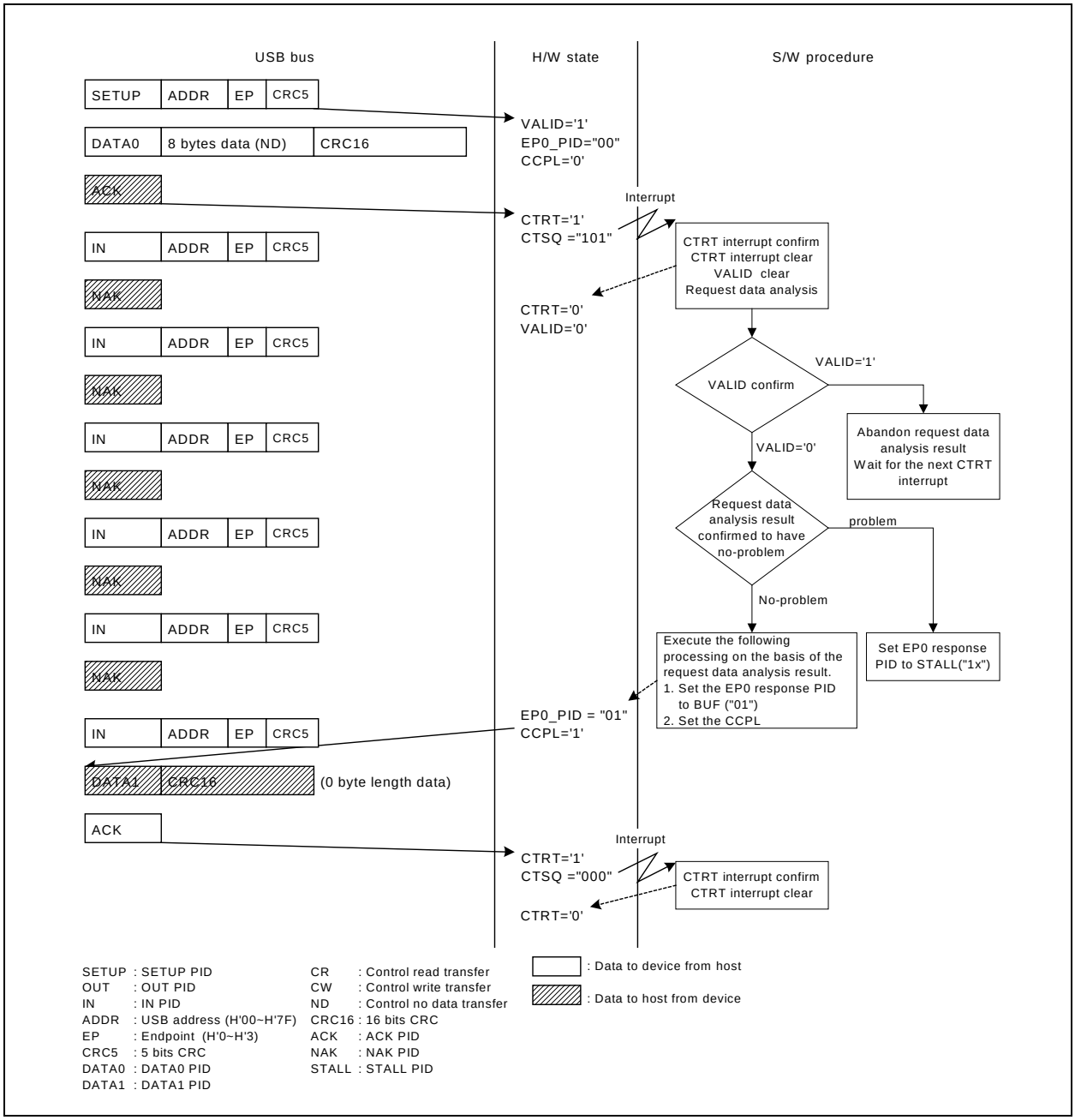


Figure 3.9 Examples of No Data Control Transition Operations

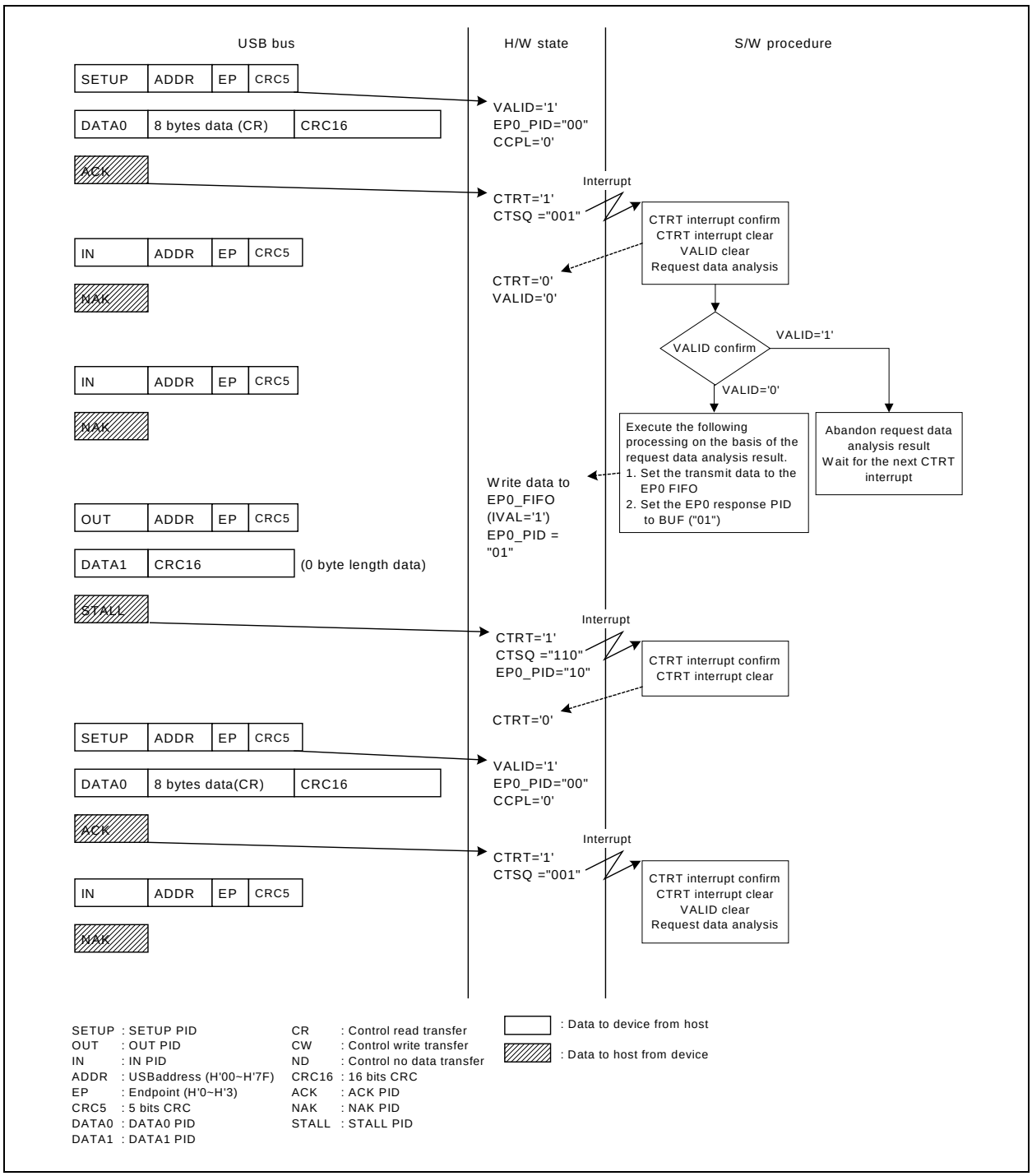


Figure 3.10 Examples of Control Transfer Error Operations

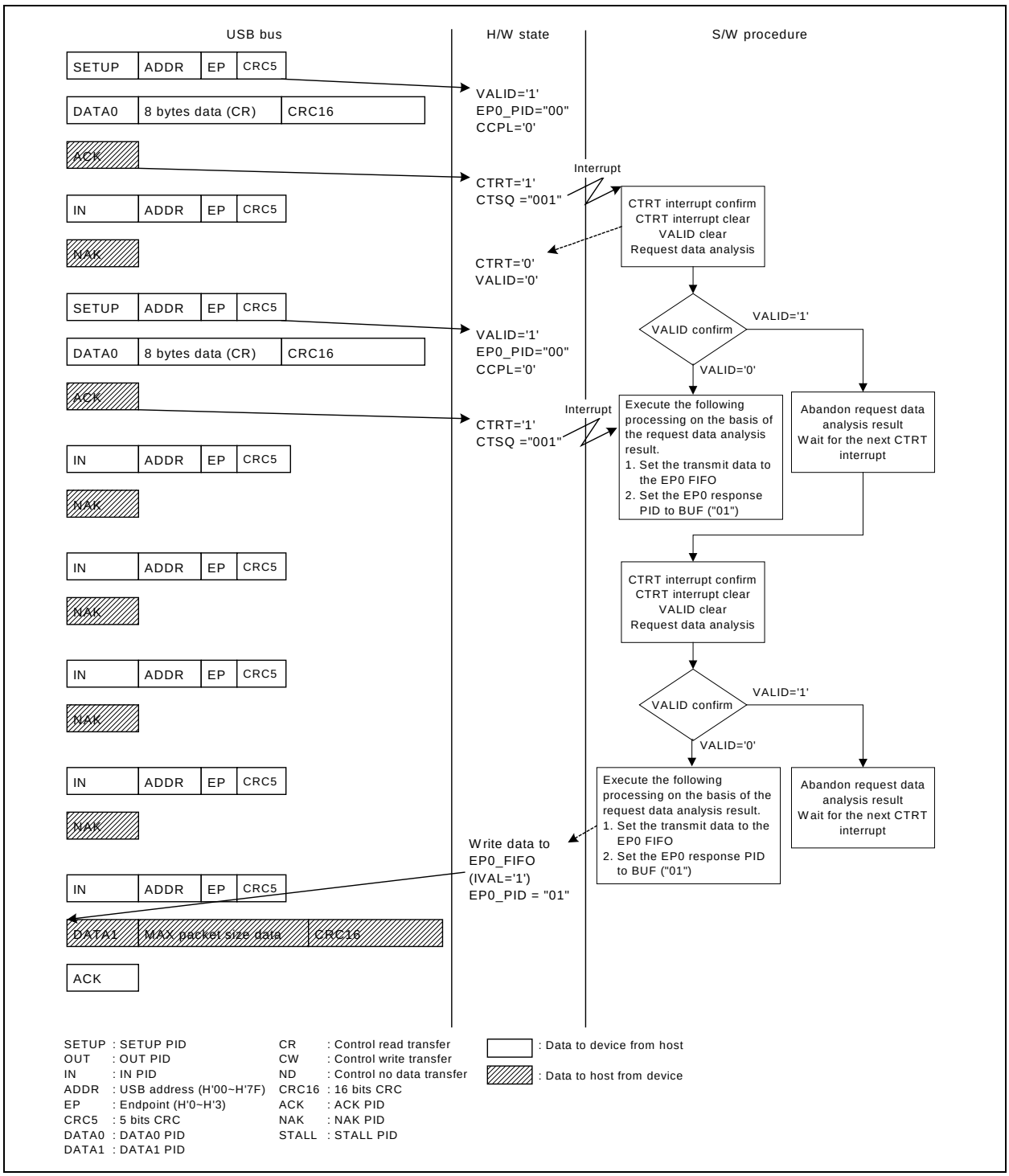


Figure 3.11 Examples of Setup Continuous Operations (1)

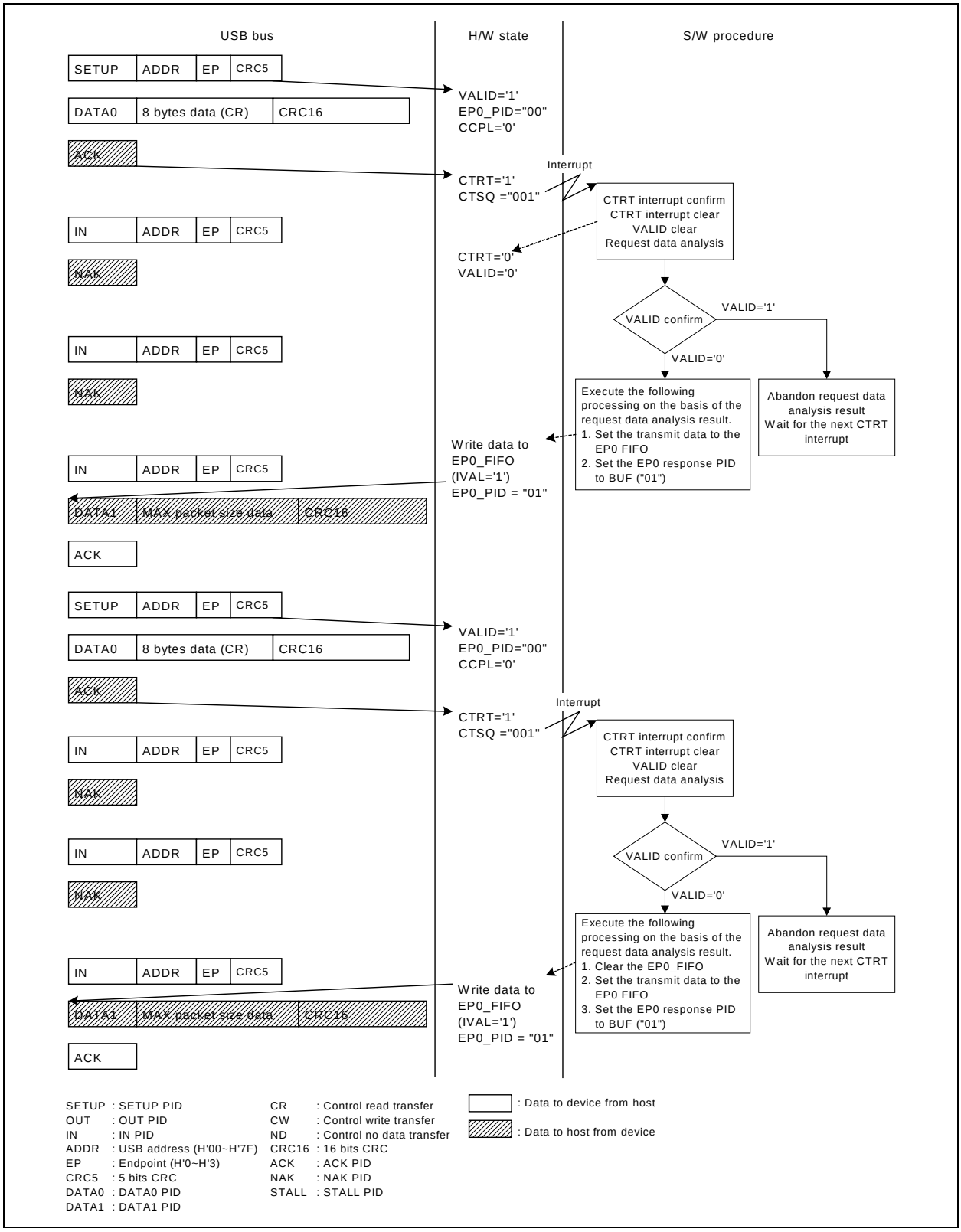


Figure 3.12 Examples of Setup Continuous Operations (2)

3.5 Enumeration

Figure 3.13 shows the overview of enumeration operations.

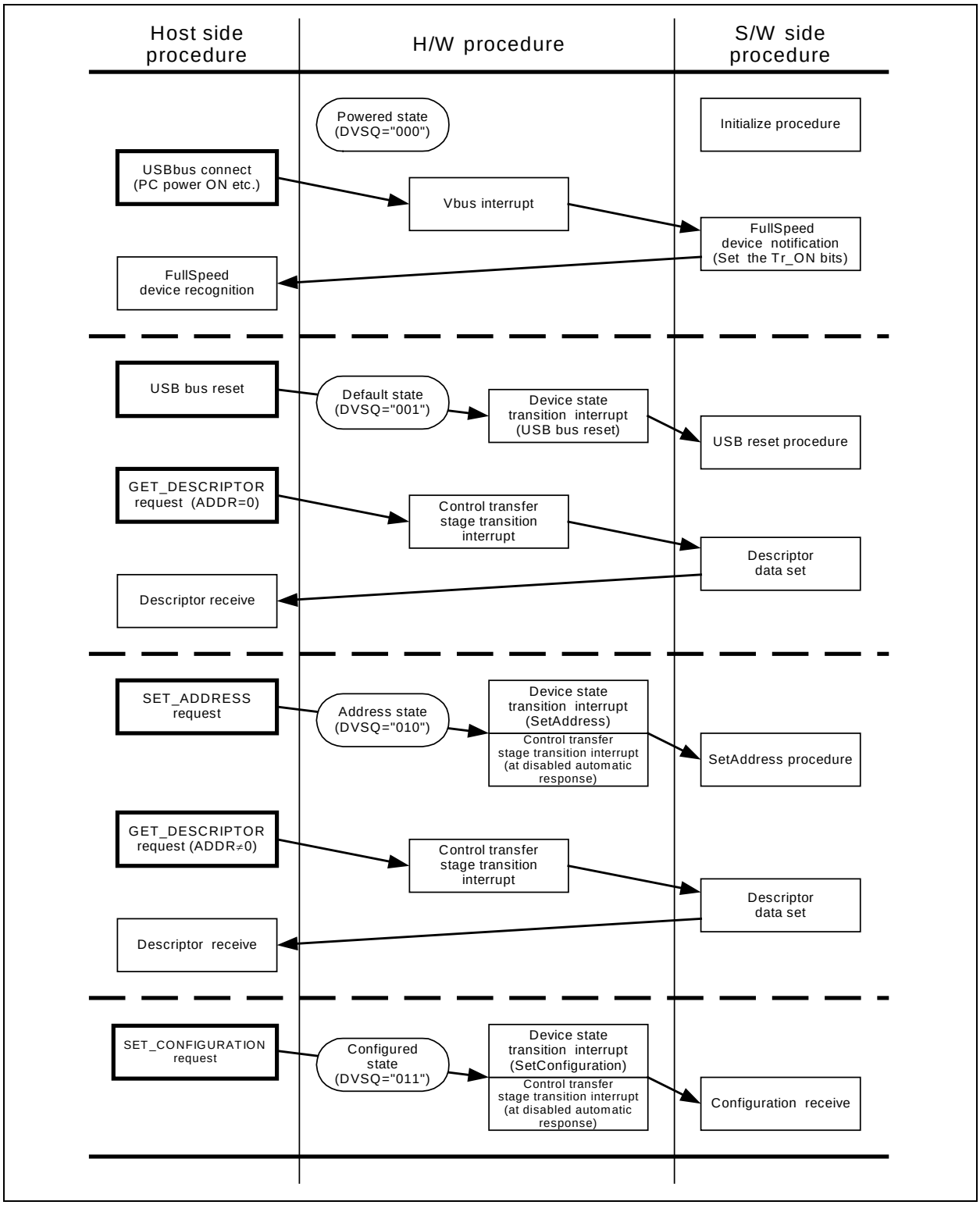


Figure 3.13 Overview of Bus · Enumeration Operations

3.5.1 FIFO Buffer Management

The M66291 is equipped with the registers below in order to execute high-level management of the FIFO buffer set to continuous transmit/receive mode.

(1) SIE_FIFO Status Register
This register can forcibly toggle the FIFO buffer at SIE side of double buffer, enabling the CPU to access to the SIE side FIFO. Further, the CPU can refer to the received data number in the SIE side FIFO.

(2) Transaction Count Register
When the continuous transfer mode buffer set in the OUT bulk transfer, the data receive count by MAX packet size is specified, enabling the transaction only for the set count. It is convenient for the DMA transfer.

(3) FIFO Status Register
This register is used for referring to the FIFO buffer status.

3.5.2 Cautions at FIFO Data Access

Make sure of the items as follows when accessing the FIFO Data Register.
When 8-bit width is selected in CPU interface:
The FIFO data can not be set to 16-bit mode by the register bit (Octl), while *LWR pin becomes valid as the write strobe at 8-bit mode.
When 16-bit width is selected in CPU interface:
The FIFO data can be set both to 16-bit and 8-bit modes by the register bit (Octl).

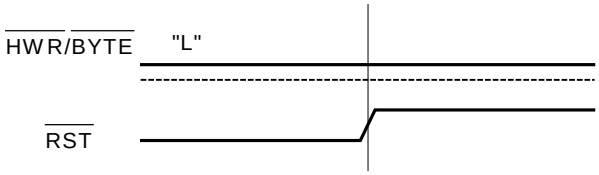
B-1) 16-bit mode (Octl bit =“0”)
When accessing data for write, assert *HWR and *LWR pins simultaneously for word access, and *LWR pin for byte access. At byte access, D7 to 0 become valid.

B-2) 8-bit mode (Octl bit =“1”)
When accessing data for write, *LWR pin is valid as the write strobe. Here, D7 to 0 become valid.
When accessing data for read, D15 to 8 and D7 to 0 are the same.

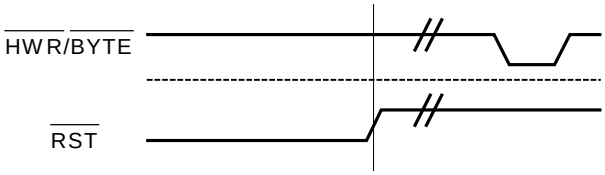
3.5.3 CPU Interface Bus Width Selection

The bus width is selected by the *HWR/*BYTE pin level at the rising of the *RST pin.
The 8-bit width is selected when *HWR/*BYTE pin is “L” level and 16-bit when it is “H” level.
With the 8-bit width selected, fix the *HWR/*BYTE pin to “L”.

When select to 8-bit bus width



When select to 16-bit bus width



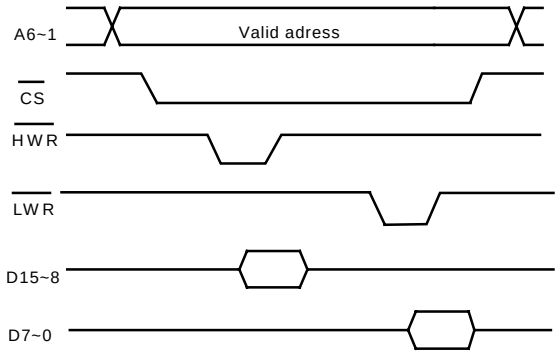
3.5.4 Combination of CPU Interface Input Pins

CPU Interface	*CS	*HWR	*LWR	*RD	Valid address	D15-8	D7-0	Remarks
8-bit width	L	L	L	H	A6-0	Note 1	Data input	Writes the lower byte
	L	L	H	L	A6-0	Note 1	Data output	Reads the lower byte
	H	X	X	X	A6-0	Note 1	Hi-Z	
16-bit width	L	L	H	H	A6-1	Data input	Hi-Z	Writes the upper byte
	L	H	L	H	A6-1	Hi-Z	Data input	Writes the lower byte
	L	L	L	H	A6-1	Data input	Data input	Writes the upper and lower bytes
	L	H	H	L	A6-1	Data output	Data output	Reads the upper and lower bytes
	H	X	X	X	A6-1	Hi-Z	Hi-Z	

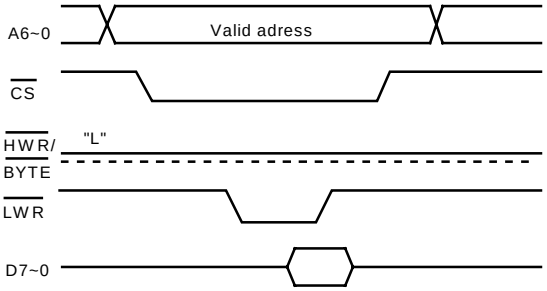
X : Don’t care
Hi-Z : High impedance
Note 1: The D15/A0 become input pins, while the others depend on the ports setting.
Note 2: The above figure is not applicable when accessing to the FIFO Data Register.

3.5.5 Register Data Access

(1) Writing when CPU interface 16-bit width is selected
When 16-bit width is selected, A6 to 1 becomes valid.
Further, *HWR pin becomes valid as the write strobe for D15 to 8 while *LWR pin for D7 to 0 at the time of data writing.



(2) Writing when CPU interface 8-bit width is selected
When 8-bit width is selected, A6 to 0 becomes valid.
Further, *LWR pin becomes valid as the write strobe at the time of data writing. Here, fix the *HWR/*BYTE pin to "L" level.



Note: The above figures are not applicable when accessing the FIFO Data Register.

3.5.6 Clock

48 MHz clock is needed for the internal operation of the M66291.
A built-in PLL enables an external clock of 6, 12, 24, or 48 MHz to be input. Selection is realized by XTAL bit of the USB Operation Enable Register. When an external 48 MHz clock is used, the PLL is not needed, so the PLL operation should be disabled.
A built-in oscillation buffer enables the device to be clocked from a crystal unit.

The device is set to standby state by the USB Operation Enable Register. Oscillation is halted (clock input halted) by XCKE bit, PLL is halted by PLLC bit, and clock supply to the USB block is halted by SCKE bit.
To prevent unstable behavior, clock supply to USB block must be applied as follow:
a. Enables clock input by the XCKE,
b. Wait until oscillation stabilizes,
c. Start PLL by the PLLC bit,
d. Wait until PLL oscillation stabilizes (less than 1ms),
e. then start clock supply to USB block by the SCKE bit.

4 ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
CoreVcc	USB Core supply voltage	-0.3 ~ +4.2	V
IOVcc	System interface supply voltage	-0.3 ~ +6.5	V
Vbus	Vbus input voltage	-0.3 ~ +5.5	V
VI(IO)	System interface input voltage	-0.3 ~ IOVcc+0.3	V
VO(IO)	System interface output voltage	-0.3 ~ IOVcc+0.3	V
Pd	Power dissipation	400	mW
Ts t g	Storage temperature	-55 ~ +150	°C

4.2 Recommended Operating Conditions

Symbol	Parameter		Ratings			Unit
			Min.	Typ.	Max.	
CoreVcc	USB Core supply voltage	To p r = 0 ~ +70 °C	3.0	3.3	3.6	V
		To p r = -20 ~ +85 °C	3.15	3.3	3.45	V
IOVcc	System interface supply voltage	5V	4.5	5.0	5.5	V
		3V	2.7	3.3	3.6	V
GND	Supply voltage			0		V
VI(IO)	System interface input voltage		0		IOVcc	V
VI(Vbus)	Input voltage (only Vbus input)		0		5.25	V
VO(IO)	System interface output voltage		0		IOVcc	V
To p r	Operating temperature	USB transfer state	0	+25	+70	°C
		Not USB transfer state	-20	+25	+85	°C
tr, tf	Input rise, fall time	Normal input			500	ns
		Schmidt trigger input			5	ms

4.3 Electrical Characteristics (IOVcc=2.7~3.6V,CoreVcc=3.0~3.6V)

Symbol	Parameter		Condition		Limits			Unit
					Min.	Typ.	Max.	
VIH	"H" input voltage	Xin	CoreVcc = 3.6V		2.52		3.6	V
VIL	"L" input voltage		CoreVcc = 3.0V		0		0.9	V
VIH	"H" input voltage	Note1	IOVcc = 3.6V		0.7IOVcc		3.6	V
VIL	"L" input voltage		IOVcc = 2.7V		0		0.3IOVcc	V
VT+	Threshold voltage in positive direction	Note 2	IOVcc = 3.3V		1.4		2.4	V
VT-	Threshold voltage in negative direction				0.5		1.65	V
VTH	Hysteresis voltage					0.8		V
VO H	"H" output voltage	Xout	CoreVcc = 3.0V	IOH = -50uA	2.6			V
VO L	"L" output voltage			IOL = 50uA			0.4	V
VO H	"H" output voltage	Note 3	IOVcc = 2.7V	IOH = -2mA	IOVcc-0.4			V
VO L	"L" output voltage			IOL = 2mA			0.4	V
VO H	"H" output voltage	Note 4	IOVcc = 2.7V	IOH = -4mA	IOVcc-0.4			V
VO L	"L" output voltage			IOL = 4mA			0.4	V
VT+	Threshold voltage in positive direction	Note 5	CoreVcc=3.3V		1.4		2.4	V
VT-	Threshold voltage in negative direction				0.5		1.65	V
II H	"H" input current		IOVcc = 3.6V	VI = IOVcc			10	uA
II L	"L" input current			VI = GND			-10	uA
IOZH	"H" output current in off status	D	IOVcc = 3.6V	VO = IOVcc			10	uA
IOZL	"L" output current in off status	15-0		VO = GND			-10	uA
Rd v	Pull down resistance	Note 5				500		kΩ
Rd t	Pull down resistance	Note 6				50		kΩ
Icc(A)	Average supply current in operation mode	Note 7	f(Xin)=48MHz,IOVcc=3.6V, CoreVcc=3.6V,USB transmit state			15	30	mA
Icc(S)	Supply current in static mode	Note 7	Oscillator disable, PLL disable, USB transceiver enable, TrON=H/L output *CS,*HWR/*BYTE,*LWR, *Dack0,*Dack1=IOVcc, D15-0=0 ~ IOVcc, Other input VI=IOVcc or GND IOVcc = 3.6V,CoreVcc=3.6V Vbus=5.0V, suspend state			30	200	uA
Icc(S)	Supply current in static mode	Note 7	Oscillator disable, PLL disable, USB transceiver enable, TrON=Hi-Z *CS,*HWR/*BYTE,*LWR, *Dack0,*Dack1=IOVcc, D15-0=0 ~ IOVcc, Other input VI=IOVcc or GND IOVcc = 3.6V,CoreVcc=3.6V Vbus=GND, H/W reset state			10	100	uA

Note 1: A6-1, TEST input pins and D15-0 input/output pins
Note 2: *CS, *RD, *LWR, *HWR/*BYTE, *Dack0, *Dack1, *TC1, *RST input pins
Note 3: *INT0, *Dreq0, *Dreq1 output pins
Note 4: D15-0 input/output pins, *INT1/SOF output pins
Note 5: Vbus input pin
Note 6: TEST input pin
Note 7: The supply current is the total of IOVcc, CoreVcc.

4.4 Electrical Characteristics (IOVcc=4.5~5.5V,CoreVcc=3.0~3.6V)

Symbol	Parameter		Condition		Limits			Unit
					Min.	Typ.	Max.	
VIH	"H" input voltage	Xin	CoreVcc = 3.6V		2.52		3.6	V
VIL	"L" input voltage		CoreVcc = 3.0V		0		0.9	V
VIH	"H" input voltage	Note 1	IOVcc = 5.5V		0.7IOVcc		5.5	V
VIL	"L" input voltage		IOVcc = 4.5V		0		0.3IOVcc	V
VT+	Threshold voltage in positive direction	Note 2	IOVcc = 5.0V		2.3		3.7	V
VT-	Threshold voltage in negative direction				1.25		2.3	V
VTH	Hysteresis voltage					0.8		V
VO H	"H" output voltage	Xout	CoreVcc = 3.0V	IOH = -50uA	2.6			V
VO L	"L" output voltage			IOL = 50uA			0.4	V
VO H	"H" output voltage	Note 3	IOVcc = 4.5V	IOH = -2mA	4.1			V
VO L	"L" output voltage			IOL = 2mA			0.4	V
VO H	"H" output voltage	Note 4	IOVcc = 4.5V	IOH = -4mA	4.1			V
VO L	"L" output voltage			IOL = 4mA			0.4	V
VT+	Threshold voltage in positive direction	Note 5	CoreVcc=3.3V		1.4		2.4	V
VT-	Threshold voltage in negative direction				0.5		1.65	V
II H	"H" input current		IOVcc = 5.5V	Vi= IOVcc			10	uA
II L	"L" input current			Vi = GND			-10	uA
IOZH	"H" output current in off status	D	IOVcc = 5.5V	Vo = IOVcc			10	uA
IOZL	"L" output current in off status	15-0		Vo = GND			-10	uA
Rd v	Pull down resistance	Note 5				500		kΩ
Rd t	Pull down resistance	Note 6				50		kΩ
Icc(A)	Average supply current in operation mode	Note 7	f(Xin)=48MHz,IOVcc=5.5V, CoreVcc=3.6V,USB transmit state			15	30	mA
Icc(S)	Supply current in static mode	Note 7	Oscillator disable, PLL disable, USB transceiver enable, TrON=H/L output *CS,*HWR/*BYTE,*LWR, *Dack0,*Dack1=IOVcc, D15-0=0 ~ IOVcc, Other input VI=IOVcc or GND IOVcc = 5.5V,CoreVcc=3.6V Vbus=5.0V, suspend state			30	200	uA
Icc(S)	Supply current in static mode	Note 7	Oscillator disable, PLL disable, USB transceiver enable, TrON=Hi-Z *CS,*HWR/*BYTE, *LWR, *Dack0,*Dack1=IOVcc, D15-0=0 ~ IOVcc, Other input VI=IOVcc or GND IOVcc = 5.5V,CoreVcc=3.6V Vbus=GND,H/W reset state			10	100	uA

Note 1: A6-1, TEST input pins and D15-0 input/output pins
Note 2: *CS, *RD, *LWR, *HWR/*BYTE, *Dack0, *Dack1, *TC1, *RST input pins
Note 3: *INT0, *Dreq0, *Dreq1 output pins
Note 4: D15-0 input/output pins, *INT1/SOF output pins
Note 5: Vbus input pin
Note 6: TEST input pin
Note 7: The supply current is the total of IOVcc, CoreVcc.

4.5 Electrical Characteristics (D+/D-)

4.5.1 DC Characteristics

Symbol	Parameter	Test condition		Limits			Unit
				Min.	Typ.	Max.	
VDI	Differential input sensitivity	|(D+)-(D-)|		0.2			V
VCM	Differential common mode range			0.8		2.5	V
VSE	Single ended receiver threshold			0.8		2.0	V
VOL	"L" output voltage	CoreVcc = 3.0V	RL of 1.5KΩ to 3.6V			0.3	V
VOH	"H" output voltage		RL of 1.5KΩ to GND	2.8		3.6	V
IOZL	"L" output current in off status	CoreVcc = 3.6V	VO =0V	-10		10	uA
IOZH	"H" output current in off status		VO =3.6V	-10		10	uA
Ro(Pch)	Output impedance	CoreVcc = 3.3V	VO =0V	4	7	15	Ω
Ro(Nch)	Output impedance		VO =3.3V	4	7	15	Ω

4.5.2 AC Characteristics

Symbol	Parameter	Test condition		Limits			Unit
				Min.	Typ.	Max.	
tr	Rise transition time	10% to 90% of the data signal : amplitude	CL=50pF	4		20	ns
tf	Fall transition time	90% to 10% of the data signal : amplitude	CL=50pF	4		20	ns
TRFM	Rise/fall time matching	tr/tf		90		110	%
VCRS	Output signal crossover voltage	CL=50pF		1.3		2.0	V

4.6 Switching Characteristics (IOVcc=2.7~3.6V or 4.5~5.5V)

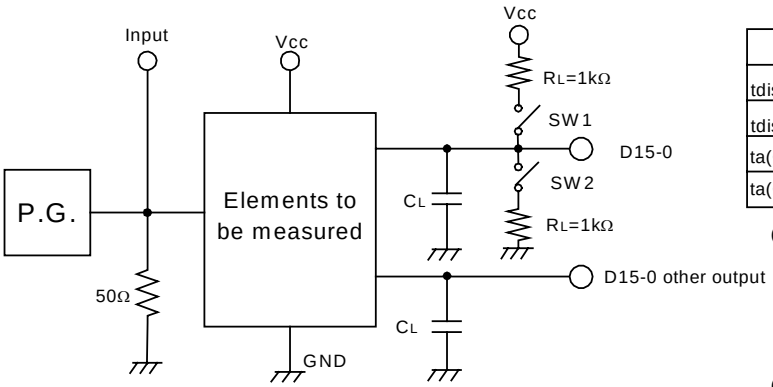
Symbol	Parameter	Test conditions	Limits			Unit	Refer No.
			Min.	Typ.	Max.		
ta(A)	Address access time	CL=50pF			40	ns	1
tv(A)	Data valid time after address		0			ns	2
ta(CTRL)	Control access time				30	ns	3
tv(CTRL)	Data valid time after control		0			ns	4
ten(CTRL)	Control output enable time		0		20	ns	5
tdis(CTRL)	Output disable time after control		0		20	ns	6
tdis(CTRL-Dreq)	Dreq disable time after control				50	ns	7
tdis(Dack -Dreq)	Dreq disable time after Dack				50	ns	8
ta(Dack)	Dack access time				30	ns	9
ten(Dack)	Output enable time after Dack		0		20	ns	10
tv(Dack)	Data valid time after Dack		0			ns	11
tdis(Dack)	Output disable time after Dack		0		20	ns	12
tdis(CTRLH -Dreq)	Dreq disable time after control				50	ns	13
td(CTRL-INT)	INT negate delay time				250	ns	14
twh(INT)	INT "H" pulse width		650			ns	15
twh(Dreq)	Dreq "H" pulse width		50			ns	16
ten(Dack -Dreq)	Dreq enable time after Dack		30			ns	17
ten(CTRL-Dreq)	Dreq enable time after control		50			ns	18

4.7 Timing Requirements (IOVcc=2.7~3.6V or 4.5~5.5V)

Symbol	Parameter	Test conditions	Limits			Unit	Refer
			Min.	Typ.	Max.		No.
tsuw(A)	Address write setup time		30			ns	㉚
tsur(A)	Address read setup time		0			ns	㉛
thw(A)	Address write hold time		0			ns	㉜
thr(A)	Address read hold time		30			ns	㉝
tw(CTRL)	Control pulse width (Write)		30			ns	㉞
trec(CTRL)	Control recovery time (FIFO)		30			ns	㉟
trecr(CTRL)	Control recovery time (REG)		15			ns	㊱
tw(Dack)	Dack pulse width		30			ns	㊲
tsu(D)	Data setup time		20			ns	㊳
th(D)	Data hold time		0			ns	㊴
tw(cycle)	FIFO access cycle time		100			ns	㊵
tsud(A)	DMA address setup time		15			ns	㊶
thd(A)	DMA address hold time		0			ns	㊷
tw(RST)	Reset pulse width		100			ns	㊸
tst(RST)	Control start time after RESET		500			ns	㊹
tsu(BYTE)	Byte mode setup time		250			ns	㊺
th(BYTE)	Byte mode hold time		250			ns	㊻
twr(CTRL)	Control pulse width (Read)		50			ns	㊼
td1(Dack-TC)	TC delay time 1		0			ns	㊽
td2(Dack-TC)	TC delay time 2				30	ns	㊾

4.8 Measurement circuit

4.8.1 Pins except for USB buffer block

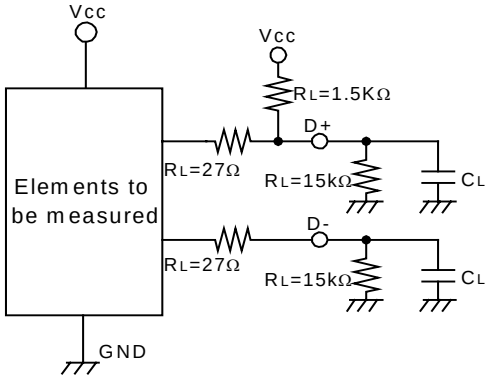


Item	SW1	SW2
tdis(CTRL(LZ))	close	open
tdis(CTRL(HZ))	open	close
ta(CTRL(ZL))	close	open
ta(CTRL(ZH))	open	close

(1) Input pulse level : 0 ~ 3.3V, 0 ~ 5.0V
Input pulse rise/fall time : tr,tf=3ns
Input timing standard voltage : IOVcc/2
Output timing judge voltage : IOVcc/2
(The tdis (LZ) is judged by 10% of the output amplitude and the tdis (HZ) by 90% of the output amplitude.)

(2) The electrostatic capacity CL includes the stray capacitance of the wire connection and the input capacitance of the probe.

4.8.2 USB buffer block



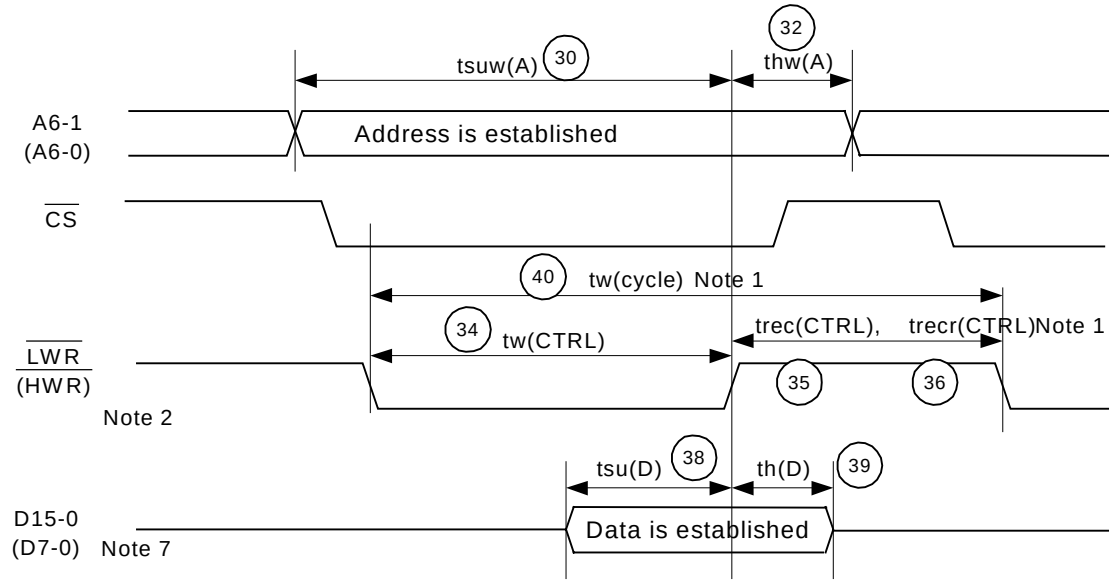
(1) The tr and tf are judged by the transition time of the 10% amplitude point and 90% amplitude point respectively.

(2) The electrostatic capacity CL includes the stray capacitance of the wire connection and the input capacitance of the probe.

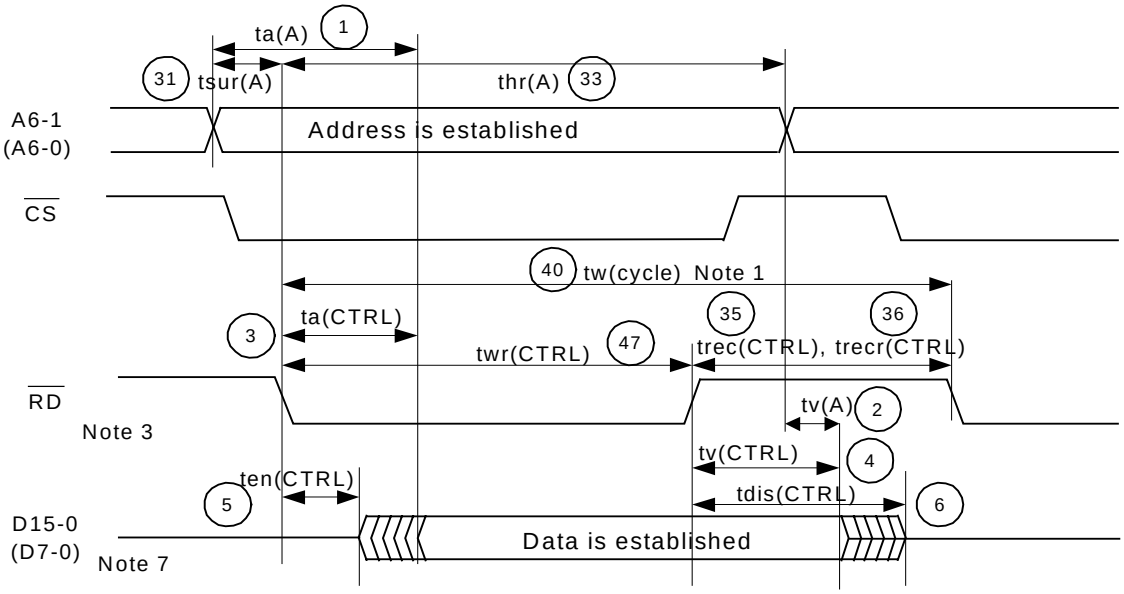
4.9 Timing Diagram

4.9.1 CPU interface timing

(1-1) Write timing (*RD="H")



(1-2) Read timing (*LWR="H", *HWR="H")

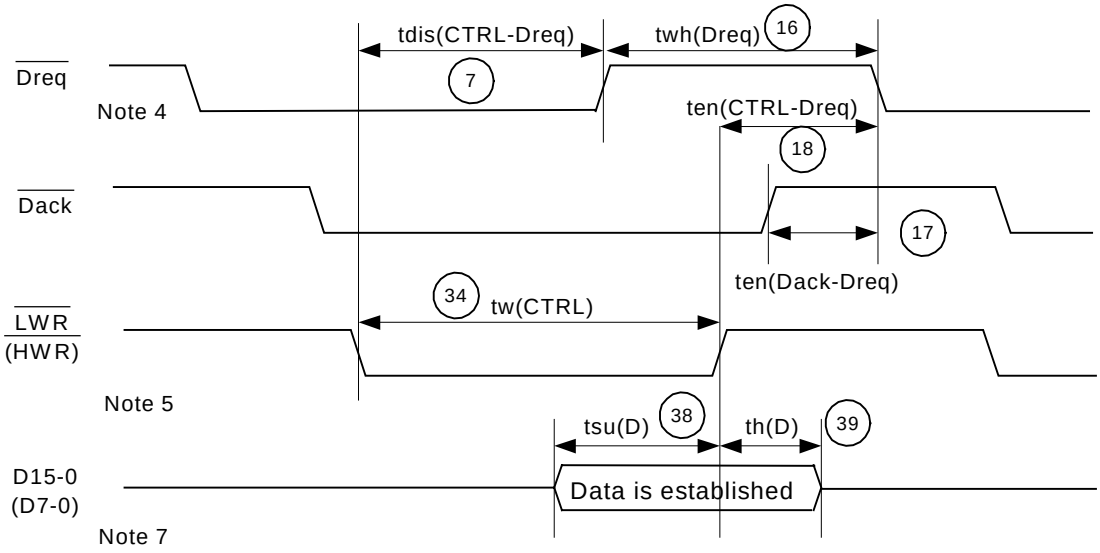


Note 1: tw(cycle), trec(CTRL) are necessary for making access to FIFO.
Further trecr(CTRL) is valid at the time of register access.
Note 2: Writing through the combination of *CS, *HWR and *LWR is carried out during the overlap of active (“L”).
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (“L”).
Note 3: Reading through the combination of *CS, *RD is carried out during the overlap of active (“L”).
The specification from the falling edge is valid from the latest active signal.
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (“L”).
Note 7: In 8-bit Mode, D7~0 and A6~0 become valid.

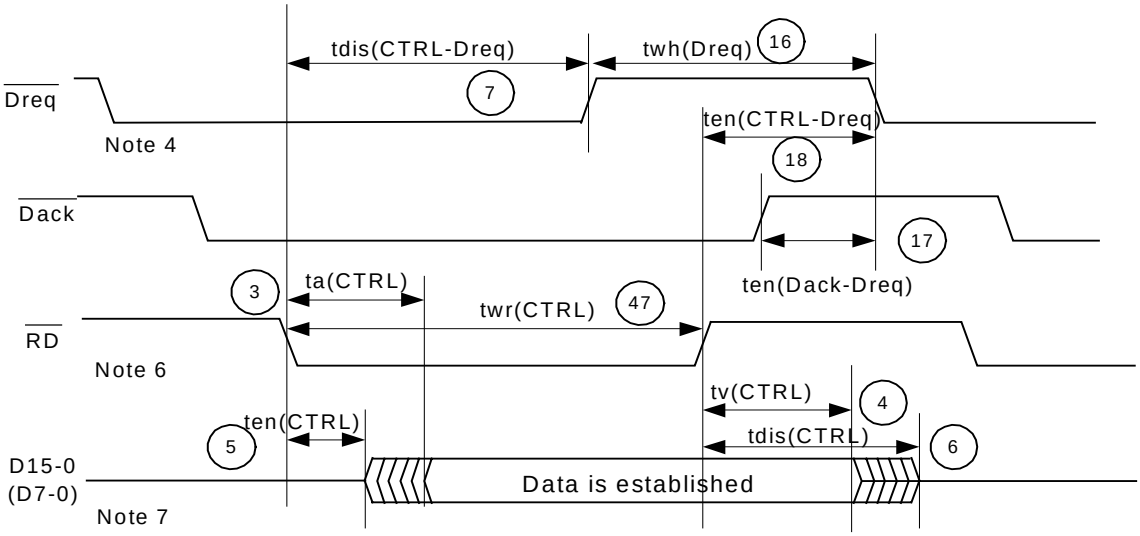
4.9.2 DMA Transfer Timing 1

When set to Cycle Steal Transfer (DMA Transfer Mode Register: BUST = 0)

(2-1) Write timing 1 (DMAEN=1, DFORM=00)

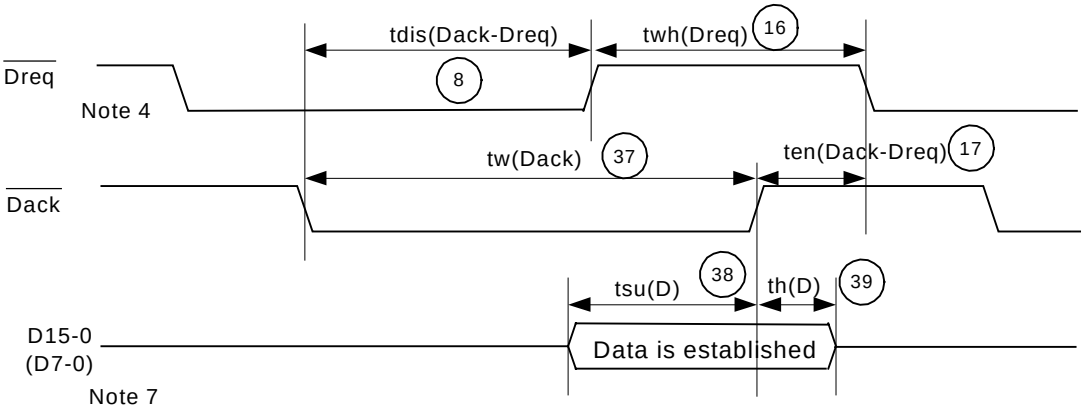


(2-2) Read timing 1 (DMAEN=1, DFORM=00)

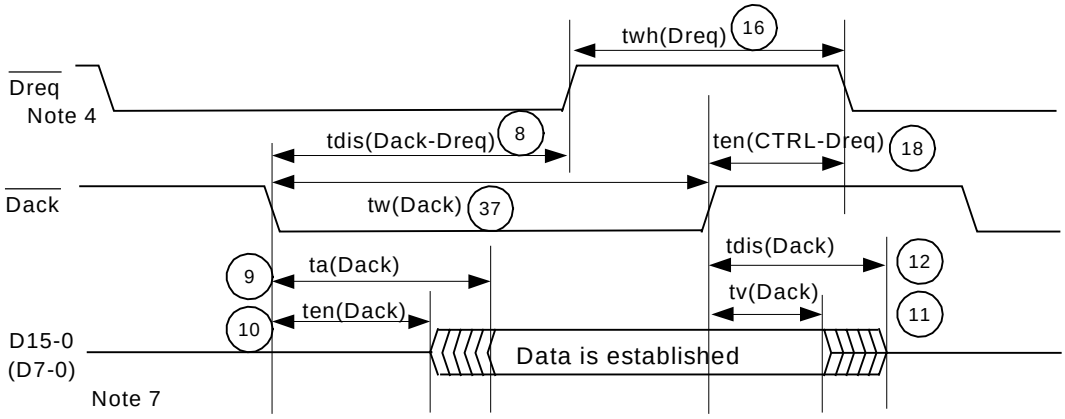


Note 4: *Dack="L" level is the condition for inactive *Dreq, and the latter signal of twh(Dreq) or ten(CTRL-Dreq) becomes valid as the specification of active *Dreq at the time of next DMA transfer.
Note 5: Writing through the combination of *Dack, *HWR and *LWR is carried out during the overlap of active (“L”).
The specification of the rising edge is valid from the earliest inactive signal.
The specification of pulse width is valid during the overlap of active (“L”).
Note 6: Reading through the combination of *Dack and *RD is carried out during the overlap of active (“L”).
The specification from the falling edge is valid from the latest active signal.
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width is valid during the overlap of active (“L”).
Note 7: In 8-Bit Mode, D7~0 becomes valid.

(2-3) Write timing 2 (DMAEN=1, DFORM=01)

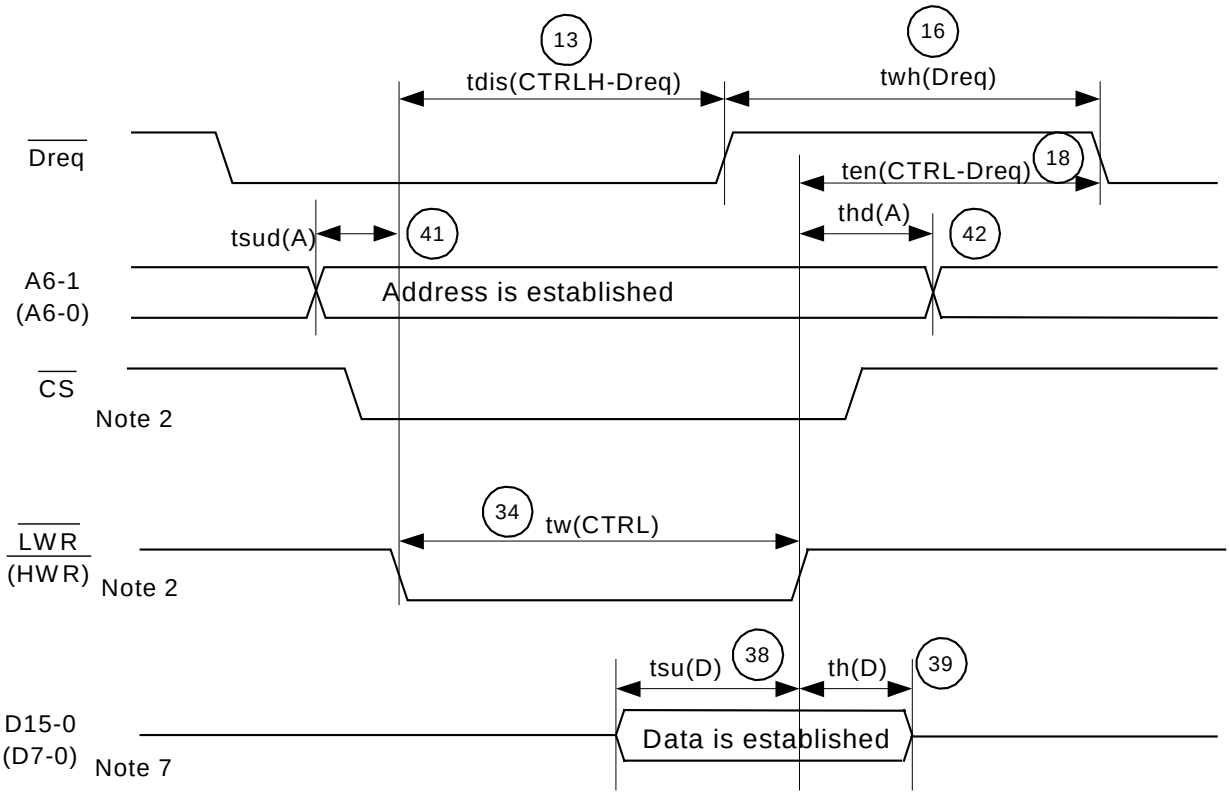


(2-4) Read timing 2 (DMAEN=1, DFORM=01)



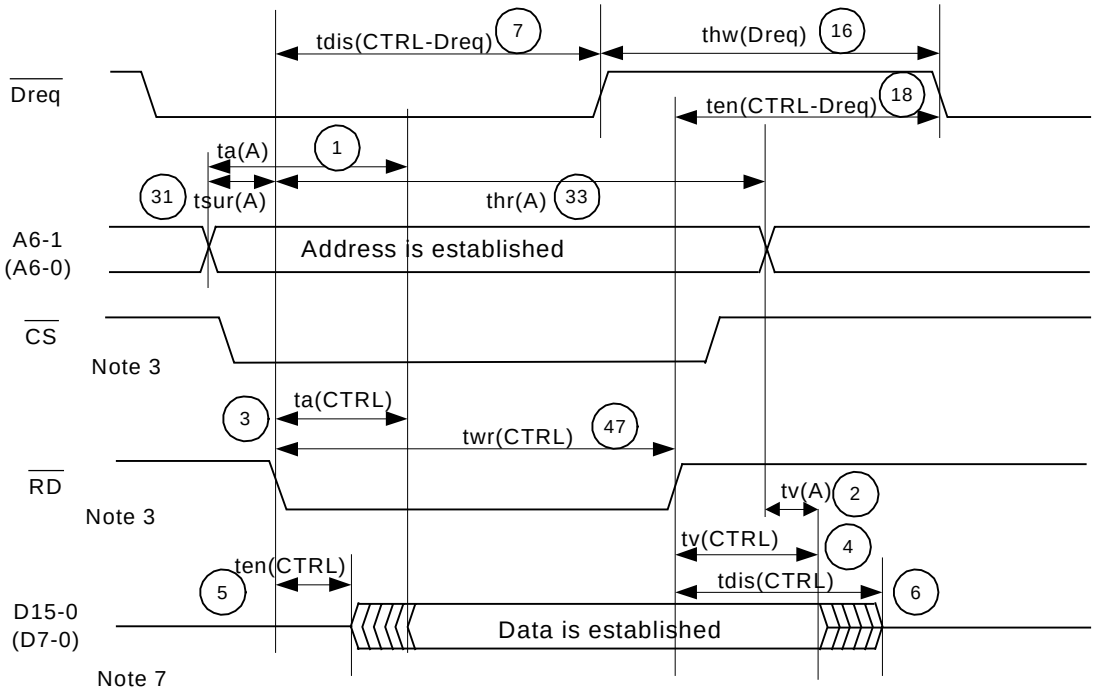
Note 4: *Dack="L" level is the condition for inactive *Dreq, and the latter signal of twh(Dreq) or ten(Dack-Dreq) becomes valid as the specification of active *Dreq at the time of next DMA transfer.
Note 7: In 8-Bit Mode, D7~0 becomes valid.

(2-5) Write timing 3 (DMAEN=1, DFORM=10) (*RD="H")



Note 2: Writing through the combination of *CS, *HWR and *LWR is carried out during the overlap of active ("L").
The specification of the rising edge is valid from the earliest inactive signal.
The specification of pulse width is valid during the overlap of active ("L").
Note 7: In 8-Bit Mode, D7~0 and A6~0 become valid.

(2-6) Read timing 3 (DMAEN=1, DFORM=10) (*LWR="H", *HWR="H")

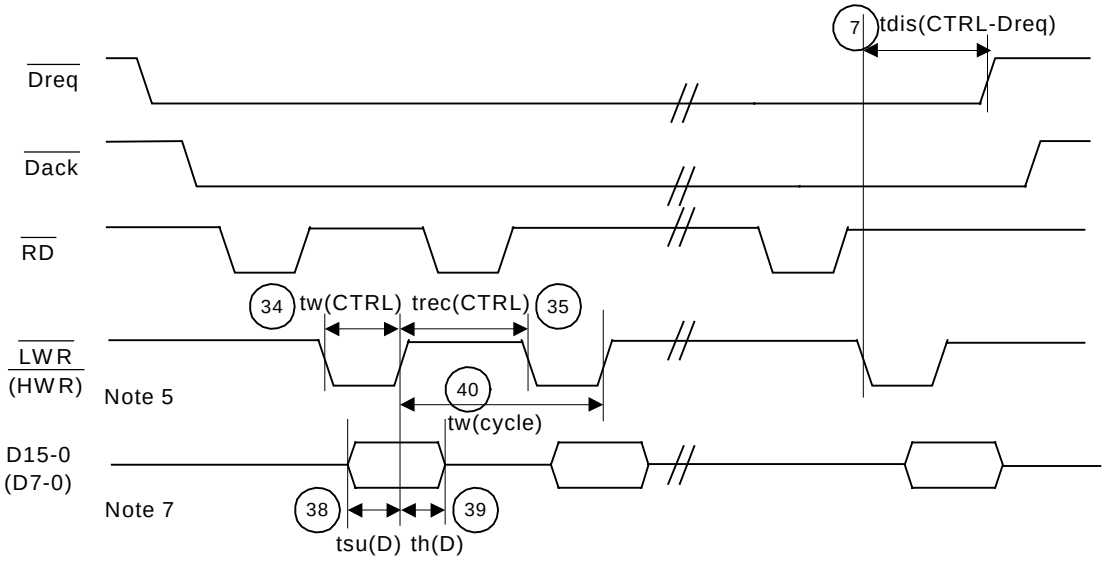


Note 3: Reading through the combination of *CS and *RD is carried out during the overlap of active ("L").
The specification of the falling edge is valid from the latest active signal.
The specification of the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active ("L").
Note 7: In 8-Bit Mode, D7~0 and A6~0 become valid.

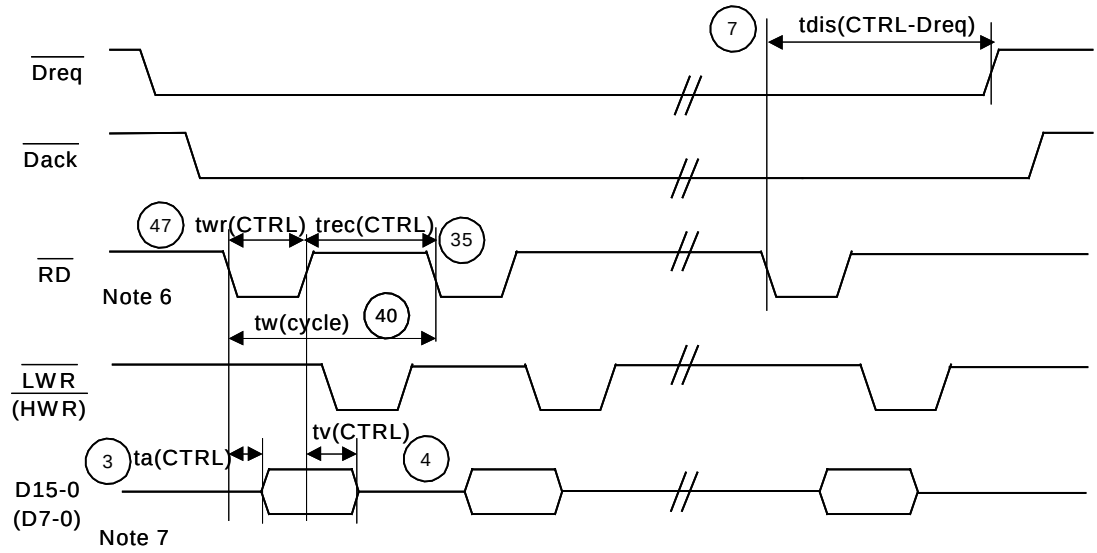
4.9.3 DMA Transfer Timing 2

When set to Burst Transfer (DMA Transfer Mode Register : BUST=1)

(3-1) Write timing (DMAEN=1, DFORM=00)

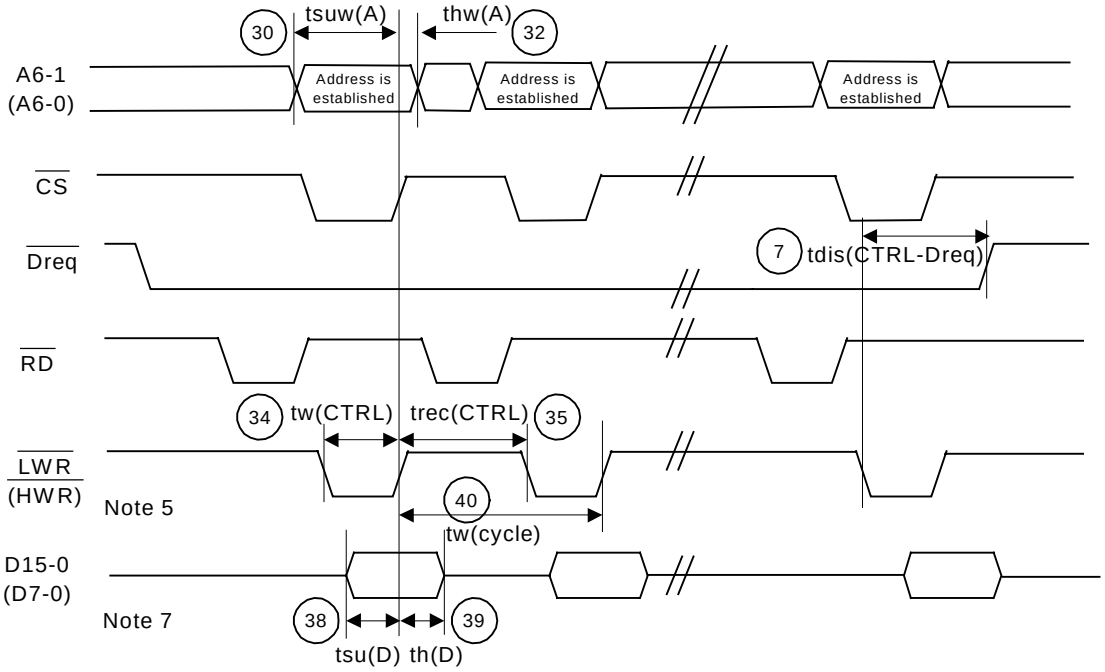


(3-2) Read timing (DMAEN=1, DFORM=00)

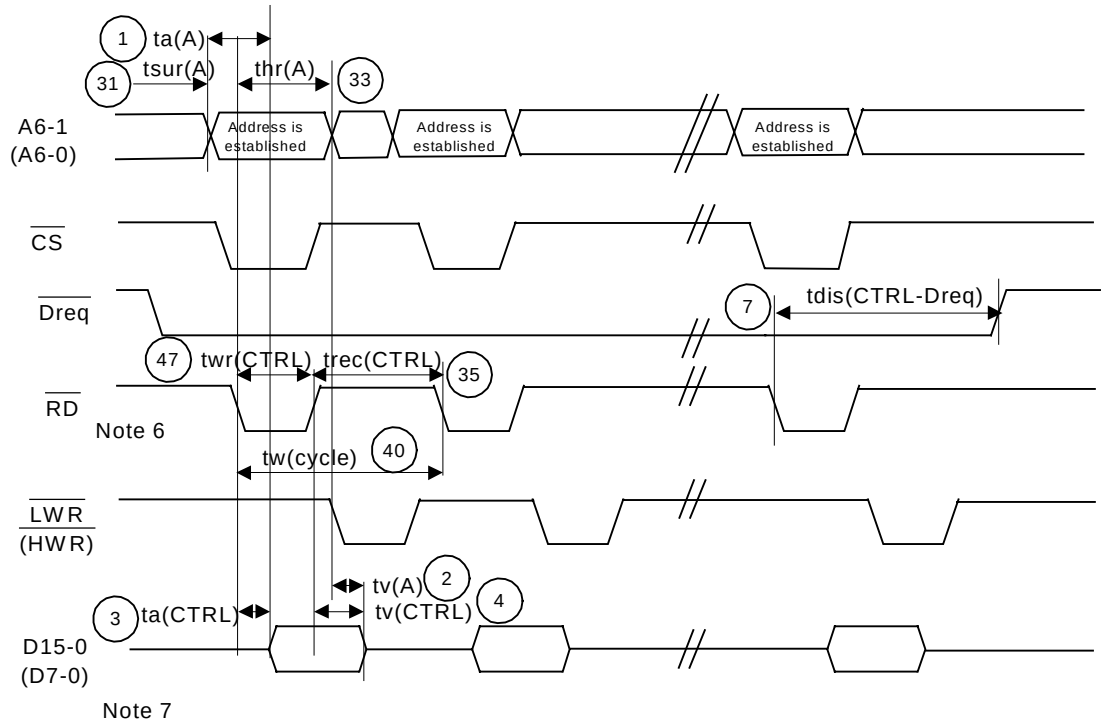


Note 5: Writing through the combination of *Dack, *HWR and *LWR is carried out during the overlap of active ("L"):
The specification of the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active ("L").
Note 6: Reading through the combination of *Dack and *RD is carried out during the overlap of active ("L").
The specification from the falling edge is valid from the latest active signal.
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active ("L").
Note 7: In 8-Bit Mode, D7~0 becomes valid.

(3-3) Write timing (DMAEN=1, DFORM=10)

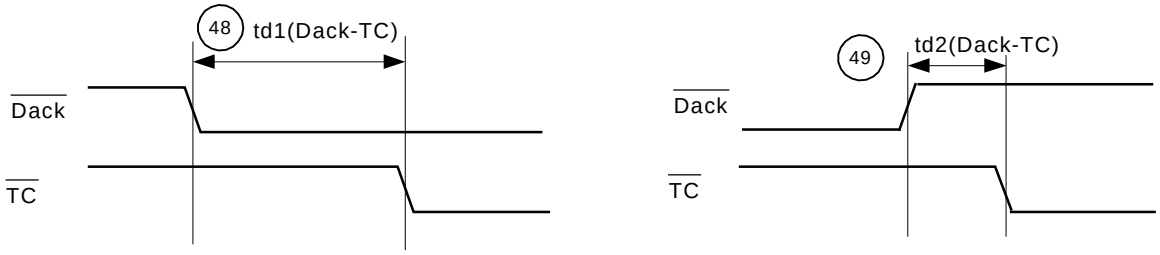


(3-4) Read timing (DMAEN=1, DFORM=10)

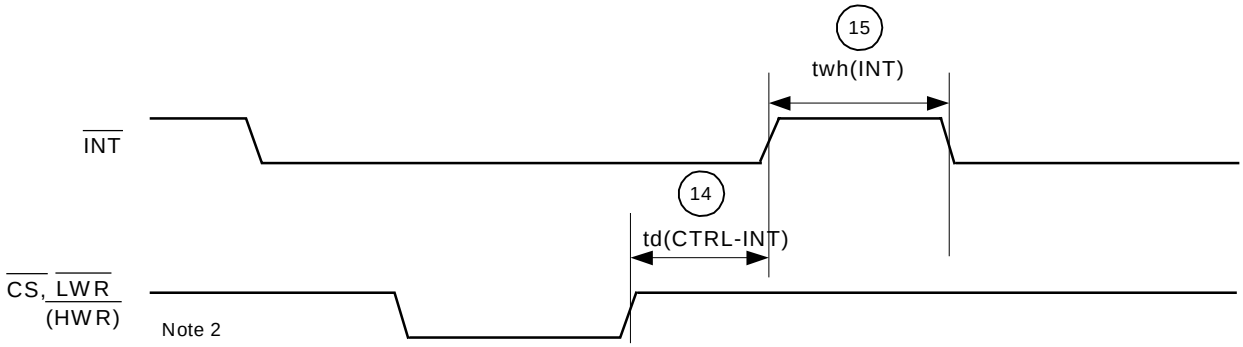


Note 5: Writing through the combination of *Dack, *HWR and *LWR is carried out during the overlap of active (“L).
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (“L”).
Note 6: Reading through the combination of *Dack and *RD is carried out during the overlap of active (“L”).
The specification from the falling edge is valid from the latest active signal.
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (“L”).
Note 7: In 8-Bit Mode, D7~0 becomes valid.

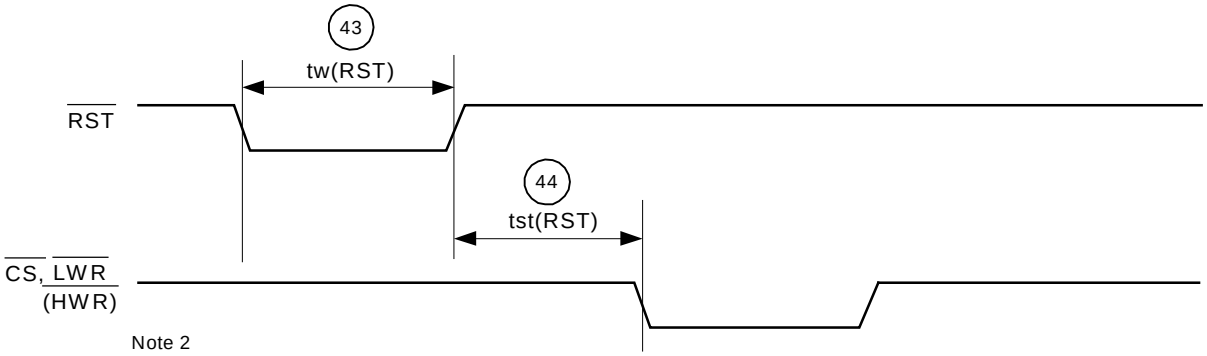
(3-5) TC timing



4.10 Interrupt Timing

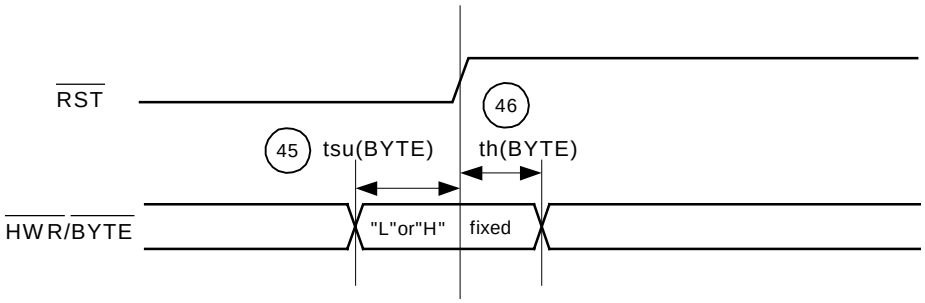


4.11 Reset Timing



Note 2: Writing through the combination of *CS, *HWR and *LWR is carried out during the overlap of active (“L”). The specification from the rising edge is valid from the earliest inactive signal.

4.12 Bus Interface Select Timing

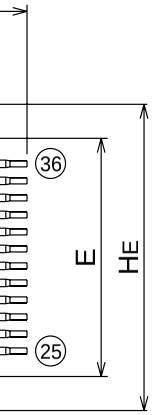


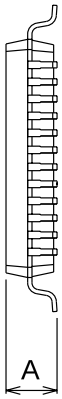
REVISION HISTORY	M66291 Data Sheet

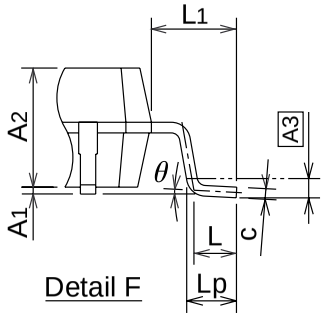
Rev.	Date	Description	
		Page	Summary
1.00	Apr 9, 2001	-	First edition issued
1.01	Nov 1, 2004	1,6	Modified: USB Specification **Revision 2.0**
		3	Added: M66291HP Pin Configration
		9	Moved: How to Read Register Tables
		10,42,43,60, 69,77,78	Modified: **M66291**
		102	Modified: 4.2 Recommended Operating Conditions (CoreVcc,Topr)
		125	Added: 52PJV-A PKG Code.

Plastic 48pin 7X7mm body LQFP

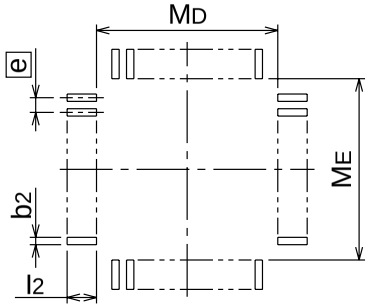
JEDEC Code	Weight(g)	Lead Material
–	–	Cu Alloy







Detail F

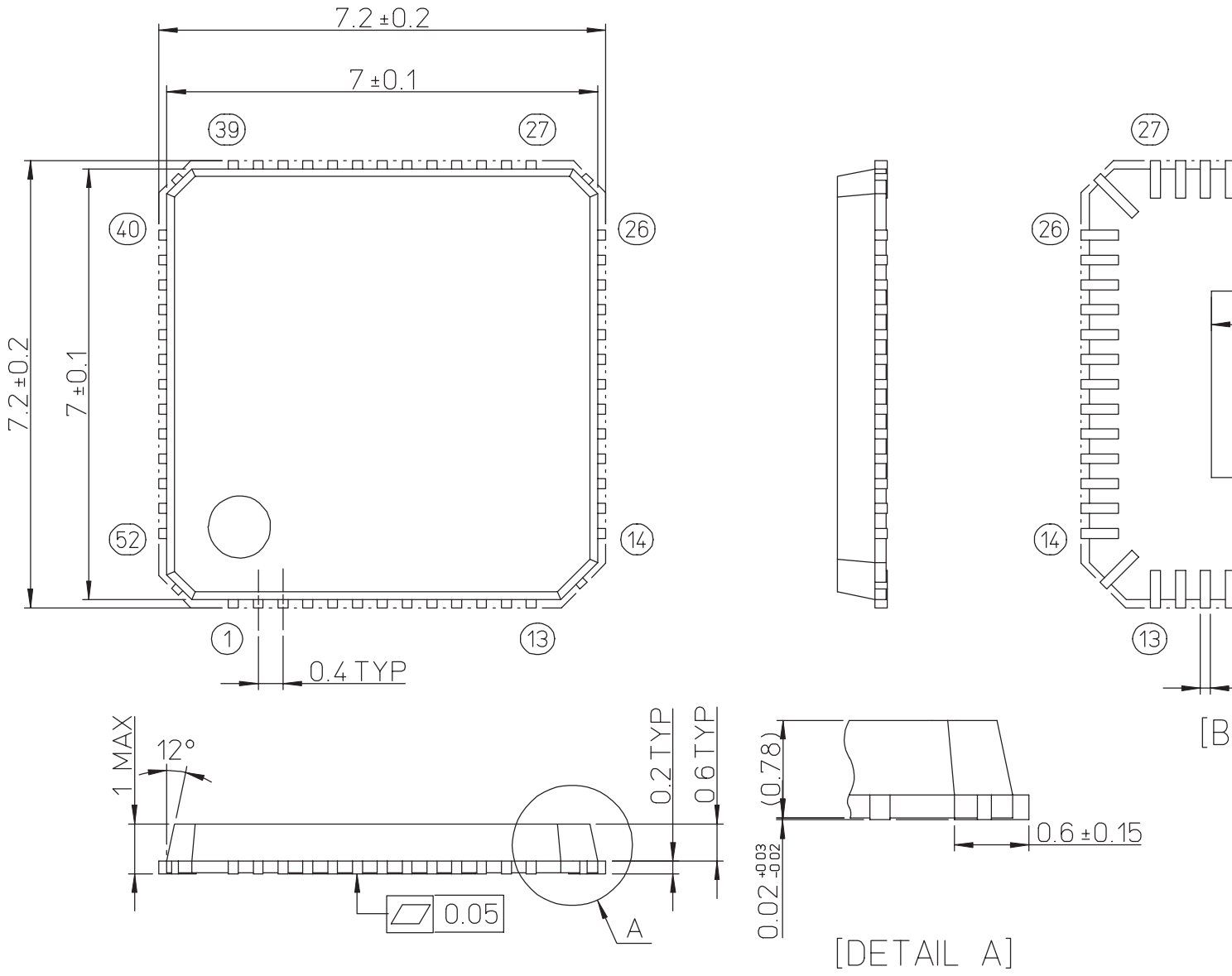


Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	–	0.5	–
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
L	0.35	0.5	0.65
L_1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b_2	–	0.225	–
l_2	1.0	–	–
M_D	–	7.4	–
M_E	–	7.4	–

52PJV-A

Plastic



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