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38D5 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0158-0304
Rev.3.04
May 20, 2008

DESCRIPTION

The 38D5 Group is the 8-bit microcomputer based on the 740 Family core technology.
The 38D5 Group is pin-compatible with the 38C5 Group.
The 38D5 Group has an LCD drive control circuit, an A/D converter, a serial interface, and a ROM correction function as additional functions.
The QzROM version and the flash memory version are available.
The flash memory version does not have a selection function for the oscillation start mode. Only the on-chip oscillator starts oscillating.
The various microcomputers include variations of memory size, and packaging. For details, refer to the section on part numbering.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.32 µs
  (at 12.5 MHz oscillation frequency)
- Memory size (QzROM version)
  ROM ..... 32 K to 60 K bytes
  RAM ..... 1536 to 2048 bytes
- Memory size (Flash memory version)
  ROM ..... 60 K bytes
  RAM ..... 2048 bytes
- Programmable input/output ports .. 59 (common to SEG: 36)
- Interrupts ..... 17 sources, 16 vectors
  (Key input interrupt included)
- Timers ..... 8-bit × 4, 16-bit × 2
- Serial interface
  Serial I/O1 .....8-bit × 1 (UART or Clock-synchronized)
  Serial I/O2 ..... 8-bit × 1 (Clock-synchronized)
- PWM ..... 10-bit × 2, 16-bit × 1 (common to IGBT output)
- A/D converter ..... 10-bit × 8 channels
  (A/D converter can be operated in low-speed mode.)
- Watchdog timer ..... 8-bit × 1
- ROM correction function ..... 32 bytes × 2 vectors
- LED direct drive port 6
  (average current: 15 mA, peak current: 30 mA, total current: 90 mA)
- LCD drive control circuit
  Bias 1/2, 1/3
  Duty ..... Static, 2, 3, 4, 8
  Common output 4/8
  Segment output 32/36
- Main clock generating circuit 1
  (connect to external ceramic resonator or on-chip oscillator)
- Sub-clock generating circuit 1
  (connect to external quartz-crystal oscillator)
- Power source voltage (QzROM version)
  [In frequency/2 mode]
  f(XIN) ≤ 12.5 MHz..... 4.5 to 5.5 V
  f(XIN) ≤ 8 MHz..... 4.0 to 5.5 V
  f(XIN) ≤ 4 MHz..... 2.0 to 5.5 V
  f(XIN) ≤ 2 MHz..... 1.8 to 5.5 V
  [In frequency/4 mode]
  f(XIN) ≤ 16 MHz..... 4.5 to 5.5 V
  f(XIN) ≤ 8 MHz..... 2.0 to 5.5 V
  f(XIN) ≤ 4 MHz..... 1.8 to 5.5 V
  [In frequency/8 mode]
  f(XIN) ≤ 16 MHz..... 4.5 to 5.5 V
  f(XIN) ≤ 8 MHz..... 2.0 to 5.5 V
  f(XIN) ≤ 4 MHz..... 1.8 to 5.5 V
  [In low-speed mode]..... 1.8 to 5.5 V
  Note. 12.5 MHz < f(XIN) ≤ 16 MHz is not available in the frequency/2 mode.
- Power source voltage (Flash memory version)
  [In frequency/2 mode]
  f(XIN) ≤ 12.5 MHz..... 4.5 to 5.5 V
  f(XIN) ≤ 8 MHz..... 4.0 to 5.5 V
  f(XIN) ≤ 4 MHz..... 2.7 to 5.5 V
  [In frequency/4 mode]
  f(XIN) ≤ 16 MHz..... 4.5 to 5.5 V
  f(XIN) ≤ 8 MHz..... 2.7 to 5.5 V
  [In frequency/8 mode]
  f(XIN) ≤ 16 MHz..... 4.5 to 5.5 V
  f(XIN) ≤ 8 MHz..... 2.7 to 5.5 V
  [In low-speed mode]..... 2.7 to 5.5 V
  Note. 12.5 MHz < f(XIN) ≤ 16 MHz is not available in the frequency/2 mode.
- Power dissipation (QzROM version)
  - In frequency/2 mode ..... Typ. 32 mW
    (VCC = 5 V, f(XIN) = 12.5 MHz, Ta = 25°C)
  - In low-speed mode ..... Typ. 18 µW
    (VCC = 2.5 V, f(XIN) = stop, f(XCIN) = 32 kHz, Ta = 25°C)
- Power dissipation (Flash memory version)
  - In frequency/2 mode ..... Typ. 20 mW
    (VCC = 5 V, f(XIN) = 12.5 MHz, Ta = 25°C)
  - In low-speed mode ..... Typ. 1.1 mW
    (VCC = 2.7 V, f(XIN) = stop, f(XCIN) = 32 kHz, Ta = 25°C)
- Operating temperature range ..... –20 to 85°C

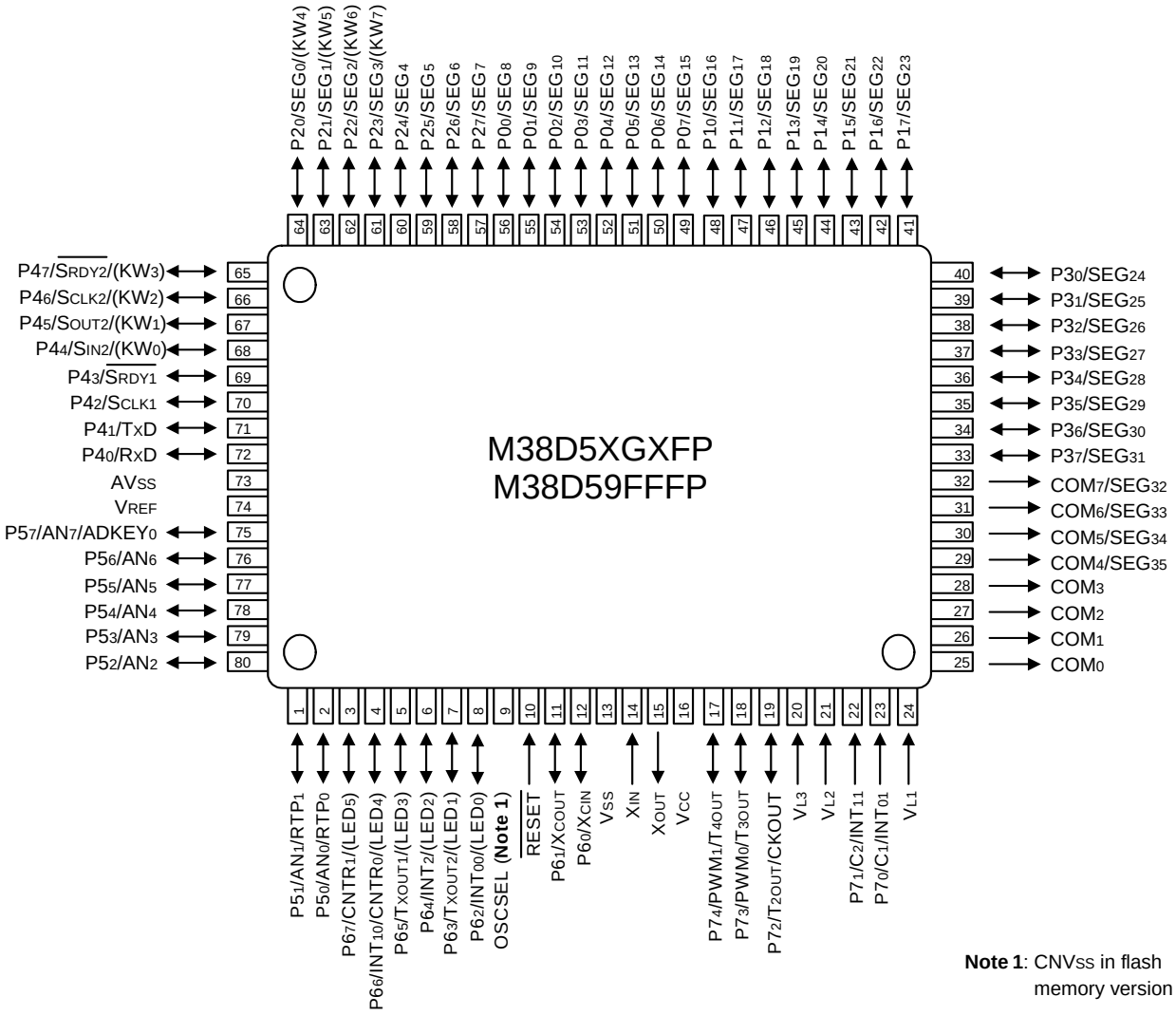
Flash Memory Mode

- Program/Erase voltage ..... VCC = 2.7 to 5.5 V
- Program method ..... Programming in unit of byte
- Erase method ..... Block erasing
- Program/Erase control by software command

APPLICATION

Household products, Consumer electronics, etc.

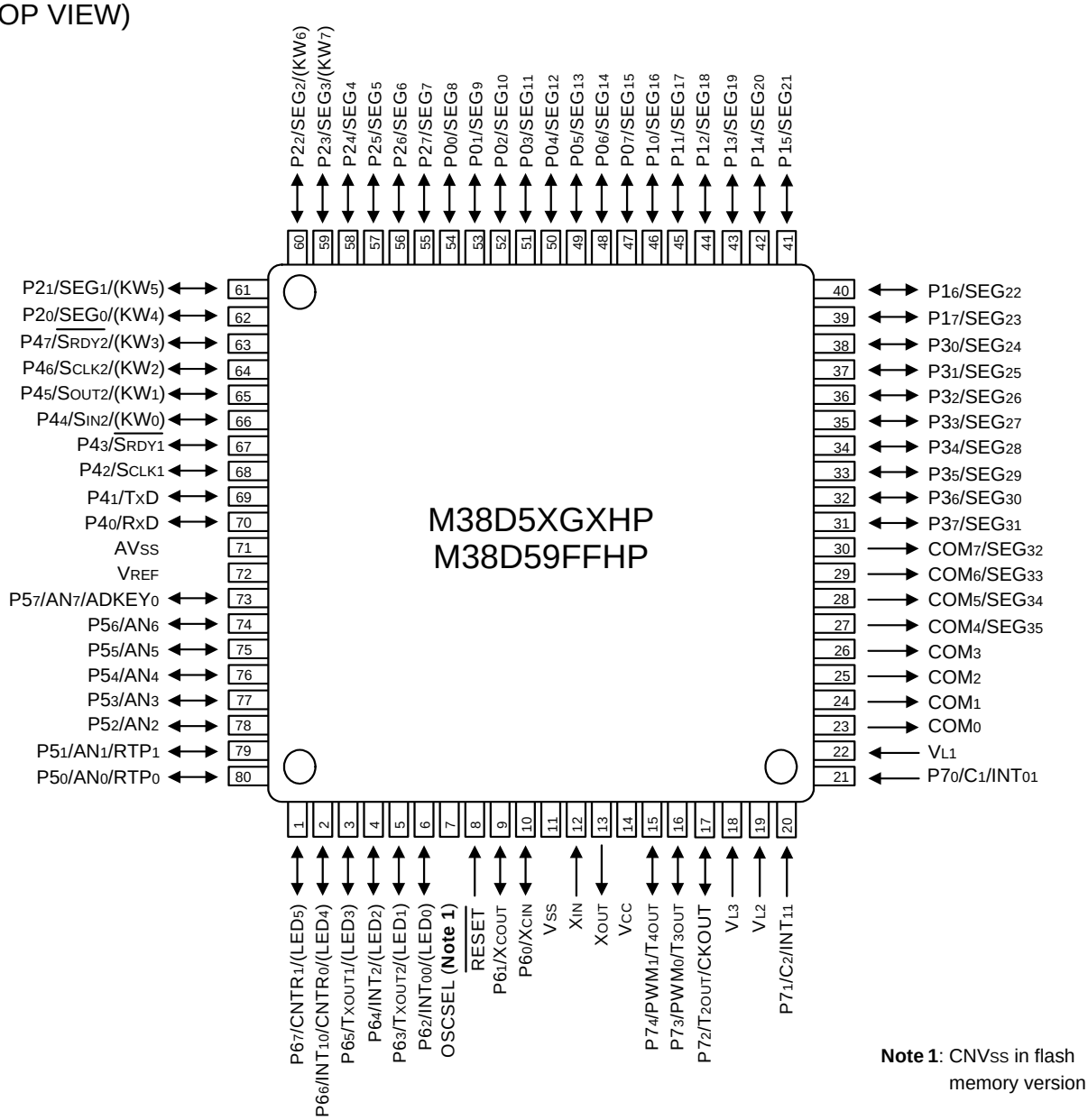
PIN CONFIGURATION
(TOP VIEW)



Package type : PRQP0080GB-A(80P6N-A)

Fig. 1 Pin configuration (QFP Package)

PIN CONFIGURATION
(TOP VIEW)



Package type : PLQP0080KB-A(80P6Q-A)

Fig. 2 Pin configuration (LQFP package)

Table 1 Performance overview (1)

Parameter			Function
Number of basic instructions			71
Instruction execution time			0.32 μs (Minimum instruction, Oscillation frequency 12.5 MHz)
Oscillation frequency			16 MHz (Maximum)(1)
Memory sizes (QzROM version)	ROM		32 K to 60 K bytes
	RAM		1536 to 2048 bytes
Memory sizes (Flash memory version)	ROM		60 K bytes
	RAM		2048 bytes
Input port	$P7_0$, $P7_1$		2-bit × 1
I/O port	P0-P6, $P7_2$-$P7_4$		8-bit × 7, 3-bit × 1 (36 pins sharing SEG)
Interrupt			17 sources, 16 vectors (includes key input interrupt)
Timer			8-bit × 4, 16-bit × 2
Serial I/O1			8-bit × 1 (UART or Clock-synchronized)
Serial I/O2			8-bit × 1 (Clock-synchronized)
PWM			10-bit × 2, 16-bit × 1 (common to IGBT output)
A/D converter			10-bit × 8 (operated in low-speed mode)
Watchdog timer			8-bit × 1
ROM correction function			32 bytes × 2 vectors
LED direct drive port			6 (average current: 15 mA, peak current: 30 mA, total current: 90 mA)
LCD drive control circuit	Bias		1/2, 1/3
	Duty		Static, 2, 3, 4, 8
	Common output		4/8
	Segment output		32/36
Main clock generating circuits			Built-in (connect to external ceramic resonator or on-chip oscillator)
Sub-clock generating circuits			Built-in (connect to external quartz-crystal oscillator)
Power source voltage (QzROM version)	In frequency/2 mode (1)	$f(X_{IN}) \leq 12.5$ MHz	4.5 to 5.5 V
		$f(X_{IN}) \leq 8$ MHz	4.0 to 5.5 V
		$f(X_{IN}) \leq 4$ MHz	2.0 to 5.5 V
		$f(X_{IN}) \leq 2$ MHz	1.8 to 5.5 V
	In frequency/4 mode	$f(X_{IN}) \leq 16$ MHz	4.5 to 5.5 V
		$f(X_{IN}) \leq 8$ MHz	2.0 to 5.5 V
		$f(X_{IN}) \leq 4$ MHz	1.8 to 5.5 V
	In frequency/8 mode	$f(X_{IN}) \leq 16$ MHz	4.5 to 5.5 V
		$f(X_{IN}) \leq 8$ MHz	2.0 to 5.5 V
		$f(X_{IN}) \leq 4$ MHz	1.8 to 5.5 V
	In low-speed mode		1.8 to 5.5 V
Power source voltage (Flash memory version)	In frequency/2 mode (1)	$f(X_{IN}) \leq 12.5$ MHz	4.5 to 5.5 V
		$f(X_{IN}) \leq 8$ MHz	4.0 to 5.5 V
		$f(X_{IN}) \leq 4$ MHz	2.7 to 5.5 V
	In frequency/4 mode	$f(X_{IN}) \leq 16$ MHz	4.5 to 5.5 V
		$f(X_{IN}) \leq 8$ MHz	2.7 to 5.5 V
	In frequency/8 mode	$f(X_{IN}) \leq 16$ MHz	4.5 to 5.5 V
		$f(X_{IN}) \leq 8$ MHz	2.7 to 5.5 V
	In low-speed mode		2.7 to 5.5 V

NOTE:
1. 12.5 MHz < $f(X_{IN}) \leq 16$ MHz is not available in the frequency/2 mode.

Table 2 Performance overview (2)

Parameter		Function
Power dissipation (QzROM version)	In frequency/2 mode	Std. 32 mW (Vcc = 5 V, f(XIN) = 12.5 MHz, Ta = 25°C)
	In low-speed mode	Std. 18 µW (Vcc = 2.5 V, f(XIN) = stop, f(XCIN) = 32 kHz, Ta = 25°C)
Power dissipation (Flash memory version)	In frequency/2 mode	Std. 20 mW (Vcc = 5 V, f(XIN) = 12.5 MHz, Ta = 25°C)
	In low-speed mode	Std. 1.1 mW (Vcc = 2.7 V, f(XIN) = stop, f(XCIN) = 32 kHz, Ta = 25°C)
Input/Output characteristics	Input/Output withstand voltage	VCC
	Output current	10 mA
Operating temperature range		-20 to 85°C
Device structure		CMOS silicon gate
Package		80-pin plastic molded LQFP/QFP

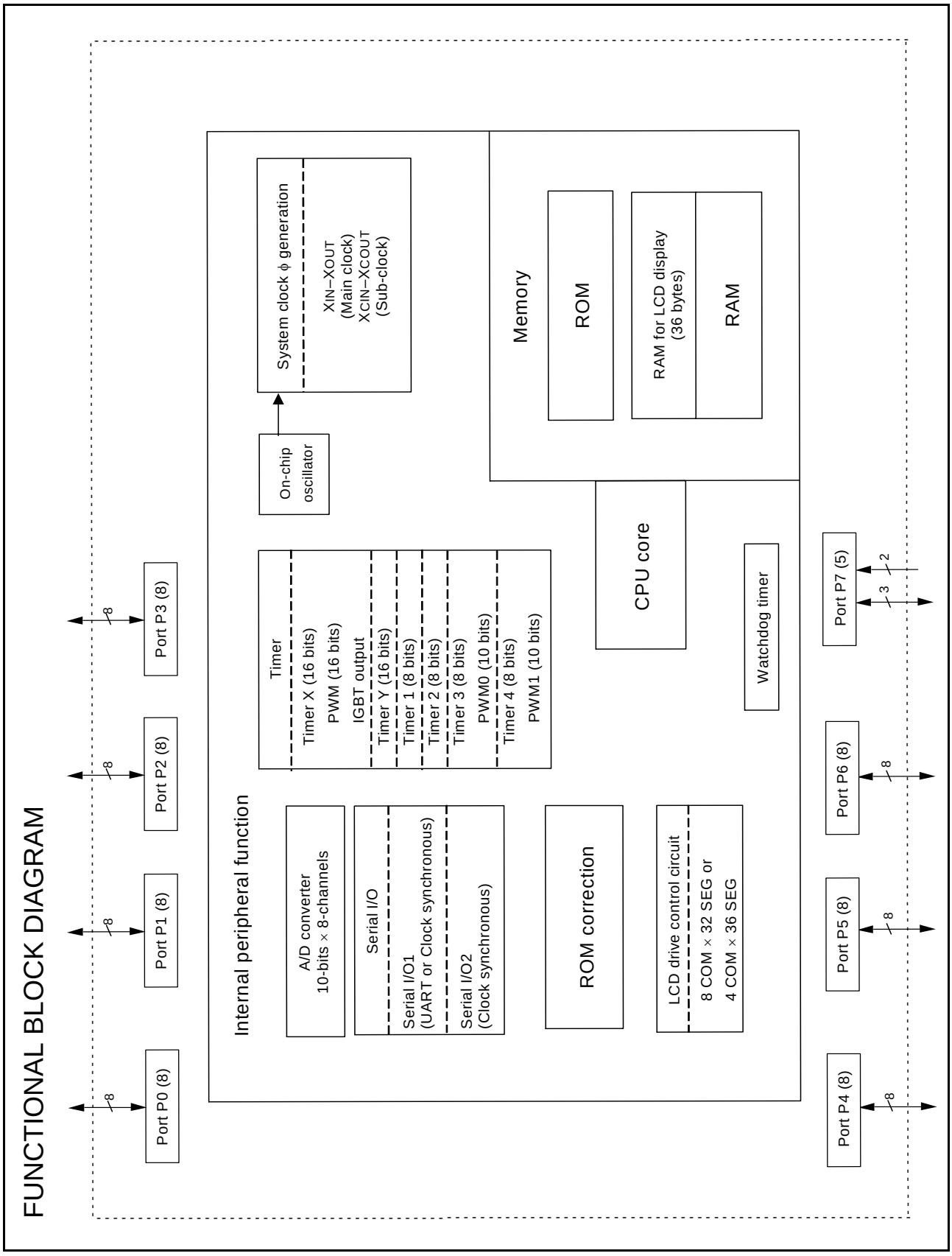


Fig. 3 Functional block diagram

PIN DESCRIPTION

Table 3 Pin description (1)

Pin	Name	Function	Function except a port function	
V_{CC}, V_{SS}	Power source	• Apply power source voltage to V_{CC}, and 0 V to V_{SS}.		
$\overline{RESET}$	Reset input	• Reset input pin for active “L”.		
X_{IN}	Clock input	• Input and output pins for the main clock generating circuit. • Connect a ceramic resonator or a quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. When an external clock is used, connect the clock source to X_{IN}, and leave X_{OUT} pin open. • Feedback resistor is built in between X_{IN} pin and X_{OUT} pin.		
X_{OUT}	Clock output			
V_{L1}, V_{L2}, V_{L3}	LCD power source	• Input 0 ≤ V_{L1} ≤ V_{L2} ≤ V_{L3} voltage. • Input 0 – V_{L3} voltage to LCD.		
COM_0– COM_3	Common output	• LCD common output pins. • COM_2 and COM_3 are not used at 1/2 duty ratio. • COM_3 is not used at 1/3 duty ratio.		
COM_4/SEG_{35}– COM_7/SEG_{32}	Common output Segment output	• LCD common/segment output pins.		
$P0_0/SEG_8$– $P0_7/SEG_{15}$	I/O port P0	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled in a bit unit.		
$P1_0/SEG_{16}$– $P1_7/SEG_{23}$	I/O port P1	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be programmed as either input or output. • Pull-up control is enabled in 4-bit unit.		
$P2_0/SEG_0/(KW_4)$– $P2_3/SEG_3/(KW_7)$	I/O port P2	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled in a bit unit.		• Key input interrupt input pins
$P2_4/SEG_4$– $P2_7/SEG_7$				
$P3_0/SEG_{24}$– $P3_7/SEG_{31}$	I/O port P3	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled in 4-bit unit.		
$P4_0/R_XD$ $P4_1/T_XD$ $P4_2/S_{CLK1}$ $P4_3/\overline{S_{RDY1}}$	I/O port P4	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled in 4-bit unit.	• Serial I/O1 function pins	
$P4_4/S_{IN2}/(KW_0)$ $P4_5/S_{OUT2}/(KW_1)$ $P4_6/S_{CLK2}/(KW_2)$ $P4_7/\overline{S_{RDY2}}/(KW_3)$			• Serial I/O2 function pins	• Key input interrupt input pins

Table 4 Pin description (2)

Pin	Name	Function	Function except a port function	
$P5_0/AN_0/RTP_0$ $P5_1/AN_1/RTP_1$	I/O port P5	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled in a bit unit.	• AD converter input pins	• Real time port function pins
$P5_2/AN_2$– $P5_6/AN_6$				
$P5_7/AN_7/ADKEY_0$				• ADKEY input pin
$P6_0/X_{CIN}$ $P6_1/X_{COUT}$	I/O port P6	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled in a bit unit. • $P6_2$ to $P6_7$ (6 bits) are enabled to output large current for LED drive.	• Sub clock generating I/O pins (oscillator connected)	
$P6_2/INT_{00}/(LED_0)$ $P6_3/T_{XOUT2}/(LED_1)$ $P6_4/INT_2/(LED_2)$			• External interrupt pin	
			• Timer X output pin	
			• External interrupt pin	
$P6_5/T_{XOUT1}/(LED_3)$			• Timer X output pin	
$P6_6/INT_{10}/CNTR_0/(LED_4)$ $P6_7/CNTR_1/(LED_5)$			• Timer X, Timer Y output pins	• External interrupt pins
$P7_0/C_1/INT_{01}$ $P7_1/C_2/INT_{11}$	Input port P7	• 2-bit input port. • CMOS input level.	• External interrupt pins	• External capacitor connect pins for a voltage multiplier of LCD.
$P7_2/T_{2OUT}/CKOUT$	I/O port P7	• 3-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled in 3-bit unit.	• Clock output pin	• Timer 2 output pin
$P7_3/PWM_0/T_{3OUT}$ $P7_4/PWM_1/T_{4OUT}$			• PWM output pins	• Timer 3 output pin • Timer 4 output pin
OSCSEL (Only QzROM version)	Oscillation start selection pin	• Whether oscillation starts by an oscillator between the X_{IN} and X_{OUT} pins or an on-chip oscillator is selected. • V_{PP} power source input pin in the QzROM writing mode.		
CNV_{SS} (Only flash memory version)	CNV_{SS}	• Pin for controlling the operating mode of the chip. Connect to V_{SS}.		
V_{REF}	Analog reference voltage	• Reference voltage input pin for A/D converter.		
AV_{SS}	Analog power source	• Analog power source input pin for A/D converter. Connect to V_{SS}.		

PART NUMBERING

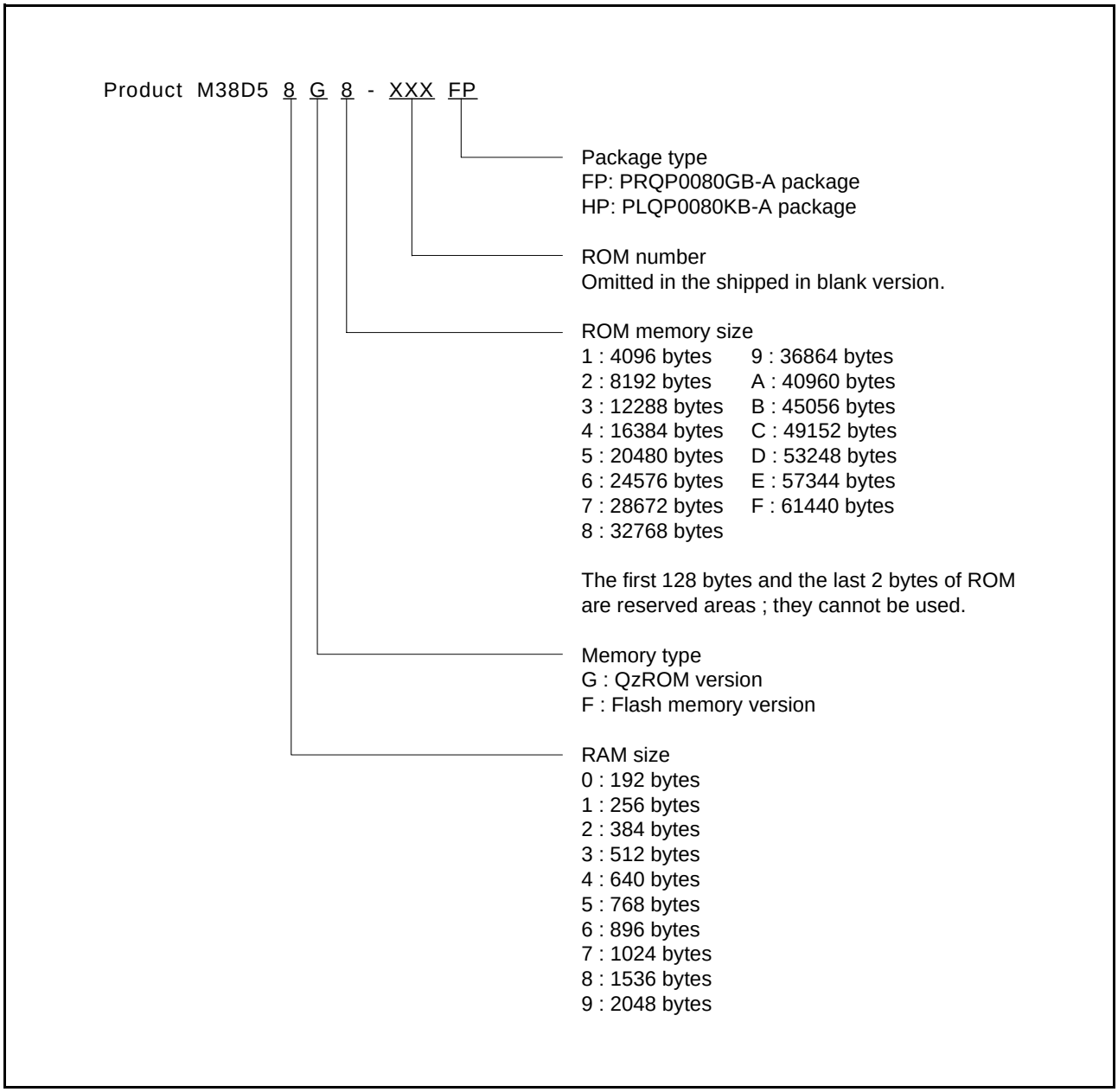


Fig. 4 Part numbering

GROUP EXPANSION

Renesas plans to expand the 38D5 Group as follows.

Memory Size

<QzROM version>
- ROM size ..... 32 K to 60 K bytes
- RAM size ..... 1536 to 2048 bytes

<Flash memory version>
- ROM size ..... 60 K bytes
- RAM size ..... 2048 bytes

Packages

- PRQP0080GB-A ..... 0.8 mm-pitch plastic molded QFP
- PLQP0080KB-A .....0.5 mm-pitch plastic molded LQFP

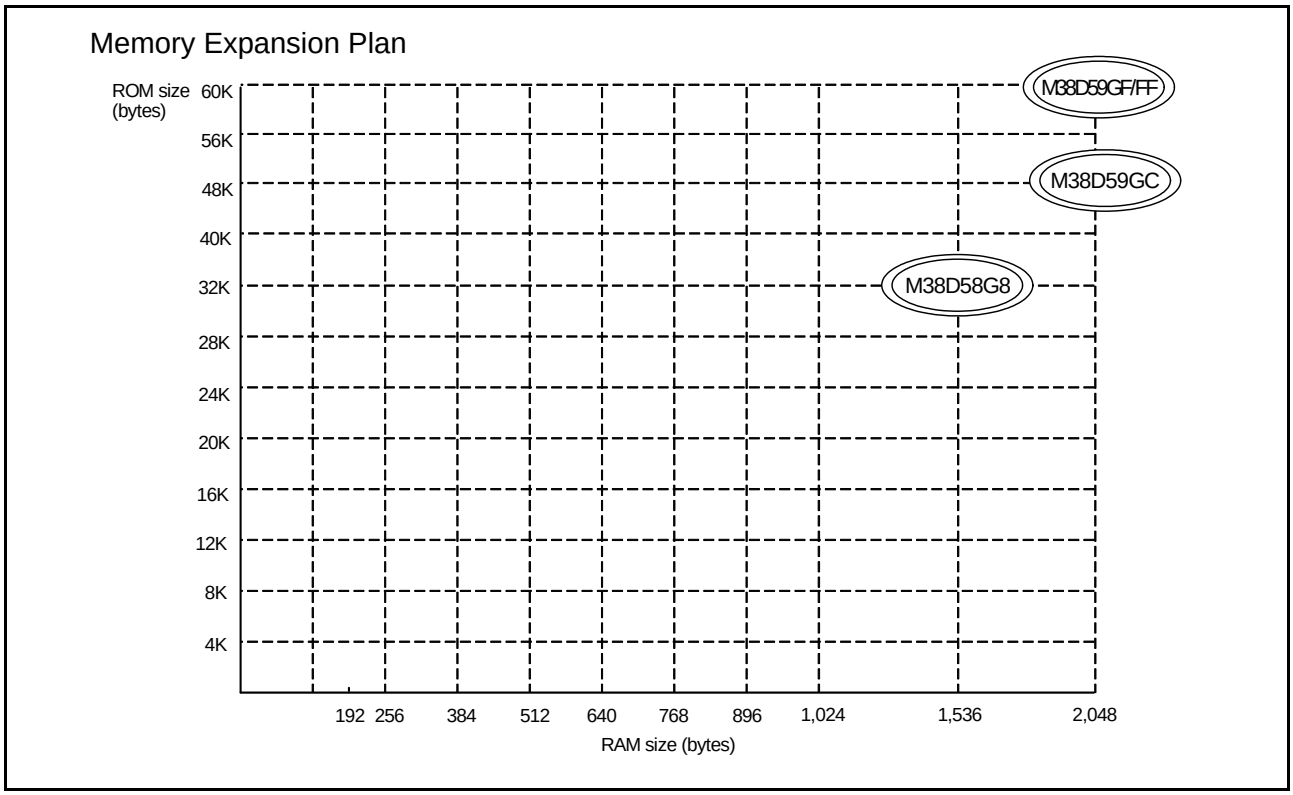


Fig. 5 Memory expansion plan

Currently supported products are listed below.

Table 5 Support products As of Apr. 2008

Part No.	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38D58G8-XXXFP	32768 (32638)	1536	PRQP0080GB-A	QzROM version
M38D58G8-XXXHP			PLQP0080KB-A	
M38D58G8FP	32768 (32638)	1536	PRQP0080GB-A	QzROM version (blank)
M38D58G8HP			PLQP0080KB-A	
M38D59GC-XXXFP	49152 (49022)	2048	PRQP0080GB-A	QzROM version
M38D59GC-XXXHP			PLQP0080KB-A	
M38D59GCFP	49152 (49022)	2048	PRQP0080GB-A	QzROM version (blank)
M38D59GCHP			PLQP0080KB-A	
M38D59GF-XXXFP	61440 (61310)	2048	PRQP0080GB-A	QzROM version
M38D59GF-XXXHP			PLQP0080KB-A	
M38D59GFFP	61440 (61310)	2048	PRQP0080GB-A	QzROM version (blank)
M38D59GFHP			PLQP0080KB-A	
M38D59FFFP	61440 (61310)	2048	PRQP0080GB-A	Flash memory version
M38D59FFHP			PLQP0080KB-A	

Table 6 Differences between QzROM and flash memory versions

	QzROM version		Flash memory version
Oscillation circuit at reset and at returning from stop mode	Main clock X_{IN} or on-chip oscillator selectable by OSCSEL pin		On-chip oscillator
Termination of OSCEL/CNV_{SS} pin	OSCSEL = "H"	OSCSEL = "L"	CNV_{SS} = "L"
Main clock oscillation at reset and at returning from stop mode	Oscillation on	Stop	Stop
On-chip oscillator oscillation at reset and at returning from stop mode	Stop	Oscillation on	Oscillation on
System clock ϕ oscillation at reset and at returning from stop mode	$f(X_{IN})/8$	f(OCO)/32	f(OCO)/32
Mounting of main clock oscillation circuit	Required	Optional	Optional
On-chip oscillator oscillation in low speed-mode	Stop		Stop by setting the on-chip oscillator stop bit because it is not stopped.
Writing "1" to on-chip oscillator stop bit in on-chip oscillator mode	On-chip oscillator is stopped		On-chip oscillator is not stopped
Reset input "L" pulse width	2 μs or more		2 ms or more
Absolute maximum rating: OSCSEL/CNV_{SS} pin	–0.3 to 8.0		–0.3 to V_{CC} + 0.3
Minimum operating power source voltage	1.8 V		2.7 V
A/D converter minimum operating power source voltage	2.0 V		2.7 V

NOTE:
1. For detailed specifications, confirm the descriptions in the Datasheet.

Notes on Differences between QzROM and Flash Memory Versions

(1) The memory map, the writing modes and programming circuits vary because of the differences in their internal memories.
(2) The oscillation parameters of X_{IN}-X_{OUT} and X_{CIN}-X_{COUT} may vary.
(3) The QzROM version and the flash memory version MCUs differ in their manufacturing processes, built-in ROM, and layout patterns. Because of these differences, characteristic values, operation margins, A/D conversion accuracy, noise immunity, and noise radiation may vary within the specified range of electrical characteristics.
(4) When switching from the flash memory version to the QzROM version, implement system evaluations equivalent to those implemented in the flash memory version.
(5) The both operations except the electrical characteristics are same at the emulator (emulator MCU board: M38D59T-RLFS).

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The 38D5 Group uses the standard 740 Family instruction set. Refer to the 740 Family Software Manual for details on the instruction set.
Machine-resident 740 Family instructions are as follows:
The FST and SLW instructions cannot be used.
The STP, WIT, MUL, and DIV instructions can be used.
The central processing unit (CPU) has six registers. Figure 6 shows the 740 Family CPU register structure.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as arithmetic data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.
The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0”, the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.
The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 7.
Table 7 shows the push and pop instructions of accumulator or processor status register.
Store registers other than those described in Figure 7 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

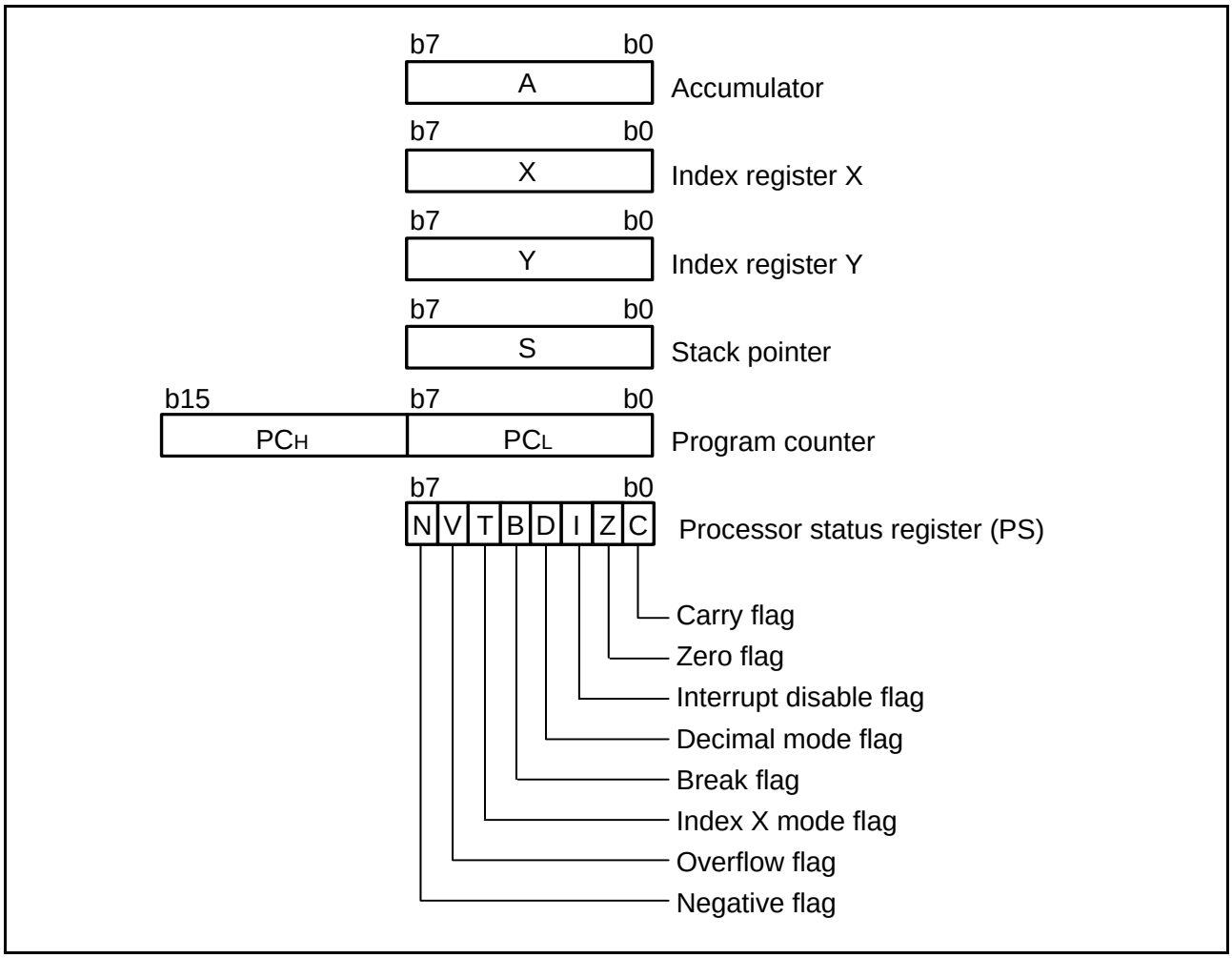


Fig. 6 740 Family CPU register structure

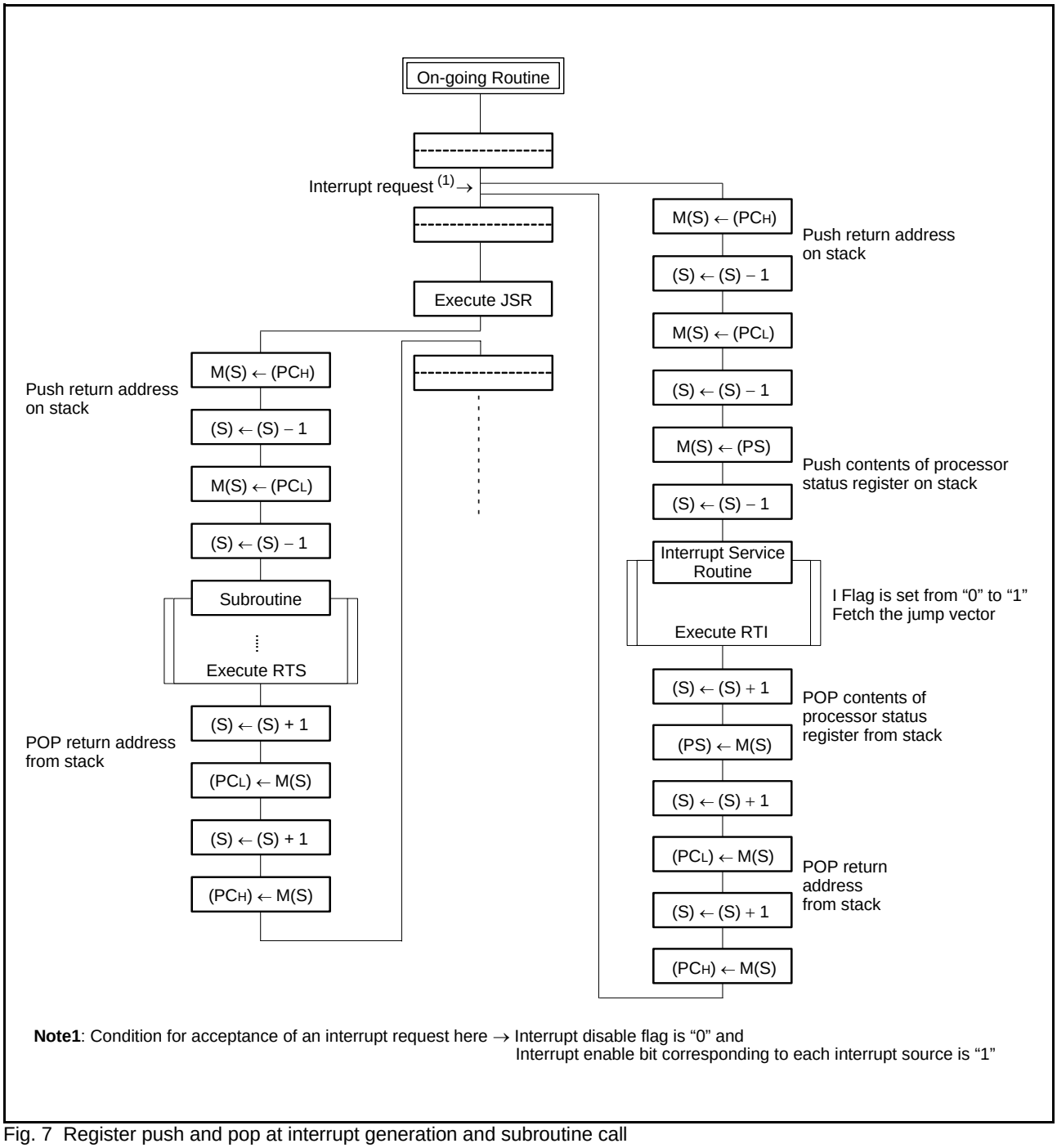


Fig. 7 Register push and pop at interrupt generation and subroutine call

Table 7 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor Status Register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

- Bit 0: Carry flag (C)
  The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.
- Bit 1: Zero flag (Z)
  The Z flag is set to "1" if the result of an immediate arithmetic operation or a data transfer is "0", and set to "0" if the result is anything other than "0".
- Bit 2: Interrupt disable flag (I)
  The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
  Interrupts are disabled when the I flag is "1".
- Bit 3: Decimal mode flag (D)
  The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".
  Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.
- Bit 4: Break flag (B)
  The B flag is used to indicate that the current interrupt was generated by the BRK instruction. When the BRK instruction is generated, the B flag is set to "1" automatically. When the other interrupts are generated, the B flag is set to "0", and the processor status register is pushed onto the stack.
- Bit 5: Index X mode flag (T)
  When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.
- Bit 6: Overflow flag (V)
  The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.
- Bit 7: Negative flag (N)
  The N flag is set to "1" if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 8 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

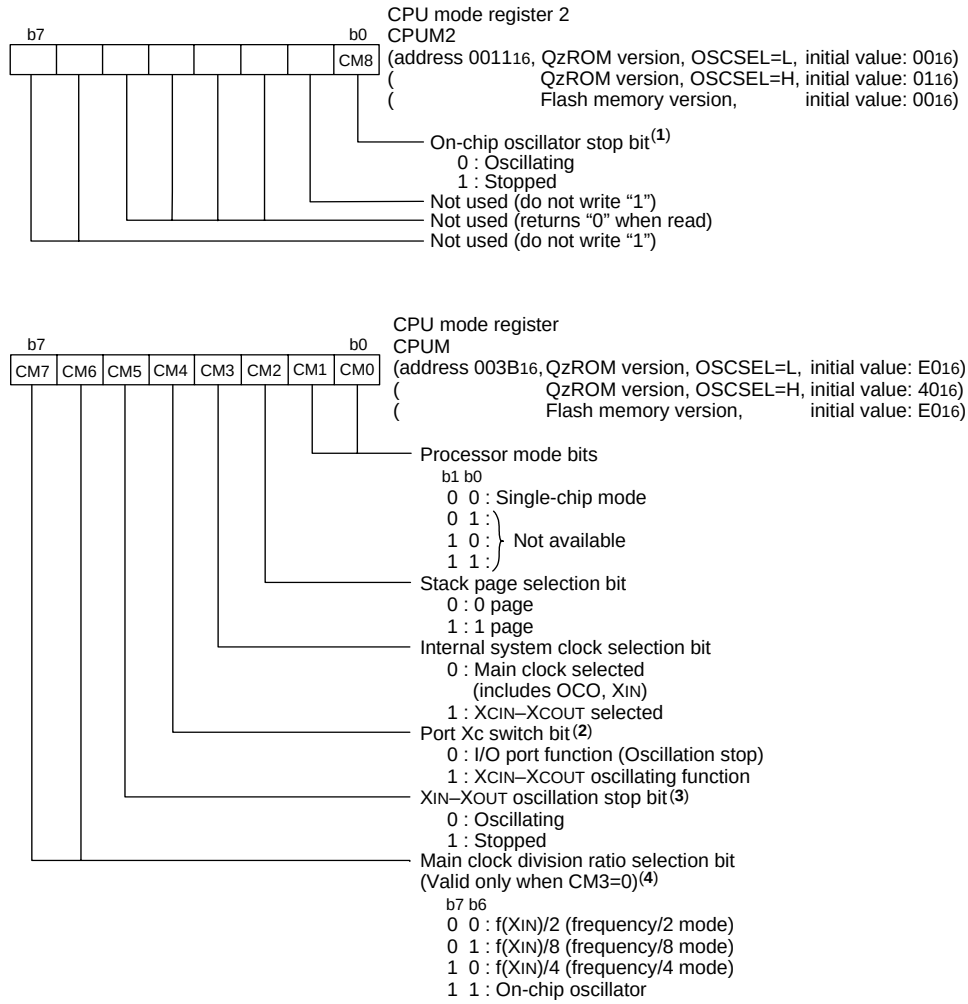
[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit, etc. This register is allocated at address 003B16.
After the system is released from reset, the mode depends on the OSCSEL pin state in the QzROM version.
When the OSCSEL pin state is GND level, only the on-chip oscillator starts oscillation. The XIN-XOUT oscillation stops oscillating, and XCIN and XCOUT pins function as I/O ports. The operating mode is the on-chip oscillator mode.
When the OSCSEL pin state is Vcc level, the XIN-XOUT oscillation divided by 8 starts oscillation. The on-chip oscillator stops oscillating, and the XCIN and XCOUT pins function as I/O ports. The operating mode is the frequency/8 mode.

In the flash memory version, only the on-chip oscillator starts oscillating. The XIN-XOUT oscillation stops oscillating, and the XCIN and XCOUT pins function as I/O ports. The operating mode is the on-chip oscillator mode.
When the main clock or sub-clock is used, after the XIN-XOUT oscillation and the XCIN-XCOUT oscillation are enabled, wait in the on-chip oscillator mode etc. until the oscillation stabilizes, and then switch the operation mode.
When the main clock is not used (XIN-XOUT oscillation and an external clock input are not used), connect the XIN pin to VCC through a resistor and leave XOUT open.

[CPU Mode Register 2 (CPUM2)] 001116

The CPU mode register 2 contains the control bits for the on-chip oscillator.
The CPU mode register 2 is allocated at address 001116.



Notes 1: When the on-chip oscillator is selected by the watchdog timer count source selection bit 2 (bit 5 of watchdog timer control register (address 002916)), the on-chip oscillator does not stop even when the on-chip oscillator stop bit is set to "1".
Also, when the low-speed mode is set, the on-chip oscillator stops regardless of the value of this bit in the QzROM version. The on-chip oscillator does not stop in the flash memory version, so set this bit to "1" to stop the oscillation.
In on-chip oscillator mode, even if this bit is set to "1", the on-chip oscillator does not stop in the flash memory version, but stops in the QzROM version.
2: In low-speed mode, the XCIN-XCOUT oscillation stops if the port XC switch bit is set to "0".
3: In XIN mode, the XIN-XOUT oscillation does not stop even if the XIN-XOUT oscillation stop bit is set to "1".
4: 12.5 MHz < f(XIN) ≤ 16 MHz is not available in the frequency/2 mode.

Fig. 8 Structure of CPU mode register

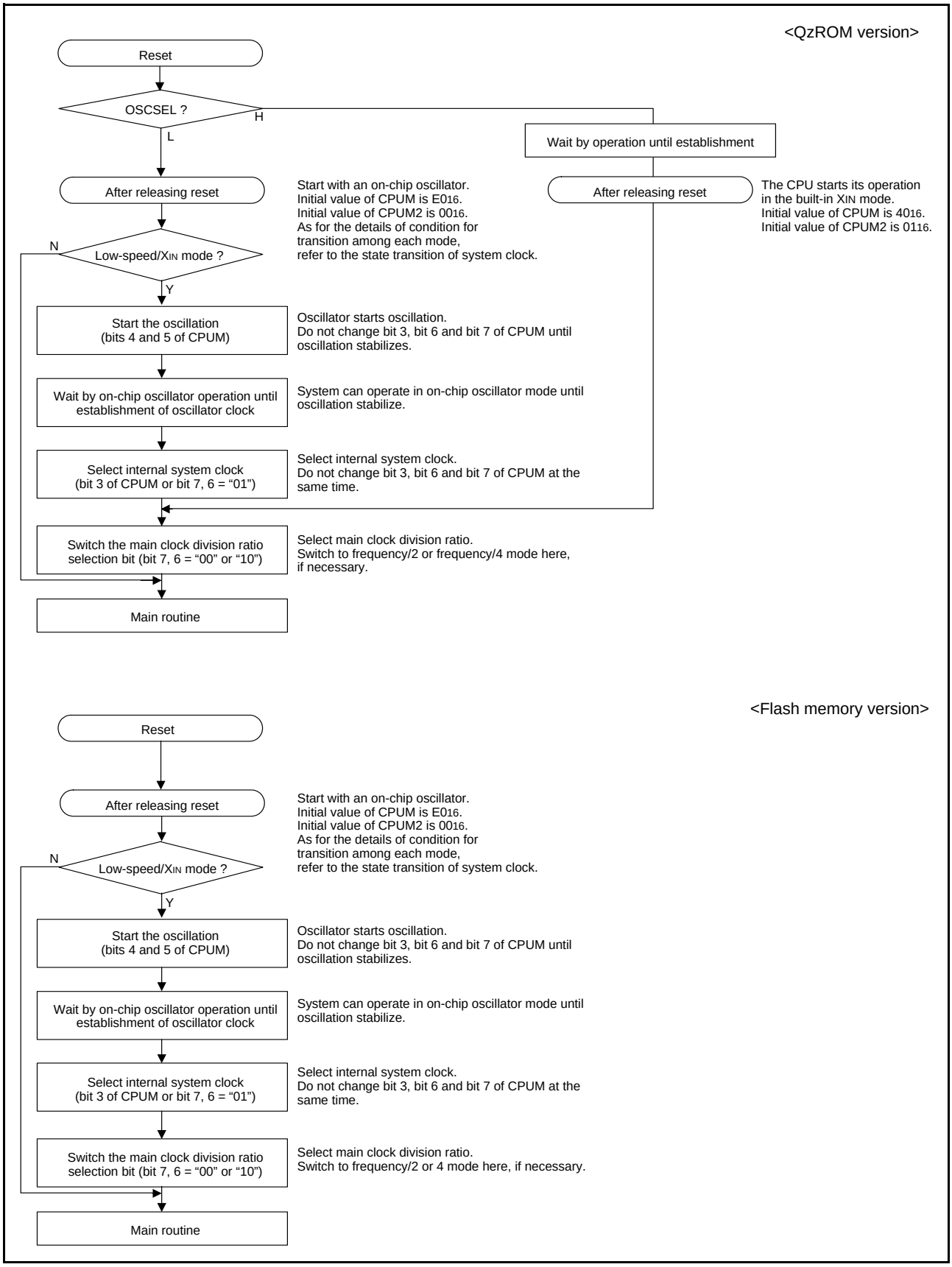


Fig. 9 Switch procedure of CPU mode register

MEMORY

• Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

• RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

• ROM

In the QzROM version, the first 128 Kbytes and the last 2 bytes are reserved for device testing and the rest is the user area. Also, 1 byte of address FFDB16 is reserved.
In the flash memory version, programming and erase operations can be performed to reserved ROM areas.

• Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

• Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

• Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

• ROM Code Protect Address in QzROM Version (Address FFDB16)

Address FFDB16 as reserved ROM area in the QzROM version is ROM code protect address. "0016" or "FE16" is written into this address when selecting the protect bit write by using a serial programmer and selecting protect enabled for writing shipment by Renesas Technology Corp. When "0016" or "FE16" is set to the ROM code protect address, the protect function is enabled, so that reading or writing from/to the corresponding area is disabled by a serial programmer.
As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.
The protect can be performed, dividing twice. The protect area 1 is from the beginning address of ROM to address "EFFF16".
As for the QzROM product shipped after writing, "0016" (protect enabled to all area), "FE16" (protect enabled to the protect area 1) or "FF16" (protect disabled) is written into the ROM code protect address when Renesas Technology Corp. performs writing. The writing of "0016", "FE16" or "FF16" can be selected as ROM option setup ("MASK option" written in the mask file converter) when ordering.
For the ROM code protect in the flash memory version, refer to the "FLASH MEMORY MODE".

<Notes>

- After a reset, the contents of RAM are undefined. Make sure to set the initial value before use.
- When Renesas ships QzROM write products, we write ROM option data* specified by the mask file converter MM to the ROM code protect address. Therefore, set FF16 to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than FF16 is set, we may ask that the ROM data be submitted again.

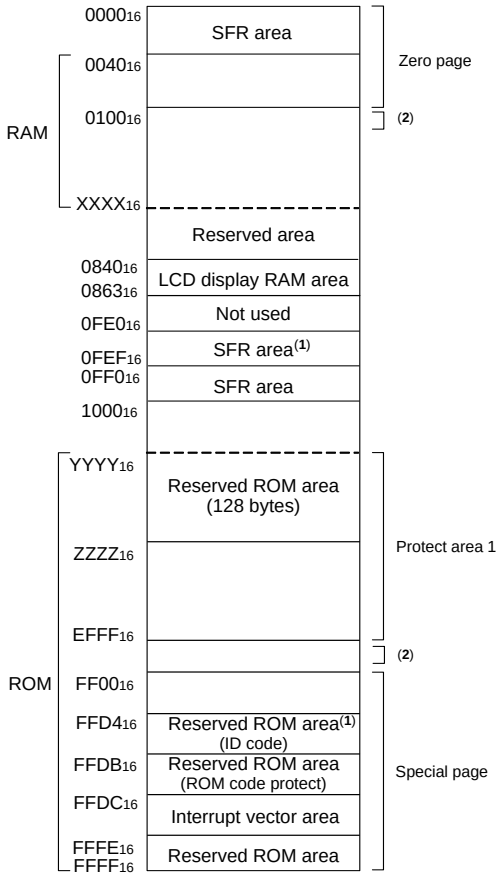
* ROM option data: mask option noted in MM

RAM area

RAM size (bytes)	Address XXXX16
192	00FF16
256	013F16
384	01BF16
512	023F16
640	02BF16
768	033F16
896	03BF16
1024	043F16
1536	063F16
2048	083F16

ROM area

ROM size (bytes)	Address YYYY16	Address ZZZZ16
4096	F00016	F08016
8192	E00016	E08016
12288	D00016	D08016
16384	C00016	C08016
20480	B00016	B08016
24576	A00016	A08016
28672	900016	908016
32768	800016	808016
36864	700016	708016
40960	600016	608016
45056	500016	508016
49152	400016	408016
53248	300016	308016
57344	200016	208016
61440	100016	108016



Note 1: This area is available in the flash memory version only.
2: ROM correction vectors are assigned. As for the details, refer to the “ROM CORRECTION FUNCTION”.
3: In the flash memory version, programming and erase operations can be performed to reserved ROM areas. Note that their areas are different from those in the QzROM version.

Fig. 10 Memory map diagram

0000₁₆	Port P0 (P0)
0001₁₆	Port P0 direction register (P0D)
0002₁₆	Port P1 (P1)
0003₁₆	Port P1 direction register (P1D)
0004₁₆	Port P2 (P2)
0005₁₆	Port P2 direction register (P2D)
0006₁₆	Port P3 (P3)
0007₁₆	Port P3 direction register (P3D)
0008₁₆	Port P4 (P4)
0009₁₆	Port P4 direction register (P4D)
000A₁₆	Port P5 (P5)
000B₁₆	Port P5 direction register (P5D)
000C₁₆	Port P6 (P6)
000D₁₆	Port P6 direction register (P6D)
000E₁₆	Port P7 (P7)
000F₁₆	Port P7 direction register (P7D)
0010₁₆	
0011₁₆	CPU mode register 2 (CPUM2)
0012₁₆	RRF register (RRFR)
0013₁₆	LCD mode register1 (LM1)
0014₁₆	LCD mode register2 (LM2)
0015₁₆	AD control register (ADCON)
0016₁₆	AD conversion register (low-order) (ADL)
0017₁₆	AD conversion register (high-order) (ADH)
0018₁₆	Transmit/receive buffer register 1 (TB1/RB1)
0019₁₆	Serial I/O1 status register (SIO1STS)
001A₁₆	Serial I/O1 control register (SIO1CON)
001B₁₆	UART control register (UARTCON)
001C₁₆	Baud rate generator (BRG)
001D₁₆	Serial I/O2 control register (SIO2CON)
001E₁₆	Reserved (1)
001F₁₆	Serial I/O2 register (SIO2)

0020₁₆	Timer 1 (T1)
0021₁₆	Timer 2 (T2)
0022₁₆	Timer 3 (T3)
0023₁₆	Timer 4 (T4)
0024₁₆	PWM01 register (PWM01)
0025₁₆	Timer 12 mode register (T12M)
0026₁₆	Timer 34 mode register (T34M)
0027₁₆	Timer 1234 mode register (T1234M)
0028₁₆	Timer 1234 frequency division selection register (PRE1234)
0029₁₆	Watchdog timer control register (WDTCON)
002A₁₆	Timer X (low-order) (TXL)
002B₁₆	Timer X (high-order) (TXH)
002C₁₆	Timer X (extension) (TXEX)
002D₁₆	Timer X mode register (TXM)
002E₁₆	Timer X control register 1 (TXCON1)
002F₁₆	Timer X control register 2 (TXCON2)
0030₁₆	Compare register 1 (low-order) (COMP1L)
0031₁₆	Compare register 1 (high-order) (COMP1H)
0032₁₆	Compare register 2 (low-order) (COMP2L)
0033₁₆	Compare register 2 (high-order) (COMP2H)
0034₁₆	Compare register 3 (low-order) (COMP3L)
0035₁₆	Compare register 3 (high-order) (COMP3H)
0036₁₆	Timer Y (low-order) (TYL)
0037₁₆	Timer Y (high-order) (TYH)
0038₁₆	Timer Y mode register (TYM)
0039₁₆	Timer Y control register (TYCON)
003A₁₆	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)
003C₁₆	Interrupt request register 1 (IREQ1)
003D₁₆	Interrupt request register 2 (IREQ2)
003E₁₆	Interrupt control register 1 (ICON1)
003F₁₆	Interrupt control register 2 (ICON2)

0FE0₁₆	Flash memory control register 0 (FMCR0)
0FE1₁₆	Flash memory control register 1 (FMCR1)
0FE2₁₆	Flash memory control register 2 (FMCR2)
0FE3₁₆	Reserved (1)
0FE4₁₆	Reserved (1)
0FE5₁₆	Reserved (1)
0FE6₁₆	Reserved (1)
0FE7₁₆	Reserved (1)
0FE8₁₆	Reserved (1)
0FE9₁₆	Reserved (1)
0FEA₁₆	Reserved (1)
0FEB₁₆	Reserved (1)
0FEC₁₆	Reserved (1)
0FED₁₆	Reserved (1)
0FEE₁₆	Reserved (1)
0FEF₁₆	Reserved (1)

0FF0₁₆	PULL register 1 (PULL1)
0FF1₁₆	PULL register 2 (PULL2)
0FF2₁₆	PULL register 3 (PULL3)
0FF3₁₆	Clock output control register (CKOUT)
0FF4₁₆	Segment output disable register 0 (SEG0)
0FF5₁₆	Segment output disable register 1 (SEG1)
0FF6₁₆	Segment output disable register 2 (SEG2)
0FF7₁₆	Key input control register (KIC)
0FF8₁₆	ROM correction address 1 high-order register (RCA1H)
0FF9₁₆	ROM correction address 1 low-order register (RCA1L)
0FFA₁₆	ROM correction address 2 high-order register (RCA2H)
0FFB₁₆	ROM correction address 2 low-order register (RCA2L)
0FFC₁₆	ROM correction enable register (RCR)
0FFD₁₆	Reserved (1)
0FFE₁₆	Reserved (1)
0FFF₁₆	Reserved (1)

Note 1: The blanks are reserved. Do not write data to these areas.
2: No memory access is allowed to the blank areas within the SFRs.
3: Addresses 0FE0₁₆ to 0FEF₁₆ are available in the flash memory version only.

Fig. 11 Memory map of special function register (SFR)

I/O PORTS

• Direction Registers (Ports P0-P6, P72-P74)

The I/O ports P0-P6, P72-P74 have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.

When "0" is written to the bit of the direction register, the corresponding pin becomes an input pin. As for ports P0–P3, when "1" is written to the bit of the direction register and the segment output disable register, the corresponding pin becomes an output pin. As for ports P4–P6, P72-P74 when "1" is written to the bit of the direction register, the corresponding pin becomes an output pin.

If data is read from a pin set to output, the value of the port latch is read, not the value of the pin itself. However, when peripheral output (RTP1, RTP0, TXOUT1, TXOUT2, T4OUT, T3OUT and T2OUT/CKOUT) is selected, the output value is read. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

• Ports P70, P71

These are input ports which are shared with the voltage multiplier. When these are read out at using the voltage multiplier, the contents are "1".

• Pull-up Control

Each individual bit of ports P0–P3 can be pulled up with a program by setting direction registers and segment output disable registers 0 to 2 (addresses 0FF416 to 0FF616).

The pin is pulled up by setting "0" to the direction register and "1" to the segment output disable register.

By setting the PULL registers (addresses 0FF016 to OFF216), ports P4–P7 can control pull-up with a program.

However, the contents of PULL register do not affect ports programmed as the output ports.

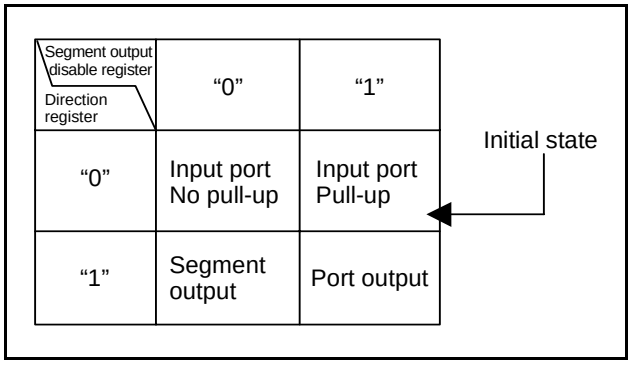
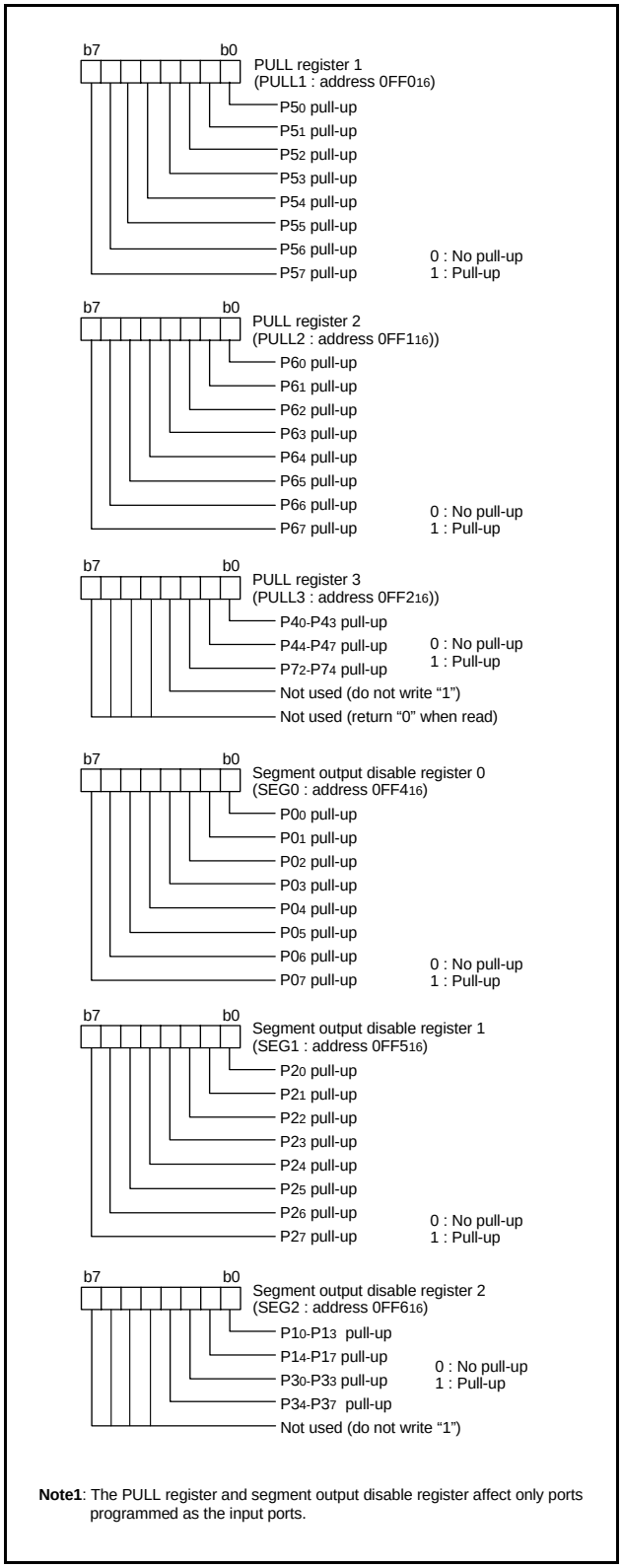


Fig. 12 Structure of ports P0 to P3



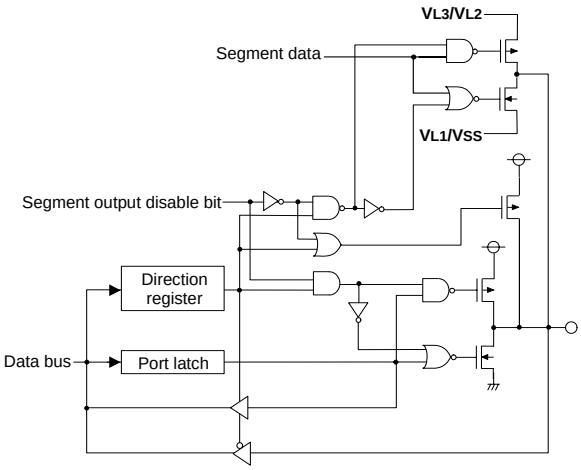
Note1: The PULL register and segment output disable register affect only ports programmed as the input ports.

Fig. 13 Structure of PULL register and segment output disable register

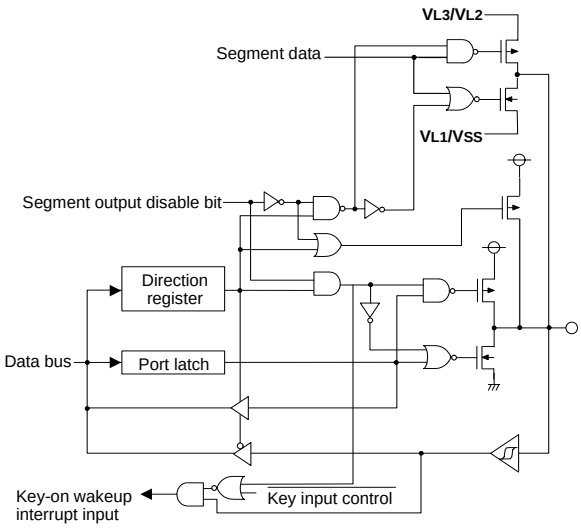
Table 9 List of I/O port function

Pin	Name	Input/Output	I/O format	Non-port function		Related SFRs	Ref. No.
P0$_0$/SEG$_8$– P0$_7$/SEG$_{15}$	Port P0	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	LCD segment output		Segment output disable register 0	(1)
P1$_0$/SEG$_{16}$– P1$_7$/SEG$_{23}$	Port P1	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output			Segment output disable register 2	
P2$_0$/SEG$_0$/(KW$_4$)– P2$_3$/SEG$_3$/(KW$_7$)	Port P2	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output		Key input (key-on wakeup) interrupt input	Segment output disable register 1 Key input control register	(2)
P2$_4$/SEG$_4$– P2$_7$/SEG$_7$						Segment output disable register 1	(1)
P3$_0$/SEG$_{24}$– P3$_7$/SEG$_{31}$	Port P3	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output			Segment output disable register 2	
P4$_0$/RxD P4$_1$/TxD P4$_2$/SCLK$_1$, P4$_3$/$\overline{\text{SRDY}_1}$	Port P4	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O1 function I/O		PULL register 3 Serial I/O1 control register Serial I/O1 status register UART control register	(3) (4) (5) (6)
P4$_4$/SIN$_2$/(KW$_0$) P4$_5$/SOUT$_2$/(KW$_1$) P4$_6$/SCLK$_2$/(KW$_2$) P4$_7$/$\overline{\text{SRDY}_2}$/(KW$_3$)				Serial I/O2 function I/O	Key input (key-on wakeup) interrupt input	PULL register 3 Serial I/O2 control register Serial I/O2 register Key input control register	(7) (8) (9) (10)
P5$_0$/AN$_0$/RTP$_0$ P5$_1$/AN$_1$/RTP$_1$	Port P5	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	A/D conversion input	Real time port function output	PULL register 1 AD control register Timer Y mode register	(11)
P5$_2$/AN$_2$– P5$_6$/AN$_6$						PULL register 1 AD control register	(12)
P5$_7$/AN$_7$/ADKEY$_0$					ADKEY input		(13)
P6$_0$/XCIN P6$_1$/XCOUT	Port P6	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Sub-clock oscillation circuit		PULL register 2 CPU mode register	(14) (15)
P6$_2$/INT$_{00}$/(LED$_0$)				External interrupt input		PULL register 2 Interrupt edge selection register	(16)
P6$_3$/TXOUT$_2$/(LED$_1$)				Timer X output 2		PULL register 2 Timer X mode register Timer X control registers 1,2	(18)
P6$_4$/INT$_2$/(LED$_2$)				External interrupt input		PULL register 2 Interrupt edge selection register	(17)
P6$_5$/TXOUT$_1$/(LED$_3$)				Timer X output 1		PULL register 2 Timer X mode register Timer X control register 1	(18)
P6$_6$/INT$_{10}$/CNTR$_0$/ (LED$_4$)				Timer X function input External interrupt input		PULL register 2 Interrupt edge selection register Timer X mode register Timer X control registers 1,2	(19)
P6$_7$/CNTR$_1$/(LED$_5$)				Timer Y function input		PULL register 2 Timer Y mode register	(17)
P7$_0$/C$_1$/INT$_{01}$ P7$_1$/C$_2$/INT$_{11}$	Port P7	Input, individual bits	CMOS compatible input level	External interrupt input LCD voltage multiplier input		Interrupt edge selection register LCD mode registers 1,2	(20)
P7$_2$/T$_{2OUT}$/ CKOUT P7$_3$/PWM$_0$/T$_{3OUT}$ P7$_4$/PWM$_1$/T$_{4OUT}$		Input/Output individual bits	CMOS compatible input level CMOS 3-state output	Timer 2 output Timer 3 output Timer 4 output	clock output PWM output	PULL register 3 Timer 1234 mode register Timer 1234 frequency division register Clock output control register	(21)
COM$_0$ –COM$_3$	Common	Output	LCD common output	LCD common output		LCD mode register 1,2	(22)
COM$_4$/SEG$_{35}$– COM$_7$/SEG$_{32}$	Common /Segment		LCD common/Segment output		LCD Segment output		(23)

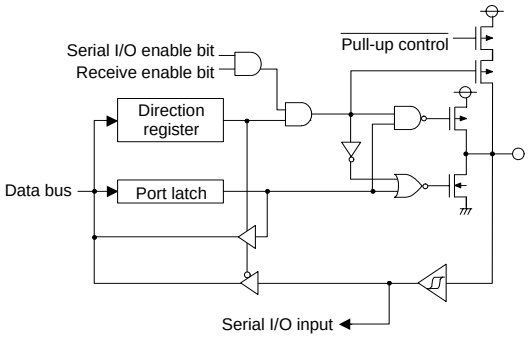
(1) Ports P0, P1, P2$_4$-P2$_7$, P3



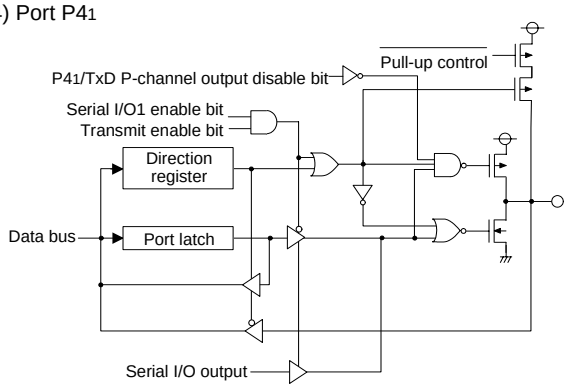
(2) Ports P2$_0$-P2$_3$



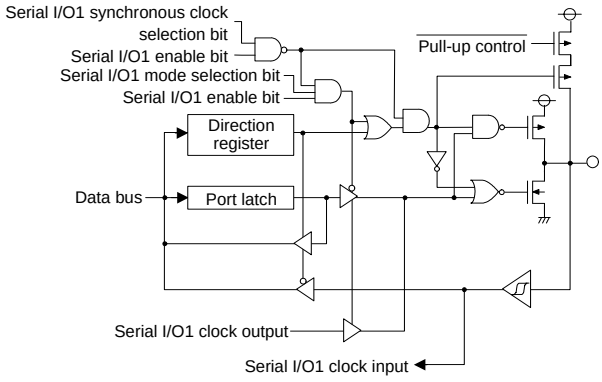
(3) Port P4$_0$



(4) Port P4$_1$



(5) Port P4$_2$



(6) Port P4$_3$

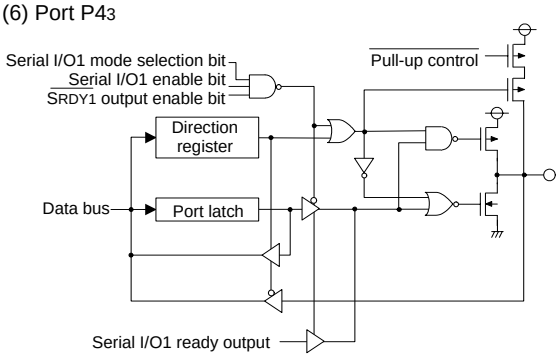
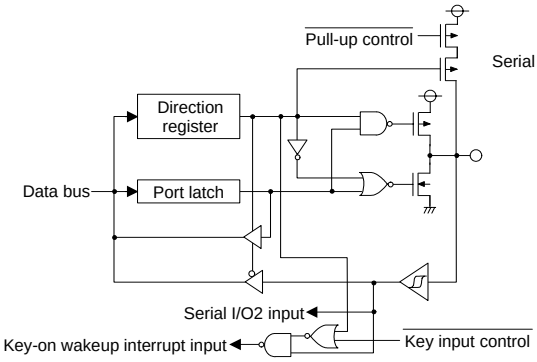
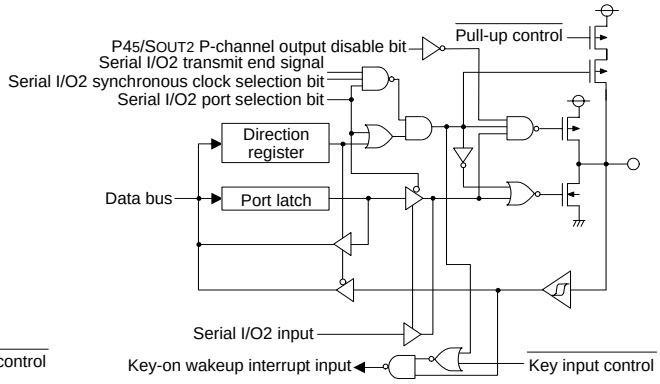


Fig. 14 Port block diagram (1)

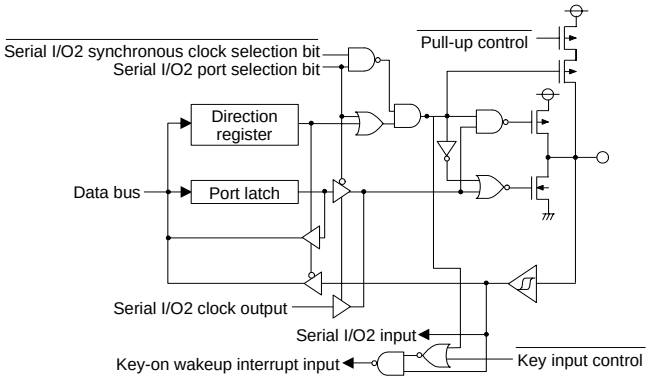
(7) Port P44



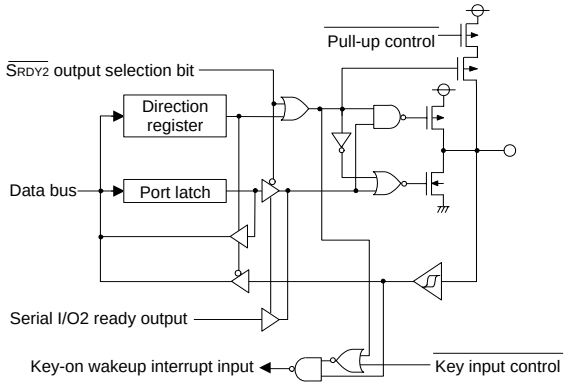
(8) Port P45



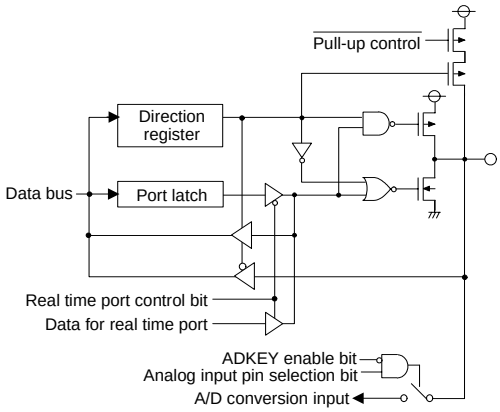
(9) Port P46



(10) Port P47



(11) Ports P50, P51



(12) Ports P52-P56

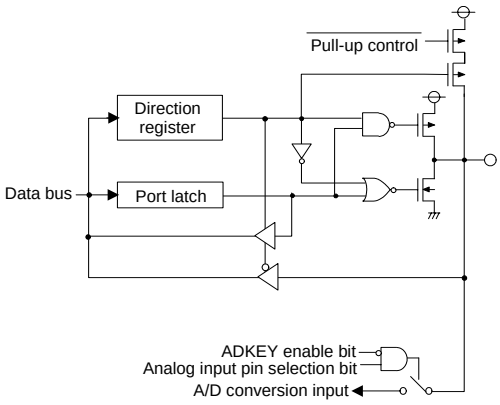
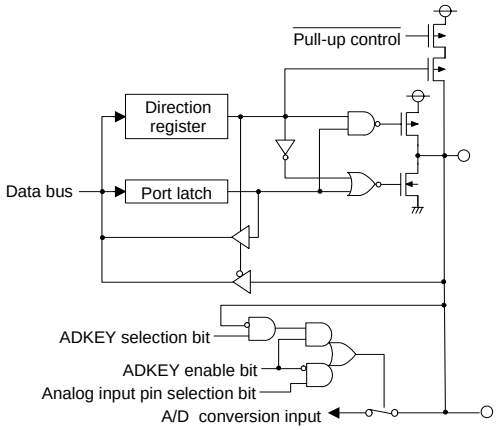
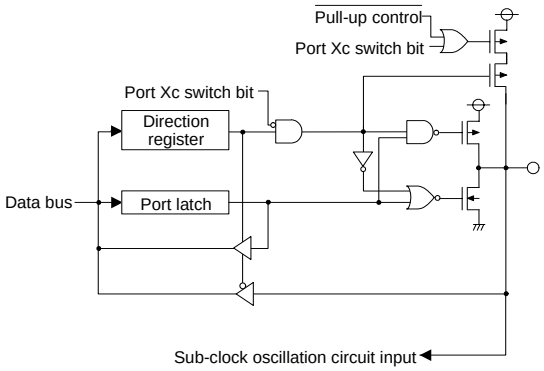


Fig. 15 Port block diagram (2)

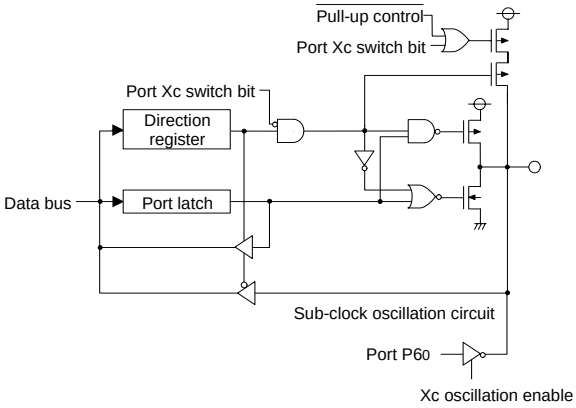
(13) Port P5$_7$



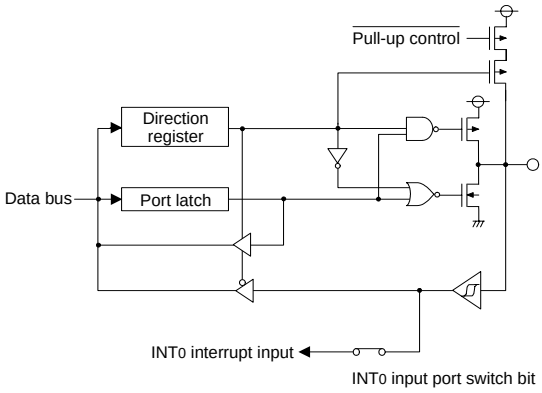
(14) Port P6$_0$



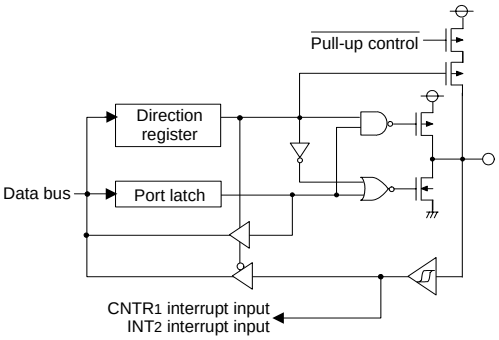
(15) Port P6$_1$



(16) Port P6$_2$



(17) Ports P6$_4$, P6$_7$



(18) Ports P6$_3$, P6$_5$

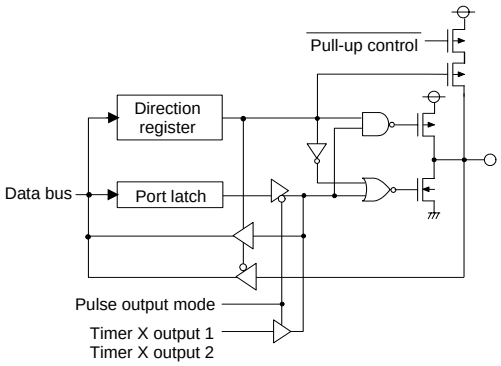


Fig. 16 Port block diagram (3)

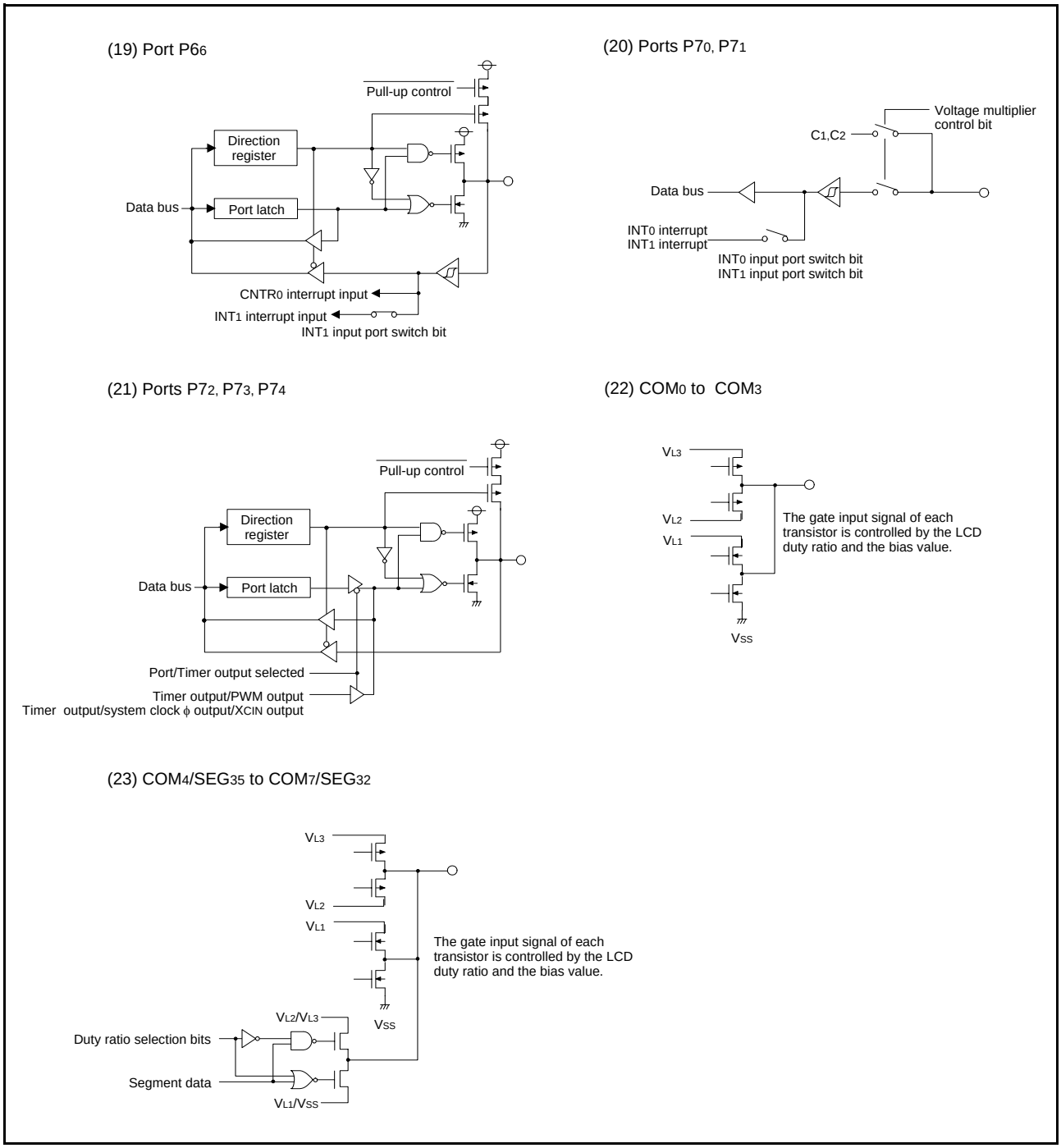


Fig. 17 Port block diagram (4)

• Termination of unused pins

• Termination of common pins

I/O ports: Select an input port or an output port and follow each processing method.
In addition, it is recommended that related registers be overwritten periodically to prevent malfunctions, etc.

Output ports: Open.

Input ports: If the input level become unstable, through current flow to an input circuit, and the power supply current may increase.
Especially, when expecting low consumption current (at STP or WIT instruction execution etc.), pull-up or pull-down input ports to prevent through current (built-in resistor can be used).
We recommend processing unused pins through a resistor which can secure $I_{OH(avg)}$ or $I_{OL(avg)}$.
Because, when an I/O port or a pin which have an output function is selected as an input port, it may operate as an output port by incorrect operation etc.

Table 10 Termination of unused pins

Pin	Termination 1	Termination 2	Termination 3
P0$_0$/SEG$_8$–P0$_7$/SEG$_{15}$	I/O port	When selecting SEG output, open.	–
P1$_0$/SEG$_{16}$–P1$_7$/SEG$_{23}$			
P2$_0$/SEG$_0$/(KW$_4$)–P2$_7$/SEG$_7$			
P3$_0$/SEG$_{24}$–P3$_7$/SEG$_{31}$			
P4$_0$/RxD		When selecting RxD function, perform termination of input port.	–
P4$_1$/TxD		When selecting TxD function, perform termination of output port.	–
P4$_2$/SCLK1		When selecting external clock input, perform termination of input port.	When selecting internal clock output, perform termination of output port.
P4$_3$/$\overline{\text{SRDY1}}$		When selecting $\overline{\text{SRDY1}}$ function, perform termination of output port.	–
P4$_4$/SIN2/(KW$_0$)		When selecting SIN2 function, perform termination of input port.	–
P4$_5$/SOUT2/(KW$_1$)		When selecting SOUT2 function, perform termination of output port.	–
P4$_6$/SCLK2/(KW$_2$)		When selecting external clock input, perform termination of output port.	When selecting internal clock output, perform termination of output port.
P4$_7$/$\overline{\text{SRDY2}}$/(KW$_3$)		When selecting SRDY2 function, perform termination of output port.	–
P5$_0$/AN$_0$/RTP$_0$ P5$_1$/AN$_1$/RTP$_1$		When selecting AN function, these pins can be opened. (A/D conversion result cannot be guaranteed.)	When selecting RTP function, perform termination of output port.
P5$_2$/AN$_2$–P5$_6$/AN$_6$			–
P5$_7$/AN$_7$/ADKEY$_0$			When selecting ADKEY function, pull-up this pin through a resistor.
P6$_0$/XCIN P6$_1$/XCOUT		Do not select XCIN–XCOUT oscillation function by program.	–
P6$_2$/INT$_{00}$/(LED$_0$)		When selecting INT function, perform termination of input port.	–
P6$_3$/TXOUT2/(LED$_1$)		When selecting TXOUT function, perform termination of output port.	–
P6$_4$/INT$_2$/(LED$_2$)		When selecting INT function, perform termination of input port.	–
P6$_5$/TXOUT1/(LED$_3$)		When selecting TXOUT function, perform termination of output port.	–
P6$_6$/INT$_{10}$/CNTR$_0$/(LED$_4$)		When selecting CNTR input function or INT function, perform termination of input port.	–
P6$_7$/CNTR$_1$/(LED$_5$)		When selecting CNTR input function, perform termination of input port.	–
P7$_0$/C$_1$/INT$_{01}$ P7$_1$/C$_2$/INT$_{11}$	Disable the voltage multiplier, and connect to VSS through a resistor.	When selecting INT function, disable the voltage multiplier, and connect to VSS through a resistor.	–
P7$_2$/T2OUT/CKOUT	I/O port	When selecting T2OUT function or CKOUT function, perform termination of output port.	–
P7$_3$/PWM$_0$/T3OUT P7$_4$/PWM$_1$/T4OUT		When selecting PWM, T3OUT, or T4OUT function, perform termination of output port.	–
VL3	Set the VL3 connect bit to “1” and apply a Vcc level voltage to VL3 pin.	Set the VL3 connect bit to “0” and leave the VL3 pin open.	–
VL2	VL3 ≥ VL2 ≥ VL1	–	–
VL1	Connect to VSS	–	–
COM$_0$–COM$_3$	Open	–	–
COM$_4$/SEG$_{35}$–COM$_7$/SEG$_{32}$	Open	–	–
VREF	Connect to VCC	–	–
XIN	When only on-chip oscillator is used, connect to VCC through a resistor.	–	–
XOUT	When external clock is input or when only on-chip oscillator is used, open.	–	–

INTERRUPTS

The 38D5 Group interrupts are vector interrupts with a fixed priority scheme, and generated by 16 sources among 17 sources: 6 external, 10 internal, and 1 software.
The interrupt sources, vector addresses(1), and interrupt priority are shown in Table 11.

Each interrupt except the BRK instruction interrupt has the interrupt request bit and the interrupt enable bit. These bits and the interrupt disable flag (I flag) control the acceptance of interrupt requests. Figure 18 shows an interrupt control diagram.

An interrupt requests is accepted when all of the following conditions are satisfied:

- Interrupt disable flag ..... "0"
- Interrupt request bit ..... "1"
- Interrupt enable bit ..... "1"

Though the interrupt priority is determined by hardware, priority processing can be performed by software using the above bits and flag.

Table 11 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses(1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset(2)	1	FFFD16	FFFC16	At reset	Non-maskable
INT0 (INT00 or INT01)(3)	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
INT1 (INT10 or INT11)(3)	3	FFF916	FFF816	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
INT2	4	FFF716	FFF616	At detection of either rising or falling edge of INT2 input	Valid when INT2 interrupt is selected External interrupt (active edge selectable)
Key input (key-on wakeup)	5	FFF516	FFF416	At falling of ports P20–P23, P44–P47 input logical level AND	Valid when Key input interrupt is selected External interrupt (falling valid)
Timer X	6	FFF316	FFF216	At timer X underflow	
Timer 1	7	FFF116	FFF016	At timer 1 underflow	
Timer 2	8	FFEF16	FFEE16	At timer 2 underflow	
Timer 3	9	FFED16	FFEC16	At timer 3 underflow	
Timer 4	10	FFEB16	FFEA16	At timer 4 underflow	
Serial I/O1 receive	11	FFE916	FFE816	At completion of serial I/O1 data receive	Valid only when serial I/O1 is selected
Serial I/O1 transmit	12	FFE716	FFE616	At completion of serial I/O1 transmit shift or transmit buffer is empty	Valid only when serial I/O1 is selected
Serial I/O2	13	FFE516	FFE416	At completion of serial I/O2 data transmit/receive	
CNTR0	14	FFE316	FFE216	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
Timer Y	15	FFE116	FFE016	At timer Y underflow	
CNTR1				At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
A/D conversion	16	FFDF16	FFDE16	At completion of A/D conversion	
BRK instruction	17	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

NOTES:
1. Vector addresses contain interrupt jump destination addresses.
2. Reset function in the same way as an interrupt with the highest priority.
3. INT0, and INT1 input pins are selected by the interrupt edge selection register (INTEDGE).

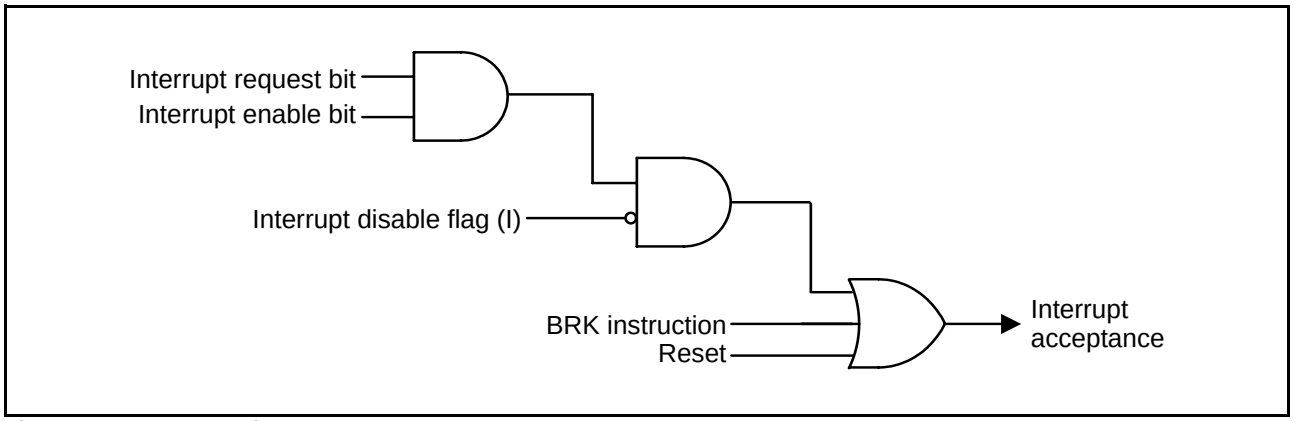


Fig. 18 Interrupt control

• Interrupt Disable Flag

The interrupt disable flag is assigned to bit 2 of the processor status register. This flag controls the acceptance of all interrupt requests except for the BRK instruction. When this flag is set to "1", the acceptance of interrupt requests is disabled. When it is set to "0", acceptance of interrupt requests is enabled. This flag is set to "1" with the SEI instruction and set to "0" with the CLI instruction.

When an interrupt request is accepted, the contents of the processor status register are pushed onto the stack while the interrupt disable flag remains set to "0". Subsequently, this flag is automatically set to "1" and multiple interrupts are disabled.

To use multiple interrupts, set this flag to "0" with the CLI instruction within the interrupt processing routine.

The contents of the processor status register are popped off the stack with the RTI instruction.

• Interrupt Request Bits

Once an interrupt request is generated, the corresponding interrupt request bit is set to "1" and remains "1" until the request is accepted. When the request is accepted, this bit is automatically set to "0".

Each interrupt request bit can be set to "0", but cannot be set to "1", by software.

• Interrupt Enable Bits

The interrupt enable bits control the acceptance of the corresponding interrupt requests. When an interrupt enable bit is set to "0", the acceptance of the corresponding interrupt request is disabled. If an interrupt request occurs in this condition, the corresponding interrupt request bit is set to "1", but the interrupt request is not accepted. When an interrupt enable bit is set to "1", acceptance of the corresponding interrupt request is enabled.

Each interrupt enable bit can be set to "0" or "1" by software.

The interrupt enable bit for an unused interrupt should be set to "0".

• Interrupt Source Selection

Any of the following combinations can be selected by the interrupt edge selection register ($003A_{16}$).

- Timer Y or $CNTR_1$

• External Interrupt Pin Selection

For external interrupts INT_0 and INT_1, the INT_0, INT_1 input port switch bit in the interrupt edge selection register (bits 4 and 5 of address $003A_{16}$) can be used to select INT_{00} and INT_{01} pin input or INT_{10} and INT_{11} pin input.

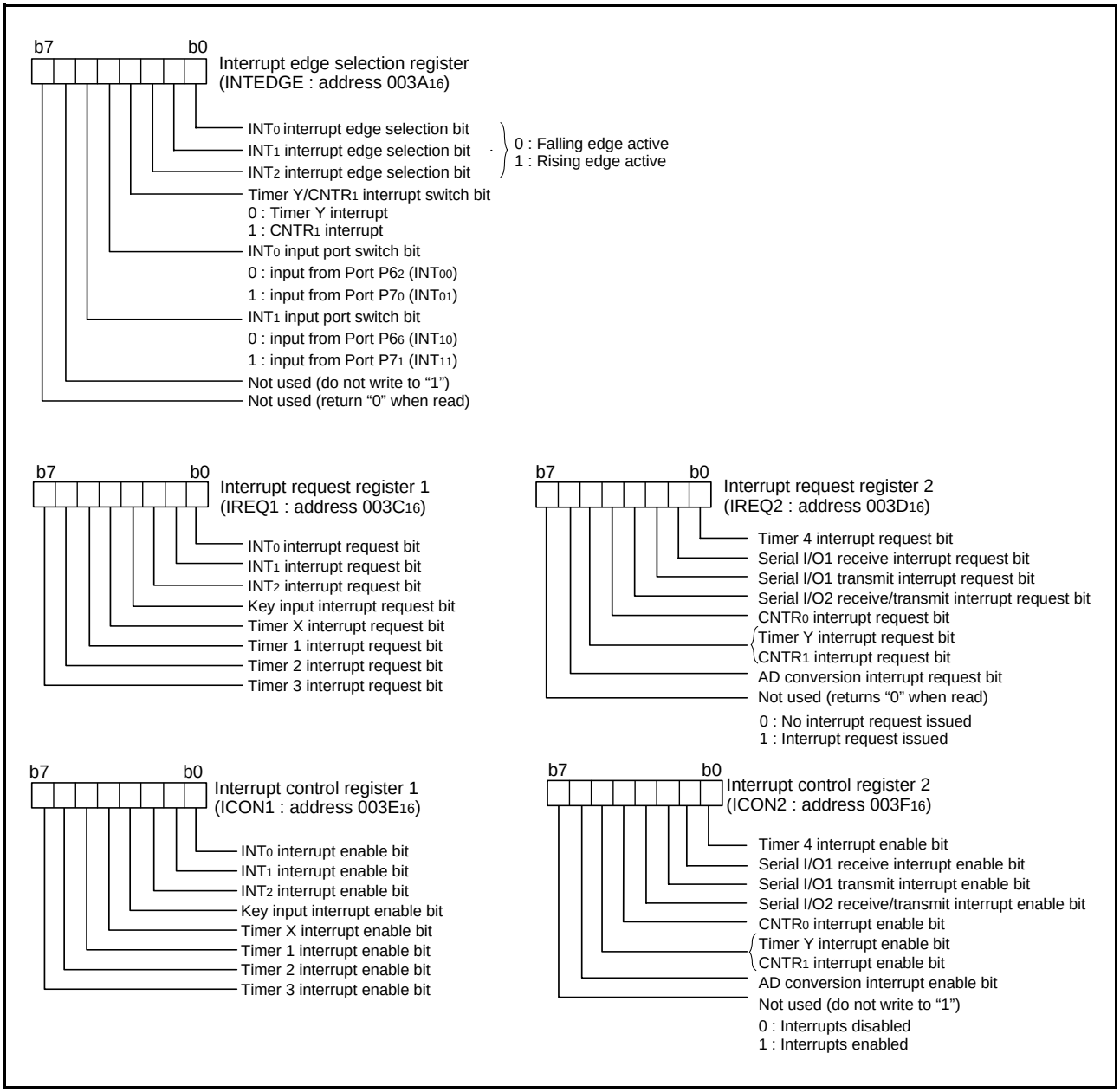


Fig. 19 Structure of interrupt-related registers

• Interrupt Request Generation, Acceptance, and Handling

Interrupts have the following three phases.

(i) Interrupt Request Generation
An interrupt request is generated by an interrupt source (external interrupt signal input, timer underflow, etc.) and the corresponding request bit is set to "1".

(ii) Interrupt Request Acceptance
Based on the interrupt acceptance timing in each instruction cycle, the interrupt control circuit determines acceptance conditions (interrupt request bit, interrupt enable bit, and interrupt disable flag) and interrupt priority levels for accepting interrupt requests. When two or more interrupt requests are generated simultaneously, the highest priority interrupt is accepted. The value of interrupt request bit for an unaccepted interrupt remains the same and acceptance is determined at the next interrupt acceptance timing point.

(iii) Handling of Accepted Interrupt Request
The accepted interrupt request is processed.

Figure 20 shows the time up to execution in the interrupt routine, and Figure 21 shows the interrupt sequence.
Figure 22 shows the timing of interrupt request generation, interrupt request bit, and interrupt request acceptance.

• Interrupt Handling Execution

When interrupt handling is executed, the following operations are performed automatically.

(1) Once the currently executing instruction is completed, an interrupt request is accepted.

(2) The contents of the program counters and the processor status register at this point are pushed onto the stack area in order from 1 to 3.
1. High-order bits of program counter (PCH)
2. Low-order bits of program counter (PCL)
3. Processor status register (PS)

(3) Concurrently with the push operation, the jump address of the corresponding interrupt (the start address of the interrupt processing routine) is transferred from the interrupt vector to the program counter.

(4) The interrupt request bit for the corresponding interrupt is set to "0". Also, the interrupt disable flag is set to "1" and multiple interrupts are disabled.

(5) The interrupt routine is executed.

(6) When the RTI instruction is executed, the contents of the registers pushed onto the stack area are popped off in the order from 3 to 1. Then, the routine that was before running interrupt processing resumes.

As described above, it is necessary to set the stack pointer and the jump address in the vector area corresponding to each interrupt to execute the interrupt processing routine.

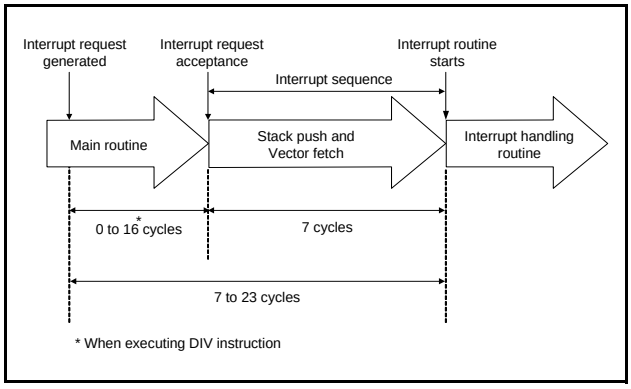


Fig. 20 Time up to execution in interrupt routine

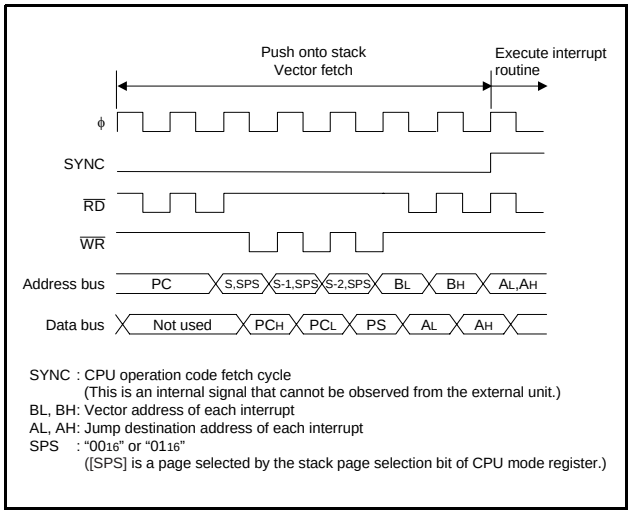


Fig. 21 Interrupt sequence

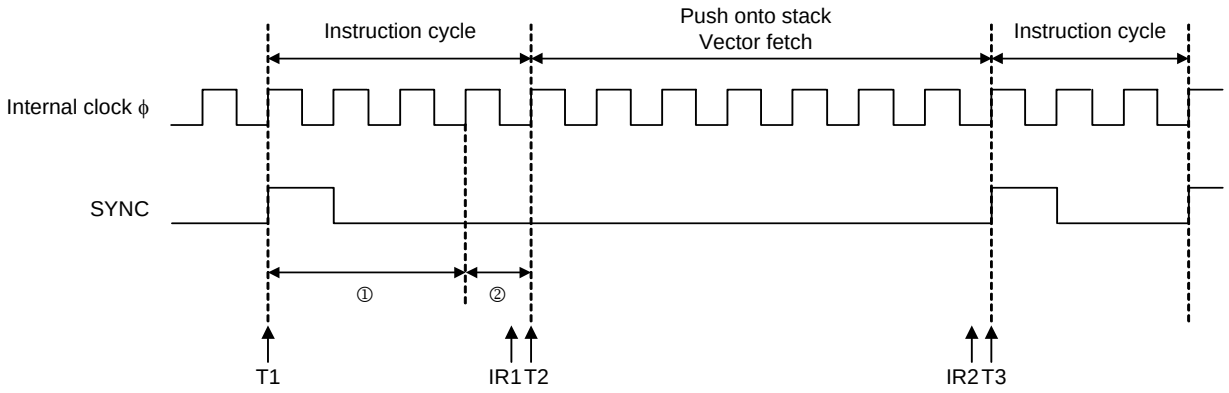
<Notes>

The interrupt request bit may be set to "1" in the following cases.

- When setting the external interrupt active edge
  Related bits: INT_0 interrupt edge selection bit
  (bit 0 of interrupt edge selection register
  (address $003A_{16}$))
  INT_1 interrupt edge selection bit
  (bit 1 of interrupt edge selection register)
  INT_2 interrupt edge selection bit
  (bit 2 of interrupt edge selection register)
  $CNTR_0$ activate edge switch bit
  (bits 6 and 7 of timer X control register 1
  (address $002E_{16}$))
  $CNTR_1$ activate edge switch bit
  (bits 6 of timer Y mode register
  (address 0038_{16}))
- When switching the interrupt sources of an interrupt vector address where two or more interrupt sources are assigned
  Related bit: Timer Y/$CNTR_1$ interrupt switch bit
  (bit 3 of interrupt edge selection register)
- When switching the INT pins
  Related bits: INT_0 input port switch bit
  (bit 4 of interrupt edge selection register)
  INT_1 input port switch bit
  (bit 5 of interrupt edge selection register)

If it is not necessary to generate an interrupt synchronized with these settings, take the following sequence.

(1) Set the corresponding enable bit to "0" (disabled).
(2) Set the interrupt edge selection bit (the active edge switch bit) or the interrupt source bit.
(3) Set the corresponding interrupt request bit to "0" after one or more instructions have been executed.
(4) Set the corresponding interrupt enable bit to "1" (enabled).



T1 T2 T3 : Interrupt acceptance timing points
IR1 IR2 : Timings points at which the interrupt request bit is set to "1".

Note : Period 2 indicates the last ϕ cycle during one instruction cycle.

(1) The interrupt request bit for an interrupt request generated during period 1 is set to "1" at timing point IR1.
(2) The interrupt request bit for an interrupt request generated during period 2 is set to "1" at timing point IR1 or IR2. The timing point at which the bit is set to "1" varies depending on conditions. When two or more interrupt requests are generated during the period 2, each request bit may be set to "1" at timing point IR1 or IR2 separately.

Fig. 22 Timing of interrupt request generation, interrupt request bit, and interrupt acceptance

• Key Input Interrupt (Key-on Wake-Up)

A key input interrupt request is generated by detecting the falling edge from any pin of ports P20–P23, P44–P47 that have been set to input mode. In other words, it is generated when AND of input level goes from "1" to "0". An example of using a key input interrupt is shown in Figure 23, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P44–P47.

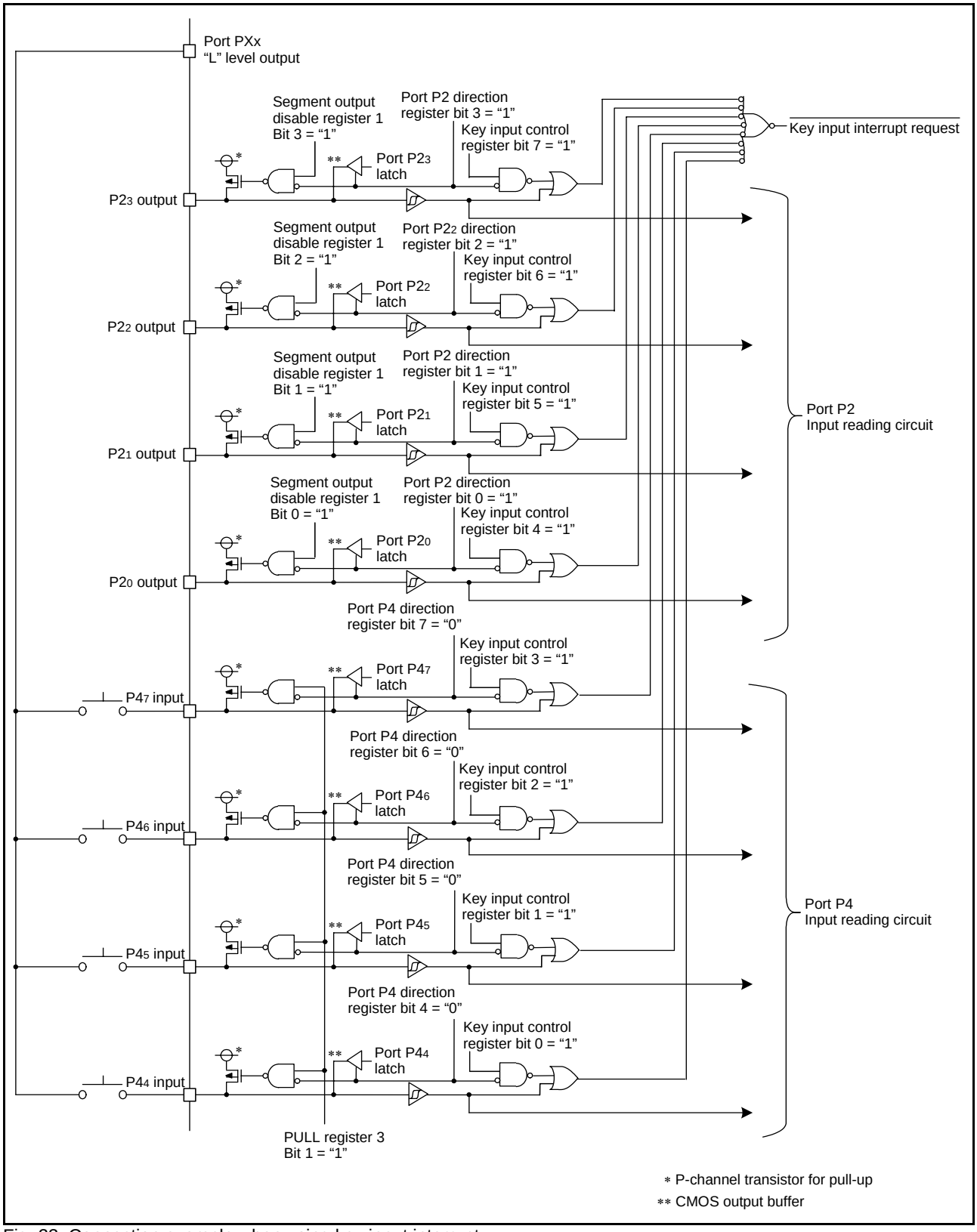


Fig. 23 Connection example when using key input interrupt

A key input interrupt is controlled by the key input control register and port direction registers. When the key input interrupt is enabled, set "1" to the key input control register. A key input of any pin of ports $P2_0$–$P2_3$, $P4_4$–$P4_7$ that have been set to input mode is accepted.

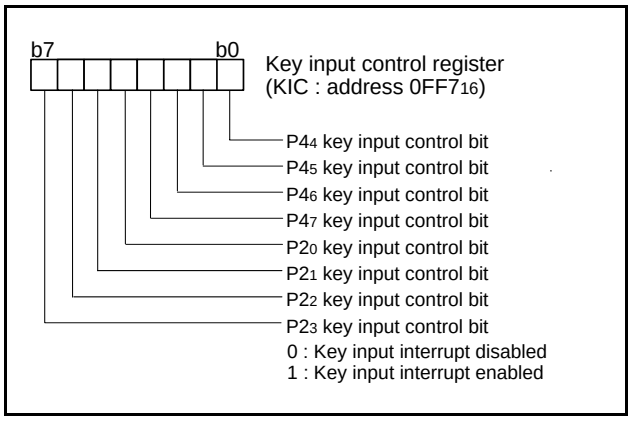


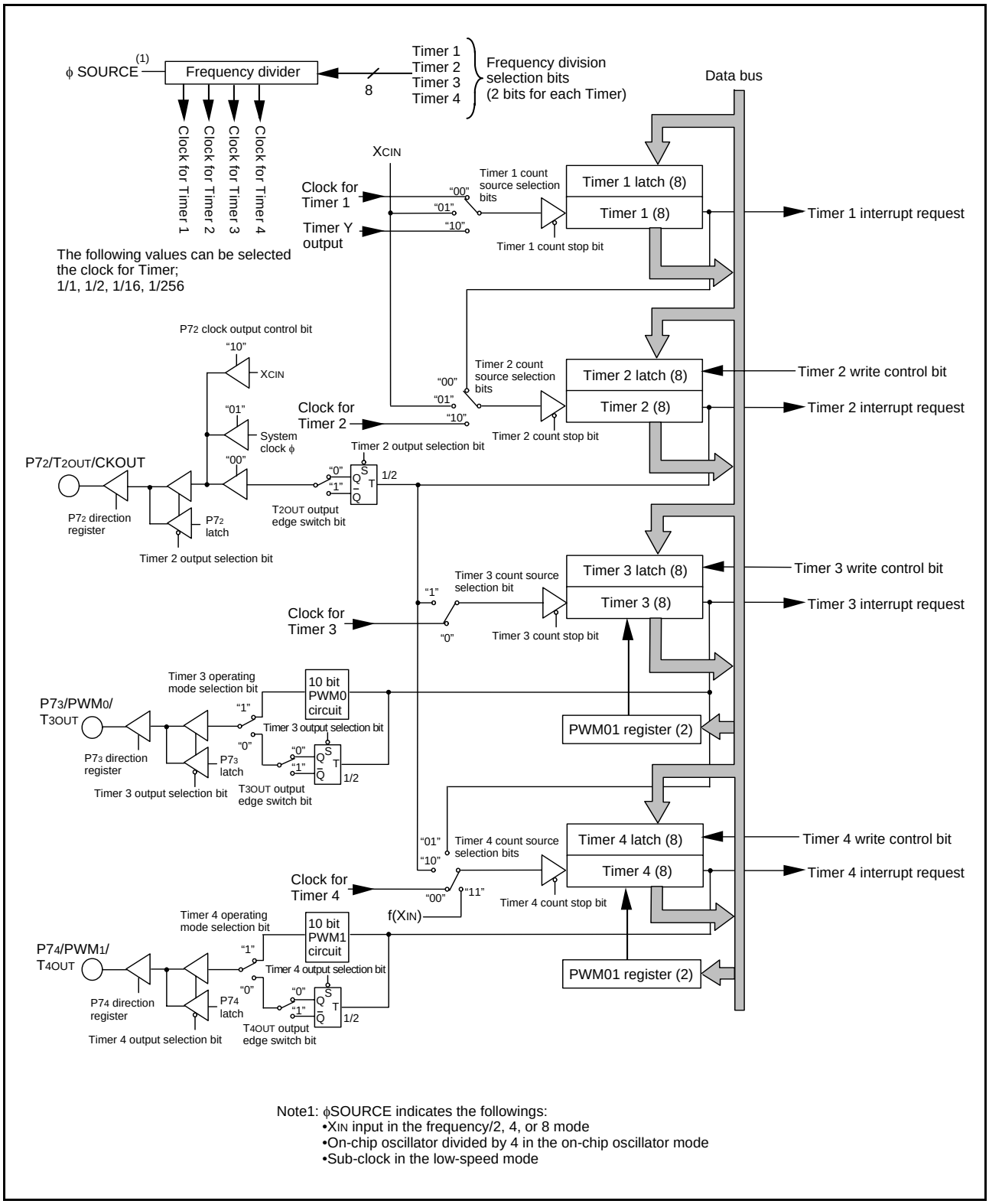
Fig. 24 Structure of key input control register

TIMERS

8-Bit Timer

The 38D5 Group has four built-in 8-bit timers: Timer 1, Timer 2, Timer 3, and Timer 4.

Each timer has the 8-bit timer latch. All timers are down-counters.
When the timer reaches "00$_{16}$", the contents of the timer latch is reloaded into the timer with the next count pulse. In this mode, the interrupt request bit corresponding to that timer is set to "1".
The count can be stopped by setting the stop bit of each timer to "1".



Note1: φSOURCE indicates the followings:
- XIN input in the frequency/2, 4, or 8 mode
- On-chip oscillator divided by 4 in the on-chip oscillator mode
- Sub-clock in the low-speed mode

Fig. 25 Timer 1-4 block diagram

• Frequency Divider For Timer

Timer 1, timer 2, timer 3 and timer 4 have the frequency divider for the count source. The count source of the frequency divider is switched to XIN, XCIN, or the on-chip oscillator OCO divided by 4 in the on-chip oscillator mode by the CPU mode register. The frequency divider is controlled by each timer division ratio selection bit. The division ratio can be selected from as follows; 1/1, 1/2, 1/16, 1/256 of f(XIN), f(XCIN) or f(OCO)/4. Switch the frequency division or count source* while the timer count is stopped.

*This also applies when the frequency divider output is selected as the timer count source and the count source is switched in conjunction with a transition between operating modes (on-chip oscillator mode, XIN mode, or low-speed mode). Be careful when changing settings in the CPU mode register.

• Timer 1, Timer 2

The count source for timer 1 and timer 2 can be set using the timer 12 mode register. XCIN may be selected as the count source. If XCIN is selected, count operation is possible regardless of whether or not the XIN input oscillator or the on-chip oscillator is operating. In addition, the timer 12 mode register can be used to output from the P72/T2OUT pin a signal to invert the polarity every time timer 2 underflows.
At reset, all bits of the timer 12 mode register are set to "0", timer 1 is set to "FF16", and timer 2 is set to "0116".
When executing the STP instruction, previously set the wait time at return.

• Timer 3, Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register. Also, by the timer 34 mode register, each time timer 3 or timer 4 underflows, the signal of which polarity is inverted can be output from P73/T3OUT pin or P74/T4OUT pin.

• Timer 3 PWM0 Mode, Timer 4 PWM1 Mode

A PWM rectangular waveform corresponding to the 10-bit accuracy can be output from the P73/PWM0 pin and P74/PWM1 pin by setting the timer 34 mode register and PWM01 register (refer to Figure 26).
One output pulse is the short interval. Four output pulses are the long interval. The "n" is the value set in the timer 3 (address 002216) or the timer 4 (address 002316). The "ts" is one period of timer 3 or timer 4 count source. "H" width of the short interval is obtained by n × ts.
However, in the long interval, "H" width of output pulse is extended for ts which is set by the PWM01 register (address 002416).

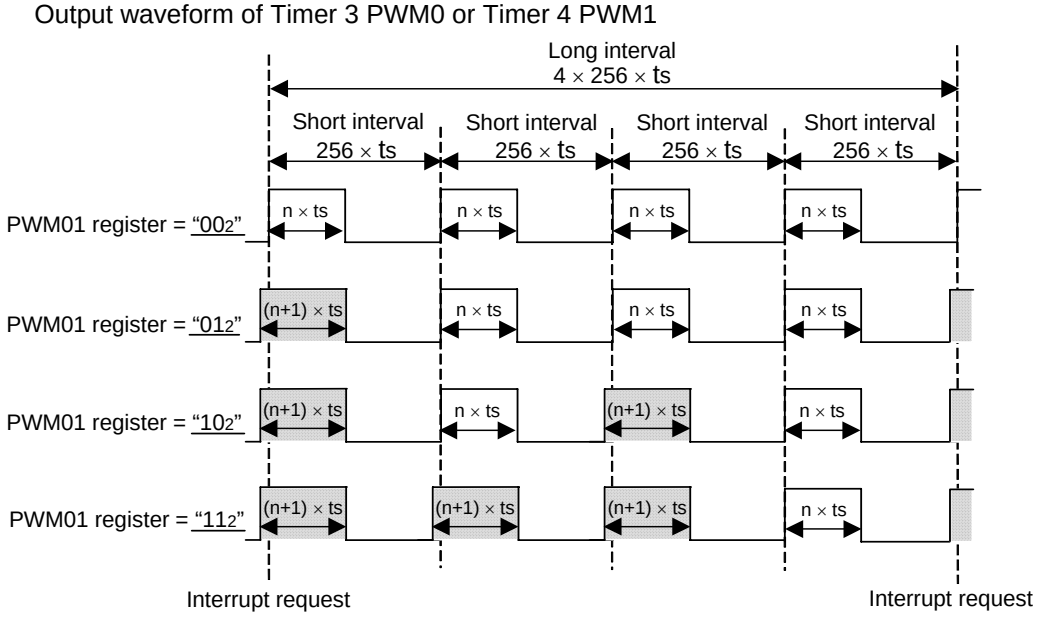
<Notes on Timer 1 to Timer 4>

(1) Timer 3 PWM0 Mode, Timer 4 PWM1 Mode

- When PWM output is suspended after starting PWM output, depending on the level of the output pulse at that time to resume an output, the delay of the one section of the short interval may be needed.
  Stop at "H": No output delay
  Stop at "L": Output is delayed time of 256 × ts
- In the PWM mode, the follows are performed every cycle of the long interval (4 × 256 × ts).
  - Generation of timer 3, timer 4 interrupt requests
  - Update of timer 3, timer 4

(2) Write to Timer 2, Timer 3, Timer 4

When writing to the latch only, if the write timing to the reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting is stopped during writing to the reload latch.



n: Setting value of Timer 3 or Timer 4
ts: One period of Timer 3 count source or Timer 4 count source
PWM01 register (address 002416) : 2-bit value corresponding to PWM0 (bits 0, 1) or PWM1 (bits 2, 3)

Fig. 26 Waveform of PWM0 and PWM1

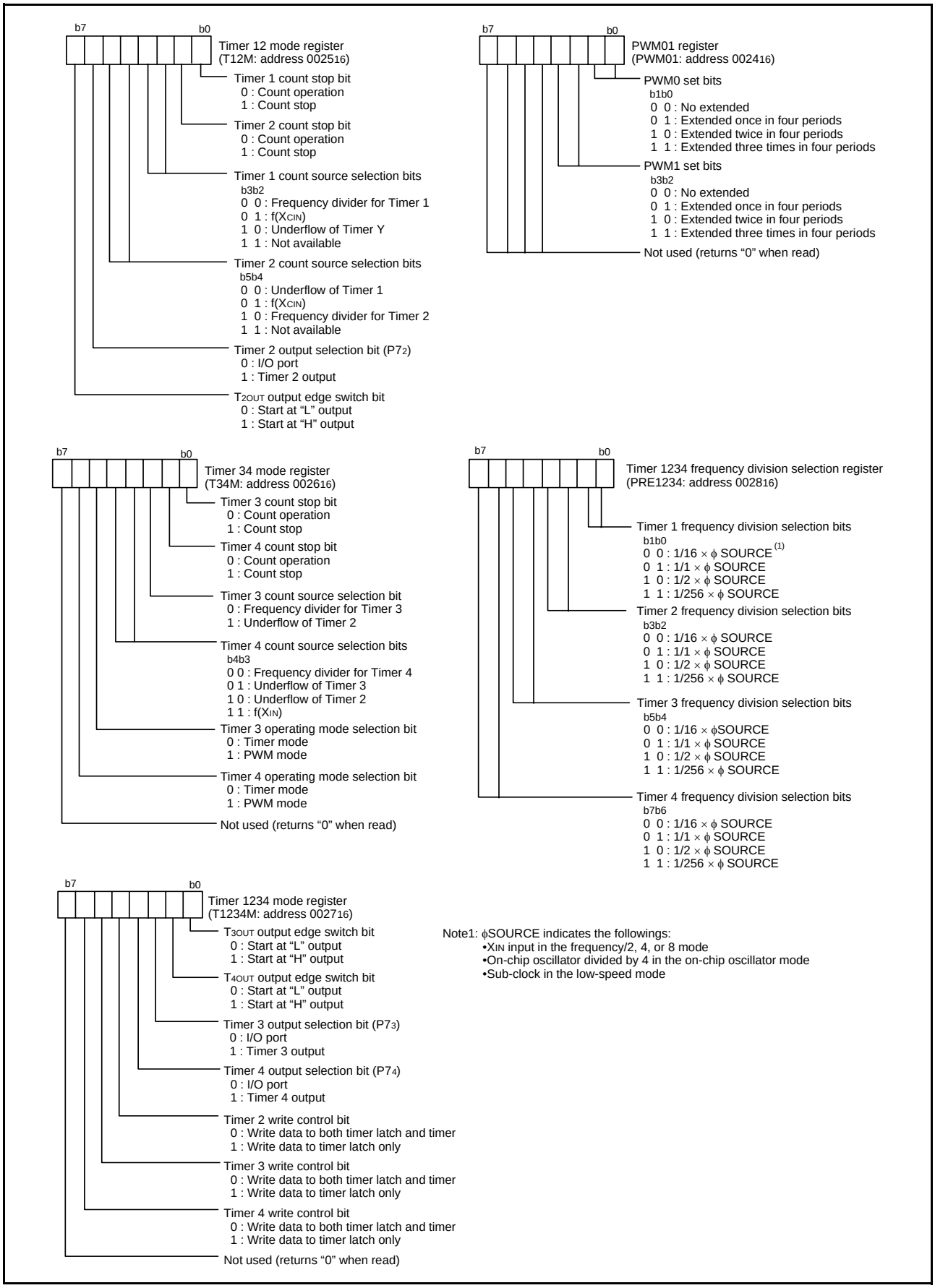
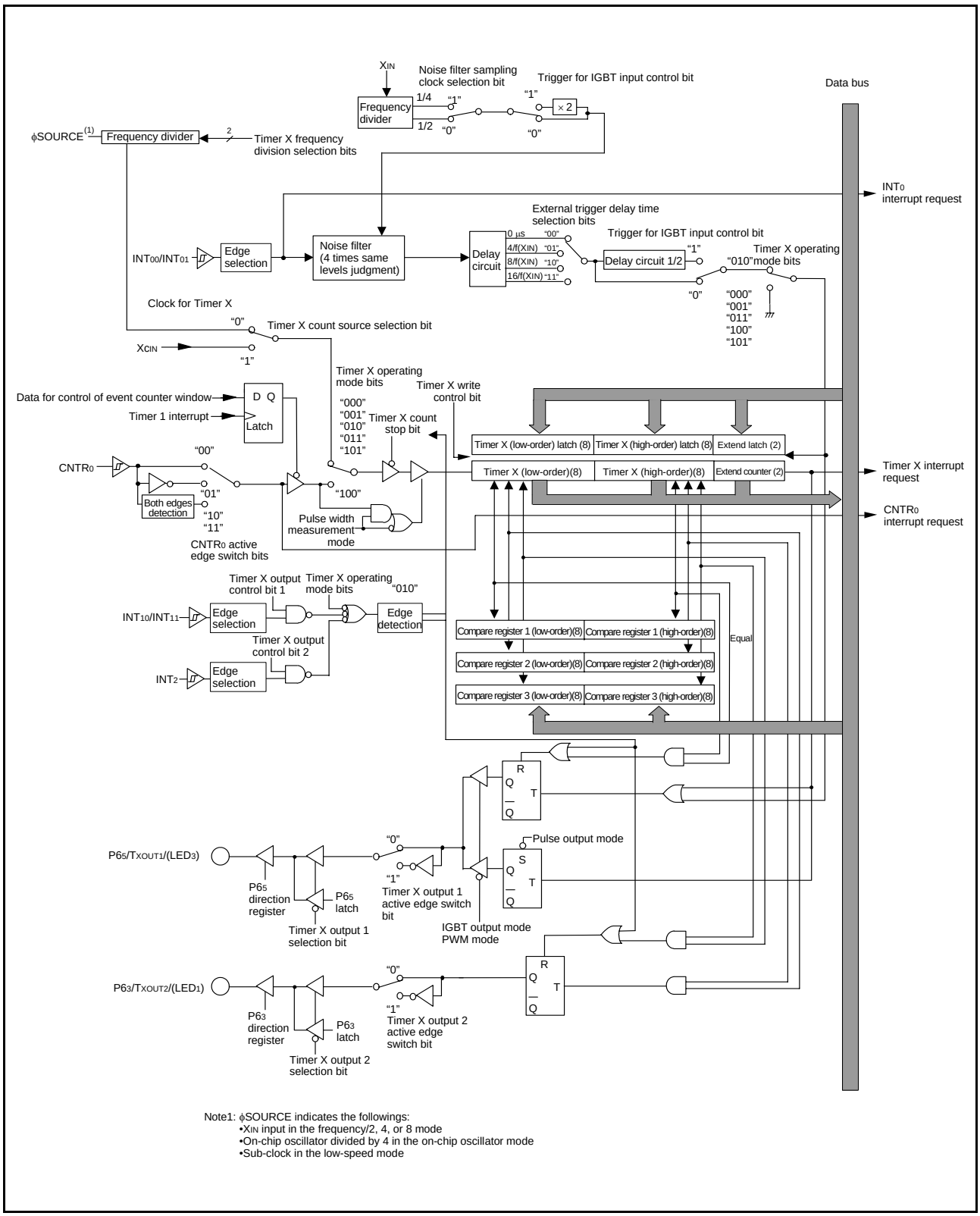


Fig. 27 Structure of timer 1 to timer 4 related registers

16-bit Timer

Read and write operation on 16-bit timer must be performed for both high and low-order bytes. When reading a 16-bit timer, read the high-order byte first. When writing to a 16-bit timer, write the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during the write operation, or when writing during the read operation.



Note1: φSOURCE indicates the followings:
- XIN input in the frequency/2, 4, or 8 mode
- On-chip oscillator divided by 4 in the on-chip oscillator mode
- Sub-clock in the low-speed mode

Fig. 28 Timer X block diagram

• **Frequency Divider For Timer**

Each timer X and timer Y have the frequency dividers for the count source. The count source of the frequency divider is switched to XIN, XCIN, or the on-chip oscillator OCO divided by 4 in the on-chip oscillator mode by the CPU mode register. The division ratio of each timer can be controlled by each timer division ratio selection bit. The division ratio can be selected from as follows;
1/1, 1/2, 1/16, 1/256 of f(XIN), f(XCIN) or f(OCO)/4.
Switch the frequency division or count source* while the timer count is stopped.

*This also applies when the frequency divider output is selected as the timer count source and the count source is switched in conjunction with a transition between operating modes (on-chip oscillator mode, XIN mode, or low-speed mode). Be careful when changing settings in the CPU mode register.

• **Timer X**

The count source for timer X can be set using the timer X mode register. XCIN may be selected as the count source. If XCIN is selected, count operation is possible regardless of whether or not the XIN input oscillator or the on-chip oscillator is operating.
The timer X operates as down-count. When the timer contents reach "0000_{16}", an underflow occurs at the next count pulse and the timer latch contents are reloaded. After that, the timer continues countdown. When the timer underflows, the interrupt request bit corresponding to the timer X is set to "1".
Six operating modes can be selected for timer X by the timer X mode register and timer X control register.

(1) Timer Mode

The count source can be selected by setting the timer X mode register. In this mode, timer X operates as the 18-bit counter by setting the timer X register (extension).

(2) Pulse Output Mode

Pulses of which polarity is inverted each time the timer underflows are output from the TXOUT1 pin. Except for that, this mode operates just as in the timer mode.
When using this mode, set the port sharing the TXOUT1 pin to output mode.

(3) IGBT Output Mode

After dummy output from the TXOUT1 pin, count starts with the INT0 pin input as a trigger. In the case that the timer X output 1 active edge switch bit is "0", when the trigger is detected or the timer X underflows, "H" is output from the TXOUT1 pin. And then, when the count value corresponds with the compare register 1 value, the TXOUT1 output becomes "L".
After noise is cleared by noise filters, judging continuous 4-time same levels with sampling clocks to be signals, the INT0 signal can use 4 types of delay time by a delay circuit.
When using this mode, set the port sharing the INT0 pin to input mode and set the port sharing the pin used as TXOUT1 or TXOUT2 function to output mode.
When the timer X output control bit 1 or 2 of the timer X control register is set to "1", the timer X count stop bit is fixed to "1" forcibly by the interrupt signal of INT1 or INT2. And then, the TXOUT1 output and TXOUT2 output can be set to "L" forcibly at the same time that the timer X stops counting.
Do not write "1" to the timer X register (extension) when using the IGBT output mode.

(4) PWM Mode

IGBT dummy output, an external trigger with the INT0 pin and output control with pins INT1 and INT2 are not used. Except for those, this mode operates just as in the IGBT output mode.
The period of PWM waveform is specified by the timer X set value. In the case that the timer X output 1 active edge switch bit is "0", the "H" interval is specified by the compare register 1 set value. In the case that the timer X output 2 active edge switch bit is "0", the "H" interval is specified by the compare registers 2 and 3 set values.
When using this mode, set the port sharing the pin used as TXOUT1 or TXOUT2 function to output mode.
Do not write "1" to the timer X register (extension) when using the PWM mode.

(5) Event Counter Mode

The timer counts signals input through the CNTR0 pin. In this mode, timer X operates as the 18-bit counter by setting the timer X register (extension). When using this mode, set the port sharing the CNTR0 pin to input mode.
In this mode, the window control can be performed by the timer 1 underflow. When the bit 5 (data for control of event counter window) of the timer X mode register is set to "1", counting is stopped at the next timer 1 underflow. When the bit is set to "0", counting is restarted at the next timer 1 underflow.

(6) Pulse Width Measurement Mode

In this mode, the count source is the output of frequency divider for timer. In this mode, timer X operates as the 18-bit counter by setting the timer X register (extension). When the bit 6 of the CNTR0 active edge switch bits is "0", counting is executed during the "H" interval of CNTR0 pin input. When the bit is "1", counting is executed during the "L" interval of CNTR0 pin input.
When using this mode, set the port sharing the CNTR0 pin to input mode.
Also, set to enable ("0") the data for control of event counter window (bit 5 of timer X mode register (address $002D_{16}$)).

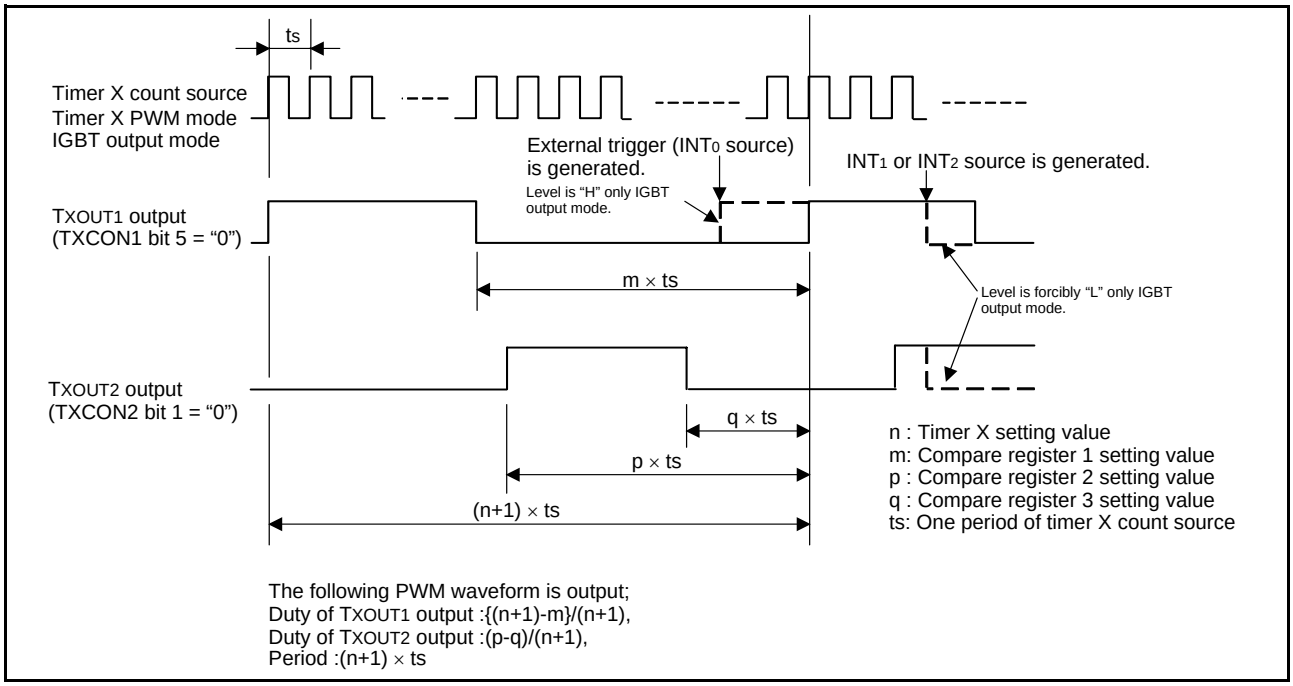


Fig. 29 Waveform of PWM/IGBT

<Notes on Timer X>

(1) Write Order to Timer X

- In the timer mode, pulse output mode, event counter mode and pulse width measurement mode, write to the following registers in the order as shown below;
  the timer X register (extension),
  the timer X register (low-order),
  the timer X register (high-order).
  Do not write to only one of them.
  When the above mode is set and timer X operates as the 16-bit counter, if the timer X register (extension) is never set after reset is released, setting the timer X register (extension) is not required. In this case, write the timer X register (low-order) first and the timer X register (high-order). However, once writing to the timer X register (extension) is executed, note that the value is retained to the reload latch.
- Write to the timer X register by the 16-bit unit. Do not read the timer X register while write operation is performed. If the write operation is not completed, normal operation will not be performed.
- In the IGBT output and PWM modes, do not write "1" to the timer X register (extension). Also, when "1" is already written to the timer X register, be sure to write "0" to the register before using.
  Write to the following registers in the order as shown below;
  the compare registers 1, 2, 3 (high- and low-order),
  the timer X register (extension),
  the timer X register (low-order),
  the timer X register (high-order).
  It is possible to use whichever order to write to the compare registers 1, 2, 3 (high- and low-order). However, write both the compare registers 1, 2, 3 and the timer X register at the same time.
  For the compare registers, set a value less than the setting value in the timer X register. Also, do not set "00$_{16}$".

(2) Read Order to Timer X

- In all modes, read the following registers in the order as shown below;
  the timer X register (extension),
  the timer X register (high-order),
  the timer X register (low-order).
  When reading the timer X register (extension) is not required, read the timer X register (high-order) first and the timer X register (low-order).
  Read order to the compare registers 1, 2, 3 is not specified.
- Read from the timer X register by the 16-bit unit. Do not write to the timer X register while read operation is performed. If the read operation is not completed, normal operation will not be performed.

(3) Write to Timer X

- Which write control can be selected by the timer X write control bit (b3) of the timer X mode register (address 2D$_{16}$), writing data to both the latch and the timer at the same time or writing data only to the latch. When writing a value to the timer X address to write to the latch only, the value is set into the reload latch and the timer is updated at the next underflow.
  After reset release, when writing a value to the timer X address, the value is set into the timer and the timer latch at the same time, because they are written at the same time.
  When writing to the latch only, if the write timing to the high-order reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting is stopped during writing to the high-order reload latch.
- Switch the frequency division or count source* while the timer count is stopped.

*This also applies when the frequency divider output is selected as the timer count source and the count source is switched in conjunction with a transition between operating modes (on-chip oscillator mode, XIN mode, or low-speed mode). Be careful when changing settings in the CPU mode register.

(4) Set of Timer X Mode Register

Set the write control bit of the timer X mode register to "1" (write to the latch only) when setting the IGBT output and PWM modes.
Output waveform simultaneously reflects the contents of both registers at the next underflow after writing to the timer X register (high-order).

(5) Output Control Function of Timer X

- When using the output control function (INT_1 and INT_2) in the IGBT output mode, set the levels of INT_1 and INT_2 to "H" in the falling edge active or to "L" in the rising edge active before switching to the IGBT output mode.

(6) Switch of $CNTR_0$ Active Edge

- When the $CNTR_0$ active edge switch bits are set, at the same time, the interrupt active edge is also affected.

When the pulse width is measured, set the bit 7 of the $CNTR_0$ active edge switch bits to "0".

(7) When Timer X Pulse Width Measurement Mode Used

When timer X pulse width measurement mode is used, enable the event counter wind control data (bit 5 of timer X mode register (address $002D_{16}$)) by setting to "0".
<Reason>
If the event counter window control data (bit 5 of timer X mode register (address $002D_{16}$)) is set to "1" (disabled) to enable/disable the $CNTR_0$ input, the input is not accepted after the timer 1 underflow.

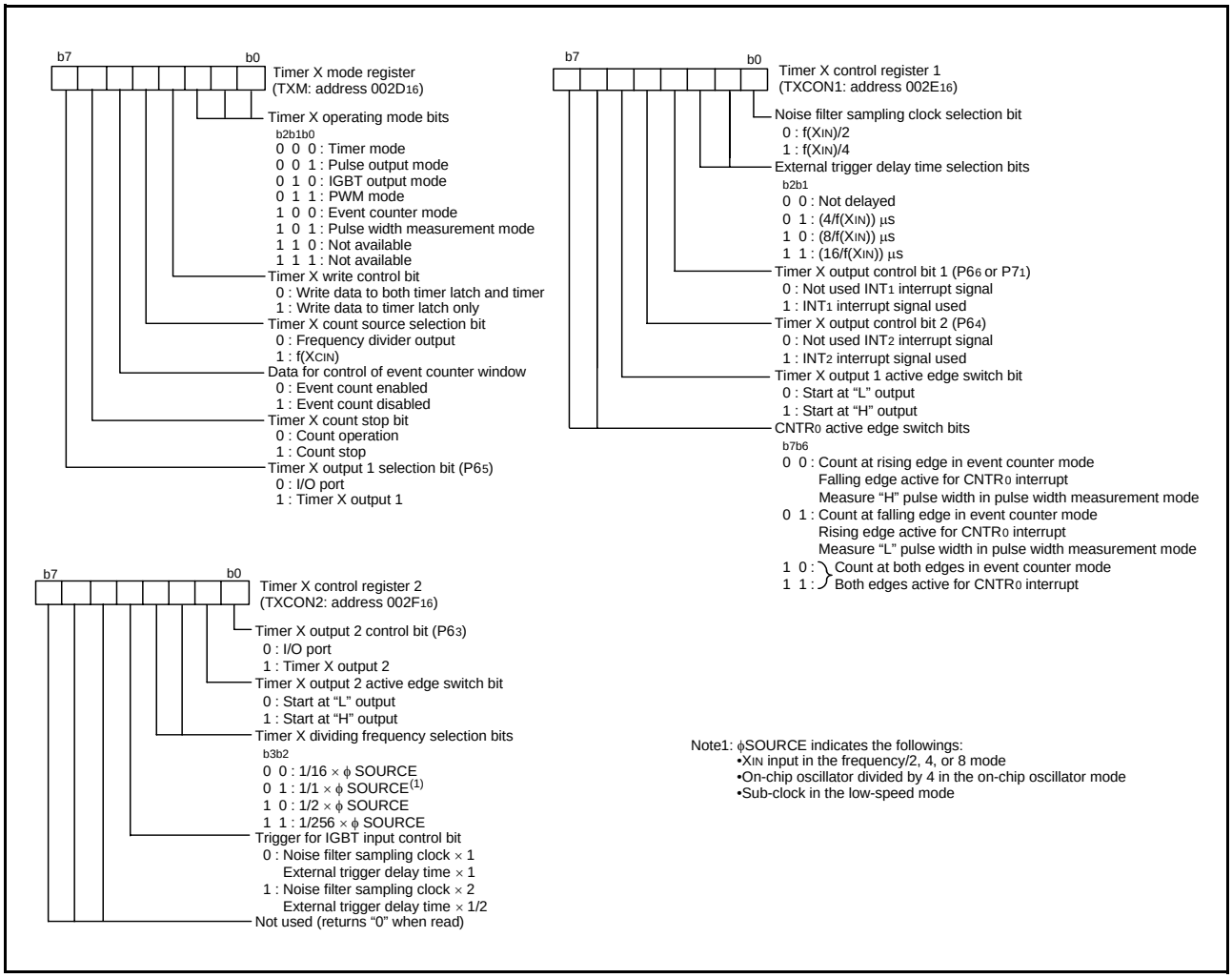


Fig. 30 Structure of Timer X related registers

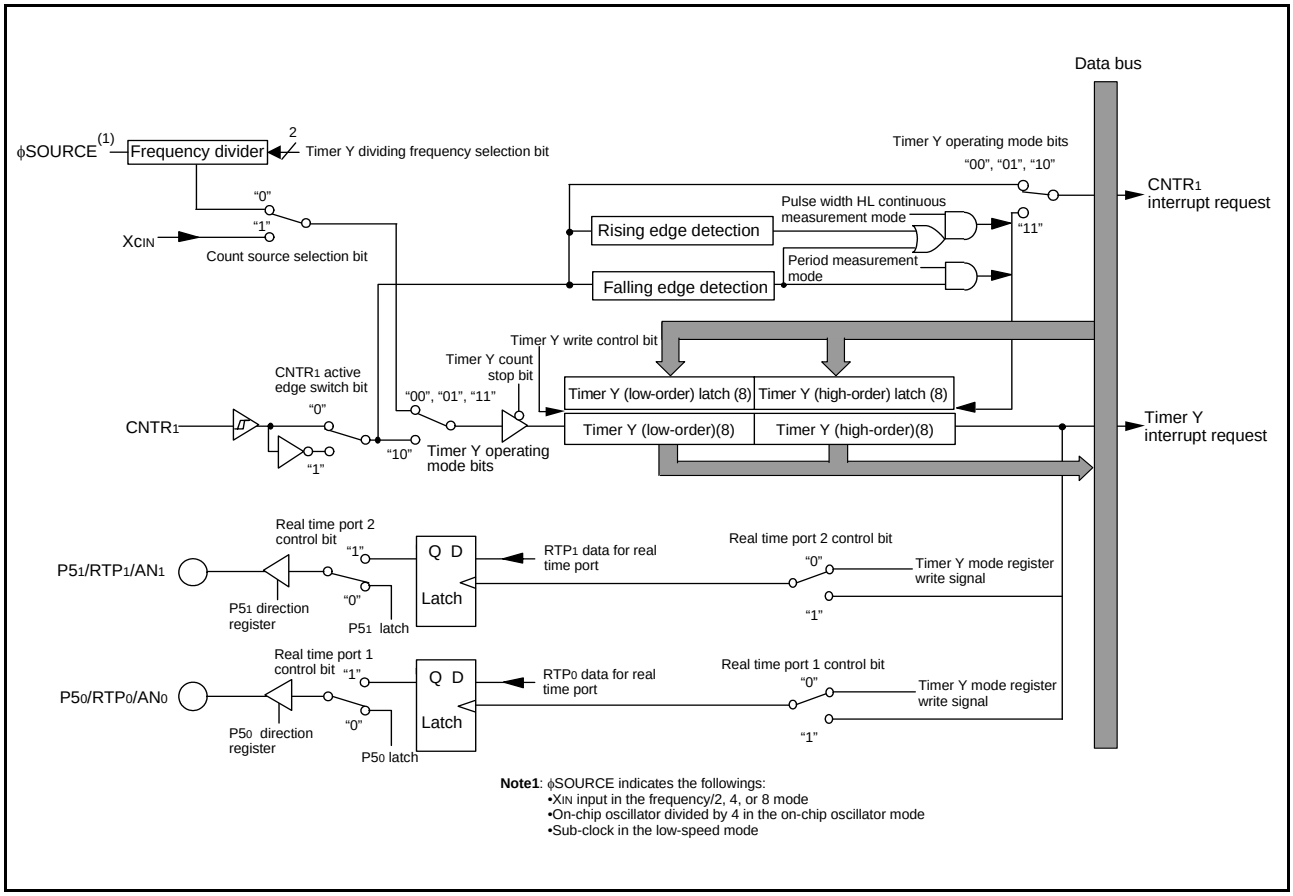


Fig. 31 Block diagram of Timer Y

• Timer Y

Timer Y is a 16-bit timer. The timer Y count source can be selected by setting the timer Y mode register. XCIN can be selected as the count source. When XCIN is selected as the count source, counting can be performed regardless of XIN oscillation or on-chip oscillator oscillation.
Four operating modes can be selected for timer Y by the timer Y mode register. Also, the real time port can be controlled.

(1) Timer Mode

The timer Y count source can be selected by setting the timer Y mode register.

(2) Period Measurement Mode

The interrupt request is generated at rising or falling edge of CNTR1 pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting. Except for that, this mode operates just as in the timer mode.
The timer value just before the reloading at rising or falling of CNTR1 pin input is retained until the timer Y is read once after the reload.
The rising or falling timing of CNTR1 pin input is found by CNTR1 interrupt. When using this mode, set the port sharing the CNTR1 pin to input mode.

(3) Event Counter Mode

The timer counts signals input through the CNTR1 pin.
Except for that, this mode operates just as in the timer mode.
When using this mode, set the port sharing the CNTR1 pin to input mode.

(4) Pulse Width HL Continuously Measurement Mode

The interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for that, this mode operates just as in the period measurement mode. When using this mode, set the port sharing the CNTR1 pin to input mode.

(5) Real Time Port Control

When the real time port function is valid, data for the real time port is output from ports P50 and P51 each time the timer Y underflows.(However, if the real time port control bit is changed from "0" to "1" after the data for real time port is set, data is output independent of the timer Y operation.) When the data for the real time port is changed while the real time port function is valid, the changed data is output at the next underflow of timer Y. Before using this function, set the P50 and P51 port direction registers to output.

<Notes on Timer Y>

• CNTR1 Interrupt Active Edge Selection

CNTR1 interrupt active edge depends on the CNTR1 active edge switch bit. However, in pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge switch bit.

• Timer Y Read/Write Control

- When reading from/writing to timer Y, read from/write to both the high-order and low-order bytes of timer Y. When the value is read, read the high-order bytes first and the low-order bytes next. When the value is written, write the low-order bytes first and the high-order bytes next.
  Write to or read from the timer Y register by the 16-bit unit. If reading from the timer Y register during write operation or writing to it during read operation is performed, normal operation will not be performed.
- Which write control can be selected by the timer Y write control bit (b0) of the timer Y control register (address 0039_{16}), writing data to both the latch and the timer at the same time or writing data only to the latch. When writing a value to the timer Y address to write to the latch only, the value is set into the reload latch and the timer is updated at the next underflow. After reset release, when writing a value to the timer Y address, the value is set into the timer and the timer latch at the same time, because they are set to write at the same time.
  When writing to the latch only, if the write timing to the high-order reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. In this time, counting is stopped during writing to the high-order reload latch.
- Switch the frequency division or count source* while the timer count is stopped.

*This also applies when the frequency divider output is selected as the timer count source and the count source is switched in conjunction with a transition between operating modes (on-chip oscillator mode, XIN mode, or low-speed mode). Be careful when changing settings in the CPU mode register.

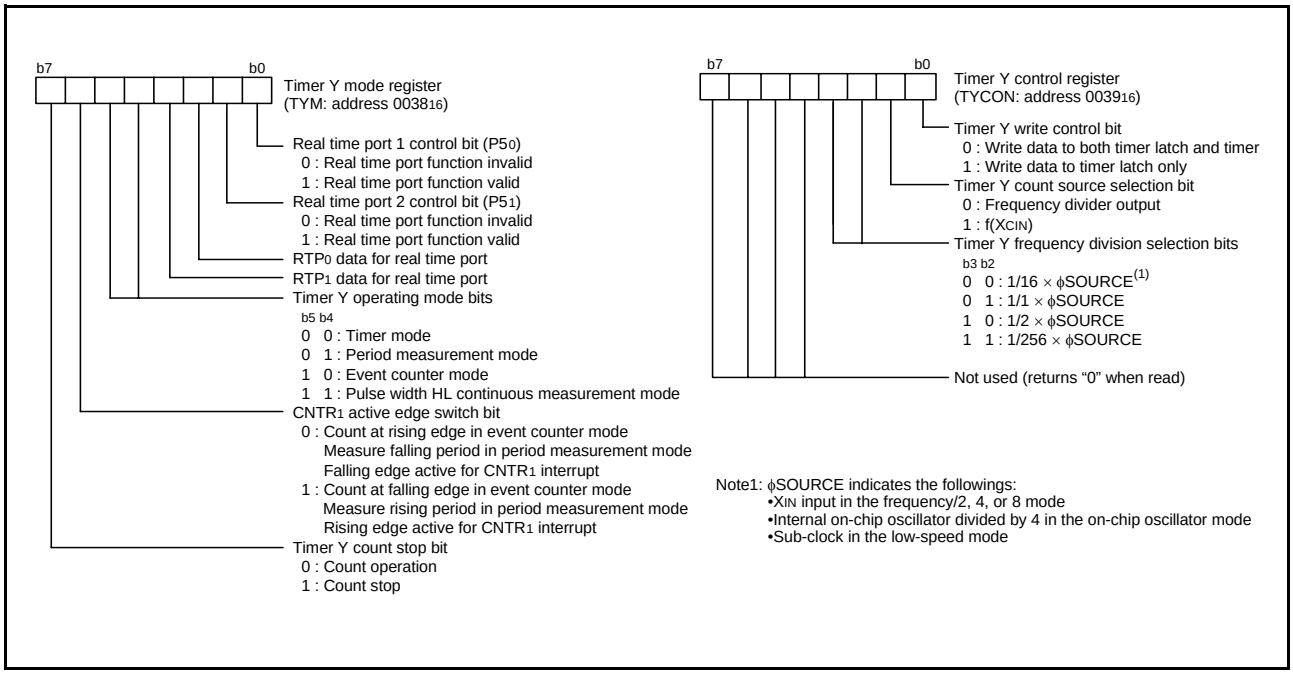


Fig. 32 Structure of Timer Y related registers

SERIAL INTERFACE

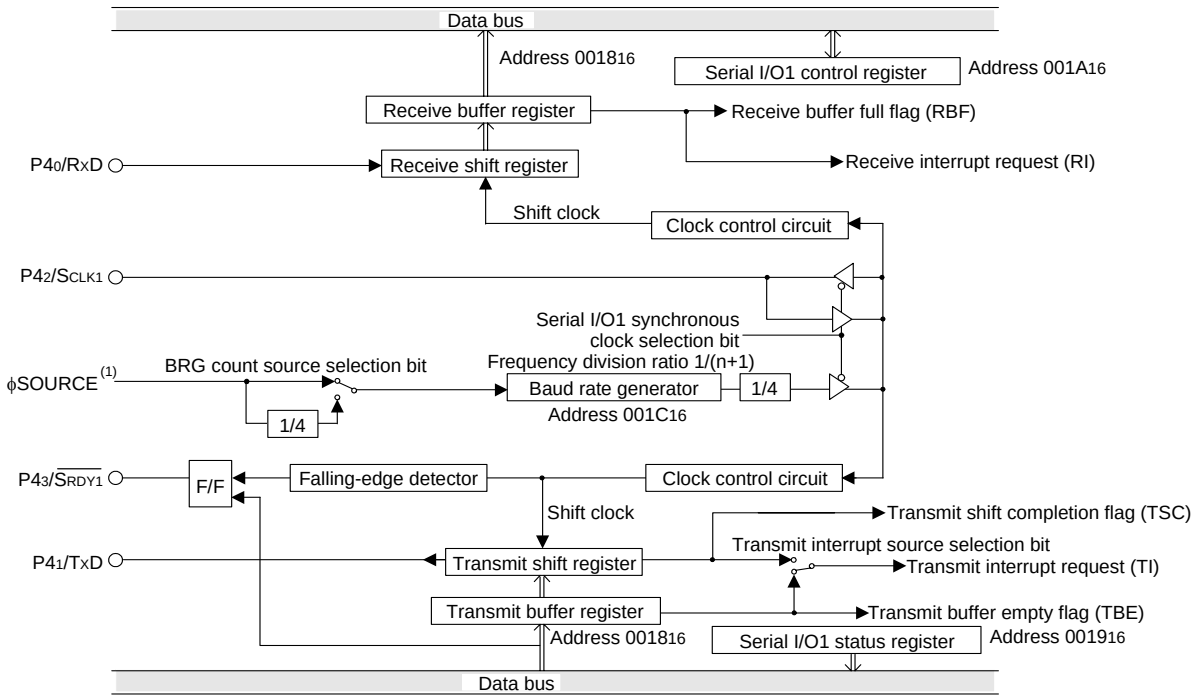
• SERIAL I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

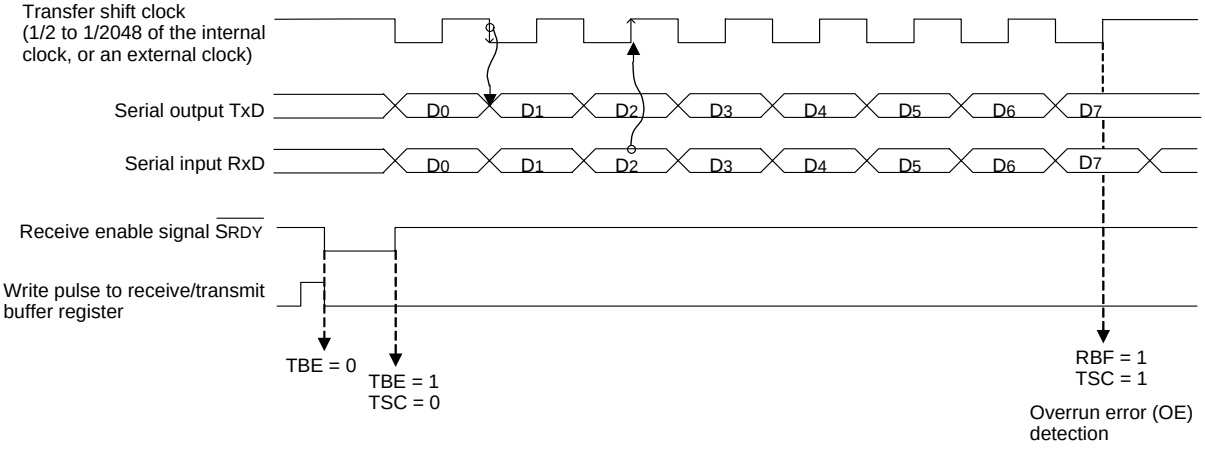
Clock synchronous serial I/O1 mode can be selected by setting the serial I/O mode selection bit of the serial I/O1 control register to "1".

For clock synchronous serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.



Note1: φSOURCE indicates the followings:
- •XIN input in the frequency/2, 4, or 8 mode
- •On-chip oscillator divided by 4 in the on-chip oscillator mode
- •Sub-clock in the low-speed mode

Fig. 33 Block diagram of clock synchronous serial I/O1



Notes 1: As the transmit interrupt (TI) source, which can be selected, either when the transmit buffer has emptied (TBE = 1) or after the transmit shift operation has ended (TSC = 1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.

2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.

3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

Fig. 34 Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by setting the serial I/O mode selection bit of the serial I/O1 control register to “0”.
Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.
The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.
The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

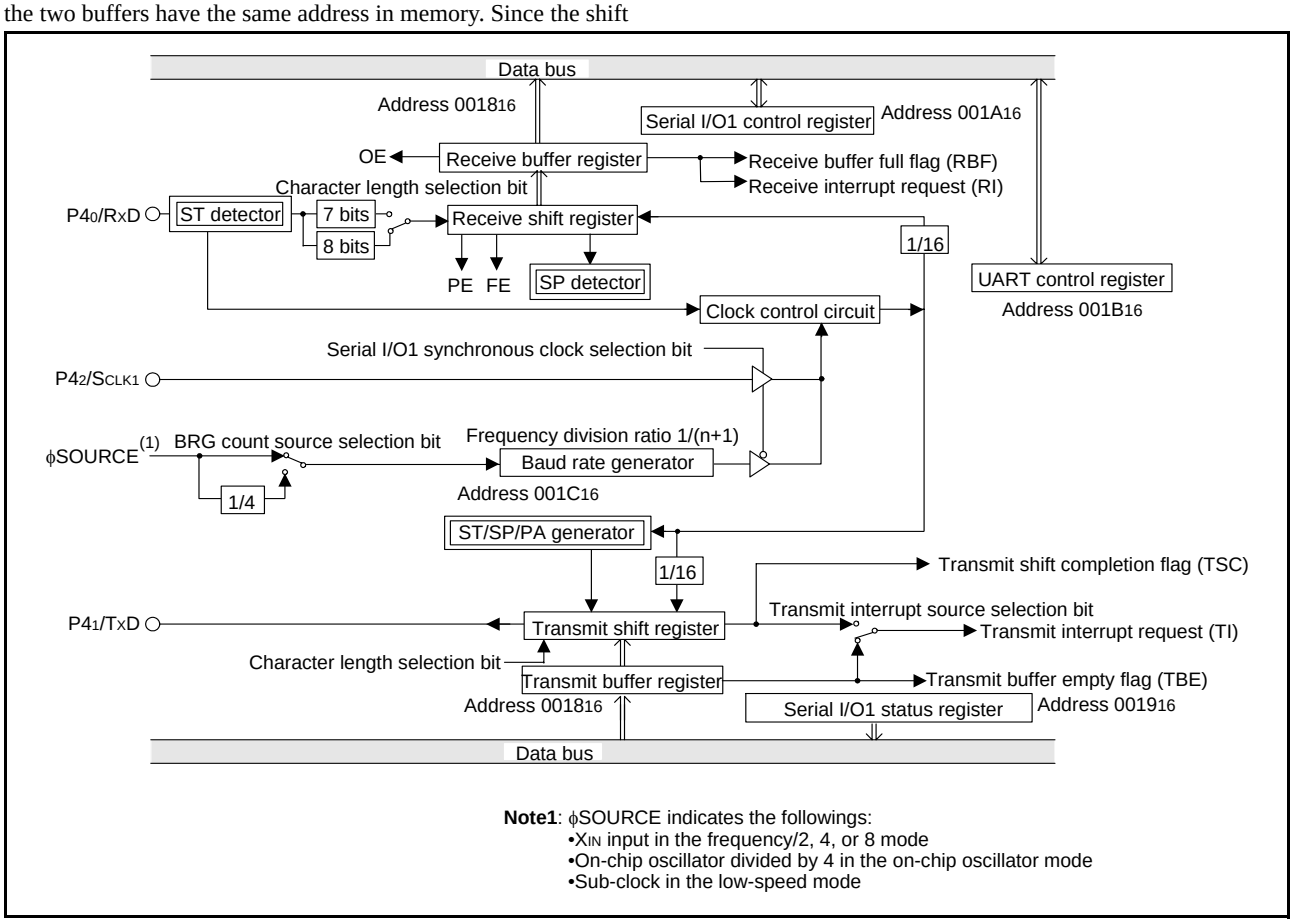
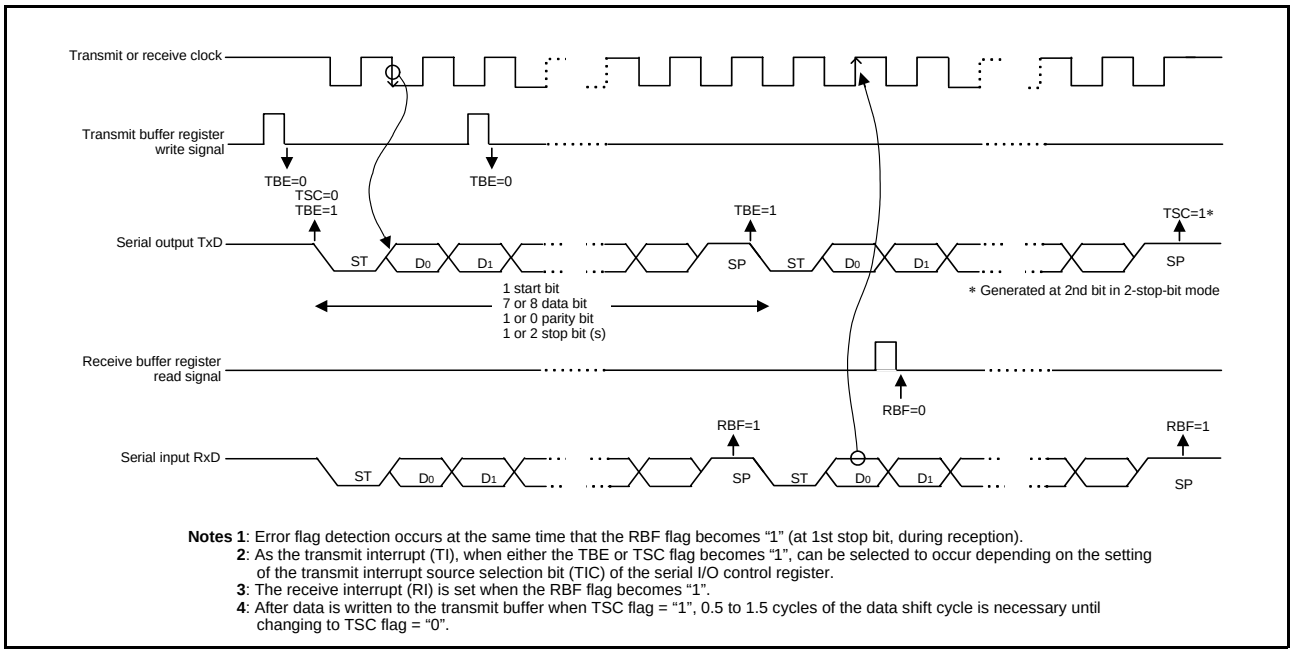


Fig. 35 Block diagram of UART serial I/O1



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1”, can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3: The receive interrupt (RI) is set when the RBF flag becomes “1”.
4: After data is written to the transmit buffer when TSC flag = “1”, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC flag = “0”.

Fig. 36 Operation of UART serial I/O1 function

[Transmit Buffer Register/Receive Buffer Register (TB1/RB1)]

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O1 Status Register (SIO1STS)]

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.
Three of the flags (bits 4 to 6) are valid only in UART mode.
The receive buffer full flag (bit 1) is set to "0" when the receive buffer register is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register sets all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively) to "0". Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also sets all the status flags to "0", including the error flags.
All bits of the serial I/O1 status register are set to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O1 Control Register (SIO1CON)]

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART Control Register (UARTCON)]

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of the data transfer and one bit (bit 4) which is always valid and sets the output structure of the $P4_1$/TxD pin.

[Baud Rate Generator (BRG)]

The baud rate generator determines the baud rate for serial transfer.
The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

<Notes on serial I/O1>

When setting transmit enable bit of serial I/O1 to "1", the serial I/O1 transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronous with the transmission enabled, take the following sequence.

(1) Set the serial I/O1 transmit interrupt enable bit to "0" (disabled).
(2) Set the transmit enable bit to "1".
(3) Set the serial I/O1 transmit interrupt request bit to "0" after 1 or more instructions have been executed.
(4) Set the serial I/O1 transmit interrupt enable bit to "1" (enabled).

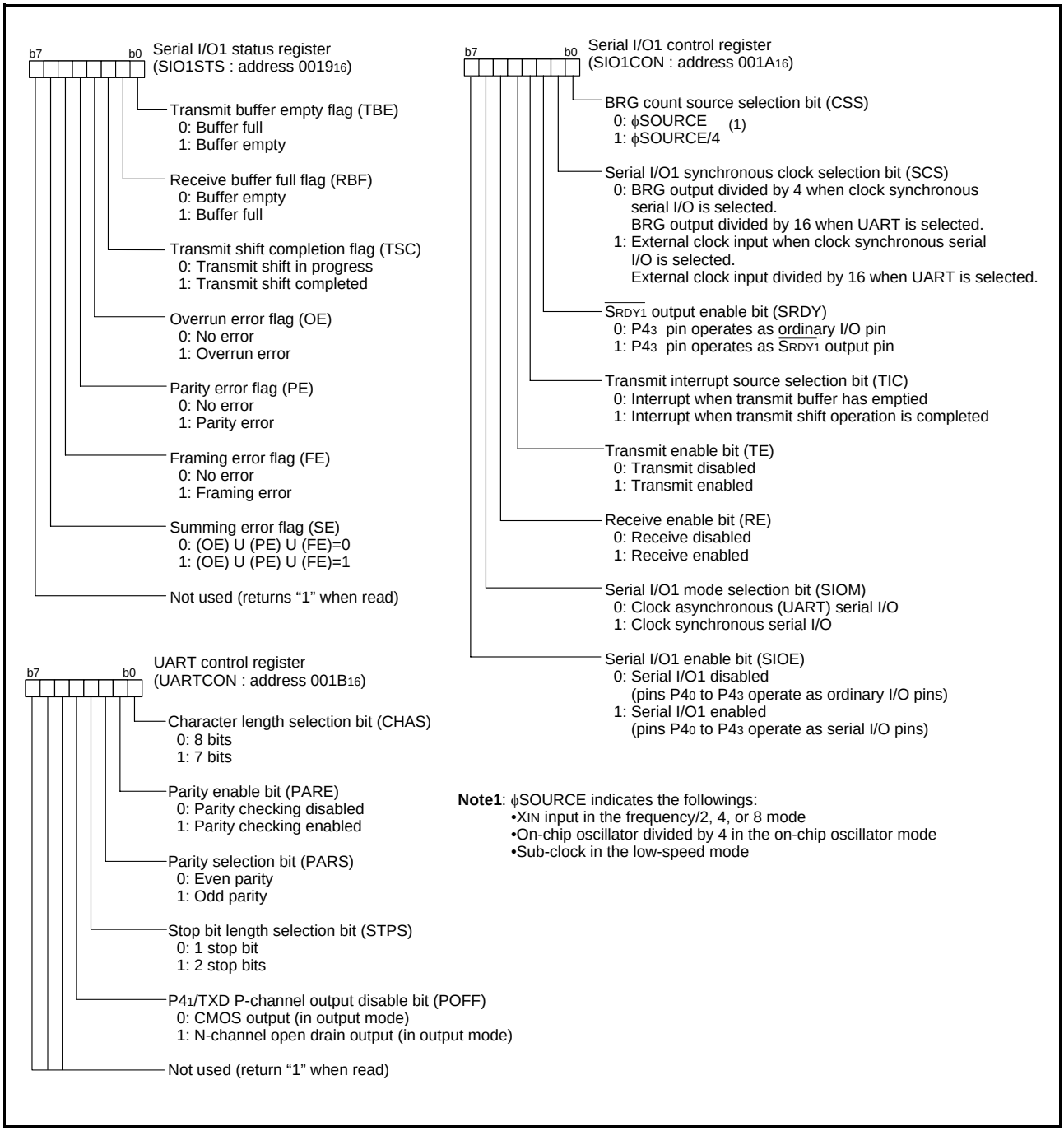


Fig. 37 Structure of serial I/O1 related registers

• Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For serial I/O2, the transmitter and the receiver must use the same clock.

When the internal clock is selected as the operating clock, a write signal to the serial I/O2 register initializes serial I/O2 and transmission/reception starts.

When the external clock is selected as the operating clock, a write signal to the serial I/O2 register initializes the serial I/O2 counter and transmission/reception is enabled. Inputting the external clock starts transmission/reception. To write to the serial I/O2 register when the external clock is selected as the operating clock, perform writing while SCLK2 is set to "H".

[Serial I/O2 control register] SIO2CON

The serial I/O2 control register contains 8bits which control various serial I/O functions.

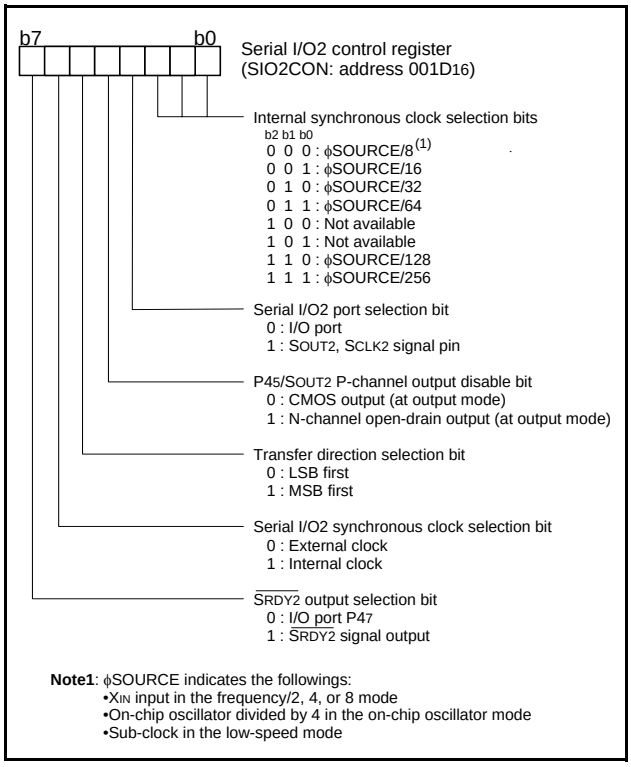


Fig. 38 Structure of serial I/O2 control registers

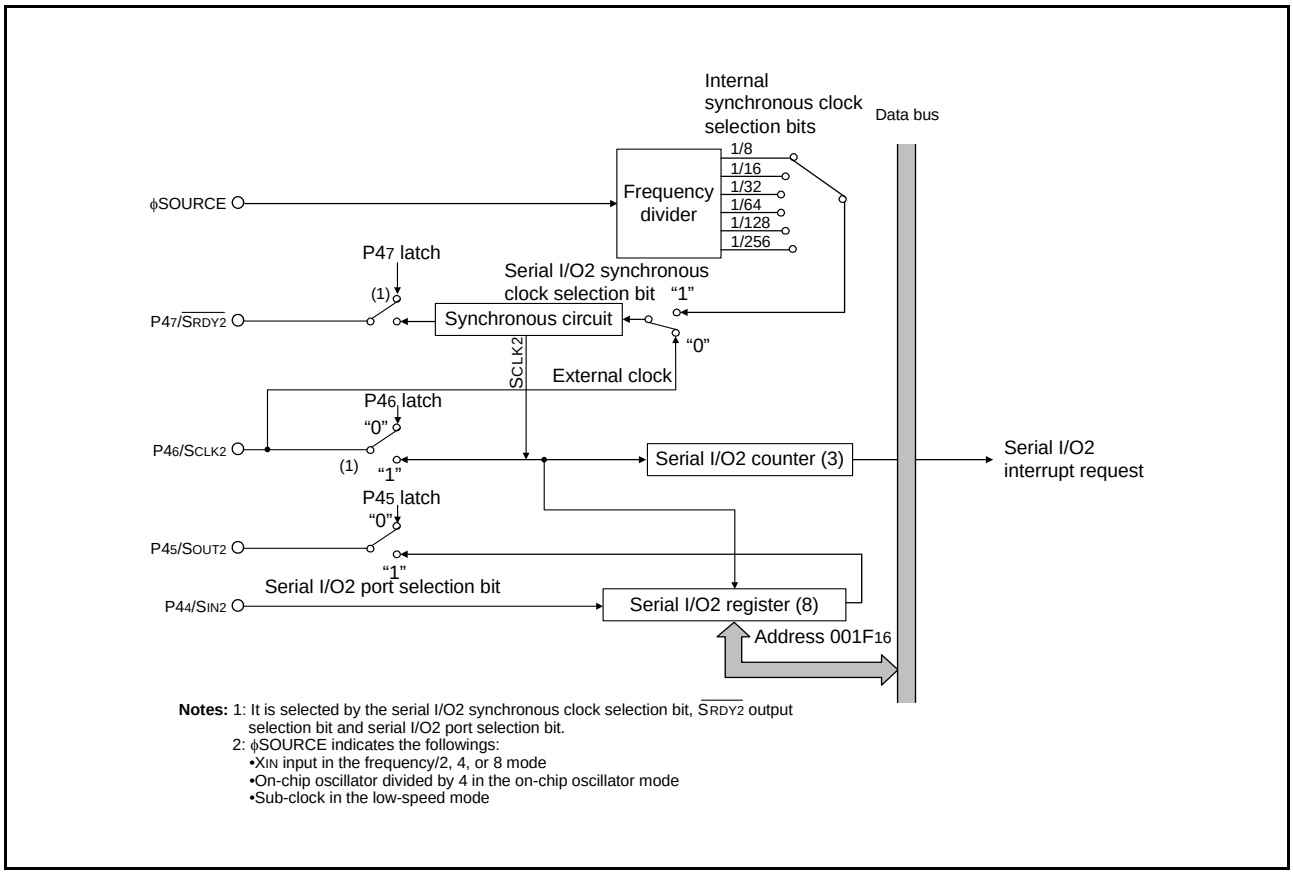


Fig. 39 Block diagram of serial I/O2

[Serial I/O2 Operation]

Writing to the serial I/O2 register initializes the serial I/O2 counter to "7".

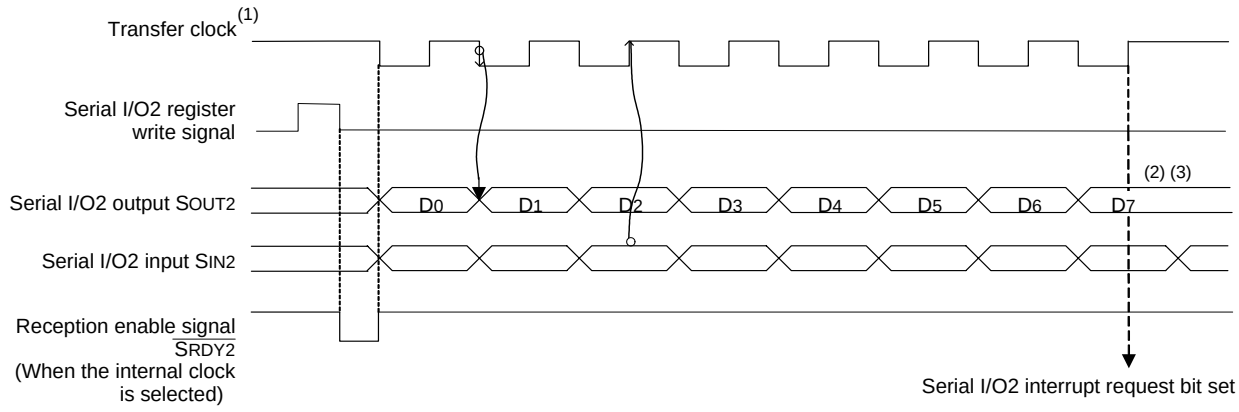
After writing, the SOUT2 pin outputs data each time the synchronous clock changes from "H" to "L". The SIN2 pin captures data each time the synchronous clock changes from "L" to "H" and the serial I/O2 register shifts 1-bit simultaneously.

When the external clock is selected as the synchronous clock, counting the synchronous clock eight times results the following:

- Serial I/O2 counter = "0"
- Synchronous clock is stopped at "H"
- Serial I/O2 interrupt request bit = "1"

After transfer is completed, the SOUT2 pin is placed in the high-impedance state.

When the external clock is selected as the synchronous clock, counting the synchronous clock eight times sets the serial I/O2 bit to "1" and the SOUT2 pin retains the D7 output level. However, if the synchronous clock is continuously input, the serial I/O2 register continues shifting and the SOUT2 pin keeps outputting transmit data.



Notes 1: When the internal clock is selected as the transfer, the dividing frequency of internal clock for transfer clock can be selected by bits 0 to 2 of serial I/O2 control register.

2: When the internal clock is selected as the synchronous clock, the SOUT2 pin is placed in the high impedance state after transfer is completed.

3: When the external clock is selected as the synchronous clock, the SOUT2 pin retains the D7 output level after transfer is completed.
However, if the synchronous clock is continuously input, the serial I/O2 register continues shifting and the SOUT2 pin keeps outputting transmit data.

Fig. 40 Serial I/O2 timing

A/D CONVERTER

The 38D5 Group has a 10-bit A/D converter. The A/D converter performs successive approximation conversion. The 38D5 Group has the ADKEY function which perform A/D conversion of the "L" level analog input from the ADKEY pin automatically.

[AD Conversion Register (ADL, ADH)]

One of these registers is a high-order register, and the other is a low-order register. The high-order 8 bits of a conversion result is stored in the AD conversion register (high-order) (address 0017_{16}), and the low-order 2 bits of the same result are stored in bit 7 and bit 6 of the AD conversion register (low-order) (address 0016_{16}).
During A/D conversion, do not read these registers.
Also, the connection between the resistor ladder and reference voltage input pin (V_{REF}) can be controlled by the V_{REF} input switch bit (bit 0 of address 0016_{16}). When "1" is written to this bit, the resistor ladder is always connected to V_{REF}. When "0" is written to this bit, the resistor ladder is disconnected from V_{REF} except during the A/D conversion.

[AD Control Register (ADCON)]

This register controls A/D converter. Bits 2 to 0 are analog input pin selection bits. Bit 3 is an AD conversion completion bit and "0" during A/D conversion. This bit is set to "1" upon completion of A/D conversion.
A/D conversion is started by setting "0" in this bit.
Bit 5 is the ADKEY enable bit. The ADKEY function is enabled by setting "1" to this bit. When this function is valid, the analog input pin selection bits are ignored. Also, when bit 5 is "1", do not set "0" to bit 3 by program.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF}, and outputs the divided voltages.

[Channel Selector]

The channel selector selects one of the input ports $P5_7/AN_7$–$P5_0/AN_0$ and inputs it to the comparator.

[Comparator and Control Circuit]

The comparator and control circuit compare an analog input voltage with the comparison voltage and store the result in the AD conversion register. When an A/D conversion is completed, the control circuit sets the AD conversion completion bit and the AD conversion interrupt request bit to "1".
The comparator is constructed linked to a capacitor. The conversion accuracy may be low because the change is lost if the conversion speed is not enough.
Accordingly, set $f(X_{IN})$ to at least 500 kHz during A/D conversion in the X_{IN} mode.
Also, do not execute the STP and WIT instructions during the A/D conversion.
In the low-speed mode and on-chip oscillator mode, there is no limit on the oscillation frequency because the on-chip oscillator is used as the A/D conversion clock. In the low-speed mode, on-chip oscillator starts oscillation automatically at the A/D conversion is executed and stops oscillation automatically at the A/D conversion is finished even though it is not oscillating.

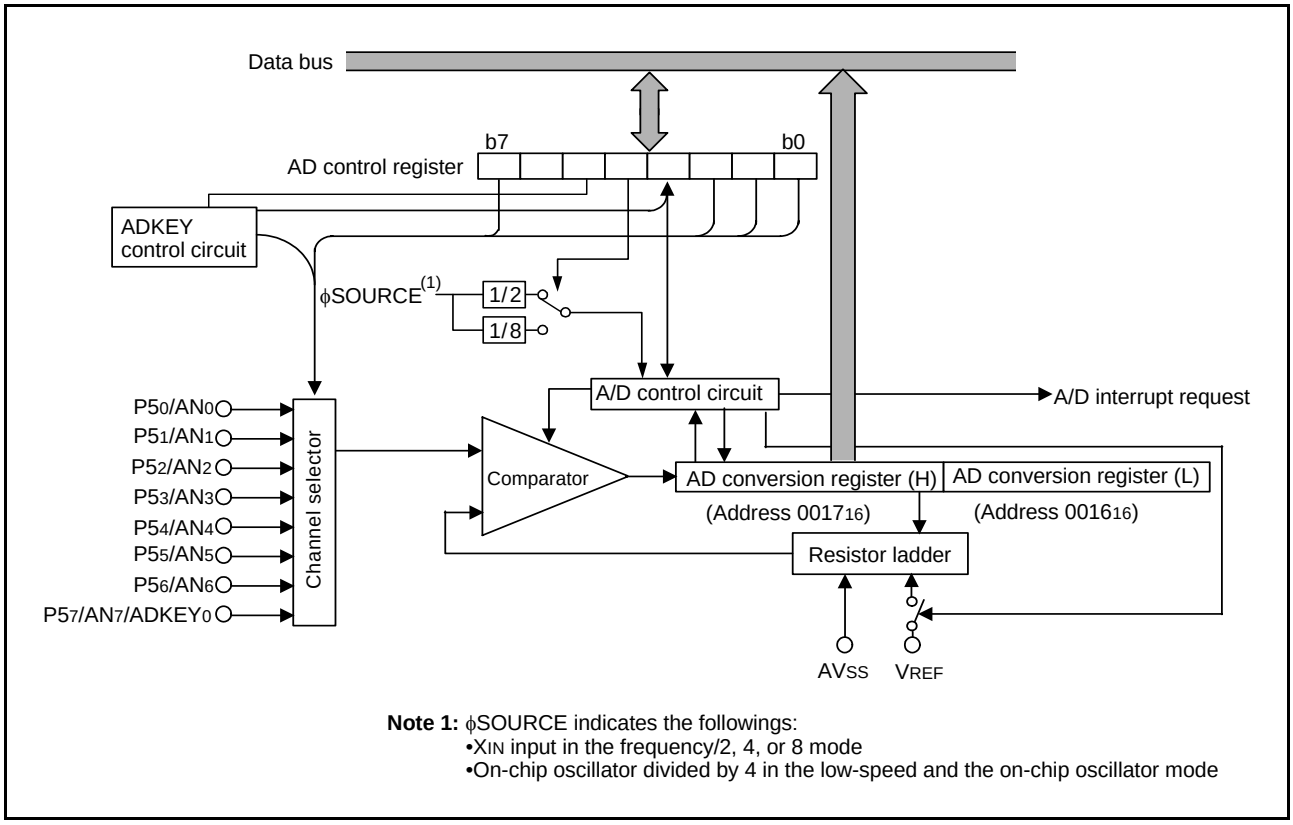


Fig. 41 Block diagram of A/D converter

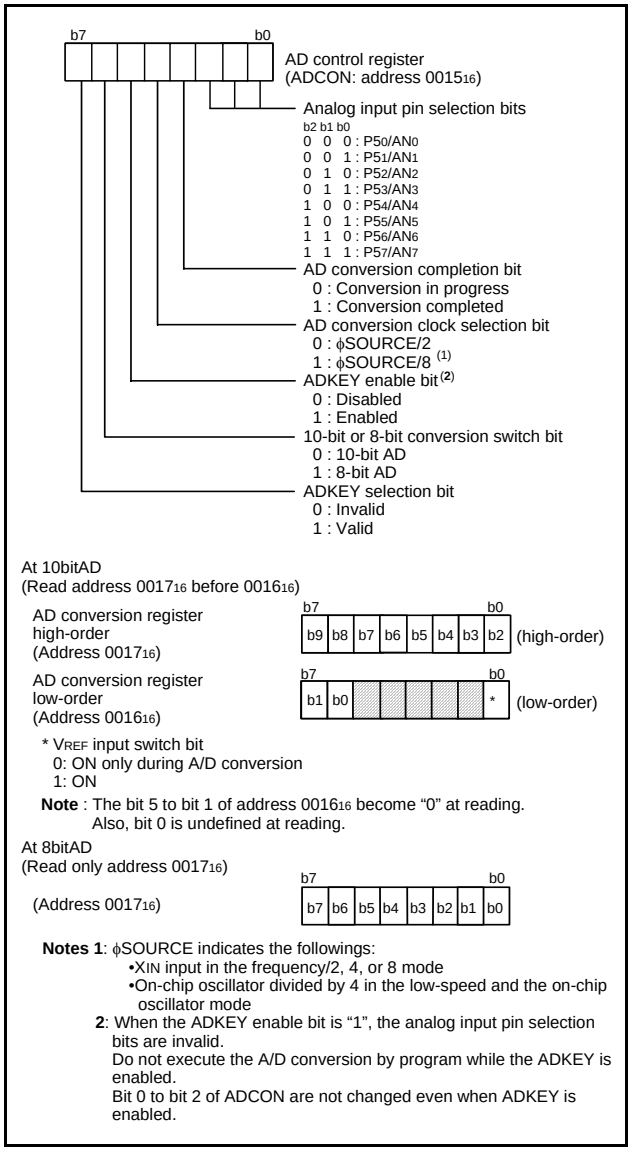


Fig. 42 Structure of AD control register

ADKEY function

The ADKEY function is used to judge the analog input voltage input from the ADKEY pin. When the A/D converter starts operating after V_{IL} ($0.7 \times Vcc-0.5$) or less is input, the event of analog voltage input can be judged with the A/D conversion interrupt.

This function can be used with the STP and WIT state.

As for the ADKEY function in 38D5 Group, the A/D conversion of analog input voltage immediately after starting ADKEY function is not performed.

Therefore, the A/D conversion result immediately after an ADKEY function is undefined. Accordingly, when the A/D conversion result of the analog input voltage input from the ADKEY pin is required, start the A/D conversion by program after the analog input pin corresponding to ADKEY is selected.

• ADKEY Selection

When the ADKEY pin is used, set the ADKEY selection bit to "1". The ADKEY selection bit is "0", just after the A/D conversion is started.

• ADKEY Enable

The ADKEY function is enabled by writing "1" to the ADKEY enable bit. Surely, in order to enable ADKEY function, set "1" to the ADKEY enable bit, after setting the ADKEY selection bit to "1".

When the ADKEY enable bit of the AD control register is "1", the analog input pin selection bits become invalid. Please do not write "0" in the AD conversion completion bit by the program during ADKEY enabled state.

[ADKEY Control Circuit]

In order to obtain a more exact conversion result, by the A/D conversion with ADKEY, execute the following;

- set the input to the ADKEY pin into a steep falling waveform,
- stabilize the input voltage within 8 clock cycles (1 μs at f(X_{IN}) = 8 MHz) after the input voltage is under V_{IL}

The threshold voltage with an actual ADKEY pin is the voltage between V_{IH}-V_{IL}.

In order not to make ADKEY operation perform superfluously in a noise etc., in the state of the waiting for an input, set the voltage of an ADKEY pin to V_{IH} ($0.9V_{CC}$) or more.

When the following operations are performed, the A/D conversion operation cannot be guaranteed.

- When the CPU mode register is operated during A/D conversion operation,
- When the AD conversion control register is operated during A/D conversion operation,
- When the STP or WIT instruction is executed during A/D conversion operation.

LCD DRIVE CONTROL CIRCUIT

The 38D5 Group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

- LCD display RAM
- Segment output disable register
- LCD mode register
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

A maximum of 36 segment output pins and 8 common output pins can be used.

Up to 256 pixels can be controlled for an LCD display. When the LCD enable bit is set to "1" after data is set in the LCD mode register, the segment output disable register, and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

.

Table 12 Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixels
1	36 dots or 8 segment LCD 4 digits
2	72 dots or 8 segment LCD 9 digits
3	108 dots or 8 segment LCD 13 digits
4	144 dots or 8 segment LCD 18 digits
8	256 dots or 8 segment LCD 32 digits

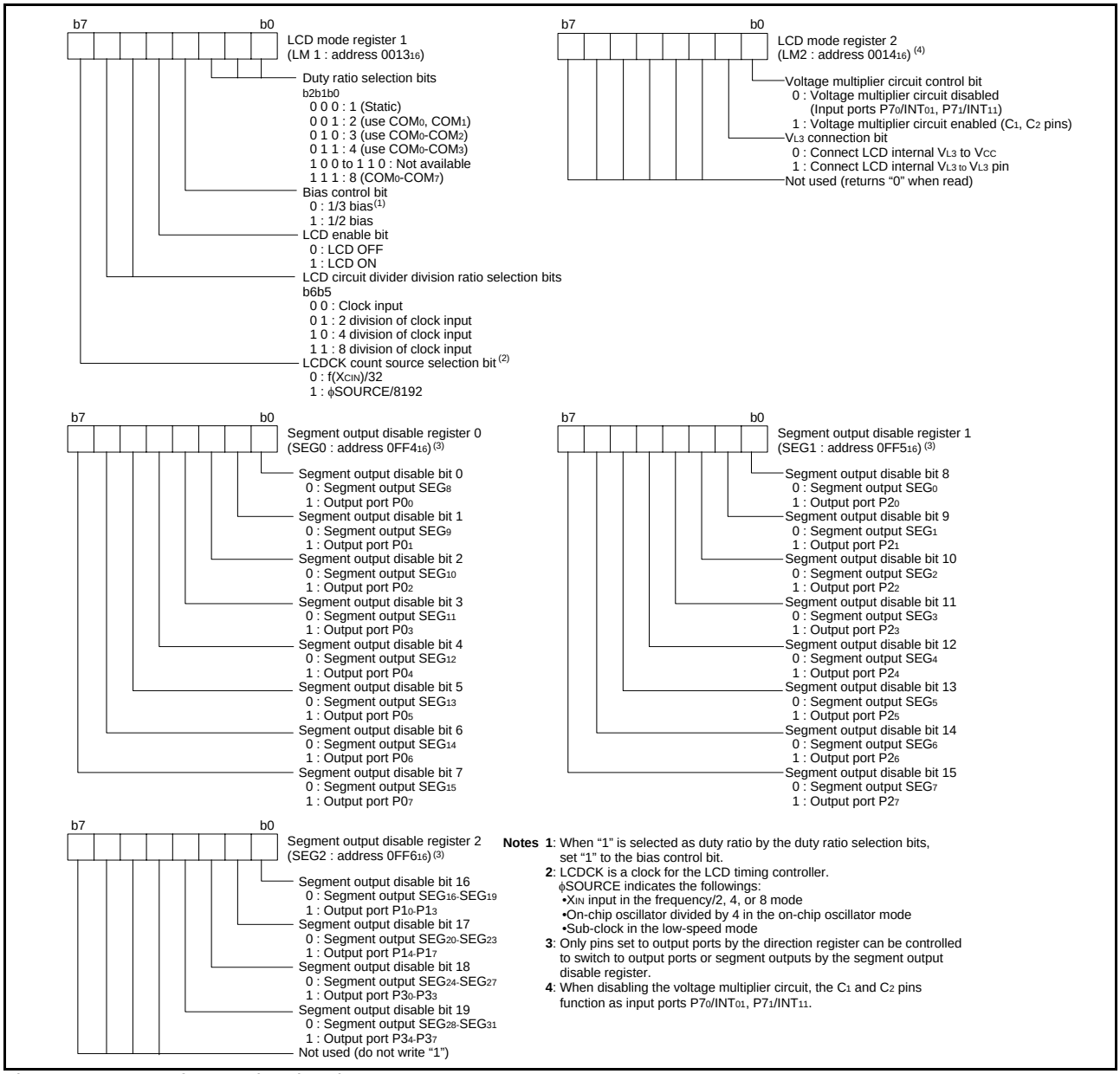


Fig. 43 Structure of LCD related registers

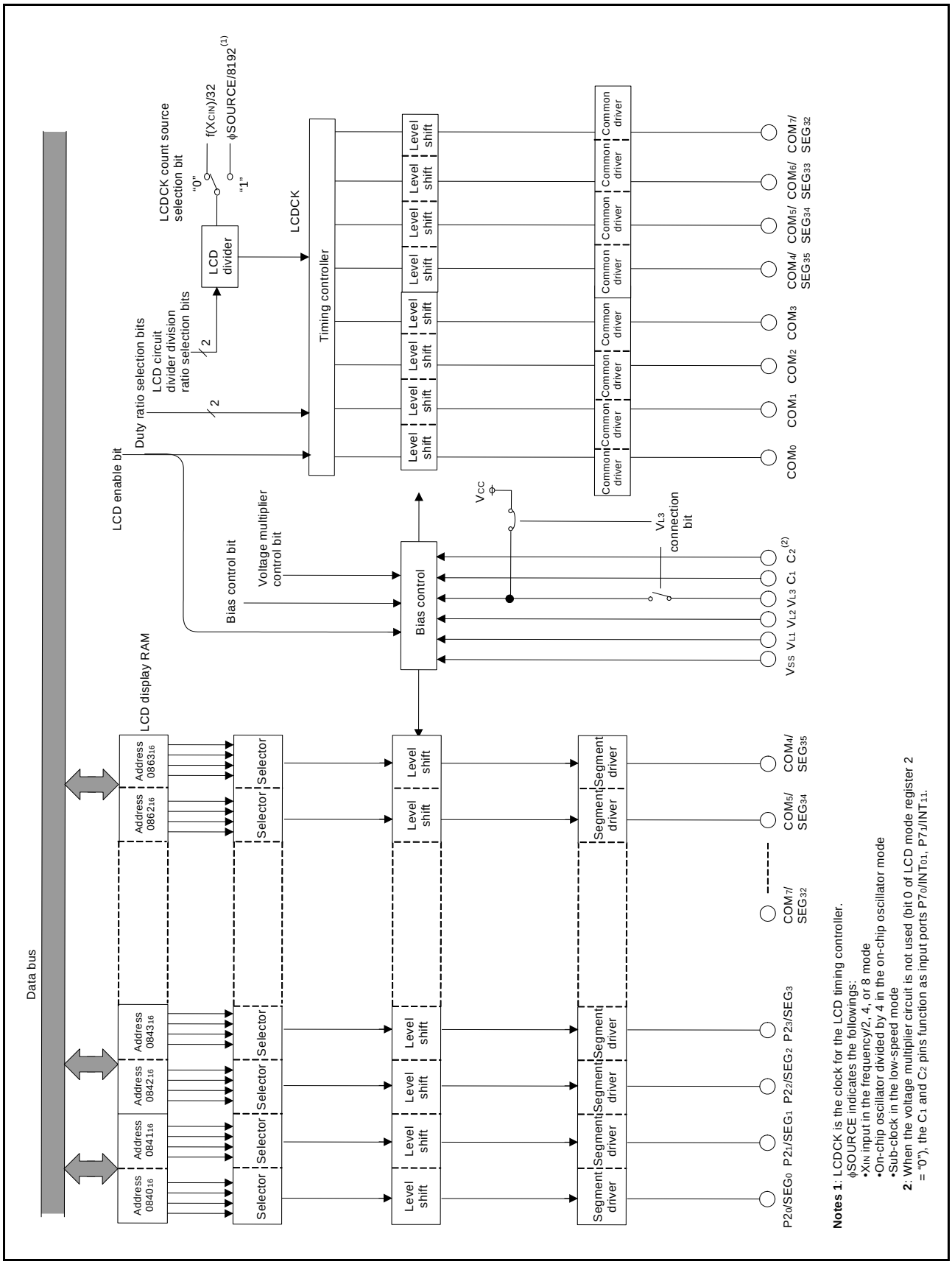


Fig. 44 Block diagram of LCD controller/driver

• Voltage Multiplier

The voltage multiplier performs threefold boosting. This circuit inputs a reference voltage for boosting from LCD power input pin V_{L1}. Set each bit of the segment output disable registers and the LCD mode registers in the following order for operating the voltage multiplier.

(1) Set the segment output disable bits (bits 0 to 19) of the segment output disable registers (SEG0, 1, 2) to "0" or "1".
(2) Set the duty ratio selection bits (bits 0 to 2), the bias control bit (bit 3), the LCD circuit divider division ratio selection bits (bits 5 and 6), and the LCDCK count source selection bit (bit 7) of the LCD mode register 1 to "0" or "1".
(3) Set the V_{L3} connection bit (bit 1 of the LCD mode register 2 (LM2)) to "1".
(4) Set the voltage multiplier control bit (bit0) of the LCD mode register 2 to "1".

When voltage is input to the V_{L1} pin during operating the voltage multiplier, voltage that is twice as large as V_{L1} occurs at the V_{L2} pin, and voltage that is three times as large as V_{L1} occurs at the V_{L3} pin.

The voltage multiplier is controlled by the voltage multiplier control bit (bit 0 of the LCD mode register 2).
In addition, when the voltage multiplier is used, set the voltage multiplier control bit to "1" (voltage multiplier enabled) after the voltage 1.3 V or more and 2.1 V or less.
When the voltage multiplier is not used, set the V_{L3} connection bit to "1" (open), and apply the suitable voltage for the power supply input pins for LCD (V_{L1}-V_{L3}).
When V_{L3} connection bit is set to be open, V_{L3} pin is in a high impedance state.
When the voltage multiplier is used, set the LCDCK frequency to 100 Hz or more. The on-chip oscillator cannot be used for LCDCK.
In a system where the multiplier circuit is used (a multiplier capacitor is externally connected between the C_1 and C_2 pins), set the voltage multiplier circuit control bit to "1" (voltage multiplier circuit enabled) before executing the STP or WIT instruction.

• Bias Control and Applied Voltage to LCD Power Input Pins

Apply the voltage value shown in Table 13 according to the bias value to the LCD power input pins. Apply the voltage value shown in Table 13 according to the bias value by setting to V_{L3} connection bit (bit 1 of LCD mode register 1) to "1", when the voltage multiplier is not used.
Select a bias value by the bias control bit (bit 3 of the LCD mode register 1).

Table 13 Bias control and applied voltage to V_{L1}–V_{L3}

Bias value	Voltage value
1/3 bias	$V_{L3} = V_{LCD}$ $V_{L2} = 2/3\ V_{LCD}$ $V_{L1} = 1/3\ V_{LCD}$
1/2 bias	$V_{L3} = V_{LCD}$ $V_{L2} = V_{L1} = 1/2\ V_{LCD}$

NOTE:
1. V_{LCD} is the maximum value of supplied voltage for the LCD panel.

• Common Pin and Duty Ratio Control

The common pins (COM_0–COM_7) to be used are determined by duty ratio. Select duty ratio by the duty ratio selection bits (bits 0, 1 and 2 of the LCD mode register1). When reset is released, V_{CC} voltage is output from the common pin.

Table 14 Duty ratio control and common pins used

Duty ratio	Duty ratio selection bits			Common pins used
	Bit 2	Bit 1	Bit 0	
1	0	0	0	COM_0
2	0	0	1	COM_0, COM_1
3	0	1	0	COM_0–COM_2
4	0	1	1	COM_0–COM_3
8	1	1	1	COM_0–COM_7

NOTE:
1. Unused common pin outputs the unselected waveform.

• Segment Signal Output Pin

The segment signal output pins (SEG_0–SEG_{31}) are shared with ports P0–P3. When these pins are used as the segment signal output pins, set the direction registers of the corresponding pins to "1", and set the segment output disable register to "0".
Also, these pins are set to the input port after reset, the V_{CC} voltage is output by the pull-up resistor.

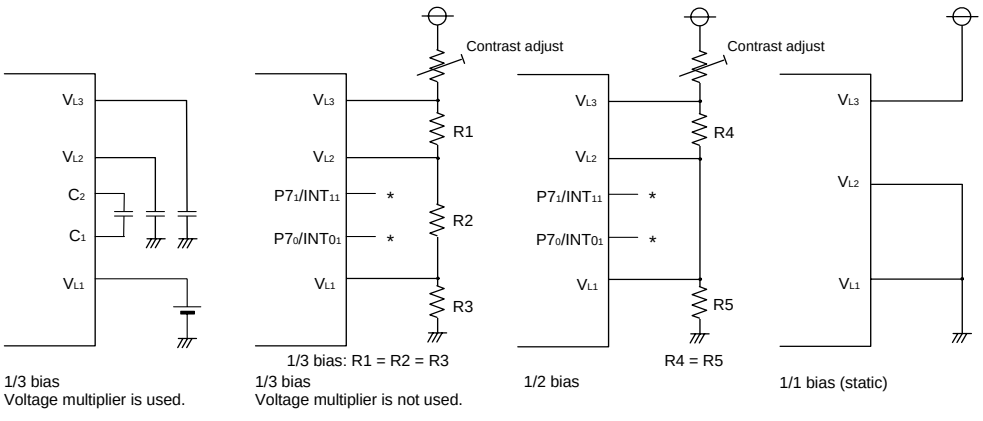


Fig. 45 Example of circuit at each bias (at external power supply input)

• LCD Display RAM

The 36-byte area of address 0840_{16} to 0863_{16} is the designated RAM for the LCD display. When "1" is written to these addresses, the corresponding segments of the LCD display panel are turned on.

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(LCDCK) = \frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency} = \frac{f(LCDCK)}{\text{duty ratio}}$$

<Notes>

(1) Executing STP Instruction

Executing the STP instruction sets the LCD enable bit (bit 4 of LCD mode register1 (address 0013_{16})) to "0" and the LCD panel turns off. To turn the LCD panel on after returning from stop mode, set the LCD enable bit to "1".

(2) V_{L3} Pin

To use the LCD drive control circuit while V_{L3} is set to the voltage equal to V_{CC}, apply the V_{CC} voltage to the V_{L3} pin and write "1" to the V_{L3} connection bit (bit 1 of LCD mode register 2 (address 0014_{16})).

at 4COM × 36SEG

Bits / Address	7	6	5	4	3	2	1	0
0840_{16}	Not used (This area can be used as normal RAM.)				SEG0			
0841_{16}					SEG1			
0842_{16}					SEG2			
0843_{16}					SEG3			
0844_{16}					SEG4			
0845_{16}					SEG5			
0846_{16}					SEG6			
0847_{16}					SEG7			
0848_{16}					SEG8			
0849_{16}					SEG9			
$084A_{16}$					SEG10			
$084B_{16}$					SEG11			
$084C_{16}$					SEG12			
$084D_{16}$					SEG13			
$084E_{16}$					SEG14			
$084F_{16}$					SEG15			
0850_{16}					SEG16			
0851_{16}					SEG17			
0852_{16}					SEG18			
0853_{16}					SEG19			
0854_{16}					SEG20			
0855_{16}					SEG21			
0856_{16}					SEG22			
0857_{16}					SEG23			
0858_{16}					SEG24			
0859_{16}					SEG25			
$085A_{16}$					SEG26			
$085B_{16}$					SEG27			
$085C_{16}$					SEG28			
$085D_{16}$					SEG29			
$085E_{16}$					SEG30			
$085F_{16}$					SEG31			
0860_{16}					SEG32			
0861_{16}					SEG33			
0862_{16}					SEG34			
0863_{16}					SEG35			
					COM3	COM2	COM1	COM0

at 8COM × 32SEG

Bits / Address	7	6	5	4	3	2	1	0
0840_{16}	SEG0							
0841_{16}	SEG1							
0842_{16}	SEG2							
0843_{16}	SEG3							
0844_{16}	SEG4							
0845_{16}	SEG5							
0846_{16}	SEG6							
0847_{16}	SEG7							
0848_{16}	SEG8							
0849_{16}	SEG9							
$084A_{16}$	SEG10							
$084B_{16}$	SEG11							
$084C_{16}$	SEG12							
$084D_{16}$	SEG13							
$084E_{16}$	SEG14							
$084F_{16}$	SEG15							
0850_{16}	SEG16							
0851_{16}	SEG17							
0852_{16}	SEG18							
0853_{16}	SEG19							
0854_{16}	SEG20							
0855_{16}	SEG21							
0856_{16}	SEG22							
0857_{16}	SEG23							
0858_{16}	SEG24							
0859_{16}	SEG25							
$085A_{16}$	SEG26							
$085B_{16}$	SEG27							
$085C_{16}$	SEG28							
$085D_{16}$	SEG29							
$085E_{16}$	SEG30							
$085F_{16}$	SEG31							
0860_{16}	Not used (This area can be used as normal RAM.)							
0861_{16}								
0862_{16}								
0863_{16}								
	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0

Fig. 46 LCD display RAM map

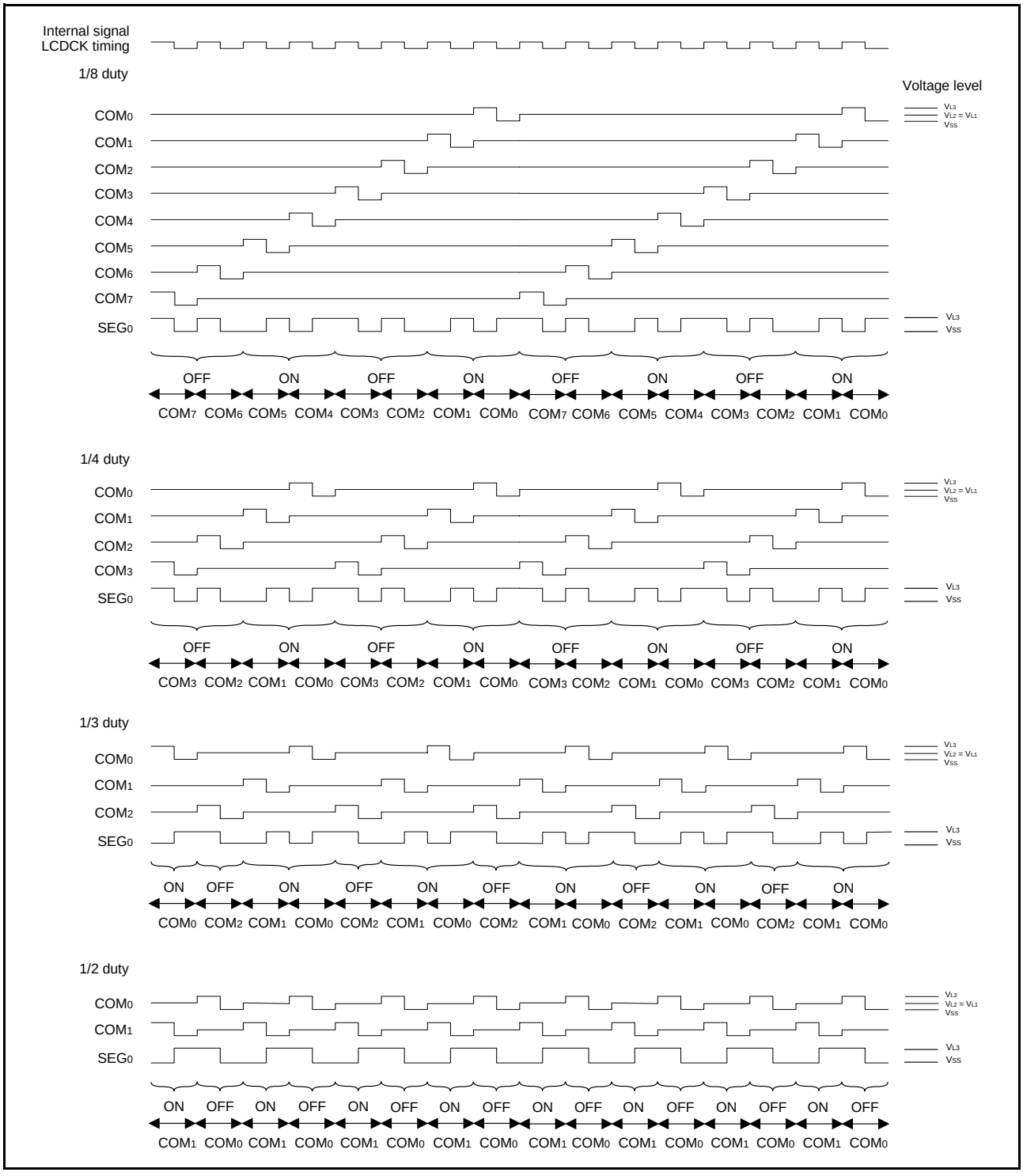


Fig. 47 LCD drive waveform (1/2 bias)

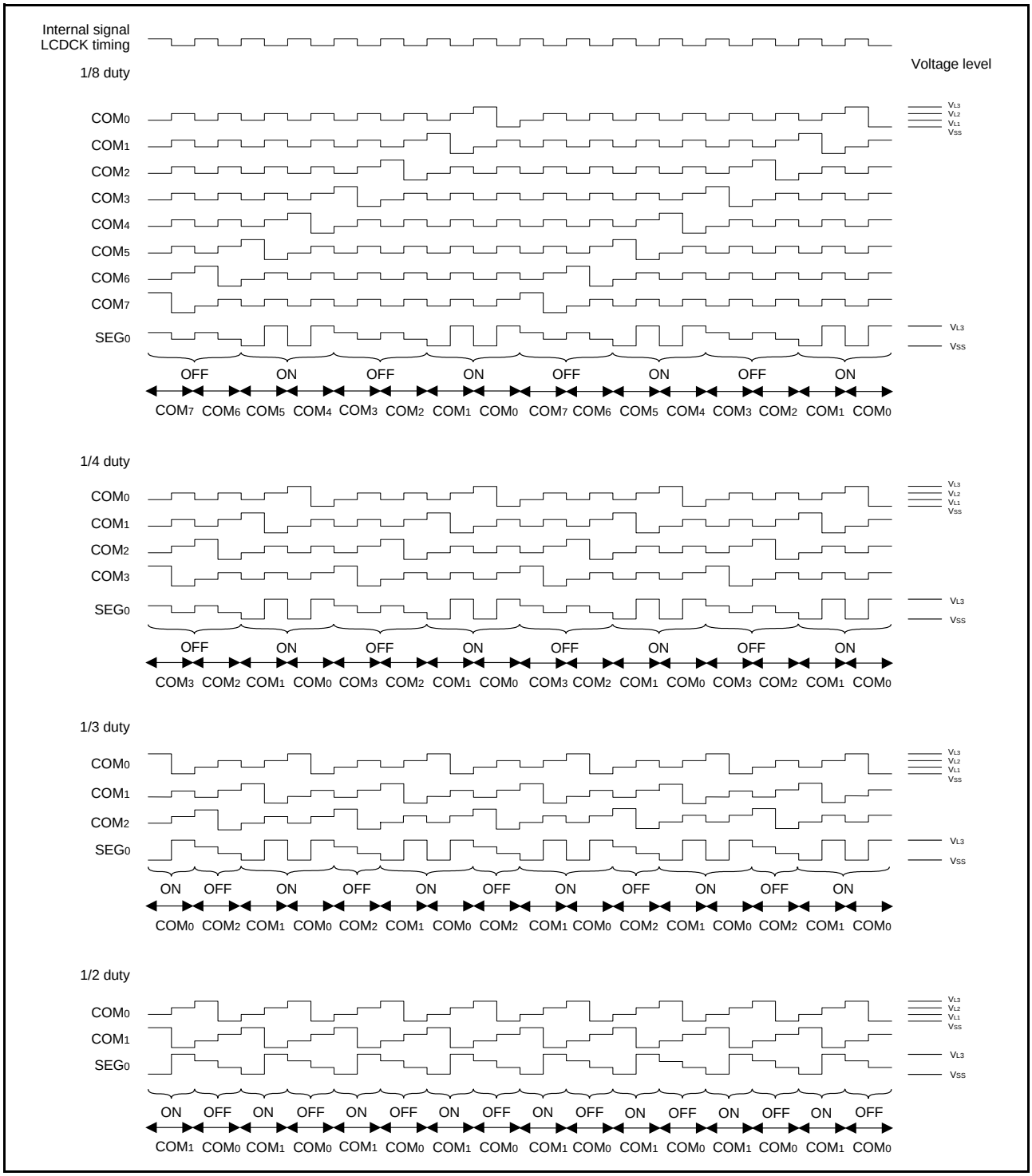


Fig. 48 LCD drive waveform (1/3 bias)

ROM CORRECTION FUNCTION

A part of program in ROM can be corrected.
Set the start address of the corrected ROM data (i.e. an Op code address of the beginning instruction) to the ROM correction address high-order and low-order registers.
When the program is being executed and the value of the program counter matches with the set address value in the ROM correction address registers, the program is branched to the ROM correction vectors and then the correction program can be executed by setting it to the ROM correction vectors.
Use the JMP instruction (3-byte instruction) to return the main program from the correction program.
The correctable area is up to two. There are two vectors for ROM correction.
Also, ROM correction vector can be selected from the RAM area or ROM area by the ROM correction memory selection bit.

	RAM area RC2 = "0"	ROM area RC2 = "1"
Vector 1	address 0100_{16}	address $F100_{16}$
Vector 2	address 0120_{16}	address $F120_{16}$

The ROM correction function is controlled by the ROM correction address 1 enable bit and ROM correction address 2 enable bit.
If the ROM correction function is not used, the ROM correction vector may be used as normal RAM/ROM. When using the ROM correction vector as normal RAM/ROM, make sure to set bits 1 and 0 in the ROM correction enable register to "0" (Disable).

<Notes>

1. When using the ROM correction function, set the ROM correction address registers and then enable the ROM correction with the ROM correction enable register.
2. Do not set addresses other than the ROM area in the ROM correction address registers.
   Do not set the same ROM correction addresses in both the ROM correction address registers 1 and ROM correction address registers 2.
3. It is necessary to contain the process for ROM correction in the program.

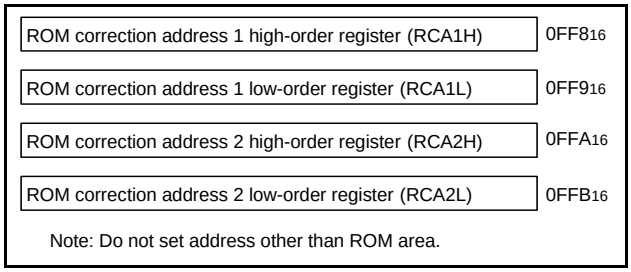


Fig. 49 ROM correction address register

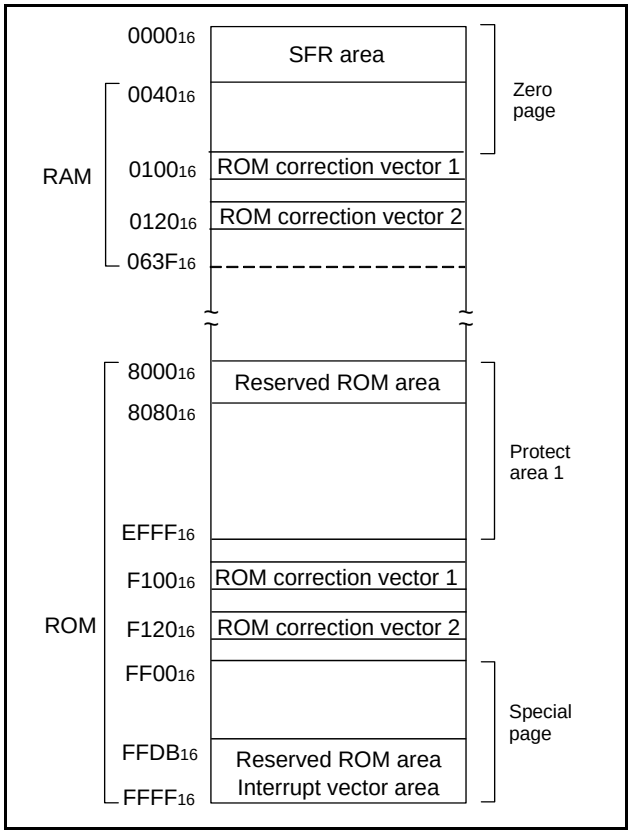


Fig. 50 Memory map of M38D58G8

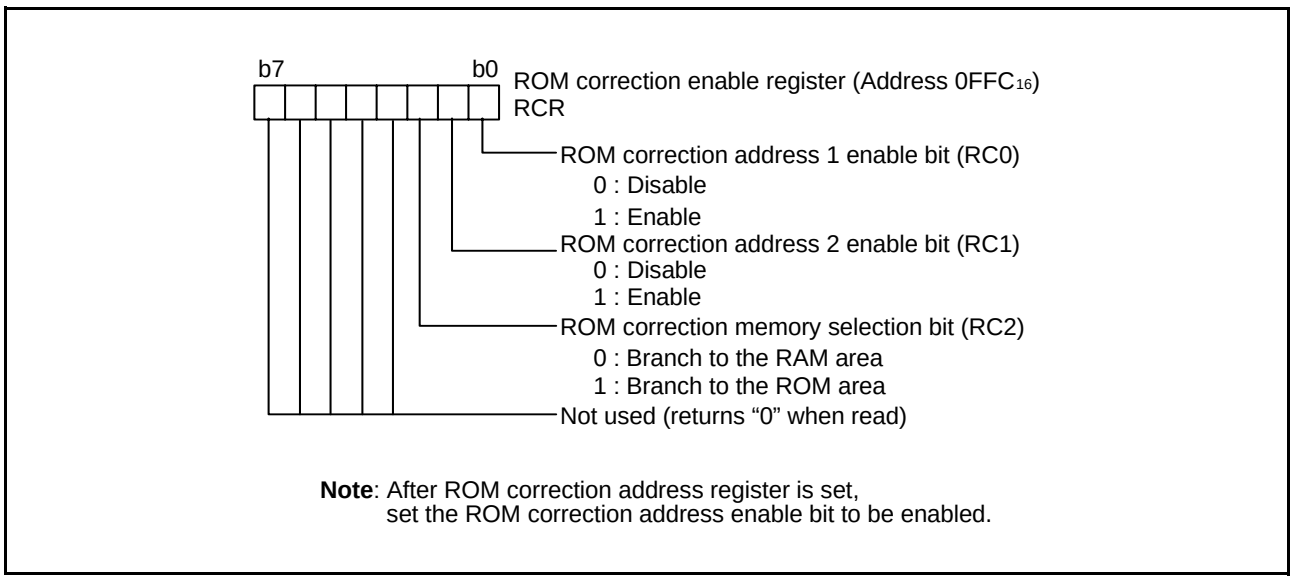


Fig. 51 Structure of ROM correction enable register

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit counter.

• Initial Value of Watchdog Timer

At reset or writing to the watchdog timer control register, each watchdog timer is set to "FF16". Instructions such as STA, LDM and CLB to generate the write signals can be used.
The written data in bits 7, 6 or 5 are not valid, and the above values are set.
Bits 7 to 5 can be rewritten only once after releasing reset.
After rewriting it is disable to write any data to this bit. This bit becomes "0" after reset.

• Standard Operation of Watchdog Timer

The watchdog timer is in the stop state at reset and the watchdog timer starts to count down by writing an optional value in the watchdog timer control register. An internal reset occurs at an underflow of the watchdog timer. Then, reset is released after the reset release time is elapsed, the program starts from the reset vector address.
Normally, writing to the watchdog timer control register before an underflow of the watchdog timer is programmed. If writing to the watchdog timer control register is not executed, the watchdog timer does not operate.
When reading the watchdog timer control register is executed, the contents of the high-order 5-bit counter, the count source selection bit 2 (bit 5), the STP instruction function selection bit (bit 6), and the count source selection bit (bit 7) are read out.

• Bit 6 of Watchdog Timer Control Register

1. When bit 6 of the watchdog timer control register is "0", the MCU enters the stop mode by execution of STP instruction. Just after releasing the stop mode, the watchdog timer restarts counting (Note 1). When executing the WIT instruction, the watchdog timer does not stop.
2. When bit 6 is "1", execution of STP instruction causes an internal reset. When this bit is set to "1" once, it cannot be rewritten to "0" by program. Bit 6 is "0" at reset.
3. The time until the underflow of the watchdog timer register after writing to the watchdog timer control register is executed is as follows (when the bit 7 of the watchdog timer control register is "0");
4. at XIN mode (f(XIN) = 8 MHz): 32.768 ms
5. at low-speed mode (f(XCIN) = 32 KHz): 8.19s

<Notes>

1. The watchdog timer continues to count even during the wait time set by timer 1 and timer 2 to release the stop state and in the wait mode. Accordingly, write to the watchdog timer control register to not underflow the watchdog timer in this time.
2. When the on-chip oscillator is selected by the watchdog timer count source selection bit 2, the on-chip oscillator forcibly oscillates and it cannot be stopped. Also, in this time, set the STP instruction function selection bit to "1" at this time.
   Select "0" (ϕSOURCE) the watchdog timer count source selection bit 2 at the system which on-chip oscillator is stopped.

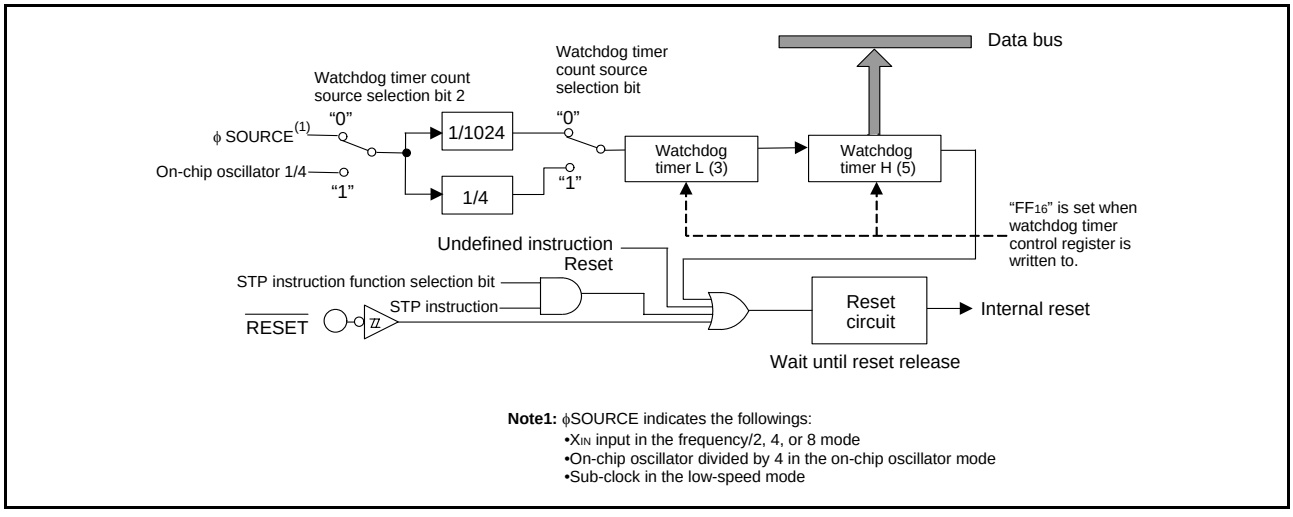


Fig. 52 Block diagram of Watchdog timer

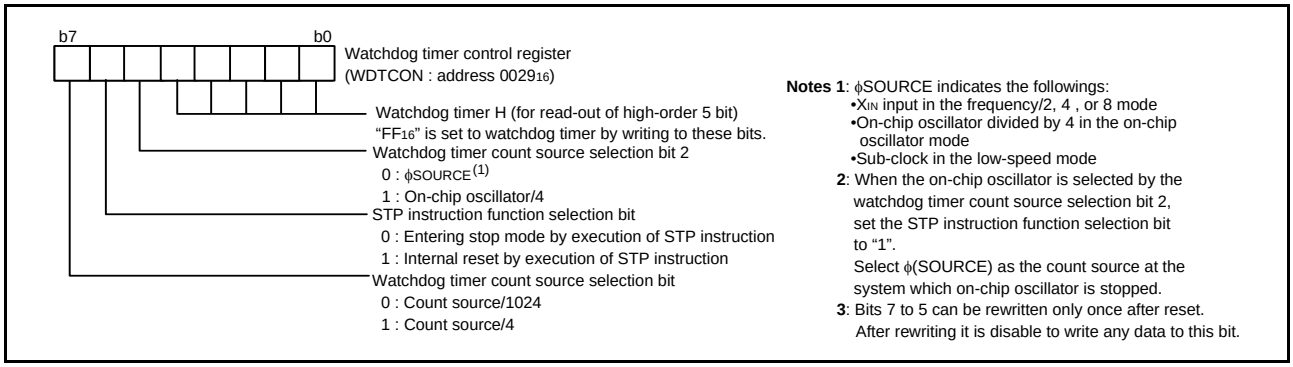


Fig. 53 Structure of Watchdog timer control register

CLOCK OUTPUT FUNCTION

A system clock ϕ can be output from I/O port P72. The triple function of I/O port, timer 2 output function and system clock ϕ output function are controlled by the clock output control register (address 0FF316) and the timer 2 output selection bit of the timer 12 mode register (address 002516).
In order to output a system clock ϕ from I/O port P72, set the timer 2 output selection bit to "1" and P72 clock output control bits of the clock output control register to "01". In order to output the same signal as oscillation frequency of sub clock XCIN, set the P72 clock output control bits to "10". When the clock output function is selected, a clock is output while the direction register of port P72 is set to the output mode.
P72 is switched to the port output or the output (timer 2 output or the clock output) except port at the cycle after the timer 2 output selection bit is switched.

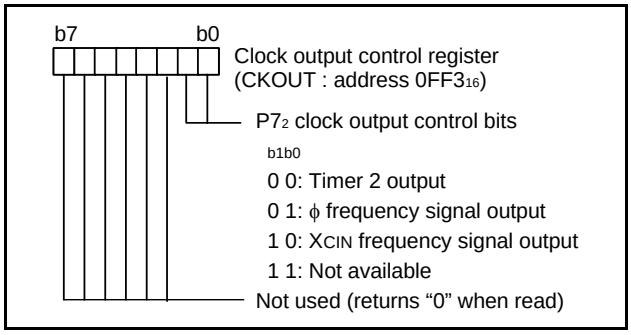


Fig. 54 Structure of clock output control register

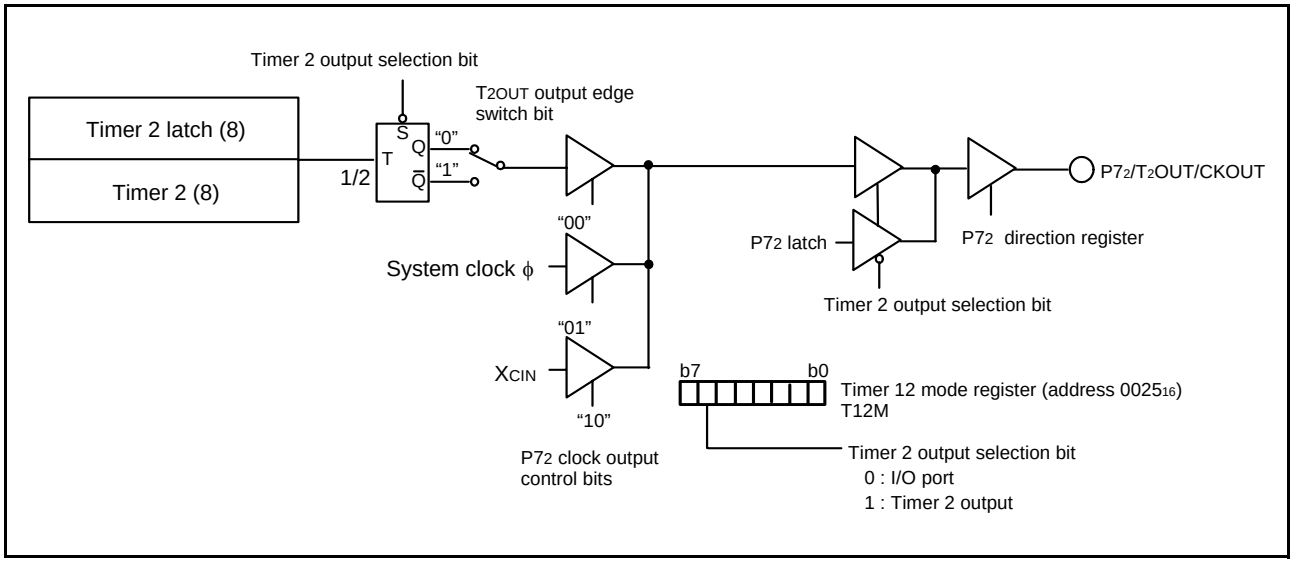


Fig. 55 Block diagram of Clock output function

Other function registers

[RRF register (RRFR)]

The RRF register (address 001216) is the 8-bit register and does not have the control function.
As for the value written in this register, high-order 4 bits and low-order 4 bits interchange.
It is initialized after reset.

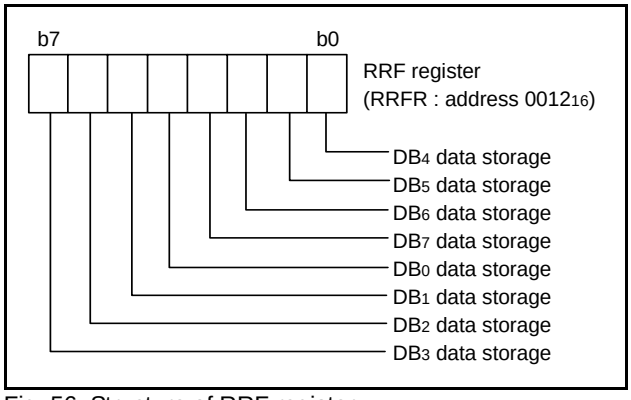


Fig. 56 Structure of RRF register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 µs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between V_{CC} (min.) and 5.5 V), reset is released.

After the reset is completed, the program starts from the address contained in address FFFD16 (high-order byte) and address FFFC16 (low-order byte). Make sure that the reset input voltage meets V_{IL} spec. When a power source voltage passes V_{CC} (min.).

In the flash memory version, input to the $\overline{\text{RESET}}$ pin in the following procedure.

• When power source is stabilized

(1) Input "L" level for 2µs or more to $\overline{\text{RESET}}$ pin.

(2) Input "H" level to $\overline{\text{RESET}}$ pin.

• At power-on

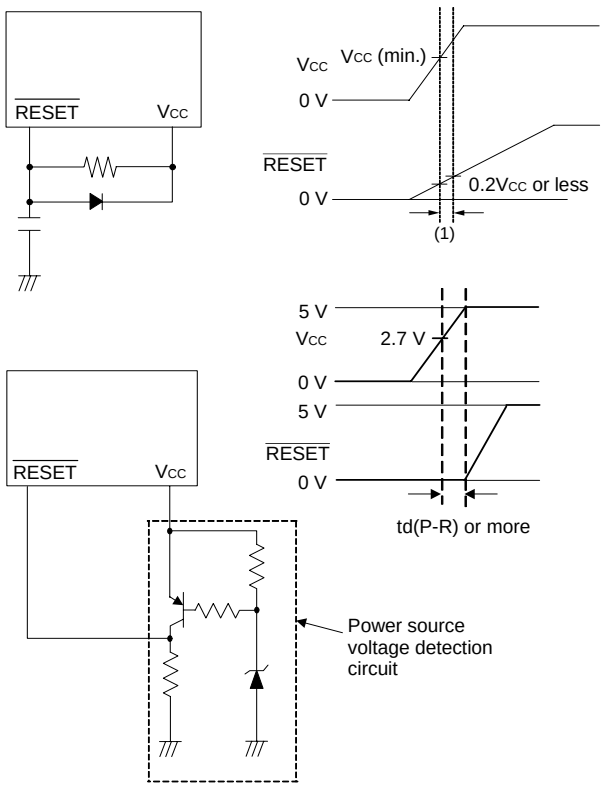
(1) Input "L" level to $\overline{\text{RESET}}$ pin.

(2) Increase the power source voltage to 2.7 V.

(3) Wait for td(P-R) until internal power source has stabilized.

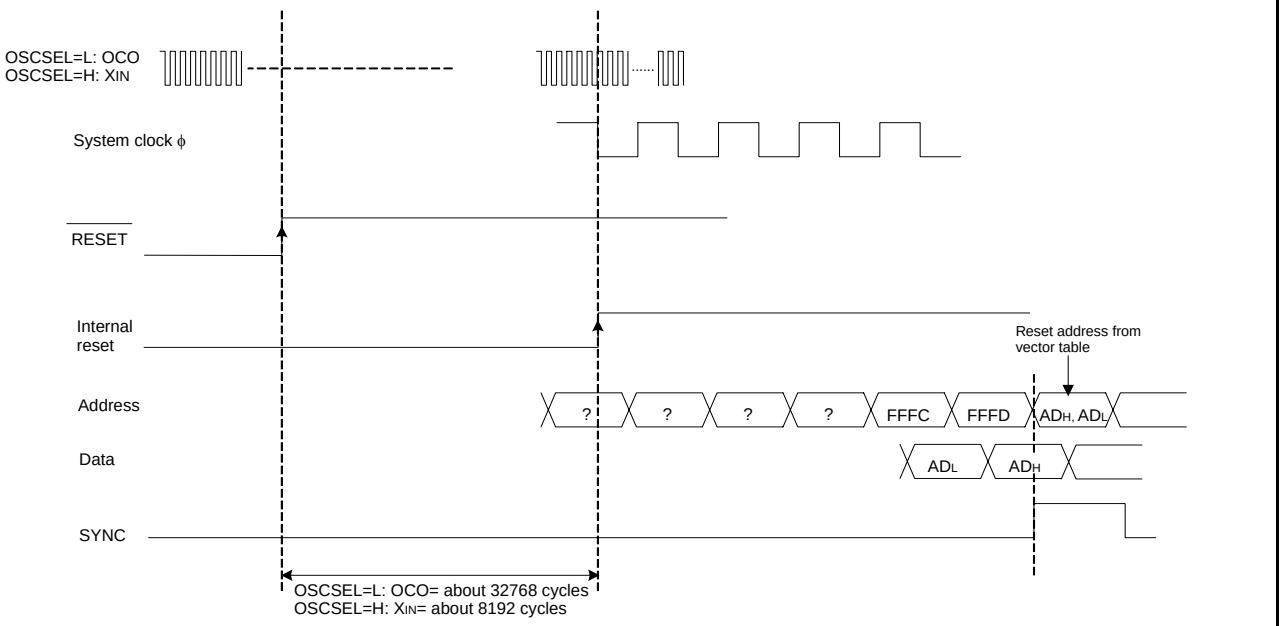
(4) Input "H" level to $\overline{\text{RESET}}$ pin.

In the QzROM version, the input level applied to the OSCSEL pin is determined when the $\overline{\text{RESET}}$ pin changes from "L" to "H".



Note 1: QzROM version: 2 µs or more
Flash memory version: td(P-R) or more

Fig. 57 Reset circuit example



Notes 1: The frequency of system clock ϕ is f(OCO)/32 or f(XIN)/8.

2: The question marks (?) indicate an undefined state.

3: In the QzROM version, the input level applied to the OSCSEL pin is determined when the $\overline{\text{RESET}}$ pin changes from "L" to "H".

Fig. 58 Reset sequence

		Address	Register contents
(1)	Port P0	0000_{16}	00_{16}
(2)	Port P0 direction register	0001_{16}	00_{16}
(3)	Port P1	0002_{16}	00_{16}
(4)	Port P1 direction register	0003_{16}	00_{16}
(5)	Port P2	0004_{16}	00_{16}
(6)	Port P2 direction register	0005_{16}	00_{16}
(7)	Port P3	0006_{16}	00_{16}
(8)	Port P3 direction register	0007_{16}	00_{16}
(9)	Port P4	0008_{16}	00_{16}
(10)	Port P4 direction register	0009_{16}	00_{16}
(11)	Port P5	$000A_{16}$	00_{16}
(12)	Port P5 direction register	$000B_{16}$	00_{16}
(13)	Port P6	$000C_{16}$	00_{16}
(14)	Port P6 direction register	$000D_{16}$	00_{16}
(15)	Port P7	$000E_{16}$	00_{16}
(16)	Port P7 direction register	$000F_{16}$	00_{16}
(17)	CPU mode register 2	0011_{16}	0 0 0 0 0 0 0 *
(18)	RRF register	0012_{16}	00_{16}
(19)	LCD mode register 1	0013_{16}	00_{16}
(20)	LCD mode register 2	0014_{16}	00_{16}
(21)	AD control register	0015_{16}	08_{16}
(22)	Serial I/O1 status register	0019_{16}	1 0 0 0 0 0 0 0
(23)	Serial I/O1 control register	$001A_{16}$	00_{16}
(24)	UART control register	$001B_{16}$	1 1 1 0 0 0 0 0
(25)	Serial I/O2 control register	$001D_{16}$	00_{16}
(26)	Timer 1	0020_{16}	FF_{16}
(27)	Timer 2	0021_{16}	01_{16}
(28)	Timer 3	0022_{16}	FF_{16}
(29)	Timer 4	0023_{16}	FF_{16}
(30)	PWM01 register	0024_{16}	00_{16}
(31)	Timer 12 mode register	0025_{16}	00_{16}
(32)	Timer 34 mode register	0026_{16}	00_{16}
(33)	Timer 1234 mode register	0027_{16}	00_{16}
(34)	Timer 1234 frequency division selection register	0028_{16}	00_{16}
(35)	Watchdog timer control register	0029_{16}	0 0 0 1 1 1 1 1

		Address	Register contents
(36)	Timer X (low-order)	$002A_{16}$	FF_{16}
(37)	Timer X (high-order)	$002B_{16}$	FF_{16}
(38)	Timer X (extension)	$002C_{16}$	00_{16}
(39)	Timer X mode register	$002D_{16}$	00_{16}
(40)	Timer X control register 1	$002E_{16}$	00_{16}
(41)	Timer X control register 2	$002F_{16}$	00_{16}
(42)	Compare register 1 (low-order)	0030_{16}	00_{16}
(43)	Compare register 1 (high-order)	0031_{16}	00_{16}
(44)	Compare register 2 (low-order)	0032_{16}	00_{16}
(45)	Compare register 2 (high-order)	0033_{16}	00_{16}
(46)	Compare register 3 (low-order)	0034_{16}	00_{16}
(47)	Compare register 3 (high-order)	0035_{16}	00_{16}
(48)	Timer Y (low-order)	0036_{16}	FF_{16}
(49)	Timer Y (high-order)	0037_{16}	FF_{16}
(50)	Timer Y mode register	0038_{16}	00_{16}
(51)	Timer Y control register	0039_{16}	00_{16}
(52)	Interrupt edge selection register	$003A_{16}$	00_{16}
(53)	CPU mode register	$003B_{16}$	* 1 * 0 0 0 0 0
(54)	Interrupt request register 1	$003C_{16}$	00_{16}
(55)	Interrupt request register 2	$003D_{16}$	00_{16}
(56)	Interrupt control register 1	$003E_{16}$	00_{16}
(57)	Interrupt control register 2	$003F_{16}$	00_{16}
(58)	PULL register 1	$0FF0_{16}$	00_{16}
(59)	PULL register 2	$0FF1_{16}$	00_{16}
(60)	PULL register 3	$0FF2_{16}$	00_{16}
(61)	Clock output control register	$0FF3_{16}$	00_{16}
(62)	Segment output disable register 0	$0FF4_{16}$	FF_{16}
(63)	Segment output disable register 1	$0FF5_{16}$	FF_{16}
(64)	Segment output disable register 2	$0FF6_{16}$	$0F_{16}$
(65)	Key input control register	$0FF7_{16}$	00_{16}
(66)	ROM correction address 1(high-order)	$0FF8_{16}$	00_{16}
(67)	ROM correction address 1(low-order)	$0FF9_{16}$	00_{16}
(68)	ROM correction address 2 (high-order)	$0FFA_{16}$	00_{16}
(69)	ROM correction address 2 (low-order)	$0FFB_{16}$	00_{16}
(70)	ROM correction enable register	$0FFC_{16}$	00_{16}
(71)	Processor status register	(PS)	× × × × × 1 × ×
(72)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

×: Not fixed
*: Depends on OSCSEL setting at the QzROM version.
In the flash memory version, the CPU mode register 2 (address 0011_{16}), is set to "00_{16}" and the CPU mode register (address $003B_{16}$) is set to "$E0_{16}$".
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 59 Internal status at reset

CLOCK GENERATING CIRCUIT

The oscillation circuit of 38D5 Group can be formed by connecting an oscillator, capacitor and resistor between XIN and XOUT (XCIN and XCOUT). To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open. The clocks that are externally generated cannot be directly input to XCIN. Use the circuit constants in accordance with the oscillator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. (An external feed-back resistor may be needed depending on conditions.) However, an about 10 MΩ external feedback resistor is needed between XCIN and XCOUT.

The 38D5 Group operation mode immediately after reset depends on the OSCSEL pin state in the QzROM version.

When the OSCSEL pin state is GND level, the only on-chip oscillator starts oscillating. The XIN-XOUT oscillation stops oscillating, and XCIN and XCOUT pins function as I/O ports. Flash memory version as same.

When the OSCSEL pin state is VCC level, the XIN-XOUT oscillation divided by 8 starts oscillating. The on-chip oscillator stops oscillating, and the XCIN and XCOUT pins function as I/O ports.

Note the following in each mode.

• XIN Mode

The XIN-XOUT oscillation does not stop even if the XIN-XOUT oscillation stop bit is set to "1".

• Low-Speed Mode

The XCIN-XCOUT oscillation stops if the port XC switch bit is set to "0".

• On-Chip Oscillator Mode

Even if the on-chip oscillator stop bit is set to "1", the on-chip oscillator oscillation does not stop in the flash memory version, but stops in the QzROM version.

• Frequency Control

(1) On-chip oscillation mode

The system clock ϕ is the on-chip oscillator oscillation divided by 32.

(2) XIN mode

Frequency/2 mode, frequency/4 mode, and frequency/8 mode are collectively referred as XIN mode.

- Frequency/8 Mode
  The system clock ϕ is the frequency of XIN divided by 8.
- Frequency/4 Mode
  The system clock ϕ is the frequency of XIN divided by 4.
- Frequency/2 Mode
  The system clock ϕ is half the frequency of XIN.

(3)Low-speed Mode

The system clock ϕ is half the frequency of sub clock.

After reset and when system returns from the stop mode, the operation mode depends on the OSCSEL pin state in the QzROM version and the flash memory version operation mode is the on-chip oscillator mode.

When the $\overline{\text{RESET}}$ pin changes from "L" to "H" and when the STP instruction is executed, determine the input level applied to the OSCSEL pin.

Refer to the clock state transition diagram for the setting of transition to each mode.

The XIN-OUT oscillation is controlled by the bit 5 of CPUM, and the sub-clock oscillation is controlled by the bit 4 of CPUM and the on-chip oscillator oscillation is controlled by the bit 0 of CPUM2.

In the on-chip oscillator mode, the oscillation by the oscillator can be stopped. In the low-speed mode, the power consumption can be reduced by stopping the XIN–XOUT oscillation.

In low-speed mode, the on-chip oscillator stops in the QzROM version regardless of the on-chip oscillator stop bit value. The on-chip oscillator does not stop in the flash memory version, so set the on-chip oscillator stop bit to "1" to stop the oscillation. Set enough time for oscillation to stabilize by programming to restart the stopped oscillation and switch the operation mode. Also, set enough time for oscillation to stabilize by programming to switch the timer count source.

<Notes on Clock Generating Circuit>

If you switch the mode between on-chip oscillator mode, XIN mode and low-speed mode, stabilize both XIN and XCIN oscillations. Especially be careful immediately after power-on and at returning from stop mode. Refer to the clock state transition diagram for the setting of transition to each mode. Set the frequency in the condition that f(XIN) > 3•f(XCIN).

When the XIN mode is not used (XIN-XOUT oscillation and external clock input are not performed), connect XIN to VCC through a resistor.

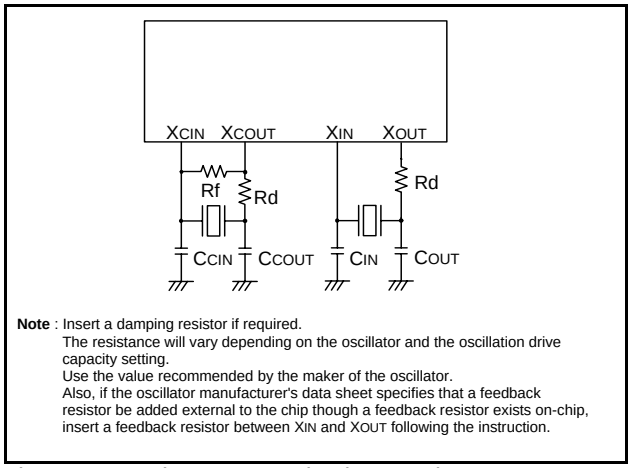
• **Oscillation Control**

(1) Stop Mode

If the STP instruction is executed, the system clock ϕ stops at an "H" level, and main clock and sub-clock oscillators stop.
In this time, values set previously to timer 1 latch and timer 2 latch are loaded automatically to timer 1 and timer 2. Set the values * to generate the wait time required for oscillation stabilization to timer 1 latch and timer 2 latch (low-order 8 bits of timer 1 and high-order 8 bits of timer 2) before the STP instruction.
The frequency divider for timer 1 is used for the timer 1 count source, and the output of timer 1 is forcibly connected to timer 2. In this time, bits 0 to 5 of the timer 12 mode register are cleared to "0".
The values of the timer 12 frequency divider selection register are not changed.
Set the interrupt enable bits of the timer 1 and timer 2 to be disabled ("0") before executing the STP instruction.
*: Reference (Set values according to your oscillator and system.)
OSCSEL = "L" of the QzROM version and flash memory version:
..... 0005_{16} or more
OSCSEL = "H" of the QzROM version:
..... $01FF_{16}$ or more
When an external interrupt is received, the clock set according to the OSCSEL pin state starts oscillating in the QzROM version. The operation mode at returning is decided by the clock that set according to the OSCSEL pin state.
Bits 3, 5, 6, and 7 of CPUM and bit 0 of CPUM2 are forcibly changed by the OSCSEL pin state. In the flash memory version, the on-chip oscillator starts oscillating and the operation mode at returning is set to on-chip oscillator mode. The bit 3 of CPUM is changed to "0", bits 5, 6 and 7 of CPUM are changed to "1", and the bit 0 of CPUM2 is changed to "0" forcibly.
Oscillator restarts when reset occurs or an interrupt request is received, but the system clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

(2) Wait Mode

If the WIT instruction is executed, only the system clock ϕ stops at an "H" state. The states of main clock, on-chip oscillator and sub clock are the same as the state before executing the WIT instruction, and oscillation does not stop. Since supply of system clock ϕ is started immediately after the interrupt is received, the instruction can be executed immediately.



Note : Insert a damping resistor if required.
The resistance will vary depending on the oscillator and the oscillation drive capacity setting.
Use the value recommended by the maker of the oscillator.
Also, if the oscillator manufacturer's data sheet specifies that a feedback resistor be added external to the chip though a feedback resistor exists on-chip, insert a feedback resistor between XIN and XOUT following the instruction.

Fig. 60 Ceramic resonator circuit example

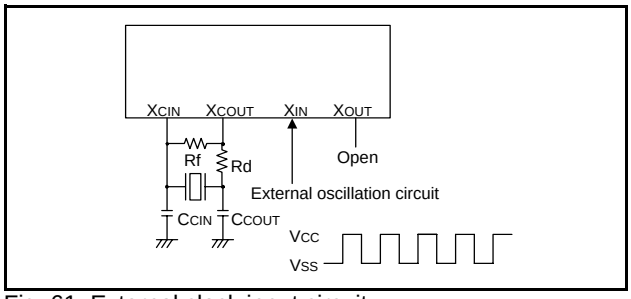
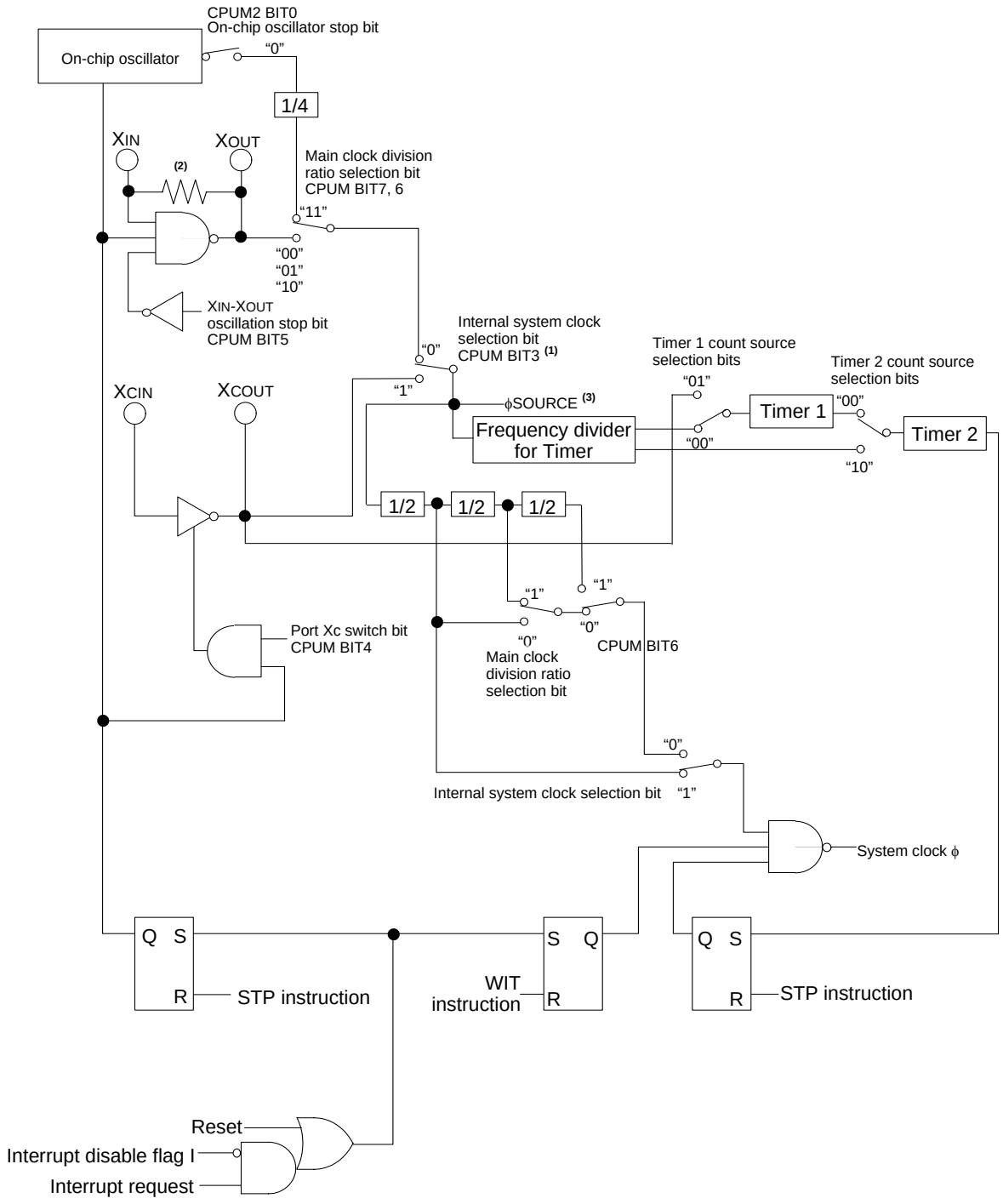


Fig. 61 External clock input circuit



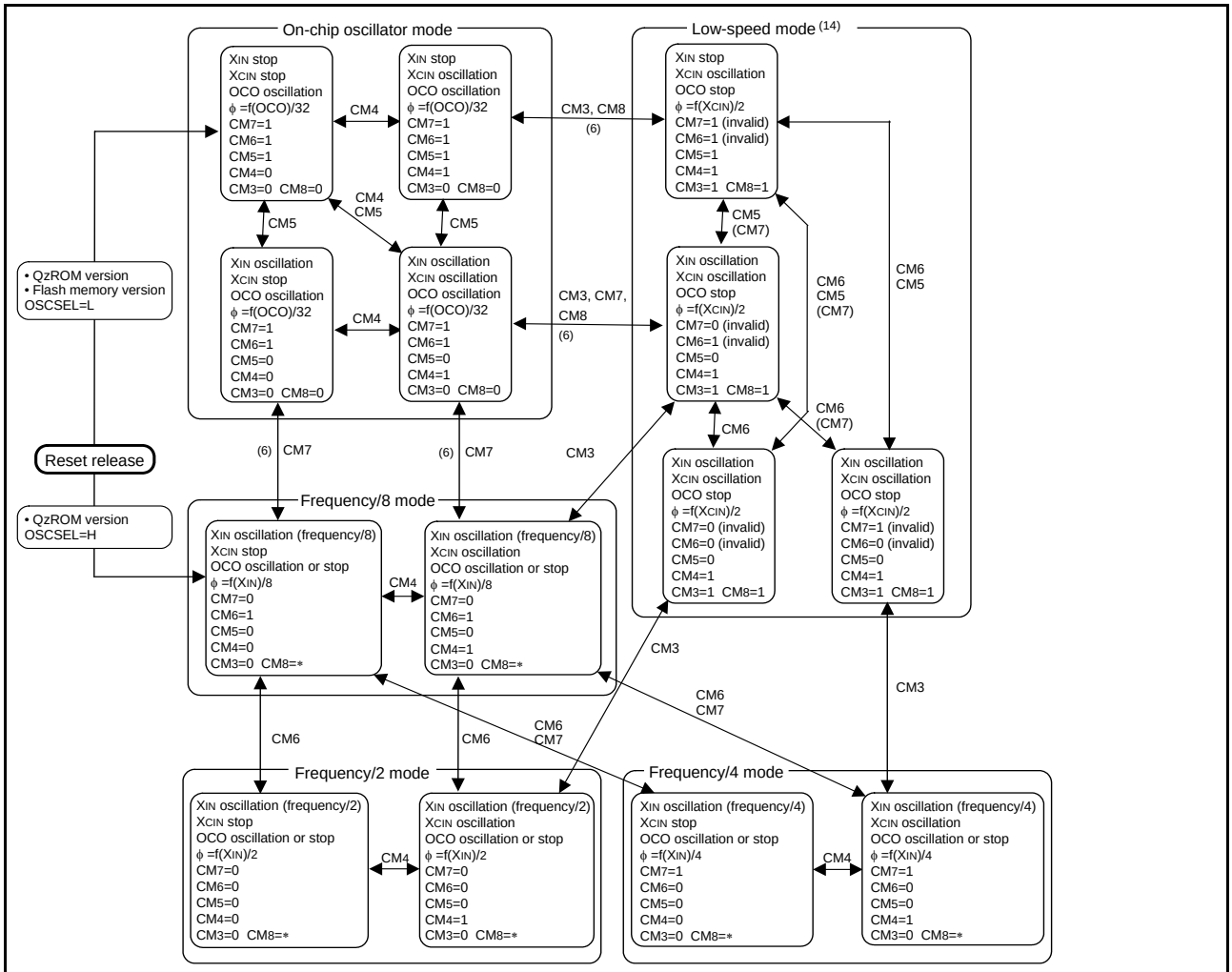
Notes 1: When the XCIN-XCOUT oscillation is selected as the system clock, set the port Xc switch bit to "1".

2: Although a feed-back resistor exists on-chip, an external feed-back resistor may be needed depending on conditions.

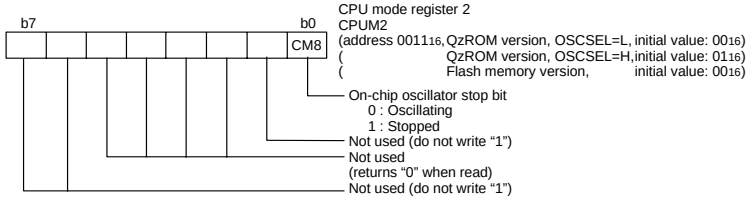
3: φSOURCE indicates the followings:
- •XIN input in the frequency/2, 4, or 8 mode
- •On-chip oscillator divided by 4 in the on-chip oscillator mode
- •Sub-clock in the low-speed mode

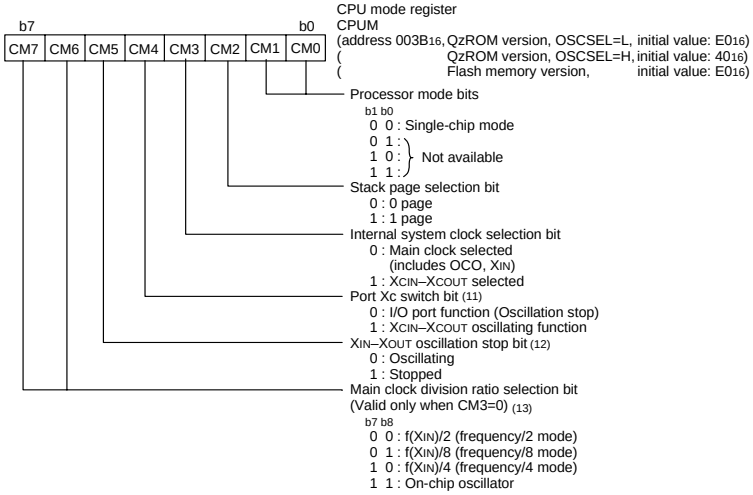
However, when used as the A/D conversion clock by the A/D converter, φSOURCE indicates the followings:
- •XIN input in the frequency/2, 4, or 8 mode
- •On-chip oscillator divided by 4 in the low-speed or the on-chip oscillator mode

Fig. 62 Clock generating circuit block diagram



* : The OCO oscillating at "0"; the OCO stopped at "1".





Notes
1: Switch the mode by the arrows shown between the mode blocks. The all modes can be switched to the stop mode or the wait mode.
2: Timer and LCD operate in the wait mode. System is returned to the source mode when the wait mode is ended.
3: The CM4 value is retained in the stop mode. When the stop mode is ended, the operation mode varies as follows:
In the QzROM version: Mode set by the OSCSEL pin state
In the flash memory version: On-chip oscillator mode
The input level applied to the OSCSEL pin is determined when executing the STP instruction.
4: Before executing the STP instruction, set the values to generate the wait time required for oscillation stabilization to timer 1 and timer 2, and set to "0" (interrupts disabled) to the interrupt enable bits of timer 1 and timer 2.
5: Execute the transition after the oscillation used in the destination mode is stabilized.
6: When system goes to on-chip oscillator mode, the oscillation stabilizing wait time is not needed.
7: The on-chip oscillator can be stopped in all kinds of state of frequency/2,4 mode.
8: In all XIN mode, stop of on-chip oscillator is enabled.
9: The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. f(OCO) indicates the oscillation frequency of on-chip oscillator.
10: When selecting the on-chip oscillator for the WDT clock, the on-chip oscillator does not stop.
Also, in low-speed mode, the on-chip oscillator stops in the QzROM version regardless of the on-chip oscillator stop bit value. The on-chip oscillator does not stop in the flash memory version, so set this bit to "1" to stop the oscillation.
In on-chip oscillator mode, even if this bit is set to "1", the on-chip oscillator oscillation does not stop in the flash memory version, but stops in the QzROM version.
11: In low-speed mode, the XCIN-XCOUT oscillation stops if the port XC switch bit is set to "0".
12: In XIN mode, the XIN-XOUT oscillation does not stop even if the XIN-XOUT oscillation stop bit is set to "1".
13: 12.5 MHz < f(XIN) ≤ 16 MHz is not available in the frequency/2 mode.
14: In the flash memory version, set the on-chip oscillator stop bit to "1" (oscillation stops) because OCO is in the state set by the setting value of the on-chip oscillator stop bit.

Fig. 63 State transitions of system clock

QzROM Writing Mode

In the QzROM writing mode, the user ROM area can be rewritten while the microcomputer is mounted on-board by using a serial programmer which is applicable for this microcomputer.
Table 15 lists the pin description (QzROM writing mode) and Figure 64 and Figure 65 show the pin connections.
Refer to Figure 66 to Figure 69 for examples of a connection with a serial programmer.
Contact the manufacturer of your serial programmer for serial programmer. Refer to the user's manual of your serial programmer for details on how to use it.

Table 15 Pin description (QzROM writing mode)

Pin	Name	I/O	Function
V_{CC}, V_{SS}	Power source	Input	• Apply 2.7 to 5.5 V to V_{CC}, and 0 V to V_{SS}.
$\overline{RESET}$	Reset input	Input	• Reset input pin for active "L". Reset occurs when $\overline{RESET}$ pin is held at an "L" level for 16 cycles or more of X_{IN}.
X_{IN}	Clock input	Input	• Set the same termination as the single-chip mode.
X_{OUT}	Clock output	Output	
V_{REF}	Analog reference voltage	Input	• Input the reference voltage of A/D converter to V_{REF}.
AVss	Analog power source	Input	• Connect AVss to Vss.
$P0_0$–$P0_7$ $P1_0$–$P1_7$ $P2_0$–$P2_7$ $P3_3$–$P3_7$ $P4_0$, $P4_4$–$P4_7$ $P5_0$–$P5_7$ $P6_0$–$P6_7$ $P7_2$–$P7_4$	I/O port	I/O	• Input "H" or "L" level signal or leave the pin open.
$P7_0$, $P7_1$	Input port	Input	• Input "H" or "L" level signal or leave the pin open.
OSCSEL	V_{PP} input	Input	• QzROM programmable power source pin.
$P4_1$	ESDA input/output	I/O	• Serial data I/O pin.
$P4_2$	ESCLK input	Input	• Serial clock input pin.
$P4_3$	ESPGMB input	Input	• Read/program pulse input pin.

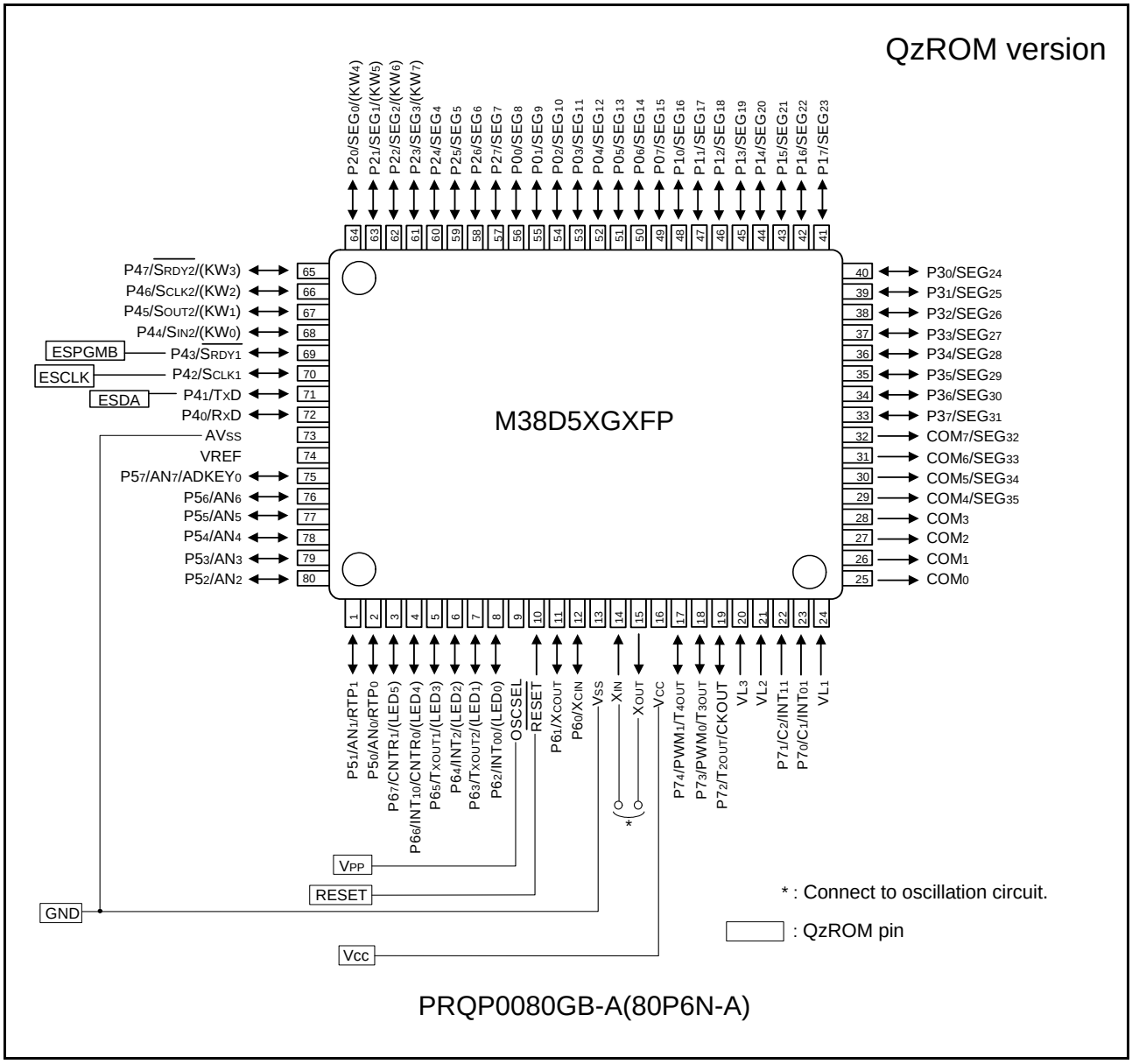


Fig. 64 Pin connection diagram (M38D5XGXFP)

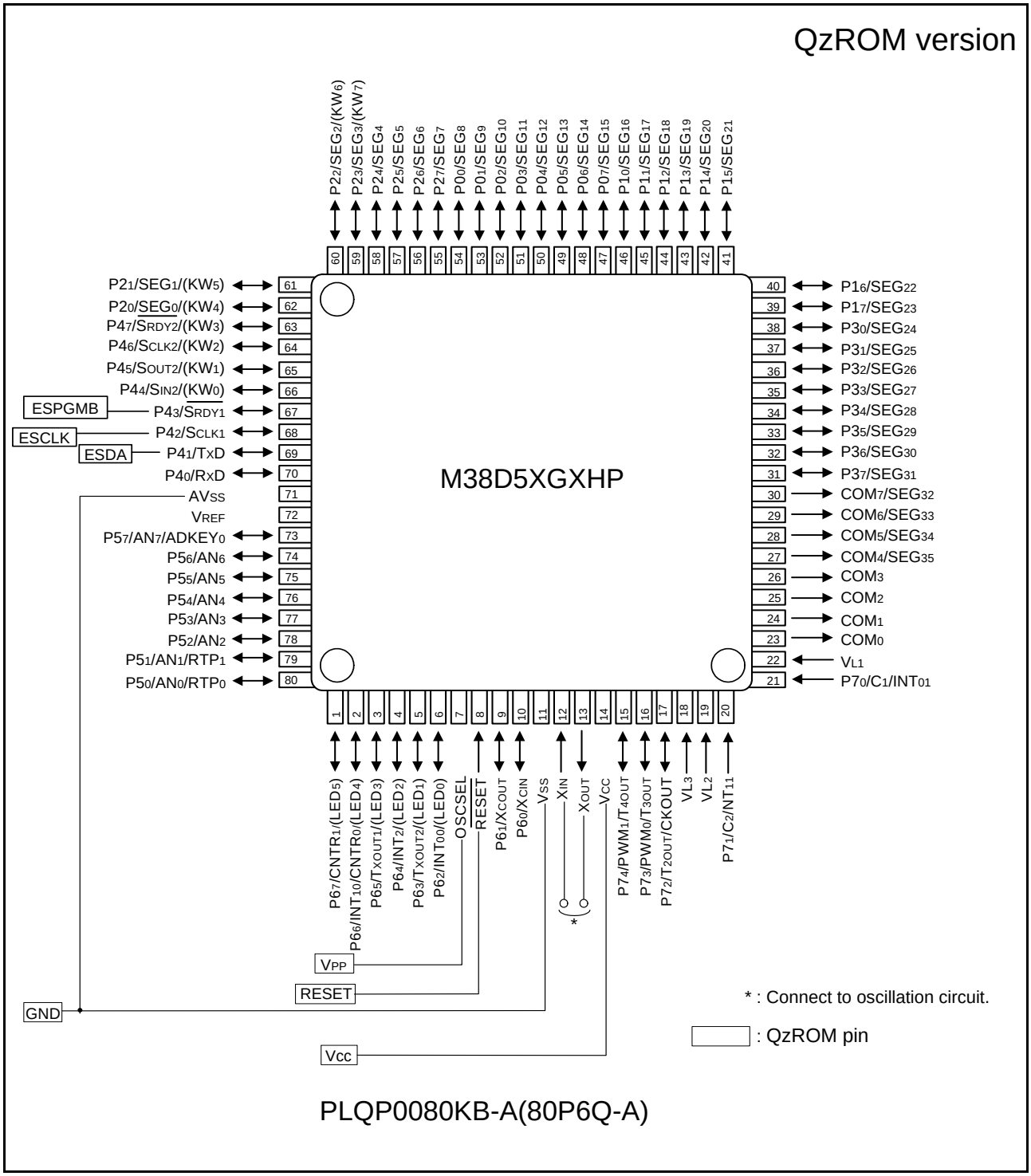
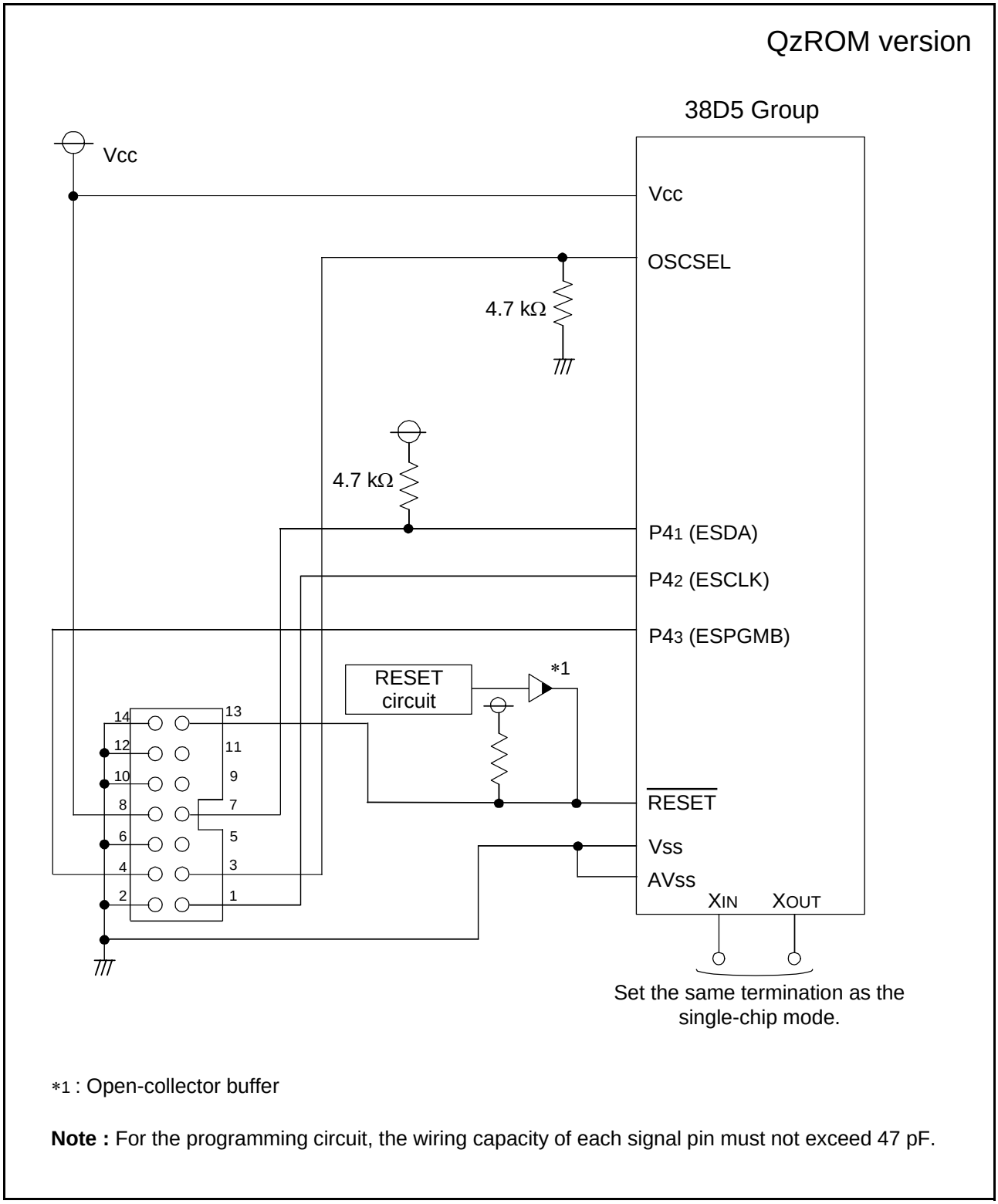


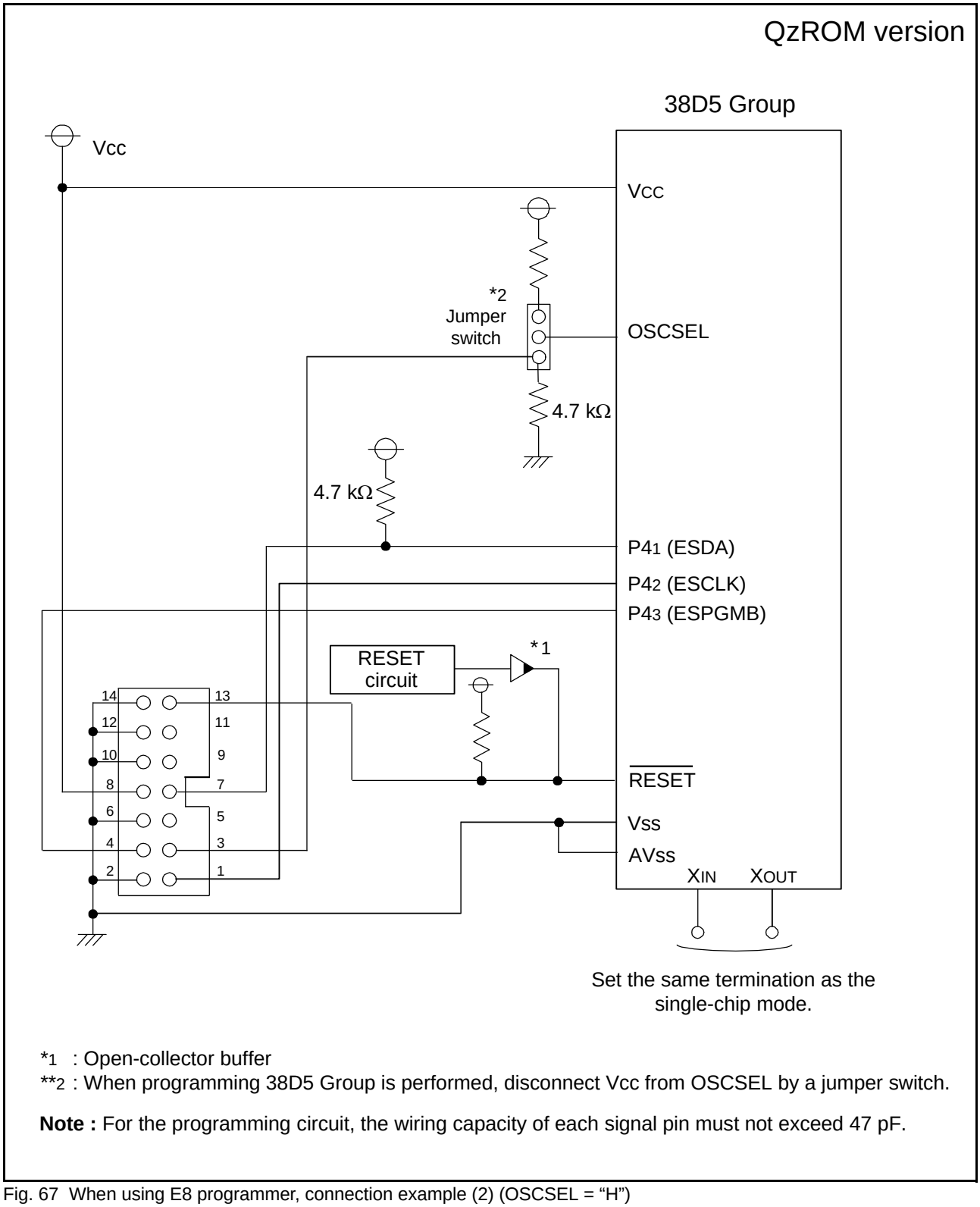
Fig. 65 Pin connection diagram (M38D5XGXHP)



*1 : Open-collector buffer

Note : For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

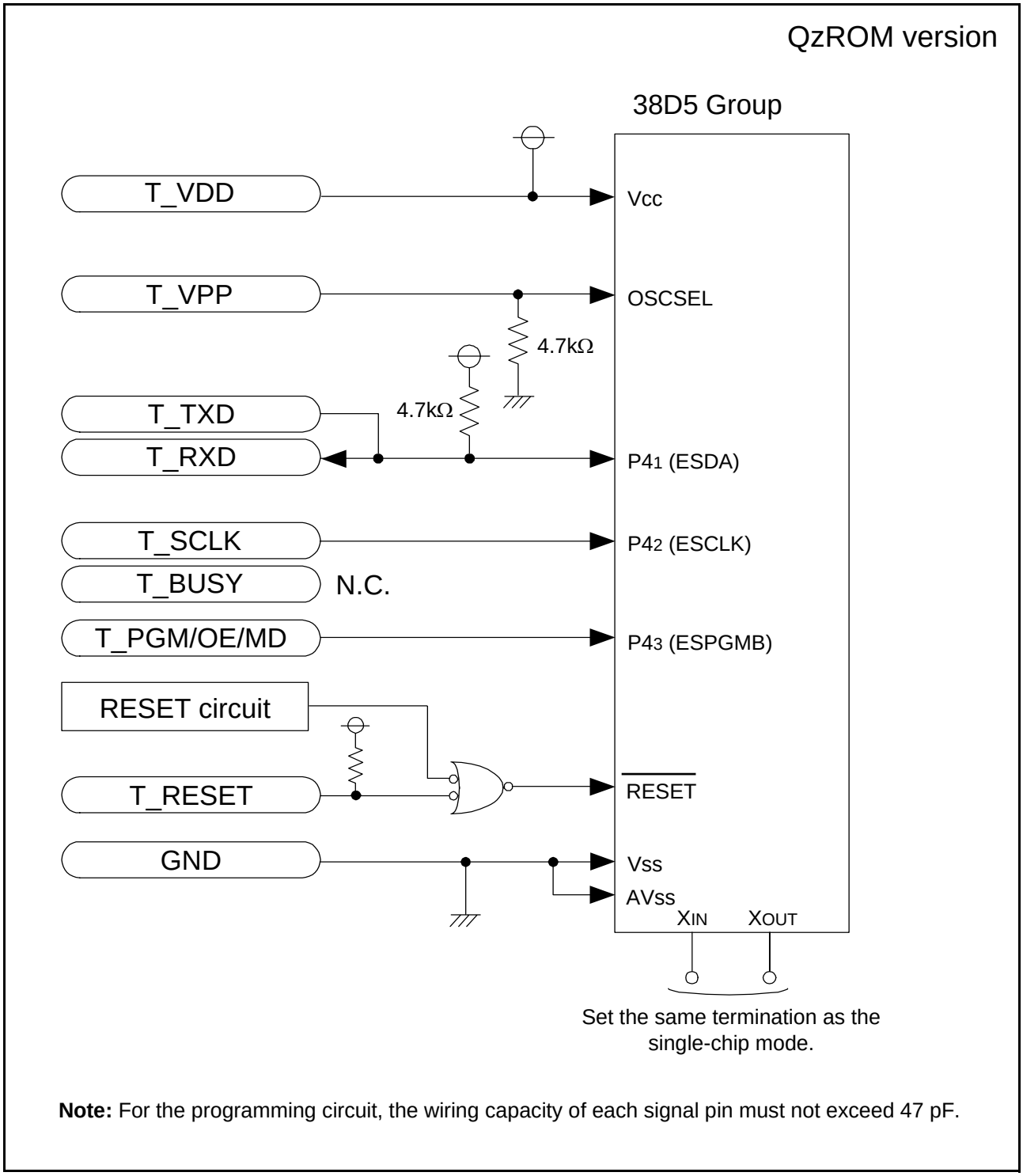
Fig. 66 When using E8 programmer, connection example (1) (OSCSEL = “L”)



*1 : Open-collector buffer
**2 : When programming 38D5 Group is performed, disconnect Vcc from OSCSEL by a jumper switch.

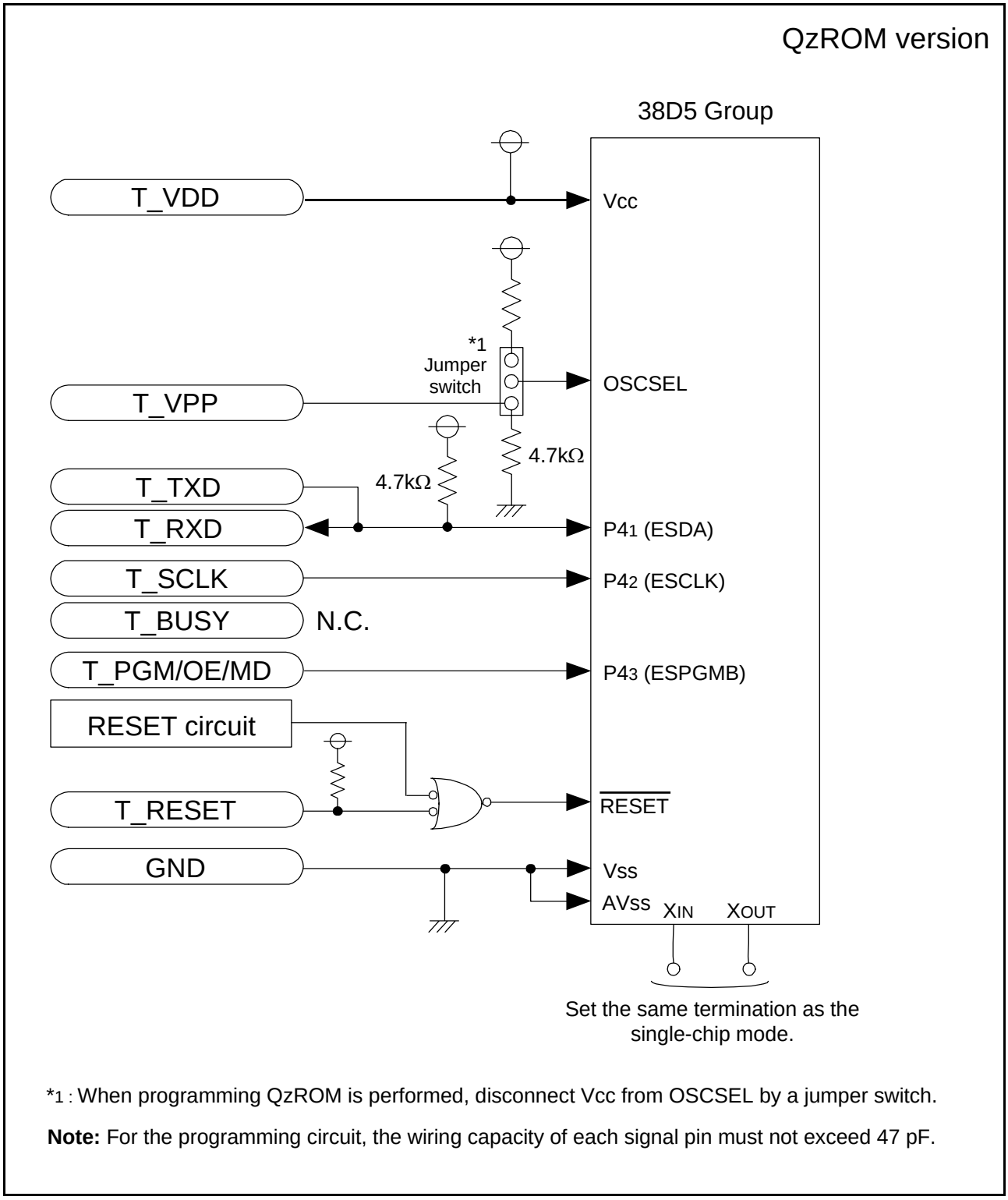
Note : For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig. 67 When using E8 programmer, connection example (2) (OSCSEL = “H”)



Note: For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig. 68 When using programmer of Suisei Electronics System Co., LTD, connection example (1) (OSCSEL = “L”)



*1 : When programming QzROM is performed, disconnect Vcc from OSCSEL by a jumper switch.

Note: For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig. 69 When using programmer of Suisei Electronics System Co., LTD, connection example (2) (OSCSEL = “H”)

FLASH MEMORY MODE

The 38D5 Group flash memory version has the flash memory that can be rewritten with a single power source.
For this flash memory, three flash memory modes are available in which to read, program, and erase: the parallel I/O and standard serial I/O modes in which the flash memory can be manipulated using a programmer and the CPU rewrite mode in which the flash memory can be manipulated by the Central Processing Unit (CPU). For details of each mode, refer to the next and after pages. Contact the manufacturer of your programmer for the programmer. Refer to the user's manual of your programmer for details on how to use it.

This flash memory version has some blocks on the flash memory as shown in Figure 70 and each block can be erased.
In addition to the ordinary User ROM area to store the MCU operation control program, the flash memory has a Boot ROM area that is used to store a program to control rewriting in CPU rewrite and standard serial I/O modes. This Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. However, the user can write a rewrite control program in this area that suits the user's application system. This Boot ROM area can be rewritten in only parallel I/O mode.

Performance overview

Table 16 lists the performance overview of the 38D5 Group flash memory version.

Table 16 Performance overview of 38D5 Group flash memory version

Parameter		Function
Power source voltage (Vcc)		V_{CC} = 2.7 to 5.5 V
Program/Erase VPP voltage (V_{PP})		V_{CC} = 2.7 to 5.5 V
Flash memory mode		3 modes; Parallel I/O mode, Standard serial I/O mode, CPU rewrite mode
Erase block division	User ROM area/Data ROM area	Refer to Figure 70.
	Boot ROM area (1)	Not divided (4K bytes)
Program method		In units of bytes
Erase method		Block erase
Program/Erase control method		Program/Erase control by software command
Number of commands		5 commands
Number of program/Erase times		100
ROM code protection		Available in parallel I/O mode and standard serial I/O mode

NOTE:
1. The Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. This Boot ROM area can be erased and written in only parallel I/O mode.

Boot Mode

The control program for CPU rewrite mode must be written into the User ROM or Boot ROM area in parallel I/O mode beforehand. (If the control program is written into the Boot ROM area, the standard serial I/O mode becomes unusable.)
See Figure 70 for details about the Boot ROM area.
Normal microcomputer mode is entered when the microcomputer is reset with pulling CNVSS pin low. In this case, the CPU starts operating using the control program in the User ROM area.
When the microcomputer is reset and the CNVSS pin high after pulling the P41/TxD pin and CNVSS pin high, the CPU starts operating (start address of program is stored into addresses FFFC16 and FFFD16) using the control program in the Boot ROM area. This mode is called the “Boot mode”. Also, User ROM area can be rewritten using the control program in the Boot ROM area.

Block Address

Block addresses refer to the maximum address of each block. These addresses are used in the block erase command.

CPU Rewrite Mode

In CPU rewrite mode, the internal flash memory can be operated on (read, program, or erase) under control of the Central Processing Unit (CPU).
In CPU rewrite mode, only the User ROM area shown in Figure 70 can be rewritten; the Boot ROM area cannot be rewritten. Make sure the program and block erase commands are issued for only the User ROM area and each block area.
The control program for CPU rewrite mode can be stored in either User ROM or Boot ROM area. In the CPU rewrite mode, because the flash memory cannot be read from the CPU, the rewrite control program must be transferred to internal RAM area before it can be executed.

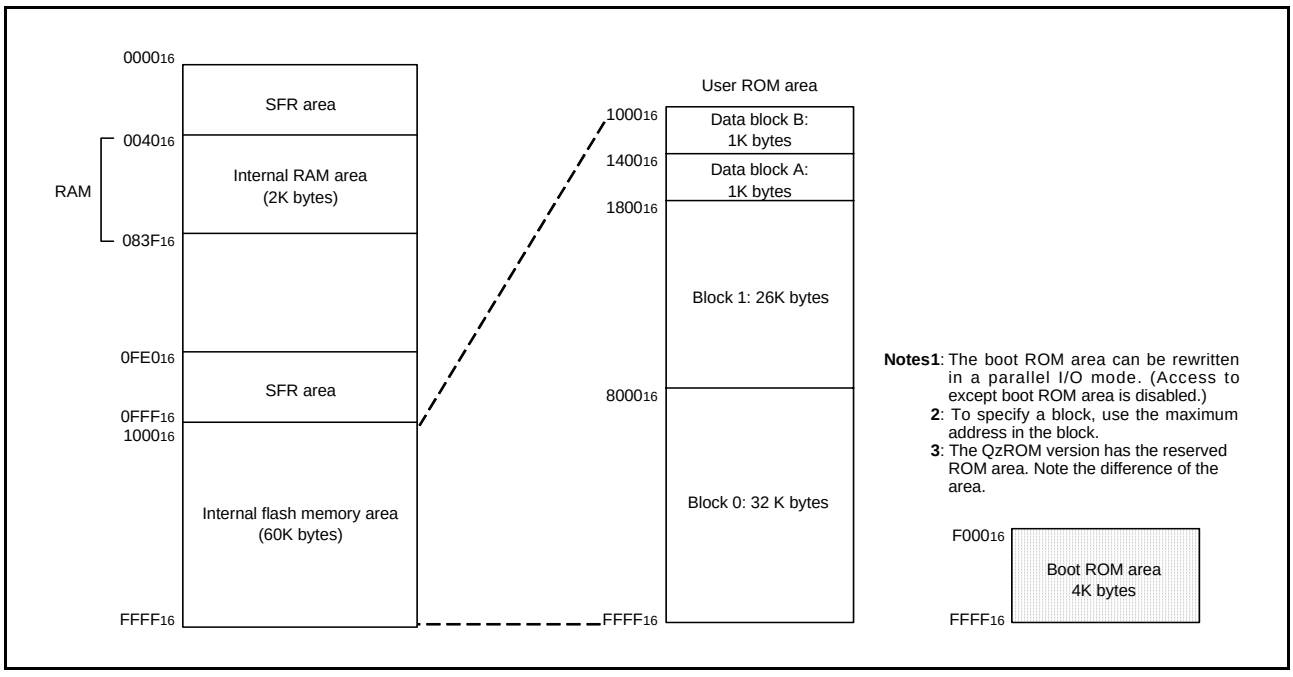


Fig 70. Block diagram of built-in flash memory

Outline Performance

CPU rewrite mode is usable in the single-chip or Boot mode. The only User ROM area can be rewritten.

In CPU rewrite mode, the CPU erases, programs and reads the internal flash memory as instructed by software commands. This rewrite control program must be transferred to internal RAM area before it can be executed.

The MCU enters CPU rewrite mode by setting “1” to the CPU rewrite mode select bit (bit 1 of address 0FE0$_{16}$). Then, software commands can be accepted.

Use software commands to control program and erase operations. Whether a program or erase operation has terminated normally or in error can be verified by reading the status register.

Figure 71 shows the flash memory control register 0.

Bit 0 of the flash memory control register 0 is the RY/$\overline{\text{BY}}$ status flag used exclusively to read the operating status of the flash memory. During programming and erase operations, it is “0” (busy). Otherwise, it is “1” (ready).

Bit 1 of the flash memory control register 0 is the CPU rewrite mode select bit. When this bit is set to “1”, the MCU enters CPU rewrite mode. And then, software commands can be accepted. In CPU rewrite mode, the CPU becomes unable to access the internal flash memory directly. Therefore, use the control program in the internal RAM for write to bit 1. To set this bit 1 to “1”, it is necessary to write “0” and then write “1” in succession to bit 1. The bit can be set to “0” by only writing “0”.

Bit 2 of the flash memory control register 0 is the user block 1 E/W enable bit. By setting combination of bit 4 (user block 0 E/W enable bit) of the flash memory control register 2 (address 0FE2$_{16}$) and this bit as shown in Table 17, E/W is disabled to user block in the CPU rewriting mode.

Bit 3 of the flash memory control register 0 is the flash memory reset bit used to reset the control circuit of internal flash memory. This bit is used when flash memory access has failed. When the CPU rewrite mode select bit is “1”, setting “1” for this bit resets the control circuit. To release the reset, it is necessary to set this bit to “0”.

Bit 5 of the flash memory control register 0 is the User ROM area select bit and is valid only in the boot mode. Setting this bit to “1” in the boot mode switches an accessible area from the boot ROM area to the user ROM area. To use the CPU rewrite mode in the boot mode, set this bit to “1”. To rewrite bit 5, execute the user original reprogramming control software transferred to the internal RAM in advance.

Bit 6 of the flash memory control register 0 is the program status flag. This bit is set to “1” when writing to flash memory is failed. When program error occurs, the block cannot be used.

Bit 7 of the flash memory control register 0 is the erase status flag.

This bit is set to “1” when erasing flash memory is failed. When erase error occurs, the block cannot be used.

Figure 72 shows the flash memory control register 1.

Bit 0 of the flash memory control register 1 is the Erase suspend enable bit. By setting this bit to “1”, the erase suspend mode to suspend erase processing temporary when block erase command is executed can be used. In order to set this bit 0 to “1”, writing “0” and “1” in succession to bit 0. In order to set this bit to “0”, write “0” only to bit 0.

Bit 1 of the flash memory control register 1 is the erase suspend request bit. By setting this bit to “1” when erase suspend enable bit is “1”, the erase processing is suspended.

Bit 6 of the flash memory control register 1 is the erase suspend flag. This bit is cleared to “0” at the flash erasing.

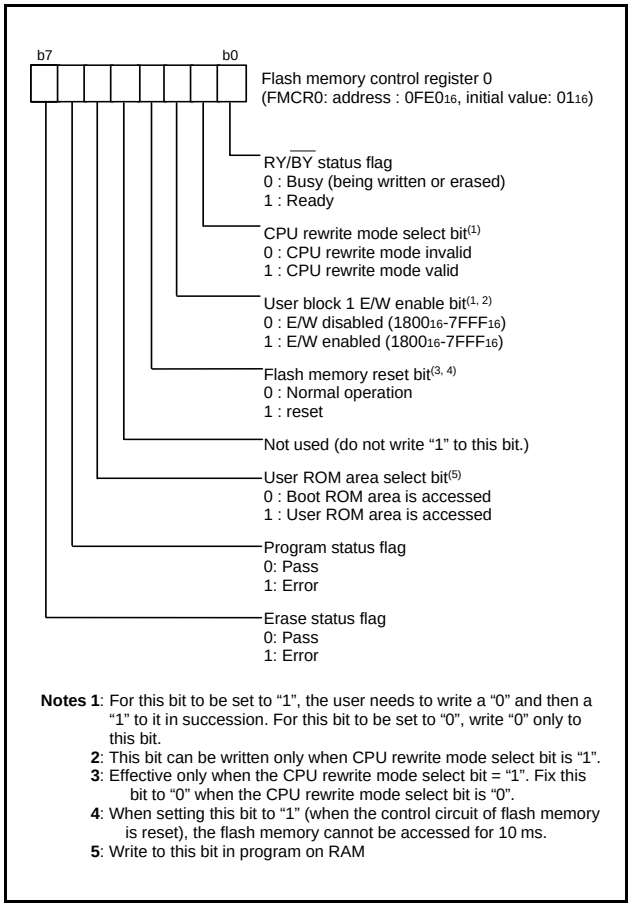


Fig 71. Structure of flash memory control register 0

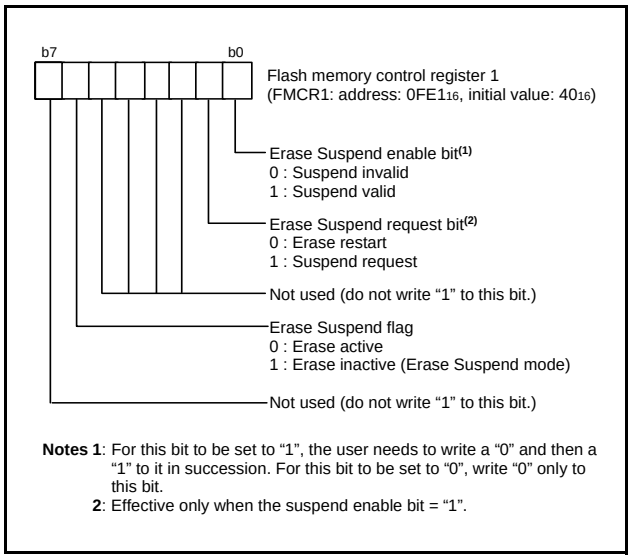
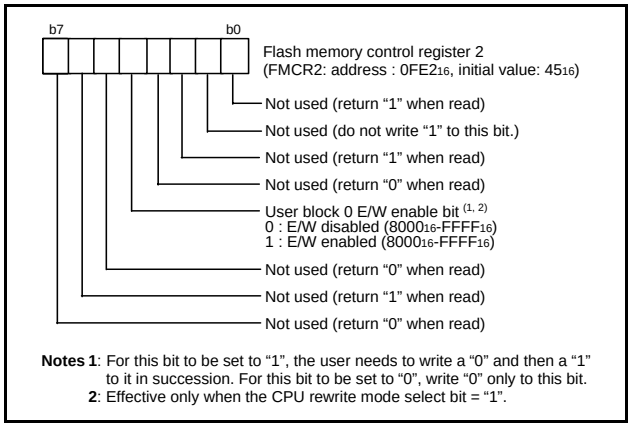


Fig 72. Structure of flash memory control register 1



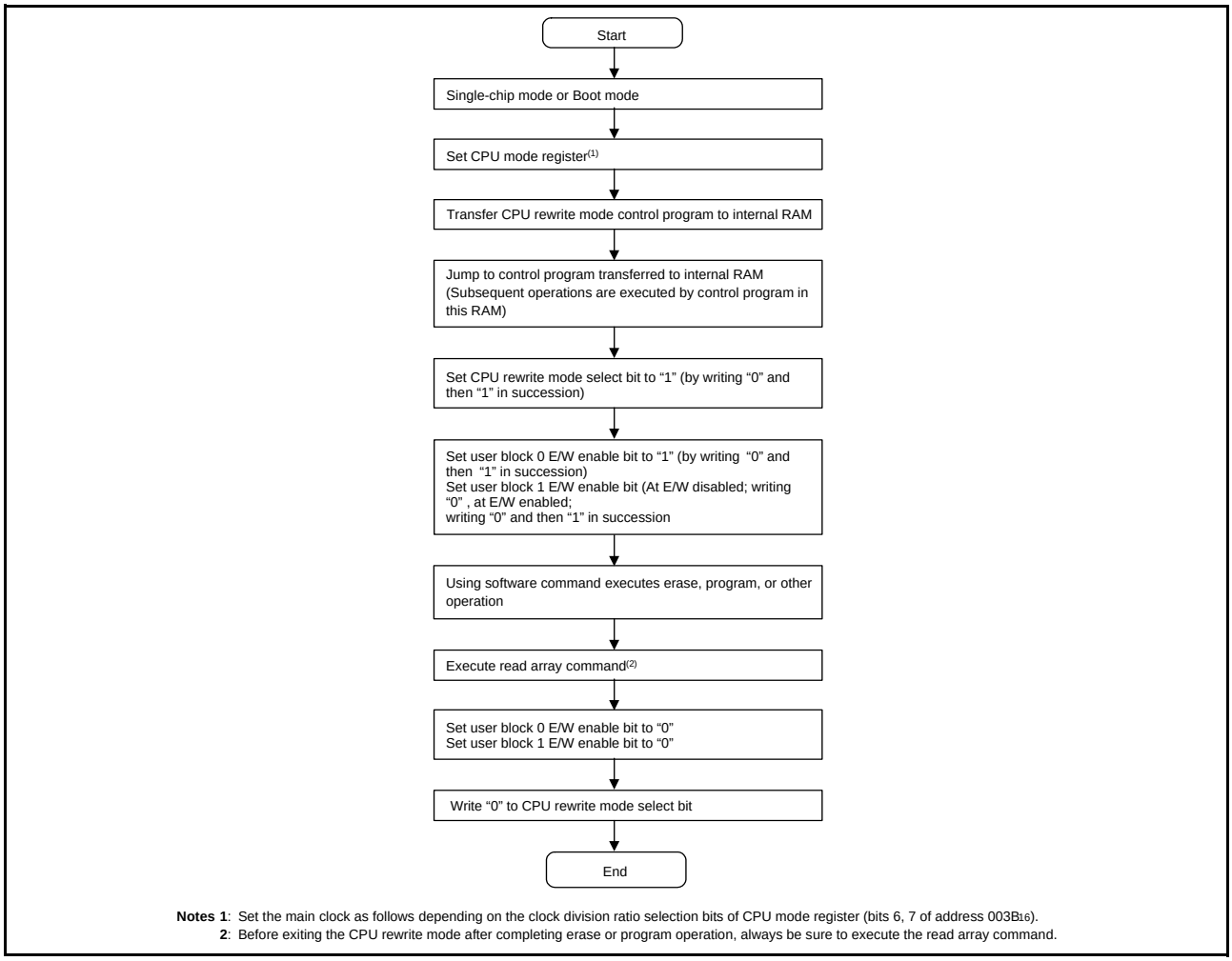
Notes 1: For this bit to be set to "1", the user needs to write a "0" and then a "1" to it in succession. For this bit to be set to "0", write "0" only to this bit.
2: Effective only when the CPU rewrite mode select bit = "1".

Fig 73. Structure of flash memory control register 2

Table 17 State of E/W inhibition function

User block 0 E/W enable bit	User block 1 E/W enable bit	User block 0 Addresses 8000₁₆ to FFFF₁₆	User block 1 Addresses 1800₁₆ to 7FFF₁₆	Data block Addresses 1000₁₆ to 17FF₁₆
0	0	E/W disabled	E/W disabled	E/W enabled
0	1	E/W disabled	E/W enabled	E/W enabled
1	0	E/W enabled	E/W disabled	E/W enabled
1	1	E/W enabled	E/W enabled	E/W enabled

Figure 74 shows a flowchart for setting/releasing CPU rewrite mode.



Notes 1: Set the main clock as follows depending on the clock division ratio selection bits of CPU mode register (bits 6, 7 of address 003B₁₆).
2: Before exiting the CPU rewrite mode after completing erase or program operation, always be sure to execute the read array command.

Fig 74. CPU rewrite mode set/release flowchart be sure to execute

<Notes on CPU Rewrite Mode>

Take the notes described below when rewriting the flash memory in CPU rewrite mode.

(1) Operation speed

During CPU rewrite mode, set the system clock ϕ to 4.0 MHz or less using the main clock division ratio selection bits (bits 6 and 7 of address $003B_{16}$).

(2) Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during CPU rewrite mode.

(3) Interrupts

The interrupts cannot be used during CPU rewrite mode because they refer to the internal data of the flash memory.

(4) Watchdog timer

If the watchdog timer has been already activated, internal reset due to an underflow will not occur because the watchdog timer is surely cleared during program or erase.

(5) Reset

Reset is always valid. The MCU is activated using the boot mode at release of reset in the condition of CNV_{SS} = "H", so that the program will begin at the address which is stored in addresses $FFFC_{16}$ and $FFFD_{16}$ of the boot ROM area.

Software Commands

Table 18 lists the software commands.
After setting the CPU rewrite mode select bit to "1", execute a software command to specify an erase or program operation.
Each software command is explained below.

• Read Array Command (FF_{16})
The read array mode is entered by writing the command code "FF_{16}" in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the contents of the specified address are read out at the data bus (D_0 to D_7).
The read array mode is retained until another command is written.

• Read Status Register Command (70_{16})
When the command code "70_{16}" is written in the first bus cycle, the contents of the status register are read out at the data bus (D_0 to D_7) by a read in the second bus cycle.
The status register is explained in the next section.

• Clear Status Register Command (50_{16})
This command is used to clear the bits SR4 and SR5 of the status register after they have been set. These bits indicate that operation has ended in an error. To use this command, write the command code "50_{16}" in the first bus cycle.

• Program Command (40_{16})
Program operation starts when the command code "40_{16}" is written in the first bus cycle. Then, if the address and data to program are written in the 2nd bus cycle, program operation (data programming and verification) will start.
Whether the write operation is completed can be confirmed by read status register or the RY/$\overline{BY}$ status flag. To read the status register, write the read status register command "70_{16}". The status register bit 7 (SR7) is set to "0" at the same time the program starts and returned to "1" upon completion of the program. The read status mode remains active until the read array command ("FF_{16}") is written.

The RY/$\overline{BY}$ status flag is set to "0" during program operation and "1" when the program operation is completed as is the status register bit 7 (SR7).
At program end, program results can be checked by reading the status register.

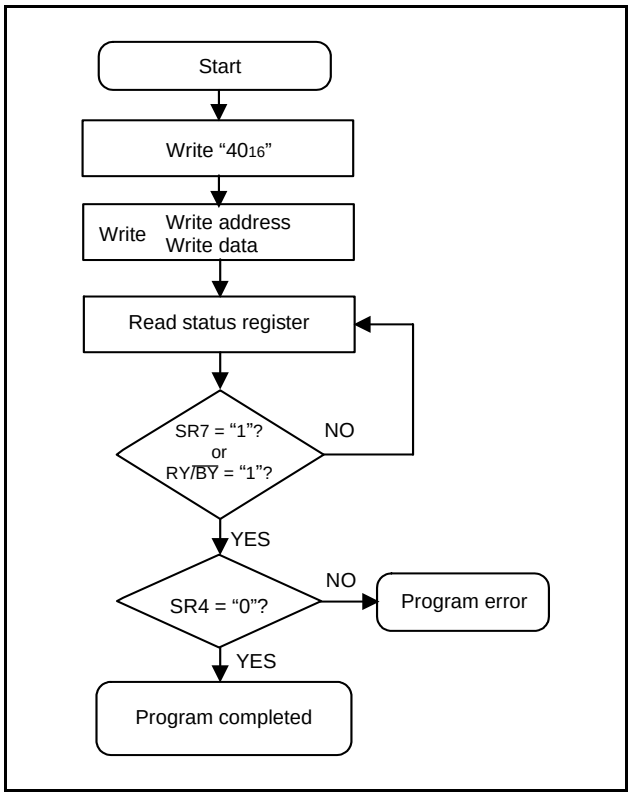


Fig 75. Program flowchart

Table 18 List of software commands (CPU rewrite mode)

Command	cycle number	First bus cycle			Second bus cycle		
		Mode	Address	Data (D_0 to D_7)	Mode	Address	Data (D_0 to D_7)
Read array	1	Write	X(4)	FF_{16}			
Read status register	2	Write	X	70_{16}	Read	X	SRD(1)
Clear status register	1	Write	X	50_{16}			
Program	2	Write	X	40_{16}	Write	WA(2)	WD(2)
Block erase	2	Write	X	20_{16}	Write	BA(3)	$D0_{16}$

NOTES:
1. SRD = Status Register Data
2. WA = Write Address, WD = Write Data
3. BA = Block Address to be erased (Input the maximum address of each block.)
4. X denotes a given address in the User ROM area.

• Block Erase Command (20_{16}/$D0_{16}$)

By writing the command code "20_{16}" in the first bus cycle and the confirmation command code "$D0_{16}$" and the block address in the second bus cycle that follows, the block erase (erase and erase verify) operation starts for the block address of the flash memory to be specified.

Whether the block erase operation is completed can be confirmed by read status register or the RY/$\overline{BY}$ status flag of flash memory control register. To read the status register, write the status register command "70_{16}". The status register bit 7 (SR7) is set to "0" at the same time the block erase operation starts and returned to "1" upon completion of the block erase operation. The read status mode at this time remains active until the read array command ("FF_{16}") is written.

The RY/$\overline{BY}$ status flag register is set to "0" during block erase operation and "1" when the block erase operation is completed as is the status register bit 7 (SR7).

After the block erase ends, erase results can be checked by reading the status register. For details, refer to the section where the status register is detailed.

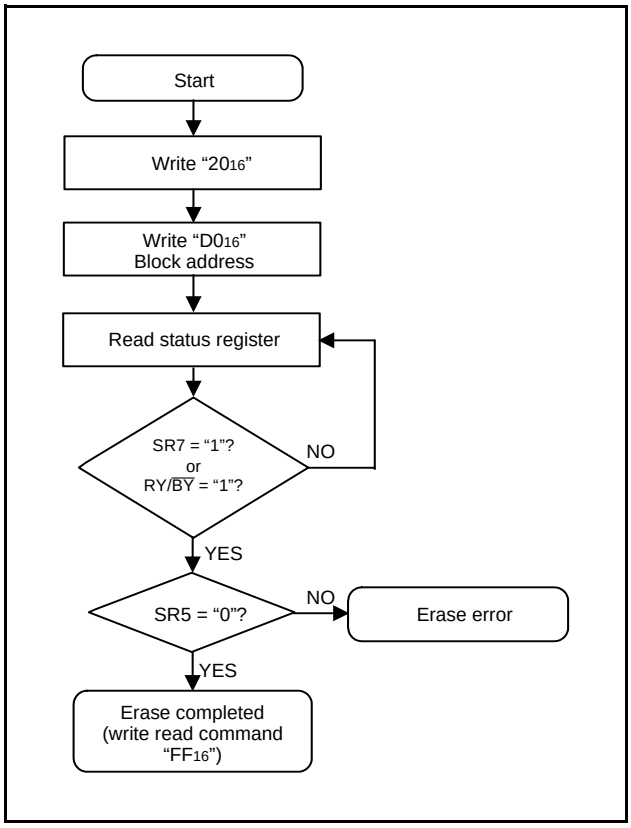


Fig 76. Erase flowchart

• Status Register

The status register shows the operating status of the flash memory and whether erase operations and programs ended successfully or in error. It can be read in the following ways:

(1) By reading an arbitrary address from the User ROM area after writing the read status register command (70_{16})

(2) By reading an arbitrary address from the User ROM area in the period from when the program starts or erase operation starts to when the read array command (FF_{16}) is input.

Also, the status register can be cleared by writing the clear status register command (50_{16}).
After reset, the status register is set to "80_{16}".
Table 19 shows the status register. Each bit in this register is explained below.

• Sequencer status (SR7)

The sequencer status indicates the operating status of the flash memory. This bit is set to "0" (busy) during write or erase operation and is set to "1" when these operations ends.
After power-on, the sequencer status is set to "1" (ready).

• Erase status (SR5)

The erase status indicates the operating status of erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is reset to "0".

• Program status (SR4)

The program status indicates the operating status of write operation.
When a write error occurs, it is set to "1".
The program status is reset to "0" when it is cleared.

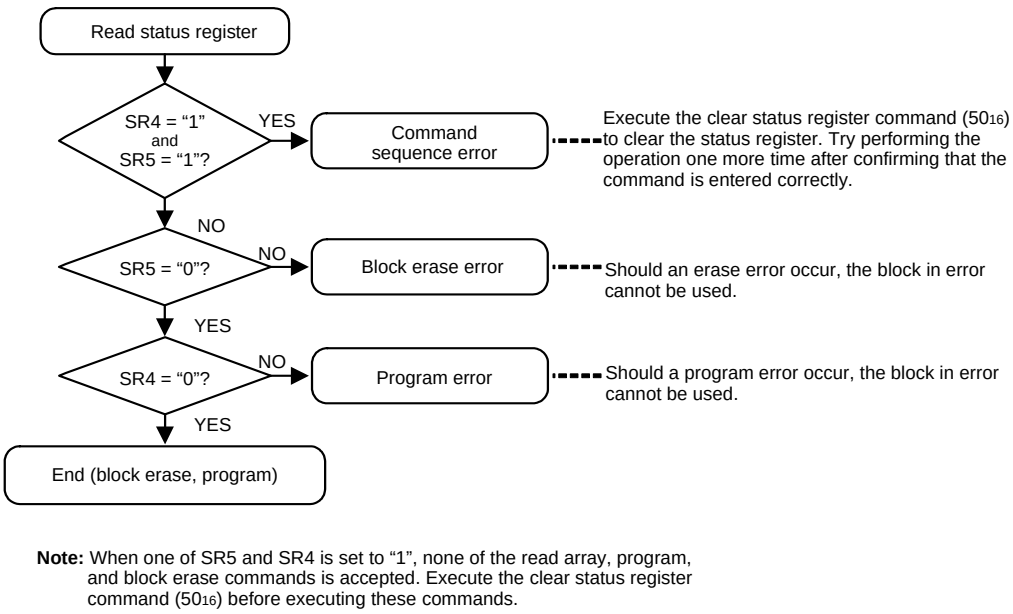
If "1" is written for any of the SR5 and SR4 bits, the read array, program, and block erase commands are not accepted. Before executing these commands, execute the clear status register command (50_{16}) and clear the status register.
Also, if any commands are not correct, both SR5 and SR4 are set to "1".

Table 19 Definition of each bit in status register

Each bit of SRD bits	Status name	Definition	
		"1"	"0"
SR7 (bit7)	Sequencer status	Ready	Busy
SR6 (bit6)	Reserved	–	–
SR5 (bit5)	Erase status	Terminated in error	Terminated normally
SR4 (bit4)	Program status	Terminated in error	Terminated normally
SR3 (bit3)	Reserved	–	–
SR2 (bit2)	Reserved	–	–
SR1 (bit1)	Reserved	–	–
SR0 (bit0)	Reserved	–	–

Full Status Check

By performing full status check, it is possible to know the execution results of erase and program operations. Figure 77 shows a full status check flowchart and the action to be taken when each error occurs.



Note: When one of SR5 and SR4 is set to "1", none of the read array, program, and block erase commands is accepted. Execute the clear status register command (50_{16}) before executing these commands.

Fig 77. Full status check flowchart and remedial procedure for errors

Functions To Inhibit Rewriting Flash Memory Version

To prevent the contents of internal flash memory from being read out or rewritten easily, this MCU incorporates a ROM code protect function for use in parallel I/O mode and an ID code check function for use in standard serial I/O mode.

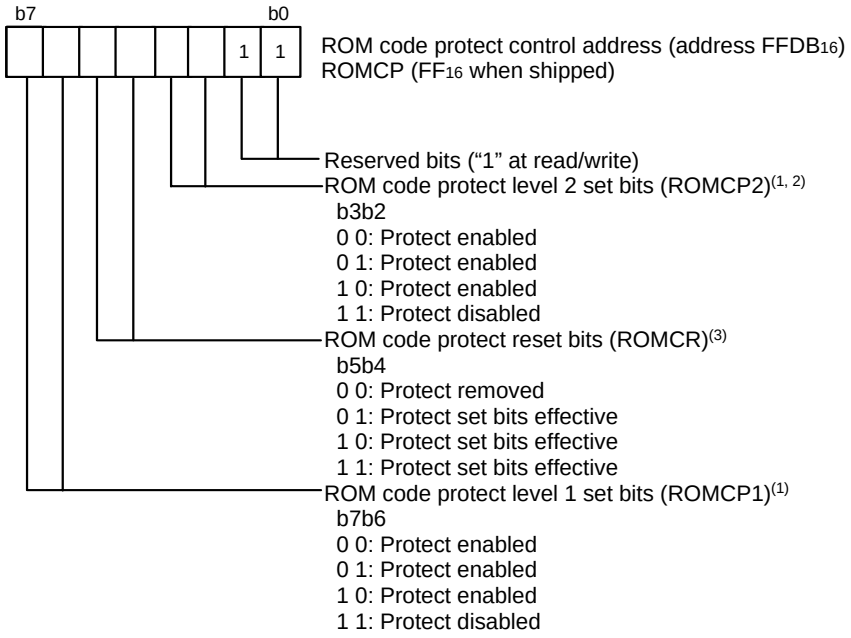
• ROM Code Protect Function

The ROM code protect function is the function to inhibit reading out or modifying the contents of internal flash memory by using the ROM code protect control address (address FFDB16) in parallel I/O mode. Figure 78 shows the ROM code protect control address (address FFDB16). (This address exists in the User ROM area.)

If one or both of the pair of ROM code protect bits is set to "0", the ROM code protect is turned on, so that the contents of internal flash memory are protected against readout and modification. The ROM code protect is implemented in two levels. If level 2 is selected, the flash memory is protected even against readout by a shipment inspection LSI tester, etc. When an attempt is made to select both level 1 and level 2, level 2 is selected by default.

If both of the two ROM code protect reset bits are set to "00", the ROM code protect is turned off, so that the contents of internal flash memory can be readout or modified. Once the ROM code protect is turned on, the contents of the ROM code protect reset bits cannot be modified in parallel I/O mode. Use standard serial I/O mode or other modes to rewrite the contents of the ROM code protect disable bits.

Rewriting of only the ROM code protect control address (address FFDB16) cannot be performed. When rewriting the ROM code protect reset bit, rewrite the whole user ROM area (block 0) containing the ROM code protect control address.



Notes 1: When ROM code protect is turned on, the internal flash memory is protected against readout or modification in parallel I/O mode.
2: When ROM code protect level 2 is turned on, ROM code readout by a shipment inspection LSI tester, etc. also is inhibited.
3: The ROM code protect reset bits can be used to turn off ROM code protect level 1 and ROM code protect level 2.
However, no change can be made in parallel I/O mode. Use serial I/O mode or other modes to change settings.

Fig 78. Structure of ROM code protect control address

• ID Code Check Function

Use this function in standard serial I/O mode. When the contents of the flash memory are not blank, the ID code sent from the programmer is compared with the ID code written in the flash memory to see if they match. If the ID codes do not match, the commands sent from the programmer are not accepted. The ID code consists of 8-bit data, and its areas are FFD4$_{16}$ to FFDA$_{16}$. Write a program which has had the ID code preset at these addresses to the flash memory.

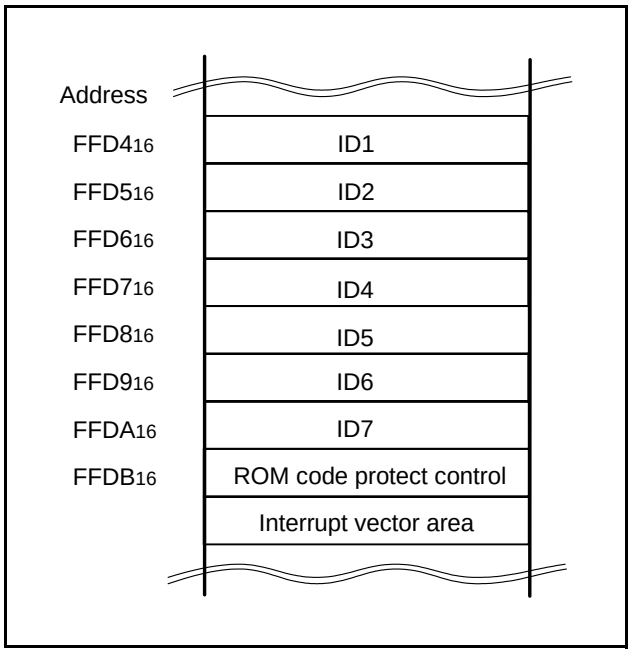


Fig 79. ID code store addresses

Parallel I/O Mode

The parallel I/O mode is used to input/output software commands, address and data in parallel for operation (read, program and erase) to internal flash memory.

• User ROM and Boot ROM Areas

In parallel I/O mode, the User ROM and Boot ROM areas shown in Figure 70 can be rewritten. Both areas of flash memory can be operated on in the same way.
The Boot ROM area is 4 Kbytes in size and located at addresses $F000_{16}$ through $FFFF_{16}$. Make sure program and block erase operations are always performed within this address range. (Access to any location outside this address range is prohibited.)
In the Boot ROM area, an erase block operation is applied to only one 4 K byte block. The boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. Therefore, using the MCU in standard serial I/O mode, do not rewrite to the Boot ROM area.

Standard serial I/O Mode

The standard serial I/O mode inputs and outputs the software commands, addresses and data needed to operate (read, program, erase, etc.) the internal flash memory. This I/O is clock synchronized serial. This mode requires a purpose-specific peripheral unit.

The standard serial I/O mode is different from the parallel I/O mode in that the CPU controls flash memory rewrite (uses the CPU rewrite mode), rewrite data input and so forth. The standard serial I/O mode is started by connecting "H" to the CNVSS pin and "H" to the P41 (BOOTENT) pin, and releasing the reset operation. (In the ordinary microcomputer mode, set CNVSS pin to "L" level.) This control program is written in the Boot ROM area when the product is shipped from Renesas. Accordingly, make note of the fact that the standard serial I/O mode cannot be used if the Boot ROM area is rewritten in parallel I/O mode. The standard serial I/ O mode has standard serial I/O mode 1 of the clock synchronous serial and standard serial I/O mode 2 of the clock asynchronous serial. Tables 20 and 21 show description of pin function (standard serial I/O mode). Figure 80 to 83 show the pin connections for the standard serial I/O mode.

In standard serial I/O mode, only the User ROM area shown in Figure 70 can be rewritten. The Boot ROM area cannot be written.

In standard serial I/O mode, a 7-byte ID code is used. When there is data in the flash memory, this function determines whether the ID code sent from the peripheral unit (programmer) and those written in the flash memory match. The commands sent from the peripheral unit (programmer) are not accepted unless the ID code matches.

Table 20 Description of pin function (Flash Memory Standard Serial I/O Mode 1)

Pin name	Signal name	I/O	Function
V_{CC},V_{SS}	Power supply	I	Apply 2.7 to 5.5 V to the V_{CC} pin and 0 V to the Vss pin.
CNV$_{SS}$	CNV$_{SS}$	I	After input of port is set, input “H” level.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin. To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 16 cycles or more of X_{IN}.
X_{IN}	Clock input	I	Connect an oscillation circuit between the X_{IN} and X_{OUT} pins. As for the connection method, refer to the “clock generating circuit”.
X_{OUT}	Clock output	O	
AV$_{SS}$	Analog power supply input		Connect AVss to V_{SS}.
V_{REF}	Reference voltage input	I	Apply reference voltage of A/D convertor to this pin.
$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$	I/O port	I/O	Input “L” or “H” level, or keep open.
$P4_0$	RxD input	I	Serial data input pin.
$P4_1$	TxD output	O	Serial data output pin.
$P4_2$	S_{CLK} input	I	Serial clock input pin.
$P4_3$	BUSY output	O	BUSY signal output pin.

Table 21 Description of pin function (Flash Memory Standard Serial I/O Mode 2)

Pin name	Signal name	I/O	Function
V_{CC},V_{SS}	Power supply	I	Apply 2.7 to 5.5 V to the Vcc pin and 0 V to the V_{SS} pin.
CNV$_{SS}$	CNV$_{SS}$	I	After input of port is set, input “H” level.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin. To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 16 cycles or more of X_{IN}.
X_{IN}	Clock input	I	Connect an oscillation circuit between the X_{IN} and X_{OUT} pins. As for the connection method, refer to the “clock generating circuit”.
X_{OUT}	Clock output	O	
AV$_{SS}$	Analog power supply input		Connect AVss to V_{SS}.
V_{REF}	Reference voltage input	I	Apply reference voltage of A/D convertor to this pin.
$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$	I/O port	I/O	Input “L” or “H” level, or keep open.
$P4_0$	RxD input	I	Serial data input pin.
$P4_1$	TxD output	O	Serial data output pin.
$P4_2$	S_{CLK} input	I	Input “L” level.
$P4_3$	BUSY output	O	BUSY signal output pin.

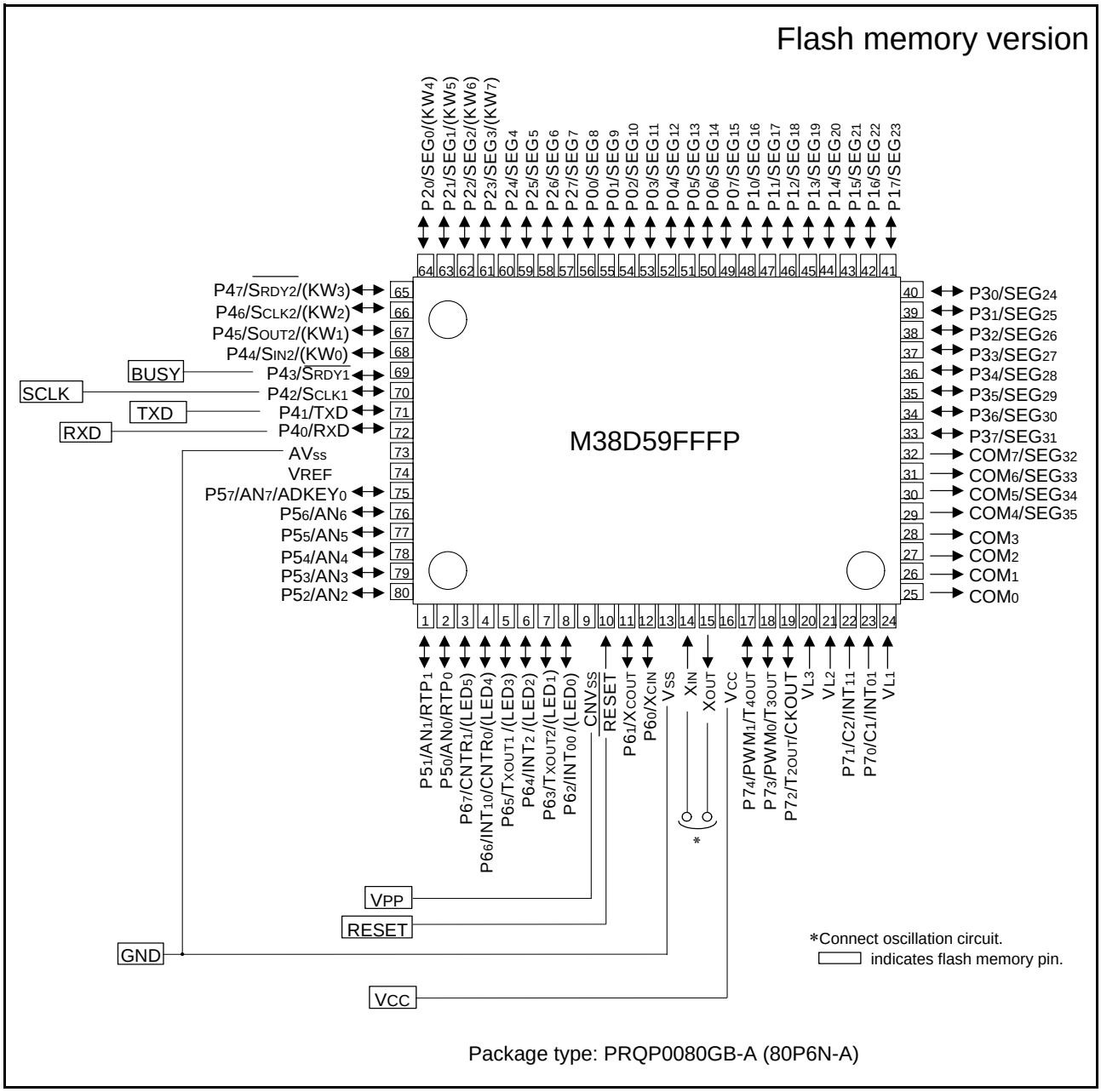
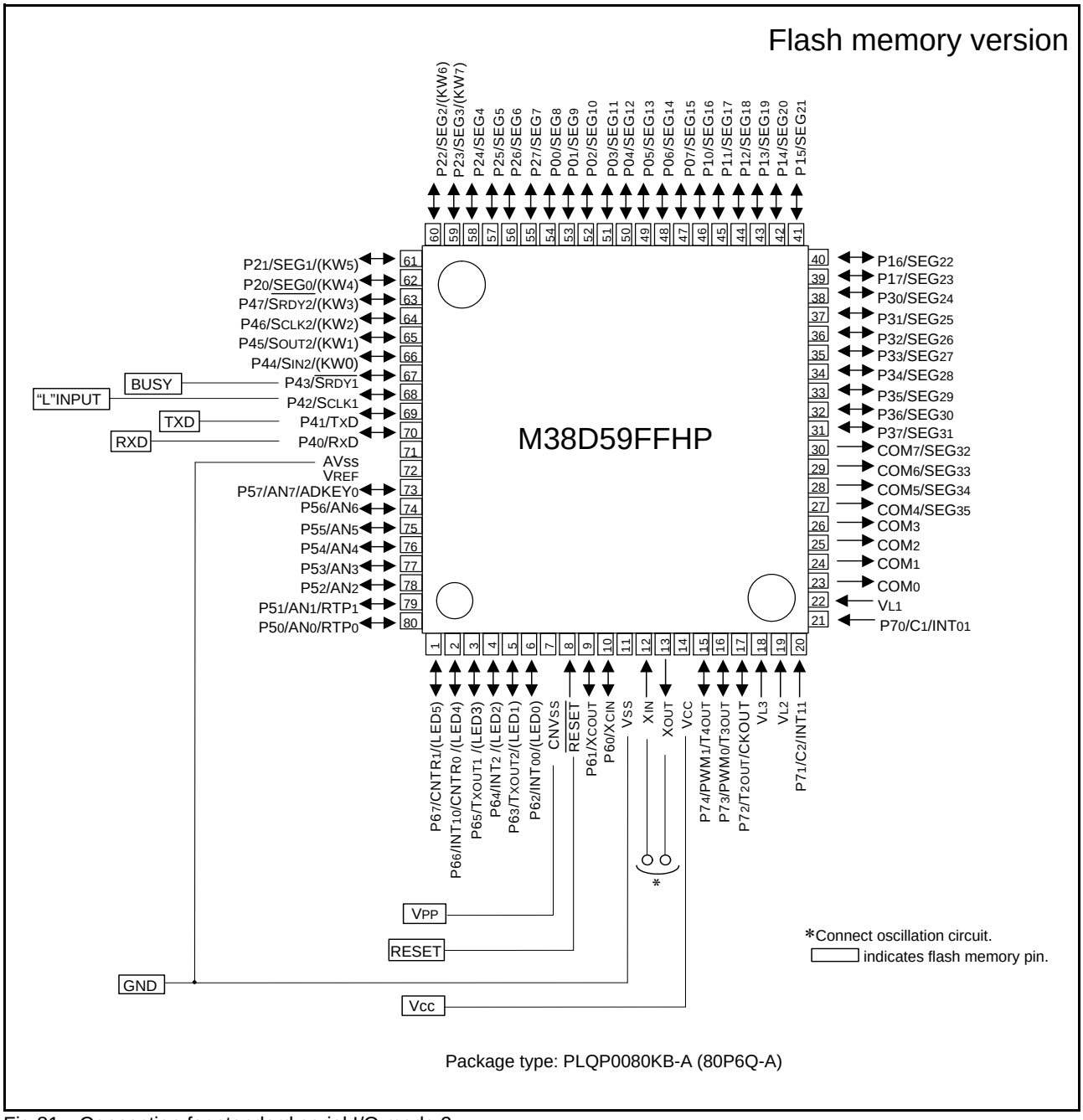
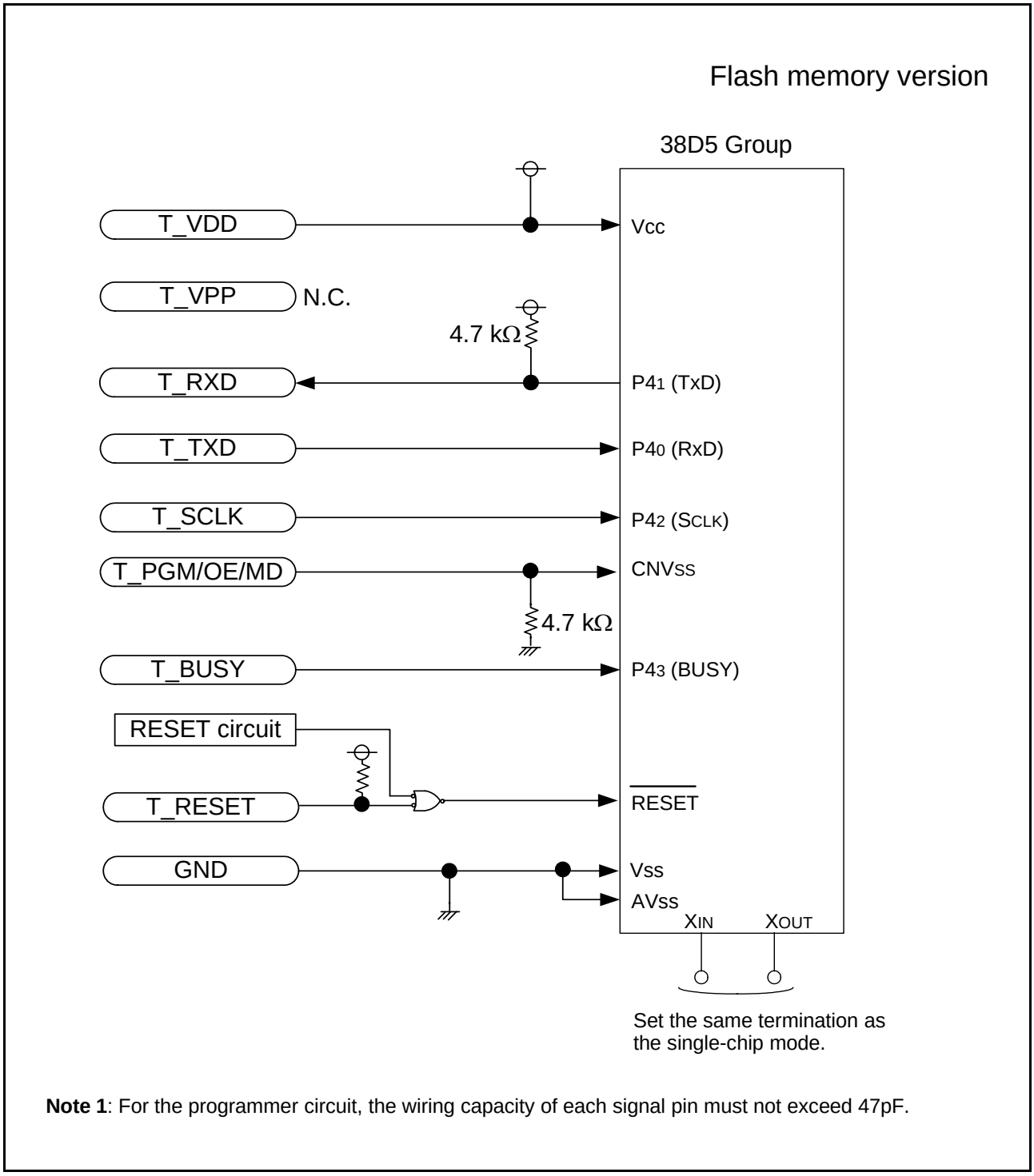


Fig 80. Connection for standard serial I/O mode 1



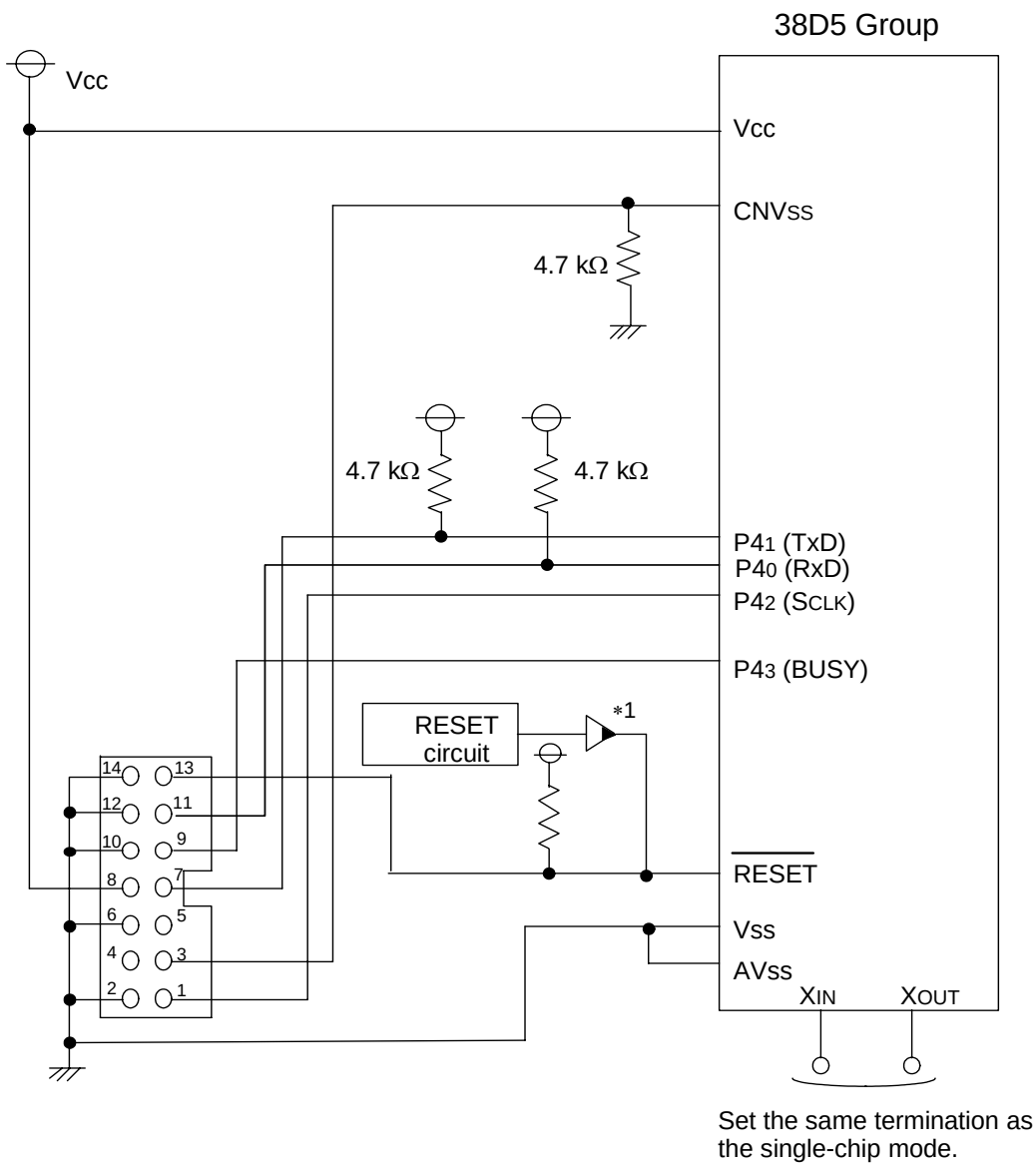
Package type: PLQP0080KB-A (80P6Q-A)

Fig 81. Connection for standard serial I/O mode 2



Note 1: For the programmer circuit, the wiring capacity of each signal pin must not exceed 47pF.

Fig 82. When using programmer (in standard serial I/O mode 1) of Suisei Electronics System Co., LTD, connection example

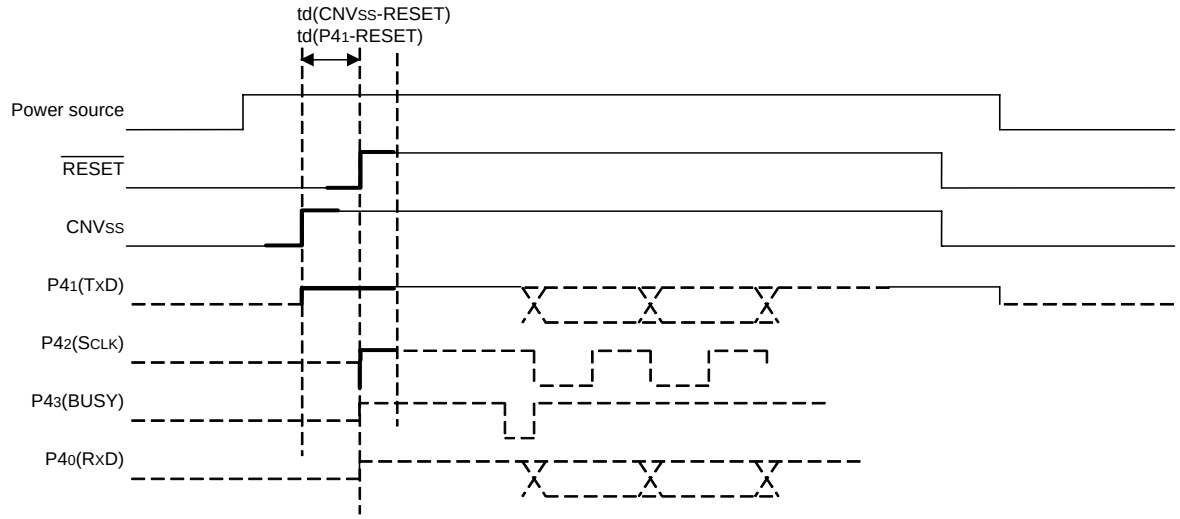


∗ 1: Open-collector buffer

Note 1: For the programmer circuit, the wiring capacity of each signal pin must not exceed 47pF.

Fig 83. When using E8 programmer (in standard serial I/O mode 1) connection example

Flash memory version

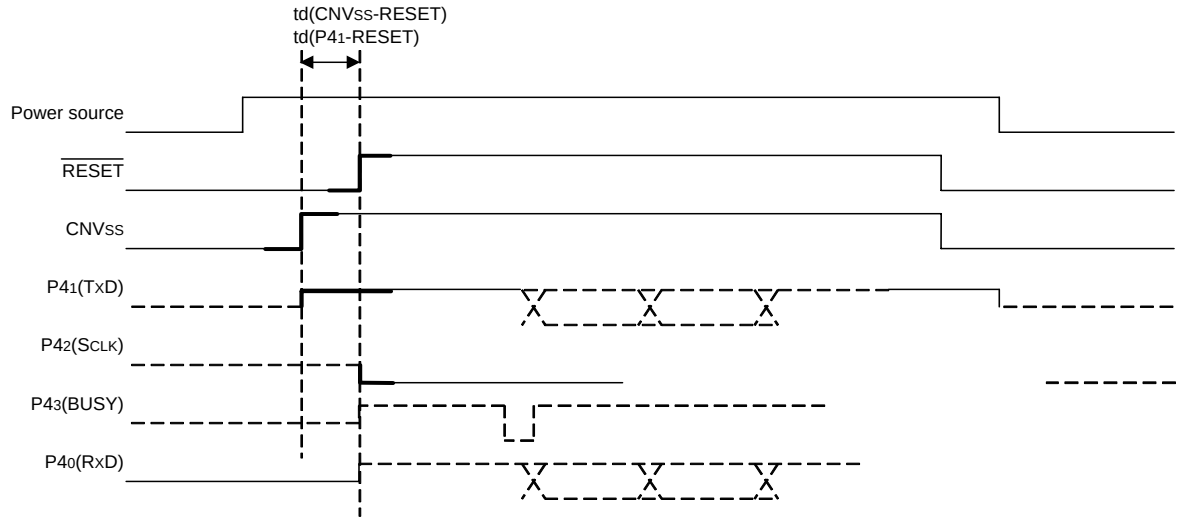


Symbol	Limits			Unit
	Min.	Typ.	Max.	
td(CNVSS-RESET)	0	-	-	ms
td(P41-RESET)	0			ms

Note: In the standard serial I/O mode 1, input "H" to the P42 pin.
Be sure to set the CNVss pin to "H" before rising RESET.
Be sure to set the P41 pin to "H" before rising RESET.

Fig 84. Operating waveform for standard serial I/O mode 1

Flash memory version



Symbol	Limits			Unit
	Min.	Typ.	Max.	
td(CNVSS-RESET)	0	-	-	ms
td(P41-RESET)	0			ms

Note: In the standard serial I/O mode 2, input "H" to the P42 pin.
Be sure to set the CNVss pin to "H" before rising RESET.
Be sure to set the P41 pin to "H" before rising RESET.

Fig 85. Operating waveform for standard serial I/O mode 2

NOTES ON USE

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution.
In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations. Initialize these flags at beginning of the program.

Interrupt

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

The division ratio is 1/(n+1) when the value n (0 to 255) is written to the timer latch.

Multiplication and Division Instructions

The index mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
The execution of these instructions does not change the contents of the processor status register.

Direction Registers

The values of the port direction registers cannot be read. This means, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS. It is also impossible to use bit operation instructions such as CLB and SEB, and read-modify-write instructions to direction registers, including calculations such as ROR. To set the direction registers, use instructions such as LDM or STA.

Serial Interface

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1".
Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

A/D Converter

The comparator is constructed linked to a capacitor. The conversion accuracy may be low because the charge is lost if the conversion speed is not enough. Accordingly, set f(XIN) to at least 500kHz during A/D conversion in the XIN mode.
Also, do not execute the STP or WIT instruction during an A/D conversion.
In the low-speed mode, since the A/D conversion is executed by the on-chip oscillator, the minimum value of f(XIN) frequency is not limited.

LCD Drive Control Circuit

Execution of the STP instruction sets the LCD enable bit (bit 4 of the LCD mode register) to "0" and the LCD panel turns off. To make the LCD panel turn on after returning from the stop mode, set the LCD enable bit to "1".

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.

Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.
In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the power source voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (VCC pin) and GND pin (Vss pin), and between power source pin (VCC pin) and analog power source pin (AVCC). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.1 μF is recommended.

LCD drive power supply

Power supply capacitor may be insufficient with the division resistance for LCD power supply, and the characteristic of the LCD panel. In this case, there is the method of connecting the bypass capacitor about 0.1 –0.33μF to VL1 –VL3 pins. The example of a strengthening measure of the LCD drive power supply is shown below.

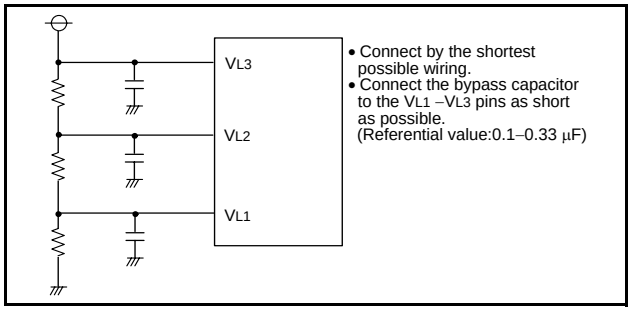


Fig. 86 Strengthening measure example of LCD drive power supply

NOTES ON QzROM VERSION

Wiring to OSCSEL pin

1. OSCSEL = L
   Connect the OSCSEL pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer. In addition connecting an approximately 5 kΩ resistor in series to the GND could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer.

2. OSCSEL = H
   Connect the OSCSEL pin the shortest possible to the VCC pattern which is supplied to the VCC pin of the microcomputer. In addition connecting an approximately 5 kΩ resistor in series to the VCC could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the VCC pattern which is supplied to the VCC pin of the microcomputer.

• Reason

The OSCSEL pin is the power source input pin for the built-in QzROM.
When programming in the QzROM, the impedance of the OSCSEL pin is low to allow the electric current for writing to flow into the built-in QzROM. Because of this, noise can enter easily. If noise enters the OSCSEL pin, abnormal instruction codes or data are read from the QzROM, which may cause a program runaway.

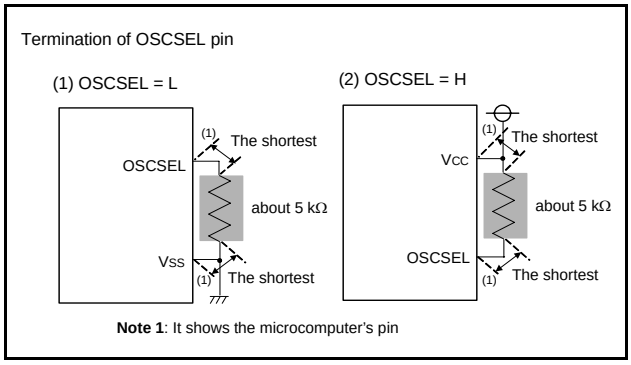


Fig. 87 Wiring for the OSCSEL pin

Precautions Regarding Overvoltage in QzROM Version

Make sure that voltage exceeding the VCC pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in figure below does not occur for OSCSEL pin (VPP power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.

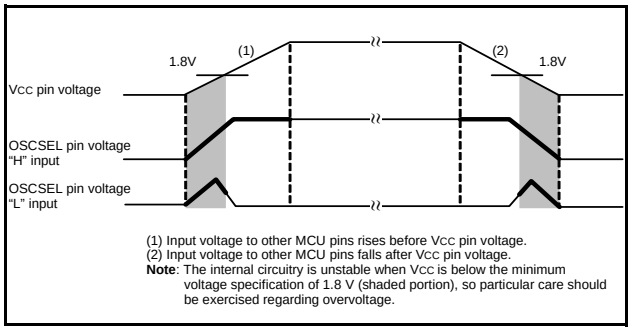


Fig. 88 Example of Overvoltage

Product shipped in blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approximate 0.1% may occur.
Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

Notes On QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .msk) which is made by the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "00$_{16}$", "FE$_{16}$" and "FF$_{16}$" can not be accepted.
- Set "FF$_{16}$" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF$_{16}$" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

Data Required For QzROM Writing Orders

The following are necessary when ordering a QzROM product shipped after writing:
1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).
Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

QzROM Receive Flow

When writing to QzROM is performed by user side, the receiving inspection by the following flow is necessary.

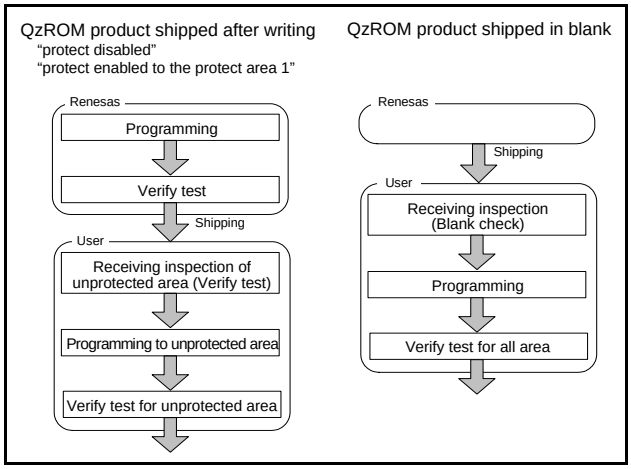


Fig. 89 QzROM receive flow

NOTES ON FLASH MEMORY VERSION

CPU Rewrite Mode

(1) Operation speed

During CPU rewrite mode, set the system clock ϕ 4.0 MHz or less using the main clock division ratio selection bits (bits 6 and 7 of address 003B16).

(2) Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during the CPU rewrite mode.

(3) Interrupts inhibited against use

The interrupts cannot be used during the CPU rewrite mode because they refer to the internal data of the flash memory.

(4) Watchdog timer

In case of the watchdog timer has been running already, the internal reset generated by watchdog timer underflow does not happen, because of watchdog timer is always clearing during program or erase operation.

(5) Reset

Reset is always valid. In case of CNVSS = "H" when reset is released, boot mode is active. So the program starts from the address contained in address FFFC16 and FFFD16 in boot ROM area.

CNVss Pin

The CNVSS pin determines the flash memory mode.
Connect the CNVSS/VPP pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer.
In addition connecting an approximately 5 kΩ resistor in series to the GND could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the GND pattern which is supplied to the Vss pin of the microcomputer.

Note. When the boot mode or the standard serial I/O mode is used, a switch of the input level to the CNVSS pin is required.

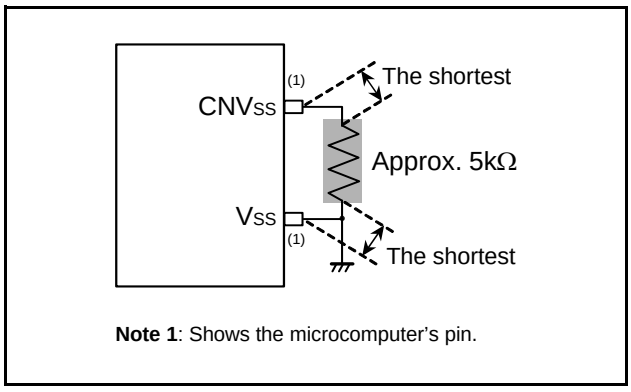


Fig 90. Wiring for the CNVss

NOTES ON DIFFERENCES BETWEEN QzROM VERSION AND FLASH MEMORY VERSION

The QzROM and flash memory versions differ in their manufacturing processes, built-in ROM, and layout patterns. Because of these differences, characteristic values, operation margins, noise immunity, and noise radiation and oscillation circuit constants may vary within the specified range of electrical characteristics.
When switching to the QzROM version, implement system evaluations equivalent to those performed in the flash memory version.
Confirm page 11 about the differences of functions.

Countermeasures against noise

(1) Shortest wiring length

1. Wiring for $\overline{\text{RESET}}$ pin
Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the Vss pin with the shortest possible wiring (within 20 mm).

• Reason
The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

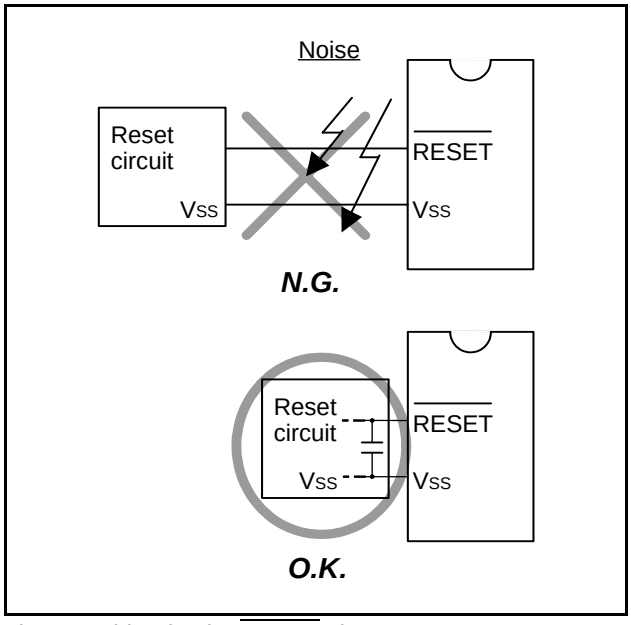


Fig. 91 Wiring for the $\overline{\text{RESET}}$ pin

2. Wiring for clock input/output pins
- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

• Reason
If noise enters clock I/O pins, clock waveforms may be deformed.
This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

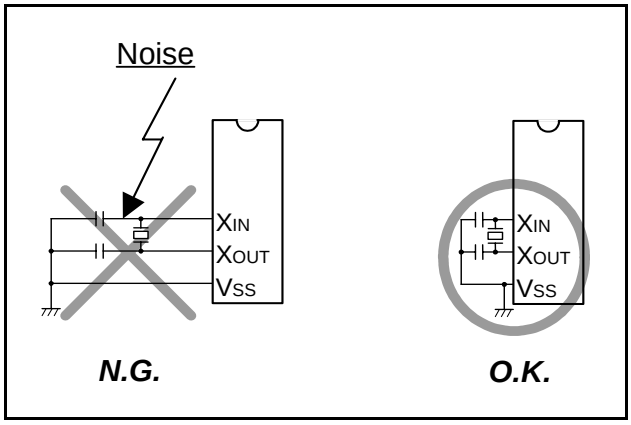


Fig. 92 Wiring for clock I/O pins

(2) Connection of bypass capacitor across Vss line and Vcc line

In order to stabilize the system operation and avoid the latch-up, connect an approximately 0.1 µF bypass capacitor across the Vss line and the Vcc line as follows:
- Connect a bypass capacitor across the Vss pin and the Vcc pin at equal length.
- Connect a bypass capacitor across the Vss pin and the Vcc pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for Vss line and Vcc line.
- Connect the power source wiring via a bypass capacitor to the Vss pin and the Vcc pin.

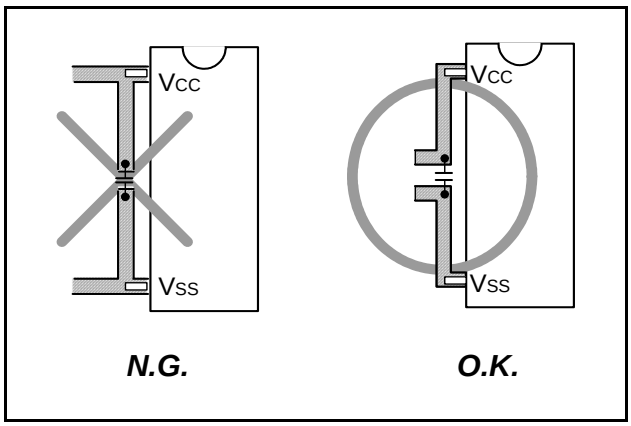


Fig. 93 Bypass capacitor across the Vss line and the Vcc line

(3) Oscillator concerns

In order to obtain the stabilized operation clock on the user system and its condition, contact the oscillator manufacturer and select the oscillator and oscillation circuit constants. Be careful especially when range of voltage and temperature is wide.
Also, take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

1. Keeping oscillator away from large current signal lines
   Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

• Reason

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

2. Installing oscillator away from signal lines where potential levels change frequently
   Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

• Reason

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

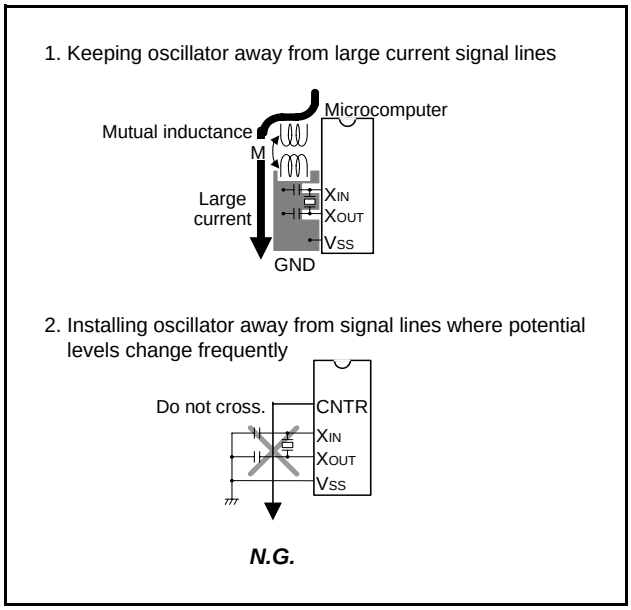


Fig. 94 Wiring for a large current signal line/Wiring of signal lines where potential levels change frequently

(4) Analog input

The analog input pin is connected to the capacitor of a voltage comparator. Accordingly, sufficient accuracy may not be obtained by the charge/discharge current at the time of A/D conversion when the analog signal source of high-impedance is connected to an analog input pin. In order to obtain the A/D conversion result stabilized more, please lower the impedance of an analog signal source, or add the smoothing capacitor to an analog input pin.

(5) Difference of memory size

When memory size differ in one group, actual values such as an electrical characteristics, A/D conversion accuracy, and the amount of proof of noise incorrect operation may differ from the ideal values.
When these products are used switching, perform system evaluation for each product of every after confirming product specification.

QzROM VERSION ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Table 22 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. When an input voltage is measured, output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_4$		–0.3 to V_{CC}+0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to 6.5	V
V_I	Input voltage C_1, C_2		–0.3 to 6.5	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC}+0.3	V
V_I	Input voltage OSCSEL		–0.3 to 8.0	V
V_O	Output voltage C_1, C_2		–0.3 to 6.5	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	At output port	–0.3 to V_{CC}+0.3	V
		At segment output	–0.3 to V_{L3}+0.3	V
V_O	Output voltage $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$	All voltages are based on V_{SS}.	–0.3 to V_{CC}+0.3	V
V_O	Output voltage V_{L3}		–0.3 to 6.5	V
V_O	Output voltage V_{L2}, SEG_{32}–SEG_{35}, COM_0–COM_3		–0.3 to V_{L3}+0.3	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC}+0.3	V
P_d	Power dissipation	Ta = 25°C	300	mW
T_{opr}	Operating temperature	———	–20 to 85	°C
T_{stg}	Storage temperature	———	–40 to 125	°C

Recommended Operating Conditions

Table 23 Recommended operating conditions (1)
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85°C unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Power source voltage (1)	Frequency/2 mode (2)	$f(X_{IN}) \leq 12.5$MHz	4.5		5.5	V
			$f(X_{IN}) \leq 8$MHz	4.0		5.5	V
			$f(X_{IN}) \leq 4$MHz	2.0		5.5	V
			$f(X_{IN}) \leq 2$MHz	1.8		5.5	V
		Frequency/4 mode	$f(X_{IN}) \leq 16$MHz	4.5		5.5	V
			$f(X_{IN}) \leq 8$MHz	2.0		5.5	V
			$f(X_{IN}) \leq 4$MHz	1.8		5.5	V
		Frequency/8 mode	$f(X_{IN}) \leq 16$MHz	4.5		5.5	V
			$f(X_{IN}) \leq 8$MHz	2.0		5.5	V
			$f(X_{IN}) \leq 4$MHz	1.8		5.5	V
		Low-speed mode		1.8		5.5	V
		On-chip oscillator mode		1.8		5.5	V
		When start oscillating (3)		$0.05 \times f + 1.9$			V
V_{SS}	Power source voltage				0		V
V_{LI}	V_{L1} input voltage	Voltage multiplier is used		1.3	1.8	2.1	V
V_{REF}	A/D converter reference voltage			2.0		V_{CC}	V
AV_{SS}	Analog power source voltage				0		V
V_{IA}	Analog input voltage AN_0–AN_7			AV_{SS}		V_{CC}	V
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_4$–$P2_7$, $P3_0$–$P3_7$, $P4_1$, $P4_3$, $P5_0$–$P5_7$, $P6_0$(CM_4=0), $P6_1$, $P6_5$, $P7_2$–$P7_4$		0.7V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$P2_0$–$P2_3$, $P4_0$, $P4_2$, $P4_4$–4_7, $P6_2$–$P6_4$, $P6_6$, $P6_7$, $P7_0$, $P7_1$		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$	$2.2V < V_{CC} \leq 5.5V$	0.8V_{CC}		V_{CC}	V
			$V_{CC} \leq 2.2V$	$V_{CC} - \frac{65 \times V_{CC} - 99}{100}$		V_{CC}	V
V_{IH}	"H" input voltage	X_{IN}		0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_4$–$P2_7$, $P3_0$–$P3_7$, $P4_1$, $P4_3$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P6_5$, $P7_2$–$P7_4$		0		0.3V_{CC}	V
V_{IL}	"L" input voltage	$P2_0$–$P2_3$, $P4_0$, $P4_2$, $P4_4$–$P4_7$, $P6_2$–$P6_4$, $P6_6$, $P6_7$, $P7_0$, $P7_1$, OSCSEL		0		0.2V_{CC}	V
V_{IL}	"L" input voltage	$\overline{RESET}$	$2.2V < V_{CC} \leq 5.5V$	0		0.2V_{CC}	V
			$V_{CC} \leq 2.2V$	0		$\frac{65 \times V_{CC} - 99}{100}$	V
V_{IL}	"L" input voltage	X_{IN}		0		0.2V_{CC}	V

NOTES:
1. When the A/D converter is used, refer to the recommended operating conditions of the A/D converter.
2. 12.5 MHz < $f(X_{IN}) \leq 16$ MHz is not available in the frequency/2 mode.
3. The oscillation start voltage and the oscillation start time differ depending on factors such as the oscillator, circuit constants, and operating temperature range. Note that oscillation start may be particularly difficult at low voltage when using a high-frequency oscillator.
   f: Oscillation frequency (1 MHz ≤ $f(X_{IN}) \leq 8$ MHz) of oscillator. When the 8 MHz oscillation is used, assign "8" to "f".

Table 24 Recommended operating conditions (2)
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = −20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P7_2$–$P7_4$			−40	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current (1) $P4_0$–4_7, $P5_0$–$P5_7$, $P6_0$–$P6_7$			−40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P7_2$–$P7_4$			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (1) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (1) $P6_2$–$P6_7$			110	mA
$\Sigma I_{OH(avg)}$	"H" total average output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P7_2$–$P7_4$			−20	mA
$\Sigma I_{OH(avg)}$	"H" total average output current (1) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$			−20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P7_2$–$P7_4$			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (1) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (1) $P6_2$–$P6_7$			90	mA
$I_{OH(peak)}$	"H" peak output current (2) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			−2	mA
$I_{OH(peak)}$	"H" peak output current (2) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$			−5	mA
$I_{OL(peak)}$	"L" peak output current (2) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			5	mA
$I_{OL(peak)}$	"L" peak output current (2) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_2$–$P7_4$			10	mA
$I_{OL(peak)}$	"L" peak output current (2) $P6_2$–$P6_7$			30	mA
$I_{OH(avg)}$	"H" average output current (3) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			−1.0	mA
$I_{OH(avg)}$	"H" average output current (3) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$			−2.5	mA
$I_{OL(avg)}$	"L" average output current (3) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			2.5	mA
$I_{OL(avg)}$	"L" average output current (3) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_2$–$P7_4$			5.0	mA
$I_{OL(avg)}$	"L" average output current (3) $P6_2$–$P6_7$			15	mA

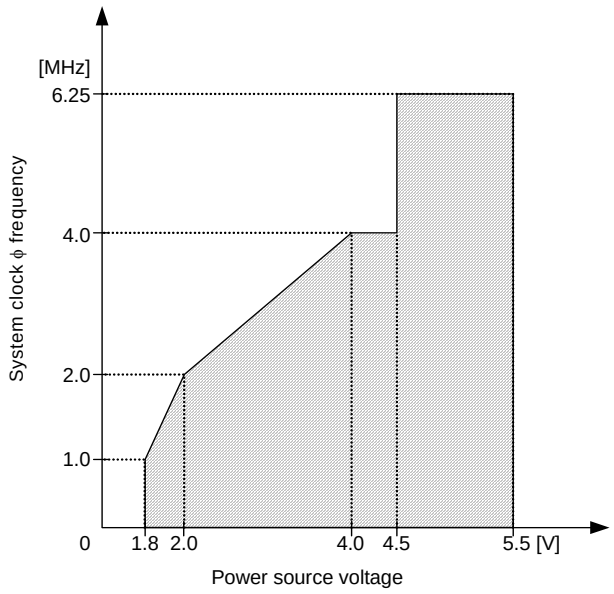
NOTES:
1. The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2. The peak output current is the peak current flowing in each port.
3. The average output current is average value measured over 100 ms.

Table 25 Recommended operating conditions (3)
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = −20 to 85°C, unless otherwise noted)

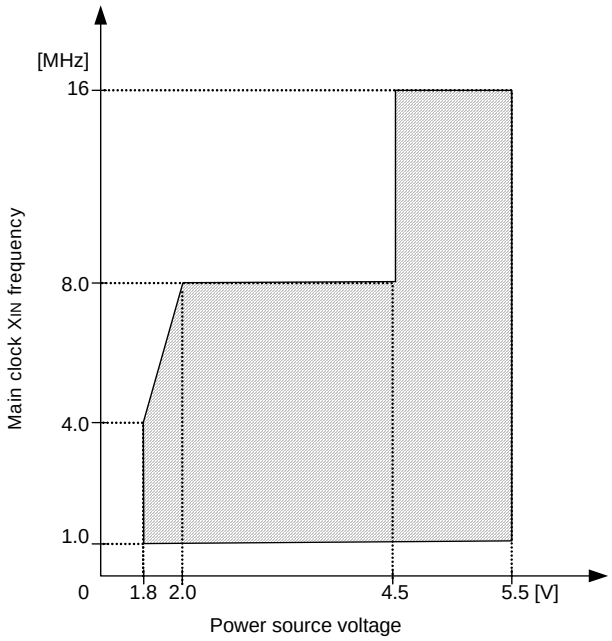
Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
f(CNTR0) f(CNTR1)	Timer X and Timer Y Input frequency (duty cycle 50%)	4.5 ≤ Vcc ≤ 5.5V			6.25	MHz
		4.0 ≤ Vcc < 4.5V			2 × Vcc −4	MHz
		2.0 ≤ Vcc < 4.0V			Vcc	MHz
		Vcc < 2.0V			5 × Vcc −8	MHz
f(Tclk)	Timer X, Timer Y, Timer 1, Timer 2, Timer 3, Timer 4 clock input frequency (Count source frequency of each timer)	4.5 ≤ Vcc ≤ 5.5V			16	MHz
		4.0 ≤ Vcc < 4.5V			4 × Vcc −8	MHz
		2.0 ≤ Vcc < 4.0V			2 × Vcc	MHz
		Vcc < 2.0V			10 × Vcc −16	MHz
f(ϕ)	System clock ϕ frequency (1)	4.5 ≤ Vcc ≤ 5.5V			6.25	MHz
		4.0 ≤ Vcc < 4.5V			4	MHz
		2.0 ≤ Vcc < 4.0V			Vcc	MHz
		Vcc < 2.0V			5 × Vcc −8	MHz
f(XIN)	Main clock input frequency (duty cycle 50%) (2)(3)	4.5 ≤ Vcc ≤ 5.5V	1.0		16	MHz
		2.0 ≤ Vcc < 4.5V	1.0		8.0	MHz
		Vcc < 2.0V	1.0		20 × Vcc −32	MHz
f(XCIN)	Sub-clock oscillation frequency (duty cycle 50%)(4)(5)			32.768	80	kHz

NOTES:
1. Relationship between system clock ϕ frequency and power source voltage is shown in the graph below.
2. When the A/D converter is used, refer to the recommended operating conditions of the A/D converter.
3. 12.5 MHz < f(XIN) ≤ 16 MHz is not available in the frequency/2 mode.
4. The oscillation start voltage and the oscillation start time differ depending on factors such as the oscillator, circuit constants, and operating temperature range. Note that oscillation start may be particularly difficult at low voltage when using a high-frequency oscillator.
5. When using the microcomputer in low-speed mode, set the clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

<System clock ϕ frequency>



<Main clock XIN frequency>



Electrical Characteristics

Table 26 Electrical characteristics (1)
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	I_{OH}= –2.5mA	V_{CC}–2.0			V
		I_{OH}= –0.6mA V_{CC}=2.5V	V_{CC}–1.0			
V_{OH}	"H" output voltage $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$ (1)	I_{OH}= –5mA	V_{CC}–2.0			V
		I_{OH}= –1.25mA	V_{CC}–0.5			
		I_{OH}= –1.25mA V_{CC}=2.5V	V_{CC}–1.0			
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	I_{OL}=5mA			2.0	V
		I_{OL}=1.25mA			0.5	
		I_{OL}=1.25mA V_{CC}=2.5V			1.0	
V_{OL}	"L" output voltage $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$ $P7_2$–$P7_4$ (1)	I_{OL}=10mA			2.0	V
		I_{OL}=2.5mA			0.5	
		I_{OL}=2.5mA V_{CC}=2.5V			1.0	
V_{OL}	"L" output voltage $P6_2$–$P6_7$	I_{OL}=15mA			2.0	V
		I_{OL}=3.0mA V_{CC}=2.5V			0.8	
V_{T+} – V_{T-}	Hysteresis INT_{00}, INT_{01}, INT_{10}, INT_{11}, INT_2, $CNTR_0$, $CNTR_1$, KW_0–KW_7			0.5		V
V_{T+} – V_{T-}	Hysteresis S_{IN2}, S_{CLK1}, S_{CLK2}, RxD			0.5		V
V_{T+} – V_{T-}	Hysteresis $\overline{RESET}$	V_{CC} = 2.0 V to 5.5 V on $\overline{RESET}$		0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I=V_{CC}			5.0	µA
I_{IH}	"H" input current $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_4$	V_I=V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$, OSCSEL	V_I=V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I=V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I=V_{SS} Pull-up "OFF"			–5.0	µA
		V_{CC}=5V, V_I=V_{SS} Pull-up "ON"	–60	–120	–240	µA
		V_{CC}=3V, V_I=V_{SS} Pull-up "ON"	–25	–50	–100	µA
I_{IL}	"L" input current $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_2$–$P7_4$	V_I=V_{SS} Pull-up "OFF"			–5.0	µA
		V_{CC}=5V, V_I=V_{SS} Pull-up "ON"	–30	–70	–140	µA
		V_{CC}=3V, V_I=V_{SS} Pull-up "ON"	–6.5	–25	–45	µA
I_{IL}	"L" input current $\overline{RESET}$, OSCSEL	V_I=V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I=V_{SS}		–4.0		µA
f(OCO)	On-chip oscillator frequency	V_{CC}=5V, Ta =25°C	2500	5000	7500	kHz

NOTE:
1. When the port Xc switch bit (bit 4 of address $003B_{16}$) of CPU mode register is "1", the drivability of $P6_1$ is different from the above.

Table 27 Electrical characteristics (2)
(Vcc = 1.8 to 5.5 V, Ta = –20 to 85°C, f(XCIN) = 32.768 kHz, output transistors in the cut-off state, A/D converter stopped, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
VRAM	RAM hold voltage	When clock is stopped			1.8		5.5	V
ICC	Power source current	Frequency/2 mode	VCC=5V	f(XIN)=12.5MHz		6.4	13	mA
				f(XIN)=12.5MHz (in WIT state)		1.5	3.0	mA
				f(XIN)=4MHz		2.2	3.0	mA
			VCC=2.5V	f(XIN)=4MHz		0.6	1.2	mA
				f(XIN)=4MHz (in WIT state)		0.3	0.6	mA
				f(XIN)=2MHz		0.4	0.8	mA
		Frequency/4 mode	VCC=5V	f(XIN)=12.5MHz		3.5	10	mA
				f(XIN)=12.5MHz (in WIT state)		1.5	3	mA
				f(XIN)=4MHz		1.5	2.5	mA
			VCC=2.5V	f(XIN)=8MHz		0.8	2.5	mA
				f(XIN)=8MHz (in WIT state)		0.3	0.6	mA
				f(XIN)=4MHz		0.5	1.0	mA
		Frequency/8 mode	VCC=5.0V	f(XIN)=12.5MHz		2.5	5.0	mA
				f(XIN)=12.5MHz (in WIT state)		1.5	3.0	mA
				f(XIN)=4MHz		1.2	1.6	mA
			VCC=2.5V	f(XIN)=8MHz		0.5	1.0	mA
				f(XIN)=8MHz (in WIT state)		0.3	0.6	mA
				f(XIN)=4MHz		0.3	0.6	mA
		Low-speed mode	VCC=5.0V	f(XIN)=stop		17	26	µA
				in WIT state		5.5	11	µA
			VCC=2.5V	f(XIN)=stop		7.0	14	µA
				in WIT state		3.5	7.0	µA
		On-chip oscillator mode f(XIN), f(XCIN) = stop		VCC=5V		270	540	µA
				VCC=2.5V		35	90	µA
				VCC=2.5V (in WIT state)		25	75	µA
		All oscillations stopped (in STP state)		Ta=25°C		0.1	1.0	µA
				Ta=85°C			10	µA
		Current increased at A/D converter operating		f(XIN)=12.5 MHz, VCC=5 V in frequency/2, 4 or 8 mode		0.5		mA
				f(XIN)= stop, VCC = 5 V in on-chip oscillator operating		0.5		mA
				f(XIN) = stop, VCC = 5 V in low-speed mode		0.4		mA

A/D Converter Characteristics

Table 28 A/D converter recommended operating condition
(Vcc = 2.0 to 5.5 V, Ta = –20 to 85°C, output transistors in cut-off state, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VCC	Power source voltage		2.0	5.0	5.5	V
VIH	"H" input voltage ADKEY0		0.9VCC		VCC	V
VIL	"L" input voltage ADKEY0		0		0.7 × VCC–0.5	V
f(φAD)	AD converter clock frequency (1) (Low-speed • on-chip oscillator mode excluded)	4.5V < VCC ≤ 5.5V			6.25	MHz
		4.0V < VCC ≤ 4.5V			4.0	MHz
		2.0V < VCC ≤ 4.0V			VCC	MHz

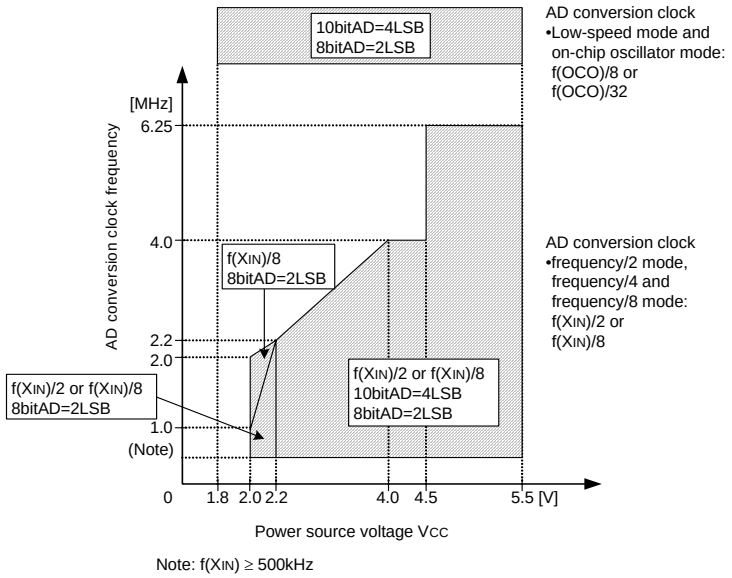
NOTE:
1. Confirm the recommended operating condition for main clock input frequency.

Table 29 A/D converter characteristics
(Vcc = 2.0 to 5.5 V, Ta = –20 to 85°C, output transistors in cut-off state, low-speed • on-chip oscillator mode included, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
–	Resolution					10	Bits
ABS	Absolute accuracy (quantification error excluded)	10bitAD mode	4.5V < Vcc ≤ 5.5V, AD conversion clock=f(XIN)/2, f(XIN)/8 ≤ 6.25MHz			4	LSB
			4.0V < Vcc ≤ 4.5V, AD conversion clock=f(XIN)/2, f(XIN)/8 ≤ 4MHz				
			2.2V ≤ Vcc ≤ 4.0V, AD conversion clock=f(XIN)/2, f(XIN)/8 ≤ VccMHz				
			2.0V ≤ Vcc ≤ 5.5V, AD conversion clock=f(OCO)/8, f(OCO)/32				
		8bitAD mode	4.5V < Vcc ≤ 5.5V, AD conversion clock=f(XIN)/2, f(XIN)/8 ≤ 6.25MHz			2	
			4.0V < Vcc ≤ 4.5V, AD conversion clock=f(XIN)/2, f(XIN)/8 ≤ 4MHz				
			2.2V < Vcc ≤ 4.0V, AD conversion clock=f(XIN)/2, f(XIN)/8 ≤ VccMHz				
			2.0V ≤ Vcc ≤ 2.2V, AD conversion clock=f(XIN)/2, f(XIN)/8 ≤ (6Vcc–11)MHz				
			2.0V ≤ Vcc ≤ 2.2V, AD conversion clock=f(XIN)/8 ≤ VccMHz				
			2.0V ≤ Vcc ≤ 5.5V, AD conversion clock=f(OCO)/8, f(OCO)/32				
tCONV	Conversion time(1)	10bitAD mode		tc(φAD)×61		tc(φAD)×62	µs
		8bitAD mode		tc(φAD)×49		tc(φAD)×50	
RLADDER	Ladder resistor			12	35	100	kΩ
IVREF	Reference input current	VREF=5.0V		50	150	200	µA
IIA	Analog input current					5.0	µA

NOTES:
1. tc(φAD): one cycle of AD conversion clock. AD conversion clock can be selected from φSOURCE/2 or φSOURCE/8. φSOURCE represents the XIN input in the frequency/2, 4 or 8 mode and internal on-chip oscillator divided by 4 in the on-chip oscillator mode or the low-speed mode.
When the A/D conversion is executed in the frequency/2 mode, frequency/4 mode, or frequency/8 mode, set f(XIN) ≥ 500 kHz.

Relationship among AD conversion clock frequency, power source voltage, AD conversion mode and absolute accuracy.



Note: f(XIN) ≥ 500kHz

Timing Requirements And Switching Characteristics

Table 30 Timing requirements (1)
(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{W(RESET)}$	Reset input “L” pulse width		2			µs
$t_{C(XIN)}$	Main clock input cycle time	4.5V ≤ Vcc ≤ 5.5V (1)	62.5			ns
		4.0V ≤ Vcc < 4.5V	125			ns
$t_{WH(XIN)}$	Main clock input “H” pulse width	4.5V ≤ Vcc ≤ 5.5V (2)	25			ns
		4.0V ≤ Vcc < 4.5V	50			ns
$t_{WL(XIN)}$	Main clock input “L” pulse width	4.5V ≤ Vcc ≤ 5.5V (2)	25			ns
		4.0V ≤ Vcc < 4.5V	50			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time		250			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width		105			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width		105			ns
$t_{WH(INT)}$	INT_{00}, INT_{01}, INT_{10}, INT_{11}, INT_2 input “H” pulse width		80			ns
$t_{WL(INT)}$	INT_{00}, INT_{01}, INT_{10}, INT_{11}, INT_2 input “L” pulse width		80			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time (3)		800			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width (3)		370			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width (3)		370			ns
$t_{su(RXD-SCLK1)}$	Serial I/O1 input setup time		220			ns
$t_{h(SCLK1-RXD)}$	Serial I/O1 input hold time		100			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time		1000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width		400			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width		400			ns
$t_{su(SIN2-SCLK2)}$	Serial I/O2 input setup time		200			ns
$t_{h(SCLK2-SIN2)}$	Serial I/O2 input hold time		200			ns

NOTES:
1. 80 ns in the frequency/2 mode.
2. 32 ns in the frequency/2 mode.
3. When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
   Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 31 Timing requirements (2)
(V_{CC} = 1.8 to 4.0 V, V_{SS} = 0 V, Ta = −20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{W(RESET)}$	Reset input “L” pulse width		2			μs
$t_{C(XIN)}$	Main clock input cycle time (X_{IN} input)	2.0V ≤ V_{CC} < 4.0V	125			ns
		V_{CC} < 2.0V	166			ns
$t_{WH(XIN)}$	Main clock input “H” pulse width	2.0V ≤ V_{CC} < 4.0V	50			ns
		V_{CC} < 2.0V	70			ns
$t_{WL(XIN)}$	Main clock input “L” pulse width	2.0V ≤ V_{CC} < 4.0V	50			ns
		V_{CC} < 2.0V	70			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	2.0V ≤ V_{CC} < 4.0V	1000/V_{CC}			ns
		V_{CC} < 2.0V	1000/(5 × V_{CC}-8)			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width		tc(CNTR)/2-20			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width		tc(CNTR)/2-20			ns
$t_{WH(INT)}$	INT_{00}, INT_{01}, INT_{10}, INT_{11}, INT_2 input “H” pulse width		230			ns
$t_{WL(INT)}$	INT_{00}, INT_{01}, INT_{10}, INT_{11}, INT_2 input “L” pulse width		230			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time (1)		2000			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width (1)		950			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width (1)		950			ns
$t_{su(RXD-SCLK1)}$	Serial I/O1 input setup time		400			ns
$t_{h(SCLK1-RXD)}$	Serial I/O1 input hold time		200			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time		2000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width		950			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width		950			ns
$t_{su(SIN2-SCLK2)}$	Serial I/O2 input setup time		400			ns
$t_{h(SCLK2-SIN2)}$	Serial I/O2 input hold time		200			ns

NOTE:
1. When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 32 Switching characteristics (1)
(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1 clock output “H” pulse width	$t_c(S_{CLK1})$/2-30			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock output “L” pulse width	$t_c(S_{CLK1})$/2-30			ns
$t_d(S_{CLK1}\text{-}T_xD)$	Serial I/O1 output delay time (1)			140	ns
$t_v(S_{CLK1}\text{-}T_xD)$	Serial I/O1 output valid time (1)	–30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time			30	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time			30	ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output “H” pulse width	$t_c(S_{CLK2})$/2-30			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output “L” pulse width	$t_c(S_{CLK2})$/2-30			ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time			40	ns
$t_d(S_{CLK2}\text{-}S_{OUT2})$	Serial I/O2 output delay time			140	ns
$t_v(S_{CLK2}\text{-}S_{OUT2})$	Serial I/O2 output valid time	–30			ns

NOTE:
1. The $P4_1$/TxD P-channel output disable bit (bit 4 of address $001B_{16}$) of UART control register is “0”.

Table 33 Switching characteristics (2)
(V_{CC} = 1.8 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1 clock output “H” pulse width	$t_c(S_{CLK1})$/2-80			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock output “L” pulse width	$t_c(S_{CLK1})$/2-80			ns
$t_d(S_{CLK1}\text{-}T_xD)$	Serial I/O1 output delay time (1)			350	ns
$t_v(S_{CLK1}\text{-}T_xD)$	Serial I/O1 output valid time (1)	-30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time			80	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time			80	ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output “H” pulse width	$t_c(S_{CLK2})$/2-80			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output “L” pulse width	$t_c(S_{CLK2})$/2-80			ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time			80	ns
$t_d(S_{CLK2}\text{-}S_{OUT2})$	Serial I/O2 output delay time			350	ns
$t_v(S_{CLK2}\text{-}S_{OUT2})$	Serial I/O2 output valid time	-30			ns

NOTE:
1. The $P4_1$/TxD P-channel output disable bit (bit 4 of address $001B_{16}$) of UART control register is “0”.

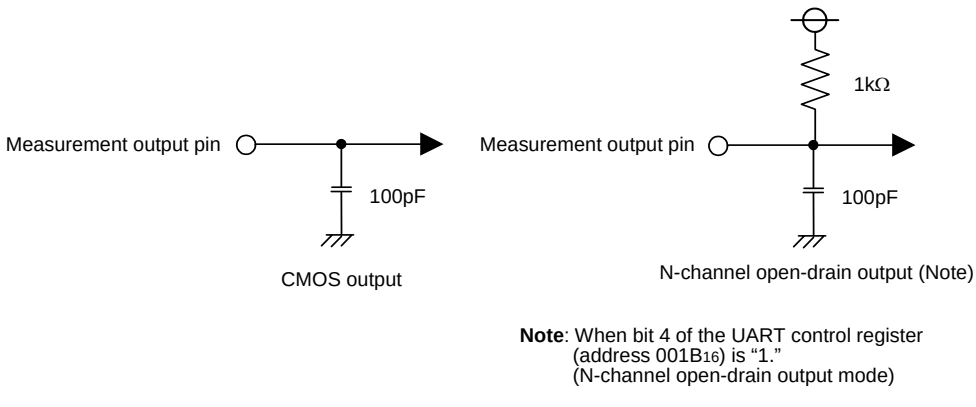


Fig 95. Circuit for measuring output switching characteristics

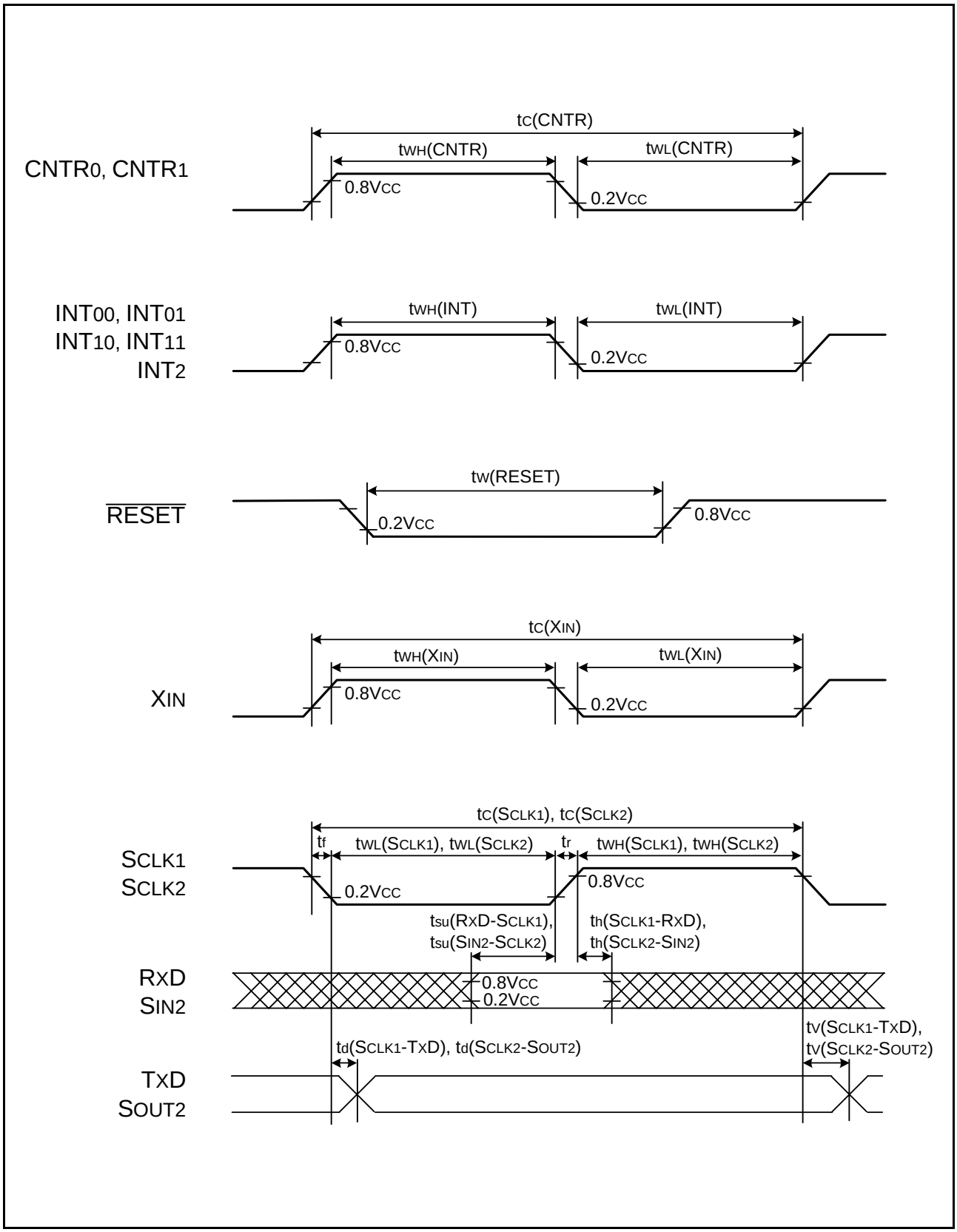


Fig 96. Timing diagram

FLASH MEMORY VERSION ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Table 34 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage		All voltages are based on V_{SS}. When an input voltage is measured, output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_4$			–0.3 to V_{CC}+0.3	V
V_I	Input voltage V_{L1}			–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}			V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}			V_{L2} to 6.5	V
V_I	Input voltage C_1, C_2			–0.3 to 6.5	V
V_I	Input voltage $\overline{RESET}$, X_{IN}, CNV_{SS}			–0.3 to V_{CC}+0.3	V
V_O	Output voltage C_1, C_2			–0.3 to 6.5	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	At output port		–0.3 to V_{CC}+0.3	V
		At segment output		–0.3 to V_{L3}+0.3	V
V_O	Output voltage $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$			–0.3 to V_{CC}+0.3	V
V_O	Output voltage V_{L3}			–0.3 to 6.5	V
V_O	Output voltage V_{L2}, SEG_{32}–SEG_{35}, COM_0–COM_3			–0.3 to V_{L3}+0.3	V
V_O	Output voltage X_{OUT}			–0.3 to V_{CC}+0.3	V
Pd	Power dissipation		Ta=25°C	300	mW
Topr	Operating temperature			–20 to 85	°C
Tstg	Storage temperature			–40 to 125	°C

Recommended Operating Conditions

Table 35 Recommended operating conditions (1)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85°C unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Power source voltage(1)	Frequency/2 mode (2)	$f(X_{IN}) \leq 12.5$MHz	4.5		5.5	V
			$f(X_{IN}) \leq 8$MHz	4.0		5.5	V
			$f(X_{IN}) \leq 4$MHz	2.7		5.5	V
		Frequency/4 mode	$f(X_{IN}) \leq 16$MHz	4.5		5.5	V
			$f(X_{IN}) \leq 8$MHz	2.7		5.5	V
		Frequency/8 mode	$f(X_{IN}) \leq 16$MHz	4.5		5.5	V
			$f(X_{IN}) \leq 8$MHz	2.7		5.5	V
		Low-speed mode		2.7		5.5	V
		On-chip oscillator mode		2.7		5.5	V
V_{SS}	Power source voltage				0		V
V_{LI}	V_{L1} input voltage	Voltage multiplier is used		1.3	1.8	2.1	V
V_{REF}	A/D converter reference voltage			2.7		V_{CC}	V
AV_{SS}	Analog power source voltage				0		V
V_{IA}	Analog input voltage	AN_0–AN_7		AV_{SS}		V_{CC}	V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_4$–$P2_7$, $P3_0$–$P3_7$,$P4_1$, $P4_3$, $P5_0$–$P5_7$, $P6_0$ (CM_4=0), $P6_1$, $P6_5$, $P7_2$–$P7_4$		0.7V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$P2_0$–$P2_3$, $P4_0$, $P4_2$, $P4_4$–$P4_7$, $P6_2$–$P6_4$, $P6_6$, $P6_7$, $P7_0$, $P7_1$		0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$		0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	X_{IN}		0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_4$–$P2_7$, $P3_0$–$P3_7$, $P4_1$, $P4_3$, $P5_0$–$P5_7$, $P6_0$ (CM_4=0), $P6_1$, $P6_5$, $P7_2$–$P7_4$		0		0.3V_{CC}	V
V_{IL}	“L” input voltage	$P2_0$–$P2_3$, $P4_0$, $P4_2$, $P4_4$–$P4_7$, $P6_2$–$P6_4$, $P6_6$, $P6_7$, $P7_0$, $P7_1$		0		0.2V_{CC}	V
V_{IL}	“L” input voltage	$\overline{RESET}$		0		0.2V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}		0		0.2V_{CC}	V

NOTES:
1. When the A/D converter is used, refer to the recommended operating conditions of the A/D converter.
2. 12.5 MHz < $f(X_{IN}) \leq$ 16 MHz is not available in the frequency/2 mode.

Table 36 Recommended operating conditions (2)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = −20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma_{OH(peak)}$	"H" total peak output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P7_2$–$P7_4$			−40	mA
$\Sigma_{OH(peak)}$	"H" total peak output current (1) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$			−40	mA
$\Sigma_{OL(peak)}$	"L" total peak output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P7_2$–$P7_4$			40	mA
$\Sigma_{OL(peak)}$	"L" total peak output current (1) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$			40	mA
$\Sigma_{OL(peak)}$	"L" total peak output current (1) $P6_2$–$P6_7$			110	mA
$\Sigma_{OH(avg)}$	"H" total average output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P7_2$–$P7_4$			−20	mA
$\Sigma_{OH(avg)}$	"H" total average output current (1) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$			−20	mA
$\Sigma_{OL(avg)}$	"L" total average output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P7_2$–$P7_4$			20	mA
$\Sigma_{OL(avg)}$	"L" total average output current (1) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$			20	mA
$\Sigma_{OL(avg)}$	"L" total average output current (1) $P6_2$–$P6_7$			90	mA
$I_{OH(peak)}$	"H" peak output current (2) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			−2	mA
$I_{OH(peak)}$	"H" peak output current (2) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$			−5	mA
$I_{OL(peak)}$	"L" peak output current (2) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			5	mA
$I_{OL(peak)}$	"L" peak output current (2) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P7_2$–$P7_4$			10	mA
$I_{OL(peak)}$	"L" peak output current (2) $P6_2$–$P6_7$			30	mA
$I_{OH(avg)}$	"H" average output current (3) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			−1.0	mA
$I_{OH(avg)}$	"H" average output current (3) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$			−2.5	mA
$I_{OL(avg)}$	"L" average output current (3) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			2.5	mA
$I_{OL(avg)}$	"L" average output current (3) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$			5.0	mA
$I_{OL(avg)}$	"L" average output current (3) $P6_2$–$P6_7$			15	mA

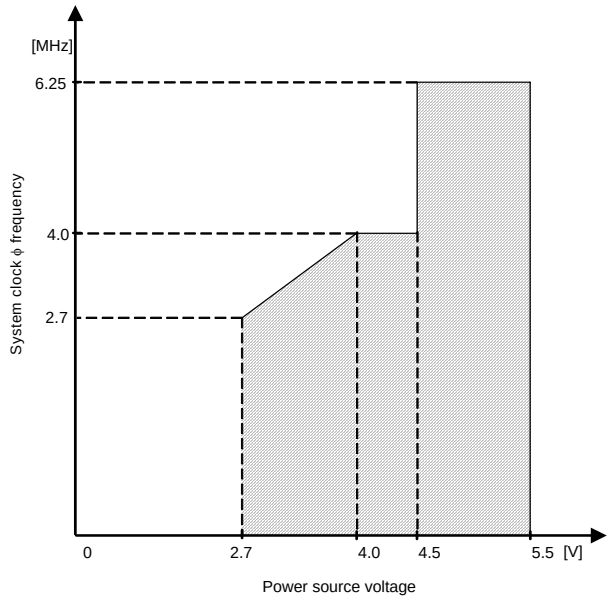
NOTES:
1. The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2. The peak output current is the peak current flowing in each port.
3. The average output current is average value measured over 100 ms.

Table 37 Recommended operating conditions (3)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = −20 to 85°C, unless otherwise noted)

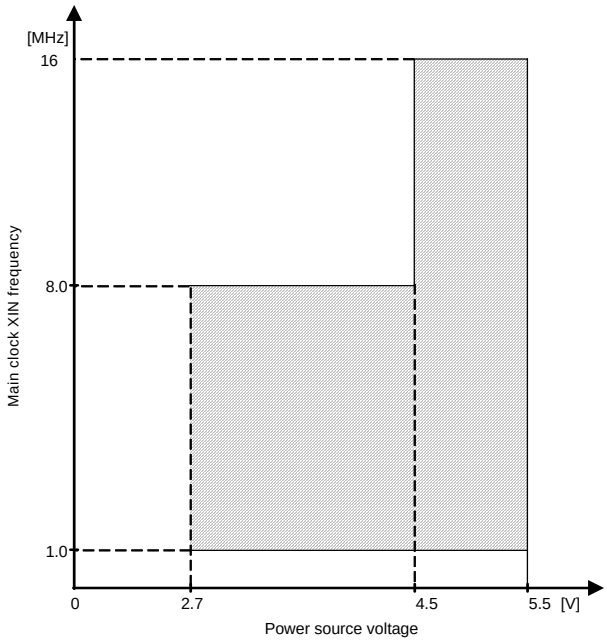
Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
f(CNTR0) f(CNTR1)	Timer X and Timer Y Input frequency (duty cycle 50%)	4.5V ≤ Vcc ≤ 5.5V			6.25	MHz
		4.0V ≤ Vcc < 4.5V			2×Vcc−4	MHz
		2.7V ≤ Vcc < 4.0V			Vcc	MHz
f(Tclk)	Timer X, Timer Y, Timer 1, Timer 2, Timer 3, Timer 4 clock input frequency (Count source frequency of each timer)	4.5V ≤ Vcc ≤ 5.5V			16	MHz
		4.0V ≤ Vcc < 4.5V			4×Vcc−8	MHz
		2.7V ≤ Vcc < 4.0V			2×Vcc	MHz
f(ϕ)	System clock ϕ frequency (1)	4.5V ≤ Vcc ≤ 5.5V			6.25	MHz
		4.0V ≤ Vcc < 4.5V			4	MHz
		2.7V ≤ Vcc < 4.0V			Vcc	MHz
f(XIN)	Main clock input frequency (duty cycle 50%) (2)(3)	4.5V ≤ Vcc ≤ 5.5V	1.0		16	MHz
		2.7V ≤ Vcc < 4.5V	1.0		8.0	MHz
f(XCIN)	Sub-clock oscillation frequency (duty cycle 50%) (4)(5)			32.768	80	kHz

NOTES:
1. Relationship between system clock ϕ frequency and power source voltage is shown in the graph below.
2. When the A/D converter is used, refer to the recommended operating conditions of the A/D converter.
3. 12.5 MHz < f(XIN) ≤ 16 MHz is not available in the frequency/2 mode.
4. The oscillation start voltage and the oscillation start time differ depending on factors such as the oscillator, circuit constants, and operating temperature range. Note that oscillation start may be particularly difficult at low voltage when using a high-frequency oscillator.
5. When using the microcomputer in low-speed mode, set the clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

<System clock ϕ frequency>



<Main clock XIN frequency>



Electrical Characteristics

Table 38 Electrical characteristics (1)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	I_{OH}= –2.5mA	V_{CC}–2.0			V
V_{OH}	"H" output voltage $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$ (1)	I_{OH}= –5mA	V_{CC}–2.0			V
		I_{OH}= –1.25mA	V_{CC}–0.5			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	I_{OL}=5mA			2.0	V
		I_{OL}=1.25mA			0.5	
V_{OL}	"L" output voltage $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$ (1)	I_{OL}=10mA			2.0	V
		I_{OL}=2.5mA			0.5	
V_{OL}	"L" output voltage $P6_2$–$P6_7$	I_{OL}=15mA			2.0	V
V_{T+}–V_{T-}	Hysteresis INT_{00}, INT_{01}, INT_{10}, INT_{11}, INT_2, $CNTR_0$, $CNTR_1$, KW_0–KW_7			0.5		V
V_{T+}–V_{T-}	Hysteresis S_{IN2}, S_{CLK1}, S_{CLK2}, RxD			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I=V_{CC}			5.0	µA
I_{IH}	"H" input current $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_4$	V_I=V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$, CNV_{SS}	V_I=V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I=V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I=V_{SS} Pull-up "OFF"			–5.0	µA
		V_{CC}=5V, V_I=V_{SS} Pull-up "ON"	–60	–120	–240	µA
		V_{CC}=3V, V_I=V_{SS} Pull-up "ON"	–25	–50	–100	µA
I_{IL}	"L" input current $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_2$–$P7_4$	V_I=V_{SS} Pull-up "OFF"			–5.0	µA
		V_{CC}=5V, V_I=V_{SS} Pull-up "ON"	–30	–70	–140	µA
		V_{CC}=3V, V_I=V_{SS} Pull-up "ON"	–6.5	–25	–45	µA
I_{IL}	"L" input current $\overline{RESET}$, CNV_{SS}	V_I=V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I=V_{SS}		–4.0		µA
f(OCO)	On-chip oscillator frequency	V_{CC}=5V, Ta=25°C	2500	5000	7500	kHz

NOTE:
1. When the port Xc switch bit (bit 4 of address $003B_{16}$) of CPU mode register is "1", the drivability of $P6_1$ is different from the above.

Table 39 Electrical characteristics (2)
(Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, f(XCIN) = 32.768 kHz, output transistors in the cut-off state, A/D converter stopped, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
VRAM	RAM hold voltage	When clock is stopped			2.2		5.5	V
ICC	Power source current	Frequency/2 mode	Vcc=5.0V	f(XIN)=12.5MHz		4.0	7.0	mA
				f(XIN)=12.5MHz (in WIT state)		2.0	3.5	mA
				f(XIN)=4MHz		2.0	3.5	mA
			Vcc=2.7V	f(XIN)=4MHz		1.5	3	mA
				f(XIN)=4MHz (in WIT state)		1.0	2.5	mA
				f(XIN)=2MHz		1.0	2.5	mA
		Frequency/4 mode	Vcc=5.0V	f(XIN)=12.5MHz		3.2	5.6	mA
				f(XIN)=12.5MHz (in WIT state)		1.6	3.2	mA
				f(XIN)=4MHz		1.6	3.2	mA
			Vcc=2.7V	f(XIN)=8MHz		1.6	3.2	mA
				f(XIN)=8MHz (in WIT state)		1.0	2.5	mA
				f(XIN)=4MHz		1.0	2.5	mA
		Frequency/8 mode	Vcc=5.0V	f(XIN)=12.5MHz		2.5	5	mA
				f(XIN)=12.5MHz (in WIT state)		1.5	3	mA
				f(XIN)=4MHz		1.5	3	mA
			Vcc=2.7V	f(XIN)=8MHz		1.5	3	mA
				f(XIN)=8MHz (in WIT state)		1.0	2.5	mA
				f(XIN)=4MHz		1.0	2.5	mA
		Low-speed mode	Vcc=5.0V	f(XIN)=stop		400	800	µA
				in WIT state Ta=25°C		4.0	10	µA
				in WIT state Ta=85°C			20	
			Vcc=2.7V	f(XIN)=stop		300	600	µA
				in WIT state Ta=25°C		3.7	9	µA
				in WIT state Ta=85°C			18	
		On-chip oscillator mode f(XIN), f(XCIN), stop		Vcc=5.0V		600	1200	µA
				Vcc=2.7V		500	1000	µA
				Vcc=2.7V (in WIT state)		500	1000	µA
		All oscillations stopped (in STP state)		Ta=25°C		0.6	3.0	µA
				Ta=85°C		1.0		µA
		Current increased at A/D converter operating		f(XIN)=12.5MHz, Vcc=5V in frequency/2, 4 or 8 mode		1.0		mA
				f(XIN)=stop, Vcc=5V in on-chip oscillator operating		1.0		mA
				f(XIN)=stop, Vcc=5V in low-speed mode		0.8		mA

A/D Converter Characteristics

Table 40 A/D converter recommended operating condition
(Vcc = 2.7 to 5.5 V, Ta = –20 to 85°C, output transistors in cut-off state, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage		2.7	5.0	5.5	V
VIH	"H" input voltage ADKEY0		0.9Vcc		Vcc	V
VIL	"L" input voltage ADKEY0		0		0.7 × Vcc – 0.5	V
f(ϕAD)	AD converter clock frequency (1) (Low-speed・on-chip oscillator mode excluded)	4.5V < Vcc ≤ 5.5V			6.25	MHz
		4.0V < Vcc ≤ 4.5V			4.0	MHz
		2.7V < Vcc ≤ 4.0V			Vcc	MHz

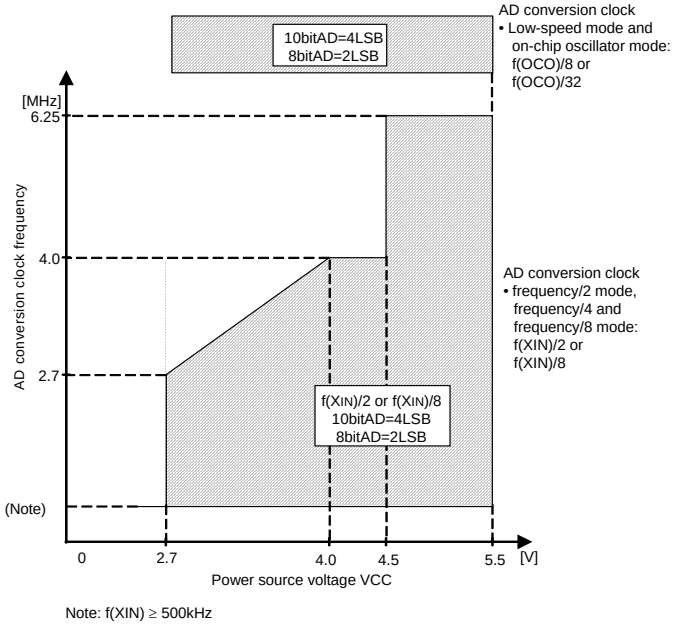
NOTE:
1. Confirm the recommended operating condition for main clock input frequency.

Table 41 A/D converter characteristics
(Vcc = 2.7 to 5.5 V, Ta = –20 to 85°C, output transistors in cut-off state, low-speed • on-chip oscillator mode included, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
–	Resolution					10	Bits
ABS	Absolute accuracy (quantification error excluded)	10bitAD mode	4.5V < Vcc ≤ 5.5V, AD conversion clock=f(XIN)/2, f(XIN)/8≤6.25MHz			4	LSB
			4.0V < Vcc ≤ 4.5V, AD conversion clock=f(XIN)/2, f(XIN)/8≤4MHz				
			2.7V ≤ Vcc ≤ 4.0V, AD conversion clock, f(XIN)/2, f(XIN)/8≤VccMHz				
			2.7V ≤ Vcc ≤ 5.5V, f(OCO)/8, f(OCO)/32				
		8bitAD mode	4.5V < Vcc ≤ 5.5V, AD conversion clock=f(XIN)/2, f(XIN)/8≤6.25MHz			2	
			4.0V < Vcc ≤ 4.5V, AD conversion clock=f(XIN)/2, f(XIN)/8≤4MHz				
			2.7V ≤ Vcc ≤ 4.0V, AD conversion clock=f(XIN)/2, f(XIN)/8≤VccMHz				
			2.7V ≤ Vcc ≤ 5.5V, f(OCO)/8, f(OCO)/32				
tCONV	Conversion time(1)	10bitAD mode		tc(φAD) × 61		tc(φAD) × 62	μs
		8bitAD mode		tc(φAD) × 49		tc(φAD) × 50	
RLADDER	Ladder resistor			12	35	100	kΩ
IVREF	Reference input current	VREF=5V		50	150	200	μA
IIA	Analog input current					5.0	μA

NOTE:
1. tc(φAD): one cycle of AD conversion clock. AD conversion clock can be selected from φSOURCE/2 or φSOURCE/8. φSOURCE represents the XIN input in the frequency/2, 4 or 8 mode and internal on-chip oscillator divided by 4 in the on-chip oscillator mode or the low-speed mode.
When the A/D conversion is executed in the frequency/2 mode, frequency/4 mode, or frequency/8 mode, set f(XIN) ≥ 500 kHz.

Relationship among AD conversion clock frequency, power source voltage, AD conversion mode and absolute accuracy.



Note: f(XIN) ≥ 500kHz

Timing Requirements And Switching Characteristics

Table 42 Power supply circuit characteristics
(Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
td(P-R)	Internal power source voltage stabilizes time at power-on	2.7 ≤ Vcc ≤ 5.5V	2			ms

Table 43 Timing requirements (1)
(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
tw(RESET)	Reset input “L” pulse width		2			µs
tc(XIN)	Main clock input cycle time	4.5V ≤ Vcc ≤ 5.5V (1)	62.5			ns
		4.0V ≤ Vcc < 4.5V	125			ns
twH(XIN)	Main clock input “H” pulse width	4.5V ≤ Vcc ≤ 5.5V (2)	25			ns
		4.0V ≤ Vcc < 4.5V	50			ns
twL(XIN)	Main clock input “L” pulse width	4.5V ≤ Vcc ≤ 5.5V (2)	25			ns
		4.0V ≤ Vcc < 4.5V	50			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time		250			ns
twH(CNTR)	CNTR0, CNTR1 input “H” pulse width		105			ns
twL(CNTR)	CNTR0, CNTR1 input “L” pulse width		105			ns
twH(INT)	INT00, INT01, INT10, INT11, INT2 input “H” pulse width		80			ns
twL(INT)	INT00, INT01, INT10, INT11, INT2 input “L” pulse width		80			ns
tc(SCLK1)	Serial I/O1 clock input cycle time (3)		800			ns
twH(SCLK1)	Serial I/O1 clock input “H” pulse width (3)		370			ns
twL(SCLK1)	Serial I/O1 clock input “L” pulse width (3)		370			ns
tsu(RxD-SCLK1)	Serial I/O1 input setup time		220			ns
th(SCLK1-RxD)	Serial I/O1 input hold time		100			ns
tc(SCLK2)	Serial I/O2 clock input cycle time		1000			ns
twH(SCLK2)	Serial I/O2 clock input “H” pulse width		400			ns
twL(SCLK2)	Serial I/O2 clock input “L” pulse width		400			ns
tsu(SIN2-SCLK2)	Serial I/O2 input setup time		200			ns
th(SCLK2-SIN2)	Serial I/O2 input hold time		200			ns

NOTES:
1. 80 ns in the frequency/2 mode.
2. 32 ns in the frequency/2 mode.
3. When bit 6 of address 001A16 is “1” (clock synchronous).
Divide this value by four when bit 6 of address 001A16 is “0” (UART).

Table 44 Timing requirements (2)
(V_{CC} = 2.7 to 4.0 V, V_{SS} = 0 V, Ta = −20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(RESET)}$	Reset input “L” pulse width	2			μs
$t_{C(XIN)}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{WH(XIN)}$	Main clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	Main clock input “L” pulse width	50			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	1000/V_{CC}			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	tc(CNTR)/2−20			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	tc(CNTR)/2−20			ns
$t_{WH(INT)}$	INT_{00}, INT_{01}, INT_{10}, INT_{11}, INT_2 input “H” pulse width	230			ns
$t_{WL(INT)}$	INT_{00}, INT_{01}, INT_{10}, INT_{11}, INT_2 input “L” pulse width	230			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time	2000			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width	950			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width	950			ns
$t_{su(RXD-SCLK1)}$	Serial I/O1 input setup time	400			ns
$t_{h(SCLK1-RXD)}$	Serial I/O1 input hold time	200			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su(SIN2-SCLK2)}$	Serial I/O2 input setup time	400			ns
$t_{h(SCLK2-SIN2)}$	Serial I/O2 input hold time	200			ns

NOTE:
1. When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 45 Switching characteristics (1)
(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ	Max.	
t_{WH} (S_{CLK1})	Serial I/O1 clock output “H” pulse width	t_{C}(S_{CLK1})/2–30			ns
t_{WL} (S_{CLK1})	Serial I/O1 clock output “L” pulse width	t_{C}(S_{CLK1})/2–30			ns
t_{d} (S_{CLK1}-TxD)	Serial I/O1 output delay time (1)			140	ns
t_{V} (S_{CLK1}-TxD)	Serial I/O1 output valid time (1)	–30			ns
t_{r} (S_{CLK1})	Serial I/O1 clock output rising time			30	ns
t_{f} (S_{CLK1})	Serial I/O1 clock output falling time			30	ns
t_{WH} (S_{CLK2})	Serial I/O2 clock output “H” pulse width	t_{C}(S_{CLK2})/2–30			ns
t_{WL} (S_{CLK2})	Serial I/O2 clock output “L” pulse width	t_{C}(S_{CLK2})/2–30			ns
t_{f} (S_{CLK2})	Serial I/O2 clock output falling time			40	ns
t_{d} (S_{CLK2}-S_{OUT2})	Serial I/O2 output delay time			140	ns
t_{V} (S_{CLK2}-S_{OUT2})	Serial I/O2 output valid time	–30			ns

NOTE:
1. The P41/TxD P-channel output disable bit (bit 4 of address 001B16) of UART control register is “0”.

Table 46 Switching characteristics (2)
(Vcc = 2.7 to 4.0 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ	Max.	
t_{WH} (S_{CLK1})	Serial I/O1 clock output “H” pulse width	t_{C}(S_{CLK1})/2–80			ns
t_{WL} (S_{CLK1})	Serial I/O1 clock output “L” pulse width	t_{C}(S_{CLK1})/2–80			ns
t_{d} (S_{CLK1}-TxD)	Serial I/O1 output delay time (1)			350	ns
t_{V} (S_{CLK1}-TxD)	Serial I/O1 output valid time (1)	–30			ns
t_{r} (S_{CLK1})	Serial I/O1 clock output rising time			80	ns
t_{f} (S_{CLK1})	Serial I/O1 clock output falling time			80	ns
t_{WH} (S_{CLK2})	Serial I/O2 clock output “H” pulse width	t_{C}(S_{CLK2})/2–80			ns
t_{WL} (S_{CLK2})	Serial I/O2 clock output “L” pulse width	t_{C}(S_{CLK2})/2–80			ns
t_{f} (S_{CLK2})	Serial I/O2 clock output falling time			80	ns
t_{d} (S_{CLK2}-S_{OUT2})	Serial I/O2 output delay time			350	ns
t_{V} (S_{CLK2}-S_{OUT2})	Serial I/O2 output valid time	–30			ns

NOTE:
1. The P41/TxD P-channel output disable bit (bit 4 of address 001B16) of UART control register is “0”.

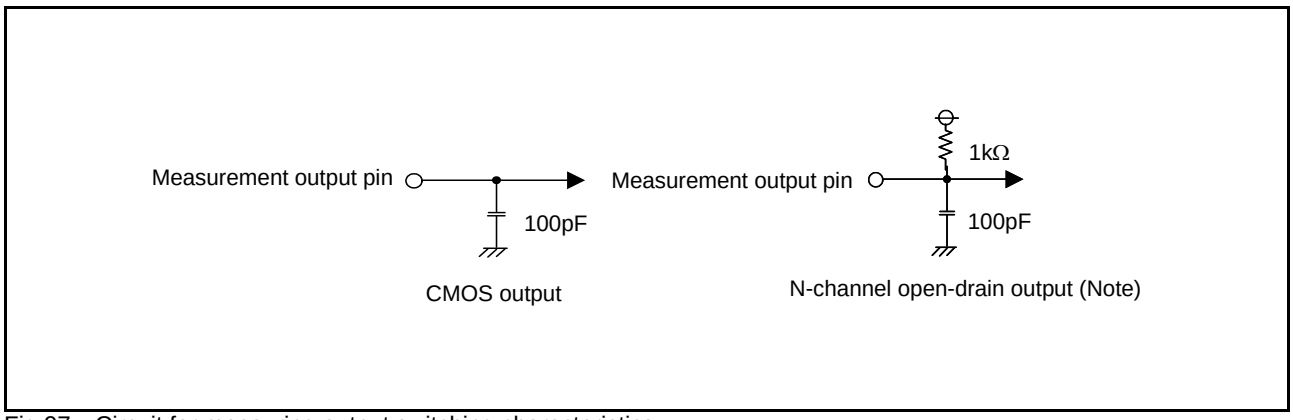


Fig 97. Circuit for measuring output switching characteristics

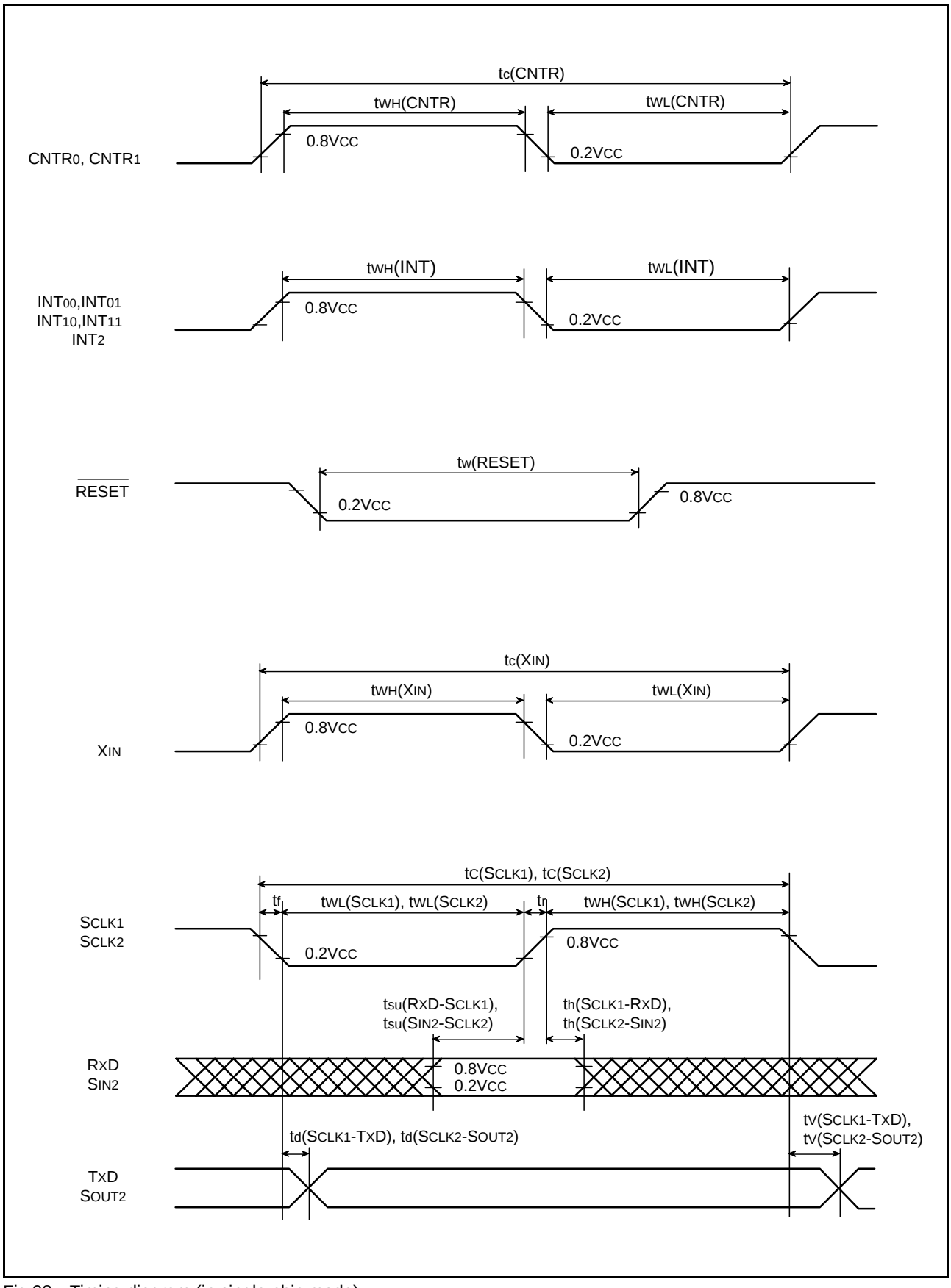
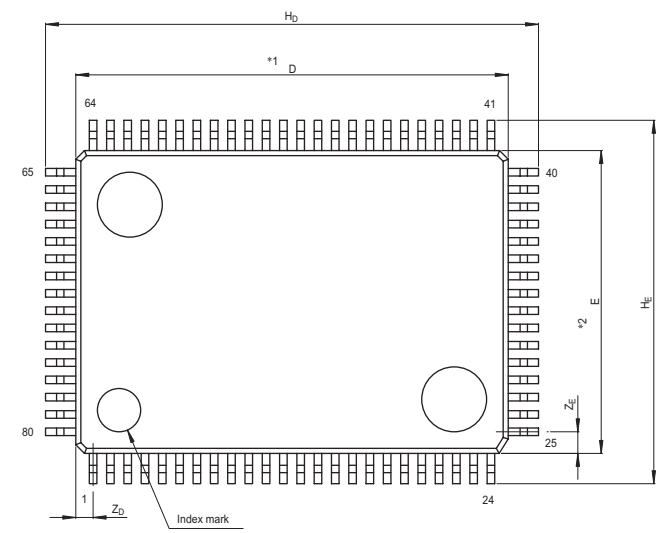


Fig 98. Timing diagram (in single-chip mode)

PACKAGE OUTLINE

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

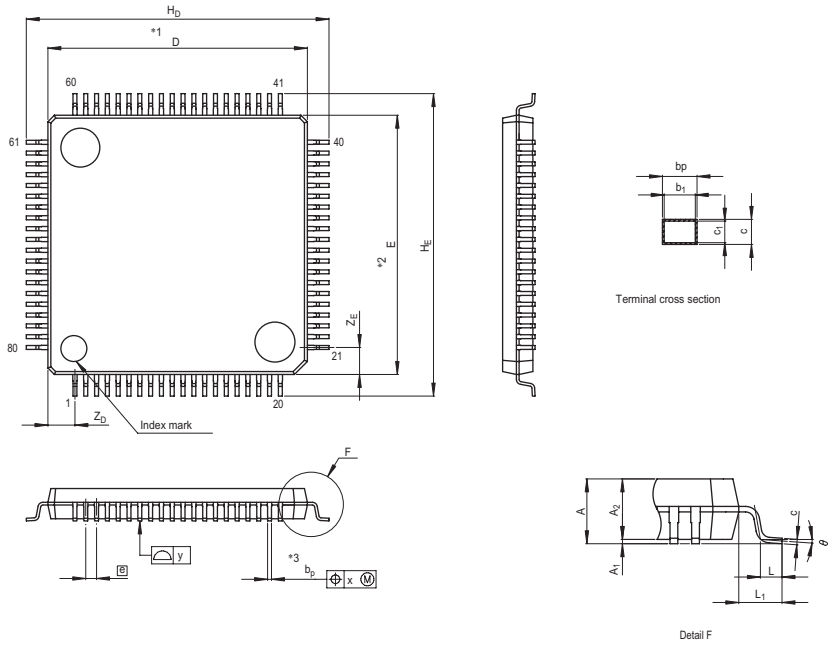
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP80-14x20-0.80	PRQP0080GB-A	80P6N-A	1.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.3	0.35	0.45
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.65	0.8	0.95
y	—	—	0.10
Z_D	—	0.8	—
Z_E	—	1.0	—
L	0.4	0.6	0.8

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

APPENDIX

Note on Programming

1. Processor Status Register

(1) Initialization of the processor status register

It is required to initialize the processor status register (PS) flags which affect program execution. It is particularly essential to initialize the T and D flags because of their effect on calculations. Initialize these flags at the beginning of the program.

<Reason>

At a reset, the contents of the processor status register (PS) are undefined except for the I flag which is "1".

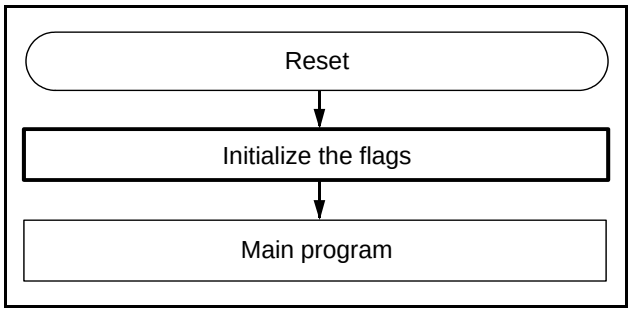


Fig. 99 Initialization of processor status register flags

(2) How to refer the processor status register

To refer the contents of the processor status register (PS), execute the PHP instruction once and then read the contents of (S+1). If necessary, execute the PLP instruction to return the stored PS to its original status.

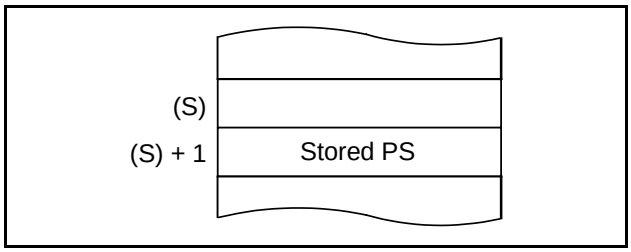


Fig. 100 Stack memory contents after PHP instruction execution

2. Decimal Calculations

(1) Instructions for decimal calculations

To perform decimal calculations, set the decimal mode (D) flag to "1" with the SED instruction and execute the ADC or SBC instruction. In that case, after the ADC or SBC instruction, execute another instruction before the SEC, CLC, or CLD instruction.

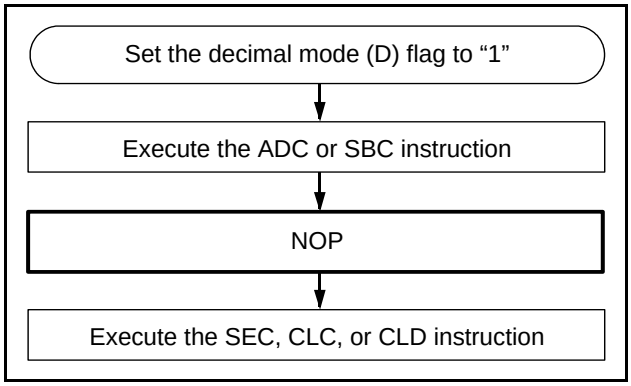


Fig. 101 Instructions for decimal calculations

(2) Status flag at decimal calculations

When the ADC or SBC instruction is executed in decimal mode (D flag = "1"), three of the status flags (N, V, and Z) are disabled. The carry (C) flag is set to "1" if a carry is generated and is cleared to "0" if a borrow is generated as a result of a calculation, so it can be used to determine whether the calculation has generated a carry or borrow.

Initialize the C flag before each calculation.

3. JMP Instruction

When using the JMP instruction (indirect addressing mode), do not specify the address where "FF16" is allocated to the low-order 8 bits as the operand.

4. Multiplication and Division Instructions

(1) The MUL and DIV instructions are not affected by the T and D flags.
(2) Executing these instructions does not change the contents of the processor status register.

5. Read-Modify-Write Instruction

Do not execute any read-modify-write instruction to the read invalid (address) SFR.
The read-modify-write instruction reads 1-byte of data from memory, modifies the data, and writes 1-byte the data to the original memory.
In the 740 Family, the read-modify-write instructions are the following:
(1) Bit handling instructions:
CLB, SEB
(2) Shift and rotate instructions:
ASL, LSR, ROL, ROR, RRF
(3) Add and subtract instructions:
DEC, INC
(4) Logical operation instructions (1's complement):
COM
Although not the read-modify-write instructions, add and subtract/logical operation instructions (ADC, SBC, AND, EOR, and ORA) when T flag = "1" operate in the way as the read-modify-write instruction. Do not execute them to the read invalid SFR.
<Reason>
When the read-modify-write instruction is executed to the read invalid SFR, the following may result:
As reading is invalid, the read value is undefined. The instruction modifies this undefined value and writes it back, so the written value will be indeterminate.

Notes on Peripheral Functions

Notes on I/O Ports

1. Use in Stand-By State

When using the MCU in stand-by state*1 for low-power consumption, do not leave the input level of an I/O port undefined. Be especially careful to the I/O ports for the N-channel open-drain.
In this case, pull-up (connect to Vcc) or pull-down (connect to Vss) these ports through a resistor.
When determining a resistance value, note the following:
- External circuit
- Variation in the output level during ordinary operation

When using a built-in pull-up resistor, note variations in current values:
- When setting as an input port: Fix the input level
- When setting as an output port: Prevent current from flowing out externally.

<Reason>
Even if a port is set to output by the direction register, when the content of the port latch is "1", the transistor becomes the OFF state, which allows the port to be in the high-impedance state. This may cause the level to be undefined depending on external circuits.
As described above, if the input level of an I/O port is left undefined, the power source current may flow because the potential applied to the input buffer in the MCU will be unstable.

*1 Stand-by state: Stop mode by executing the STP instruction
Wait mode by executing the WIT instruction

2. Modifying Output Data with Bit Handling Instruction

When the port latch of an I/O port is modified with the bit handling instruction*1, the value of an unspecified bit may change.
<Reason>
I/O ports can be set to input mode or output mode in byte units.
When the port register is read or written, the following will be operated:
- Port as input mode
  Read: Read the pin level
  Write: Write to the port latch
- Port as output mode
  Read: Read the port latch or peripheral function output (specifications vary depending on the port)
  Write: Write to the port latch (output the content of the port latch from the pin)

Meanwhile, the bit handling instructions are the read-modify-write instructions*2. Executing the bit handling instruction to the port register allows reading and writing a bit unspecified with the instruction at the same time.
If an unspecified bit is set to input mode, the pin level is read and the value is written to the port latch. At this time, if the original content of the port latch and the pin level do not match, the content of the port latch changes.
If an unspecified bit is set to output mode, the port latch is normally read, but the peripheral function output is read in some ports and the value is written to the port latch. At this time, if the original content of the port latch and the peripheral function output do not match, the content of the port latch changes.

*1 Bit handling instructions: CLB, SEB
*2 Read-modify-write instruction: Reads 1-byte of data from memory, modifies the data, and writes 1-byte of the data to the original memory.

3. Direction Registers

The values of the port direction registers cannot be read. This means, it is impossible to use the LDA instruction, memory operation instruction when the T flag is “1”, addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS. It is also impossible to use bit operation instructions such as CLB and SEB, and read-modify-write instructions to direction registers, including calculations such as ROR. To set the direction registers, use instructions such as LDM or STA.

4. Pull-Up Control

Only for the pin set to input mode, pull-up is controlled by the PULL register and the segment output disable register.

Notes on Termination of Unused Pins

1. Termination of Unused Pins

Perform the following at the shortest possible distance (20 mm or less) from the MCU pins.

(1) I/O ports

Set the ports to input mode and connect each pin to V_{CC} or V_{SS} through a resistor of 1 k to 10 kΩ. An internal pull-up resistor can also be used for the port where the internal pull-up resister is selectable.

To set the ports to output mode, leave open at “L” or “H” output.

- When setting the ports to output mode and leave open, input mode in the initial state remains until the mode of the ports are switched to output mode by a program after a reset. This may cause the voltage level of the pins to be undefined and the power source current to increase while the ports remains in input mode. For any effects on the system, careful system evaluations should be implemented on the user side.
- The direction registers may be changed due to a program runaway or noise, so reset the registers periodically by a program to increase the program reliability.

2. Termination Concerns

(1) When setting I/O ports to input mode

[1] Do not leave open

<Reason>

- The power source current may increase depending on the first-stage circuit.
- The ports are more likely affected by noise when compared with the termination shown on the above “1. (1) I/O ports”

[2] Do not connect to V_{CC} or V_{SS} directly

<Reason>

If the direction registers are changed to output mode due to a program runaway or noise, a short circuit may occur.

[3] Do not connect multiple ports in a lump to V_{CC} or V_{SS} through a resistor.

<Reason>

If the direction registers are changed to output mode due to a program runaway or noise, a short circuit may occur between the ports.

Notes on Interrupts

1. Changing Related Register Settings

If the interrupt occurrence synchronized with the following settings is not required, take the sequence shown below.

- When selecting the external interrupt active edge
- When selecting the interrupt source of the interrupt vector address where two or more interrupt sources are allocated

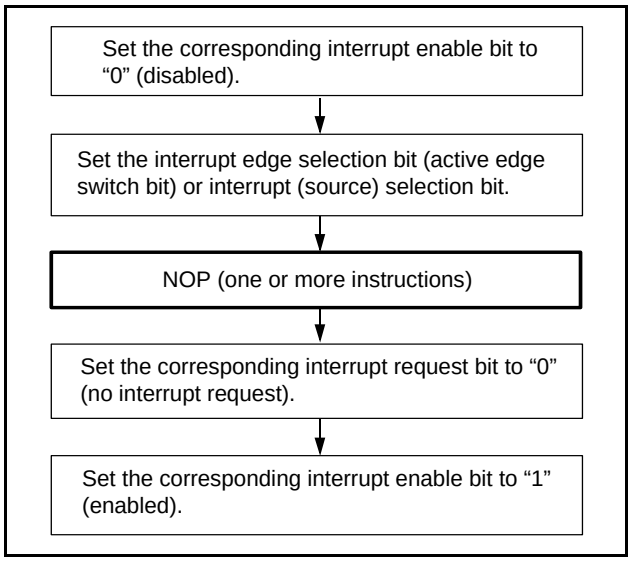


Fig. 102 Sequence for setting related register

<Reason>
In the following cases, the interrupt request bit of the corresponding interrupt may be set to "1".
<When switching the external interrupt active edge>

- INT_0 interrupt edge selection bit
  (bit 0 of interrupt edge selection register (address $003A_{16}$))
- INT_1 interrupt edge selection bit
  (bit 1 of interrupt edge selection register)
- INT_2 interrupt edge selection bit
  (bit 2 of interrupt edge selection register)
- $CNTR_0$ active edge switch bits
  (bits 6 and 7 of timer X control register 1 (address $002E_{16}$))
- $CNTR_1$ active edge switch bit
  (bits 6 of timer Y mode register (address 0038_{16}))

<When switching the interrupt source of the interrupt vector address where two or more interrupt sources are allocated>

- Timer Y/$CNTR_1$ interrupt switch bit
  (bit 3 of interrupt edge selection register)

<When switching the INT pin>

- INT_0 input port switch bit
  (bit 4 of interrupt edge selection register)
- INT_1 input port switch bit
  (bit 5 of interrupt edge select register)

2. Checking Interrupt Request Bit

To check the interrupt request bit with the BBC or BBS instruction immediately after this bit is set to "0", take the following sequence.
<Reason>
If the BBC or BBS instruction is executed immediately after the interrupt request bit is set to "0", the bit value before being set to "0" is read.

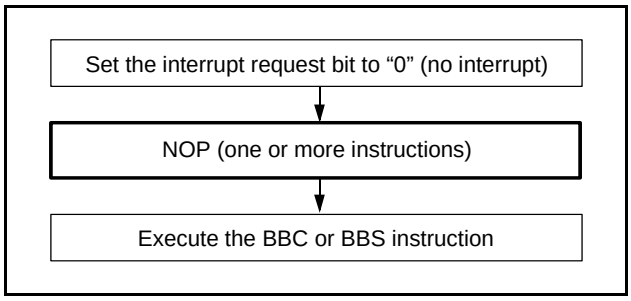


Fig. 103 Sequence for setting interrupt request bit

3. Setting Unused Interrupts

Set the interrupt enable bit of the unused interrupt to "0" (disabled).

Notes on Timers

1. Frequency Divider

All timers shares one circuit for the frequency divider to generate the count source.
Thus the frequency divider is not initialized when each individual timer is activated. When the frequency divider is selected as the count source, a one-cycle delay of the maximum count source will result between when the timer is activated and when it starts counting or outputs the waveform.
The count source cannot be observed externally.

2. Division Ratio for Timer 1 to 4

The division ratio is 1/(n+1) when the value n (0 to 255) is written to the timer latch.

3. Switching Frequency and Count Source for Timer 1 to 4, X, and Y

Switch the frequency division or count source* while the timer count is stopped.

*This also applies when the frequency divider output is selected as the timer count source and the count source is switched in conjunction with a transition between operating modes (on-chip oscillator mode, XIN mode, or low-speed mode). Be careful when changing settings in the CPU mode register.

4. Setting Timer 1 and 2 When STP Instruction Executed

Before executing the STP instruction, first set the wait time at return.

5. Setting Order to Timer 1 to 4

When switching the count source of timer 1 to timer 4, a narrow pulse may be generated at the count input, which causes the timer count value to be undefined. Also, if the timers are used in cascade connection, a narrow pulse may be generated at the output when writing to the pervious timer, which causes the next timer count value to be undefined.
Thus set the value from timer 1 in order after setting the count source of timer 1 to timer 4.

6. Write to Timer 2, 3, and 4

When writing to the latch only, if the write timing to the reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. At this time, count is stopped during write operation to the reload latch.

7. Timer 3 PWM_0 Mode, Timer 4 PWM_1 Mode

(1) When PWM output is suspended once it starts, the time to resume outputting may be delayed one section (256 × ts) of the short interval depending on the level of the output pulse at that time:
Stop at "H": No output delay
Stop at "L": Output is delayed time of 256 × ts

(2) When PWM mode is used, the interrupt requests and values of timer 3 and timer 4 are updated every cycle of the long interval (4 × 256 × ts).

8. Write Order to Timer X

(1) When timer mode, pulse output mode, event counter mode, or pulse width measurement mode is set, write to the following registers in the order below:
The timer X register (extension)
The timer X register (low-order)
The timer X register (high-order)
Writing to only one of these registers cannot be performed.
When either of the above modes is set and timer X operates as a 16-bit counter, if the timer X register (extension) is never set after a reset release, setting the timer X register (extension) is not required. In that case, write the timer X register (low-order) first and the timer X register (high-order) next. However, once the timer X register (extension) is written, note that the value is retained in the reload latch.

(2) Write to the timer X register by the 16-bit unit. Do not read the timer X register while write operation is performed. If the write operation is not completed, normal operation will not be performed.

(3) When IGBT output mode or PWM mode is set, do not write "1" to the timer X register (extension). If "1" has been already written to the timer X register, be sure to write "0" to the register before use.
Write to the following registers in the order below:
The compare registers 1, 2, 3 (high- and low-order)
The timer X register (extension)
The timer X register (low-order)
The timer X register (high-order)
The compare registers (high- and low-order) can be written in either order. However, be sure to write both the compare registers 1, 2, 3 and the timer X register at the same time.

9. Read Order to Timer X

(1) In all modes, read the following registers in the order below:
The timer X register (extension)
The timer X register (high-order)
The timer X register (low-order)
When reading the timer X register (extension) is not required, read the timer X register (high-order) first and the timer X register (low-order) next.
The read order to the compare registers 1, 2, 3 is not specified.

(2) Read the timer X register in 16-bit units. Do not write to it during read operation. If read operation is terminated in progress, normal operation will not be performed.

10. Write to Timer X

(1) Timer X can select either writing data to both the latch and the timer at the same time or writing data only by the timer X write control bit (b3) in the timer X mode register (address 002D16). When writing to the latch only, if a value is written to the timer X address, the value is set into the reload latch and the timer is updated at the next underflow. After a reset release, if a value is written to the timer X address, the value is set into the timer and the timer latch at the same time, because they are written simultaneously.
When writing to the latch only, if the write timing to the high-order reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. At this time, count is stopped during write operation to the high-order reload latch.

(2) Switch the frequency division or count source* while the timer count is stopped.

*This also applies when the frequency divider output is selected as the timer count source and the count source is switched in conjunction with a transition between operating modes (on-chip oscillator mode, XIN mode, or low-speed mode). Be careful when changing settings in the CPU mode register.

11. Setting Timer X Mode Register

When PWM mode or IGBT output mode is set, be sure to set the write control bit in the timer X mode register to "1" (writing to latch only). After writing to the timer X register (high-order), the contents of both registers are simultaneously reflected in the output waveform at the next underflow.

12. Timer X Output Control Functions

To use the output control functions (INT1 and INT2), set the levels of INT1 and INT2 to "H" for the falling edge active or to "L" for the rising edge active before switching to IGBT output mode.

13. CNTR0 Active Edge Selection

(1) Setting the CNTR0 active edge switch bits also affects the interrupt active edge at the same time.

(2) When the pulse width is measured, set bit 7 of the CNTR0 active edge switch bits to "0".

14. When Timer X Pulse Width Measurement Mode Used

When timer X pulse mode measurement mode is used, enable the event counter wind control data (bit 5 of timer X mode register (address 002D16)) by setting to "0".
<Reason>
If the event counter window control data (bit 5 of timer X mode register (address 002D16)) is set to "1" (disabled) to enable/disable the CNTR0 input, the input is not accepted after the timer 1 underflow.

15. CNTR1 Active Edge Selection

Setting the CNTR1 active edge switch bits also affects the interrupt active edge at the same time.
However, in pulse width HL continuous HL measurement mode, the CNTR1 interrupt request is generated at both rising and falling edges of the pin regardless of the settings of the CNTR1 active edge switch bits.

16. Read from/Write to Timer Y

(1) When reading from/writing to timer Y, read from/write to both the high-order and low-order bytes of timer Y. To read the value, read the high-order bytes first and the low-order bytes next. To write the value, write the low-order bytes first and the high-order bytes next.
Writing/reading should be preformed in 16-bit units. If write/read operation is changed in progress, normal operation will not be performed.

(2) Timer Y can select either writing data to both the latch and the timer at the same time or writing data only by the timer Y write control bit (b0) in the timer Y control register (address 003916). When writing to the latch only, if a value is written to the timer Y address, the value is set into the reload latch and the timer is updated at the next underflow. After a reset release, if a value is written to the timer Y address, the value is set into the timer and the timer latch at the same time, because they are written simultaneously.
When writing to the latch only, if the write timing to the high-order reload latch and the underflow timing are almost the same, the value is set into the timer and the timer latch at the same time. At this time, count is stopped during write operation to the high-order reload latch.

(3) Switch the frequency division or count source* while the timer count is stopped.

*This also applies when the frequency divider output is selected as the timer count source and the count source is switched in conjunction with a transition between operating modes (on-chip oscillator mode, XIN mode, or low-speed mode). Be careful when changing settings in the CPU mode register.

Notes on Serial I/O1

1. Write to Baud Rate Generator

Write to the baud rate generator while transmission/reception is stopped.

2. Setting Sequence When Serial I/O1 Transmit Interrupt Used

To use the serial I/O1 transmit interrupt, if the interrupt occurrence synchronized with settings is not required, take the following sequence:

(1) Set the serial I/O1 transmit interrupt enable bit (bit 2 of interrupt control register 2 (address 003F16)) to "0" (disabled).
(2) Set the transmit enable bit to "1".
(3) After one or more instructions have been executed, set the serial I/O1 transmit interrupt request bit (bit 2 of interrupt request register 2 (address 003D16)) to "0" (no interrupt).
(4) Set the serial I/O1 transmit interrupt enable bit to "1" (enabled).

<Reason>
When the transmit enable bit is set to "1", the transmit buffer empty flag (bit 0 of serial I/O1 status register) and the transmit shift completion flag are set to "1".
This allows an interrupt request to be generated regardless of which interrupt occurrence source has been selected by the transmit interrupt source selection bit (bit 3 of serial I/O1 control register) and the serial I/O1 transmit interrupt request bit is set to "1".

3. Data Transmission Control Using Transmit Shift Completion Flag

After transmit data is written to the transmit buffer register, the transmit shift completion flag (bit 2 of serial I/O1 status register (address 001916)) changes from "1" to "0" after a delay of 0.5 to 1.5 cycles of the system clock. Thus, after transmit data is written to the transmit buffer register, note this delay when controlling data transmission by referencing the transmit shift completion flag.

4. Setting Serial I/O1 Control Register

Before setting the serial I/O1 control register again, first set both the transmit enable bit and the receive enable bit to "0" and initialize the transmission and reception circuits.

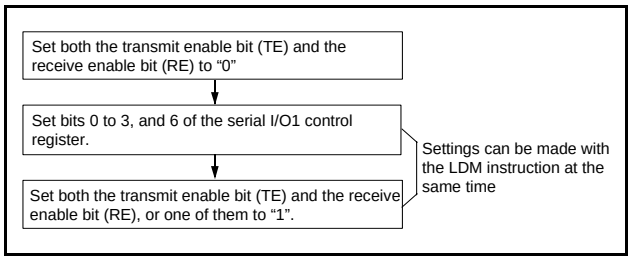


Fig. 104 Sequence of setting serial I/O1 control register

5. Pin Status After Transmission Completed

After transmission is completed, the TxD pin retains the level when transmission is completed.
When the internal clock is selected in clock synchronous serial I/O mode, the SCLK1 pin is set to "H".

6. Serial I/O1 Enable Bit during Transmit Operation

During transmission, if the serial I/O1 enable bit (bit 7 of serial I/O1 control register (address 001A16)) is set to "0", the pin function is set to an I/O port and the internal transmit operation continues even though transmit data is not output externally. Also, if the transmit buffer register is written in this state, transmit operation starts internally. If the serial I/O1 enable bit is set to "1" at this time, transmit data is output to the TxD pin from that point.

7. Transmission Control When External Clock Selected

During data transmission, if the external clock is selected as the synchronous clock, set the transmit enable bit to "1" while SCLK1 is set to "H". Also, write to the transmit buffer register while SCLK1 is set to "H".

8. Receive Operation in Clock Synchronous Serial I/O Mode

During reception in clock synchronous serial I/O mode, set both the transmit enable bit and the receive enable bit to "1". Then write dummy data to the transmit buffer register. When the internal clock is selected as the synchronous clock, the synchronous clock is output at this point and receive operation starts. When the external clock is selected, reception is enabled at this point and inputting the external clock starts transmit operation.
The P41/TxD pin outputs dummy data written in the transmit buffer register.

9. Transmit/Receive Operation in Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, set the transmit enable bit and the receive enable bit to "0" simultaneously to stop transmit/receive operations. If only one of the operations is stopped, transmission and reception cannot be synchronized, which will cause a bit error.

Notes on Serial I/O2

1. Switching Synchronous Clock

If the synchronous clock is switched by the serial I/O2 synchronous clock selection bit (bit 6 of serial I/O2 control register (address 001D16)), initialize the serial I/O2 counter (writing to serial I/O2 register (address 001F16)).

2. Notes When External Clock Selected

When the external clock is selected as the synchronous clock, the SOUT2 pin retains the D7 level after transfer is completed.
However, if the synchronous clock is continuously input, the serial I/O2 register continues shifting and the SOUT2 pin keeps outputting transmit data.
Also, write to the serial I/O2 register while SCLK2 is set to "H".
When the internal clock is selected as the synchronous clock, the SOUT2 pin is placed in the high-impedance state after transfer is completed.

Notes on A/D Conversion

1. Analog Input Pin

Set the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01 μF to 1 μF.
In addition, operations of application products should be verified thoroughly on the user side.
<Reason>
An analog input pin has a built-in capacitor for analog voltage comparison. Thus if a signal from the high impedance signal source is input to the analog input pin, charge and discharge noise will be generated. This may cause the A/D conversion/comparison accuracy to drop.

2. Clock Frequency during A/D Conversion

The comparator input consists of a capacity coupling. If the conversion rate is too low, the A/D conversion accuracy may deteriorate due to a charge lost, so set f(XIN) 500 kHz or more for A/D conversion in XIN mode. Also, do not execute the STP or WIT instruction during A/D conversion.
In low-speed mode (when on-chip oscillator is selected), as A/D conversion is performed using the internal on-chip oscillator, there is no limit on the minimum frequency for f(XIN).

3. ADKEY Function

When the ADKEY enable bit is set to “1”, the analog input pin selection bits are disabled. Do not execute the A/D conversion by a program while ADKEY is enabled. Enabling ADKEY does not change bits 0 to 2 of ADCON.

4. A/D Conversion Immediately After ADKEY Function Started

In the ADKEY function, A/D conversion is not performed to the analog input voltage immediately after starting the function. This causes the A/D conversion result immediately after starting the function to be undefined. If the A/D conversion result of the analog input voltage applied to the ADKEY pin is required, select the analog input pin corresponding to ADKEY before performing A/D conversion.

5. Input Voltage Applied to ADKEY Pin

Set the input to the ADKEY pin into a steep falling waveform and stabilize the input voltage within eight cycles (1 μs when f(XIN) = 8 MHz) from the moment the input voltage reaches VIL or lower.
The actual threshold voltage for the ADKEY pin is between VIH and VIL.
To prevent unnecessary ADKEY operation due to noise or other factors, set the ADKEY pin voltage to VIH (0.9 VCC) or more while the input is waited.

6. Register Operation during A/D Conversion

The A/D conversion operation is not guaranteed if the following are preformed:

- The CPU mode register is operated during A/D conversion operation
- The AD control register is operated during A/D conversion operation
- The STP or WIT instruction is executed during A/D conversion operation

7. A/D Converter Power Source Pin

Connect to the A/D converter power source pin to AVSS or VSS whether the A/D conversion function is used or not.
<Reason>
If the AVSS pin is left open, the MCU may operate incorrectly because the pin will be affected by noise or other factors.

Notes on LCD Drive Control Circuit

1. Multiplier Circuit

When the multiplier circuit is used, set the multiplier circuit control bit to "1" (multiplier circuit enabled) after applying a voltage from 1.3 V or more to 2.1 V or less to the V_{L1} pin.
When the multiplier circuit is not used, set the V_{L3} connection bit to "1" (open) and apply an appropriate voltage to the LCD power source input pins (V_{L1} to V_{L3}). When the V_{L3} connection bit is set open, the V_{L3} pin is placed in the high impedance state.
When the multiplier circuit is used, set the LCDCK frequency to 100 Hz or more. The on-chip oscillator cannot be used as LCDCK.
In a system where the multiplier circuit is used (a multiplier capacitor is externally connected between the C_1 and C_2 pins), set the multiplier circuit control bit to "1" (multiplier circuit enabled) before executing the STP or WIT instruction.

2. Setting Data to LCD Display RAM

To write data to the LCD display RAM when the LCD enable bit is set to "1" and while LCD is turned on, set fixed data. Rewriting with temporary data may cause LCD to flicker. The following shows a processing example to write data to the LCD display RAM while LCD is turned on.

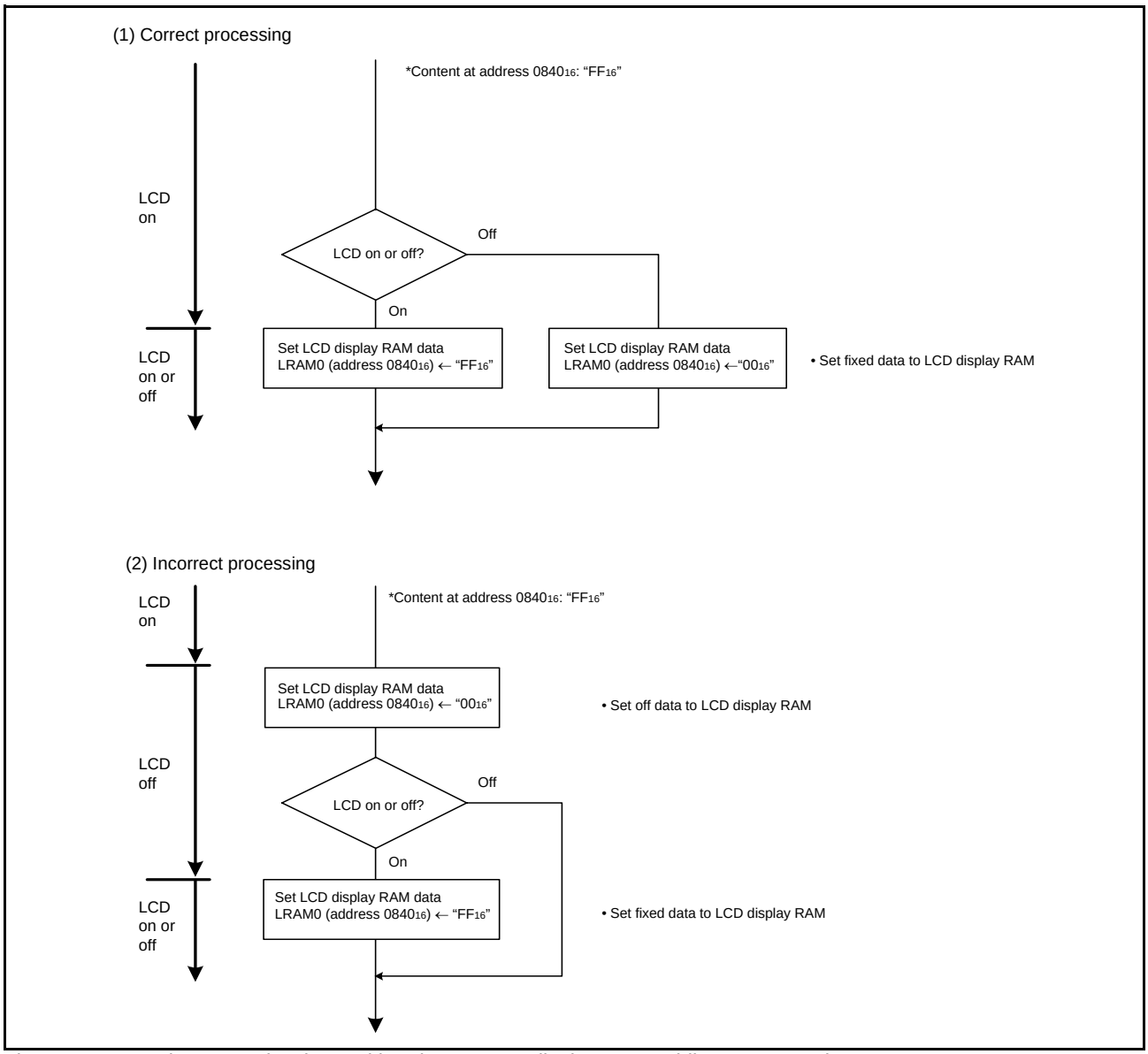


Fig. 105 Processing example when writing data to LCD display RAM While LCD Turned On

3. Executing STP Instruction

Executing the STP instruction sets the LCD enable bit (bit 4 of LCD mode register1 (address 0013_{16})) to "0" and the LCD panel turns off. To turn the LCD panel on after returning from stop mode, set the LCD enable bit to "1".

4. V_{L3} Pin

To use the LCD drive control circuit while V_{L3} is set to the voltage equal to V_{CC}, apply the V_{CC} voltage to the V_{L3} pin and write "1" to the V_{L3} connection bit (bit 1 of LCD mode register 2 (address 0014_{16})).

5. LCD Drive Power Supply

Power supply capacitor may be insufficient with the division resistance for LCD power supply, and the characteristic of the LCD panel. In this case, there is the method of connecting the bypass capacitor about 0.1 -0.33μF to VL1 -VL3 pins. The example of a strengthening measure of the LCD drive power supply is shown below.

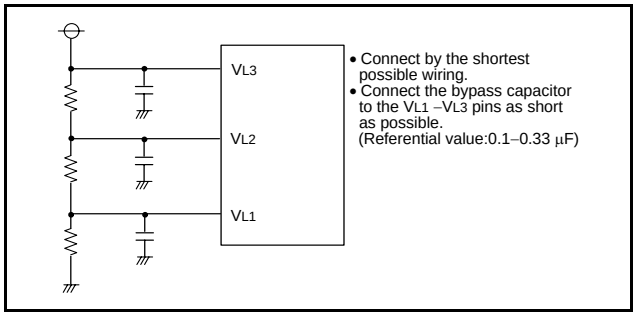


Fig. 106 Strengthening measure example of LCD drive power supply

Notes on ROM Correction Function

1. Returning to Main Program

To return to the main program from the correction program, use the JMP instruction (3-byte instruction).

2. Using ROM Correction Function

If the ROM correction function is used, be sure to enable the ROM correction enable bit after setting the ROM correction register.

3. Address

Do not set addresses other than the ROM area in the ROM correction address registers. Also, do not set the same address in the ROM correction address 1 register and the ROM correction address 2 register.

4. ROM Correction Process

Include the ROM correction process in the program beforehand.

5. Using No ROM Correction Function

If the ROM correction function is not used, the ROM correction vector can be used as normal RAM/ROM. When using as normal RAM/ROM, be sure to set bits 1 and 0 of the ROM correction enable register to "0" (disabled).

Notes on Clock Generating Circuit

1. Oscillation Circuit Constants

The oscillation circuit constants vary depending on the resonator. Use values recommended by the oscillator manufacturer.
A feed-back resistor is implemented between the X_{IN} and X_{OUT} pins (an external feed-back resistor may be required depending on conditions). As no feed-back resistor is implemented between X_{CIN} and X_{COUT}, add a feedback resistor of about 10 MΩ.

2. Transition between Modes

When the MCU transits between on-chip oscillator mode, X_{IN} mode, or low-speed mode, both the X_{IN} and X_{CIN} oscillations must be stabilized. Be especially careful when turning the power on and returning from stop mode. Refer to the clock state transition diagram for a transition between each mode. Also, set the frequency in the condition that $f(X_{IN}) \geq 3 \times (X_{CIN})$.
When X_{IN} mode is not used (the X_{IN}-X_{OUT} oscillation or external clock input to X_{IN} is not performed), connect X_{IN} to V_{CC} through a resistor.

3. Oscillation Stabilization

Before executing the STP instruction, set the values * to generate the wait time required for oscillation stabilization to timer 1 latch and timer 2 latch (low-order 8 bits of timer 1 and high-order 8 bits of timer 2).

*Referential values
(Set values according to your oscillator and system)
- OSCSEL = "L" in the flash memory and QzROM versions: ..... 0005_{16} or more
- OSCSEL = "H" in the QzROM version: ..... $01FF_{16}$ or more

4. Low-Speed Mode, X_{IN} Mode

To use low-speed mode or X_{IN} mode, wait until oscillation stabilizes after enabling the X_{IN}-X_{OUT} and X_{CIN}-X_{COUT} oscillation, then switch to the mode.

Notes on Flash Memory Mode

• CPU Rewrite Mode

(1) Operating Speed

During CPU rewrite mode, set the system clock ϕ to 4.0 MHz or less using the main clock division ratio selection bits (bits 6 and 7 of address $003B_{16}$).

(2) Prohibited Instructions

During CPU rewrite mode, the instructions which reference data in the flash memory cannot be used.

(3) Interrupts

During CPU rewrite mode, interrupts cannot be used because they reference data in the flash memory.

(4) Watchdog Timer

If the watchdog timer has been running already, the internal reset by underflow will not occur because the watchdog timer is continuously cleared during program or erase operation.

(5) Reset

Reset is always valid. If CNV_{SS} = "H" when a reset is released, boot mode is active. The program starts from the address stored in addresses $FFFC_{16}$ and $FFFD_{16}$ in boot ROM area.

Notes on Watchdog Timer

1. Watchdog Timer Underflow

The watchdog timer does not operate in stop mode, but it continues counting during the wait time to release the stop state and in wait mode. Write to the watchdog timer control register so that the watchdog timer will not underflow during these periods.

2. Stopping On-Chip Oscillator Oscillation

When the on-chip oscillator is selected by the watchdog timer count source selection bit 2, the on-chip oscillator forcibly oscillates and it cannot be stopped. Also, in this time, set the STP instruction function selection bit to "1" at this time.
Select "0" (ϕSOURCE) for the watchdog timer count source selection bit 2 at the system which on-chip oscillator is stopped.

3. Watchdog Timer Control Register

Bits 7 to 5 can be rewritten only once after a reset. After writing, rewriting is disabled because they are locked. These bits are set to "0" after a reset.

Notes on Differences between Flash Memory Version and QzROM Version

The flash memory and QzROM versions differ in their manufacturing processes, built-in ROM, memory size, and layout patterns. Because of these differences, characteristic values, operation margins, noise immunity, and noise radiation and oscillation circuit constants may vary within the specified range of electrical characteristics.
When switching to the QzROM version, implement system evaluations equivalent to those performed in the flash memory version.
Confirm page 11 about the differences of functions.

Notes on Power Source Voltage

When the power supply voltage value of the MCU is less than the value indicated in the recommended operating conditions, the MCU may not operate normally and perform unstable operation.
In a system where the power source voltage drops slowly when the power source voltage drops or the power is turned off, reset the MCU when the power source voltage is less than the recommended operating conditions, and design the system so that this unstable operation does not cause errors to it.

Notes on Handling Power Source Pins

Before using the MCU, connect a capacitor suitable for high frequencies as a bypass capacitor between the following:
The power source pin (V_{CC} pin) and the GND pin (V_{SS} pin)
The power source pin (V_{CC} pin) and the analog power source input pin (AV_{SS} pin). As a bypass capacitor, a ceramic capacitor of 0.01 μF to 0.1 μF is recommended.
Also, use the shortest possible wiring to connect a bypass capacitor between the power source pin and the GND pin and between the power source pin and the analog power source pin.

Notes on Memory

1. RAM

The RAM content is undefined at a reset. Be sure to set the initial value before use.

Notes on QzROM Version

Wiring to OSCSEL pin

(1) OSCSEL = L

Connect the OSCSEL pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer. In addition connecting an approximately 5 kΩ resistor in series to the GND could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer.

(2) OSCSEL = H

Connect the OSCSEL pin the shortest possible to the VCC pattern which is supplied to the VCC pin of the microcomputer. In addition connecting an approximately 5 kΩ resistor in series to the VCC could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the VCC pattern which is supplied to the VCC pin of the microcomputer.

<Reason>

The OSCSEL pin is the power source input pin for the built-in QzROM.

When programming in the QzROM, the impedance of the OSCSEL pin is low to allow the electric current for writing to flow into the built-in QzROM. Because of this, noise can enter easily. If noise enters the OSCSEL pin, abnormal instruction codes or data are read from the QzROM, which may cause a program runaway.

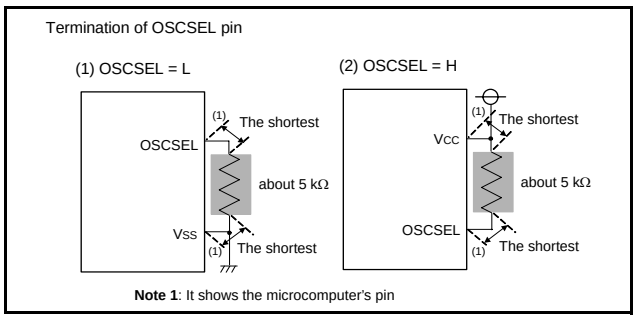


Fig. 107 Wiring for OSCSEL pin

Overvoltage in QzROM Version

Make sure that voltage exceeding the VCC pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in figure below does not occur for pin OSCSEL pin (VPP power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.

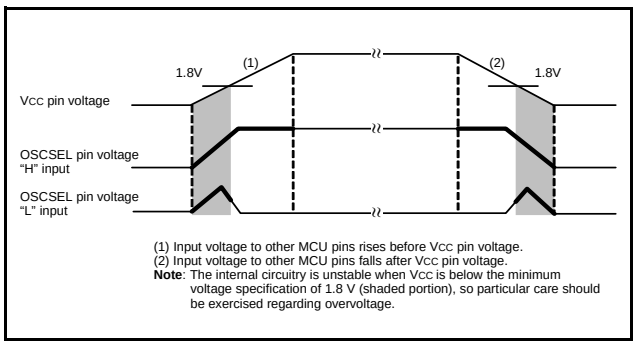


Fig. 108 Timing Diagram (Bold-lined periods are applicable)

QzROM Version Product Shipped in Blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approximate 0.1% may occur.

Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

Ordering QzROM Writing

1. Notes On QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .msk) which is made by the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "00$_{16}$", "FE$_{16}$" and "FF$_{16}$" can not be accepted.
- Set "FF$_{16}$" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF$_{16}$" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

2. Data Required for QzROM Ordering

The following are necessary when ordering a QzROM product shipped after writing:

- QzROM Writing Confirmation Form*
- Mark Specification Form*
- ROM data: Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).

Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

3. QzROM Product Receiving Procedure

When writing to QzROM is performed by user side, the receiving inspection by the following flow is necessary.

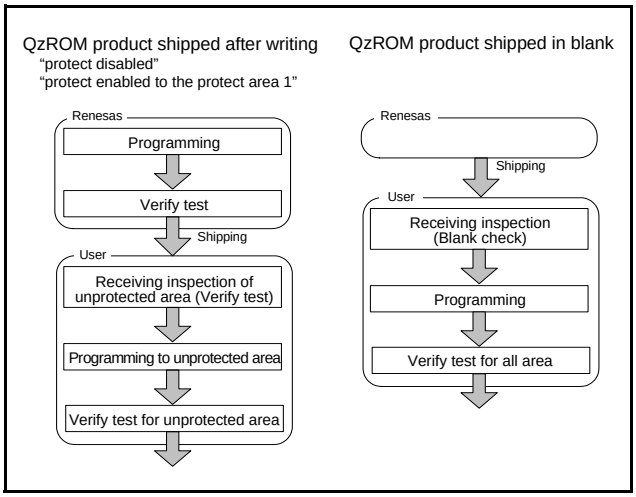


Fig. 109 QzROM receiving procedure

Notes on Flash Memory Version

CPU Rewrite Mode

1. Operating Speed

During CPU rewrite mode, set the system clock ϕ 4.0 MHz or less using the main clock division ratio selection bits (bits 6 and 7 of address 003B16).

2. Prohibited Instructions

The instructions which refer to the internal data of the flash memory cannot be used during the CPU rewrite mode.

3. Interrupts

The interrupts cannot be used during the CPU rewrite mode because they refer to the internal data of the flash memory.

4. Watchdog Timer

In case of the watchdog timer has been running already, the internal reset generated by watchdog timer underflow does not happen, because of watchdog timer is always clearing during program or erase operation.

5. Reset

Reset is always valid. In case of CNVSS = "H" when reset is released, boot mode is active. So the program starts from the address contained in address FFFC16 and FFFD16 in boot ROM area.

CNVss Pin

The CNVSS pin determines the flash memory mode.
Connect the CNVSS pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer.
In addition connecting an approximately 5 kΩ resistor in series to the GND could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer.

Note. When the boot mode or the standard serial I/O mode is used, a switch of the input level to the CNVSS pin is required.

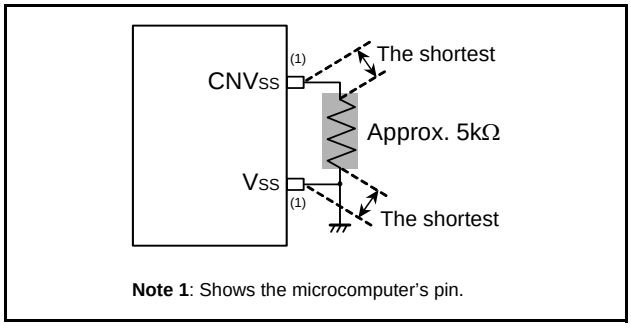


Fig. 110 Wiring for CNVSS pin

REVISION HISTORY	38D5 Group Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Aug 12, 2005	–	First edition issued
2.00	Jan 23, 2006	–	Pin name revised: CNVss → OSCSEL
		–	Frequency name revised: ROSC → OCO
		–	Mode name revised: Middle-, High-speed mode → Frequency/2, 4, 8 mode
		–	Bit names of some registers: 1. ROSC stop bit → On-chip oscillator stop bit 2. STP instruction disable bit → STP instruction function selection bit 3. Vector 1 enable bit (RC0) → ROM correction address 1 enable bit (RC0) 4. Vector 2 enable bit (RC1) → ROM correction address 2 enable bit (RC1) 5. Vector control bit (RC2) → ROM correction memory selection bit (RC2)
		1	Description, Power source voltage and Power dissipation revised.
		6	Table 2 Pin description (1): Some description of Port P1 Function revised.
		7	Table 3 Pin description (2): Description of OSCSEL added. Fig. 5 Memory expansion plan, Table 4 Support products M38D59GFFP/HP, M38D59GCFP/HP added.
		13	Some description revised. Fig. 8 Structure of CPU mode register: Note on on-chip oscillator added. Fig. 9 Switch procedure of CPU mode register: Initial values of CPUM2 added and initial value of CPUM revised.
		14	Fig. 10 Memory map diagram: Reserved ROM area $FFD4_{16}$ to $FFDC_{16}$ → $FFD0_{16}$ to $FFDC_{16}$ Note on ROM correction vector added.
		15	Fig. 11 Memory map of special function register (SFR): “Reserved area” is added to address $0FFD_{16}$, and Note added.
		22	Table 8 Termination of unused pins: X_{IN} and X_{OUT} pin termination added.
		52	ROM CORRECTION FUNCTION: Description and some bit names revised and Fig. 47 Memory map of M38D58 added.
		53	Initial Value of Watchdog Timer: Some description added. Standard Operation of Watchdog Timer: Some description eliminated. Bit 6 of Watchdog Timer Control Register added. Note 2 revised. Fig. 50 Structure of Watchdog timer control register: Name of bit 6 and description of its function revised.
		55	Fig. 55 Reset sequence revised.
		57	Fig. 56 Internal state at reset: ROM correction address 1 (low-order), ROM correction address 2 (high-order) and ROM correction address 2 (low-order) revised.
		58	Oscillation Control (1) Stop Mode: Some description revised.
		59	Fig. 58 Clock generating circuit block diagram: “or ROSC clock division ratio selection bit” eliminated.
		60	Fig. 60 State transitions of system clock on-chip oscillator mode: f(OCO) → f(OCO)/32, Note 8 to Note 10 revised and Note 12 added.
		61-65	QzROM programming mode (Overview, Pin description, Pin connection diagram, Connection example) added.
		68	(6) Wiring to OSCSEL pin revised.
		69	QzROM Receive Flow added.

REVISION HISTORY	38D5 Group Data Sheet

Rev.	Date	Description	
		Page	Summary
2.00	Jan 23, 2006	71	Table 14 Recommended operating conditions - Vcc (Power source voltage) and Note revised. - V_{IH}, V_{IL} ($\overline{RESET}$) revised.
		73	Table 16 Recommended operating conditions: all revised, Power source voltage graph added.
		74	Table 17 Electrical characteristics: ROSC → f(OCO)
		75	Table 18 Electrical characteristics: Icc revised. Table 19 A/D converter recommended operating condition revised.
		76	Table 20 A/D converter characteristics: test conditions revised. AD Power source voltage graph added.
		77	Table 21 Timing requirements 1: $t_c(X_{IN})$, $t_{wH}(X_{IN})$, $t_{wL}(X_{IN})$ revised and Note added.
		81	PACKAGE OUTLINE revised.
2.01	Mar 24, 2006	1	FEATURES: Power source voltage revised.
		4	Performance overview: Oscillation frequency and Power source voltage revised.
		17	Table 7 Related SFRs of port P7 revised.
		52	Fig. 46: Address revised.
		53	Fig. 50: Note 1 revised.
		58	(1)Stop mode: Description revised.
		59	Fig. 59 ϕ_{SOURCE} added.
		60	Fig. 60 State transitions of system clock: Note 3 revised.
		71	Table 14 : Vcc (Power source voltage) and Note 3 revised.
		73	Table 16: Power source voltage (Main clock X_{IN} frequency) graph added.
		76	Table 20 Description of f(OCO) and Note revised.
2.02	Jul 10, 2006	15	Fig. 11: Register names of ROM correction addresses 1 and 2 revised.
		22	Termination of unused pins I/O ports : Description added.
		23	Table 8 • Termination 1 (recommended) : Delete (recommended). • Termination 1 to 3 of $P7_0/C_1/INT_{01}$ and $P7_1/C_2/INT_{11}$: revised.
		29	X_{CIN} is selected as Timer 1, 2 count source : sentence is revised.
		32	X_{CIN} is selected as Timer X count source : sentence is revised.
		33	Fig. 26: (TXCON1 bit 5 = “1”)→(TXCON1 bit 5 = “0”)
		35	X_{CIN} is selected as Timer Y count source : sentence is revised.
		43	Fig. 38: ϕ_{SOURCE} clock added.
		52	Fig. 47: Border line in ROM area : revised.
		53	Fig. 49: On chip oscillator → On chip oscillator/4 Fig. 50: b5 and b7 revised.
		58	Frequency Control : Description added.
		61	Table 12: Function of V_{REF} and AV_{SS} revised.
		64 to 67	Fig. 63 to Fig. 66: Revised and added.
		76	Table 17: Parameter of I_{IH} and I_{IC} added.
2.03	Aug 31, 2006	4	Table 1: Main clock and Sub-clock generating circuit : “feedback resistor” eliminated.
		7	Table 3: AV_{SS} : GND → Analog power source
		23	Table 8: $P4_1$/TxD : input port → output port $P4_2/S_{CLK1}$: output port → input port

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Rev.	Date	Description	
		Page	Summary
2.03	Aug 31, 2006	75	Table 16: Max. of f(ϕ) : 2 × V_{CC} – 4 → 4
		76	Table 17: Test condition of V_{T+} – V_{T-} : V_{CC} = 2.0 V on $\overline{RESET}$ → V_{CC} = 2.0 V to 5.5 V on $\overline{RESET}$
2.04	Feb 02, 2007	13, 60	Table 24 Limits of t_{WH} (S_{CLK2}), t_{WL} (S_{CLK2}): t_c (S_{CLK1})/2–80 → t_c (S_{CLK2})/2–80
		14	MEMORY ROM: Description revised. ROM Code Protect Address: Description revised and added. Fig. 10: Reserved ROM area: FFD0$_{16}$ → FFDB$_{16}$
		15	Fig.8 and Fig.60: CPUM2 (bits 2 to 7) revised.
		16	• Direction Resisters: Description revised. Fig.11: ROM correction enable register → ROM correction enable register(RCR)
		23	Table 8: Terminations 1 and 2 of V_{L3} revised.
		25	• Fig.13: PULL3 (bits 4 to 7), SEG2 (bits 4 to 7) revised.
		31	Fig.19: INTEDGE(bit 6), ICON2(bit 7) revised.
		34	Fig.25: revised.
		35	Fig. 28: Note added and revised.
		36	Fig. 27: TXCON(BITS 3,4) revised.
		41	Fig. 36: Note added.
		43	• Fig.29: TYM(bits 2,3) revised. • [AD control Register], Fig.39:
		43, 44	Fig. 38: Note added.
		46	analog input selection bit → analog input pin selection bits
		51	Fig. 45: 1/3 duty revised.
		52	ROM CORRECTION FUNCTION: Description added. Fig. 47: FFD0$_{16}$ → FFDB$_{16}$.
		53	Fig. 49: Note added and revised.
		54	Fig.40: LM2(bits 1 to 7) revised. Fig.51: CKOUT(bits 2 to 7) revised.
		59	Fig. 59: Note 3 added and circuit expression is revised.
		61	Table 12: ESDA input → ESDA input/output
		64 to 66	Fig. 63 to Fig. 66: Revised.
		71	Precautions Regarding Overvoltage: Description revised and Fig. 73 added.
		72	Table 13 • V_{CC}: Oscillation start voltage → When start oscillating • V_I: OSCSEL added. • V_O: Conditions added.
		73	Table 14 • V_{IL}: OSCSEL added. • Note 3 revised.
		75	Table 16: Note 4 revised.
		78	Table 20 • T_{CONV} Limits: (Note) → (Notes 1, 2) • Note 2 revised.
		80	Note: ...set f(X_{IN}) ≤ 500 kHz → ≥ 500 kHz Table 22 tsu (R_XD-S_{CLK2}) → t_{su} (S_{IN2}-S_{CLK2})

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Rev.	Date	Description	
		Page	Summary
2.04	Feb 02, 2007	81	t_h (S_{CLK2}-RxD) → t_h (S_{CLK2}-S_{IN2}) Table 23 Limits of t_{wH} (S_{CLK2}), t_{wL} (S_{CLK2}): t_c (S_{CLK1})/2–30 → t_c (S_{CLK2})/2–30
3.01	Aug 08, 2007	–	38D5 Group (Flash Memory Version For Development) Datasheet (No. REJ03B0197) is merged.
		1	Flash memory version contents: added DESCRIPTION: Description added Memory size (QzROM version): 640 bytes → 1536 bytes Power dissipation (Flash memory version): revised
		2	Fig. 1: Flash memory version: “M38D59FFFP” added, Notes: added
		3	Fig. 2: Flash memory version: “M38D59FFHP” added, Notes: added
		4	Table 1: Flash memory version contents: added and separates to Table 2 (Next page) Memory size (QzROM version); 640 bytes → 1536 bytes I/O port; 32 pins → 36 pins
		7	Table 3: I/O port P3, I/O port P4: revised
		8	Table 4: OSCSEL → CNV_{SS}/function: revised
		9	Fig.4 “Memory type”: Flash memory version added
		10	Memory Type: deleted Memory size (QzROM version): 640 bytes → 1536 bytes Fig. 5: Under development products → mass-produced Table 5: Flash memory version products added
		11	Table 6, Notes on Differences between QzROM and Flash Memory Versions: added
		12	Central Processing Unit: revised
		15	Fig. 8: Flash memory version contents: added Notes: revised
		16	Fig. 9: Flash memory version contents: added Low/X_{IN} mode? → Low-speed/X_{IN} mode?
		17	Memory: Flash memory version contents: added • ROM is revised • ROM code Protect Address in QzROM version is revised Fig. 10: revised
		18	Fig. 11: revised
		19	Fig. 13: Do not write “1” → Not used (do not write “1”)
		23	Fig. 16 (14) Port $P6_0$: Revised port Xc switch bit input to low-active
		27 to 31	INTERRUPTS: revised
		28	• Interrupt Source Selection: interrupt source selection register → interrupt edge selection register • External Interrupt Pin Selection: INT_0, INT_1 interrupt switch bit → INT_0, INT_1 input port switch bit
		29	Fig. 19: Do not write “1” → Not used (do not write “1”)
		31	<Notes>: Related registers → Related bits, and its explain is revised
		34	Fig. 25: Figure title is revised $P7_2$ clock output control bit block is revised
		35	• Frequency Divided For Timer: revised <Notes on Timer 1 to Timer 4>: (2)Writing to Timer 2, Timer 3, Timer 4 → (2)Write Timer 2, Timer 3, Timer4
		37	Fig. 28: Figure title is revised Timer X output 1 edge switch bit → Timer X output 1 active edge switch bit

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3.01	Aug 08, 2007	37	Fig. 28: Timer X output 2 edge switch bit → Timer X output 2 active edge switch bit
		38	• Frequency Divided For Timer: revised timer X1 output edge switch bit → timer X output 1 active edge switch bit timer X2 output edge switch bit → timer X output 2 active edge switch bit (6) Pulse Width Measurement Mode: revised
		39	(1) Write Order to Timer X: description added (2) Read Order to Timer X: revised (3) Write to Timer X: revised
		40	(7) When Timer X Pulse Width Measurement Mode Used: added Fig. 30: Timer X output 1 edge switch bit → Timer X output 1 active edge switch bit
		41	• Timer Y: revised (5) Real Time Port Control: moved from <Notes on Timer Y>
		42	• Real Time Port Control: moved to "• Timer Y"
		47	• Serial I/O2: revised Fig. 39: Serial I/O counter 2 → Serial I/O2 counter Serial I/O shift register 2 → Serial I/O2 register
		48	[Serial I/O2 Operation]: added Fig. 40: revised
		49	[Comparator and Control Circuit]: revised
		50	ADKEY function: moved from the next page.
		51	Fig. 43: Added the note number to each register Do not write "1" → Not used (do not write "1")
		53	• Voltage Multiplier: revised • Bias Control and Applied Voltage to LCD Power Input Pins: evised Fig. 45: revised title is revised
		56	<Notes>: added
		57	Fig. 50: revised
		58	• Initial Value of Watchdog Timer: revised <Notes>: revised Fig. 52: Watchdog timer selection bit 2 → Watchdog timer count source selection bit 2 Fig. 53: revised
		59	Title "[RRF register] RRFR": added
		60	RESET CIRCUIT: description added Fig. 57, Fig. 58: revised
		61	Fig. 59: (18) RRF register (RRFR) → (18) RRF register Notes revised
		62	CLOCK GENERATING CIRCUIT, and • Frequency Control: Description added
		64	• Oscillation Control: Description added
		65	Fig. 63: revised
		66	Table 15: Function of V_{CC}, V_{SS} pins: 1.8 to 5.5 → 2.7 to 5.5
		69, 70	Fig. 66 and 67: revised
		73 to 91	FLASH MEMORY MODE: added
		92	NOTES ON PROGRAMMING is merged to NOTES ON USE
		93	NOTES ON QzROM VERSION is separated
		94	NOTES ON FLASH MEMORY VERSION and NOTES ON DEFFAERENCES BETWEEN QzROM VERSION AND FLASH MEMORY VERSION are added

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3.01	Aug 08, 2007	97, 108	Table 22 and 35: V_I of OCESEL are added V_O of COM_0-COM_3 are added V_O of ports and SEG_{32}-SEG_{35} are revised
		98-106	Table 23 to 34: V_{SS}=0V is added to test conditions
		98	Table 24: V_{IH} of $\overline{RESET}$ is revised
		101	Table 27: V_{CC} test conditions are revised
		103	Table 30: At 10bitAD: 2.2V < V_{CC} ≤ 4.0V → 2.2V ≤ V_{CC} ≤ 4.0V 1.8V < V_{CC} ≤ 5.5V → 2.0V ≤ V_{CC} ≤ 5.5V At 8bitAD: 2.0V < V_{CC} ≤ 2.2V → 2.0V ≤ V_{CC} ≤ 2.2V 1.8V < V_{CC} ≤ 5.5V → 2.0V ≤ V_{CC} ≤ 5.5V
		104, 115	Table 31 and 45: Each main clock input condition (V_{CC}) are revised.
		105	Table 32: 2.0V ≤ V_{CC} ≤ 4.0V → 2.0V ≤ V_{CC} < 4.0V V_{CC} ≤ 2.0V → V_{CC} < 2.0V Note 1 is added
		108	Table 35: CNV_{SS} is added Storage temperature is revised
		112	Table 40: Limits value of I_{IL} are revised
		113	Table 41: All limits value are revised
		113, 114	Table 41, 42, and 43: V_{SS}=0V is added to test conditions
		114	Table 43: 2.7V < V_{CC} ≤ 4.0V → 2.7V ≤ V_{CC} ≤ 4.0V 2.7V ≤ V_{CC} ≤ 5.5V and test conditions of f(OCO)/8 and f(OCO)/32 are added
		115	Table 44 are added Table 45: “Main clock input “L” pulse width” is added Note 1 is revised
		120-133	Appendix: added
3.02	Sep 11, 2007	10	Table 5: Latest revised date of products list
		17	Fig. 10: Brancket indicates the ROM area is modified
		53	Fig. 45: VL1 external capacitor → external power supply
		98	Marge the “Recommended operating conditions (1)” table and “Recommended operating conditions (2)”
		109	Marge the “Recommended operating conditions (1)” table and “Recommended operating conditions (2)”
		125	2nd item of “8. Write Order to Timer X” is added
		126	2nd item of “10. Write to Timer X” is deleted
3.03	Oct 02 2007	40	“(7) When Timer X Pulse Width Measurement Mode Used” is revised
		64	Fig. 62 is revised
		65	Fig. 63 is revised
		76	Fig. 73 is revised Table 17 is revised
3.04	May 20 2008	4	Table 1: LCD drive control circuit; Duty “Static” added
		17	<Notes>: added
		19	Fig. 11: $0FFE_{16}$, $0FFF_{16}$; “Reserved” added
		20	• Direction Registers (Ports P0-P6, $P7_2$-$P7_4$) “Depending on the pin, ... may be read.” is deleted

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3.04	May 20 2008	21”	Table 9: “$P4_5/S_{IN2}/(KW_1)$” → “$P4_5/S_{OUT2}/(KW_1)$” “$P4_2/S_{CLK2}/(KW_2)$” → “$P4_6/S_{CLK2}/(KW_2)$” “$P4_3/\overline{S_{RDY2}}/(KW_3)$” → “$P4_7/\overline{S_{RDY2}}/(KW_3)$”
		22	Fig. 14 is revised
		27	Table 10: “$P2_0/SEG_0$-$P2_7/SEG_7$” → “$P2_0/SEG_0/(KW_4)$-$P2_7/SEG_7$”
		68	Fig. 64: “$P2_0/SEG_0(KW_4)$” → “$P2_0/SEG_0/(KW_4)$” “$P2_1/SEG_1(KW_5)$” → “$P2_1/SEG_1/(KW_5)$” “$P2_2/SEG_2(KW_6)$” → “$P2_2/SEG_2/(KW_6)$” “$P2_3/SEG_3(KW_7)$” → “$P2_3/SEG_3/(KW_7)$”
		69	Fig. 65: “$P2_2/SEG_2(KW_6)$” → “$P2_2/SEG_2/(KW_6)$” “$P2_3/SEG_3(KW_7)$” → “$P2_3/SEG_3/(KW_7)$” “$P5_6/AN_{10}$” → “$P5_6/AN_6$”
		77	Fig. 73 is revised
		89	Fig. 81: “$P5_6/AN_{10}$” → “$P5_6/AN_6$”
		94, 133	Notes On QzROM Writing Orders is revised

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