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Renesas Electronics Corporation

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3850 Group (Spec.A QzROM version)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0125-0213

Rev.2.13

Apr 17, 2009

DESCRIPTION

The 3850 group (spec.A QzROM version) is the 8-bit microcomputer based on the 740 family core technology.

The 3850 group (spec.A QzROM version) is designed for the household products and office automation equipment and includes serial interface functions, 8-bit timer, and A/D converter.

FEATURES

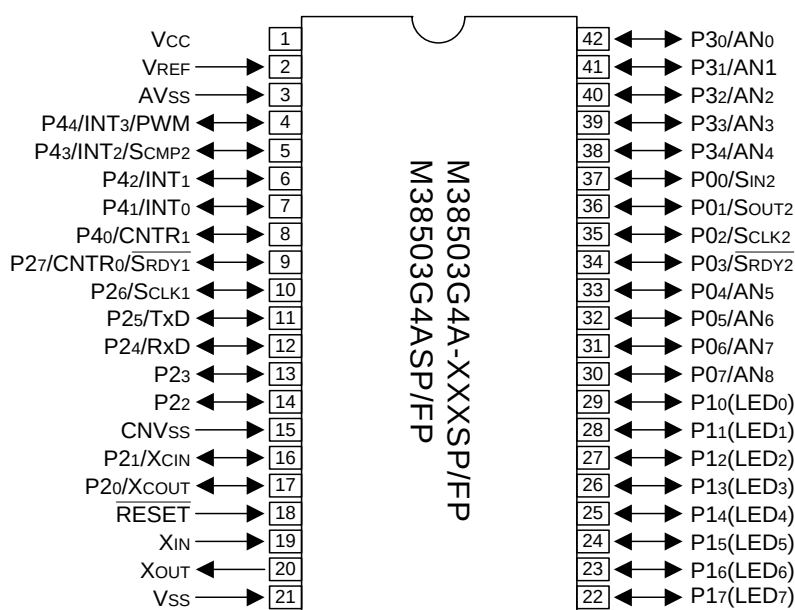
- Basic machine-language instructions 71
- Minimum instruction execution time 0.32 μ s
(at 12.5 MHz oscillation frequency)
- Memory size
 - ROM 16 K bytes
 - RAM 512 bytes
- Programmable input/output ports 34
- On-chip software pull-up resistor Built-in
- Interrupts 15 sources, 14 vectors
- Timers 8-bit $\times$ 4
- Serial interface
 - Serial I/O1 8-bit $\times$ 1 (UART or Clock-synchronized)
 - Serial I/O2 8-bit $\times$ 1 (Clock-synchronized)
- PWM 8-bit $\times$ 1
- A/D converter 10-bit $\times$ 9 channels
- Watchdog timer 16-bit $\times$ 1

- Clock generating circuit Built-in 2 circuits
(connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
 - [In high-speed mode]
 - $f(XIN) \leq 12.5$ MHz 4.0 to 5.5 V
 - $f(XIN) \leq 6.0$ MHz 2.7 to 5.5 V
 - $f(XIN) \leq 4.2$ MHz 2.2 to 5.5 V
 - $f(XIN) \leq 2.1$ MHz 2.0 to 5.5 V
 - [In middle-speed mode]
 - $f(XIN) \leq 12.5$ MHz 2.7 to 5.5 V
 - $f(XIN) \leq 8.4$ MHz 2.2 to 5.5 V
 - $f(XIN) \leq 4.2$ MHz 1.8 to 5.5 V
 - [In low-speed mode]
 - $f(XCIN) \leq 50$ kHz 1.8 to 5.5 V
- Power dissipation
 - In high-speed mode 30 mW (typ.)
(at 12.5 MHz oscillation frequency, at 5 V power source voltage)
 - In low-speed mode 45 μ W (typ.)
(at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range -20 to 85 $^{\circ}$ C

APPLICATION

Household products, Consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : SP PRDP0042BA-A (42P4B) (42-pin shrink plastic-molded SDIP)
Package type : FP PRSP0042GA-A/B (42P2R-A/E) (42-pin plastic-molded SSOP).

Fig 1. Pin configuration

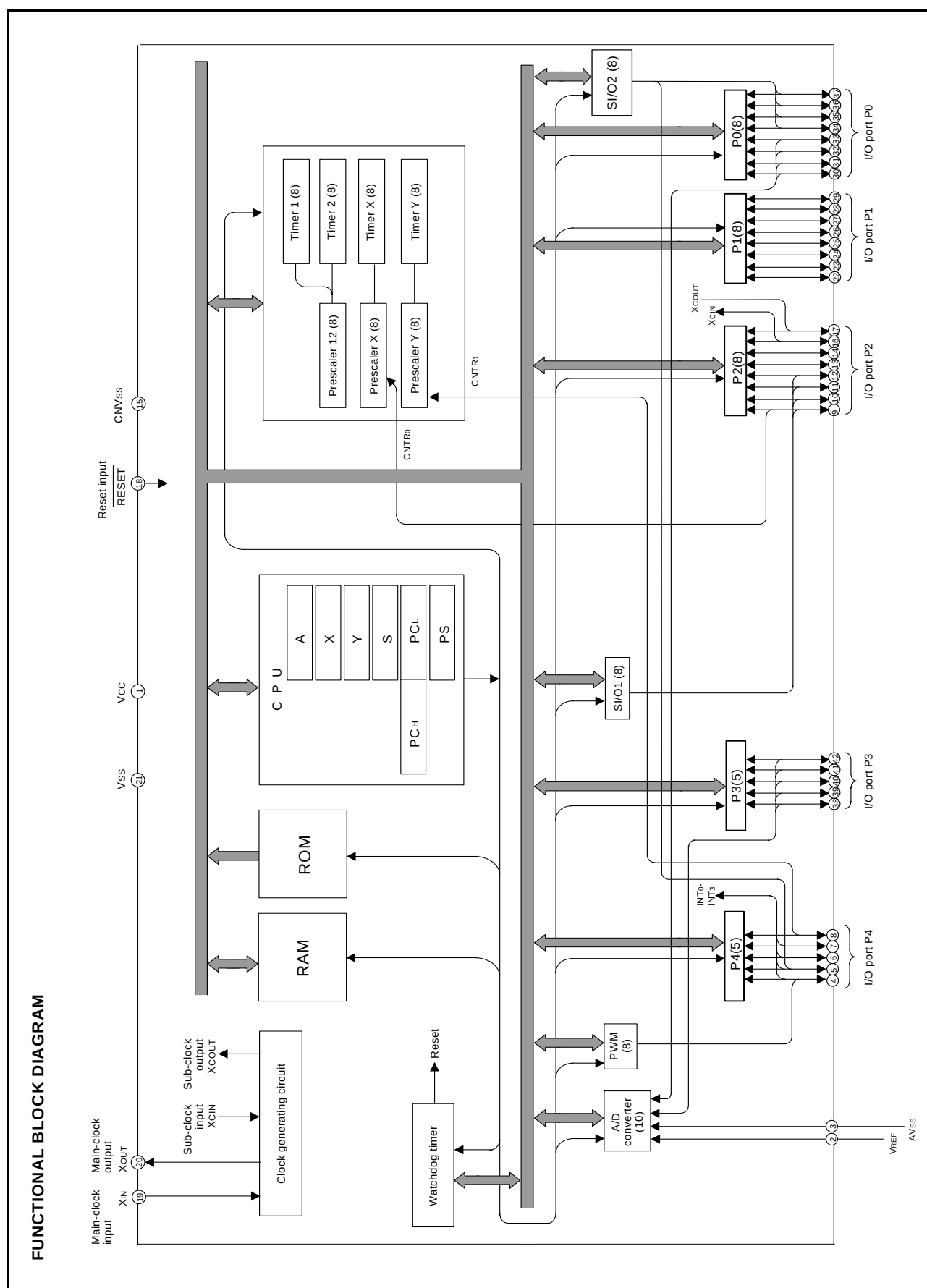


Fig 2. Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	
			Function except a port function
Vcc, Vss	Power source	Apply voltage of 1.8 V–5.5 V to Vcc, and 0 V to Vss.	
CNVss	CNVss input	- This pin controls the operation mode of the chip and is shared with the VPP pin which is the power source input pin for programming the built-in QzROM. - Normally connected to Vss.	
VREF	Reference voltage	Reference voltage input pin for A/D converter.	
AVss	Analog power source	- Analog power source input pin for A/D converter. - Connect to Vss.	
RESET	Reset input	Reset input pin for active "L".	
XIN	Clock input	- Input and output pins for the clock generating circuit. - Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. - When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
XOUT	Clock output		
P00/SIN2 P01/SOUT2 P02/SCLK2 P03/SRDY2	I/O port P0	8-bit CMOS I/O port. - I/O direction register allows each pin to be individually programmed as either input or output. - CMOS compatible input level. - CMOS 3-state output structure. - Pull-up control is enabled in a byte unit.	Serial I/O2 function pin
P04/AN5–P07/AN8			A/D converter input pin
P10–P17	I/O port P1	P10 to P17 (8 bits) are enabled to output large current for LED drive.	
P20/XCOUT P21/XCIN	I/O port P2	8-bit CMOS I/O port. - I/O direction register allows each pin to be individually programmed as either input or output. - CMOS compatible input level. - P20, P21, P24, to P27: CMOS3-state output structure. - P22, P23: N-channel open-drain structure. - Pull-up control of P20, P21, P24–P27 is enabled in a byte unit.	Sub-clock generating circuit I/O pins (connect a resonator)
P22 P23			
P24/RxD P25/TxD P26/SCLK1			Serial I/O1 function pin
P27/CNTR0/SRDY1			Serial I/O1 function pin Timer X function pin
P30/AN0–P34/AN4	I/O port P3	5-bit CMOS I/O port with the same function as port P0. - CMOS compatible input level. - CMOS 3-state output structure. - Pull-up control is enabled in a bit unit.	A/D converter input pin
P40/CNTR1	I/O port P4	5-bit CMOS I/O port with the same function as port P0. - CMOS compatible input level. - CMOS 3-state output structure. - Pull-up control is enabled in a bit unit.	Timer Y function pin
P41/INT0 P42/INT1			Interrupt input pins
P43/INT2/SCMP2			Interrupt input pin SCMP2 output pin
P44/INT3/PWM			Interrupt input pin PWM output pin

PART NUMBERING

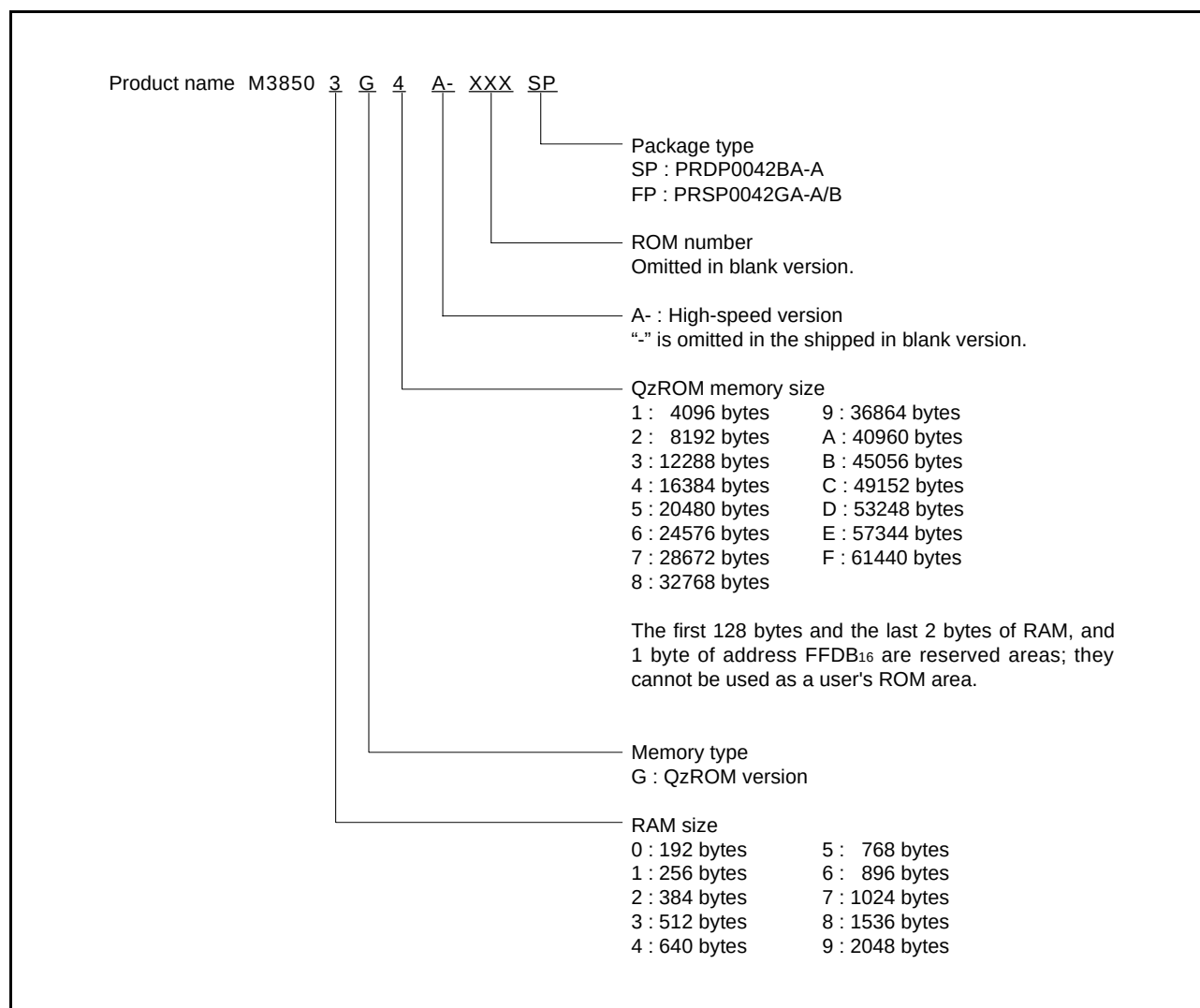


Fig 3. Part numbering

GROUP EXPANSION

Renesas Technology expands the 3850 group (spec.A QzROM version) as follows.

Memory Type

Support for QzROM version.

Memory Size

- ROM size 16 K bytes
- RAM size 512 bytes

Packages

- PRDP0042BA-A 42-pin shrink plastic-molded SDIP
- PRSP0042GA-A/B 42-pin plastic-molded SSOP

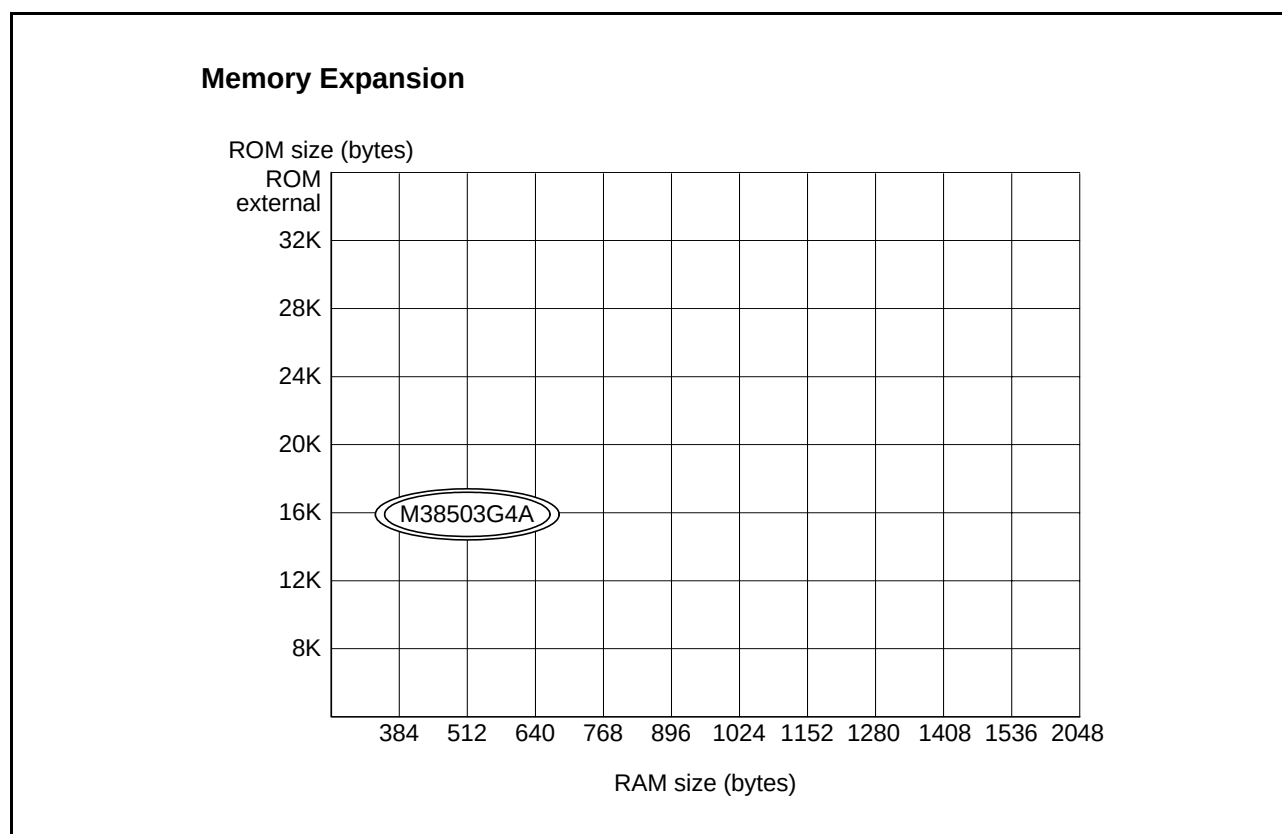


Fig 4. Memory expansion

Table 2 Support products (spec.A QzROM version)

Product name	ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38503G4A-XXXSP	16384 (16253)	512	PRDP0042BA-A	QzROM version (Programmed shipment) ⁽¹⁾
M38503G4A-XXXFP			PRSP0042GA-A/B	
M38503G4ASP	16384 (16253)	512	PRDP0042BA-A	QzROM version (blank) ⁽¹⁾
M38503G4AFP			PRSP0042GA-A/B	

NOTES:

1. This means a shipment of which User ROM has been programmed.
The user ROM area of a blank product is blank.

GROUP DESCRIPTION

The QzROM version, mask ROM version and the flash memory version of 3850 group (Spec.A) are mass production. Currently support products are listed below.

Table 3 Support products (mask ROM version and flash memory version of Spec.A)

Product name	ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38503M2A-XXXSP	8192 (8062)	512	PRDP0042BA-A	Mask ROM version
M38503M2A-XXXFP			PRSP0042GA-A/B	
M38503M4A-XXXSP	16384 (16254)	512	PRDP0042BA-A	
M38503M4A-XXXFP			PRSP0042GA-A/B	
M38504M6A-XXXSP	24576 (24446)	640	PRDP0042BA-A	
M38504M6A-XXXFP			PRSP0042GA-A/B	
M38507M8A-XXXSP	32768 (32635)	1024	PRDP0042BA-A	Flash memory version
M38507M8A-XXXFP			PRSP0042GA-A/B	
M38507F8ASP	32768	1024	PRDP0042BA-A	
M38507F8AFP			PRSP0042GA-A/B	

Table 4 Differences among 3850 group (standard), 3850 group (spec.H), and 3850 group (spec.A)

		3850 group (standard) ⁽¹⁾	3850 group (spec.H) ⁽¹⁾	3850 group (spec.A)	
				Mask ROM version Flash memory version	QzROM version
Serial interface		1: Serial I/O (UART1 or Clock-synchronized)	2: Serial I/O1 (UART1 or Clock-synchronized) Serial I/O2 (Clock-synchronized)	2: Serial I/O1 (UART1 or Clock-synchronized) Serial I/O2 (Clock-synchronized)	
A/D converter		Unserviceable in low-speed mode Analog input: 5 channels	Serviceable in low-speed mode Analog input: 5 channels	Serviceable in low-speed mode Analog input: 9 channels	
LED port		5: P13–P17	8: P10–P17	8: P10–P17	
Software pull-up resistor		Not available	Not available	Built-in (Port P0–P4)	
Absolute maximum ratings	Power source voltage	–0.3 to 7.0 V	–0.3 to 6.5 V	–0.3 to 6.5 V	
	CNV _{SS} input voltage	–0.3 to 13.0 V	–0.3 to V _{CC} + 0.3 V	–0.3 to V _{CC} + 0.3 V	–0.3 to 8.0 V
Maximum operating frequency ⁽²⁾		8.0 MHz	8.0 MHz	12.5 MHz	
Minimum operating power source voltage ⁽²⁾		2.7 V	2.7 V	2.7 V	1.8 V

NOTES:

- We are currently not receiving an new order for the standard version and Spec.H. We are currently receiving an new order for Spec.A.
- For detail of the absolute maximum ratings, the electrical characteristics, and the recommended operating conditions, refer to each datasheet.

Notes on differences among 3850 group (standard), 3850 group (spec.H), and 3850 group (spec.A)

- The absolute maximum ratings of 3850 group (spec.A) is smaller than that of 3850 group (standard).
 - Power source voltage V_{CC} = –0.3 to 6.5 V
 - CNV_{SS} input voltage V_I = –0.3 to V_{CC} + 0.3 V (QzROM: 8.0V)
- The oscillation circuit constants of X_{IN}-X_{OUT}, X_{CIN}-X_{COUT} may be some differences among 3850 group (standard), 3850 group (spec.H), and 3850 group (spec.A).

- Do not write any data to the reserved area and the reserved bit. (Do not change the contents after reset.)
- Fix bit 3 of the CPU mode register to “1”.
- Be sure to perform the termination of unused pins.

FUNCTIONAL DESCRIPTION

CENTRAL PROCESSING UNIT (CPU)

The 3850 group (spec.A) uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is "0", the high-order 8 bits becomes "0016". If the stack page selection bit is "1", the high-order 8 bits becomes "0116".

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.

Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls (see Table 5).

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

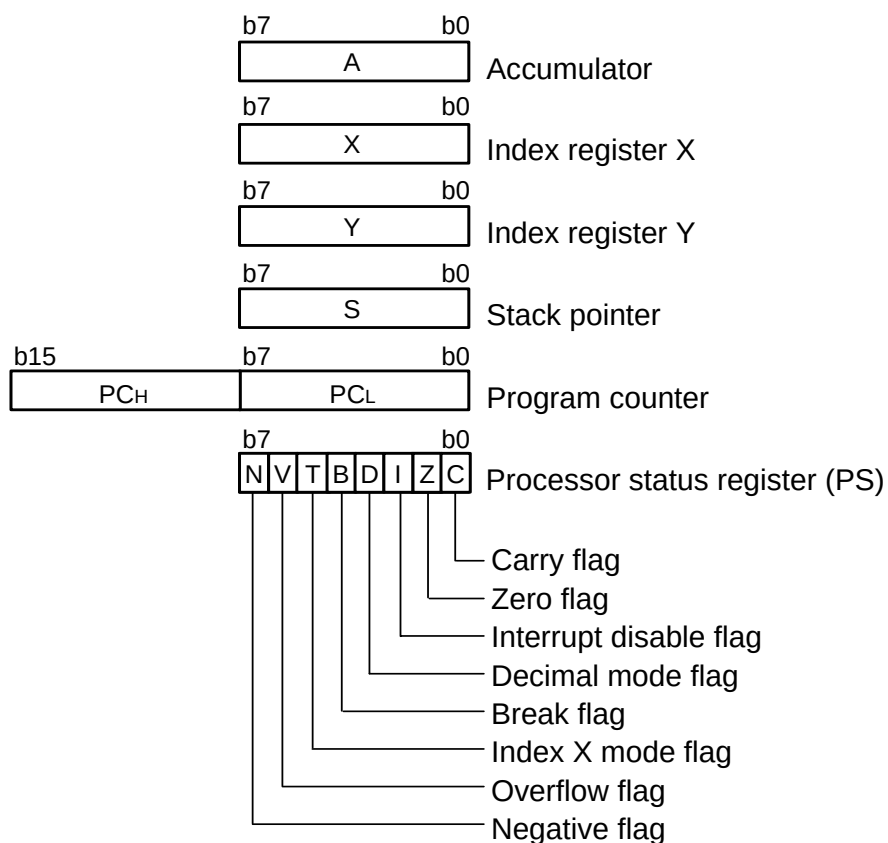


Fig 5. 740 Family CPU register structure

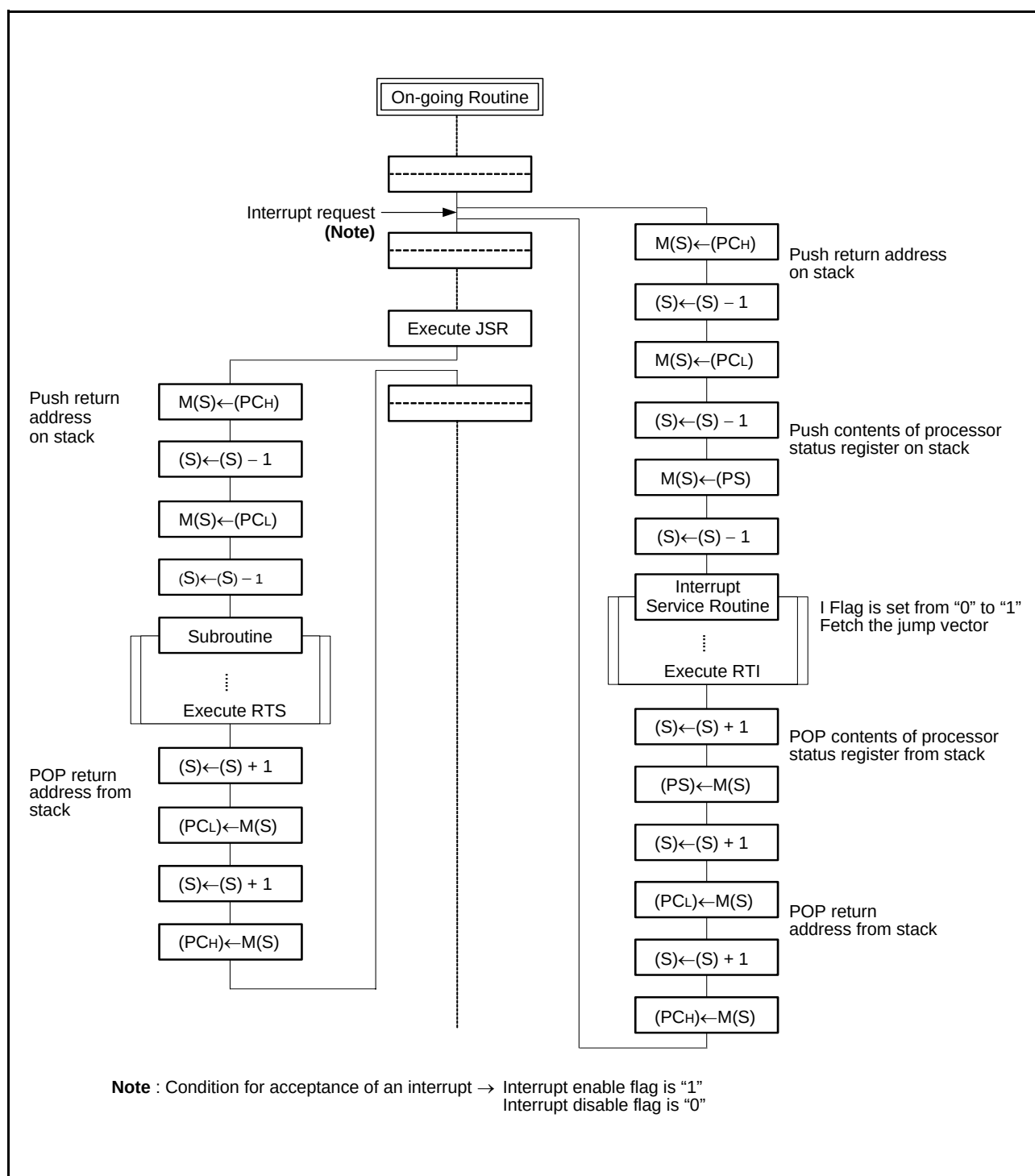


Fig 6. Register push and pop at interrupt generation and subroutine call

Table 5 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction. Interrupts are disabled when the I flag is "1".

Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".
Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1".

Bit 5: Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.

Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 6 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B₁₆

The CPU mode register contains the stack page selection bit, the internal system clock control bits, etc.

The CPU mode register is allocated at address 003B₁₆.

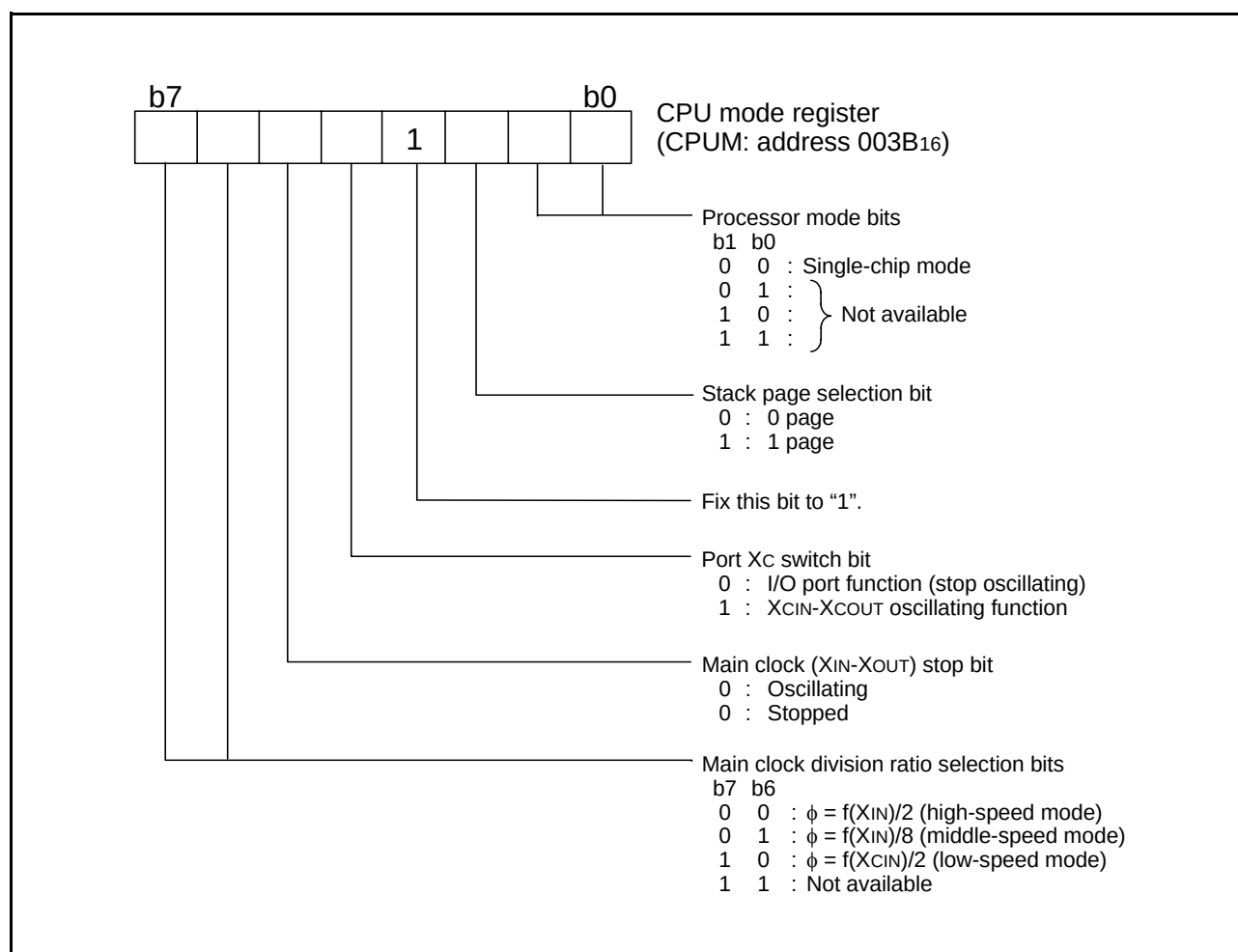


Fig 7. Structure of CPU mode register

MEMORY**• Special Function Register (SFR) Area**

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

• RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

• ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

In the QzROM version, 1 byte of address FFDB₁₆ is also a reserved area.

• Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

• Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

• Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

• ROM Code Protect Address (address FFDB₁₆)

Address FFDB₁₆, which is the reserved ROM area of QzROM, is the ROM code protect address. "00₁₆" is written into this address when selecting the protect bit write by using a serial programmer or selecting protect enabled for writing shipment by Renesas Technology corp.. When "00₁₆" is set to the ROM code protect address, the protect function is enabled, so that reading or writing from/to QzROM is disabled by a serial programmer.

As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.

As for the QzROM product shipped after writing, "00₁₆" (protect enabled) or "FF₁₆" (protect disabled) is written into the ROM code protect address when Renesas Technology corp. performs writing.

The writing of "00₁₆" or "FF₁₆" can be selected as ROM option setup ("MASK option" written in the mask file converter) when ordering.

<Notes>

Since the contents of RAM are undefined at reset, be sure to set an initial value before use.

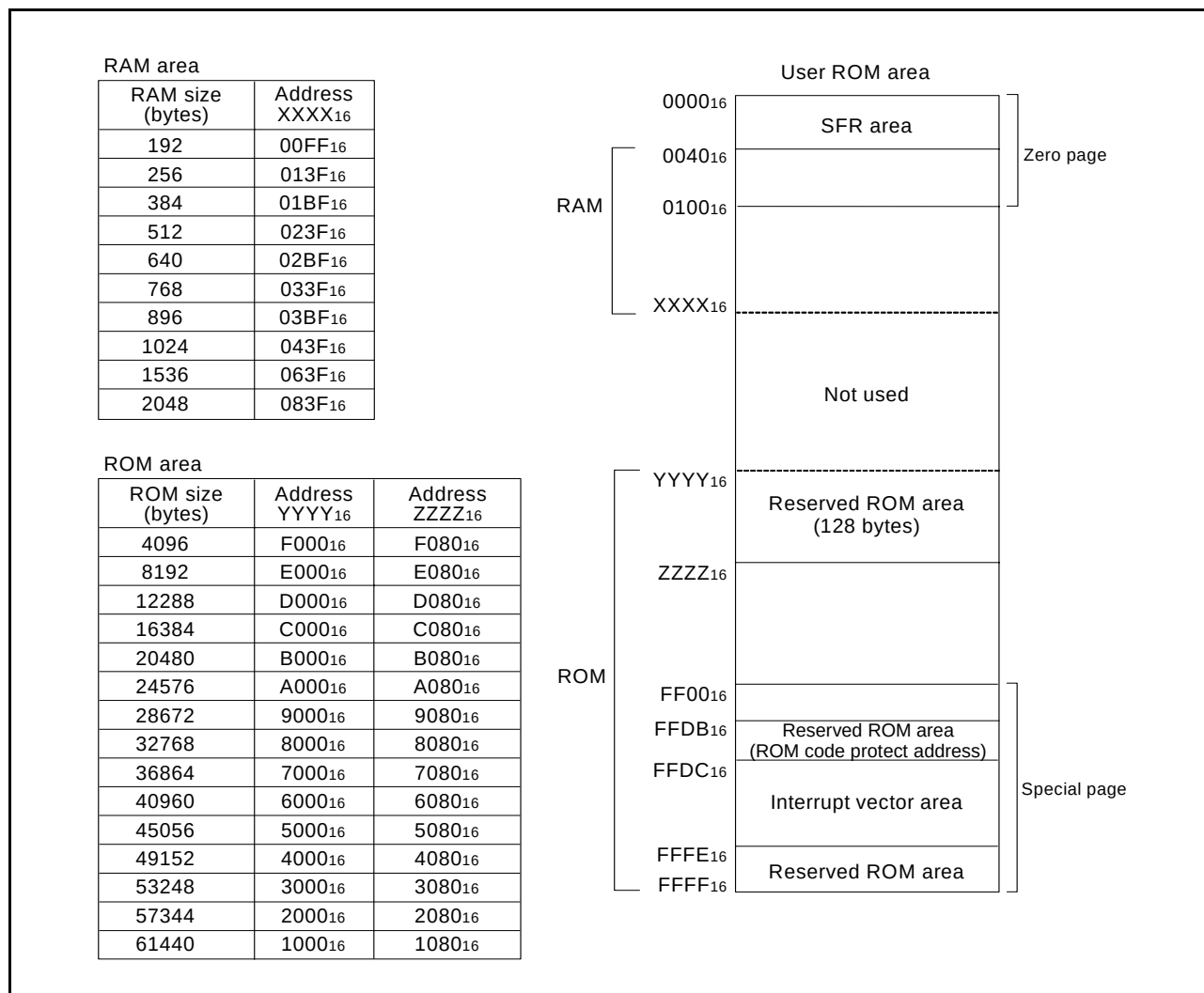


Fig 8. Memory map diagram

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Prescaler 12 (PRE12)
0001 ₁₆	Port P0 direction register (P0D)	0021 ₁₆	Timer 1 (T1)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer 2 (T2)
0003 ₁₆	Port P1 direction register (P1D)	0023 ₁₆	Timer XY mode register (TM)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Prescaler X (PREX)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer X (TX)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	Prescaler Y (PREY)
0007 ₁₆	Port P3 direction register (P3D)	0027 ₁₆	Timer Y (TY)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Timer count source selection register (TCSS)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	
000A ₁₆		002A ₁₆	
000B ₁₆		002B ₁₆	Reserved *
000C ₁₆		002C ₁₆	Reserved *
000D ₁₆		002D ₁₆	Reserved *
000E ₁₆		002E ₁₆	Reserved *
000F ₁₆		002F ₁₆	Reserved *
0010 ₁₆		0030 ₁₆	Reserved *
0011 ₁₆		0031 ₁₆	Reserved *
0012 ₁₆	Port P0, P1, P2 pull-up control register (PULL012)	0032 ₁₆	
0013 ₁₆	Port P3 pull-up control register (PULL3)	0033 ₁₆	
0014 ₁₆	Port P4 pull-up control register (PULL4)	0034 ₁₆	AD control register (ADCON)
0015 ₁₆	Serial I/O2 control register 1 (SIO2CON1)	0035 ₁₆	AD conversion low-order register (ADL)
0016 ₁₆	Serial I/O2 control register 2 (SIO2CON2)	0036 ₁₆	AD conversion high-order register (ADH)
0017 ₁₆	Serial I/O2 register (SIO2)	0037 ₁₆	AD input selection register (ADSEL)
0018 ₁₆	Transmit/Receive buffer register (TB/RB)	0038 ₁₆	MISRG
0019 ₁₆	Serial I/O1 status register (SIOSTS)	0039 ₁₆	Watchdog timer control register (WDTCON)
001A ₁₆	Serial I/O1 control register (SIOCON)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	UART control register (UARTCON)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Baud rate generator (BRG)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆	PWM control register (PWMCON)	003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆	PWM prescaler (PREPWM)	003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆	PWM register (PWM)	003F ₁₆	Interrupt control register 2 (ICON2)
		00FE ₁₆	Reserved *

* Reserved : Do not write any data to this addresses, because these areas are reserved.

Fig 9. Memory map of special function register (SFR)

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

By setting the port P0, P1, P2 pull-up control register (address 001216), the port P3 pull-up control register (address 001316), or the port P4 pull-up control register (address 001416), ports can control pull-up with a program. However, the contents of these registers do not affect ports programmed as the output ports.

Table 7 I/O port function

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
P00/SIN2 P01/SOUT2 P02/SCLK2 P03/SRDY2	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O	Serial I/O2 control register	(1) (2) (3) (4)
P04/AN5– P07/AN8				A/D converter input	AD control register AD input selection register	(13)
P10–P17	Port P1					(5)
P20/XCOUT P21/XCIN	Port P2			Sub-clock generating circuit	CPU mode register	(6) (7)
P22 P23						(8)
P24/RxD P25/TxD P26/SCLK1						
P27/CNTR0/ SRDY1	Port P3 ⁽¹⁾		CMOS compatible input level N-channel open-drain output	Serial I/O1 function I/O Timer X function I/O	Serial I/O1 control register Timer XY mode register	(9) (10) (11) (12)
P30/AN0– P34/AN4				A/D converter input	AD control register AD input selection register	(13)
P40/CNTR1	Port P4 ⁽¹⁾			Timer Y function I/O	Timer XY mode register	(14)
P41/INT0 P42/INT1				External interrupt input	Interrupt edge selection register	(15)
P43/INT2/ SCMP2				External interrupt input SCMP2 output	Interrupt edge selection register Serial I/O2 control register	(16)
P44/INT3/ PWM				External interrupt input PWM output	Interrupt edge selection register PWM control register	(17)

NOTES:

1. When bits 5 to 7 of Ports P3 and P4 are read out, the contents are undefined.

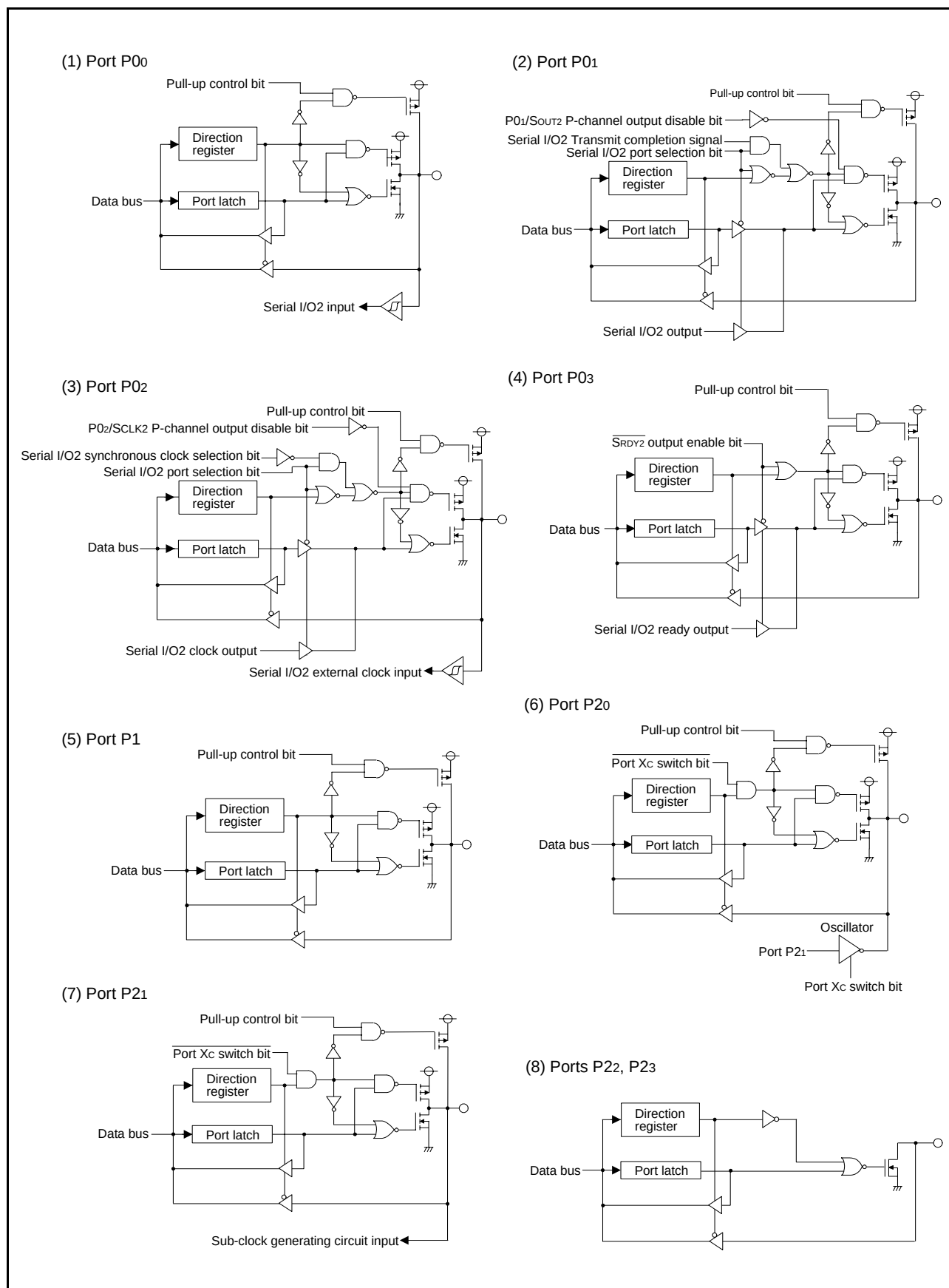


Fig 10. Port block diagram (1)

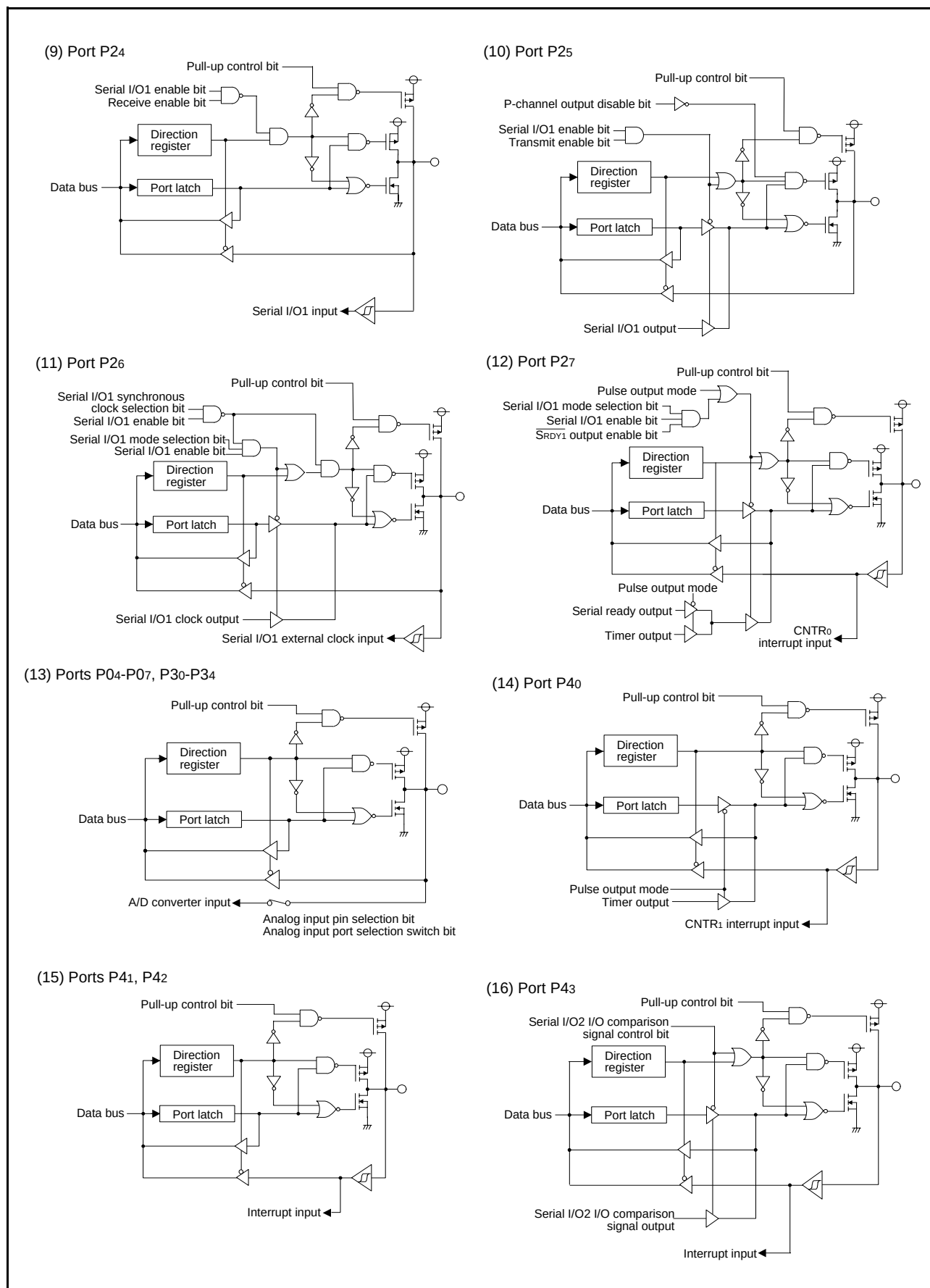


Fig 11. Port block diagram (2)

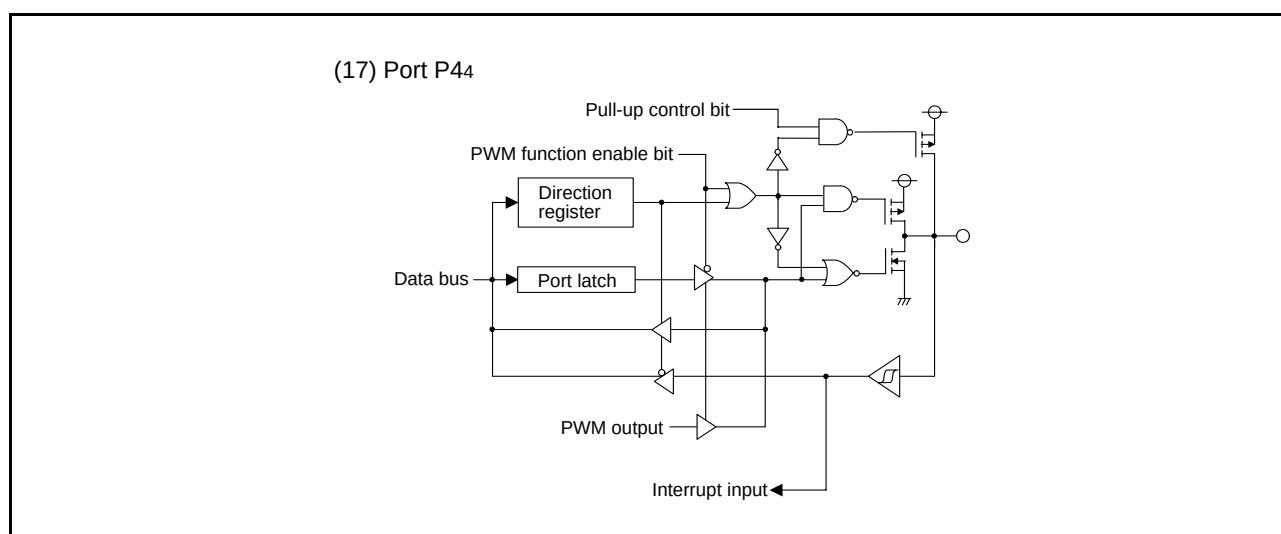


Fig 12. Port block diagram (3)

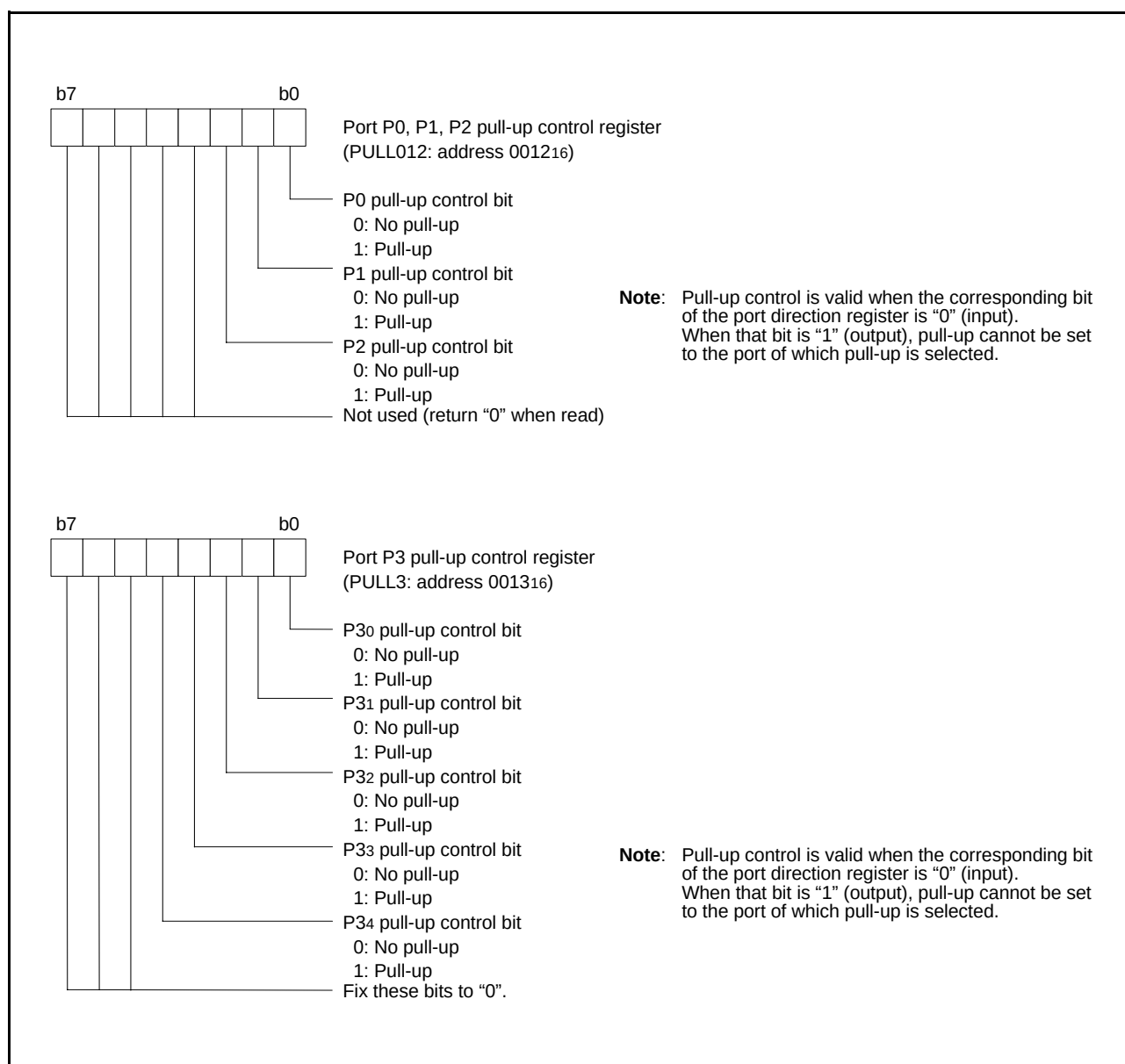


Fig 13. Structure of port registers (1)

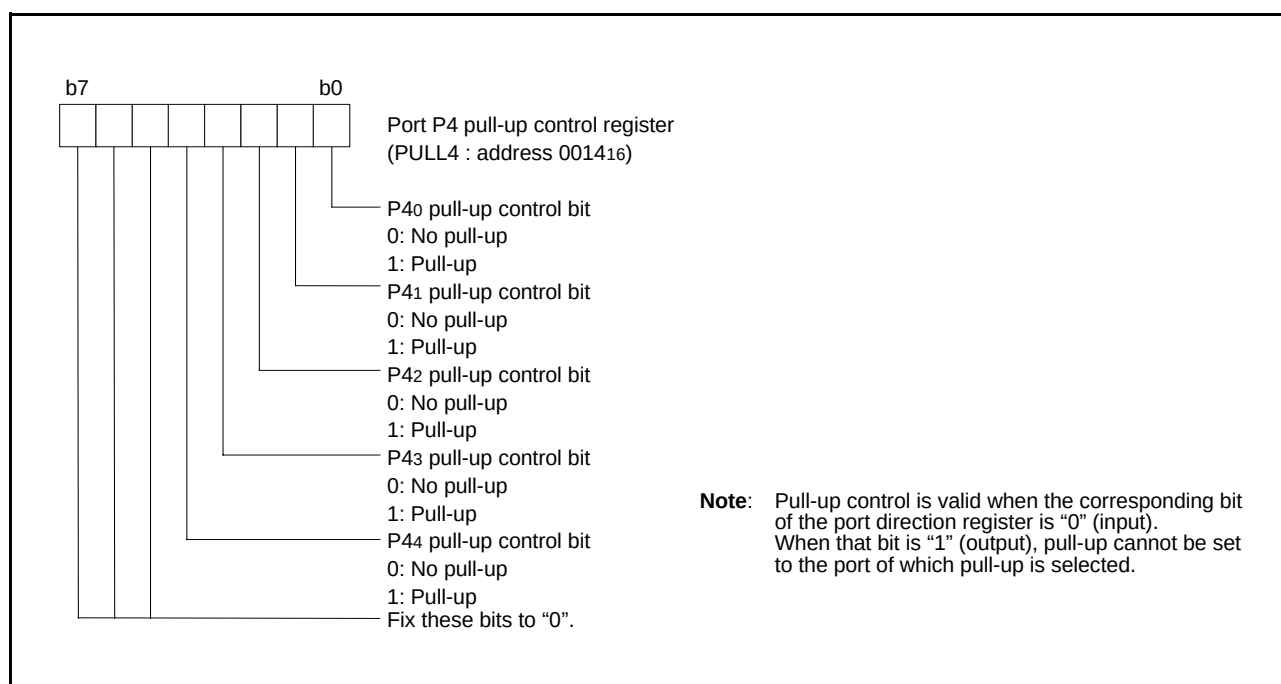


Fig 14. Structure of port registers (2)

INTERRUPTS

Interrupts occur by 15 sources among 15 sources: six external, eight internal, and one software.

• Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

• Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

<Notes>

When setting the followings, the interrupt request bit may be set to "1".

- When setting external interrupt active edge
Related register: Interrupt edge selection register (address 003A16)
Timer XY mode register (address 002316)
- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
Related register: Interrupt edge selection register (address 003A16)

When not requiring for the interrupt occurrence synchronized with these setting, take the following sequence.

- (1) Set the corresponding interrupt enable bit to "0" (disabled).
- (2) Set the interrupt edge select bit (the active edge selection bit) or the interrupt source select.
- (3) Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
- (4) Set the corresponding interrupt enable bit to "1" (enabled).

Table 8 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses ⁽¹⁾		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset ⁽²⁾	1	FFFD ₁₆	FFFC ₁₆	At reset	Non-maskable
INT ₀	2	FFFB ₁₆	FFFA ₁₆	At detection of either rising or falling edge of INT ₀ input	External interrupt (active edge selectable)
Reserved	3	FFF9 ₁₆	FFF8 ₁₆	Reserved	
INT ₁	4	FFF7 ₁₆	FFF6 ₁₆	At detection of either rising or falling edge of INT ₁ input	External interrupt (active edge selectable)
INT ₂	5	FFF5 ₁₆	FFF4 ₁₆	At detection of either rising or falling edge of INT ₂ input	External interrupt (active edge selectable)
INT ₃ /Serial I/O ₂	6	FFF3 ₁₆	FFF2 ₁₆	At detection of either rising or falling edge of INT ₃ input/ At completion of serial I/O ₂ data reception/transmission	External interrupt (active edge selectable) Switch by Serial I/O ₂ /INT ₃ interrupt source bit
Reserved	7	FFF1 ₁₆	FFF0 ₁₆	Reserved	
Timer X	8	FFEF ₁₆	FFEE ₁₆	At timer X underflow	
Timer Y	9	FFED ₁₆	FFEC ₁₆	At timer Y underflow	
Timer 1	10	FFEB ₁₆	FFEA ₁₆	At timer 1 underflow	STP release timer underflow
Timer 2	11	FFE9 ₁₆	FFE8 ₁₆	At timer 2 underflow	
Serial I/O ₁ reception	12	FFE7 ₁₆	FFE6 ₁₆	At completion of serial I/O ₁ data reception	Valid when serial I/O ₁ is selected
Serial I/O ₁ Transmission	13	FFE5 ₁₆	FFE4 ₁₆	At completion of serial I/O ₁ transfer shift or when transmission buffer is empty	Valid when serial I/O ₁ is selected
CNTR ₀	14	FFE3 ₁₆	FFE2 ₁₆	At detection of either rising or falling edge of CNTR ₀ input	External interrupt (active edge selectable)
CNTR ₁	15	FFE1 ₁₆	FFE0 ₁₆	At detection of either rising or falling edge of CNTR ₁ input	External interrupt (active edge selectable)
A/D converter	16	FFDF ₁₆	FFDE ₁₆	At completion of A/D conversion	
BRK instruction	17	FFDD ₁₆	FFDC ₁₆	At BRK instruction execution	Non-maskable software interrupt

NOTES:

1. Vector addresses contain interrupt jump destination addresses.
2. Reset function in the same way as an interrupt with the highest priority.

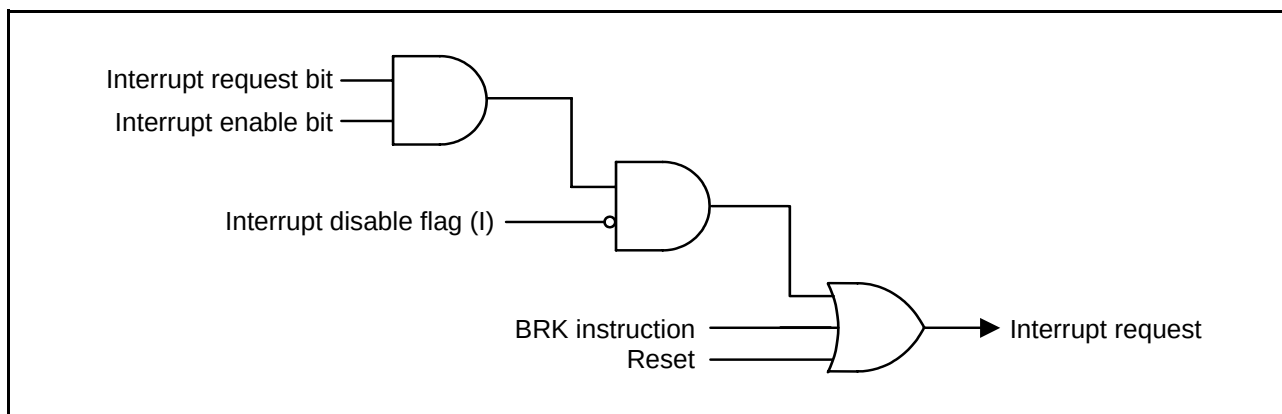


Fig 15. Interrupt control

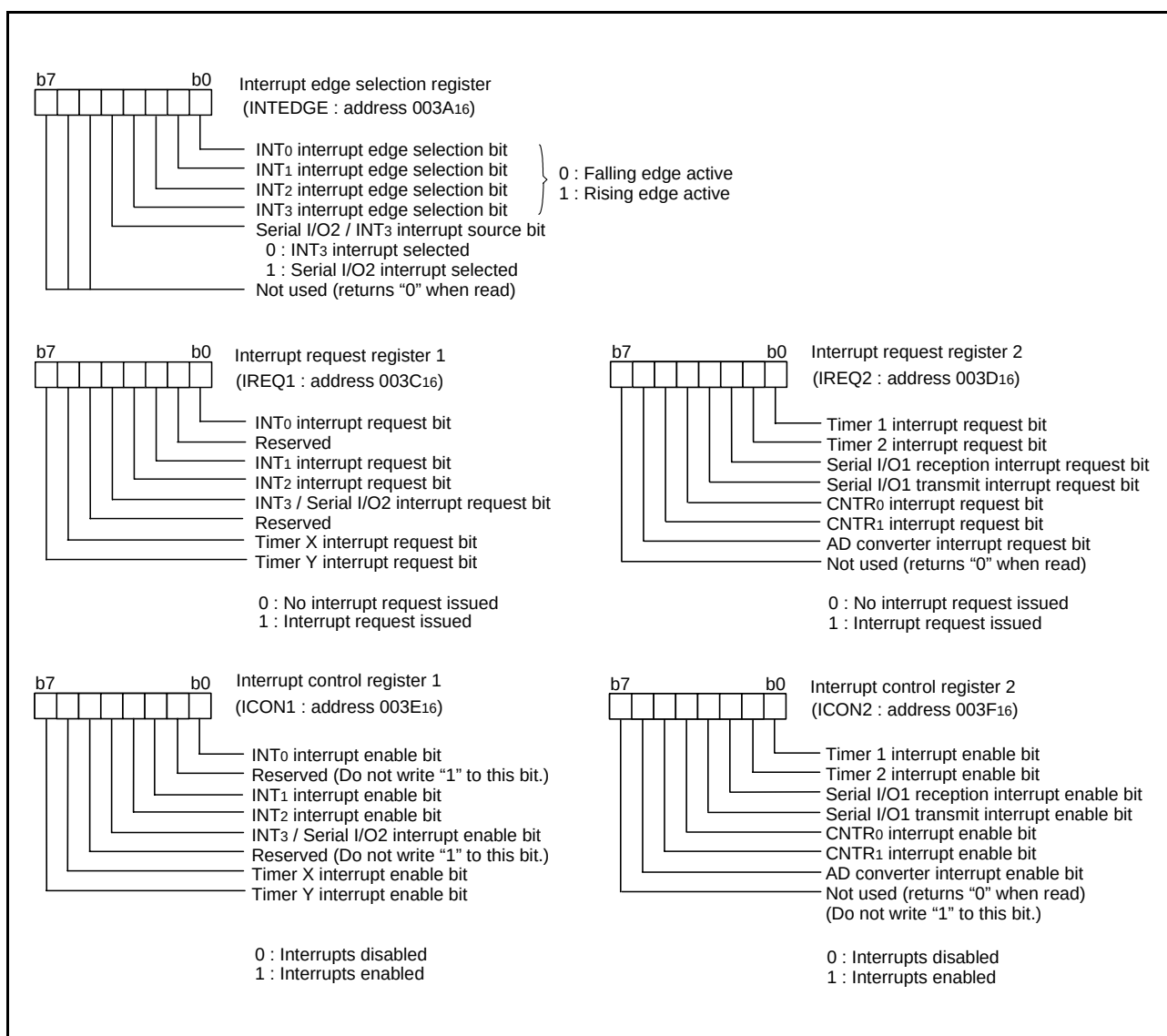


Fig 16. Structure of interrupt-related registers

TIMERS

The 3850 group (spec.A) has four timers: timer X, timer Y, timer 1, and timer 2.

The division ratio of each timer or prescaler is given by $1/(n + 1)$, where n is the value in the corresponding timer or prescaler latch. All timers are count down. When the timer reaches "0016", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

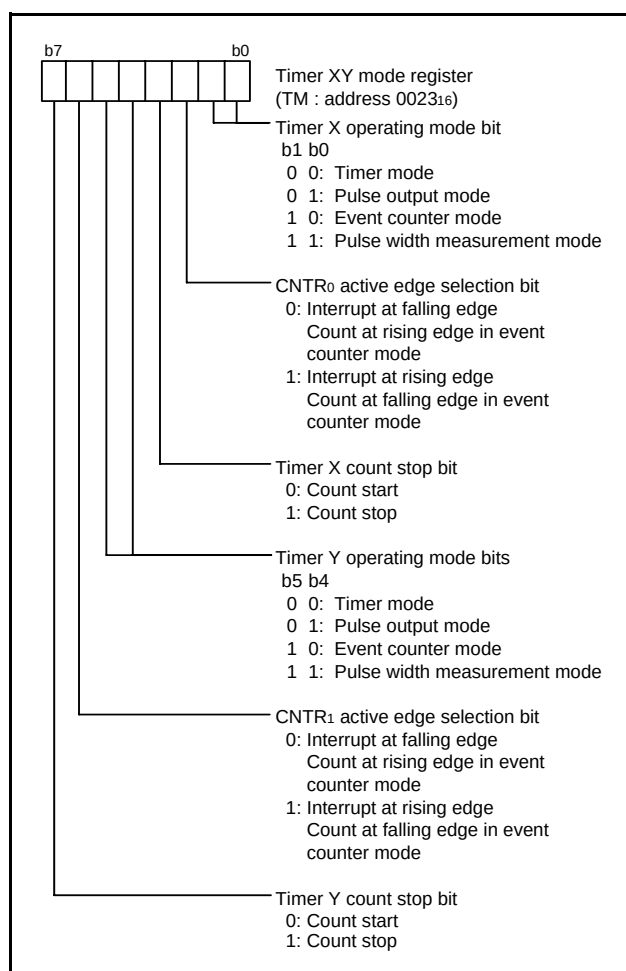


Fig 17. Structure of timer XY mode register

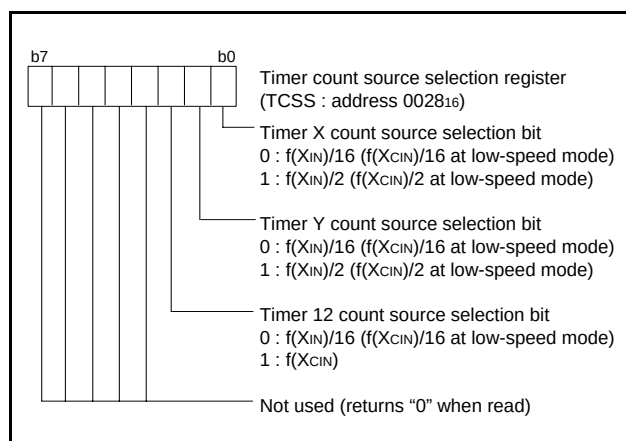


Fig 18. Structure of timer count source selection register

• Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency which is selected by timer 12 count source selection bit. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer underflow sets the interrupt request bit.

• Timer X and Timer Y

Timer X and Timer Y can each select in one of four operating modes by setting the timer XY mode register.

(1) Timer Mode

The timer counts the count source selected by Timer count source selection bit.

(2) Pulse Output Mode

The timer counts the count source selected by Timer count source selection bit. Whenever the contents of the timer reach "0016", the signal output from the CNTR0 (or CNTR1) pin is inverted. If the CNTR0 (or CNTR1) active edge selection bit is "0", output begins at "H".

If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port P27 (or port P40) direction register to output mode.

(3) Event Counter Mode

Operation in event counter mode is the same as in timer mode, except that the timer counts signals input through the CNTR0 or CNTR1 pin.

When the CNTR0 (or CNTR1) active edge selection bit is "0", the rising edge of the CNTR0 (or CNTR1) pin is counted. When the CNTR0 (or CNTR1) active edge selection bit is "1", the falling edge of the CNTR0 (or CNTR1) pin is counted.

(4) Pulse Width Measurement Mode

If the CNTR0 (or CNTR1) active edge selection bit is "0", the timer counts the selected signals by the count source selection bit while the CNTR0 (or CNTR1) pin is at "H". If the CNTR0 (or CNTR1) active edge selection bit is "1", the timer counts it while the CNTR0 (or CNTR1) pin is at "L".

The count can be stopped by setting "1" to the timer X (or timer Y) count stop bit in any mode. The corresponding interrupt request bit is set each time a timer underflows.

<Notes>

When switching the count source by the timer 12, X and Y count source bits, the value of timer count is altered in unconsiderable amount owing to generating of a thin pulses in the count input signals.

Therefore, select the timer count source before set the value to the prescaler and the timer.

When timer X/timer Y underflow while executing the instruction which sets "1" to the timer X/timer Y count stop bits, the timer X/ timer Y interrupt request bits are set to "1". Timer X/Timer Y interrupts are received if these interrupts are enabled at this time. The timing which interrupt is accepted has a case after the instruction which sets "1" to the count stop bit, and a case after the next instruction according to the timing of the timer underflow. When this interrupt is unnecessary, set "0" (disabled) to the interrupt enable bit and then set "1" to the count stop bit.

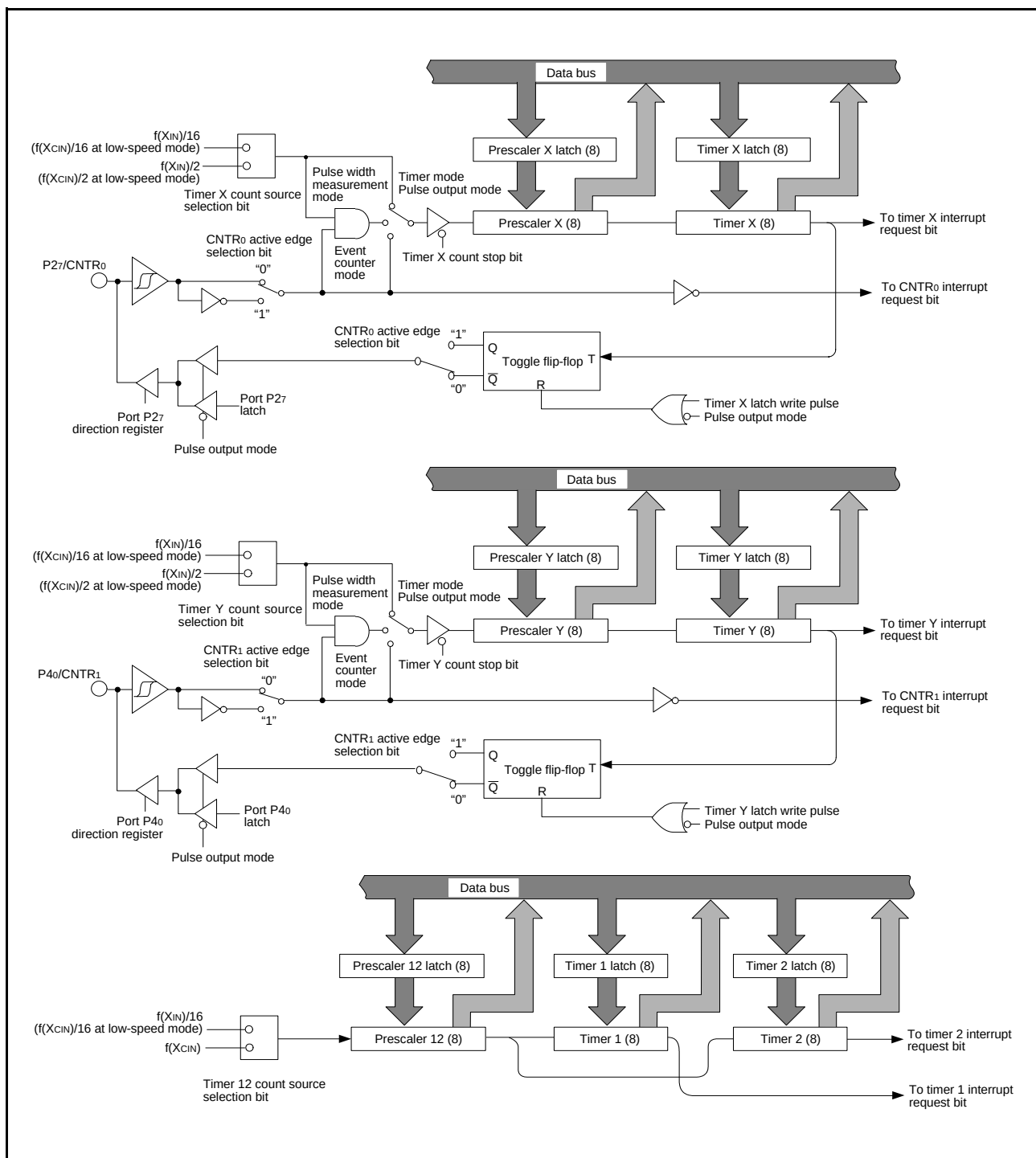


Fig 19. Block diagram of timer X, timer Y, timer 1, and timer 2

SERIAL INTERFACE

• Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O1. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6 of address 001A16) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

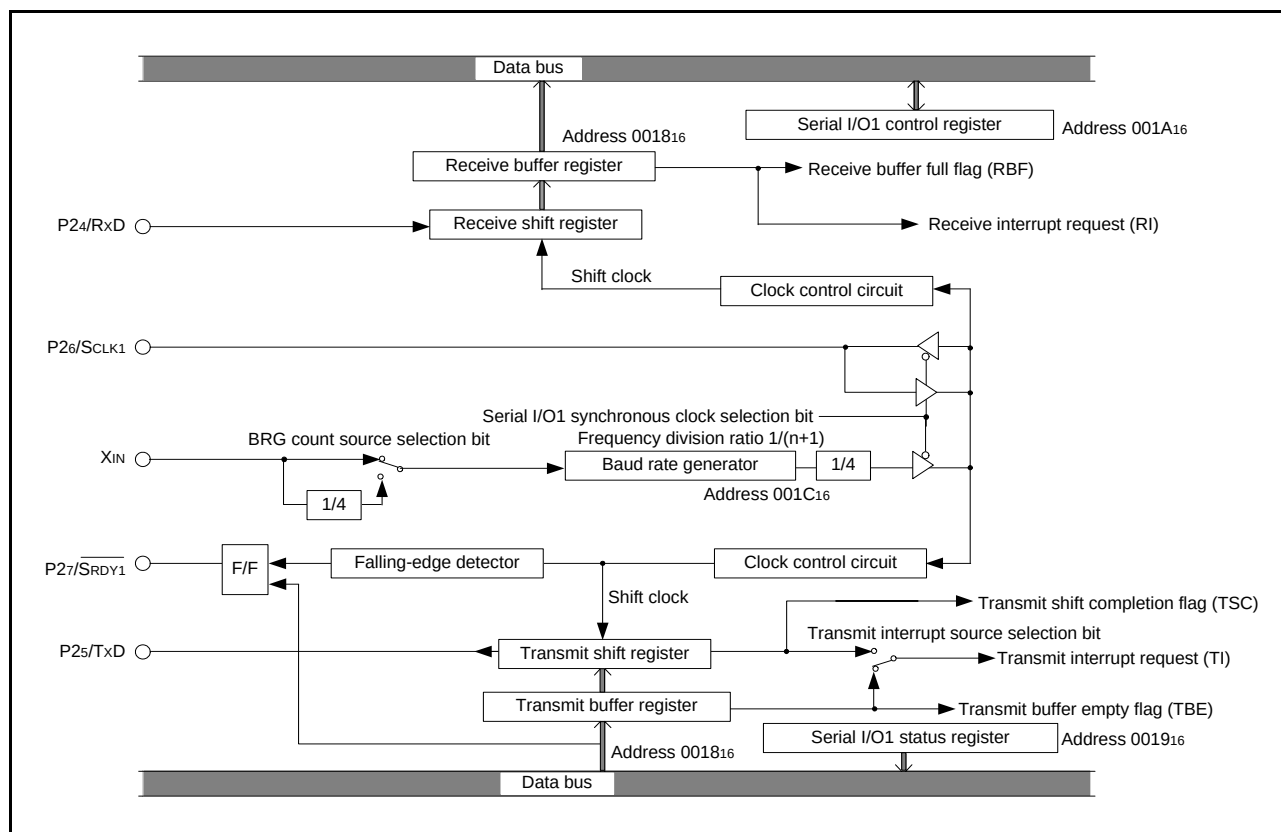


Fig 20. Block diagram of clock synchronous serial I/O1

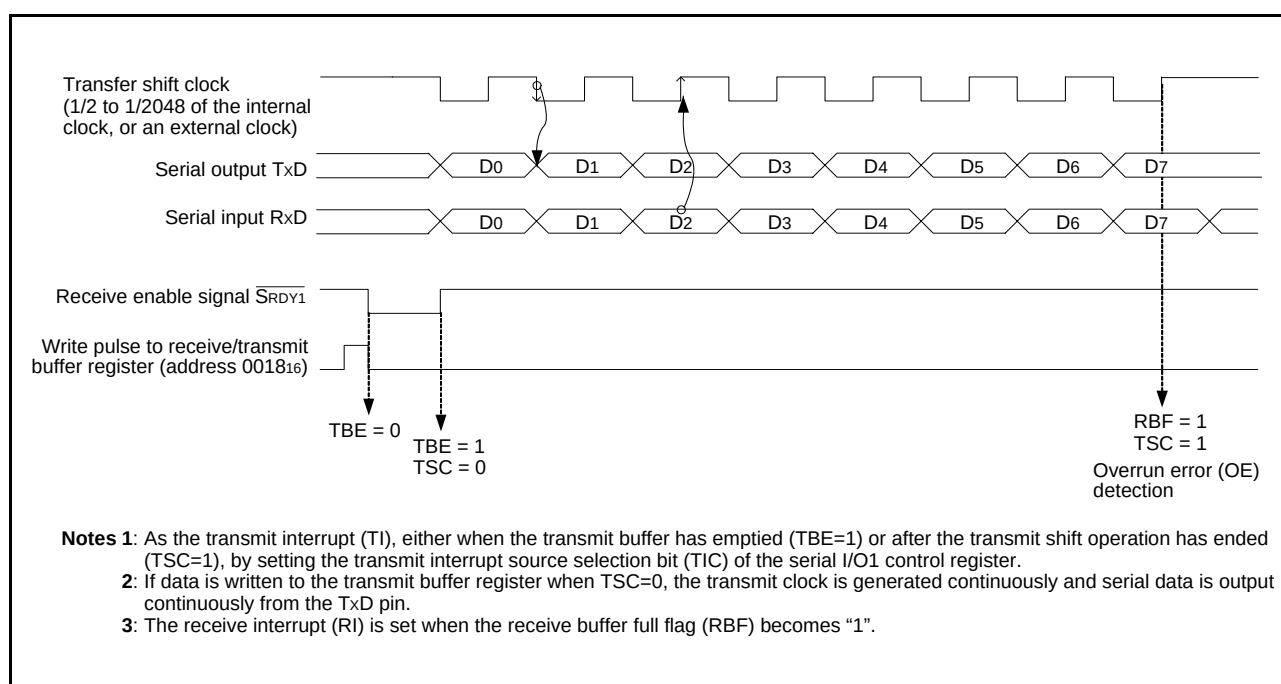


Fig 21. Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit (b6) of the serial I/O1 control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data

is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

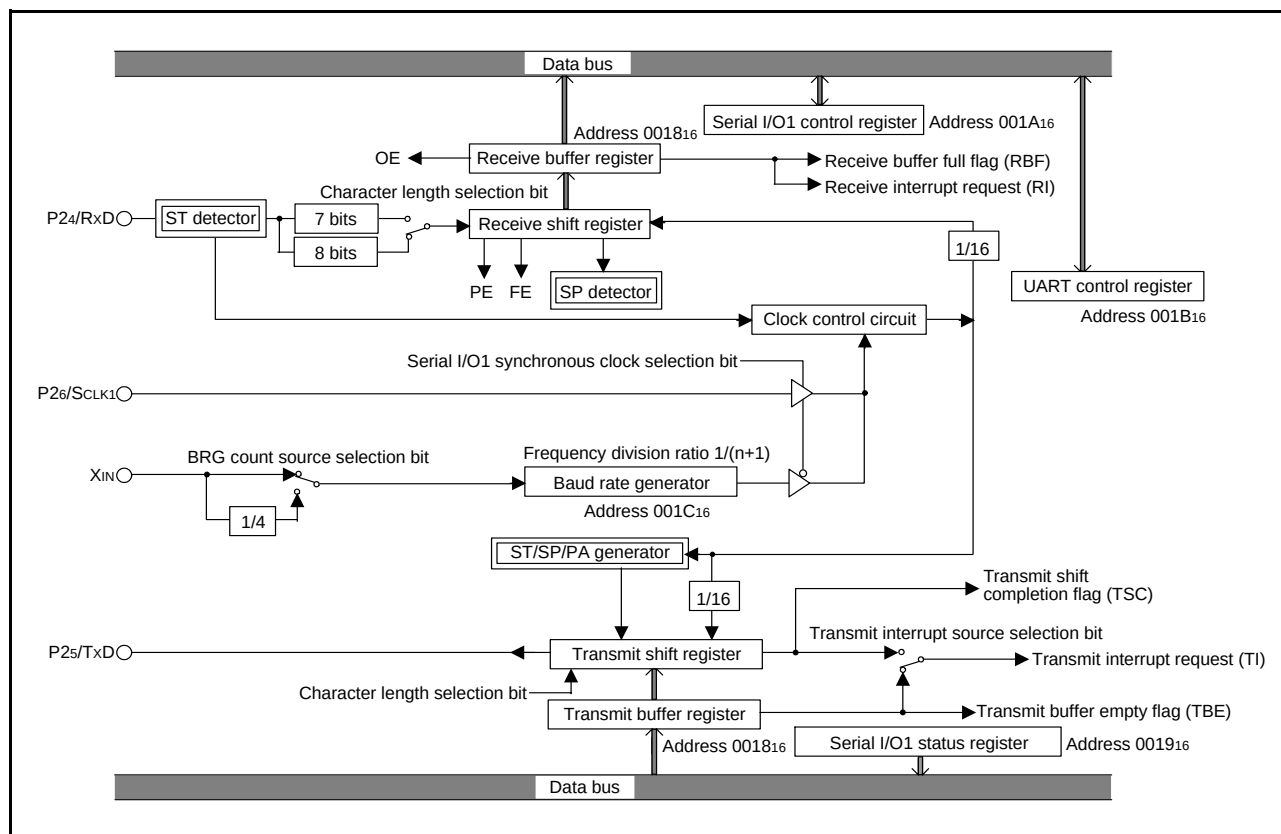


Fig 22. Block diagram of UART serial I/O1

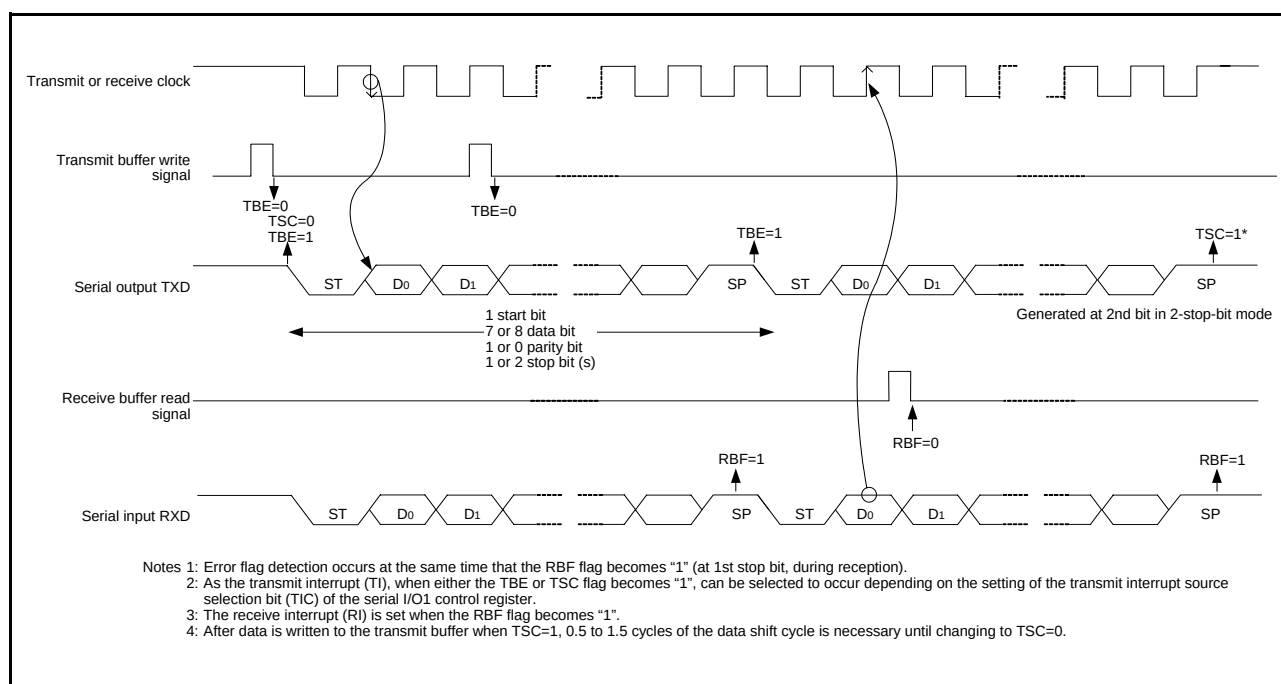


Fig 23. Operation of UART serial I/O1 function

[Transmit Buffer Register/Receive Buffer Register (TB/RB)] 0018₁₆

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O1 Status Register (SIOSTS)] 0019₁₆

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O1 Control Register (SIOCON)] 001A₁₆

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART Control Register (UARTCON)] 001B₁₆

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P25/TxD pin.

[Baud Rate Generator (BRG)] 001C₁₆

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

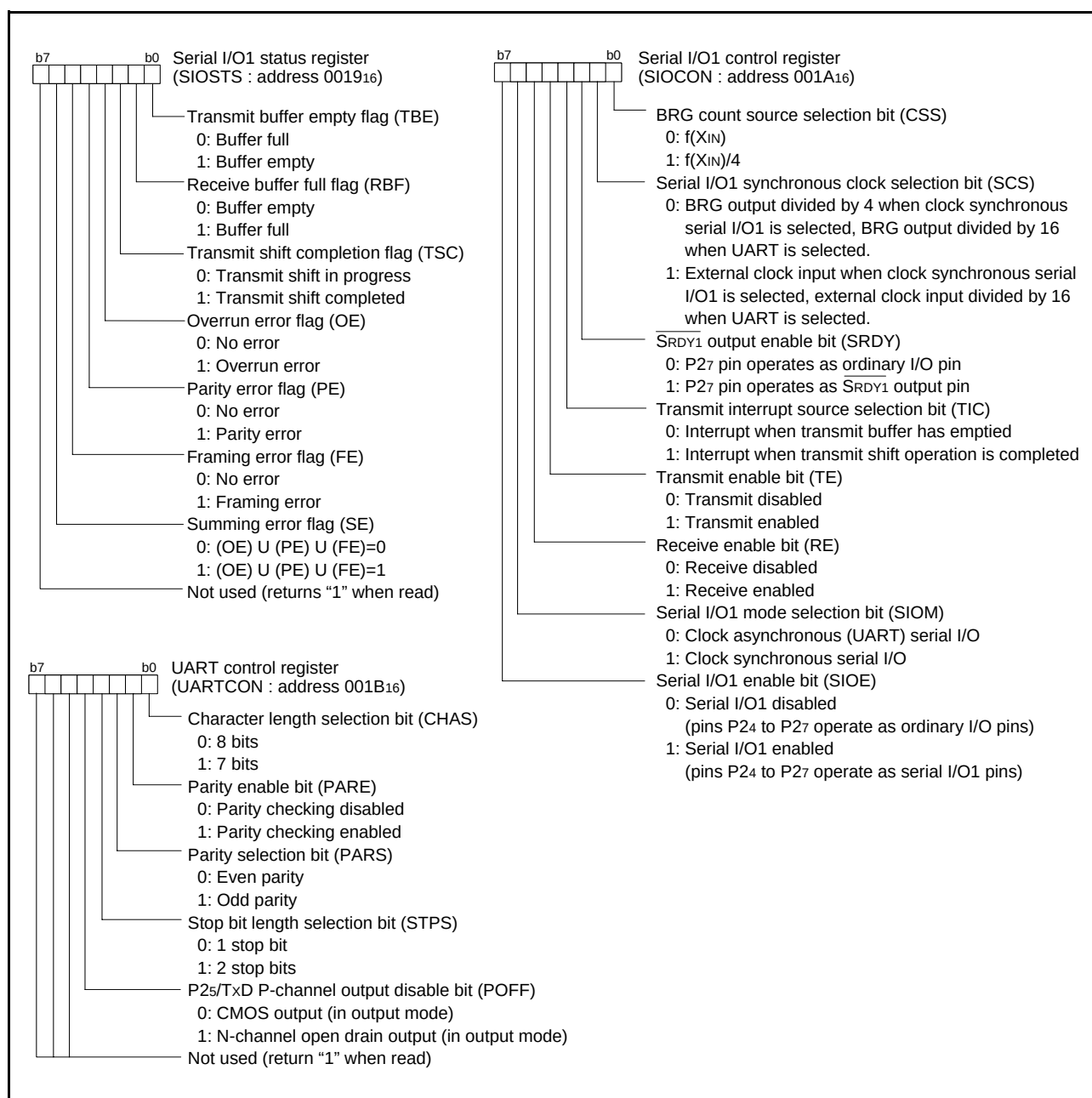


Fig 24. Structure of serial I/O1 control registers

<Notes on serial interface>

When setting the transmit enable bit to "1", the serial I/O1 transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

- (1) Set the serial I/O1 transmit interrupt enable bit to "0" (disabled).
- (2) Set the transmit enable bit to "1".
- (3) Set the serial I/O1 transmit interrupt request bit to "0" after 1 or more instructions have been executed.
- (4) Set the serial I/O1 transmit interrupt enable bit to "1" (enabled).

• Serial I/O2

The serial I/O2 can be operated only as the clock synchronous type. As a synchronous clock for serial transfer, either internal clock or external clock can be selected by the serial I/O2 synchronous clock selection bit (b6) of serial I/O2 control register 1.

The internal clock incorporates a dedicated divider and permits selecting 6 types of clock by the internal synchronous clock selection bits (b2, b1, b0) of serial I/O2 control register 1.

Regarding SOUT2 and SCLK2 being output pins, either CMOS output format or N-channel open-drain output format can be selected by the P01/SOUT2, P02/SCLK2 P-channel output disable bit (b7) of serial I/O2 control register 1.

When the internal clock has been selected, a transfer starts by a write signal to the serial I/O2 register (address 001716). After completion of data transfer, the level of the SOUT2 pin goes to high impedance automatically but bit 7 of the serial I/O2 control register 2 is not set to "1" automatically.

When the external clock has been selected, the contents of the serial I/O2 register is continuously shifted while transfer clocks are input. Accordingly, control the clock externally. Note that the SOUT2 pin does not go to high impedance after completion of data transfer.

To cause the SOUT2 pin to go to high impedance in the case where the external clock is selected, set bit 7 of the serial I/O2 control register 2 to "1" when SCLK2 is "H" after completion of data transfer. After the next data transfer is started (the transfer clock falls), bit 7 of the serial I/O2 control register 2 is set to "0" and the SOUT2 pin is put into the active state.

Regardless of the internal clock to external clock, the interrupt request bit is set after the number of bits (1 to 8 bits) selected by the optional transfer bit is transferred. In case of a fractional number of bits less than 8 bits as the last data, the received data to be stored in the serial I/O2 register becomes a fractional number of bits close to MSB if the transfer direction selection bit of serial I/O2 control register 1 is LSB first, or a fractional number of bits close to LSB if the transfer direction selection bit is MSB first. For the remaining bits, the previously received data is shifted.

At transmit operation using the clock synchronous serial I/O, the SCMP2 signal can be output by comparing the state of the transmit pin SOUT2 with the state of the receive pin SIN2 in synchronization with a rise of the transfer clock. If the output level of the SOUT2 pin is equal to the input level to the SIN2 pin, "L" is output from the SCMP2 pin. If not, "H" is output. At this time, an INT2 interrupt request can also be generated. Select a valid edge by bit 2 of the interrupt edge selection register (address 003A16).

[Serial I/O2 Control Registers 1, 2 (SIO2CON1 / SIO2CON2)] 001516, 001616

The serial I/O2 control registers 1 and 2 are containing various selection bits for serial I/O2 control as shown in Figure 25.

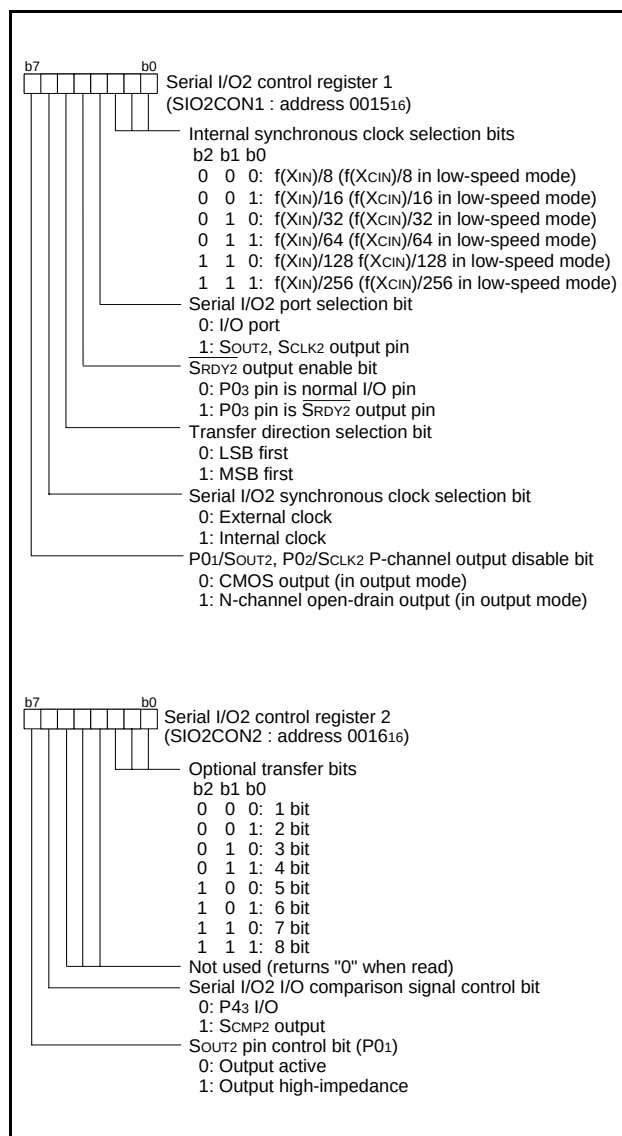


Fig 25. Structure of Serial I/O2 control registers 1, 2

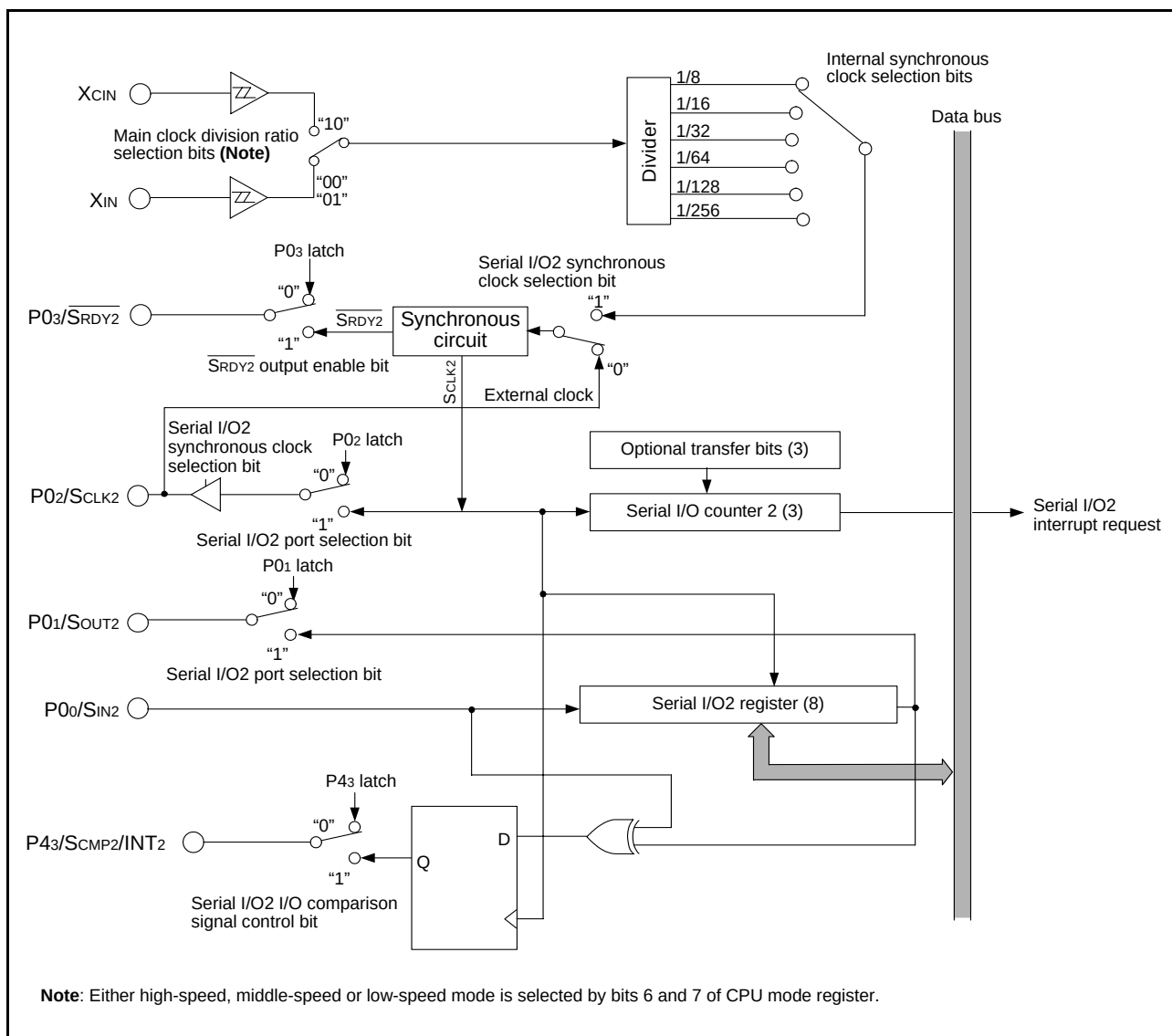


Fig 26. Block diagram of Serial I/O2

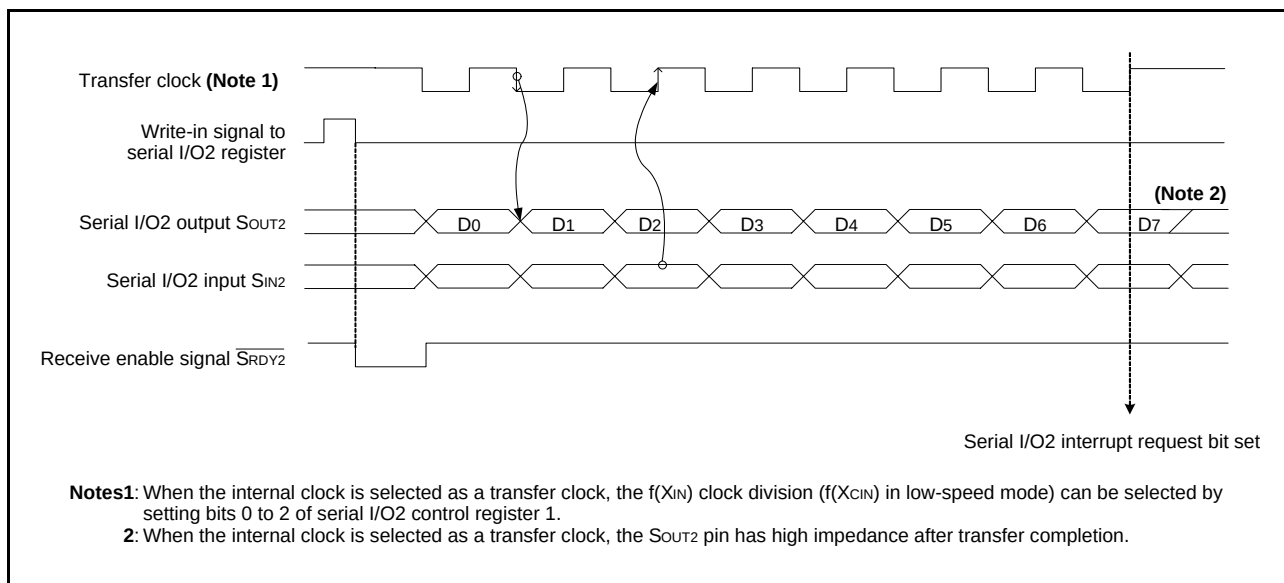


Fig 27. Timing chart of Serial I/O2

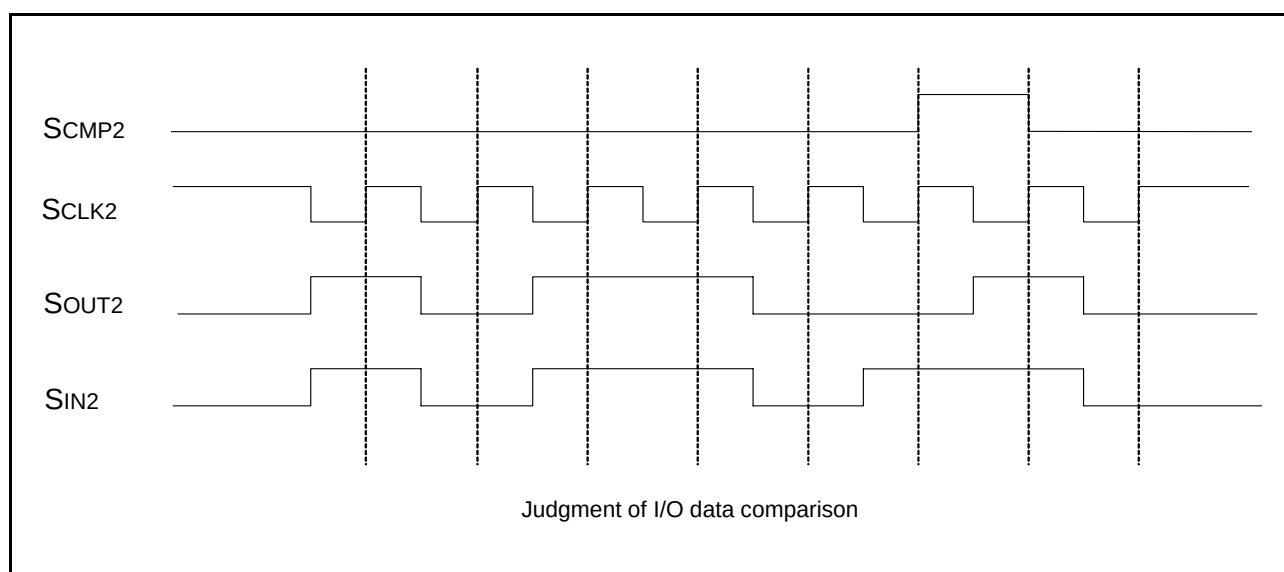


Fig 28. SCMP2 output operation

PWM (PWM: Pulse Width Modulation)

The 3850 group (spec.A) has a PWM function with an 8-bit resolution, based on a signal that is the clock input X_{IN} or that clock input divided by 2.

• Data Setting

The PWM output pin also functions as port P44. Set the PWM period by the PWM prescaler, and set the “H” term of output pulse by the PWM register.

If the value in the PWM prescaler is n and the value in the PWM register is m (where $n = 0$ to 255 and $m = 0$ to 255):

PWM period = $255 \times (n+1) / f(X_{IN})$

= $31.875 \times (n+1) \mu s$

(when $f(X_{IN}) = 8 \text{ MHz}$, count source selection bit = “0”)

Output pulse “H” term = PWM period $\times m / 255$

= $0.125 \times (n+1) \times m \mu s$

(when $f(X_{IN}) = 8 \text{ MHz}$, count source selection bit = “0”)

• PWM Operation

When bit 0 (PWM enable bit) of the PWM control register is set to “1”, operation starts by initializing the PWM output circuit, and pulses are output starting at an “H”.

If the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

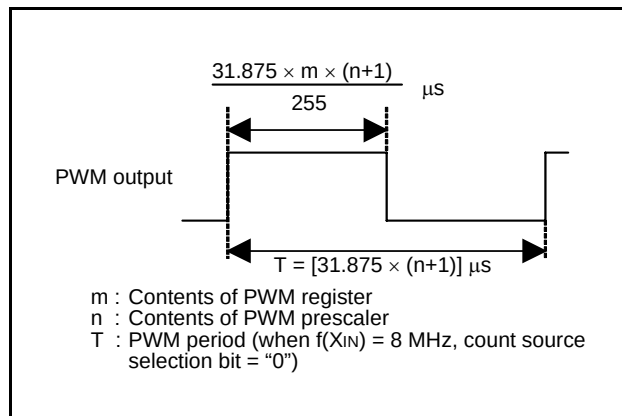


Fig 29. Timing of PWM period

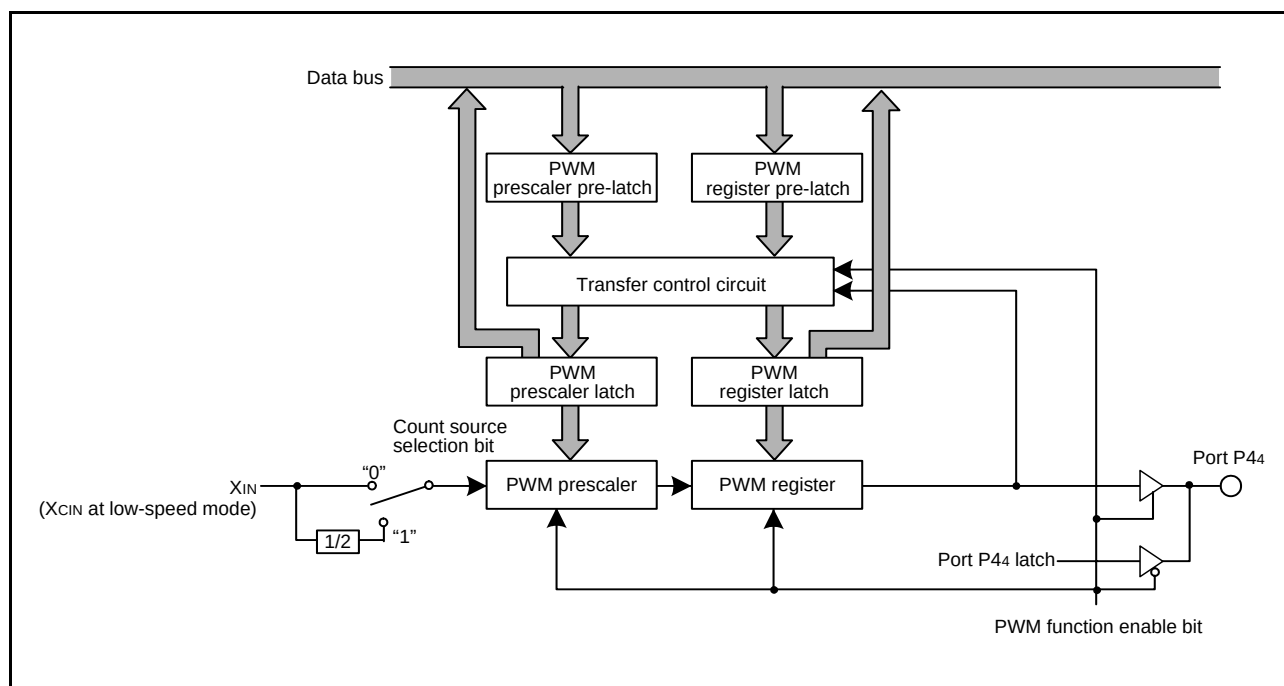


Fig 30. Block diagram of PWM function

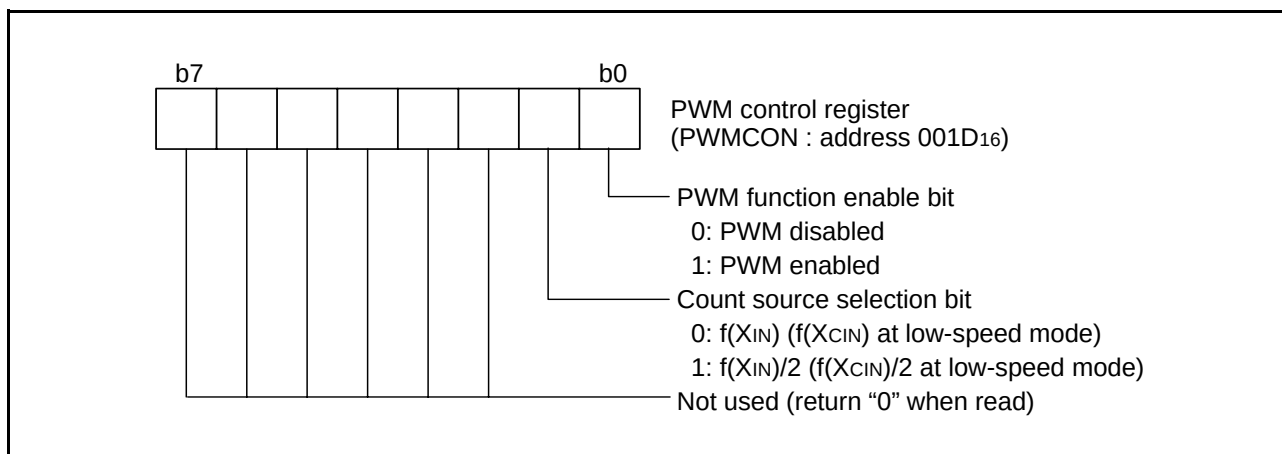


Fig 31. Structure of PWM control register

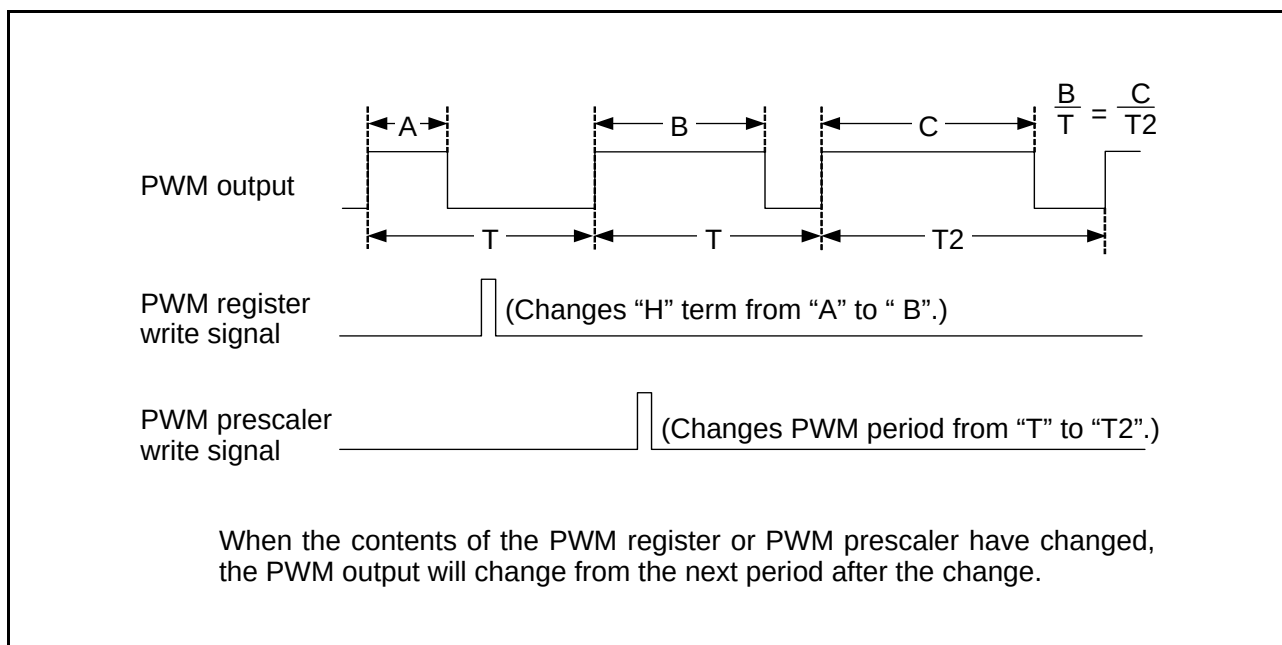


Fig 32. PWM output timing when PWM register or PWM prescaler is changed

<Notes>

The PWM starts after the PWM function enable bit is set to enable and "L" level is output from the PWM pin. The length of this "L" level output is as follows:

$$\frac{n+1}{2 \times f(X_{IN})} \text{ sec} \quad (\text{Count source selection bit} = 0, \text{ where } n \text{ is the value set in the prescaler})$$

$$\frac{n+1}{f(X_{IN})} \text{ sec} \quad (\text{Count source selection bit} = 1, \text{ where } n \text{ is the value set in the prescaler})$$

A/D CONVERTER

[AD Conversion Registers (ADL, ADH)] 0035₁₆, 0036₁₆

The AD conversion registers are read-only registers that store the result of an A/D conversion. Do not read these registers during an A/D conversion.

[AD Control Register (ADCON)] 0034₁₆

The AD control register controls the A/D conversion process. Bits 0 to 2 select a specific analog input pin. By setting a value to these bits, when bit 0 of the AD input selection register (address 0037₁₆) is "0", P30/AN0-P34/AN4 can be selected, and when bit 0 of the AD input selection register is "1", P04/AN5-P07/AN8 can be selected.

Bit 4 indicates the completion of an A/D conversion. The value of this bit remains at "0" during an A/D conversion and changes to "1" when an A/D conversion ends. Writing "0" to this bit starts the A/D conversion.

[AD Input Selection Register (ADSEL)] 0037₁₆

The analog input port selection switch bit is assigned to bit 0 of the AD input selection register. When "0" is set to the analog input port selection switch bit, P30/AN0-P34/AN4 can be selected by the analog input pin selection bits (b2, b1, b0) of the AD control register (address 0034₁₆). When "1" is set to the analog input port selection switch bit, P04/AN5-P07/AN8 can be selected by the analog input pin selection bits (b2, b1, b0) of the AD control register (address 0034₁₆).

• Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF into 1024 and outputs the divided voltages.

• Channel Selector

The channel selector selects one of ports P30/AN0 to P34/AN4, P04/AN5 to P07/AN8 and inputs the voltage to the comparator.

• Comparator and Control Circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage, and the result is stored in the AD conversion registers. When an A/D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

Note that because the comparator consists of a capacitor coupling, set $f(X_{IN})$ to 500 kHz or more during an A/D conversion.

When the A/D converter is operated at low-speed mode, $f(X_{IN})$ and $f(X_{CIN})$ do not have the lower limit of frequency, because of the A/D converter has a built-in self-oscillation circuit.

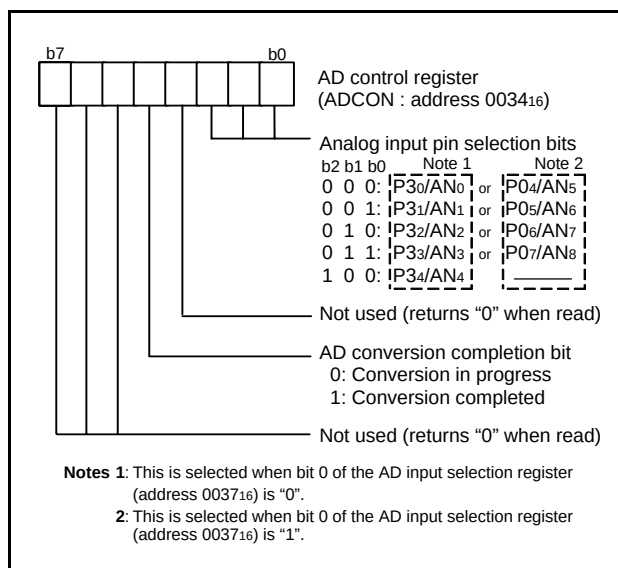


Fig 33. Structure of AD control register

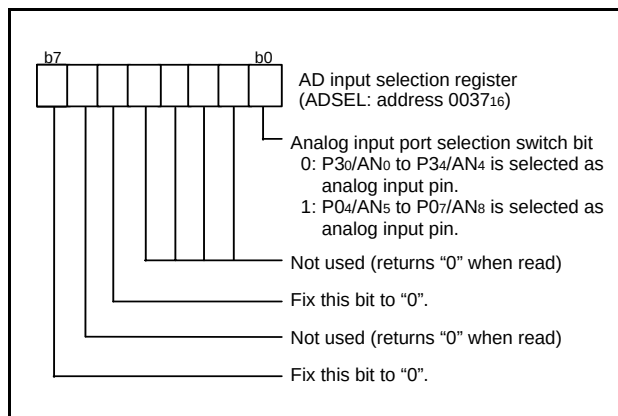


Fig 34. Structure of AD input selection register

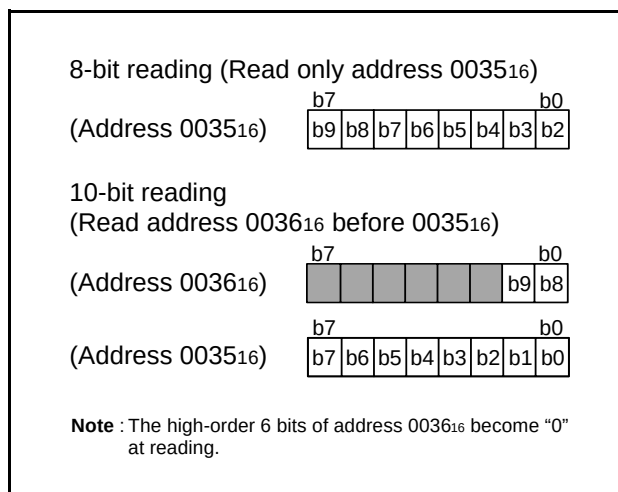


Fig 35. Structure of AD conversion registers

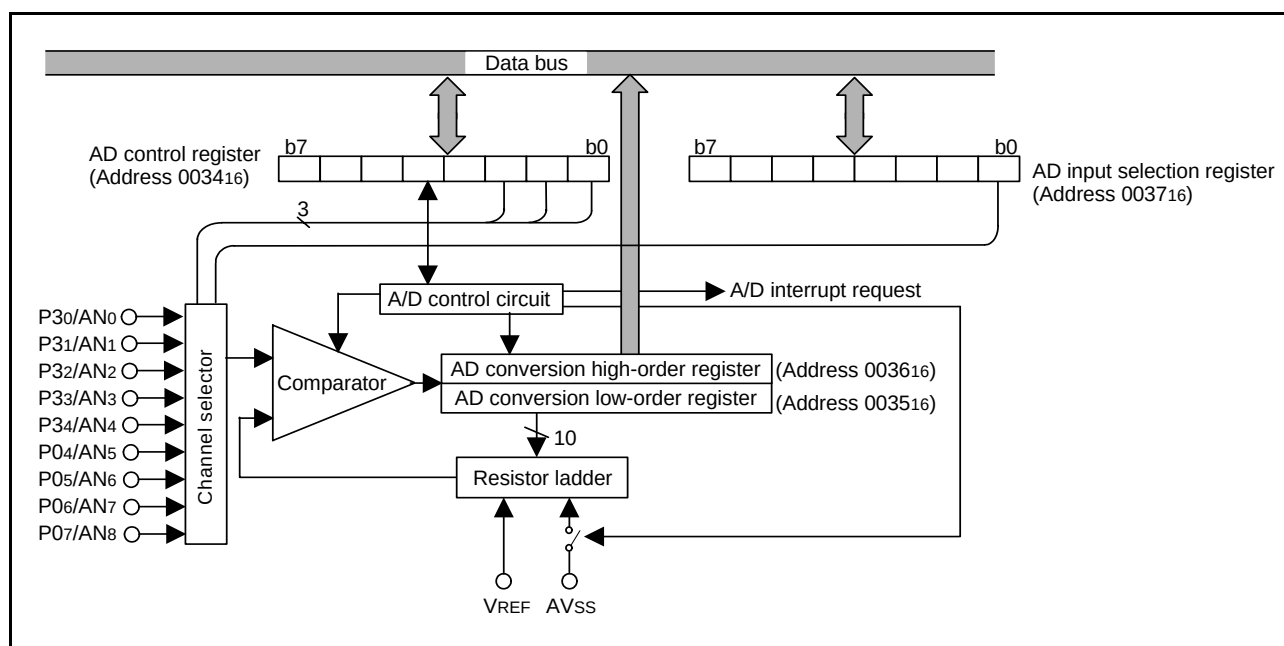


Fig 36. Block diagram of A/D converter

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

• Initial value of watchdog timer

At reset or writing to the watchdog timer control register (address 0039₁₆), each of watchdog timer H and L is set to "FF₁₆". Any instruction which generates a write signal such as the instructions of STA, LDM, CLB and others can be used to write. The data of bits 6 and 7 are only valid when writing to the watchdog timer control register. Each of watchdog timer is set to "FF₁₆" regardless of the written data of bits 0 to 5.

Bit 6 can be written to only once after reset release.

After this bit is written, it cannot be rewritten because it is locked.

• Operation of Watchdog Timer

The watchdog timer stops at reset and starts to count down by writing to the watchdog timer control register. An internal reset occurs at an underflow of the watchdog timer H. The reset is released after waiting for a reset release time and the program is processed from the reset vector address. Accordingly, programming is usually performed so that writing to the watchdog timer control register may be started before an underflow. If writing to the watchdog timer control register is not performed once, the watchdog timer does not function.

• Bit 6 of Watchdog Timer Control Register

- When bit 6 of the watchdog timer control register is "0", the MCU enters the stop mode by execution of STP instruction. Just after releasing the stop mode, the watchdog timer restarts counting (Note). When executing the WIT instruction, the watchdog timer does not stop.
- When bit 6 is "1", execution of STP instruction causes an internal reset. When this bit is set to "1" once, it cannot be rewritten to "0" by program. Bit 6 is "0" at reset.

The required time after writing to the watchdog timer control register to an underflow of the watchdog timer H is shown as follows.

When bit 7 of the watchdog timer control register is "0":

32 s at $X_{CIN} = 32.768$ kHz frequency and
83.886ms at $X_{IN} = 12.5$ MHz frequency.

When bit 7 of the watchdog timer control register is "1":

125 ms at $X_{CIN} = 32.768$ kHz frequency and
327.68 μ s at $X_{IN} = 12.5$ MHz frequency.

- Notes 1. The watchdog timer continues to count for waiting for a stop mode release time. Do not generate an underflow of the watchdog timer H during that time.
2. The watchdog timer cannot be used in the middle-speed mode. (The internal reset may not be generated correctly, depending on the underflow timing of the watchdog timer.)

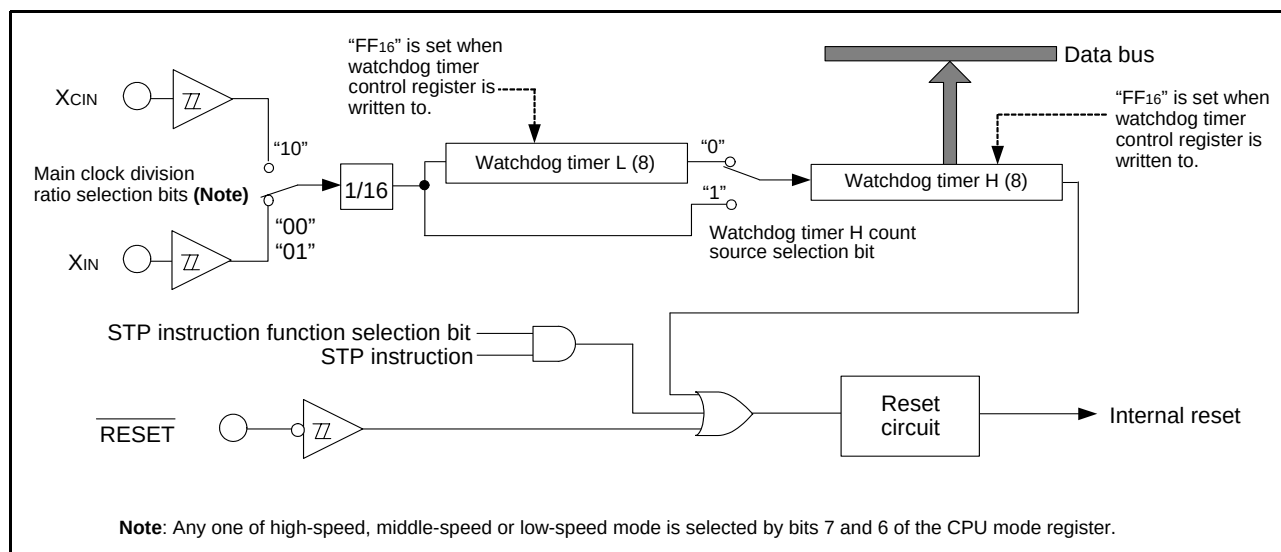


Fig 37. Block diagram of Watchdog timer

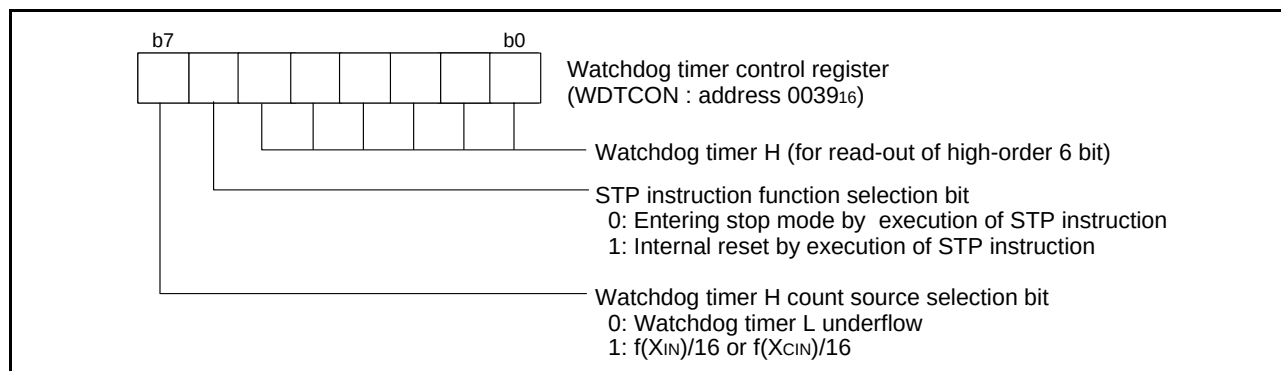


Fig 38. Structure of Watchdog timer control register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin must be held at an “L” level for 20 cycles or more of X_{IN} . Then the $\overline{\text{RESET}}$ pin is returned to an “H” level (the power source voltage must be between 1.8 V and 5.5 V, and the oscillation must be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD₁₆ (high-order byte) and address FFFC₁₆ (low-order byte). Make sure that the reset input voltage is less than 0.28 V for V_{CC} of 1.8 V.

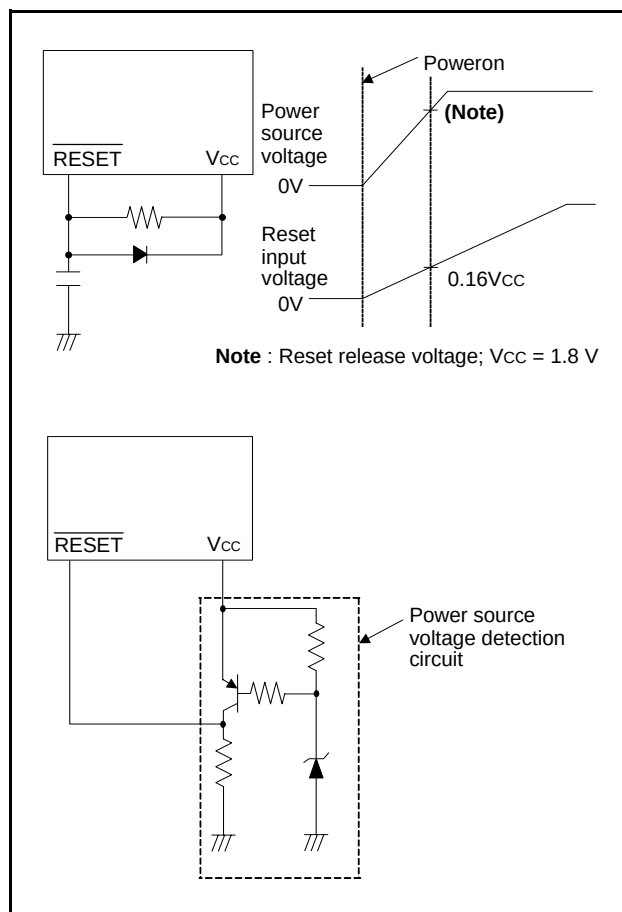


Fig 39. Reset circuit example

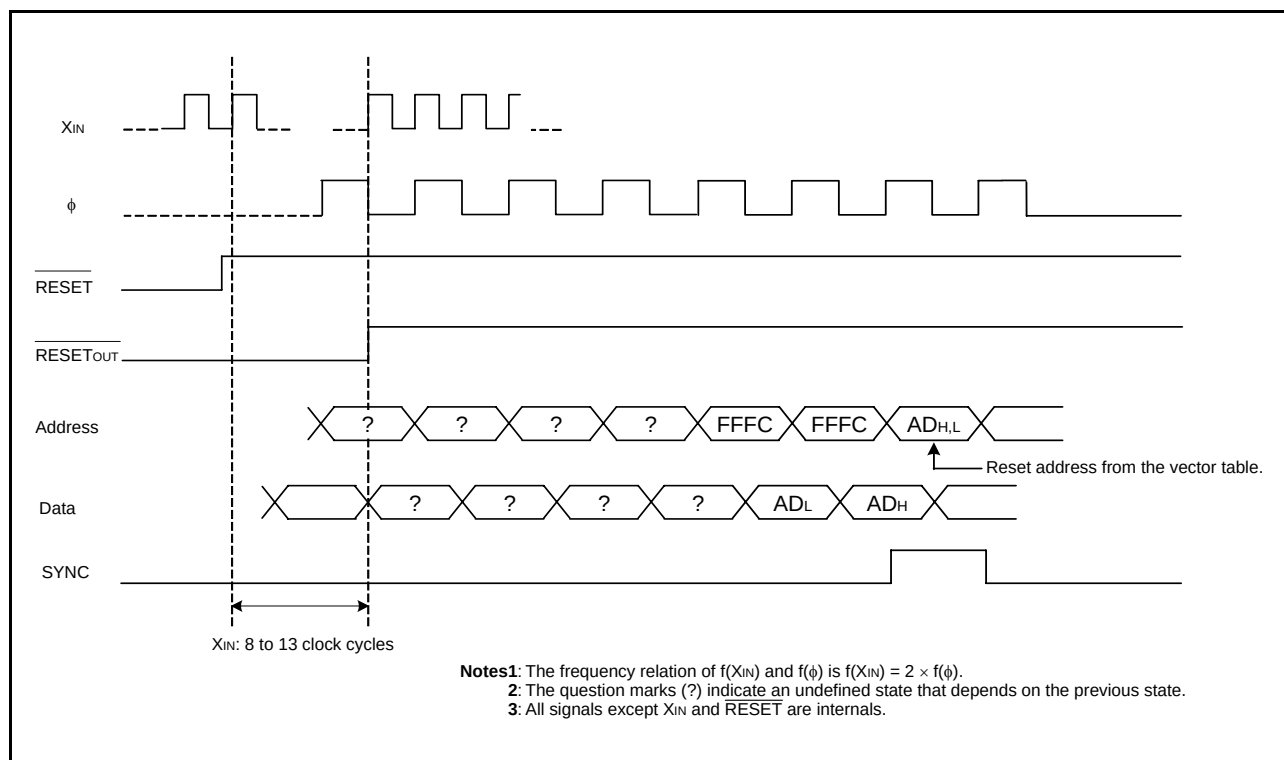


Fig 40. Reset sequence

Address		Register contents	Address		Register contents
(1)	Port P0 (P0)	0000 ₁₆ 00₁₆	(34)	AD control register (ADCON)	0034 ₁₆ 0 0 0 1 0 0 0 0
(2)	Port P0 direction register (P0D)	0001 ₁₆ 00₁₆	(35)	AD conversion low-order register (ADL)	0035 ₁₆ X X X X X X X X
(3)	Port P1 (P1)	0002 ₁₆ 00₁₆	(36)	AD conversion high-order register (ADH)	0036 ₁₆ 0 0 0 0 0 0 X X
(4)	Port P1 direction register (P1D)	0003 ₁₆ 00₁₆	(37)	AD input selection register (ADSEL)	0037 ₁₆ 00₁₆
(5)	Port P2 (P2)	0004 ₁₆ 00₁₆	(38)	MISRG	0038 ₁₆ 00₁₆
(6)	Port P2 direction register (P2D)	0005 ₁₆ 00₁₆	(39)	Watchdog timer control register (WDTCON)	0039 ₁₆ 0 0 1 1 1 1 1 1
(7)	Port P3 (P3)	0006 ₁₆ 00₁₆	(40)	Interrupt edge selection register (INTEDGE)	003A ₁₆ 00₁₆
(8)	Port P3 direction register (P3D)	0007 ₁₆ 00₁₆	(41)	CPU mode register (CPUM)	003B ₁₆ 0 1 0 0 1 0 0 0
(9)	Port P4 (P4)	0008 ₁₆ 00₁₆	(42)	Interrupt request register 1 (IREQ1)	003C ₁₆ 00₁₆
(10)	Port P4 direction register (P4D)	0009 ₁₆ 00₁₆	(43)	Interrupt request register 2 (IREQ2)	003D ₁₆ 00₁₆
(11)	Port P0, P1, P2 pull-up control register (PULL012)	0012 ₁₆ 00₁₆	(44)	Interrupt control register 1 (ICON1)	003E ₁₆ 00₁₆
(12)	Port P3 pull-up control register (PULL3)	0013 ₁₆ 00₁₆	(45)	Interrupt control register 2 (ICON2)	003F ₁₆ 00₁₆
(13)	Port P4 pull-up control register (PULL4)	0014 ₁₆ 00₁₆	(46)	Processor status register	(PS) X X X X X 1 X X
(14)	Serial I/O2 control register 1 (SIO2CON1)	0015 ₁₆ 00₁₆	(47)	Program counter	(PC _H) FFFD₁₆ contents
(15)	Serial I/O2 control register 2 (SIO2CON2)	0016 ₁₆ 0 0 0 0 0 1 1 1			(PC _L) FFFC₁₆ contents
(16)	Serial I/O2 register (SIO2)	0017 ₁₆ X X X X X X X X	Note : X : Not fixed Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.		
(17)	Transmit/Receive buffer register (TB/RB)	0018 ₁₆ X X X X X X X X			
(18)	Serial I/O1 status register (SIOSTS)	0019 ₁₆ 1 0 0 0 0 0 0 0			
(19)	Serial I/O1 control register (SIOCON)	001A ₁₆ 00₁₆			
(20)	UART control register (UARTCON)	001B ₁₆ 1 1 1 0 0 0 0 0			
(21)	Baud rate generator (BRG)	001C ₁₆ X X X X X X X X			
(22)	PWM control register (PWMCON)	001D ₁₆ 00₁₆			
(23)	PWM prescaler (PREPWM)	001E ₁₆ X X X X X X X X			
(24)	PWM register (PWM)	001F ₁₆ X X X X X X X X			
(25)	Prescaler 12 (PRE12)	0020 ₁₆ FF₁₆			
(26)	Timer 1 (T1)	0021 ₁₆ 01₁₆			
(27)	Timer 2 (T2)	0022 ₁₆ 00₁₆			
(28)	Timer XY mode register (TM)	0023 ₁₆ 00₁₆			
(29)	Prescaler X (PREX)	0024 ₁₆ FF₁₆			
(30)	Timer X (TX)	0025 ₁₆ FF₁₆			
(31)	Prescaler Y (PREY)	0026 ₁₆ FF₁₆			
(32)	Timer Y (TY)	0027 ₁₆ FF₁₆			
(33)	Timer count source selection register (TCSS)	0028 ₁₆ 00₁₆			

Fig 41. Internal status at reset

CLOCK GENERATING CIRCUIT

The 3850 group (spec. A QzROM version) has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. (An external feed-back resistor may be needed depending on conditions.) However, an external feed-back resistor is needed between XCIN and XCOUT. Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

• Frequency Control

(1) Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset is released, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of XIN.

(3) Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

(4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1". When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.

The sub-clock XCIN-XCOUT oscillating circuit can not directly input clocks that are generated externally. Accordingly, make sure to cause an external resonator to oscillate.

<Note>

The internal reset may not be generated correctly in the middle-speed mode, depending on the underflow timing of the watchdog timer.

When using the watchdog timer, operate the MCU in any mode other than the middle-speed mode.

Oscillation Control

(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillation stops. When the oscillation stabilizing time set after STP instruction released bit (bit 0 of address 003816) is "0", the prescaler 12 is set to "FF16" and timer 1 is set to "0116". When the oscillation stabilizing time set after STP instruction released bit is "1", set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.

After STP instruction is released, the input of the prescaler 12 is connected to count source which had set at executing the STP instruction, and the output of the prescaler 12 is connected to timer 1. Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock ϕ is supplied for the first time, when timer 1 underflows. This ensures time for the clock oscillation using the ceramic resonators to be stabilized. When the oscillator is restarted by reset, apply "L" level to the RESET pin until the oscillation is stable since a wait time will not be generated.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that the interrupts will be received to release the STP or WIT state, their interrupt enable bits must be set to "1" before executing of the STP or WIT instruction.

When releasing the STP state, the input of the prescaler and timer 1 is connected to the count source which had set at executing the STP instruction and the prescaler 12 and timer 1 will start counting. Set the timer 1 interrupt enable bit to "0" before executing the STP instruction.

<Notes>

- If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after power on and at returning from the stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that $f(XIN) > 3 \times f(XCIN)$.
- When using the oscillation stabilizing time set after STP instruction released bit set to "1", evaluate time to stabilize oscillation of the used oscillator and set the value to the timer 1 and prescaler 12.

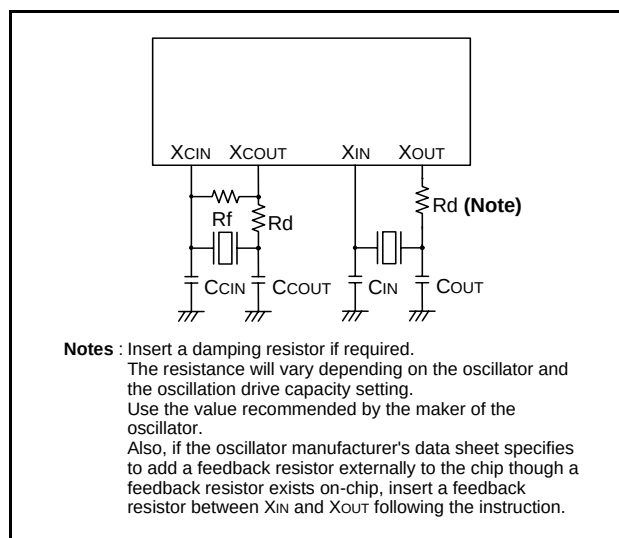


Fig 42. Ceramic resonator circuit

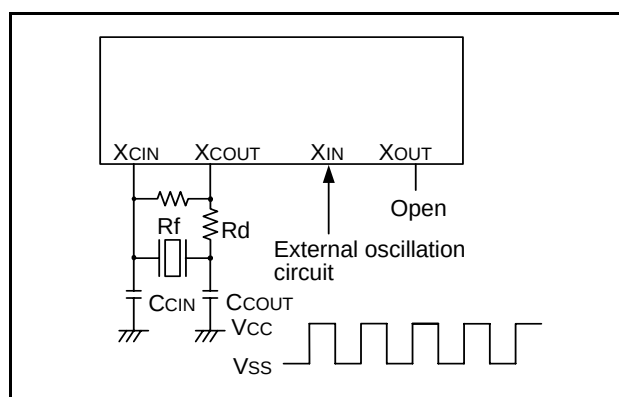


Fig 43. External clock input circuit

[MISRG (MISRG)] 003816

MISRG consists of three control bits (bits 1 to 3) for middle-speed mode automatic switch and one control bit (bit 0) for oscillation stabilizing time set after STP instruction released. By setting the middle-speed mode automatic switch start bit to "1" while operating in the low-speed mode and setting the middle-speed mode automatic switch set bit to "1", XIN oscillation automatically starts and the mode is automatically switched to the middle-speed mode.

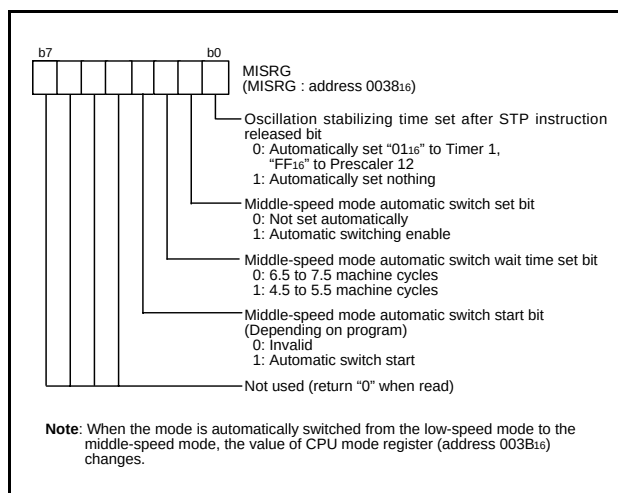


Fig 44. Structure of MISRG

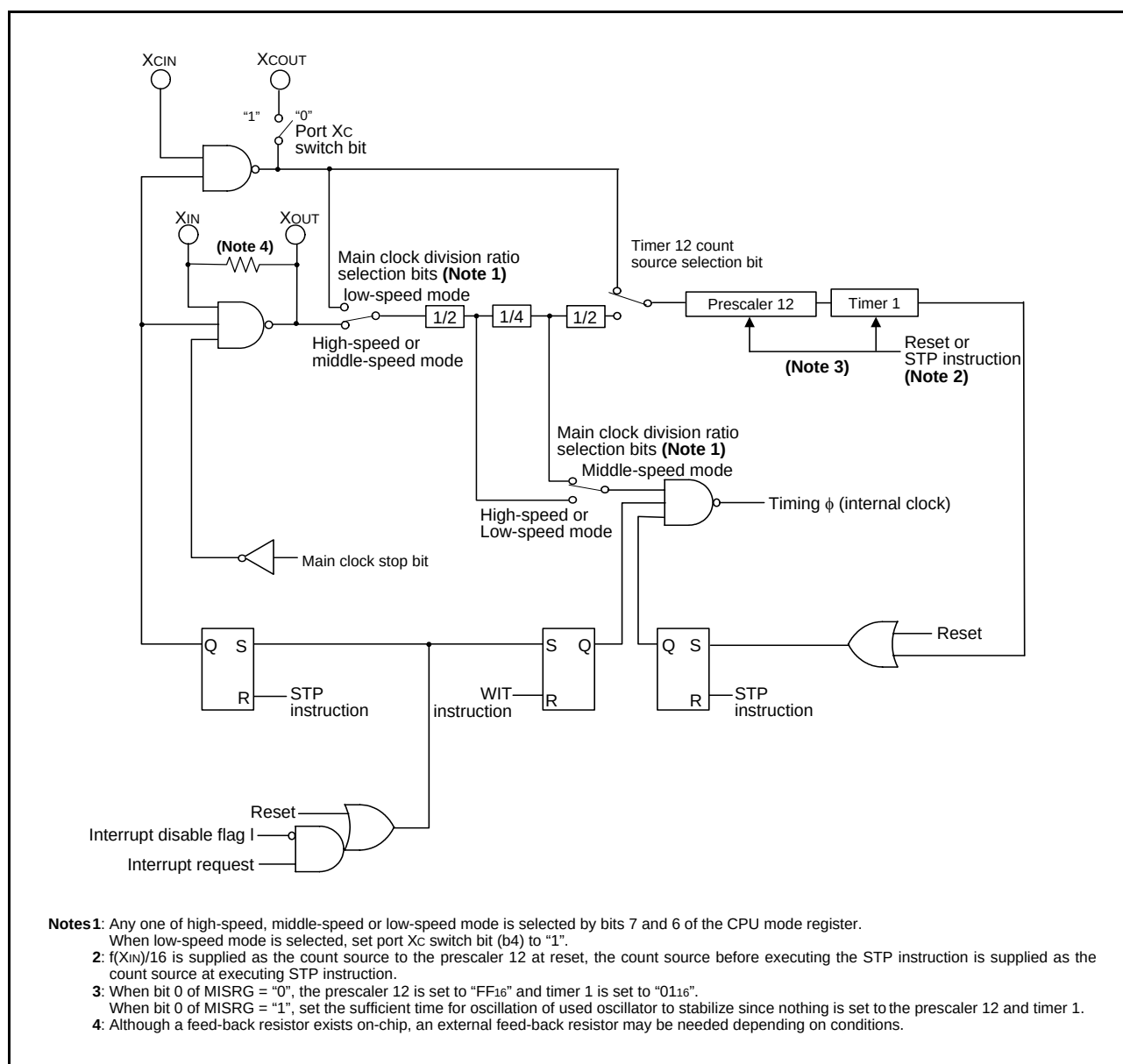


Fig 45. System clock generating circuit block diagram (Single-chip mode)

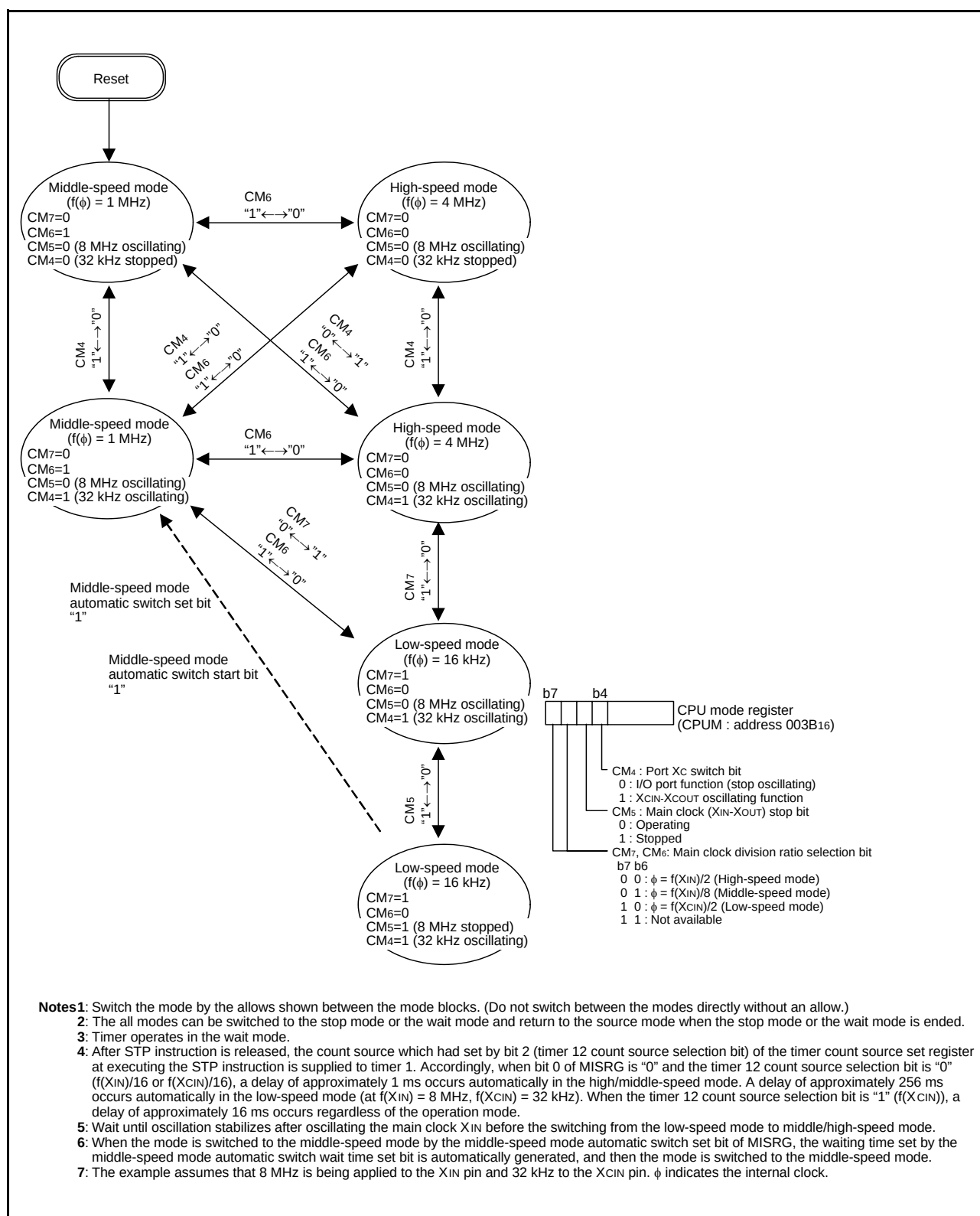


Fig 46. State transitions of system clock

ELECTRICAL CHARACTERISTICS**Absolute maximum ratings**

Table 9 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Power source voltage	All voltages are based on V _{SS} .	–0.3 to 6.5	V
V _I	Input voltage P00-P07, P10-P17, P20, P21, P24-P27, P30-P34, P40-P44, V _{REF}	When an input voltage is measured, output transistors are cut off.	–0.3 to V _{CC} + 0.3	V
V _I	Input voltage P22, P23		–0.3 to 5.8	V
V _I	Input voltage $\overline{\text{RESET}}$, X _{IN}		–0.3 to V _{CC} + 0.3	V
V _I	Input voltage CNV _{SS}		–0.3 to 8.0	V
V _O	Output voltage P00-P07, P10-P17, P20, P21, P24-P27, P30-P34, P40-P44, X _{OUT}		–0.3 to V _{CC} + 0.3	V
V _O	Output voltage P22, P23		–0.3 to 5.8	V
P _d	Power dissipation	T _a =25°C	1000 ⁽¹⁾	mW
T _{opr}	Operating temperature	–	–20 to 85	°C
T _{stg}	Storage temperature	–	–40 to 125	°C

NOTES:

1. The rating becomes 300mW at the PRSP0042GA-A/B package.

Recommended operating conditions

Table 10 Recommended operating conditions (1) ($V_{CC} = 1.8$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
Vcc	Power source voltage ⁽¹⁾	When start oscillating ⁽²⁾		2.0	5.0	5.5	V
		High-speed mode f(φ) = f(X _{IN})/2	f(X _{IN}) ≤ 12.5 MHz	4.0	5.0	5.5	V
			f(X _{IN}) ≤ 6.0 MHz	2.7	5.0	5.5	V
			f(X _{IN}) ≤ 4.2 MHz	2.2	5.0	5.5	V
			f(X _{IN}) ≤ 2.1 MHz	2.0	5.0	5.5	V
		Middle-speed mode f(φ) = f(X _{IN})/8	f(X _{IN}) ≤ 12.5 MHz	2.7	5.0	5.5	V
			f(X _{IN}) ≤ 8.4 MHz	2.2	5.0	5.5	V
			f(X _{IN}) ≤ 4.2 MHz	1.8	5.0	5.5	V
Low-speed mode f(φ) = f(X _{CIN})/2	f(X _{CIN}) ≤ 50 kHz	1.8	5.0	5.5	V		
Vss	Power source voltage				0		V
V _{IH}	“H” input voltage P00-P07, P10-P17, P20, P21, P24-P27, P30-P34, P40-P44	1.8 ≤ V _{CC} < 2.7 V		0.85 V _{CC}		V _{CC}	V
		2.7 ≤ V _{CC} < 5.5 V		0.8 V _{CC}		V _{CC}	
V _{IH}	“H” input voltage P22, P23	1.8 ≤ V _{CC} < 2.7 V		0.85 V _{CC}		5.8	V
		2.7 ≤ V _{CC} ≤ 5.5 V		0.8 V _{CC}		5.8	
V _{IH}	“H” input voltage RESET, X _{IN}	1.8 ≤ V _{CC} < 2.7 V		0.85 V _{CC}		V _{CC}	V
		2.7 ≤ V _{CC} ≤ 5.5 V		0.8 V _{CC}		V _{CC}	
V _{IH}	“H” input voltage CNV _{SS}	1.8 ≤ V _{CC} < 2.7 V		0.85 V _{CC}		8.0	V
		2.7 ≤ V _{CC} ≤ 5.5 V		0.8 V _{CC}		8.0	
V _{IL}	“L” input voltage P00-P07, P10-P17, P20, P21, P24-P27, P30-P34, P40-P44	1.8 ≤ V _{CC} < 2.7 V		0		0.16 V _{CC}	V
		2.7 ≤ V _{CC} ≤ 5.5 V		0		0.2 V _{CC}	
V _{IH}	“H” input voltage P22, P23	1.8 ≤ V _{CC} < 2.7 V		0		0.16 V _{CC}	V
		2.7 ≤ V _{CC} ≤ 5.5 V		0		0.2 V _{CC}	
V _{IL}	“L” input voltage RESET	1.8 ≤ V _{CC} < 2.7 V		0		0.16 V _{CC}	V
		2.7 ≤ V _{CC} ≤ 5.5 V		0		0.2 V _{CC}	
V _{IL}	“L” input voltage X _{IN}	1.8 ≤ V _{CC} < 2.7 V		0		0.16 V _{CC}	V
V _{IL}	“L” input voltage CNV _{SS}	1.8 ≤ V _{CC} < 2.7 V		0		0.16 V _{CC}	V
		2.7 ≤ V _{CC} ≤ 5.5 V		0		0.2 V _{CC}	
f(X _{IN})	Main clock input oscillation frequency ⁽³⁾	High-speed mode f(φ) = f(X _{IN})/2	4.0 ≤ V _{CC} ≤ 5.5 V			12.5	MHz
			2.7 ≤ V _{CC} ≤ 5.5 V			6.0	MHz
			2.2 ≤ V _{CC} ≤ 5.5 V			4.2	MHz
			2.0 ≤ V _{CC} ≤ 5.5 V			2.1	MHz
		Middle-speed mode f(φ) = f(X _{IN})/8	2.7 ≤ V _{CC} ≤ 5.5 V			12.5	MHz
			2.2 ≤ V _{CC} ≤ 5.5 V			8.4	MHz
1.8 ≤ V _{CC} ≤ 5.5 V				4.2	MHz		
f(X _{CIN})	Sub-clock input oscillation frequency ^(3, 4)				32.768	50	kHz

NOTES:

- When the A/D converter is used, refer to the recommended operating condition for A/D conversion.
- The start voltage and the start time for oscillation depend on the using oscillator, oscillation circuit constant value and operating temperature range, etc.. Particularly a high-frequency oscillator might require some notes in the low voltage operation.
- When the oscillation frequency has a duty cycle of 50%.
- When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

Table 11 Recommended operating conditions (2) ($V_{CC} = 1.8$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current ⁽¹⁾ P00-P07, P10-P17, P20, P21, P24-P27, P30-P34, P40-P44			-10	mA
$I_{OL(peak)}$	"L" peak output current ⁽¹⁾ P00-P07, P20-P27, P30-P34, P40-P44			10	mA
$I_{OL(peak)}$	"L" peak output current ⁽¹⁾ P10-P17			20	mA
$I_{OH(avg)}$	"H" average output current ⁽²⁾ P00-P07, P10-P17, P20, P21, P24-P27, P30-P34, P40-P44			-5	mA
$I_{OL(avg)}$	"L" average output current ⁽²⁾ P00-P07, P20-P27, P30-P34, P40-P44			5	mA
$I_{OL(avg)}$	"L" average output current ⁽²⁾ P10-P17			15	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current ⁽³⁾ P00-P07, P10-P17, P30-P34			-80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current ⁽³⁾ P20, P21, P24-P27, P40-P44,			-80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current ⁽³⁾ P00-P07, P30-P34			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current ⁽³⁾ P10-P17			120	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current ⁽³⁾ P20-P27, P40-P44			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current ⁽³⁾ P00-P07, P10-P17, P30-P34			-40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current ⁽³⁾ P20, P21, P24-P27, P40-P44			-40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current ⁽³⁾ P00-P07, P30-P34			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current ⁽³⁾ P10-P17			60	mA
$\Sigma I_{OL(avg)}$	"L" total average output current ⁽³⁾ P20-P27, P40-P44			40	mA

NOTES:

1. The peak output current is the peak current flowing in each port.
2. The average output current $I_{OL(avg)}$, $I_{OH(avg)}$ are average value measured over 100 ms.
3. The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Electrical characteristics

Table 12 Electrical characteristics (1) ($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{OH}	“H” output voltage ⁽¹⁾ P00-P07, P10-P17, P20, P21, P24-P27, P30-P34, P40-P44	I _{OH} = -10 mA 4.0 ≤ V _{CC} ≤ 5.5 V	V _{CC} - 2.0			V
		I _{OH} = -1.0 mA 1.8 ≤ V _{CC} ≤ 5.5 V	V _{CC} - 1.0			
V _{OL}	“L” output voltage P00-P07, P20-P27, P30-P34, P40-P44	I _{OL} = 10 mA 4.0 ≤ V _{CC} ≤ 5.5 V			2.0	V
		I _{OL} = 1.0 mA 1.8 ≤ V _{CC} ≤ 5.5 V			1.0	
V _{OL}	“L” output voltage P10-P17	I _{OL} = 20 mA 4.0 ≤ V _{CC} ≤ 5.5 V			2.0	V
		I _{OL} = 10 mA 2.7 ≤ V _{CC} ≤ 5.5 V			1.0	
		I _{OL} = 1.6 mA 1.8 ≤ V _{CC} ≤ 5.5 V			1.0	
V _{T+} - V _{T-}	Hysteresis CNTR0, CNTR1, INT0-INT3			0.4		V
V _{T+} - V _{T-}	Hysteresis RxD, SCLK1, SCLK2, SIN2			0.5		V
V _{T+} - V _{T-}	Hysteresis RESET			0.5		V
I _{IH}	“H” input current P00-P07, P10-P17, P20, P21, P24-P27, P30-P34, P40-P44	V _I = V _{CC} Pin floating, Pull-up Transistor “off”			5.0	μA
I _{IH}	“H” input current RESET, CNV _{SS}	V _I = V _{CC}			5.0	μA
I _{IH}	“H” input current X _{IN}	V _I = V _{CC}		4.0		μA
I _{IL}	“L” input current P00-P07, P10-P17, P20-P27, P30-P34, P40-P44	V _I = V _{SS} Pin floating, Pull-up Transistor “off”			-5.0	μA
I _{IL}	“L” input current RESET, CNV _{SS}	V _I = V _{SS}			-5.0	μA
I _{IL}	“L” input current X _{IN}	V _I = V _{SS}		-4.0		μA
I _{IL}	“L” input current (at Pull-up) P00-P07, P10-P17, P20, P21, P24-P27, P30-P34, P40-P44	V _I = V _{SS} V _{CC} = 5.0 V	-25	-60	-120	μA
		V _I = V _{SS} V _{CC} = 3.0 V	-8	-22	-40	μA
V _{RAM}	RAM hold voltage	When clock stopped	1.8			V

NOTES:

1. P25 is measured when the P25/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is “0”.

Table 13 Electrical characteristics (2) ($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I _{CC}	Power source current	High-speed mode ⁽¹⁾	f(X _{IN}) = 12.5 MHz f(X _{CIN}) = 32.768 kHz		6.0	13.0	mA
			f(X _{IN}) = 8.0 MHz f(X _{CIN}) = 32.768 kHz		4.3	10.0	mA
			f(X _{IN}) = 12.5 MHz (in WIT state) f(X _{CIN}) = 32.768 kHz		1.8	4.5	mA
			f(X _{IN}) = 8.0 MHz (in WIT state) f(X _{CIN}) = 32.768 kHz		1.4	4.2	mA
		Middle-speed mode ⁽¹⁾	f(X _{IN}) = 12.5 MHz f(X _{CIN}) = stopped		2.8	7.0	mA
			f(X _{IN}) = 8.0 MHz f(X _{CIN}) = stopped		2.0	6.5	mA
			f(X _{IN}) = 12.5 MHz (in WIT state) f(X _{CIN}) = stopped		1.8	4.2	mA
			f(X _{IN}) = 8.0 MHz (in WIT state) f(X _{CIN}) = stopped		1.3	4.0	mA
		Low-speed mode (V _{CC} = 5.0 V) ⁽¹⁾	f(X _{IN}) = stopped f(X _{CIN}) = 32.768 kHz		75	200	μA
			f(X _{IN}) = stopped f(X _{CIN}) = 32.768 kHz (in WIT state)		65	100	μA
		Low-speed mode (V _{CC} = 3.0 V) ⁽¹⁾	f(X _{IN}) = stopped f(X _{CIN}) = 32.768 kHz		15	55	μA
			f(X _{IN}) = stopped f(X _{CIN}) = 32.768 kHz (in WIT state)		10	20	μA
		Increment when A/D conversion is executed			300		μA
		All oscillation stopped (in STP state) ⁽¹⁾	T _a = 25 °C		0.1	1.0	μA
			T _a = 85 °C			10	μA

NOTES:

- Output transistors are cut off.

A/D converter recommended operating conditions

Table 14 A/D converter recommended operating conditions
 ($V_{CC} = 2.2$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (When A/D converter is used)		2.2	5.0	5.5	V
V_{REF}	A/D convert reference voltage		2.0		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage AN_0 - AN_8		AV_{SS}		V_{CC}	V
$f(X_{IN})$	Main clock input oscillation frequency (When A/D converter is used)	High-speed mode $f(\phi) = f(X_{IN})/2$	$4.0 \leq V_{CC} \leq 5.5$ V	0.5	12.5	MHz
			$2.7 \leq V_{CC} \leq 5.5$ V	0.5	6.0	MHz
			$2.2 \leq V_{CC} \leq 5.5$ V	0.5	4.2	MHz
		Middle-speed mode $f(\phi) = f(X_{IN})/8$	$2.7 \leq V_{CC} \leq 5.5$ V	0.5	12.5	MHz
			$2.2 \leq V_{CC} \leq 5.5$ V	0.5	8.4	MHz

A/D converter characteristics

Table 15 A/D converter characteristics
 ($V_{CC} = 2.2$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	bit
—	Absolute accuracy	$2.2 \leq V_{CC} < 2.7$ V			± 5	LSB
		$2.7 \leq V_{CC} \leq 5.5$ V			± 4	LSB
t_{CONV}	Conversion time	High-speed mode, Middle-speed mode			61	$2t_c(X_{IN})$
		Low-speed mode		40		μs
R_{LADDER}	Ladder resistor			35		k Ω
I_{VREF}	Reference power source input current	$V_{REF} = 5.0$ V V_{REF} "on"	50	150	200	μA
		$V_{REF} = 5.0$ V V_{REF} "off"			5.0	μA
$I_{I(AD)}$	A/D port input current			0.5	5.0	μA

Timing Requirements

Table 16 Timing requirements (1) ($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\overline{RESET})$	Reset input "L" pulse width	20			X_{IN} cycle
$t_c(X_{IN})$	External clock input cycle time	80			ns
$t_{WH}(X_{IN})$	External clock input "H" pulse width	32			ns
$t_{WL}(X_{IN})$	External clock input "L" pulse width	32			ns
$t_c(CNTR)$	CNTR0, CNTR1 input cycle time	200			ns
$t_{WH}(CNTR)$	CNTR0, CNTR1 input "H" pulse width	80			ns
$t_{WL}(CNTR)$	CNTR0, CNTR1 input "L" pulse width	80			ns
$t_{WH}(INT)$	INT0 to INT3 input "H" pulse width	80			ns
$t_{WL}(INT)$	INT0 to INT3 input "L" pulse width	80			ns
$t_c(SCLK1)$	Serial I/O1 clock input cycle time ⁽¹⁾	800			ns
$t_{WH}(SCLK1)$	Serial I/O1 clock input "H" pulse width ⁽¹⁾	370			ns
$t_{WL}(SCLK1)$	Serial I/O1 clock input "L" pulse width ⁽¹⁾	370			ns
$t_{su}(RxD-SCLK1)$	Serial I/O1 input setup time	220			ns
$t_h(SCLK1-RxD)$	Serial I/O1 input hold time	100			ns
$t_c(SCLK2)$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH}(SCLK2)$	Serial I/O2 clock input "H" pulse width	400			ns
$t_{WL}(SCLK2)$	Serial I/O2 clock input "L" pulse width	400			ns
$t_{su}(SIN2-SCLK2)$	Serial I/O2 clock input setup time	200			ns
$t_h(SCLK2-SIN2)$	Serial I/O2 clock input hold time	200			ns

NOTES:

- When $f(X_{IN}) = 8$ MHz and bit 6 of address 001A₁₆ is "1" (clock synchronous).
Divide this value by four when $f(X_{IN}) = 8$ MHz and bit 6 of address 001A₁₆ is "0" (UART).

Table 17 Timing requirements (2) ($V_{CC} = 2.7$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\overline{RESET})$	Reset input "L" pulse width	20			X_{IN} cycle
$t_c(X_{IN})$	External clock input cycle time	166			ns
$t_{WH}(X_{IN})$	External clock input "H" pulse width	66			ns
$t_{WL}(X_{IN})$	External clock input "L" pulse width	66			ns
$t_c(CNTR)$	CNTR0, CNTR1 input cycle time	500			ns
$t_{WH}(CNTR)$	CNTR0, CNTR1 input "H" pulse width	230			ns
$t_{WL}(CNTR)$	CNTR0, CNTR1 input "L" pulse width	230			ns
$t_{WH}(INT)$	INT0 to INT3 input "H" pulse width	230			ns
$t_{WL}(INT)$	INT0 to INT3 input "L" pulse width	230			ns
$t_c(SCLK1)$	Serial I/O1 clock input cycle time ⁽¹⁾	2000			ns
$t_{WH}(SCLK1)$	Serial I/O1 clock input "H" pulse width ⁽¹⁾	950			ns
$t_{WL}(SCLK1)$	Serial I/O1 clock input "L" pulse width ⁽¹⁾	950			ns
$t_{su}(RxD-SCLK1)$	Serial I/O1 input setup time	400			ns
$t_h(SCLK1-RxD)$	Serial I/O1 input hold time	200			ns
$t_c(SCLK2)$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH}(SCLK2)$	Serial I/O2 clock input "H" pulse width	950			ns
$t_{WL}(SCLK2)$	Serial I/O2 clock input "L" pulse width	950			ns
$t_{su}(SIN2-SCLK2)$	Serial I/O2 clock input setup time	400			ns
$t_h(SCLK2-SIN2)$	Serial I/O2 clock input hold time	300			ns

NOTES:

- When $f(X_{IN}) = 4$ MHz and bit 6 of address 001A₁₆ is "1" (clock synchronous).
Divide this value by four when $f(X_{IN}) = 4$ MHz and bit 6 of address 001A₁₆ is "0" (UART).

Switching characteristics

Table 18 Switching characteristics (1) ($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{WH}(SCLK1)$	Serial I/O1 clock output "H" pulse width	Fig. 47	$t_c(SCLK1)/2-30$			ns
$t_{WL}(SCLK1)$	Serial I/O1 clock output "L" pulse width		$t_c(SCLK1)/2-30$			ns
$t_d(SCLK1-TxD)$	Serial I/O1 output delay time ⁽¹⁾				140	ns
$t_v(SCLK1-TxD)$	Serial I/O1 output valid time ⁽¹⁾		-30			ns
$t_r(SCLK1)$	Serial I/O1 clock output rising time				30	ns
$t_f(SCLK1)$	Serial I/O1 clock output falling time				30	ns
$t_{WH}(SCLK2)$	Serial I/O2 clock output "H" pulse width		$t_c(SCLK2)/2-160$			ns
$t_{WL}(SCLK2)$	Serial I/O2 clock output "L" pulse width		$t_c(SCLK2)/2-160$			ns
$t_d(SCLK2-SOUT2)$	Serial I/O2 output delay time ⁽²⁾				200	ns
$t_v(SCLK2-SOUT2)$	Serial I/O2 output valid time ⁽²⁾		0			ns
$t_f(SCLK2)$	Serial I/O2 clock output falling time				30	ns
$t_r(CMOS)$	CMOS output rising time ⁽³⁾			10	30	ns
$t_f(CMOS)$	CMOS output falling time ⁽³⁾			10	30	ns

NOTES:

1. When the P25/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B₁₆) is "0".
2. When the P01/SOUT2 and P02/SCLK2 P-channel output disable bit of the Serial I/O2 control register 1 (bit 7 of address 0015₁₆) is "0".
3. The XOUT pin is excluded.

Table 19 Switching characteristics (2) ($V_{CC} = 2.7$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{WH}(SCLK1)$	Serial I/O1 clock output "H" pulse width	Fig. 47	$t_c(SCLK1)/2-50$			ns
$t_{WL}(SCLK1)$	Serial I/O1 clock output "L" pulse width		$t_c(SCLK1)/2-50$			ns
$t_d(SCLK1-TxD)$	Serial I/O1 output delay time ⁽¹⁾				350	ns
$t_v(SCLK1-TxD)$	Serial I/O1 output valid time ⁽¹⁾		-30			ns
$t_r(SCLK1)$	Serial I/O1 clock output rising time				50	ns
$t_f(SCLK1)$	Serial I/O1 clock output falling time				50	ns
$t_{WH}(SCLK2)$	Serial I/O2 clock output "H" pulse width		$t_c(SCLK2)/2-240$			ns
$t_{WL}(SCLK2)$	Serial I/O2 clock output "L" pulse width		$t_c(SCLK2)/2-240$			ns
$t_d(SCLK2-SOUT2)$	Serial I/O2 output delay time ⁽²⁾				400	ns
$t_v(SCLK2-SOUT2)$	Serial I/O2 output valid time ⁽²⁾		0			ns
$t_f(SCLK2)$	Serial I/O2 clock output falling time				50	ns
$t_r(CMOS)$	CMOS output rising time ⁽³⁾			20	50	ns
$t_f(CMOS)$	CMOS output falling time ⁽³⁾			20	50	ns

NOTES:

1. When the P25/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B₁₆) is "0".
2. When the P01/SOUT2 and P02/SCLK2 P-channel output disable bit of the Serial I/O2 control register 1 (bit 7 of address 0015₁₆) is "0".
3. The XOUT pin is excluded.

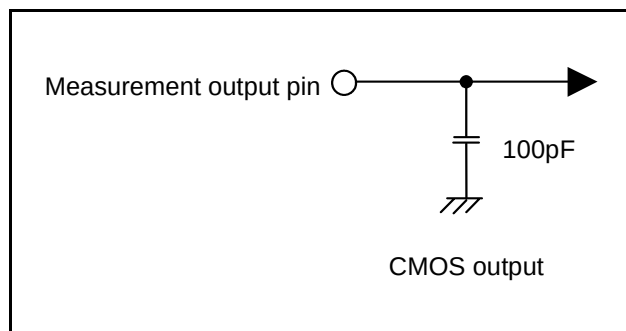


Fig 47. Circuit for measuring output switching characteristics

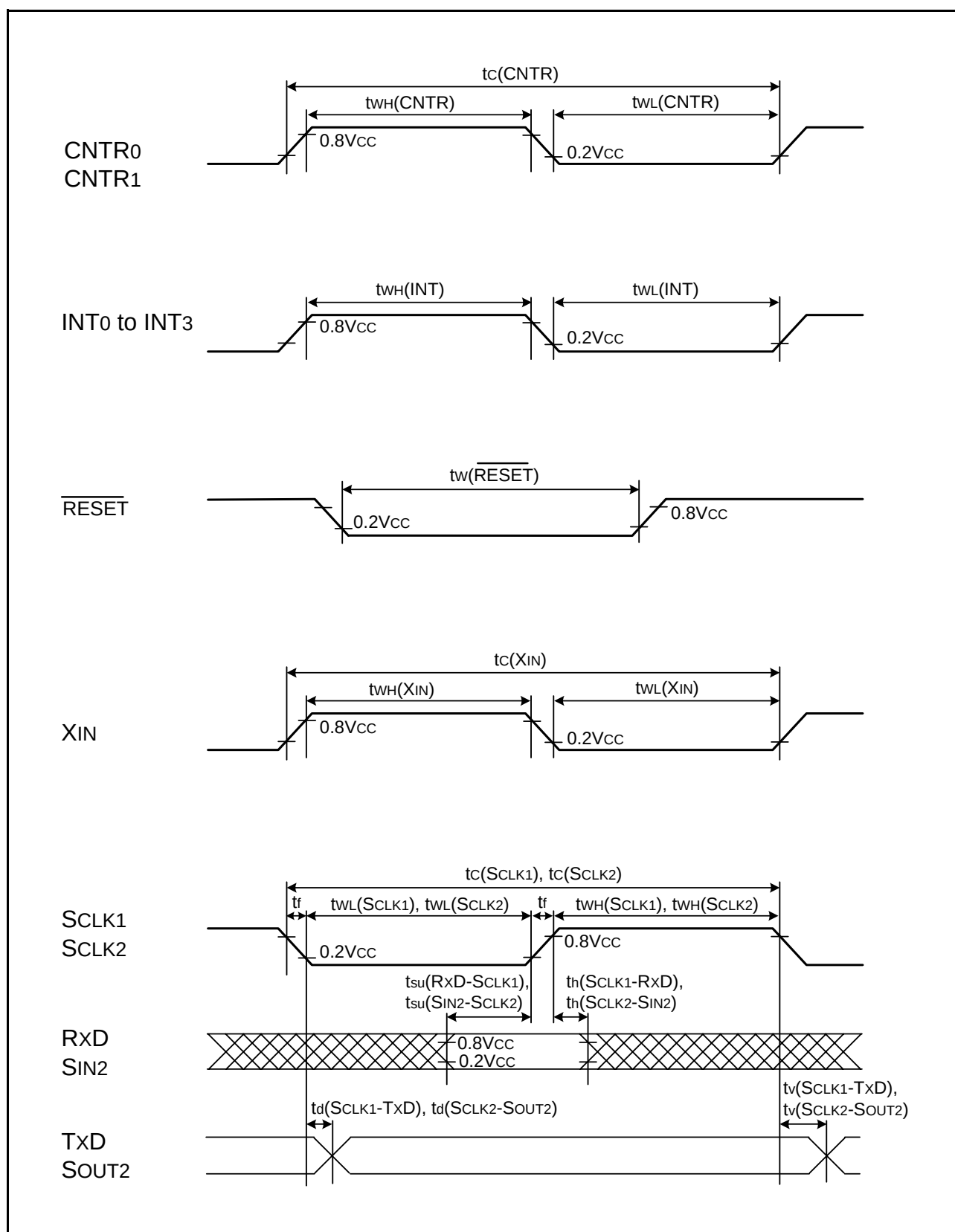
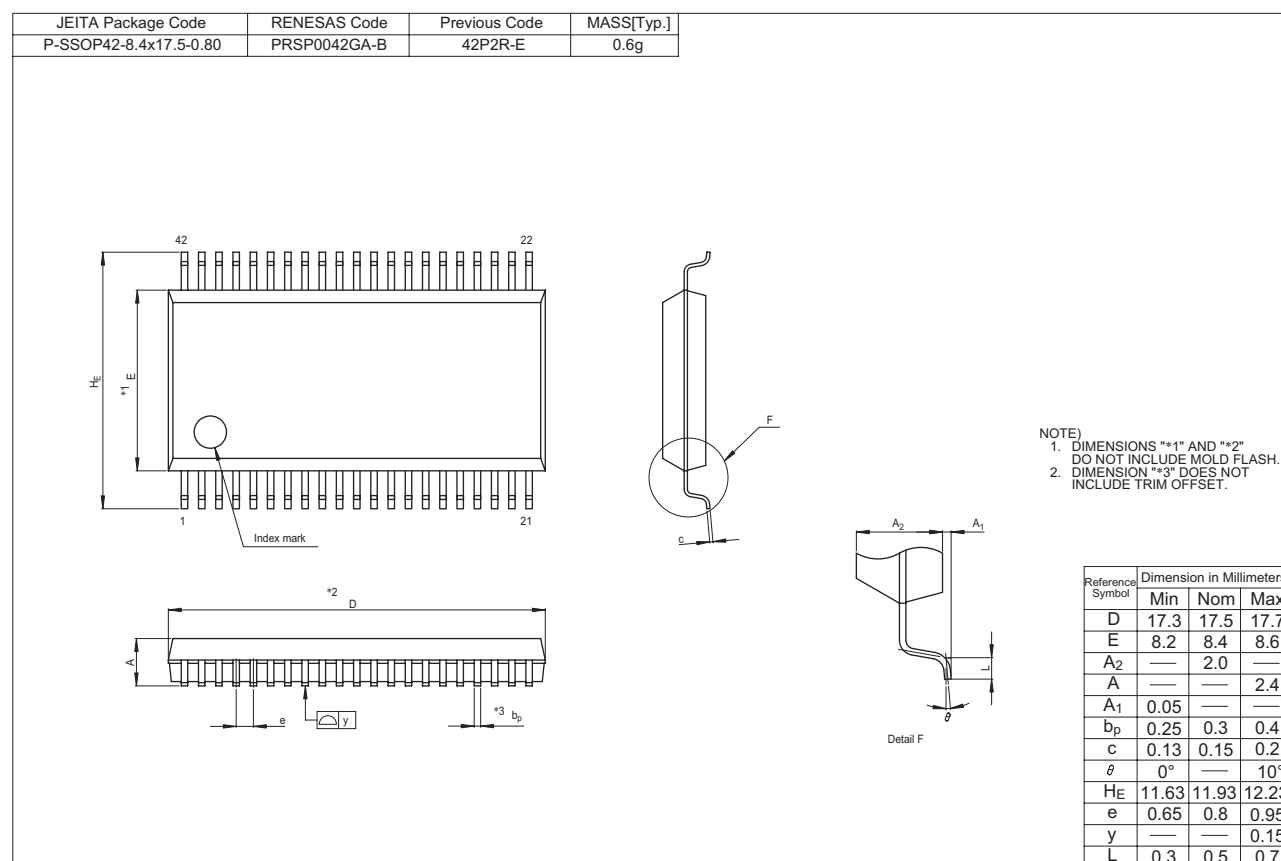
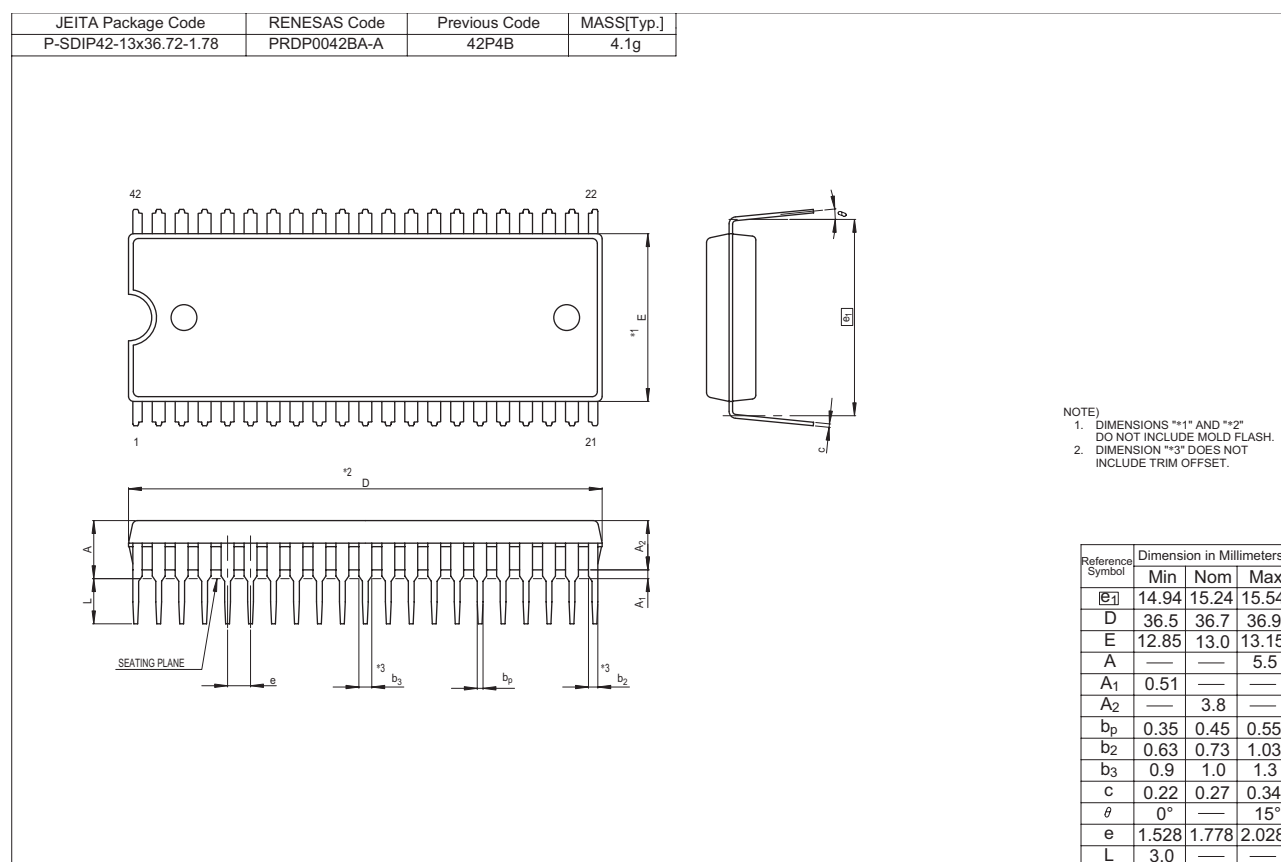


Fig 48. Timing diagram

PACKAGE OUTLINE

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.



APPENDIX

NOTES ON PROGRAMMING

1. Processor Status Register

(1) Initializing of processor status register

Flags which affect program execution must be initialized after a reset.

In particular, it is essential to initialize the T and D flags because they have an important effect on calculations.

<Reason>

After a reset, the contents of the processor status register (PS) are undefined except for the I flag which is "1".

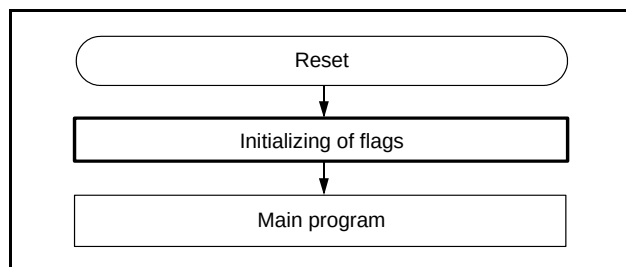


Fig 49. Initialization of processor status register

(2) How to reference the processor status register

To reference the contents of the processor status register (PS), execute the PHP instruction once then read the contents of (S+1). If necessary, execute the PLP instruction to return the PS to its original status.

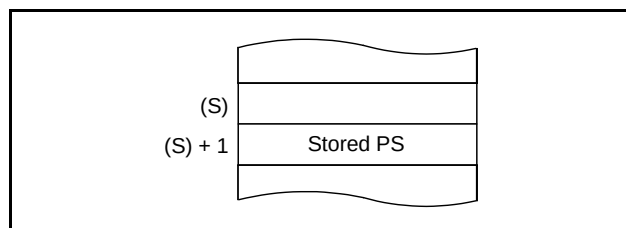


Fig 50. Stack memory contents after PHP instruction execution

2. BRK instruction

(1) Interrupt priority level

When the BRK instruction is executed with the following conditions satisfied, the interrupt execution is started from the address of interrupt vector which has the highest priority.

- Interrupt request bit and interrupt enable bit are set to "1".
- Interrupt disable flag (I) is set to "1" to disable interrupt.

3. Decimal calculations

(1) Execution of decimal calculations

The ADC and SBC are the only instructions which will yield proper decimal notation, set the decimal mode flag (D) to "1" with the SED instruction. After executing the ADC or SBC instruction, execute another instruction before executing the SEC, CLC, or CLD instruction.

(2) Notes on status flag in decimal mode

When decimal mode is selected, the values of three of the flags in the status register (the N, V, and Z flags) are invalid after a ADC or SBC instruction is executed.

The carry flag (C) is set to "1" if a carry is generated as a result of the calculation, or is cleared to "0" if a borrow is generated. To determine whether a calculation has generated a carry, the C flag must be initialized to "0" before each calculation. To check for a borrow, the C flag must be initialized to "1" before each calculation.

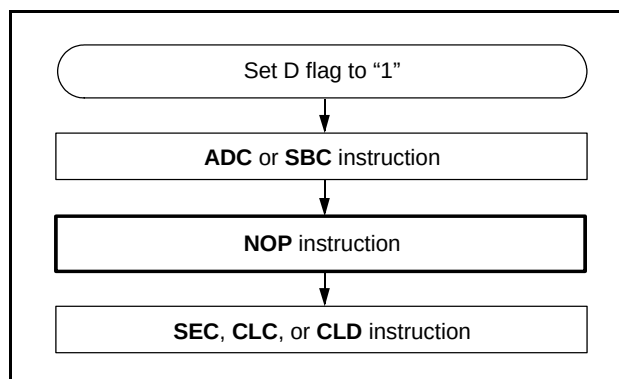


Fig 51. Execution of decimal calculations

4. JMP instruction

When using the JMP instruction in indirect addressing mode, do not specify the last address on a page as an indirect address.

5. Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

6. Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

7. Instruction Execution Time

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the 740 Family Software Manual.

The frequency of the internal clock ϕ is the twice the X_{IN} cycle in high-speed mode, 8 times the X_{IN} cycle in middle-speed mode, and the twice the X_{CIN} in low-speed mode.

8. Reserved Area, Reserved Bit

Do not write any data to the reserved area in the SFR area and the special page. (Do not change the contents after reset.)

9. CPU Mode Register

Be sure to fix bit 3 of the CPU mode register (address 003B16) to "1".

NOTES ON PERIPHERAL FUNCTIONS**Notes on Input and Output Ports****1. Notes in standby state**

In standby state*1, do not make input levels of an I/O port “undefined”, especially for I/O ports of the N-channel open-drain. When setting the N-channel open-drain port as an output, do not make input levels of an I/O port “undefined”, too.

Pull-up (connect the port to VCC) or pull-down (connect the port to VSS) these ports through a resistor.

When determining a resistance value, note the following points:

- External circuit
- Variation of output levels during the ordinary operation

<Reason>

When setting as an input port with its direction register, the transistor becomes the OFF state, which causes the ports to be the high-impedance state.

Accordingly, the potential which is input to the input buffer in a microcomputer is unstable in the state that input levels of an I/O port are “undefined”. This may cause power source current.

In I/O ports of N-channel open-drain, when the contents of the port latch are “1”, even if it is set as an output port with its direction register, it becomes the same phenomenon as the case of an input port.

NOTES:

4. Standby state: stop mode by executing STP instruction
wait mode by executing WIT instruction

2. Modifying output data with bit managing instruction

When the port latch of an I/O port is modified with the bit managing instruction*2, the value of the unspecified bit may be changed.

<Reason>

The bit managing instructions are read-modify-write form instructions for reading and writing data by a byte unit. Accordingly, when these instructions are executed on a bit of the port latch of an I/O port, the following is executed to all bits of the port latch.

- As for bit which is set for input port:
The pin state is read in the CPU, and is written to this bit after bit managing.
- As for bit which is set for output port:
The bit value is read in the CPU, and is written to this bit after bit managing.

Note the following:

- Even when a port which is set as an output port is changed for an input port, its port latch holds the output data.
- As for a bit of which is set for an input port, its value may be changed even when not specified with a bit managing instruction in case where the pin state differs from its port latch contents.

NOTES:

5. Bit managing instructions: SEB and CLB instructions

Termination of Unused Pins**1. Terminate unused pins**

(1) I/O ports:

- Set the I/O ports for the input mode and connect them to VCC or VSS through each resistor of 1 kΩ to 10 kΩ. In the port which can select a internal pull-up resistor, the internal pull-up resistor can be used.

Set the I/O ports for the output mode and open them at “L” or “H”.

- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

(2) The AVSS pin when not using the A/D converter:

- When not using the A/D converter, handle a power source pin for the A/D converter, AVSS pin as follows:
AVSS: Connect to the VSS pin.

2. Termination remarks

(1) Input ports and I/O ports:

Do not open in the input mode.

<Reason>

- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination (1) in 1 shown on the above.

(2) I/O ports:

When setting for the input mode, do not connect to VCC or VSS directly.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between a port and VCC (or VSS).

(3) I/O ports:

When setting for the input mode, do not connect multiple ports in a lump to VCC or VSS through a resistor.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

- At the termination of unused pins, perform wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

Notes on Interrupts

1. Change of relevant register settings

When the setting of the following registers or bits is changed, the interrupt request bit may be set to "1". When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

- Interrupt edge selection register (address 003A16)
- Timer XY mode register (address 002316)

Set the above listed registers or bits as the following sequence.

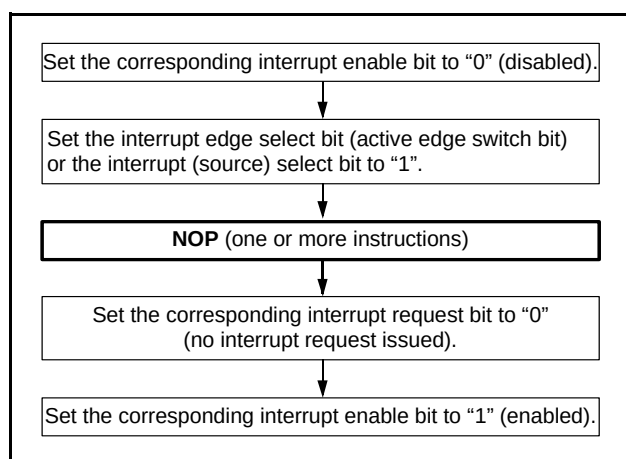


Fig 52. Sequence of changing relevant register

<Reason>

When setting the followings, the interrupt request bit may be set to "1".

- When setting external interrupt active edge
Concerned register: Interrupt edge selection register (address 003A16)
Timer XY mode register (address 002316)
- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated.
Concerned register: Interrupt edge selection register (address 003A16)

2. Check of interrupt request bit

When executing the BBC or BBS instruction to an interrupt request bit of an interrupt request register immediately after this bit is set to "0" by using a data transfer instruction, execute one or more instructions before executing the BBC or BBS instruction.

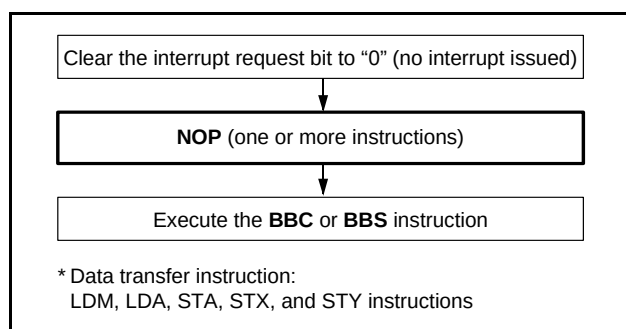


Fig 53. Sequence of check of interrupt request bit

<Reason>

If the BBC or BBS instruction is executed immediately after an interrupt request bit of an interrupt request register is cleared to "0", the value of the interrupt request bit before being cleared to "0" is read.

3. Interrupt Request Register 1

Be sure to fix bits 1 and 5 of the Interrupt request register 1 (address 003C16) to "0".

Notes on Timer

- If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.
- When switching the count source by the timer 12, X and Y count source selection bits, the value of timer count is altered in unconsiderable amount owing to generating of thin pulses in the count input signals.
Therefore, select the timer count source before set the value to the prescaler and the timer.

Notes on Serial Interface

1. Notes when selecting clock synchronous serial I/O (Serial I/O1)

(1) Stop of transmission operation

Clear the serial I/O1 enable bit and the transmit enable bit to "0" (Serial I/O1 and transmit disabled).

<Reason>

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to "0" (Serial I/O1 disabled), the internal transmission is running (in this case, since pins TxD, RxD, SCLK1, and $\overline{\text{SRDY1}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

(2) Stop of receive operation

Clear the receive enable bit to "0" (receive disabled), or clear the serial I/O1 enable bit to "0" (Serial I/O1 disabled).

(3) Stop of transmit/receive operation

Clear the transmit enable bit and receive enable bit to "0" simultaneously (transmit and receive disabled).
(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

<Reason>

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.

In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to "0" (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O1 enable bit to "0" (Serial I/O1 disabled) (refer to (1) in 1).

(4) $\overline{\text{SRDY1}}$ output of reception side (Serial I/O1)

When signals are output from the $\overline{\text{SRDY1}}$ pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the $\overline{\text{SRDY1}}$ output enable bit, and the transmit enable bit to "1" (transmit enabled).

2. Notes when selecting clock asynchronous serial I/O (Serial I/O1)

(1) Stop of transmission operation

Clear the transmit enable bit to "0" (transmit disabled).

<Reason>

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to "0" (Serial I/O1 disabled), the internal transmission is running (in this case, since pins TxD, RxD, SCLK1, and $\overline{\text{SRDY1}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

(2) Stop of receive operation

Clear the receive enable bit to "0" (receive disabled).

(3) Stop of transmit/receive operation

Only transmission operation is stopped.

Clear the transmit enable bit to "0" (transmit disabled).

<Reason>

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to "0" (Serial I/O1 disabled), the internal transmission is running (in this case, since pins TxD, RxD, SCLK1, and $\overline{\text{SRDY1}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

Only receive operation is stopped.

Clear the receive enable bit to "0" (receive disabled).

3. Setting serial I/O1 control register again (Serial I/O1)

Set the serial I/O1 control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to "0".

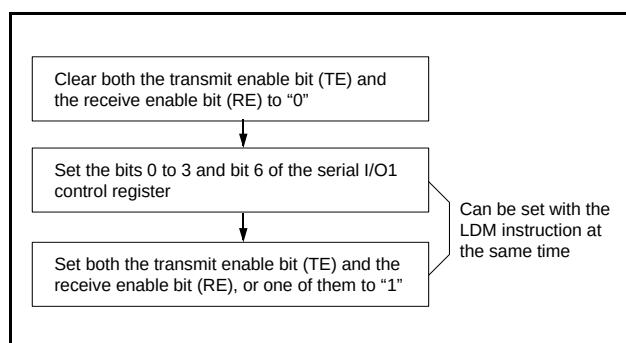


Fig 54. Sequence of setting serial I/O1 control register again

4. Data transmission control with referring to transmit shift register completion flag (Serial I/O1)

The transmit shift register completion flag changes from "1" to "0" with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

5. Transmit interrupt request when transmit enable bit is set (Serial I/O1)

When the transmit interrupt is used, set the transmit interrupt enable bit to transmit enabled as shown in the following sequence.

- (1) Set the interrupt enable bit to "0" (disabled) with CLB instruction.
- (2) Prepare serial I/O for transmission/reception.
- (3) Set the interrupt request bit to "0" with CLB instruction after 1 or more instruction has been executed.
- (4) Set the interrupt enable bit to "1" (enabled).

<Reason>

When the transmission enable bit is set to "1", the transmit buffer empty flag and transmit shift register completion flag are set to "1".

The interrupt request is generated and the transmission interrupt request bit is set regardless of which of the two timings listed below is selected as the timing for the transmission interrupt to be generated.

- Transmit buffer empty flag is set to "1"
- Transmit shift register completion flag is set to "1"

6. Transmission control when external clock is selected (Serial I/O1 clock synchronous mode)

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to "1" at "H" of the SCLK1 input level. Also, write the transmit data to the transmit buffer register (serial I/O shift register) at "H" of the SCLK1 input level.

7. Transmit data writing (Serial I/O2)

In the clock synchronous serial I/O, when selecting an external clock as synchronous clock, write the transmit data to the serial I/O2 register (serial I/O shift register) at "H" of the transfer clock input level.

Notes on PWM

The PWM starts after the PWM enable bit is set to enable and "L" level is output from the PWM pin.

The length of this "L" level output is as follows:

$$\frac{n+1}{2 \times f(\text{XIN})} \quad (\text{s}) \quad \begin{array}{l} \text{(Count source selection bit = "0",} \\ \text{where n is the value set in the prescaler)} \end{array}$$

$$\frac{n+1}{f(\text{XIN})} \quad (\text{s}) \quad \begin{array}{l} \text{(Count source selection bit = "1",} \\ \text{where n is the value set in the prescaler)} \end{array}$$

Notes on A/D Converter

1. Analog input pin

Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01 μF to 1 μF . Further, be sure to verify the operation of application products on the user side.

<Reason>

An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A/D conversion precision to be worse.

2. A/D converter power source pin

The AVSS pin is A/D converter power source pin. Regardless of using the A/D conversion function or not, connect it as following:

- AVSS: Connect to the VSS line

<Reason>

If the AVSS pin is opened, the microcomputer may have a failure because of noise or others.

3. Clock frequency during A/D conversion

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. Thus, make sure the following during an A/D conversion.

- $f(\text{XIN})$ is 500 kHz or more in middle-/high-speed mode.
- Do not execute the STP instruction.
- When the A/D converter is operated at low-speed mode, $f(\text{XIN})$ do not have the lower limit of frequency, because of the A/D converter has a built-in self-oscillation circuit.

4. AD Input Selection Register

Be sure to fix bits 5 and 7 of the AD input selection register (address 0037₁₆) to “0”.

Notes on Watchdog Timer

- Make sure that the watchdog timer does not underflow while waiting Stop release, because the watchdog timer keeps counting during that term.
- When the STP instruction function selection bit has been set to “1”, it is impossible to switch it to “0” by a program.
- The watchdog timer cannot be used in the middle-speed mode. (The internal reset may not be generated correctly, depending on the underflow timing of the watchdog timer.)

Notes on RESET Pin

1. Connecting capacitor

In case where the RESET signal rise time is long, connect a ceramic capacitor or others across the RESET pin and the VSS pin. Use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following:

- Make the length of the wiring which is connected to a capacitor as short as possible.
- Be sure to verify the operation of application products on the user side.

<Reason>

If the several nanosecond or several ten nanosecond impulse noise enters the RESET pin, it may cause a microcomputer failure.

2. Reset release after power on

When releasing the reset after power on, such as power-on reset, release reset after XIN passes more than 20 cycles in the state where the power supply voltage is 1.8 V or more and the XIN oscillation is stable.

<Reason>

To release reset, the RESET pin must be held at an “L” level for 20 cycles or more of XIN in the state where the power source voltage is between 1.8 V and 5.5 V, and XIN oscillation is stable.

Notes on Using Stop Mode

1. Register setting

Since values of the prescaler 12 and Timer 1 are automatically reloaded when returning from the stop mode, set them again, respectively. (When the oscillation stabilizing time set after STP instruction released bit is “0”)

When using the oscillation stabilizing time set after STP instruction released bit set to “1”, evaluate time to stabilize oscillation of the used oscillator and set the value to the timer 1 and prescaler 12.

2. Clock restoration

After restoration from the stop mode to the normal mode by an interrupt request, the contents of the CPU mode register previous to the STP instruction execution are retained. Accordingly, if both main clock and sub clock were oscillating before execution of the STP instruction, the oscillation of both clocks is resumed at restoration.

In the above case, when the main clock side is set as a system clock, the oscillation stabilizing time for approximately 8,000 cycles of the XIN input is reserved at restoration from the stop mode. At this time, note that the oscillation on the sub clock side may not be stabilized even after the lapse of the oscillation stabilizing time of the main clock side.

Notes on Wait Mode

- Clock restoration

If the wait mode is released by a reset when XCIN is set as the system clock and XIN oscillation is stopped during execution of the WIT instruction, XCIN oscillation stops, XIN oscillations starts, and XIN is set as the system clock.

In the above case, the RESET pin should be held at “L” until the oscillation is stabilized.

Notes on Restarting Oscillation

- Restarting oscillation

Usually, when the MCU stops the clock oscillation by STP instruction and the STP instruction has been released by an external interrupt source, the fixed values of Timer 1 and Prescaler 12 (Timer 1 = “01₁₆”, Prescaler 12 = “FF₁₆”) are automatically reloaded in order for the oscillation to stabilize. The user can inhibit the automatic setting by writing “1” to bit 0 of MISRG (address 0038₁₆).

However, by setting this bit to “1”, the previous values, set just before the STP instruction was executed, will remain in Timer 1 and Prescaler 12. Therefore, you will need to set an appropriate value to each register, in accordance with the oscillation stabilizing time, before executing the STP instruction.

<Reason>

Oscillation will restart when an external interrupt is received. However, internal clock ϕ is supplied to the CPU only when Timer 1 starts to underflow. This ensures time for the clock oscillation using the ceramic resonators to be stabilized.

Handling of Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (VCC pin) and GND pin (VSS pin) and between power source pin (VCC pin) and analog power source input pin (AVSS pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of $0.01\ \mu\text{F}$ – $0.1\ \mu\text{F}$ is recommended.

Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.

In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the power source voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

Electric Characteristic Differences Between Flash Memory, Mask ROM and QzROM Version MCUs

There are differences in the manufacturing processes and the mask pattern among flash memory, mask ROM, and QzROM version MCUs due to the differences of the ROM type. Even when the ROM type is the same, when the memory size is different, the manufacturing processes and the mask pattern differ. For these reasons, the oscillation circuit constants and the characteristics such as a characteristic value, operation margin, noise immunity, and noise radiation within the limits of electrical characteristics may differ.

When manufacturing an application system, please perform sufficient evaluations in each product. Especially, when switching a product (example: change from the mask ROM version to QzROM version), please perform sufficient evaluations by the switching product in the stage before mass-producing an application system.

Product Shipped in Blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur. Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

QzROM Version

Connect the CNVSS/VPP pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer. In addition connecting an approximately $5\ \text{k}\Omega$ resistor in series to the GND could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer.

• Reason

The CNVSS/VPP pin is the power source input pin for the built-in QzROM. When programming in the QzROM, the impedance of the VPP pin is low to allow the electric current for writing to flow into the built-in QzROM. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal instruction codes or data are read from the QzROM, which may cause a program runaway.

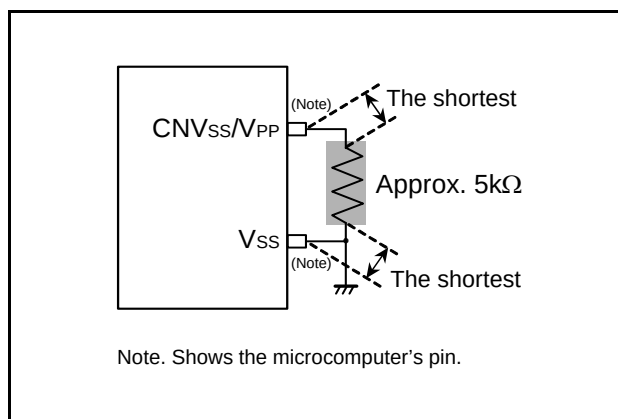


Fig 55. Wiring for the CNVSS/VPP

Notes On QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .mask) which is made by the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "0016" and "FF16" can not be accepted.
- Set "FF16" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF16" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

DATA REQUIRED FOR QzROM WRITING ORDERS

The following are necessary when ordering a QzROM product shipped after writing:

1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (<http://www.renesas.com/homepage.jsp>). Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

REVISION HISTORY	3850 Group (Spec.A QzROM version) Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Dec. 10, 2004	–	First edition issued
		–	<Updating from Shortsheet (REJ03B0123-0100Z; Rev.1.00)>
		1	- Power source voltage is revised. - Power dissipation is partly revised. APPLICATION is partly deleted.
		5	Table 2 is partly added. Note of Table 2 is added.
2.00	Sep. 09, 2005	–	Delete the following: "PRELIMINARY"
		1, 4-6	Package name of 42P4B is revised. 42P4B → PRDP0042BA-A
		3	Table 1 is partly revised.
		4	Fig.3 is partly revised.
		6	Table 4 is partly revised.
			Notes on differences among 3850 group (standard), 3850 group (spec.H), and 3850 group
		11	ROM Code Protect Address (address FFDB₁₆) is added. Fig.8 is partly revised.
		12	Fig.9 is partly revised.
		13	Table 7 is partly revised.
		16	Fig.12 is partly revised.
		35	WATCHDOG TIMER is revised.
			Fig.38 is partly revised.
		38	Oscillation Control (1) Stop mode is partly revised.
		41	Reserved Area is revised. Reserved Area → Reserved Area, Reserved bit
		42	The followings are added; Flash Memory Version / QzROM Version is deleted.
		43	Table 9 is partly revised.
		53	PACKAGE OUTLINE of 42P4B is revised.
2.01	Oct. 13, 2005	5	Note 1 of Table 2 is partly revised.
		11	ROM Code Protect Address (address FFDB₁₆) is partly revised.
		42	Notes On QzROM Writing Orders, Notes On ROM Code Protect are partly revised.
2.10	Nov. 14, 2005	35	Fig 37. Block diagram of Watchdog timer;
		42	QzROM version; approximately 1 k to 5 kΩ resistor → approximately 5 kΩ resistor
		53	Package Outline is revised
		54-59	Appendix added
2.11	Dec. 19, 2008	1,4-6,43	Package name of 42P2R-A/E is revised. 42P2R-A/E → PRSP0042GA-A/B
		11	Fig.8 is partly revised.
		35	Initial value of watchdog timer is partly added. When bit 7 of the watchdog timer control register is "0": 65.536ms at X _{IN} = 16MHz frequency.→ 83.886ms at X _{IN} = 12.5 MHz frequency. "1": 256μs at X _{IN} = 16MHz frequency.→ 327.68μs at X _{IN} = 12.5 MHz frequency.

REVISION HISTORY	3850 Group (Spec.A QzROM version) Data Sheet
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Rev.	Date	Description	
		Page	Summary
2.11	Dec. 19, 2008	38	(2) Wait mode is partly revised.
		41-42	Deleted
		55	the STP instruction disable bit → the STP instruction function selection bit
		56	Notes On QzROM Writing Orders is revised.
2.13	Apr. 17, 2009	–	"MAEC TECHNICAL NEWS" reflected: M740-33-0211
		35	Note 2 added
		38	• Frequency Control <Note> added
		56	Notes on Watchdog Timer revised

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