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April 1st, 2010
Renesas Electronics Corporation

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7544 Group (QzROM version)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0108-0103
Rev.1.03
Mar 31, 2009

DESCRIPTION

The 7544 Group is the 8-bit microcomputer based on the 740 family core technology.

The 7544 Group has a serial interface, 8-bit timers, a 16-bit timer, and an A/D converter, and is useful for control of home electric appliances and office automation equipment.

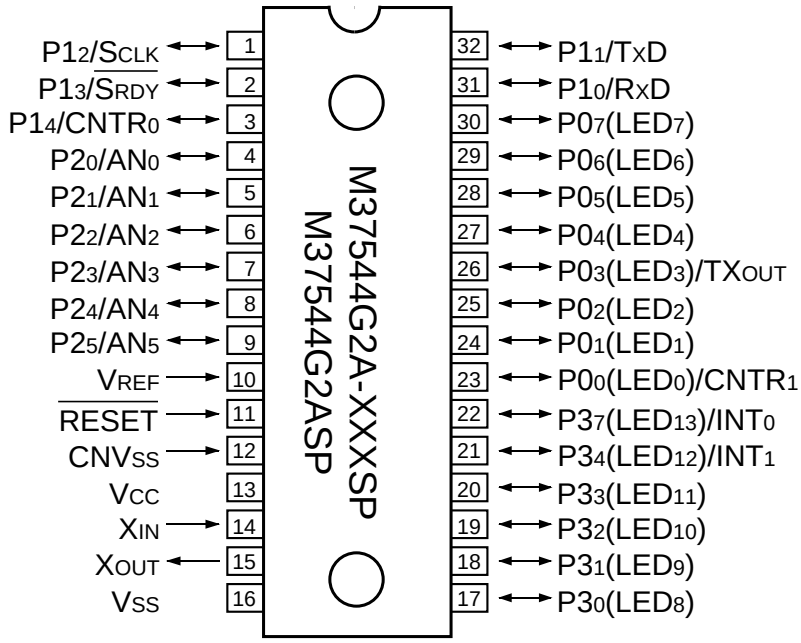
FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.25 µs
  (at 8 MHz oscillation frequency, double-speed mode for the shortest instruction)
- Memory size ROM ..... 8 K bytes
  RAM ..... 256 bytes
- Programmable I/O ports 25
- Interrupts ..... 12 sources, 12 vectors
- Timers ..... 8-bit × 2
  ..... 16-bit × 1
- Serial interface ..... 8-bit × 1 (UART or Clock-synchronized)
- A/D converter ..... 8-bit × 6 channels
- Clock generating circuit ..... Built-in type
  (low-power dissipation by an on-chip oscillator enabled)
  (connect to external ceramic resonator or quartz-crystal oscillator permitting RC oscillation)
- Watchdog timer ..... 16-bit × 1
- Power source voltage
  XIN oscillation frequency at ceramic/quartz-crystal oscillation, in double-speed mode
  At 8 MHz ..... 4.5 to 5.5 V
  At 4 MHz ..... 4.0 to 5.5 V
  At 2 MHz ..... 2.4 to 5.5 V
  At 1 MHz ..... 2.2 to 5.5 V
  XIN oscillation frequency at ceramic/quartz-crystal oscillation, in high-speed mode
  At 8 MHz ..... 4.0 to 5.5 V
  At 4 MHz ..... 2.4 to 5.5 V
  At 2 MHz ..... 2.2 to 5.5 V
  XIN oscillation frequency at RC oscillation
  At 4 MHz ..... 4.0 to 5.5 V
  At 2 MHz ..... 2.4 to 5.5 V
  At 1 MHz ..... 2.2 to 5.5 V
  XIN oscillation frequency at on-chip oscillator ..... 1.8 to 5.5 V
- Power dissipation ..... 22.5mW(standard)
- Operating temperature range ..... –20 to 85 °C

APPLICATION

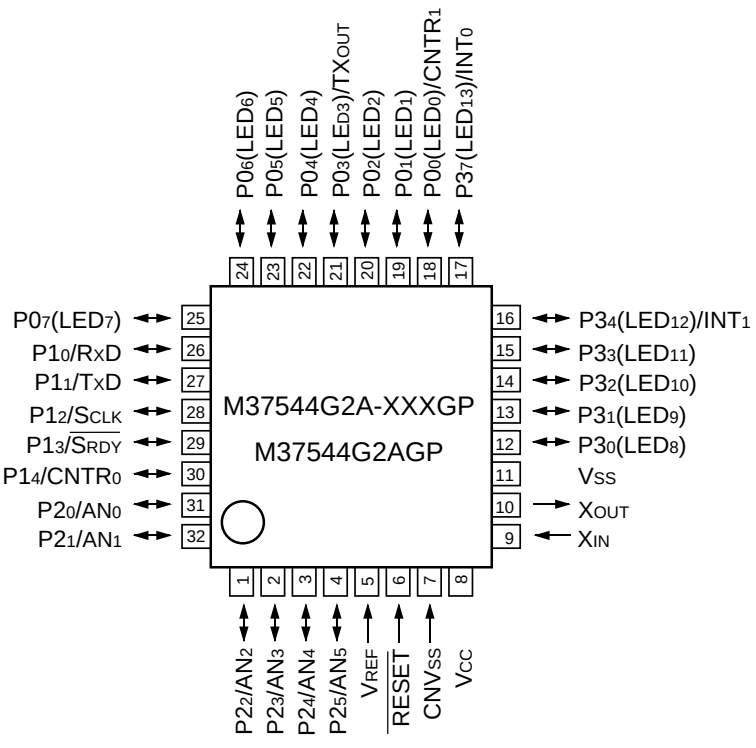
Office automation equipment, factory automation equipment, home electric appliances, consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : PRDP0032BA-A (32P4B)

Fig. 1 Pin configuration (PRDP0032BA-A type)



Package type : PLQP0032GB-A (32P6U-A)

Fig. 2 Pin configuration (PLQP0032GB-A type)

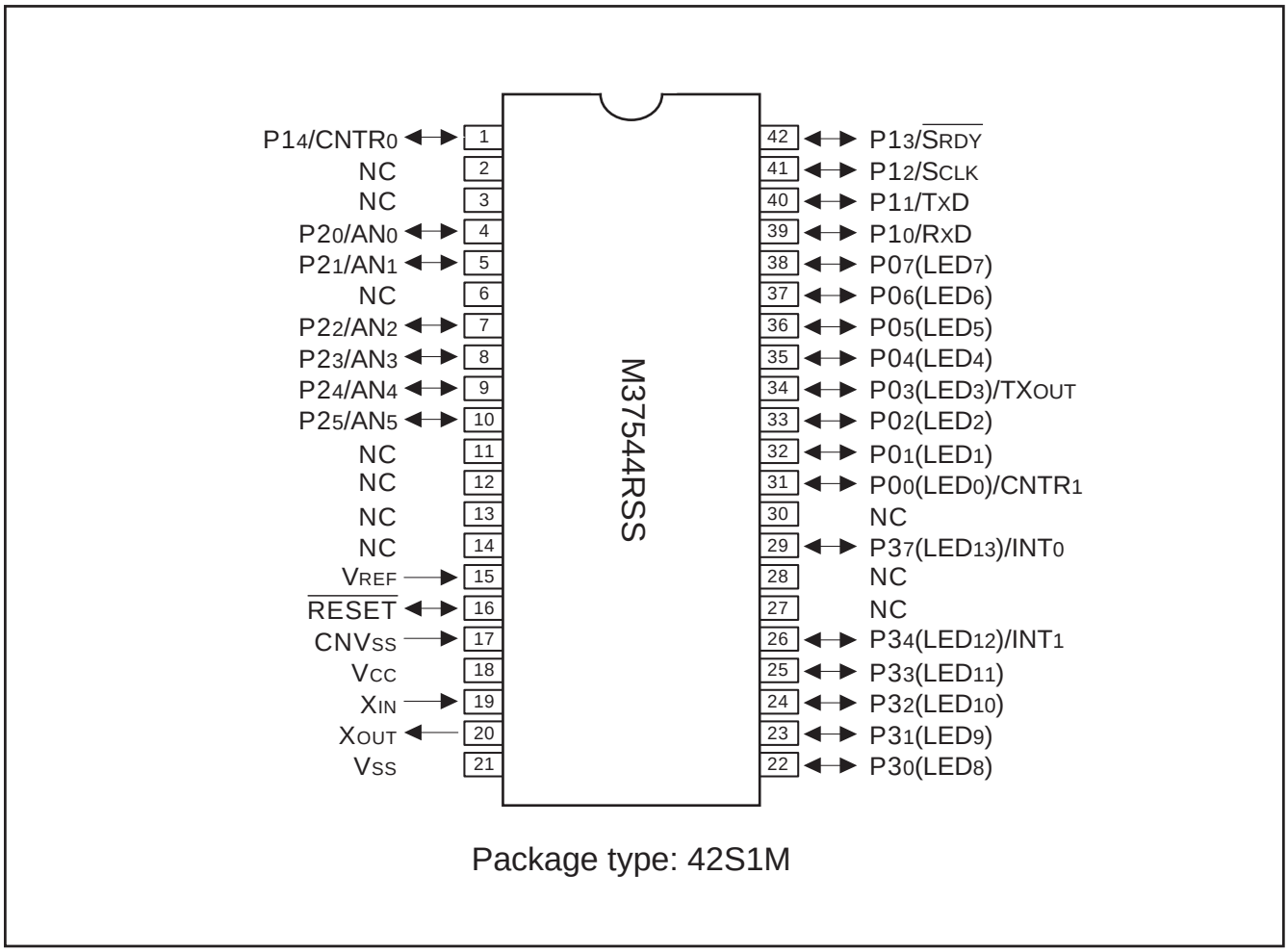


Fig. 3 Pin configuration (42S1M type)

Table 1 Performance overview

Parameter			Function
Number of basic instructions			71
Instruction execution time			0.25 μs (Minimum instruction, oscillation frequency = 8MHz, double-speed mode)
Oscillation frequency			8 MHz (Maximum)
Memory sizes	ROM		8 K bytes
	RAM		256 bytes
Input output port	P0, P1, P2, P3		8-bit × 1, 6-bit × 2, 5-bit × 1
Interrupt			12 sources, 12 vectors
Timer			8-bit × 2, 16-bit × 1
Serial interface			8-bit × 1 (UART or Clock-synchronized)
A/D converter			8-bit resolution × 6 channels
Watchdog timer			16-bit × 1
Clock generating circuits			Low-power dissipation by an on-chip oscillator enabled (connect to external ceramic resonator or quartz-crystal oscillator permitting RC oscillation)
Power source voltage (ceramic oscillation frequency)	In high-,middle-speed mode	8MHz	4.0 to 5.5 V
		4MHz	2.4 to 5.5 V
		2MHz	2.2 to 5.5 V
	In double-speed mode	8MHz	4.5 to 5.5 V
		4MHz	4.0 to 5.5 V
		2MHz	2.4 to 5.5 V
		1MHz	2.2 to 5.5 V
Power source voltage (RC oscillation frequency)	In high-,middle-speed mode	4MHz	4.5 to 5.5 V
		2MHz	2.4 to 5.5 V
		1MHz	2.2 to 5.5 V
Power source voltage (In on-chip oscillator frequency)			1.8 to 5.5V
Power dissipation			Std. 22.5 mW
Operating temperature range			-20 to 85 °C
Device structure			CMOS sillicon gate
Package			32-pin plastic molded SDIP/LQFP

FUNCTIONAL BLOCK

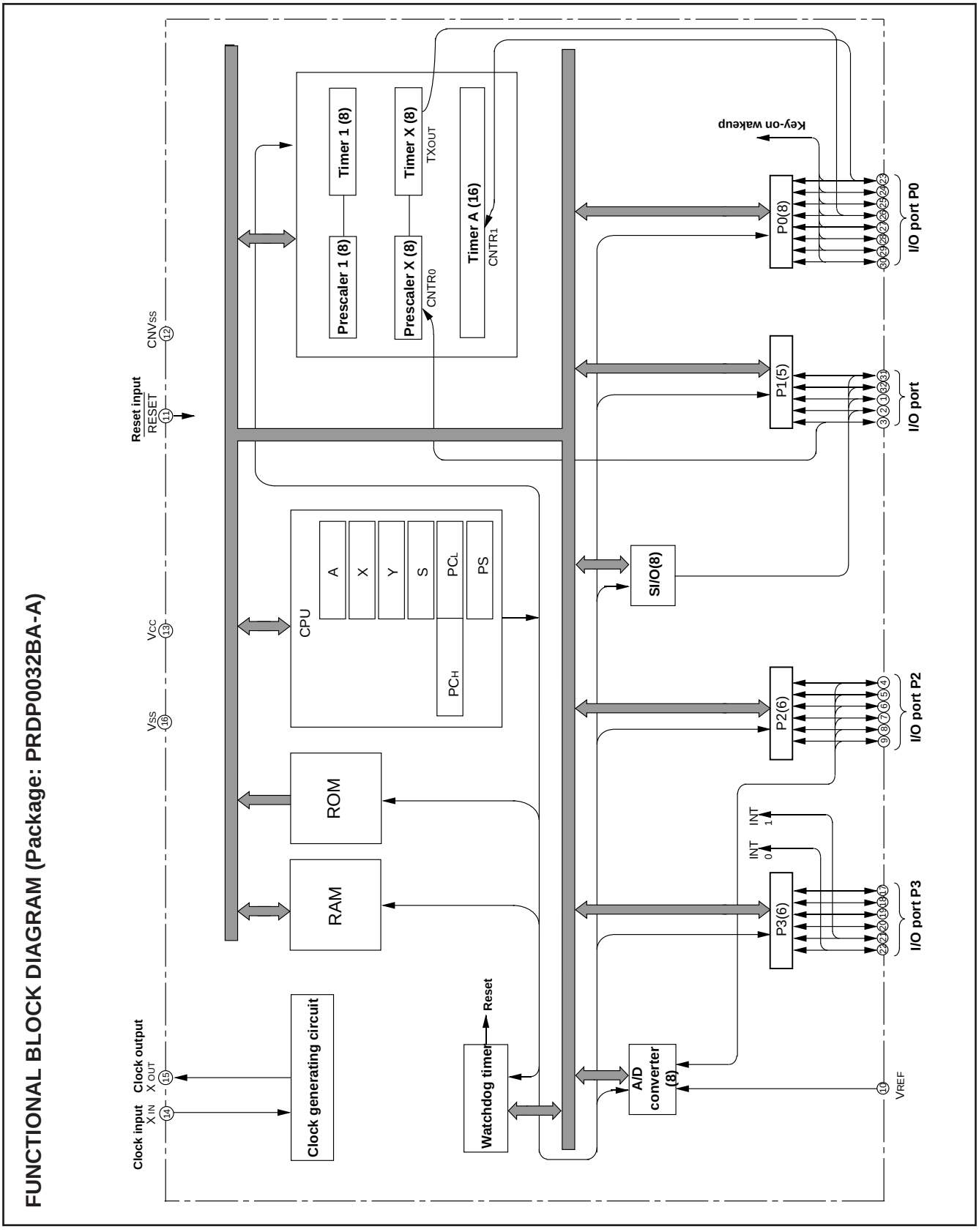


Fig. 4 Functional block diagram (PRDP0032BA-A package)

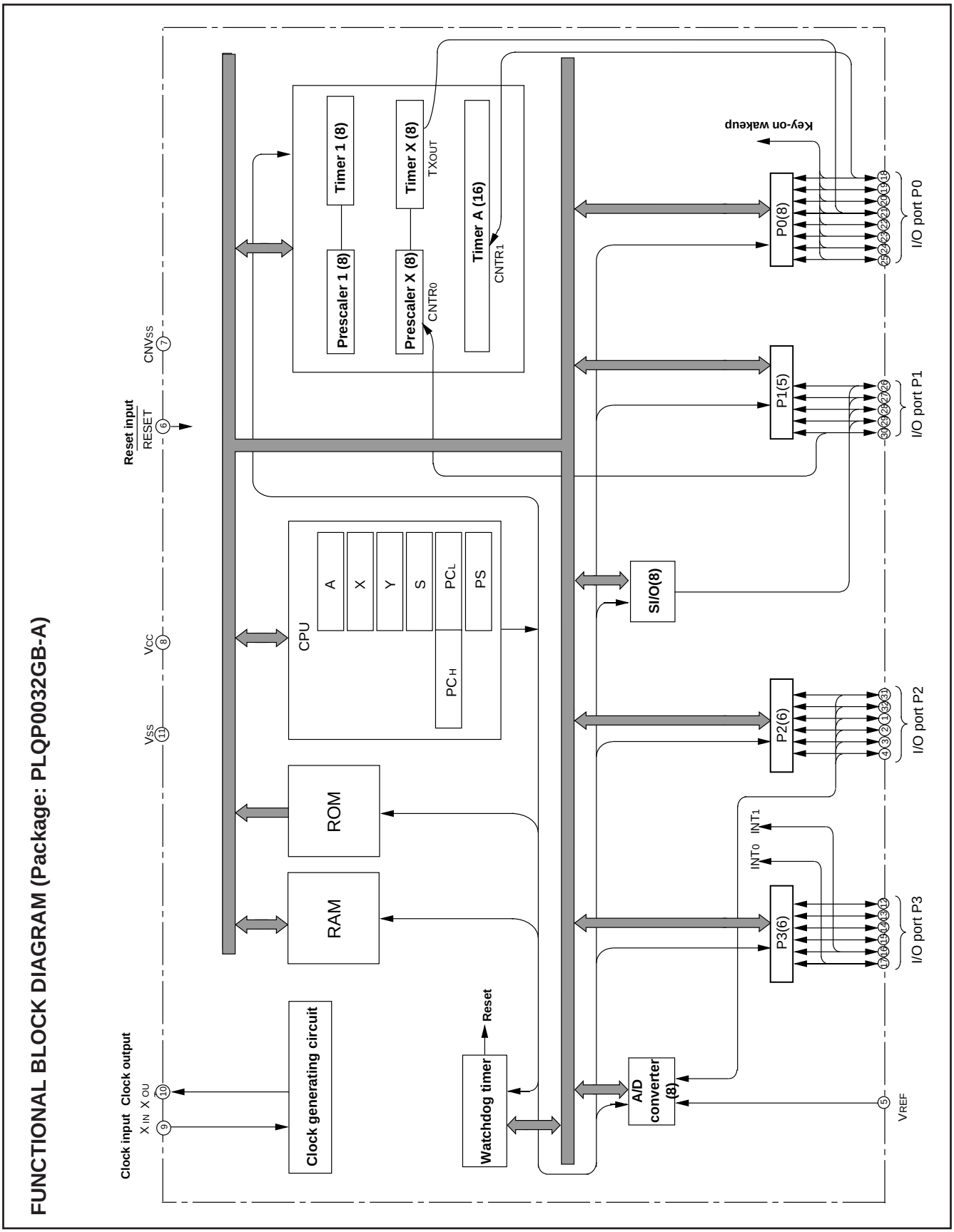


Fig. 5 Functional block diagram (PLQP0032GB-A package)

PIN DESCRIPTION

Table 2 Pin description

Pin	Name	Function	Function expect a port function
Vcc, Vss	Power source	•Apply voltage of 1.8 to 5.5 V to Vcc, and 0 V to Vss.	
VREF	Analog reference voltage	•Reference voltage input pin for A/D converter	
CNVss	CNVss	•Chip operating mode control pin, which is always connected to Vss.	
$\overline{\text{RESET}}$	Reset input	•Reset input pin for active “L”	
XIN	Clock input	•Input and output pins for main clock generating circuit •Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins. •For using RC oscillator, short between the XIN and XOUT pins, and connect the capacitor and resistor. •If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. • When the on-chip oscillator is selected as the main clock, connect XIN pin to VCC and leave XOUT open.	
XOUT	Clock output		
P00/CNTR1 P01 P02 P03/TXOUT P04–P07	I/O port P0	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •P0 can output a large current for driving LED. •Whether a built-in pull-up resistor is to be used or not can be determined by program.	• Key-input (key-on wake up interrupt input) pins • Timer X and timer A function pin
P10/RxD P11/TxD	I/O port P1	•5-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •CMOS/TTL level can be switched for P10 and P12	• Serial I/O function pin
P12/SCLK P13/$\overline{\text{SRDY}}$			
P14/CNTR0			• Timer X function pin
P20/AN0–P25/AN5	I/O port P2	•6-bit I/O port having almost the same function as P0 •CMOS compatible input level •CMOS 3-state output structure	• Input pins for A/D converter
P30–P33	I/O port P3	•6-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level (CMOS/TTL level can be switched for P34 and P37). •CMOS 3-state output structure •P3 can output a large current for driving LED.	
P34/INT1 P37/INT0		•Whether a built-in pull-up resistor is to be used or not can be determined by program.	• Interrupt input pins

GROUP EXPANSION

We are planning to expand the 7544 group (QzROM version) as follow:

Memory type

Support for QzPROM version.

Memory size

ROM size ..... 8 K bytes
RAM size ..... 256 bytes

Package

PRDP0032BA-A ..... 32-pin plastic molded SDIP
PLQP0032GB-A ..... 0.8 mm-pitch 32-pin plastic molded LQFP
4S1M ..... 42-pin shrink ceramic PIGGY BACK

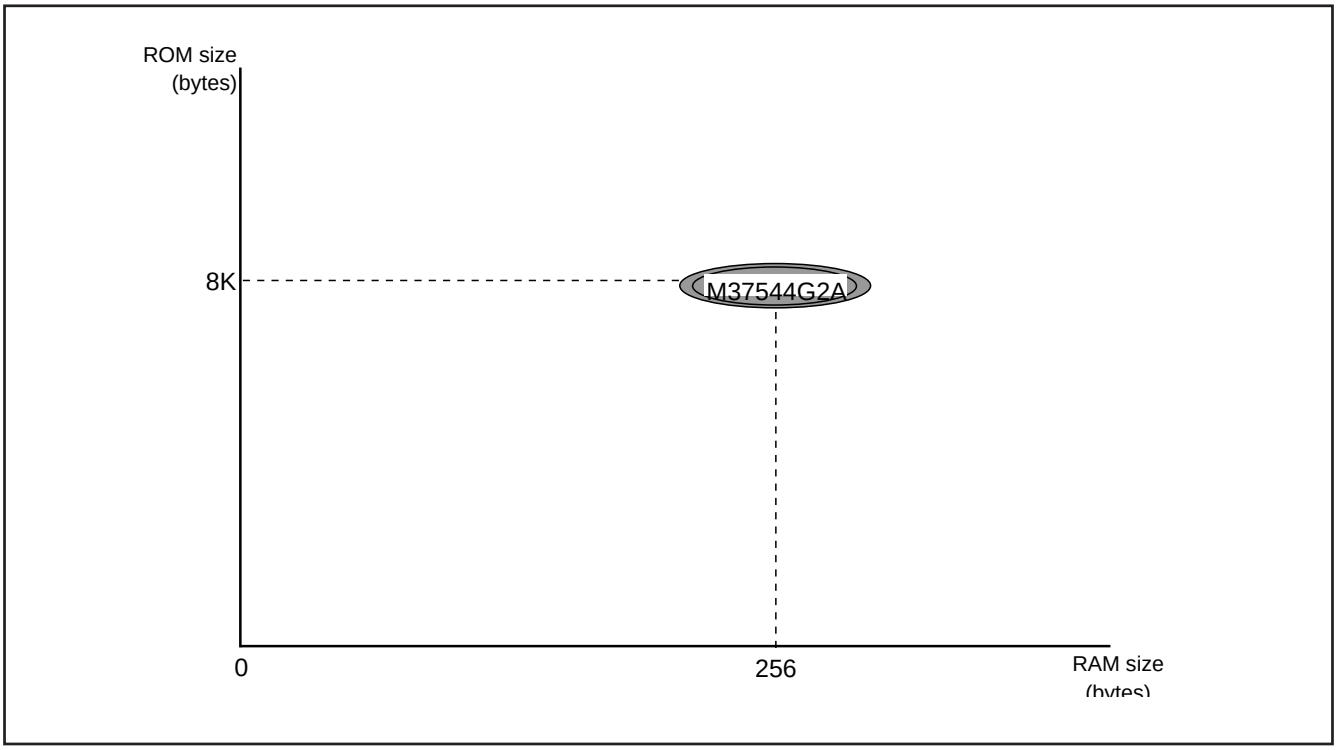


Fig. 6 Memory expansion plan

Currently supported products are listed below.

Table 3 List of supported products

Part number	ROM size (bytes) ROM size for User ()	RAM size (bytes)	Package	Remarks
M37544G2A-XXXSP	8192 (8062)	256	PRDP0032BA-A	QzROM version
M37544G2A-XXXGP			PLQP0032GB-A	QzROM version
M37544G2ASP			PRDP0032BA-A	QzROM version (blank)
M37544G2AGP			PLQP0032GB-A	QzROM version (blank)
M37544RSS	–		42S1M	Emulator MCU

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The MCU uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine-language instructions or the SERIES 740 <SOFTWARE> USER'S MANUAL for details on each instruction set.

Machine-resident 740 family instructions are as follows:

1. The FST and SLW instructions cannot be used.
2. The MUL and DIV instructions can be used.
3. The WIT instruction can be used.
4. The STP instruction can be used.

This instruction cannot be used while CPU operates by an on-chip oscillator.

Accumulator (A)

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

Index register X (X), Index register Y (Y)

Both index register X and index register Y are 8-bit registers. In the index addressing modes, the value of the OPERAND is added to the contents of register X or register Y and specifies the real address.

When the T flag in the processor status register is set to "1", the value contained in index register X becomes the address for the second OPERAND.

Stack pointer (S)

The stack pointer is an 8-bit register used during subroutine calls and interrupts. The stack is used to store the current address data and processor status when branching to subroutines or interrupt routines.

The lower eight bits of the stack address are determined by the contents of the stack pointer. The upper eight bits of the stack address are determined by the Stack Page Selection Bit. If the Stack Page Selection Bit is "0", then the RAM in the zero page is used as the stack area. If the Stack Page Selection Bit is "1", then RAM in page 1 is used as the stack area.

The Stack Page Selection Bit is located in the SFR area in the zero page. Note that the initial value of the Stack Page Selection Bit varies with each microcomputer type. Also some microcomputer types have no Stack Page Selection Bit and the upper eight bits of the stack address are fixed. The operations of pushing register contents onto the stack and popping them from the stack are shown in Fig. 8.

Program counter (PC)

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

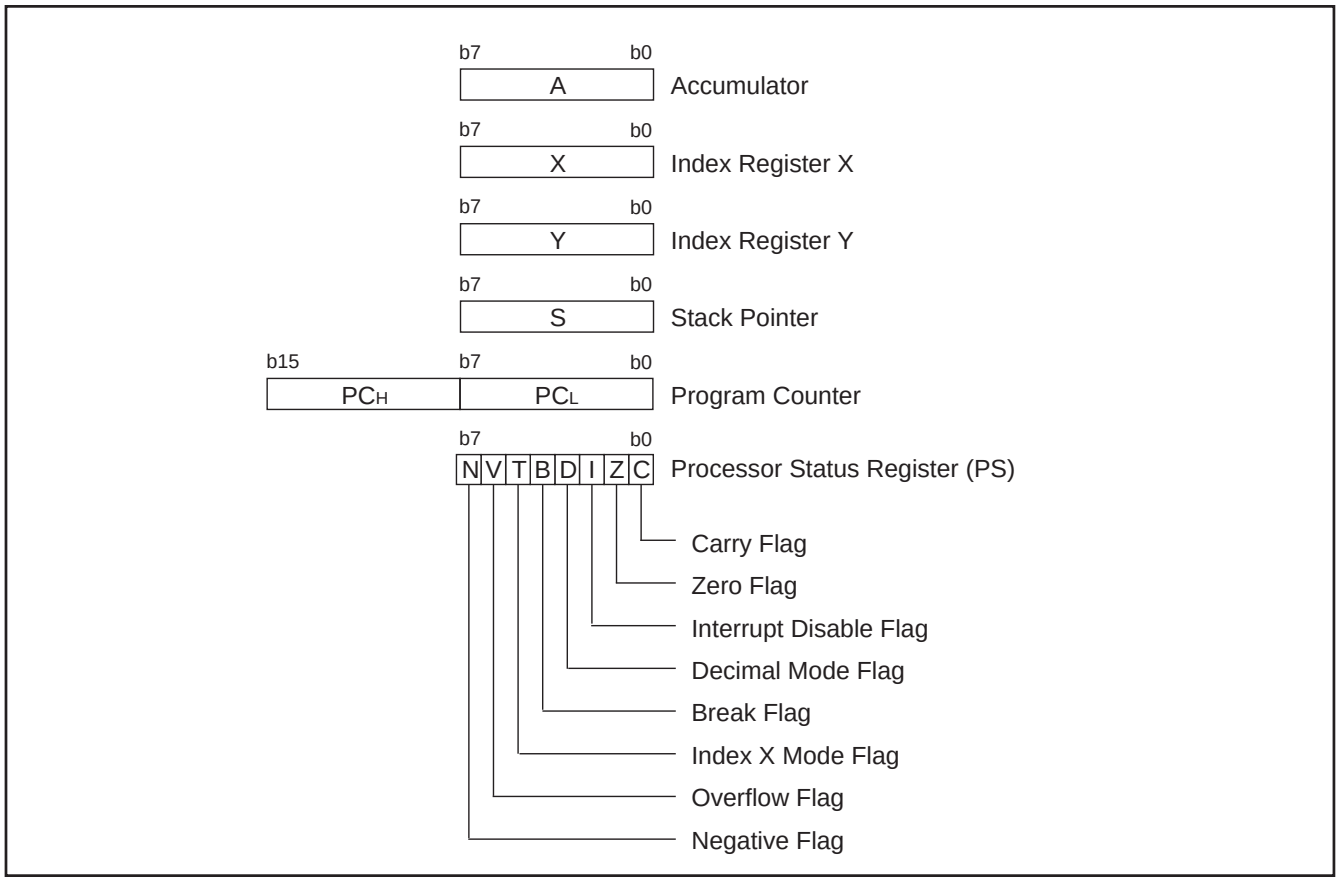


Fig. 7 740 Family CPU register structure

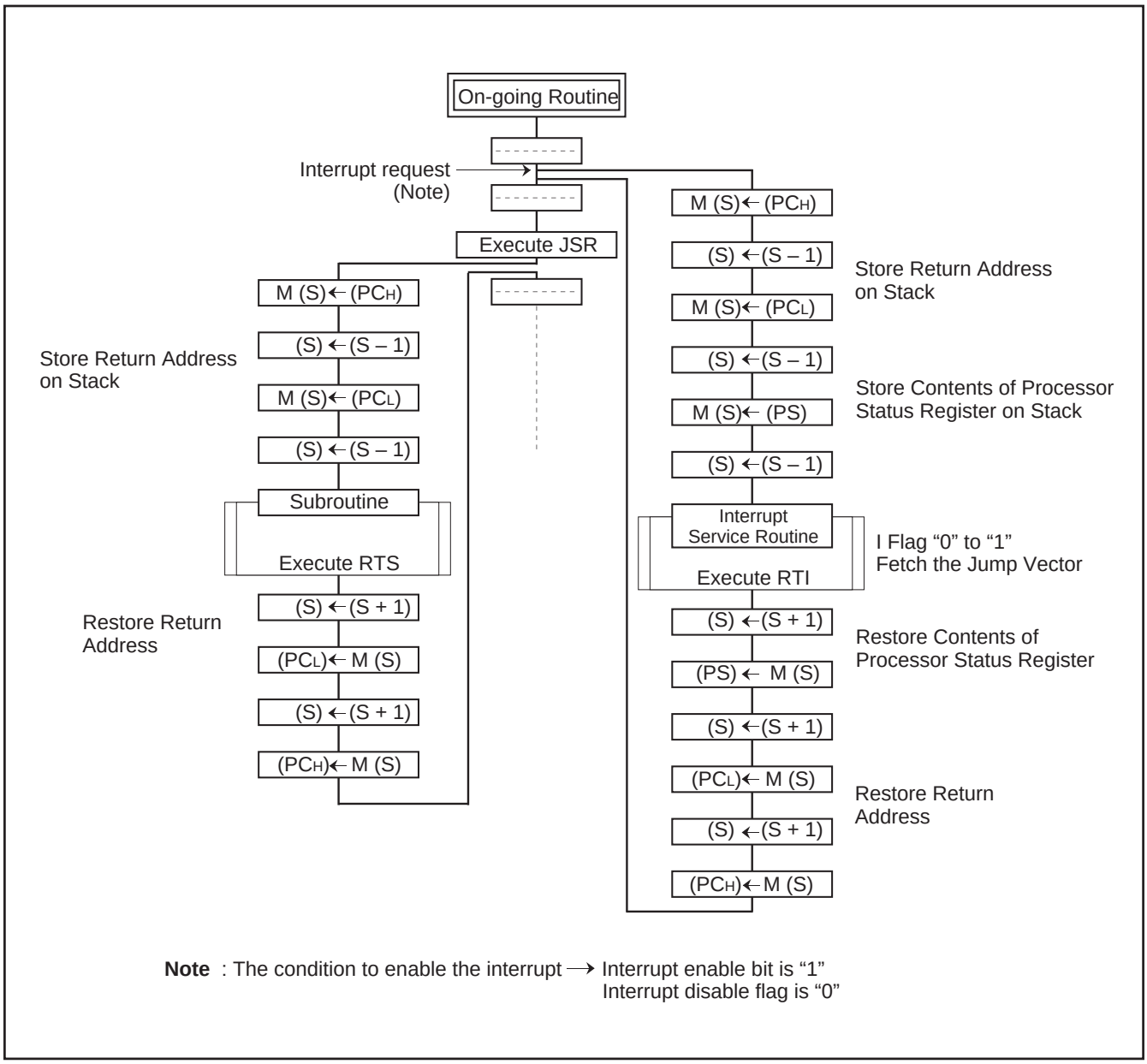


Fig. 8 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

Processor status register (PS)

The processor status register is an 8-bit register consisting of flags which indicate the status of the processor after an arithmetic operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

After reset, the Interrupt disable (I) flag is set to “1”, but all other flags are undefined. Since the Index X mode (T) and Decimal mode (D) flags directly affect arithmetic operations, they should be initialized in the beginning of a program.

(1) Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

(2) Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

(3) Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction. Interrupts are disabled when the I flag is “1”.

When an interrupt occurs, this flag is automatically set to “1” to prevent other interrupts from interfering until the current interrupt is serviced.

(4) Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”.

Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

(5) Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”. The saved processor status is the only place where the break flag is ever set.

(6) Index X mode flag (T)

When the T flag is “0”, arithmetic operations are performed between accumulator and memory, e.g. the results of an operation between two memory locations is stored in the accumulator. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations, i.e. between memory and memory, memory and I/O, and I/O and I/O. In this case, the result of an arithmetic operation performed on data in memory location 1 and memory location 2 is stored in memory location 1. The address of memory location 1 is specified by index register X, and the address of memory location 2 is specified by normal addressing modes.

(7) Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

(8) Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU mode register] CPUM

The CPU mode register contains the stack page selection bit. This register is allocated at address 003B16.

Switching method of CPU mode register

Switch the CPU mode register (CPUM) at the head of program after releasing Reset in the following method.

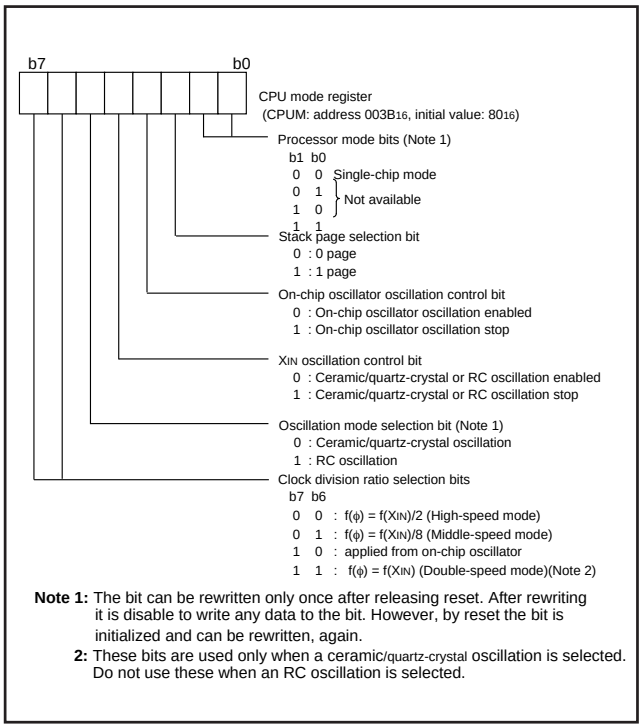


Fig. 9 Structure of CPU mode register

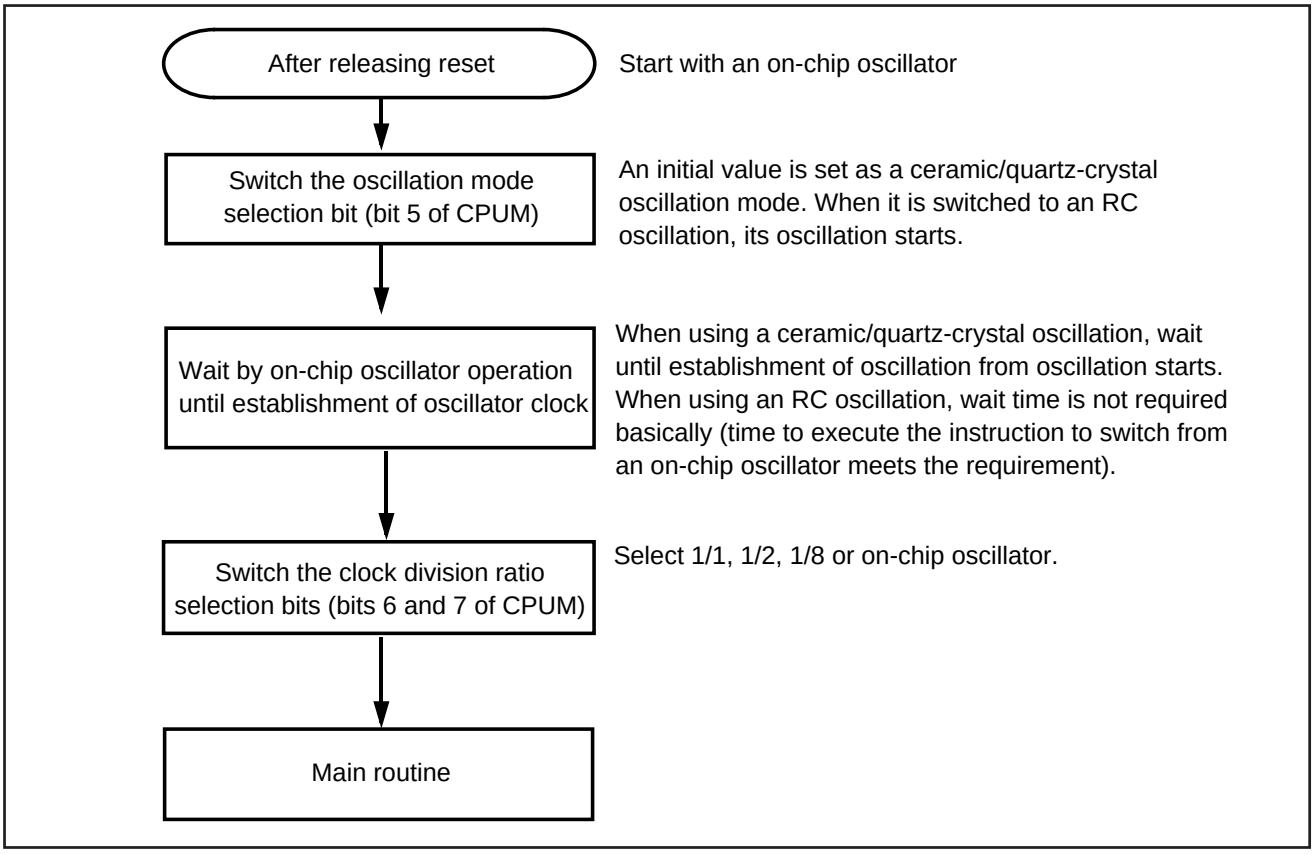


Fig. 10 Switching method of CPU mode register

Memory

Special function register (SFR) area

The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

ROM Code Protect Address (address FFD4$_{16}$)

Address FFD4$_{16}$, which is the reserved ROM area of QzROM, is the ROM code protect address. "00$_{16}$" is written into this address when selecting the protect bit write by using a serial programmer or selecting protect enabled for writing shipment by Renesas Technology corp.. When "00$_{16}$" is set to the ROM code protect address, the protect function is enabled, so that reading or writing from/to QzROM is disabled by a serial programmer.

As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.

As for the QzROM product shipped after writing, "00$_{16}$" (protect enabled) or "FF$_{16}$" (protect disabled) is written into the ROM code protect address when Renesas Technology corp. performs writing. The writing of "00$_{16}$" or "FF$_{16}$" can be selected as the ROM (referred to as "Mask option setup" in MM) when ordering.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000$_{16}$ to 00FF$_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses FF00$_{16}$ to FFFF$_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

■ Note on use

The content of RAM is undefined when the microcomputer is reset. The initial values must be surely set before you use it.

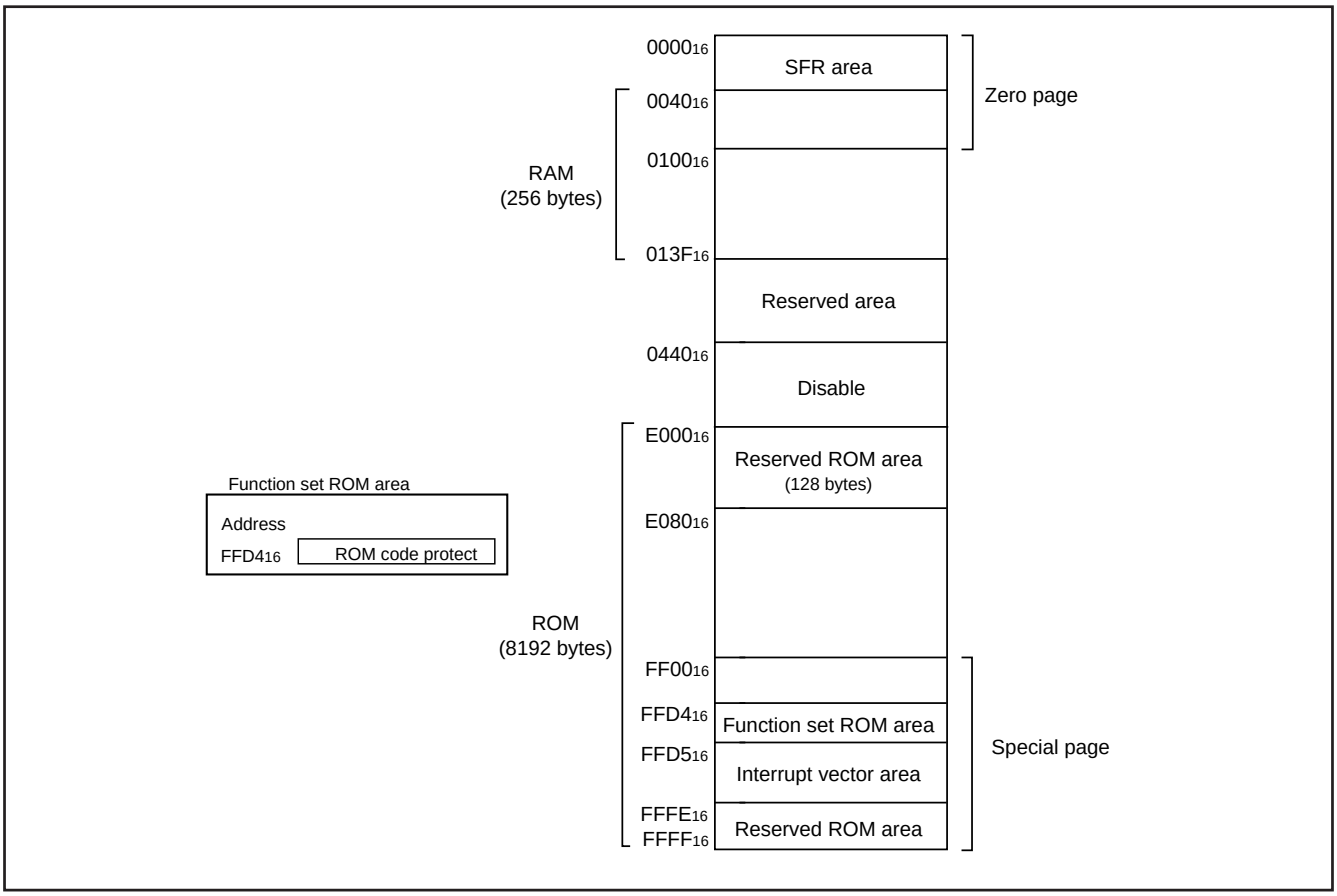


Fig. 11 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Reserved
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Reserved
0002_{16}	Port P1 (P1)	0022_{16}	Reserved
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Reserved
0004_{16}	Port P2 (P2)	0024_{16}	Reserved
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Reserved
0006_{16}	Port P3 (P3)	0026_{16}	Reserved
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Reserved
0008_{16}	Reserved	0028_{16}	Prescaler 1 (PRE1)
0009_{16}	Reserved	0029_{16}	Timer 1 (T1)
$000A_{16}$	Reserved	$002A_{16}$	Reserved
$000B_{16}$	Reserved	$002B_{16}$	Timer X mode register (TXM)
$000C_{16}$	Reserved	$002C_{16}$	Prescaler X (PREX)
$000D_{16}$	Reserved	$002D_{16}$	Timer X (TX)
$000E_{16}$	Reserved	$002E_{16}$	Timer count source set register1 (TCSS1)
$000F_{16}$	Reserved	$002F_{16}$	Timer count source set register2 (TCSS2)
0010_{16}	Reserved	0030_{16}	Reserved
0011_{16}	Reserved	0031_{16}	Reserved
0012_{16}	Reserved	0032_{16}	Reserved
0013_{16}	Reserved	0033_{16}	Reserved
0014_{16}	Reserved	0034_{16}	A/D control register (ADCON)
0015_{16}	Reserved	0035_{16}	A/D register (AD)
0016_{16}	Pull-up control register (PULL)	0036_{16}	Reserved
0017_{16}	Port P1P3 control register (P1P3C)	0037_{16}	Reserved
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	MISRG
0019_{16}	Serial I/O status register (SIOSTS)	0039_{16}	Watchdog timer control register (WDTCON)
$001A_{16}$	Serial I/O control register (SIOCON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Timer A mode register (TAM)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$	Timer A (low-order) (TAL)	$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Timer A (high-order) (TAH)	$003F_{16}$	Interrupt control register 2 (ICON2)

Note : Do not access to the SFR area including nothing.

Fig. 12 Memory map of special function register (SFR)

I/O Ports

[Direction registers] PiD

The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output.

When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port.

When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.

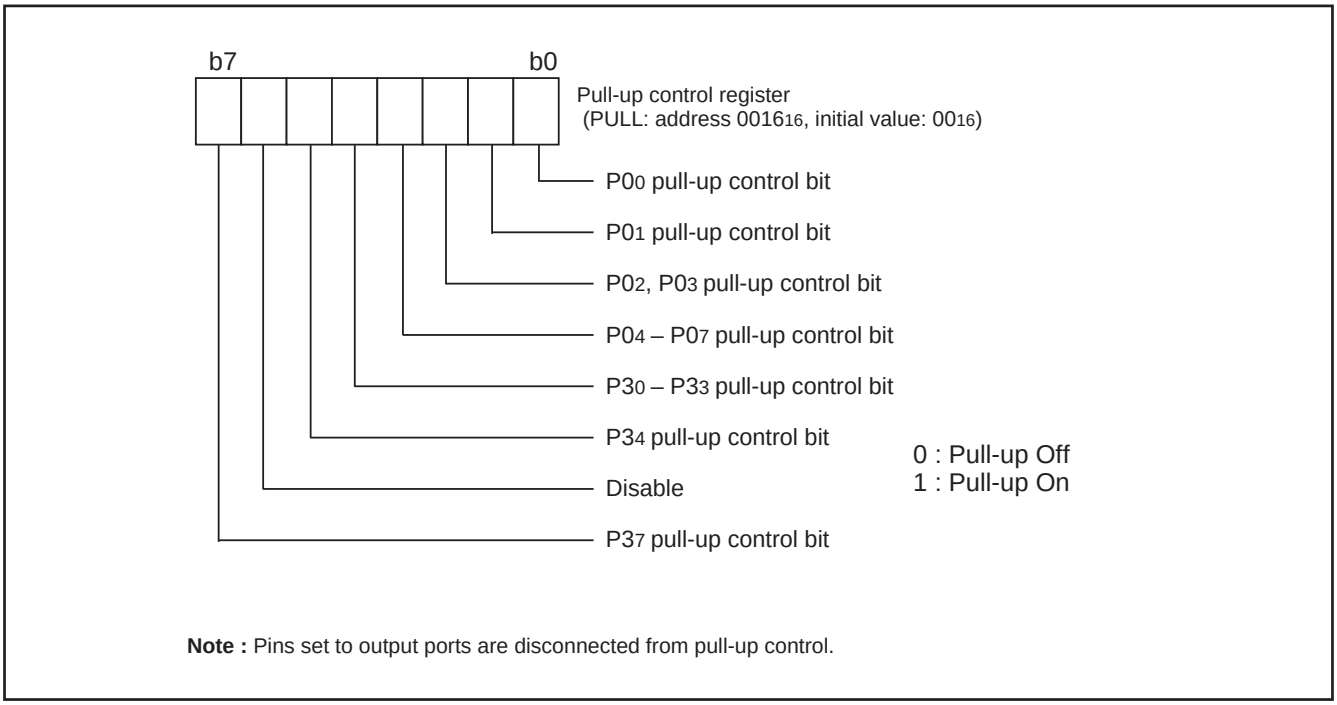
If a pin set to input is written to, only the port latch is written to and the pin remains floating.

[Pull-up control register] PULL

By setting the pull-up control register (address 0016_{16}), ports P0 and P3 can exert pull-up control by program. However, pins set to output are disconnected from this control and cannot exert pull-up control.

[Port P1P3 control register] P1P3C

By setting the port P1P3 control register (address 0017_{16}), a CMOS input level or a TTL input level can be selected for ports $P1_0$, $P1_2$, $P3_4$, and $P3_7$ by program.



Note : Pins set to output ports are disconnected from pull-up control.

Fig. 13 Structure of pull-up control register

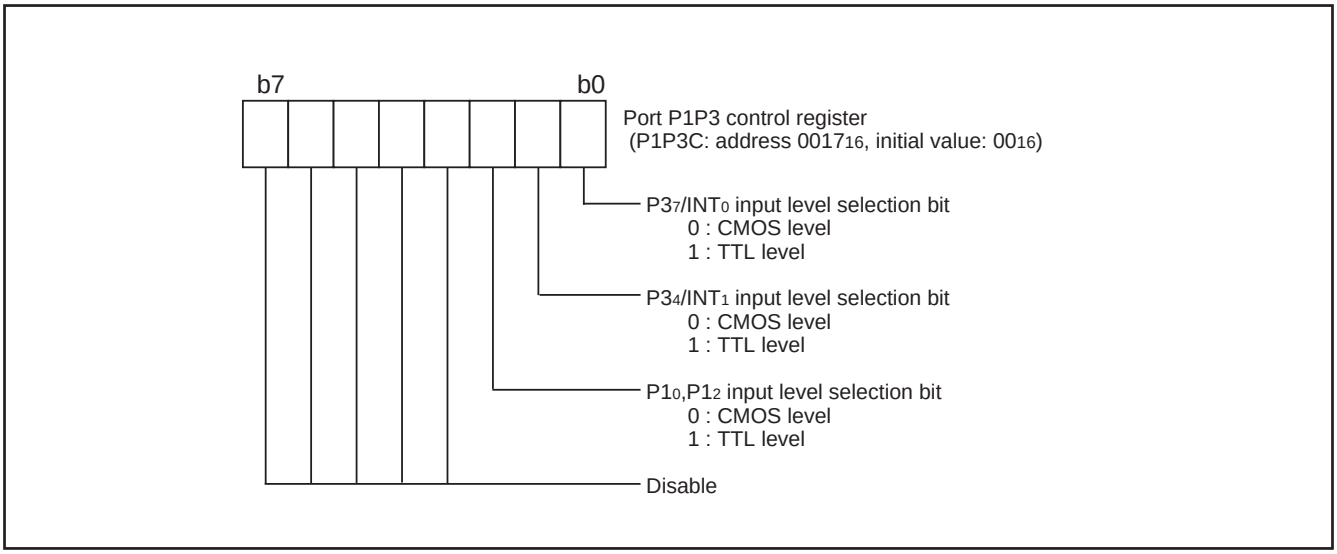


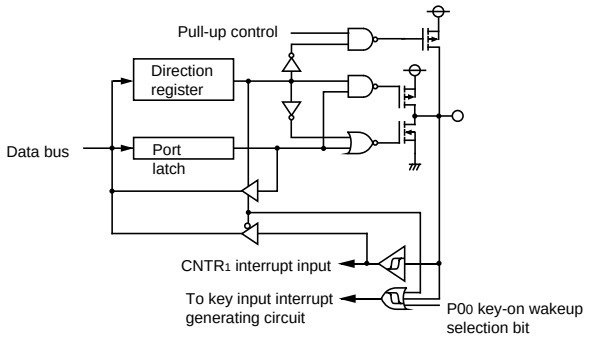
Fig. 14 Structure of port P1P3 control register

Table 6 I/O port function table

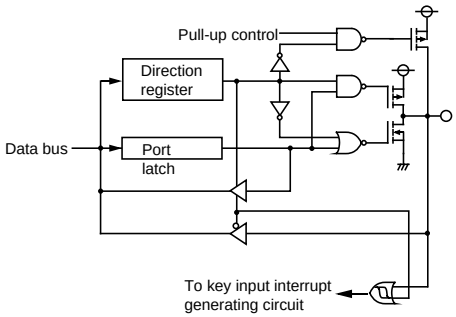
Pin	Name	Input/output	I/O format	Non-port function	Related SFRs	Diagram No.
$P0_0$/CNTR$_1$ $P0_1$ $P0_2$ $P0_3$/TX$_{OUT}$ $P0_4$–$P0_7$	I/O port P0	I/O individual bits	•CMOS compatible input level •CMOS 3-state output (**Note**)	Key input interrupt Timer X function output Timer A function input	Pull-up control register Timer X mode register Timer A mode register Interrupt edge selection register	(1) (2) (3)
$P1_0$/RxD $P1_1$/TxD $P1_2$/S$_{CLK}$ $P1_3$/$\overline{S_{RDY}}$	I/O port P1			Serial I/O function input/output	Serial I/O control register Port P1,P3 control register	(4) (5) (6) (7)
$P1_4$/CNTR$_0$				Timer X function input/output	Timer X mode register	(8)
$P2_0$/AN$_0$– $P2_5$/AN$_5$	I/O port P2			A/D conversion input	A/D control register	(9)
$P3_0$–$P3_3$	I/O port P3				Pull-up control register	(10)
$P3_4$/INT$_1$ $P3_7$/INT$_0$				External interrupt input	Interrupt edge selection register Pull-up control register Port P1,P3 control register	(11)

Note : Ports $P1_0$, $P1_2$, $P3_4$, and $P3_7$ are CMOS/TTL level.

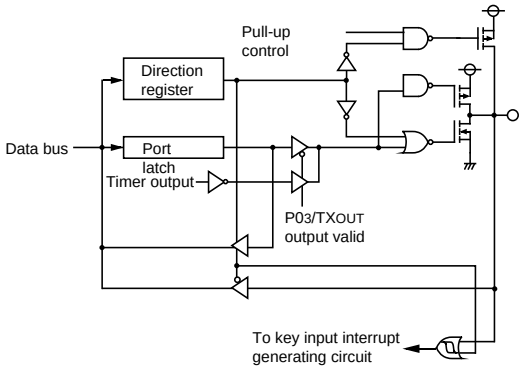
(1)Port P0$_0$



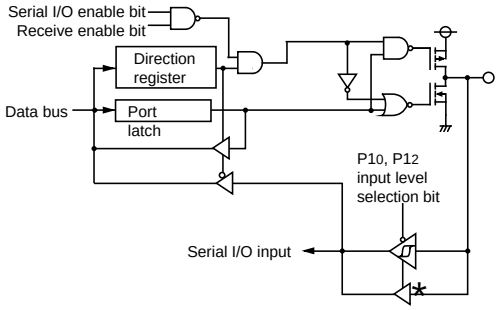
(2)Ports P0$_1$,P0$_2$,P0$_4$–P0$_7$



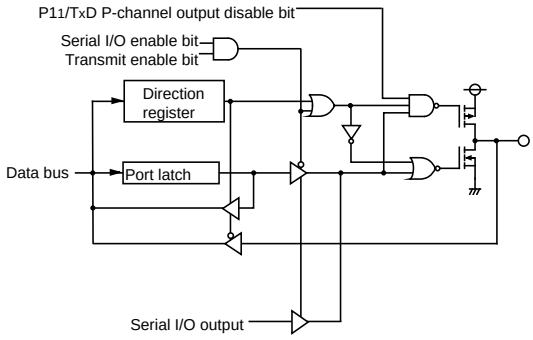
(3)Port P0$_3$



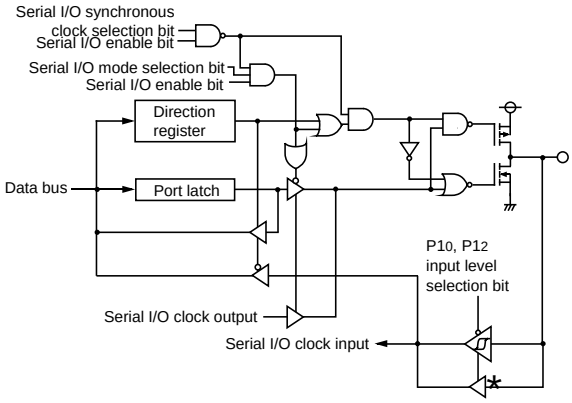
(4)Port P1$_0$



(5)Port P1$_1$



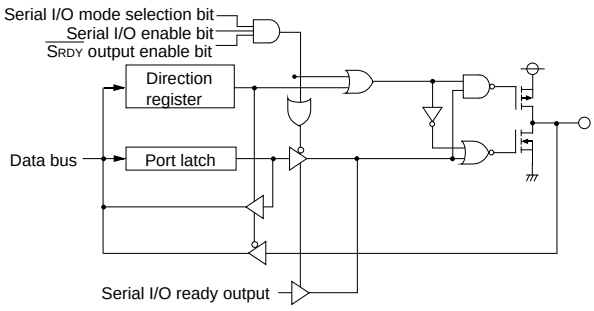
(6)Port P1$_2$



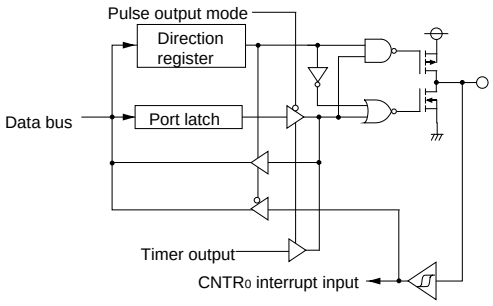
* P10, P12, P34, and P37 input level are switched to the CMOS/TTL level by the port P1P3 control register.
When the TTL level is selected, there is no hysteresis characteristics.

Fig. 15 Block diagram of ports (1)

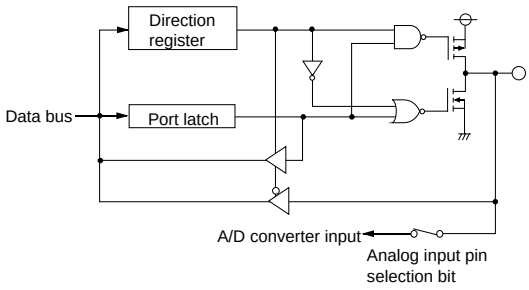
(7) Port P1$_3$



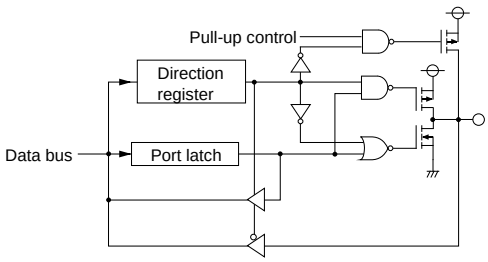
(8) Port P1$_4$



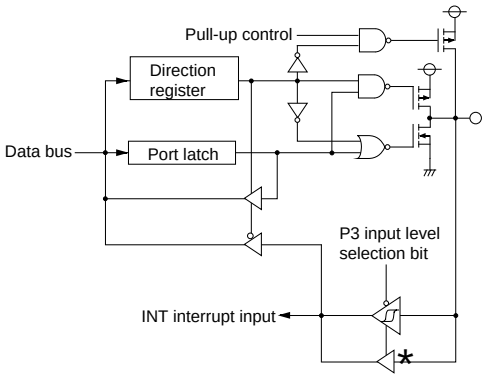
(9) Ports P2$_0$–P2$_5$



(10) Ports P3$_0$–P3$_3$



(11) Ports P3$_4$, P3$_7$



* P1$_0$, P1$_2$, P3$_4$, and P3$_7$ input level are switched to the CMOS/TTL level by the port P1P3 control register. When the TTL level is selected, there is no hysteresis characteristics.

Fig. 16 Block diagram of ports (2)

Termination of unused pins

• Termination of common pins

I/O ports: Select an input port or an output port and follow each processing method.

Output ports: Open.

Input ports: If the input level become unstable, through current flow to an input circuit, and the power supply current may increase.
Especially, when expecting low consumption current (at STP or WIT instruction execution etc.), pull-up or pull-down input ports to prevent through current (built-in resistor can be used).
We recommend processing unused pins through a resistor which can secure $I_{OH(avg)}$ or $I_{OL(avg)}$.
Because, when an I/O port or a pin which have an output function is selected as an input port, it may operate as an output port by incorrect operation etc.

Table 7 Termination of unused pins

Pin	Termination 1 (recommend)	Termination 2	Termination 3	Termination 4
P0$_0$/CNTR$_1$	I/O port	When selecting CNTR$_1$ input function, perform termination of input port.	When selecting CNTR$_1$ output function, perform termination of output port.	When selecting key-on wakeup function, perform termination of input port.
P0$_1$, P0$_2$		-	-	
P0$_3$/TXOUT		When selecting TXOUT function, perform termination of output port.	-	
P0$_4$ to P0$_7$		-	-	
P1$_0$/RXD		When selecting RXD function, perform termination of input port.	-	-
P1$_1$/TXD		When selecting TXD function, perform termination of output port.	-	-
P1$_2$/SCLK		When selecting external clock input, perform termination of input port.	When selecting internal clock output, perform termination of output port.	-
P1$_3$/$\overline{\text{SRDY}}$		When selecting $\overline{\text{SRDY}}$ function, perform termination of output port.	-	-
P1$_4$/CNTR$_0$		When selecting CNTR$_0$ input function, perform termination of input port.	When selecting CNTR$_0$ output function, perform termination of output port.	-
P2$_0$/AN$_0$ to P2$_5$/AN$_5$		When selecting AN function, perform termination of input port.	-	-
P3$_0$ to P3$_3$		-	-	-
P3$_4$/INT$_1$		When selecting INT$_1$ function, perform termination of input port.	-	-
P3$_7$/INT$_0$		When selecting INT$_0$ function, perform termination of input port.	-	-
VREF	Vss.	-	-	-
XIN	When only on-chip oscillator is used, connect to VCC through a registor.	-	-	-
XOUT	When external clock is input or when only on-chip oscillator is used, open.	-	-	-

Interrupts

The 7544 Group interrupts are vector interrupts with a fixed priority scheme, and generated by 12 sources: 5 external, 6 internal, and 1 software.

The interrupt sources, vector addresses(1) , and interrupt priority are shown in Table 8.

Each interrupt except the BRK instruction interrupt has the interrupt request bit and the interrupt enable bit. These bits and the interrupt disable flag (I flag) control the acceptance of interrupt requests. Fig. 17 shows an interrupt control diagram.

An interrupt request is accepted when all of the following conditions are satisfied:

- Interrupt disable flag.....“0”
- Interrupt request bit.....“1”
- Interrupt enable bit.....“1”

Though the interrupt priority is determined by hardware, priority processing can be performed by software using the above bits and flag.

Table 8 Interrupt vector addresses and priority

Interrupt source	Priority	Vector addresses (**Note 1**)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
Reset (**Note 2**)	1	$FFFD_{16}$	$FFFC_{16}$	At reset input	Non-maskable
Serial I/O receive	2	$FFFB_{16}$	$FFFA_{16}$	At completion of serial I/O data receive	
Serial I/O transmit	3	$FFF9_{16}$	$FFF8_{16}$	At completion of serial I/O transmit shift or when transmit buffer is empty	
INT_0	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	5	$FFF5_{16}$	$FFF4_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Key-on wake-up	6	$FFF3_{16}$	$FFF2_{16}$	At falling of conjunction of input logical level for port P0 (at input)	External interrupt (valid at falling)
$CNTR_0$	7	$FFF1_{16}$	$FFF0_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	8	$FFEF_{16}$	$FFEE_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
Timer X	9	$FFED_{16}$	$FFEC_{16}$	At timer X underflow	
Reserved area	—	$FFEB_{16}$	$FFEA_{16}$	Not available	
Reserved area	—	$FFE9_{16}$	$FFE8_{16}$	Not available	
Timer A	10	$FFE7_{16}$	$FFE6_{16}$	At timer A underflow	
Reserved area	—	$FFE5_{16}$	$FFE4_{16}$	Not available	
A/D conversion	11	$FFE3_{16}$	$FFE2_{16}$	At completion of A/D conversion	
Timer 1	12	$FFE1_{16}$	$FFE0_{16}$	At timer 1 underflow	STP release timer underflow
Reserved area	—	$FFDF_{16}$	$FFDE_{16}$	Not available	
BRK instruction	13	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1: Vector addressed contain internal jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

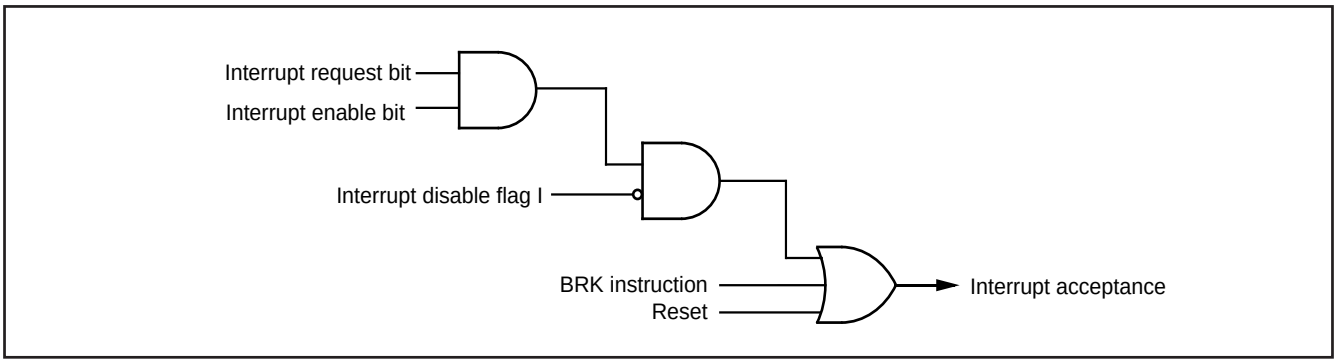


Fig. 17 Interrupt control

• Interrupt Disable Flag

The interrupt disable flag is assigned to bit 2 of the processor status register. This flag controls the acceptance of all interrupt requests except for the BRK instruction. When this flag is set to "1", the acceptance of interrupt requests is disabled. When it is set to "0", the acceptance of interrupt requests is enabled. This flag is set to "1" with the SEI instruction and set to "0" with the CLI instruction.

When an interrupt request is accepted, the contents of the processor status register are pushed onto the stack while the interrupt disable flag remains set to "0". Subsequently, this flag is automatically set to "1" and multiple interrupts are disabled.

To use multiple interrupts, set this flag to "0" with the CLI instruction within the interrupt processing routine.

The contents of the processor status register are popped off the stack with the RTI instruction.

• Interrupt Request Bits

Once an interrupt request is generated, the corresponding interrupt request bit is set to "1" and remains "1" until the request is accepted. When the request is accepted, this bit is automatically set to "0".

Each interrupt request bit can be set to "0", but cannot be set to "1", by software.

• Interrupt Enable Bits

The interrupt enable bits control the acceptance of the corresponding interrupt requests. When an interrupt enable bit is set to "0", the acceptance of the corresponding interrupt request is disabled. If an interrupt request occurs in this condition, the corresponding interrupt request bit is set to "1", but the interrupt request is not accepted. When an interrupt enable bit is set to "1", the acceptance of the corresponding interrupt request is enabled.

Each interrupt enable bit can be set to "0" or "1" by software.

The interrupt enable bit for an unused interrupt should be set to "0".

• Interrupt edge selection

The valid edge of external interrupt INT_0 and INT_1 can be selected by the interrupt edge selection bit of the interrupt edge selection register ($003A_{16}$), respectively.

• Key-on wakeup

Enable/disable of a key-on wakeup of pin $P0_0$ can be selected by the key-on wakeup enable bit of the interrupt edge selection register ($003A_{16}$), respectively.

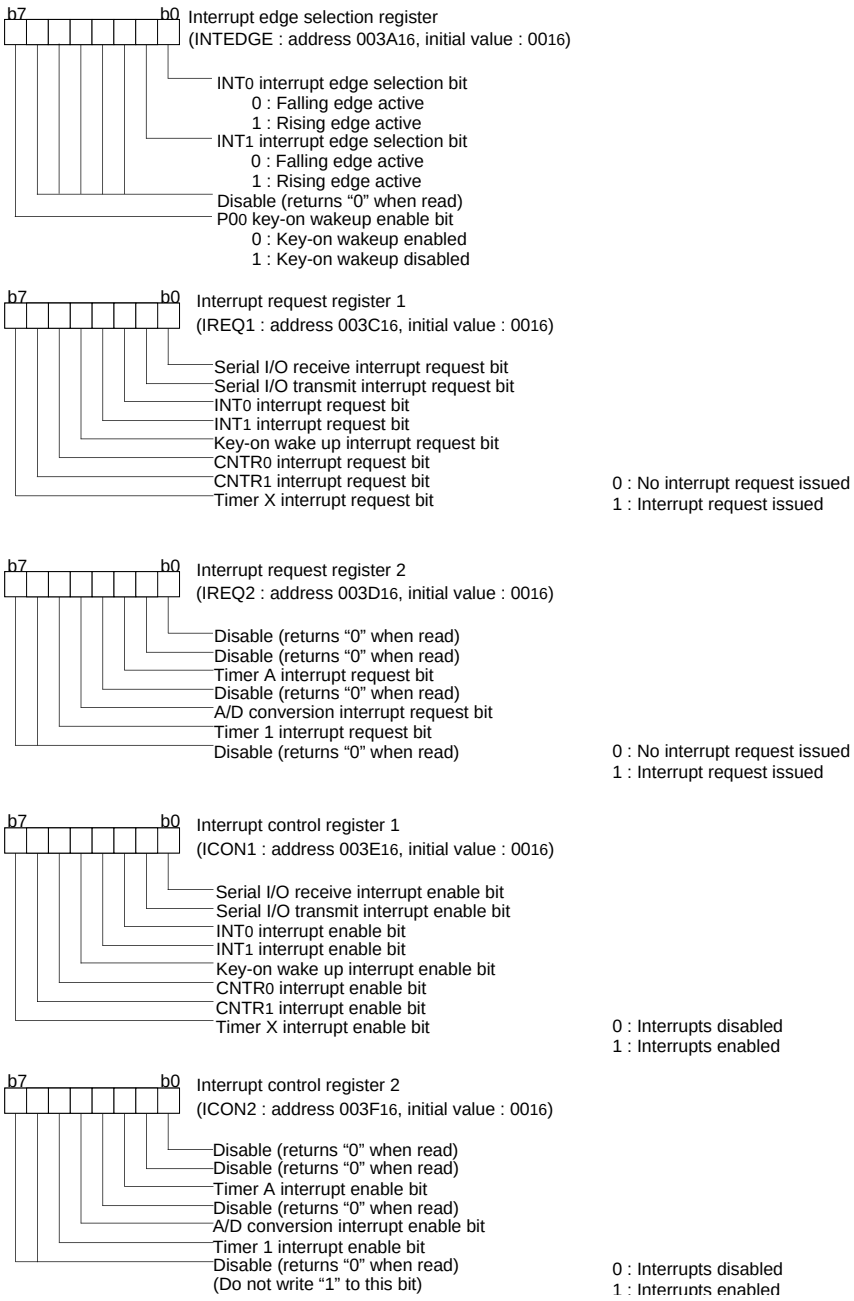


Fig. 18 Structure of Interrupt-related registers

• Interrupt Request Generation, Acceptance, and Handling

Interrupts have the following three phases.

(i) Interrupt Request Generation
An interrupt request is generated by an interrupt source (external interrupt signal input, timer underflow, etc.) and the corresponding request bit is set to “1”.

(ii) Interrupt Request Acceptance
Based on the interrupt acceptance timing in each instruction cycle, the interrupt control circuit determines acceptance conditions (interrupt request bit, interrupt enable bit, and interrupt disable flag) and interrupt priority levels for accepting interrupt requests. When two or more interrupt requests are generated simultaneously, the highest priority interrupt is accepted. The value of the interrupt request bit for an unaccepted interrupt remains the same and acceptance is determined at the next interrupt acceptance timing point.

(iii) Handling of Accepted Interrupt Request
The accepted interrupt request is processed.

Fig. 19 shows the time up to execution in the interrupt processing routine, and Fig. 20 shows the interrupt sequence.
Fig. 21 shows the timing of interrupt request generation, interrupt request bit, and interrupt request acceptance.

• Interrupt Handling Execution

When interrupt handling is executed, the following operations are performed automatically.

(1) Once the currently executing instruction is completed, an interrupt request is accepted.
(2) The contents of the program counters and the processor status register at this point are pushed onto the stack area in order from 1 to 3.
1.High-order bits of program counter (PCH)
2.Low-order bits of program counter (PCL)
3.Processor status register (PS)
(3) Concurrently with the push operation, the jump address of the corresponding interrupt (the start address of the interrupt processing routine) is transferred from the interrupt vector to the program counter.
(4) The interrupt request bit for the corresponding interrupt is set to “0”. Also, the interrupt disable flag is set to “1” and multiple interrupts are disabled.
(5) The interrupt routine is executed.
(6) When the RTI instruction is executed, the contents of the registers pushed onto the stack area are popped off in the order from 3 to 1. Then, the routine that was before running interrupt processing resumes.

As described above, it is necessary to set the stack pointer and the jump address in the vector area corresponding to each interrupt to execute the interrupt processing routine.

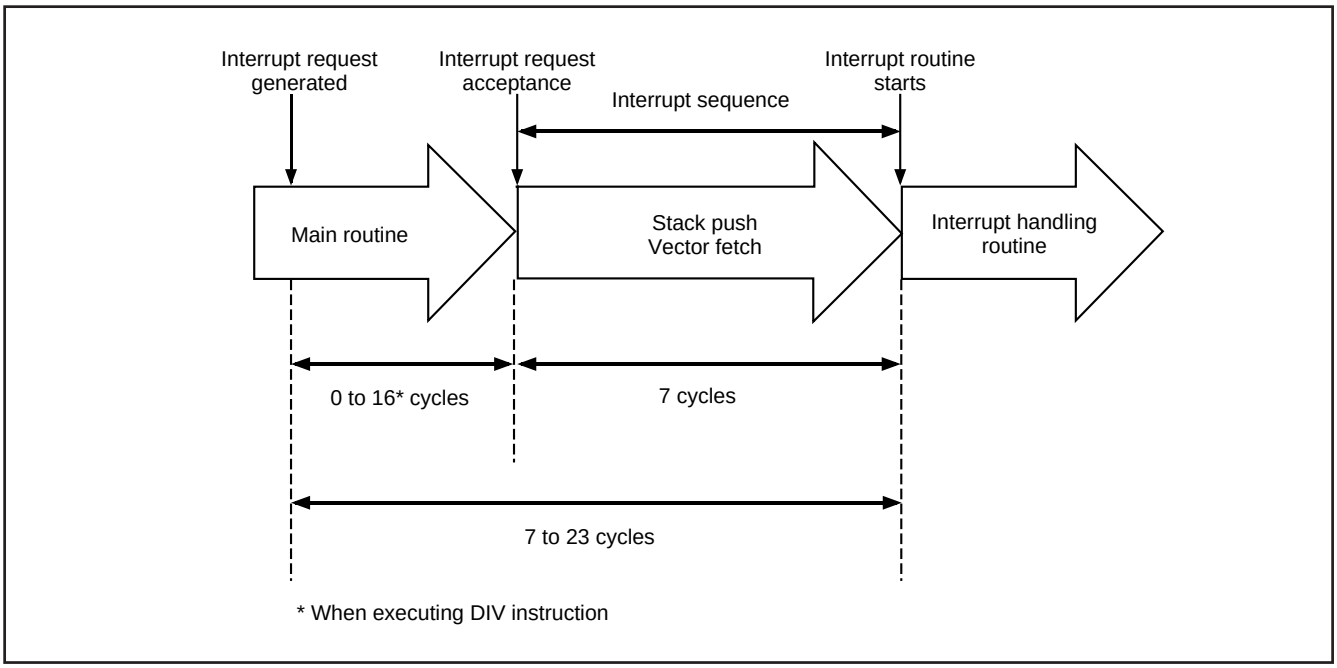
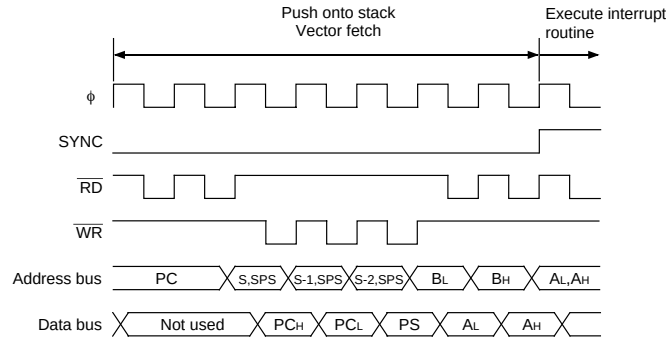
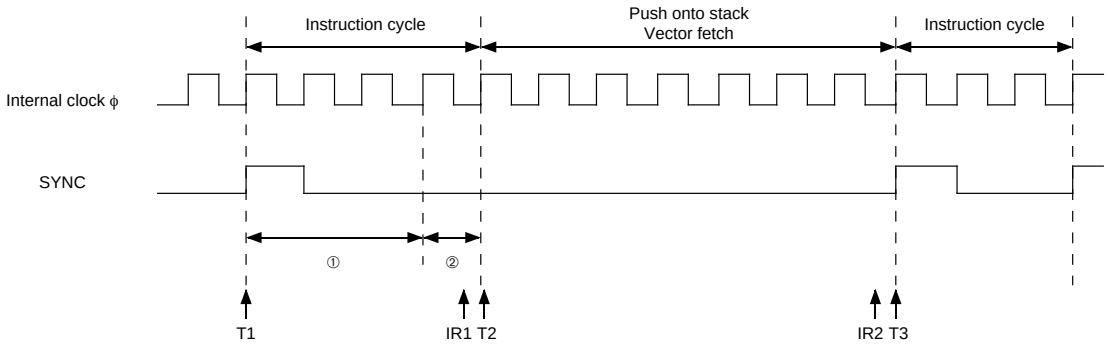


Fig. 19 Time up to execution in interrupt routine



SYNC : CPU operation code fetch cycle
(This is an internal signal that cannot be observed from the external unit.)
B_L, B_H : Vector address of each interrupt
A_L, A_H : Jump destination address of each interrupt
SPS : "00_{16}" or "01_{16}"
([SPS] is a page selected by the stack page selection bit of CPU mode register.)

Fig. 20 Interrupt sequence



T1 T2 T3 : Interrupt acceptance timing points
IR1 IR2 : Timings points at which the interrupt request bit is set to "1".

Note : Period 2 indicates the last ϕ cycle during one instruction cycle.

(1) The interrupt request bit for an interrupt request generated during period 1 is set to "1" at timing point IR1.
(2) The interrupt request bit for an interrupt request generated during period 2 is set to "1" at timing point IR1 or IR2. The timing point at which the bit is set to "1" varies depending on conditions. When two or more interrupt requests are generated during the period 2, each request bit may be set to "1" at timing point IR1 or IR2 separately.

Fig. 21 Timing of interrupt request generation, interrupt request bit, and interrupt acceptance

■ Notes on Interrupts

When setting the followings, the interrupt request bit of the corresponding interrupt may be set to "1".
<When switching external interrupt active edge>
- INT_0 interrupt edge selection bit
  (bit 0 of Interrupt edge selection register (address $003A_{16}$))
- INT_1 interrupt edge selection bit
  (bit 1 of Interrupt edge selection register)
- $CNTR_0$ active edge switch bit
  (bit 2 of timer X mode register (address $002B_{16}$))
- $CNTR_1$ active edge switch bit
  (bit 6 of timer A mode register (address $100D_{16}$))

If it is not necessary to generate an interrupt synchronized with these settings, take the following sequence.
(1) Set the corresponding enable bit to "0" (disabled).
(2) Set the interrupt edge selection bit (the active edge switch bit) or the interrupt source bit.
(3) Set the corresponding interrupt request bit to "0" after one or more instructions have been executed.
(4) Set the corresponding interrupt enable bit to "1" (enabled).

Key Input Interrupt (Key-On Wake-Up)

A key-on wake-up interrupt request is generated by applying “L” level to any pin of port P0 that has been set to input mode.
In other words, it is generated when the AND of input level goes from “1” to “0”. An example of using a key input interrupt is shown in Fig. 22, where an interrupt request is generated by pressing one of the keys provided as an active-low key matrix which uses ports P0$_0$ to P0$_3$ as input ports.

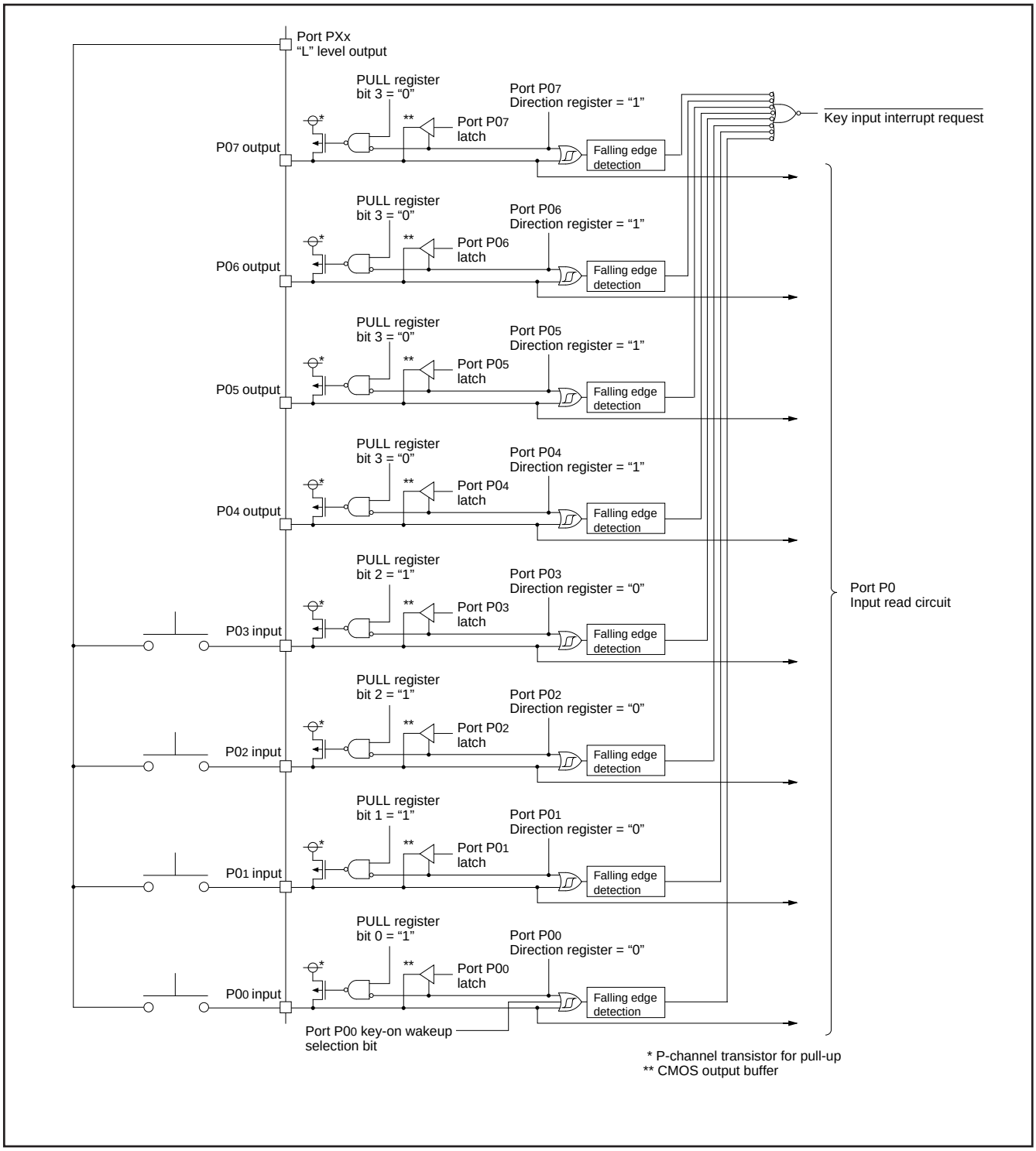


Fig. 22 Connection example when using key input interrupt and port P0 block diagram

Timers

The 7544 Group has 3 timers: timer 1, timer A and timer X.
The division ratio of every timer and prescaler is 1/(n+1) provided that the value of the timer latch or prescaler is n.
All the timers are down count timers. When a timer reaches "0", an underflow occurs at the next count pulse, and the corresponding timer latch is reloaded into the timer. When a timer underflows, the interrupt request bit corresponding to each timer is set to "1".

●Timer 1

Timer 1 is an 8-bit timer and counts the prescaler output.
When Timer 1 underflows, the timer 1 interrupt request bit is set to "1".
Prescaler 1 is an 8-bit prescaler and counts the signal selected by the timer 1 count source selection bit.
Prescaler 1 and Timer 1 have the prescaler 1 latch and the timer 1 latch to retain the reload value, respectively. The value of prescaler 1 latch is set to Prescaler 1 when Prescaler 1 underflows. The value of timer 1 latch is set to Timer 1 when Timer 1 underflows.
When writing to Prescaler 1 (PRE1) is executed, the value is written to both the prescaler 1 latch and Prescaler 1.
When writing to Timer 1 (T1) is executed, the value is written to both the timer 1 latch and Timer 1.
When reading from Prescaler 1 (PRE1) and Timer 1 (T1) is executed, each count value is read out.
Timer 1 always operates in the timer mode.
Prescaler 1 counts the signal selected by the timer 1 count source selection bit. Each time the count clock is input, the contents of Prescaler 1 is decremented by 1. When the contents of Prescaler 1 reach "00_{16}", an underflow occurs at the next count clock, and the prescaler 1 latch is reloaded into Prescaler 1 and count continues. The division ratio of Prescaler 1 is 1/(n+1) provided that the value of Prescaler 1 is n.
The contents of Timer 1 is decremented by 1 each time the underflow signal of Prescaler 1 is input. When the contents of Timer 1 reach "00_{16}", an underflow occurs at the next count clock, and the timer 1 latch is reloaded into Timer 1 and count continues. The division ratio of Timer 1 is 1/(m+1) provided that the value of Timer 1 is m. Accordingly, the division ratio of Prescaler 1 and Timer 1 is 1/((n+1)×(m+1)) provided that the value of Prescaler 1 is n and the value of Timer 1 is m.
Timer 1 cannot stop counting by software.

●Timer A

Timer A is a 16-bit timer and counts the signal selected by the timer A count source selection bit. When Timer A underflows, the timer A interrupt request bit is set to "1".
Timer A consists of the low-order of Timer A (TAL) and the high-order of Timer A (TAH).
Timer A has the timer A latch to retain the reload value. The value of timer A latch is set to Timer A at the timing shown below.
• When Timer A underflows.
• When an active edge is input from $CNTR_1$ pin (valid only when period measurement mode and pulse width HL continuously measurement mode).
When writing to both the low-order of Timer A (TAL) and the high-order of Timer A (TAH) is executed, the value is written to both the timer A latch and Timer A.
When reading from the low-order of Timer A (TAL) and the high-order of Timer A (TAH) is executed, the following values are read out according to the operating mode.
• In timer mode, event counter mode:
The count value of Timer A is read out.
• In period measurement mode, pulse width HL continuously measurement mode:
The measured value is read out.

Be sure to write to/read out the low-order of Timer A (TAL) and the high-order of Timer A (TAH) in the following order;
Read
Read the high-order of Timer A (TAH) first, and the low-order of Timer A (TAL) next and be sure to read out both TAH and TAL.
Write
Write to the low-order of Timer A (TAL) first, and the high-order of Timer A (TAH) next and be sure to write to both TAL and TAH.

Timer A can be selected in one of 4 operating modes by setting the timer A mode register.

(1) Timer mode

Timer A counts the selected by the timer A count source selection bit. Each time the count clock is input, the contents of Timer A is decremented by 1. When the contents of Timer A reach "0000_{16}", an underflow occurs at the next count clock, and the timer A latch is reloaded into Timer A. The division ratio of Timer A is 1/(n+1) provided that the value of Timer A is n.

(2) Period measurement mode

In the period measurement mode, the pulse period input from the $P0_0$/$CNTR_1$ pin is measured.
$CNTR_1$ interrupt request is generated at rising/falling edge of $CNTR_1$ pin input signal. Simultaneously, the value in the timer A latch is reloaded in Timer A and count continues. The active edge of $CNTR_1$ pin input signal can be selected from rising or falling by the $CNTR_1$ active edge switch bit .The count value when trigger input from $CNTR_1$ pin is accepted is retained until Timer A is read once.

(3) Event counter mode

Timer A counts signals input from the P00/CNTR1 pin.

Except for this, the operation in event counter mode is the same as in timer mode.

The active edge of CNTR1 pin input signal can be selected from rising or falling by the CNTR1 active edge switch bit .

(4) Pulse width HL continuously measurement mode

In the pulse width HL continuously measurement mode, the pulse width ("H" and "L" levels) input to the P00/CNTR1 pin is measured. CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode.

The count value when trigger input from the CNTR1 pin is accepted is retained until Timer A is read once.

Timer A can stop counting by setting "1" to the timer A count stop bit in any mode.

Also, when Timer A underflows, the timer A interrupt request bit is set to "1".

Note on Timer A is described below;

■ Note on Timer A

CNTR1 interrupt active edge selection

CNTR1 interrupt active edge depends on the CNTR1 active edge switch bit.

When this bit is "0", the CNTR1 interrupt request bit is set to "1" at the falling edge of the CNTR1 pin input signal. When this bit is "1", the CNTR1 interrupt request bit is set to "1" at the rising edge of the CNTR1 pin input signal.

However, in the pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge switch bit.

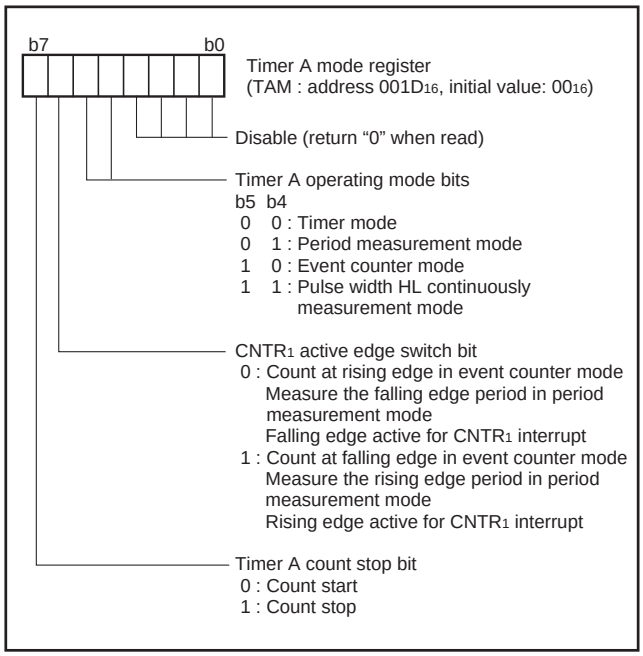


Fig. 23 Structure of timer A mode register

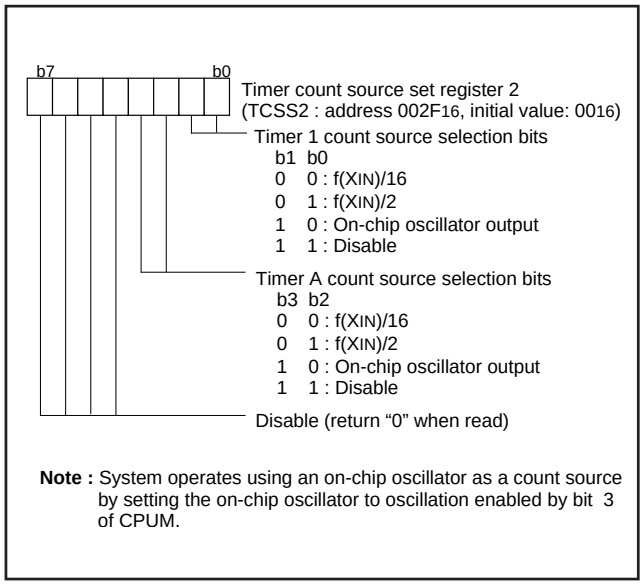


Fig. 24 Timer count source set register 2

●Timer X

Timer X is an 8-bit timer and counts the prescaler X output.
When Timer X underflows, the timer X interrupt request bit is set to “1”.
Prescaler X is an 8-bit prescaler and counts the signal selected by the timer X count source selection bit.
Prescaler X and Timer X have the prescaler X latch and the timer X latch to retain the reload value, respectively. The value of prescaler X latch is set to Prescaler X when Prescaler X underflows. The value of timer X latch is set to Timer X when Timer X underflows.
When writing to Prescaler X (PREX) and Timer X (TX) is executed, writing to “latch only” or “latch and prescaler (timer)” can be selected by the setting value of the timer X write control bit.
When reading from Prescaler X (PREX) and Timer X (TX) is executed, each count value is read out.

Timer X can be selected in one of 4 operating modes by setting the timer X operating mode bits of the timer X mode register.

(1) Timer mode

Prescaler X counts the count source selected by the timer X count source selection bits. Each time the count clock is input, the contents of Prescaler X is decremented by 1. When the contents of Prescaler X reach “00_{16}”, an underflow occurs at the next count clock, and the prescaler X latch is reloaded into Prescaler X and count continues. The division ratio of Prescaler X is 1/(n+1) provided that the value of Prescaler X is n.
The contents of Timer X is decremented by 1 each time the underflow signal of Prescaler X is input. When the contents of Timer X reach “00_{16}”, an underflow occurs at the next count clock, and the timer X latch is reloaded into Timer X and count continues. The division ratio of Timer X is 1/(m+1) provided that the value of Timer X is m. Accordingly, the division ratio of Prescaler X and Timer X is 1/((n+1)×(m+1)) provided that the value of Prescaler X is n and the value of Timer X is m.

(2) Pulse output mode

In the pulse output mode, the waveform whose polarity is inverted each time timer X underflows is output from the $CNTR_0$ pin.
The output level of $CNTR_0$ pin can be selected by the $CNTR_0$ active edge switch bit. When the $CNTR_0$ active edge switch bit is “0”, the output of $CNTR_0$ pin is started at “H” level. When this bit is “1”, the output is started at “L” level.
Also, the inverted waveform of pulse output from $CNTR_0$ pin can be output from TX_{OUT} pin by setting “1” to the $P0_3/TX_{OUT}$ output valid bit.
When using a timer in this mode, set the port $P1_4$ and $P0_3$ direction registers to output mode.

(3) Event counter mode

The timer A counts signals input from the $P1_4/CNTR_0$ pin.
Except for this, the operation in event counter mode is the same as in timer mode.
The active edge of $CNTR_0$ pin input signal can be selected from rising or falling by the $CNTR_0$ active edge switch bit .

(4) Pulse width measurement mode

In the pulse width measurement mode, the pulse width of the signal input to $P1_4/CNTR_0$ pin is measured.
The operation of Timer X can be controlled by the level of the signal input from the $CNTR_0$ pin.
When the $CNTR_0$ active edge switch bit is “0”, the signal selected by the timer X count source selection bit is counted while the input signal level of $CNTR_0$ pin is “H”. The count is stopped while the pin is “L”. Also, when the $CNTR_0$ active edge switch bit is “1”, the signal selected by the timer X count source selection bit is counted while the input signal level of $CNTR_0$ pin is “L”. The count is stopped while the pin is “H”.

Timer X can stop counting by setting “1” to the timer X count stop bit in any mode.
Also, when Timer X underflows, the timer X interrupt request bit is set to “1”.

Note on Timer X is described below;

■ Note on Timer X

$CNTR_0$ interrupt active edge selection
$CNTR_0$ interrupt active edge depends on the $CNTR_0$ active edge switch bit.
When this bit is “0”, the $CNTR_0$ interrupt request bit is set to “1” at the falling edge of $CNTR_0$ pin input signal. When this bit is “1”, the $CNTR_0$ interrupt request bit is set to “1” at the rising edge of $CNTR_0$ pin input signal.

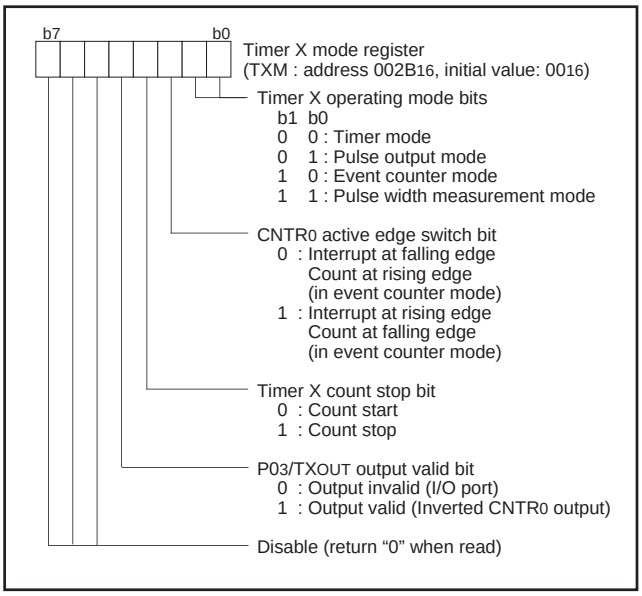


Fig. 25 Structure of timer X mode register

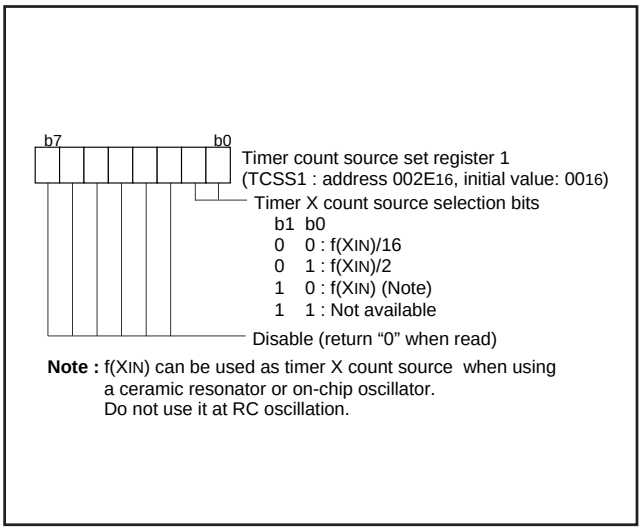


Fig. 26 Timer count source set register 1

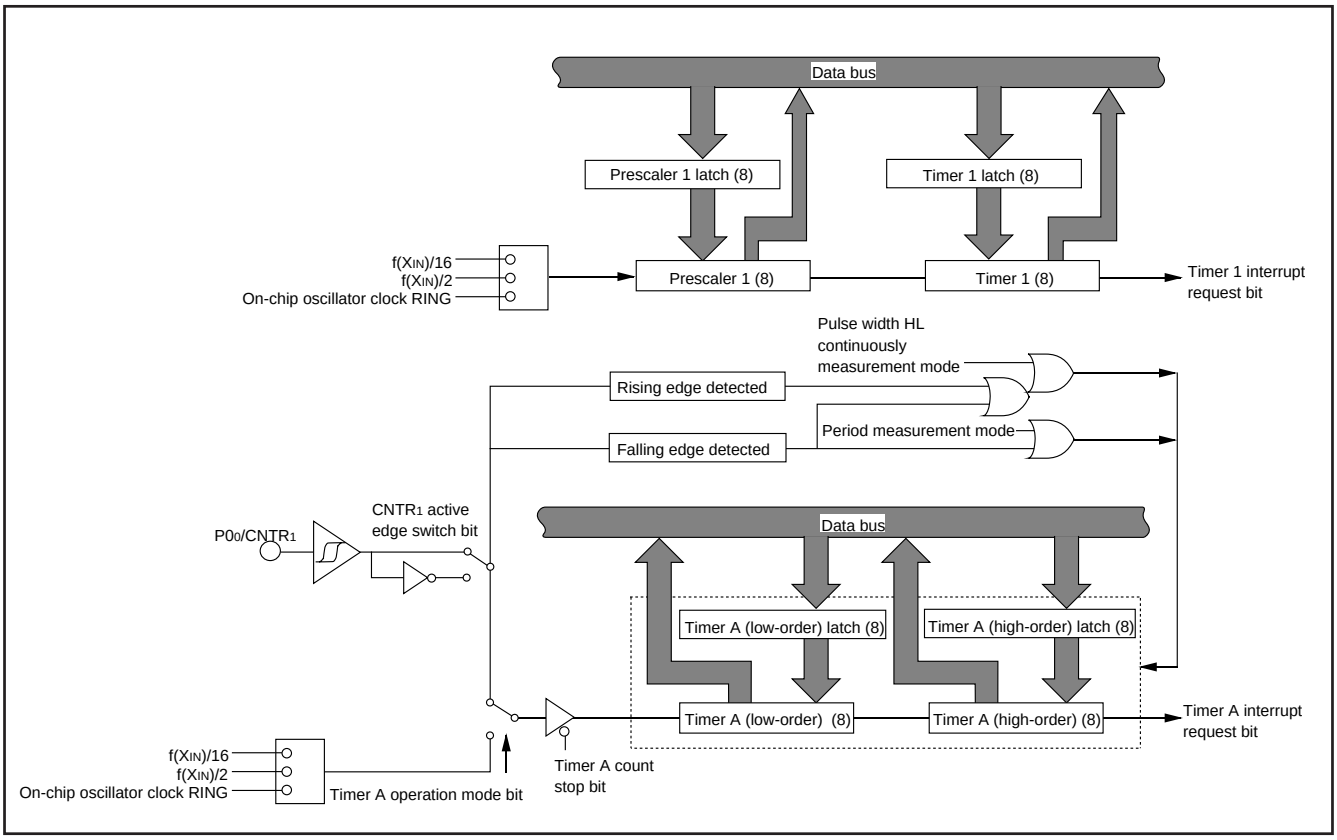


Fig. 27 Block diagram of timer 1 and timer A

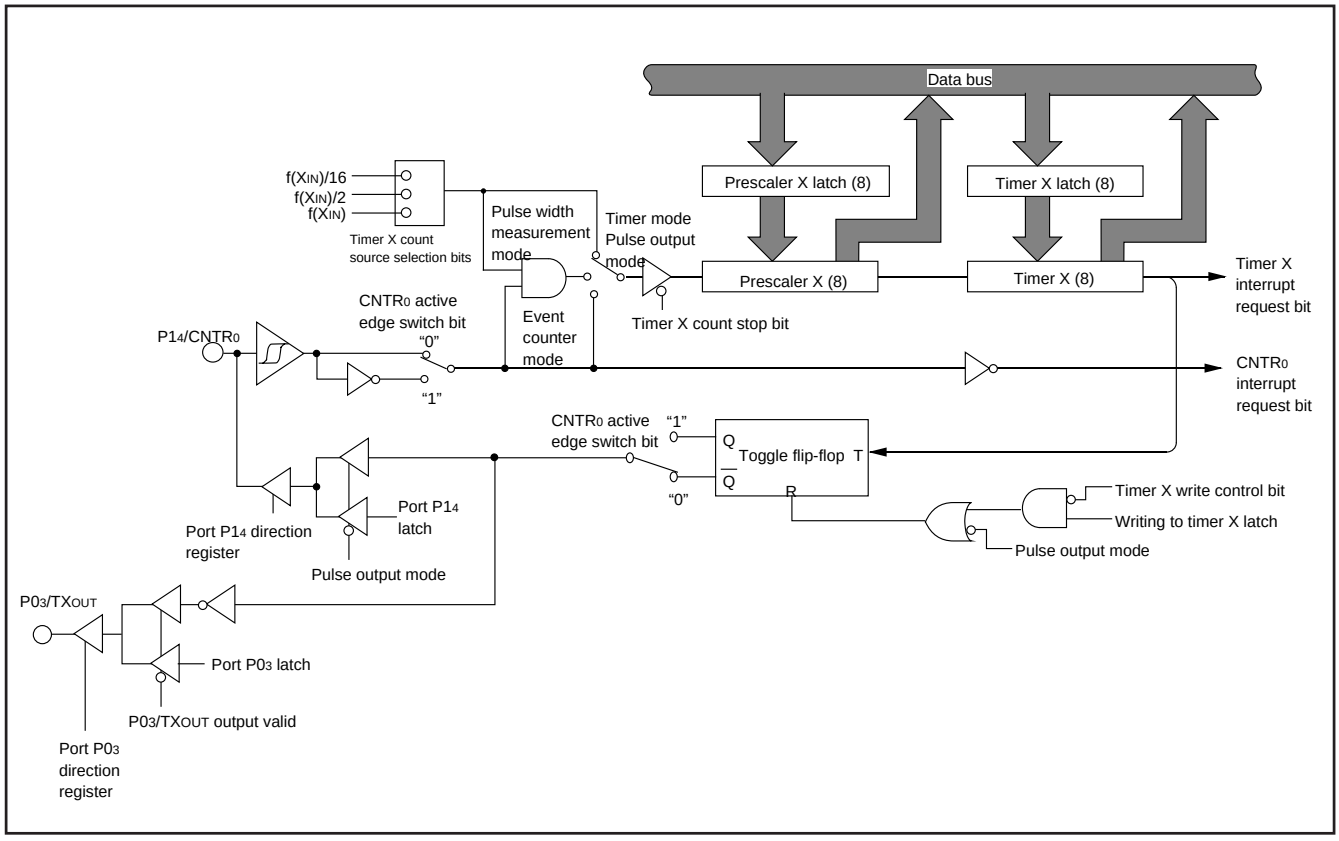


Fig. 28 Block diagram of timer X

Serial Interface
●Serial I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O mode selection bit of the serial I/O control register (bit 6) to “1”.

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

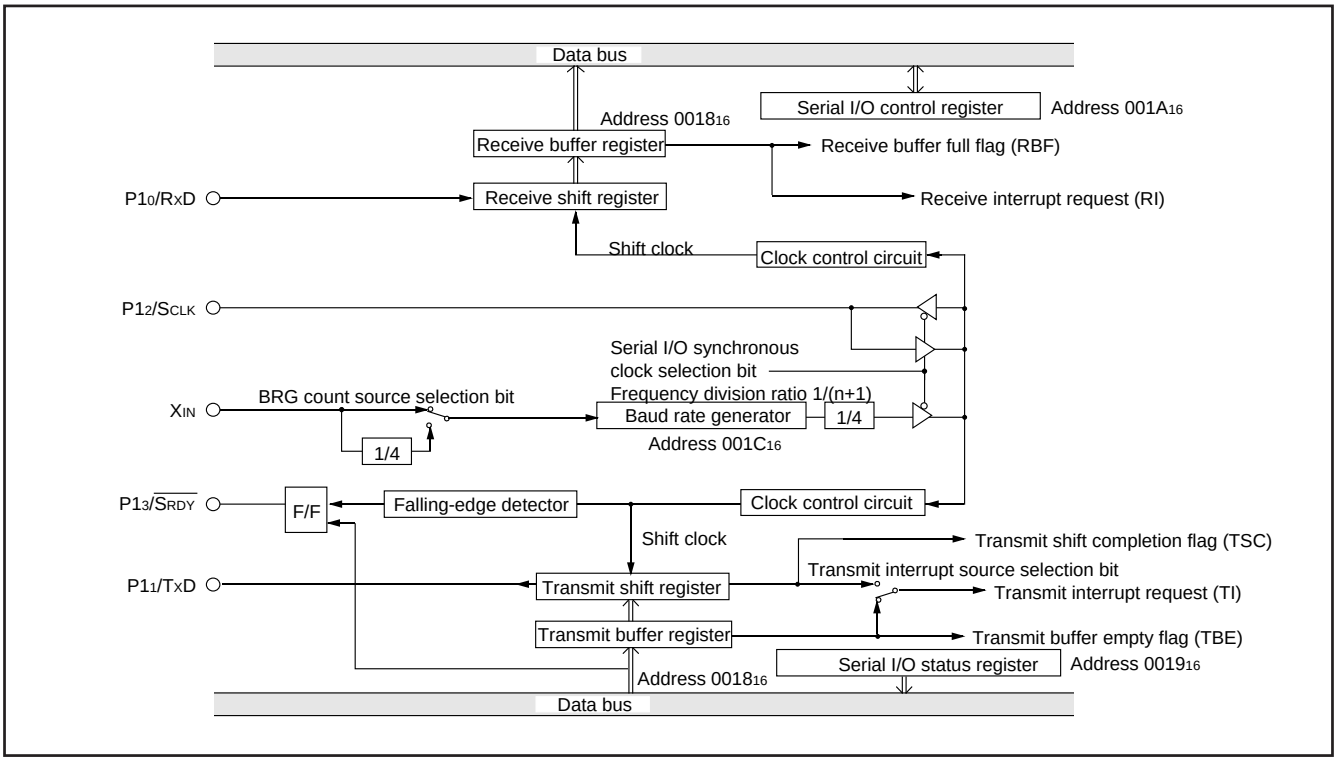
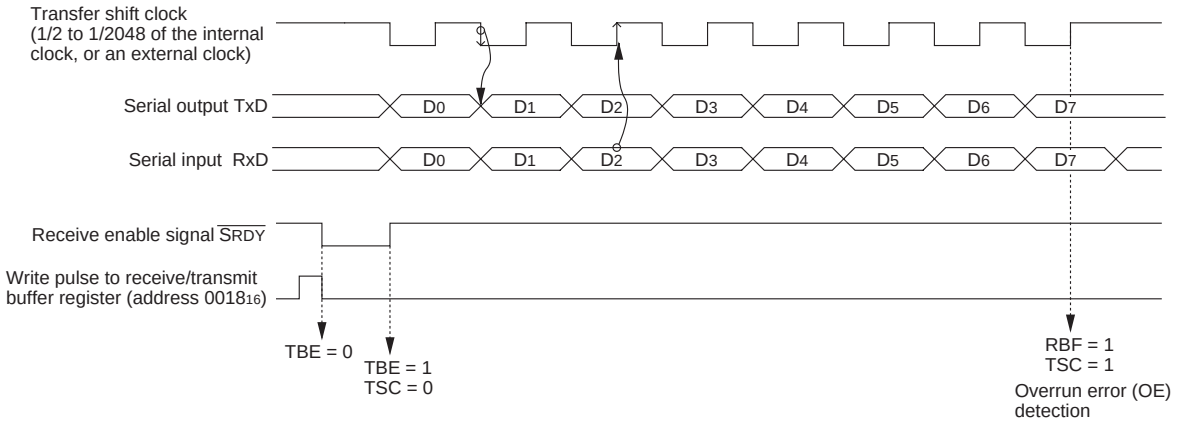


Fig. 29 Block diagram of clock synchronous serial I/O



Notes 1: As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O control register.

2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.

3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes “1” .

Fig. 30 Operation of clock synchronous serial I/O function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

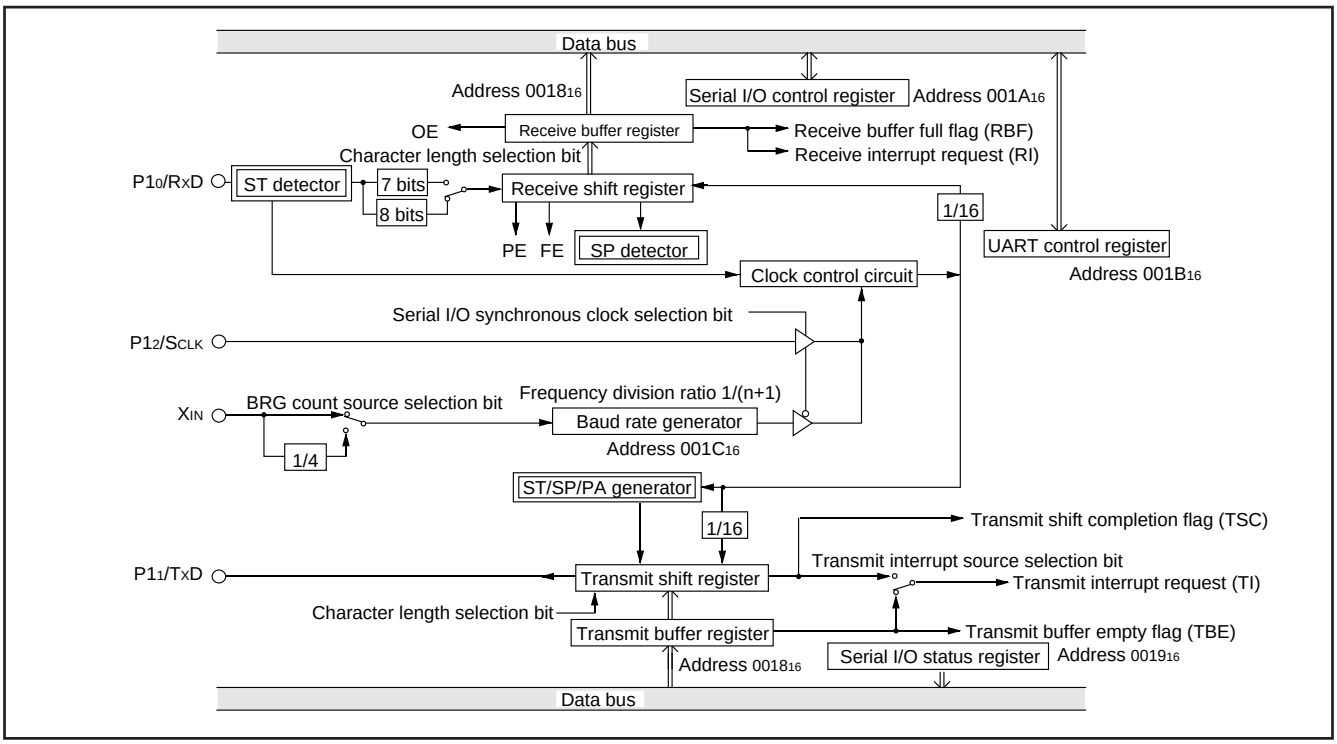
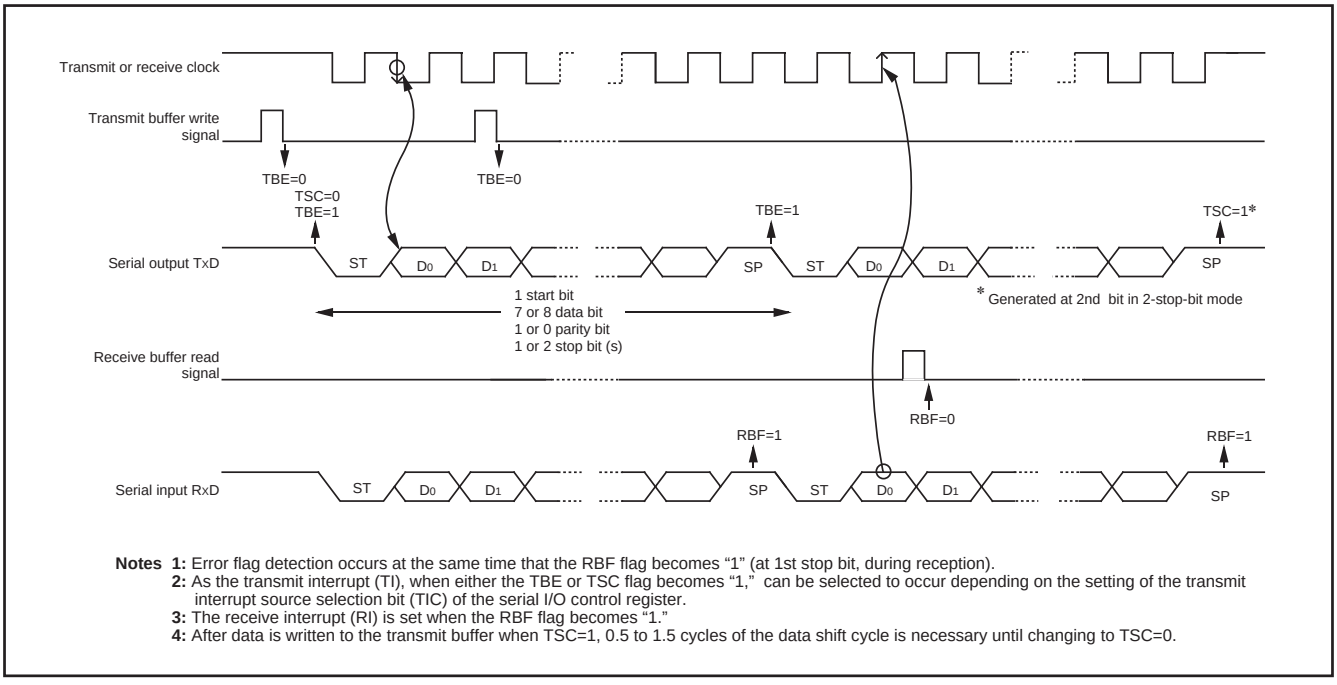


Fig. 31 Block diagram of UART serial I/O



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1,” can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3: The receive interrupt (RI) is set when the RBF flag becomes “1.”
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 32 Operation of UART serial I/O function

[Transmit buffer register/receive buffer register (TB/RB)] 0018$_{16}$

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O status register (SIOSTS)] 0019$_{16}$

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the serial I/O control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit of the serial I/O control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O control register (SIOCON)] 001A$_{16}$

The serial I/O control register consists of eight control bits for the serial I/O function.

[UART control register (UARTCON)] 001B$_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P11/TXD pin.

[Baud rate generator (BRG)] 001C$_{16}$

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■ Notes on serial I/O

• Serial I/O interrupt

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
② Set the transmit enable bit to "1".
③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
④ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

• I/O pin function when serial I/O is enabled.

The functions of P12 and P13 are switched with the setting values of a serial I/O mode selection bit and a serial I/O synchronous clock selection bit as follows.

(1) Serial I/O mode selection bit → "1" :
Clock synchronous type serial I/O is selected.
Setup of a serial I/O synchronous clock selection bit
"0" : P12 pin turns into an output pin of a synchronous clock.
"1" : P12 pin turns into an input pin of a synchronous clock.
Setup of a SRDY output enable bit (SRDY)
"0" : P13 pin can be used as a normal I/O pin.
"1" : P13 pin turns into a SRDY output pin.

(2) Serial I/O mode selection bit → "0" :
Clock asynchronous (UART) type serial I/O is selected.
Setup of a serial I/O synchronous clock selection bit
"0": P12 pin can be used as a normal I/O pin.
"1": P12 pin turns into an input pin of an external clock.
When clock asynchronous (UART) type serial I/O is selected, it is P13 pin. It can be used as a normal I/O pin.

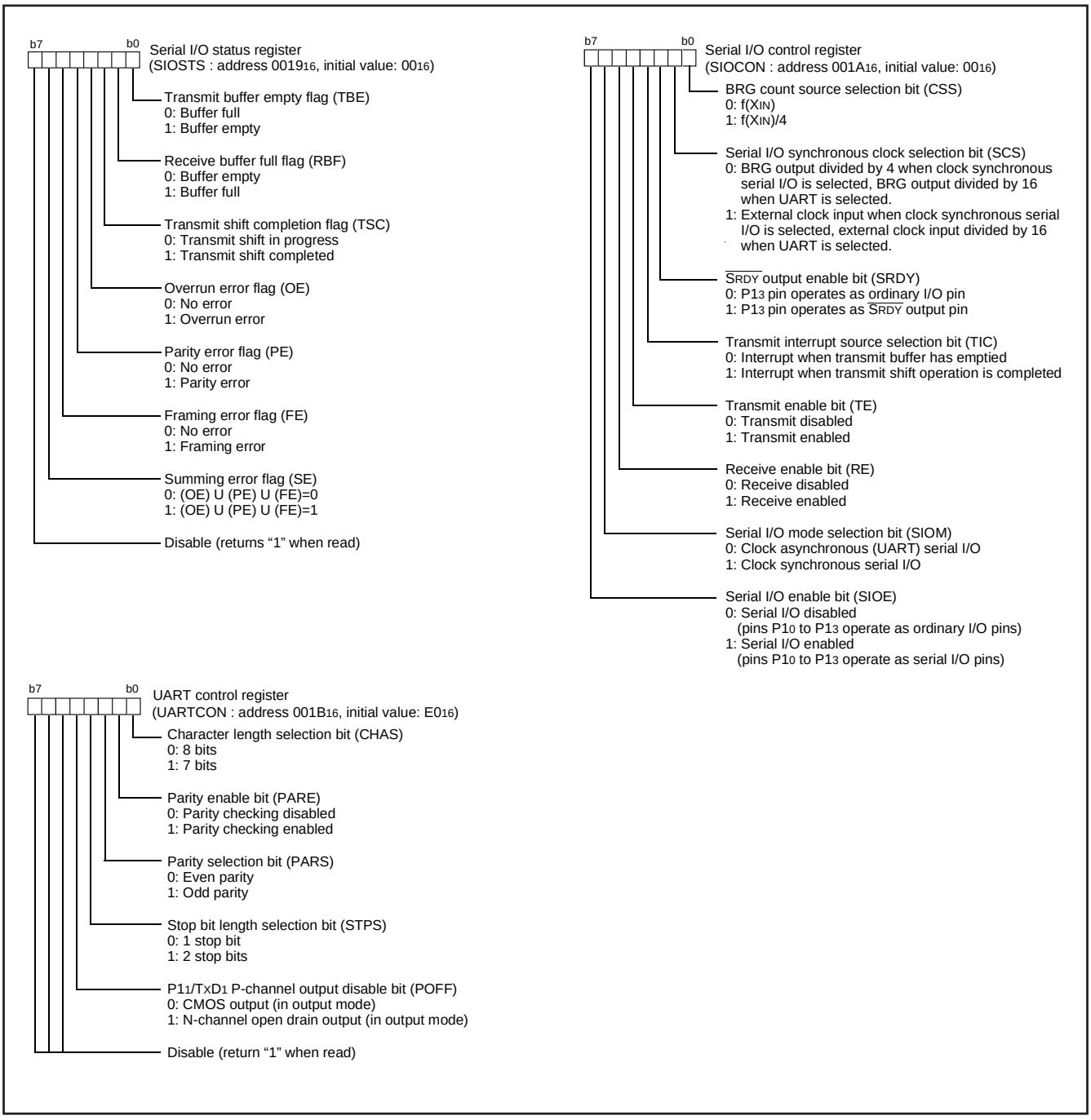


Fig. 33 Structure of serial I/O-related registers

A/D Converter

The functional blocks of the A/D converter are described below.

[A/D conversion register] AD

The A/D conversion register is a read-only register that stores the result of A/D conversion. Do not read out this register during an A/D conversion.

[A/D control register] ADCON

The A/D control register controls the A/D converter. Bit 2 to 0 are analog input pin selection bits. Bit 4 is the AD conversion completion bit. The value of this bit remains at “0” during A/D conversion, and changes to “1” at completion of A/D conversion.
A/D conversion is started by setting this bit to “0”.

[Comparison voltage generator]

The comparison voltage generator divides the voltage between AVSS and VREF by 256, and outputs the divided voltages.

[Channel selector]

The channel selector selects one of ports P25/AN5 to P20/AN0, and inputs the voltage to the comparator.

[Comparator and control circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores its result into the A/D conversion register. When A/D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to “1”. Because the comparator is constructed linked to a capacitor, set f(XIN) to 500 kHz or more during A/D conversion.

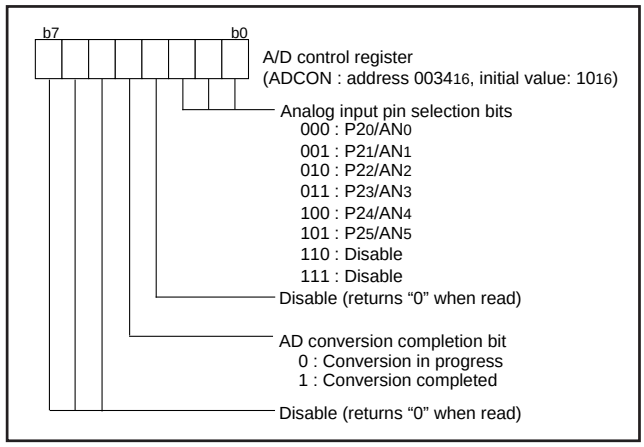


Fig. 34 Structure of A/D control register

■ Notes on A/D converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Make sure that f(XIN) is 500 kHz or more during A/D conversion.
As for AD translation accuracy, on the following operating conditions, accuracy may become low.

(1) Since the analog circuit inside a microcomputer becomes sensitive to noise when VREF voltage is set up lower than Vcc voltage, accuracy may become low rather than the case where VREF voltage and Vcc voltage are set up to the same value..

(2) When VREF voltage is lower than [3.0 V], the accuracy at the low temperature may become extremely low compared with that at room temperature. When the system would be used at low temperature, the use at VREF=3.0 V or more is recommended.

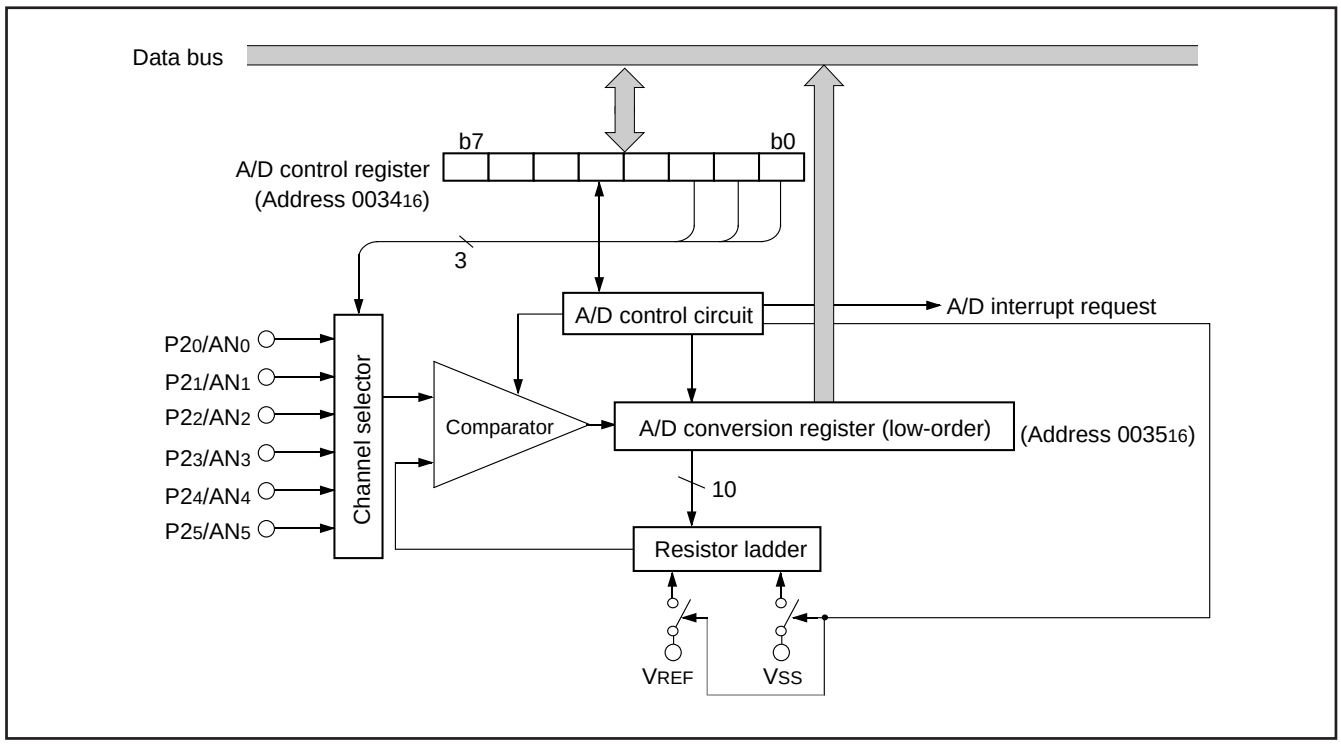


Fig. 35 Block diagram of A/D converter

Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway. The watchdog timer consists of an 8-bit watchdog timer H and an 8-bit watchdog timer L, being a 16-bit counter.

Standard operation of watchdog timer

The watchdog timer stops when the watchdog timer control register (address 0039_{16}) is not set after reset. Writing an optional value to the watchdog timer control register (address 0039_{16}) causes the watchdog timer to start to count down. When the watchdog timer H underflows, an internal reset occurs. Accordingly, it is programmed that the watchdog timer control register (address 0039_{16}) can be set before an underflow occurs.
When the watchdog timer control register (address 0039_{16}) is read, the values of the high-order 6-bit of the watchdog timer H, STP instruction function selection bit and watchdog timer H count source selection bit are read.

Initial value of watchdog timer

By a reset or writing to the watchdog timer control register (address 0039_{16}), the watchdog timer H is set to "FF_{16}" and the watchdog timer L is set to "FF_{16}".

Operation of watchdog timer H count source selection bit

A watchdog timer H count source can be selected by bit 7 of the watchdog timer control register (address 0039_{16}). When this bit is "0", the count source becomes a watchdog timer L underflow signal. The detection time is 131.072 ms at f(X_{IN})=8 MHz.
When this bit is "1", the count source becomes f(X_{IN})/16 or on-chip oscillator/16. In this case, the detection time is 512 μs at f(X_{IN})=8 MHz.
This bit is cleared to "0" after reset.

Operation of STP instruction function selection bit

The function of the STP instruction can be set by the STP instruction function selection bit (bit 6 of WDTCON).
When "0" is set to this bit, system enters into the stop mode at the STP instruction execution.
When "1" is set to this bit, internal reset occurs at the STP instruction execution.
Once this bit is set to "1", it cannot be changed to "0" by program.
This bit is cleared to "0" after reset.

■ **Notes on watchdog timer**

1. The watchdog timer is operating during the wait mode. Write data to the watchdog timer control register to prevent timer underflow.

2. The watchdog timer stops during the stop mode. However, the watchdog timer is running during the oscillation stabilizing time after the **STP** instruction is released. In order to avoid the underflow of the watchdog timer, the watchdog timer count source selection bit (bit 7 of watchdog timer control register (address 0039_{16})) before executing the **STP** instruction.

3. The **STP** instruction function selection bit (bit 6 of watchdog timer control register (address 0039_{16})) can be rewritten only once after releasing reset. After rewriting it is disable to write any data to this bit.

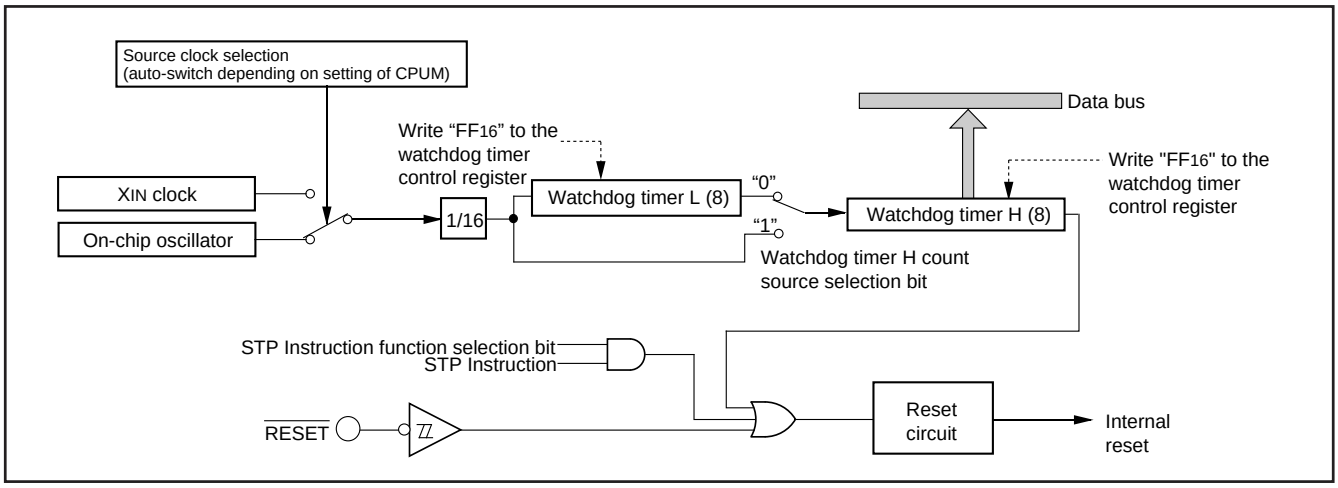


Fig. 36 Block diagram of watchdog timer

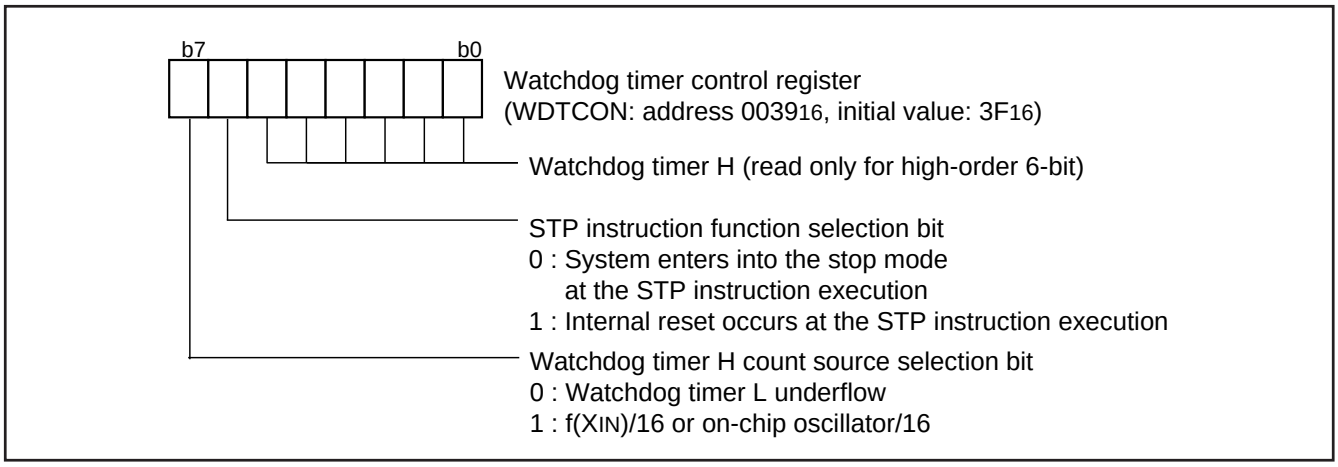


Fig. 37 Structure of watchdog timer control register

Reset Circuit

The 7544 group starts operation by the on-chip oscillator after system is released from reset.
Accordingly, when the rising of power supply voltage passes 2.2V, set the reset input voltage to become below 0.2Vcc (0.44V).
Moreover, switch CPU clock to the external oscillator after the rising of power supply voltage passes the minimum operation voltage and after an oscillation is stabilized.

Note: The minimum operation voltage is decided by the division ratio of an external oscillator's frequency and a CPU clock. Decide on an external oscillator's oscillation stabilizing time after fully evaluating an oscillator's stabilizing time used.

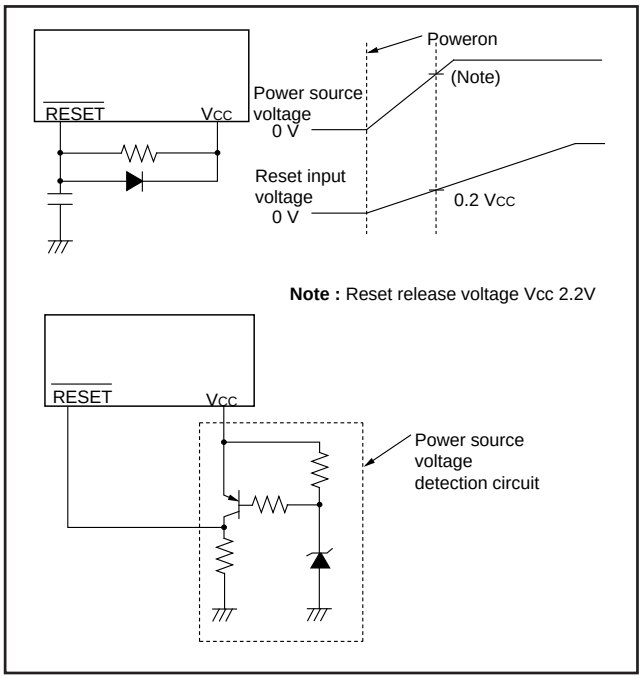


Fig. 38 Example of reset circuit

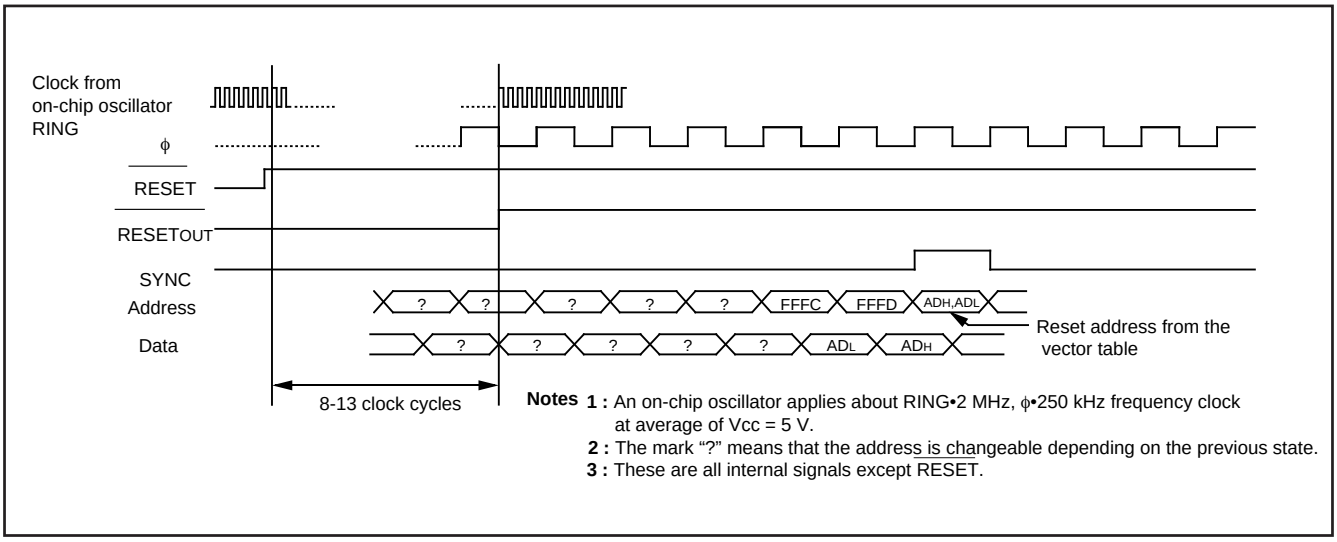


Fig. 39 Timing diagram at reset

		Address	Register contents
(1)	Port P0 direction register	0001_{16}	00_{16}
(2)	Port P1 direction register	0003_{16}	X X X 0 0 0 0 0
(3)	Port P2 direction register	0005_{16}	X X 0 0 0 0 0 0
(4)	Port P3 direction register	0007_{16}	0 X X 0 0 0 0 0
(5)	Pull-up control register	0016_{16}	00_{16}
(6)	Port P1P3 control register	0017_{16}	00_{16}
(7)	Serial I/O status register	0019_{16}	1 0 0 0 0 0 0 0
(8)	Serial I/O control register	$001A_{16}$	00_{16}
(9)	UART control register	$001B_{16}$	1 1 1 0 0 0 0 0
(10)	Timer A mode register	$001D_{16}$	00_{16}
(11)	Timer A (low-order)	$001E_{16}$	FF_{16}
(12)	Timer A (high-order)	$001F_{16}$	FF_{16}
(13)	Prescaler 1	0028_{16}	FF_{16}
(14)	Timer 1	0029_{16}	0 0 0 0 0 0 0 1
(15)	Timer X mode register	$002B_{16}$	00_{16}
(16)	Prescaler X	$002C_{16}$	FF_{16}
(17)	Timer X	$002D_{16}$	FF_{16}
(18)	Timer count source set register 1	$002E_{16}$	00_{16}
(19)	Timer count source set register 2	$002F_{16}$	00_{16}
(20)	A/D control register	0034_{16}	0 0 0 1 0 0 0 0
(21)	MISRG	0038_{16}	00_{16}
(22)	Watchdog timer control register	0039_{16}	0 0 1 1 1 1 1 1
(23)	Interrupt edge selection register	$003A_{16}$	00_{16}
(24)	CPU mode register	$003B_{16}$	1 0 0 0 0 0 0 0
(25)	Interrupt request register 1	$003C_{16}$	00_{16}
(26)	Interrupt request register 2	$003D_{16}$	00_{16}
(27)	Interrupt control register 1	$003E_{16}$	00_{16}
(28)	Interrupt control register 2	$003F_{16}$	00_{16}
(29)	Processor status register	(PS)	X X X X X 1 X X
(30)	Program counter	(PC_H)	Contents of address $FFFD_{16}$
		(PC_L)	Contents of address $FFFC_{16}$

X : Undefined

The content of other registers is undefined when the microcomputer is reset.
The initial values must be surely set before you use it.

Fig. 40 Internal status of microcomputer at reset

Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between XIN and XOUT, and an RC oscillation circuit can be formed by connecting a resistor and a capacitor.
Use the circuit constants in accordance with the resonator manufacturer's recommended values.
No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. (An external feed-back resistor may be needed depending on conditions.)

(1) On-chip oscillator operation

When the MCU operates by the on-chip oscillator for the main clock, connect XIN pin to VCC and leave XOUT pin open.
The clock frequency of the on-chip oscillator depends on the supply voltage and the operation temperature range.
Be careful that variable frequencies when designing application products.

(2) Ceramic resonator and quartz-crystal oscillator

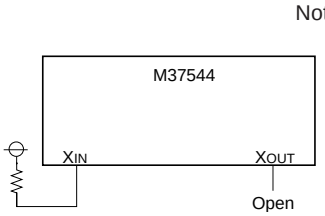
When the ceramic resonator and quartz-crystal oscillator is used for the main clock, connect the ceramic/quartz-crystal oscillator and the external circuit to pins XIN and XOUT at the shortest distance. A feedback resistor is built in between pins XIN and XOUT.

(3) RC oscillation

When the RC oscillation is used for the main clock, connect the XIN pin and XOUT pin to the external circuit of resistor R and the capacitor C at the shortest distance.
The frequency is affected by a capacitor, a resistor and a microcomputer.
So, set the constants within the range of the frequency limits.

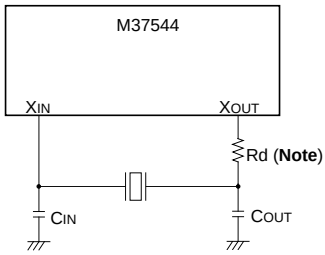
(4) External clock

When the external signal clock is used for the main clock, connect the XIN pin to the clock source and leave XOUT pin open.



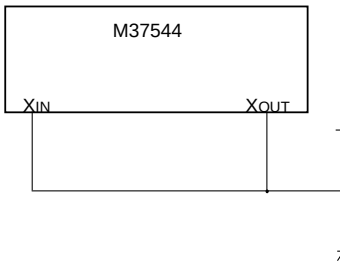
Note: The clock frequency of the on-chip oscillator depends on the supply voltage and the operation temperature range.
Be careful that variable frequencies and obtain the sufficient margin.

Fig. 41 Processing of XIN and XOUT pins at on-chip oscillator operation



Note: Insert a damping resistor if required.
The resistance will vary depending on the oscillator and the oscillation drive capacity setting.
Use the value recommended by the maker of the oscillator.
Also, if the oscillator manufacturer's data sheet specifies that a feedback resistor be added external to the chip through a feedback resistor exists on-chip, insert a feedback resistor between XIN and XOUT following the instruction.

Fig. 42 External circuit of ceramic resonator and quartz-crystal oscillator



Note: Connect the external circuit of resistor R and the capacitor C at the shortest distance.
The frequency is affected by a capacitor, a resistor and a microcomputer.
So, set the constants within the range of the frequency limits.

Fig. 43 External circuit of RC oscillation

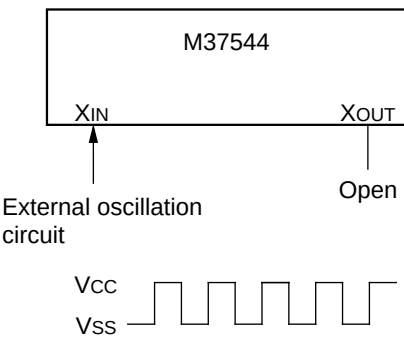


Fig. 44 External clock input circuit

(1) Oscillation control

• Stop mode

When the STP instruction is executed, the internal clock φ stops at an "H" level and the XIN oscillator stops. At this time, timer 1 is set to "01$_{16}$" and prescaler 1 is set to "FF$_{16}$" when the oscillation stabilization time set bit after release of the STP instruction is "0". On the other hand, timer 1 and prescaler 1 are not set when the above bit is "1". Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used. Single selected by the timer 1 count source selection bit is connected to the input of prescaler 1. When an external interrupt is accepted, oscillation is restarted but the internal clock φ remains at "H" until timer 1 underflows. As soon as timer 1 underflows, the internal clock φ is supplied. This is because when a ceramic/quartz-crystal oscillator is used, some time is required until a start of oscillation. In case oscillation is restarted by reset, no wait time is generated. So apply an "L" level to the $\overline{\text{RESET}}$ pin while oscillation becomes stable. Also, the STP instruction cannot be used while CPU is operating by an on-chip oscillator.

• Wait mode

If the WIT instruction is executed, the internal clock φ stops at an "H" level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

■ Notes on clock generating circuit

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 1 after fully appreciating the oscillation stabilization time of the oscillator to be used.

• Switch of ceramic/quartz-crystal and RC oscillations

After releasing reset the operation starts by starting an on-chip oscillator. Then, a ceramic/quartz-crystal oscillation or an RC oscillation is selected by setting bit 5 of the CPU mode register.

• Double-speed mode

When a ceramic/quartz-crystal oscillation is selected, a double-speed mode can be used. Do not use it when an RC oscillation is selected.

• CPU mode register

Bits 5, 1 and 0 of CPU mode register are used to select oscillation mode and to control operation modes of the microcomputer. In order to prevent the dead-lock by error-writing (ex. program run-away), these bits can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. (The emulator MCU "M37544RSS" is excluded.)

Also, when the read-modify-write instructions (SEB, CLB) are executed to bits 2 to 4, 6 and 7, bits 5, 1 and 0 are locked.

• Clock division ratio, XIN oscillation control, on-chip oscillator control

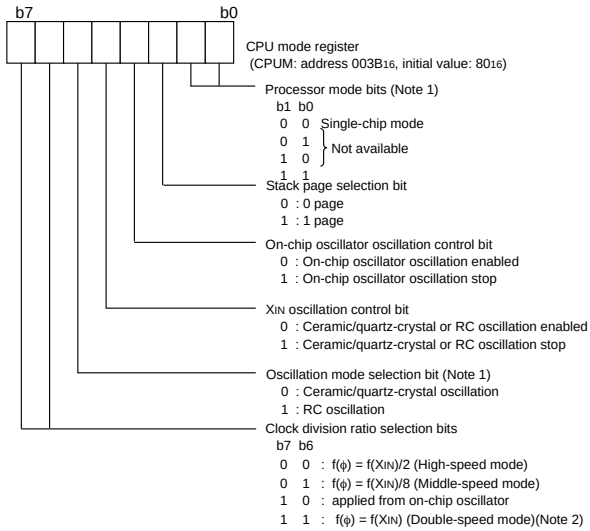
The state transition shown in Fig. 49 can be performed by setting the clock division ratio selection bits (bits 7 and 6), XIN oscillation control bit (bit 4), on-chip oscillator oscillation control bit (bit 3) of CPU mode register. Be careful of notes on use in Fig. 49.

• Count source (Timer 1, Timer A, Timer X, Serial I/O, A/D converter, Watchdog timer)

The count sources of these functions are affected by the clock division selection bit of the CPU mode register.

The f(XIN) clock is supplied to the watchdog timer when selecting f(XIN) as the CPU clock.

The on-chip oscillator output is supplied to these functions when selecting the on-chip oscillator output as the CPU clock.



Note 1: The bit can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. However, by reset the bit is initialized and can be rewritten, again.
(It is not disable to write any data to the bit for emulator MCU "M37544RSS".)

2: These bits are used only when a ceramic/quartz-crystal oscillation is selected. Do not use these when an RC oscillation is selected.

Fig. 45 Structure of CPU mode register

● Oscillation stop detection circuit

The oscillation stop detection circuit is used for reset occurrence when a ceramic resonator or an oscillation circuit stops by disconnection. When internal reset occurs, reset because of oscillation stop can be detected by setting “1” to the oscillation stop detection status bit.

Also, when using the oscillation stop detection circuit, an on-chip oscillator is required.

Fig. 49 shows the state transition.

The oscillation stop detection status bit retains “1”, not initialized, when the oscillation stop reset occurs. The oscillation stop detection status bit is initialized to “0” when the external reset occurs. Accordingly, reset by oscillation stop can be confirmed by using this bit.

■ Notes on Oscillation Stop Detection Circuit

- Oscillation stop detection status bit is initialized by the following operation.
  (1) External reset
  (2) Write “0” data to the ceramic or RC oscillation stop detection function active bit.
- The oscillation stop detection circuit is not included in the emulator MCU “M37544RSS”.

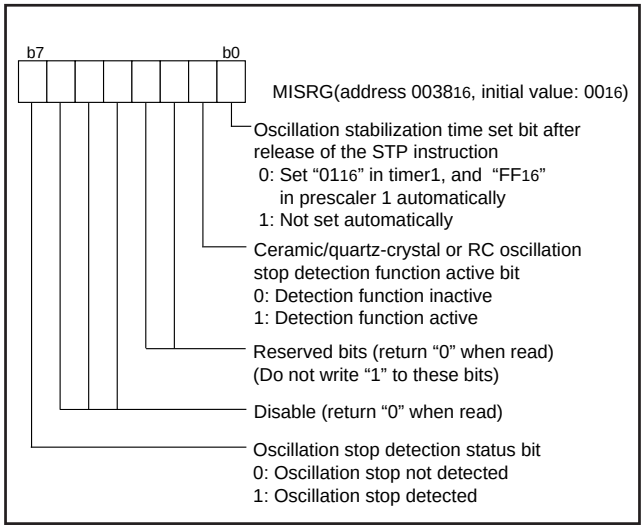


Fig. 46 Structure of MISRG

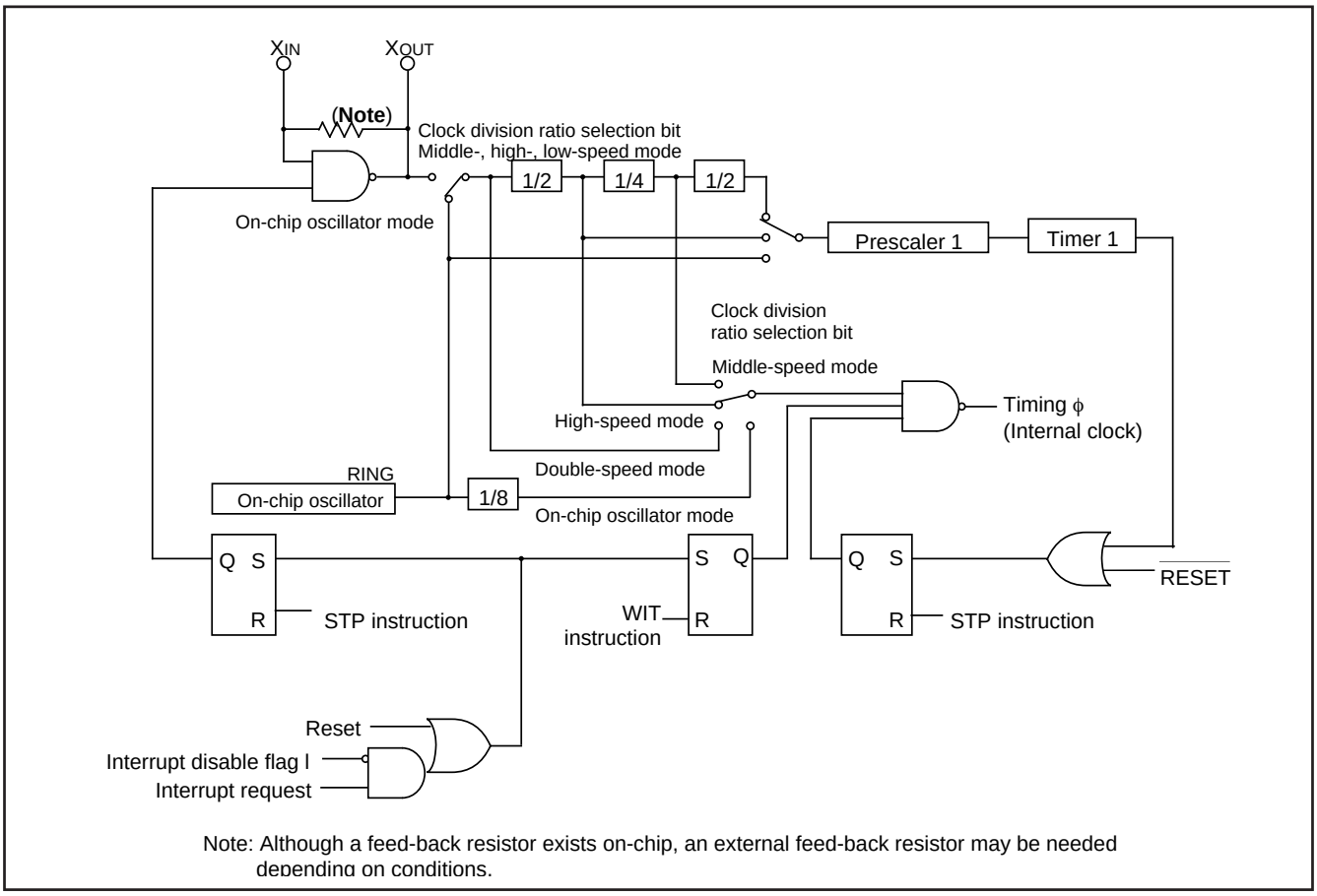


Fig. 47 Block diagram of internal clock generating circuit (for ceramic/quartz-crystal resonator)

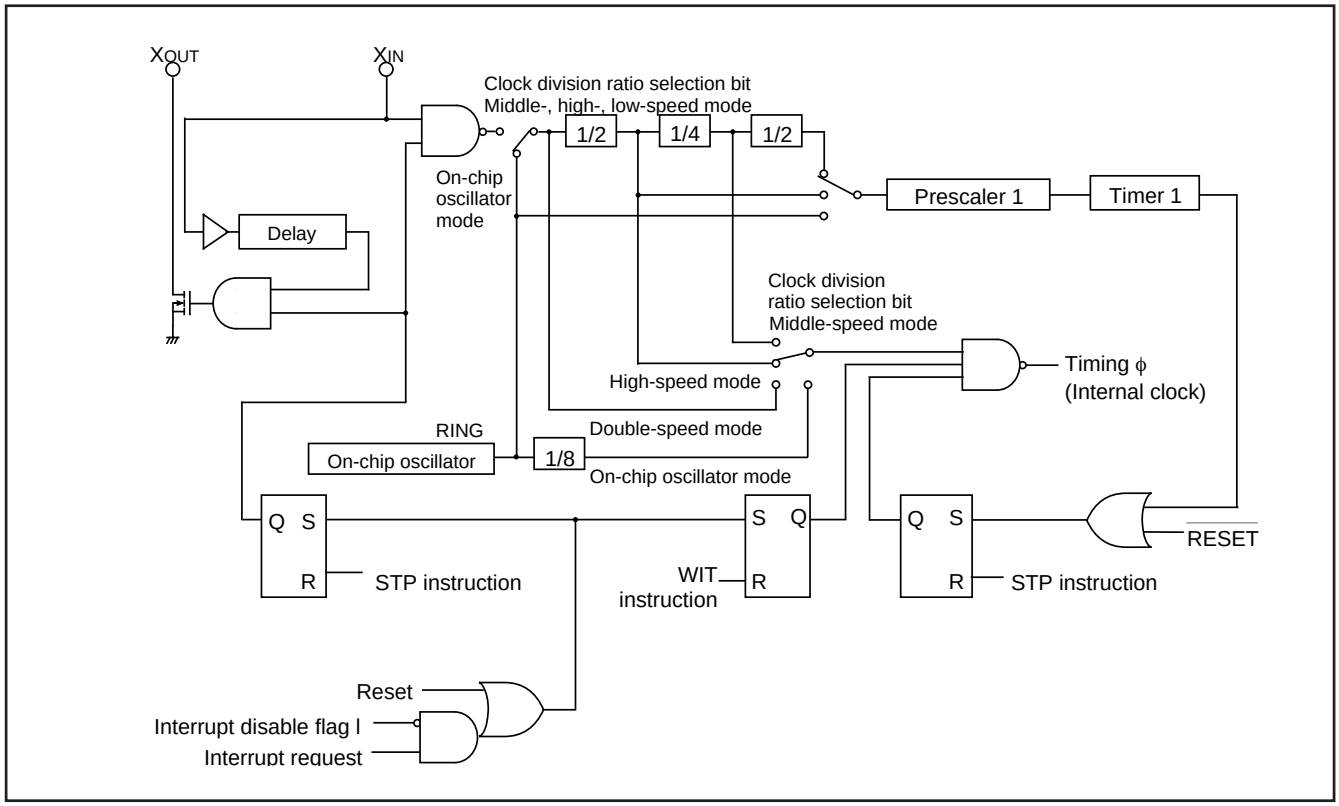


Fig. 48 Block diagram of internal clock generating circuit (for RC oscillation)

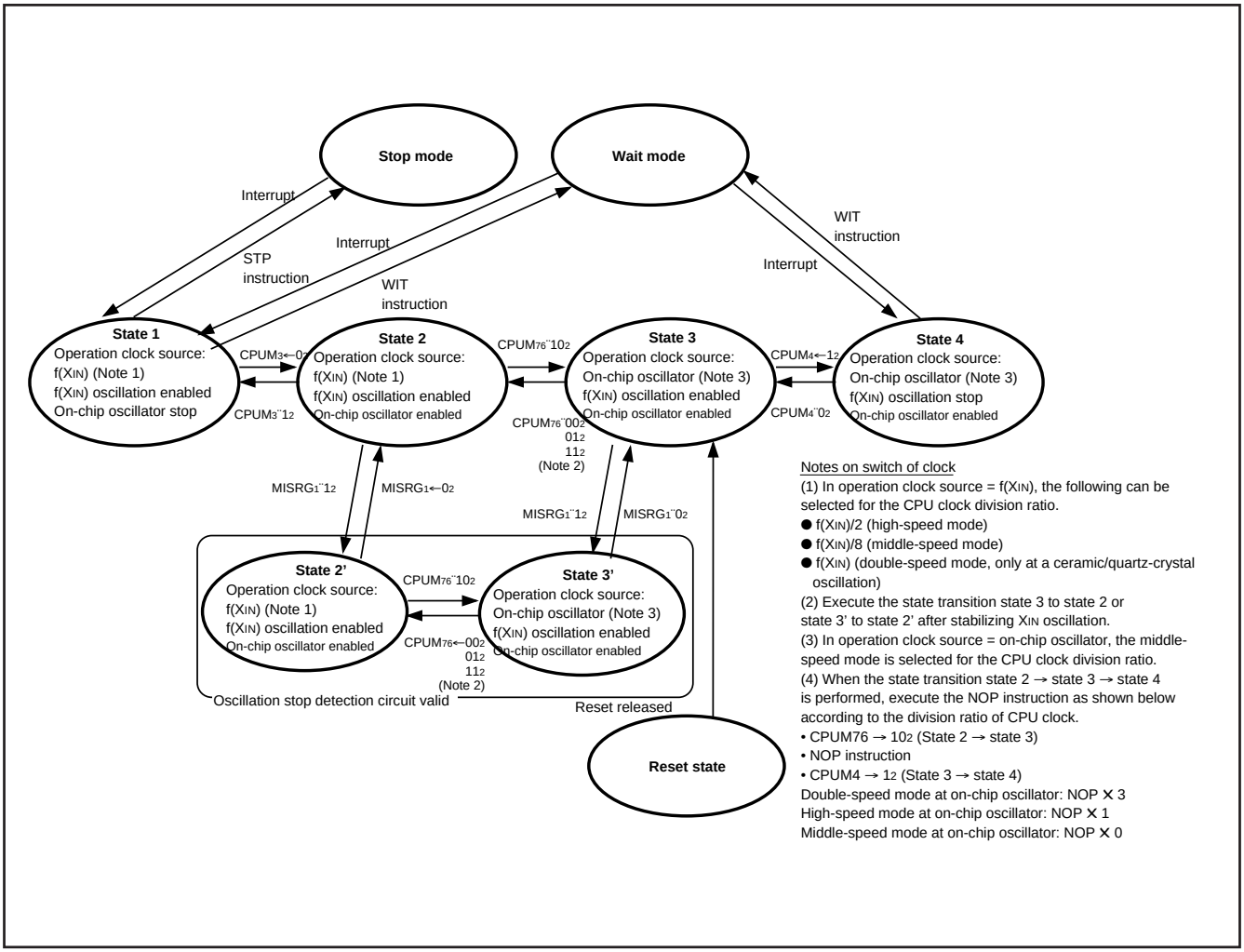


Fig. 49 State transition

QzROM Writing Mode

In the QzROM writing mode, the user ROM area can be rewritten while the microcomputer is mounted on-board by using a serial programmer which is applicable for this microcomputer.
Table 9 lists the pin description (QzROM writing mode) and Fig. 50 and Fig. 51 show the pin connections.
Refer to Fig. 52 and Fig. 53 for example of a connection with a serial programmer.
Contact the manufacturer of your serial programmer for serial programmer . Refer to the user's manual of your serial programmer for details on how to use it.

Table 9 Pin description (QzROM writing mode)

Pin	Name	I/O	Function
V_{CC}, V_{SS}	Power source	Input	•Apply 1.8 to 5.5V to V_{CC}, and 0V to V_{SS}.
$\overline{RESET}$	Reset input	Input	•Reset input pin for active “L”. Reset occurs when $\overline{RESET}$ pin is hold at an “L” level for 16 cycles or more of X_{IN}.
X_{IN}	Clock input	Input	•Set the same termination as the single-chip mode.
X_{OUT}	Clock output	Output	
V_{REF}	Analog reference voltage	Input	•Input the reference voltage of A/D converter to V_{REF}.
$P0_0$–$P0_7$ $P1_3$–$P1_4$ $P2_0$–$P2_5$ $P3_0$–$P3_4$, $P3_7$	I/O port	I/O	•Input “H” or “L” level signal or leave the pin open.
CNV_{SS}	V_{PP} input	Input	•QzROM programmable power source pin.
$P1_1$	ESDA input/output	I/O	•Serial data I/O pin.
$P1_2$	ESCLK input	Input	•Serial clock input pin.
$P1_0$	ESPGMB input	Input	•Read/program pulse input pin.

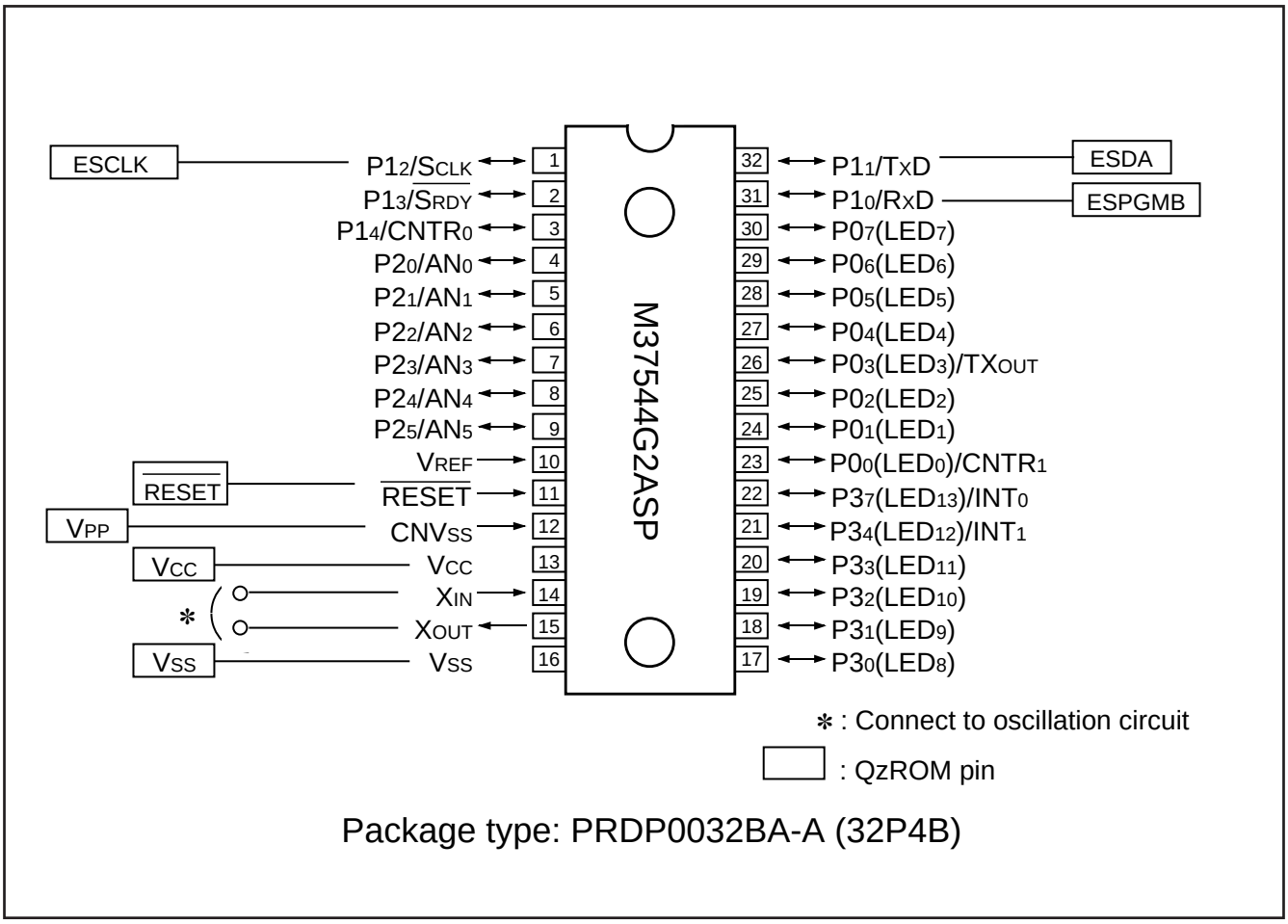
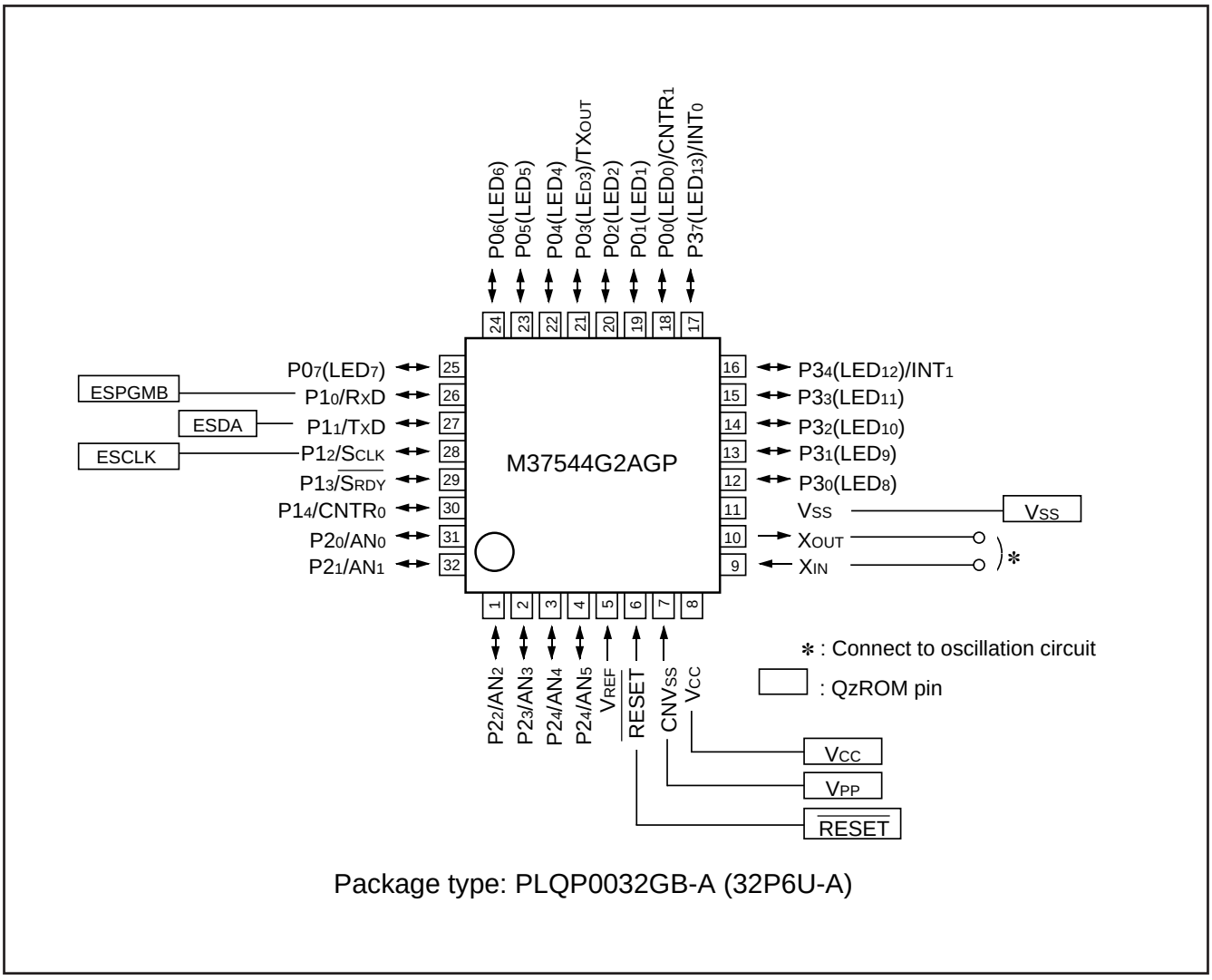
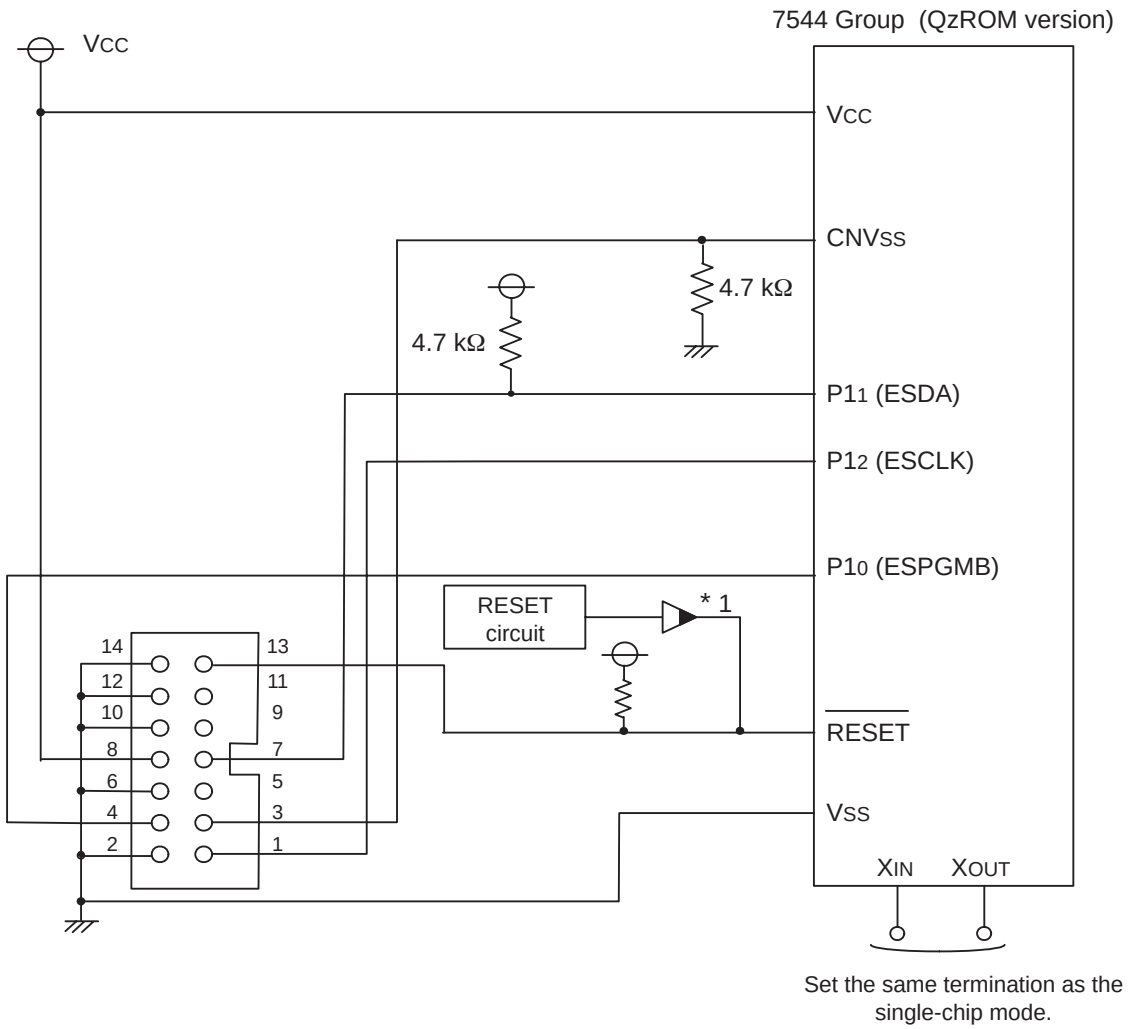


Fig. 50 Pin connection diagram (M37544G2ASP)



Package type: PLQP0032GB-A (32P6U-A)

Fig. 51 Pin connection diagram (M37544G2AGP)



* 1: Open-collector buffer

Note: For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig. 52 When using E8 programmer, connection example

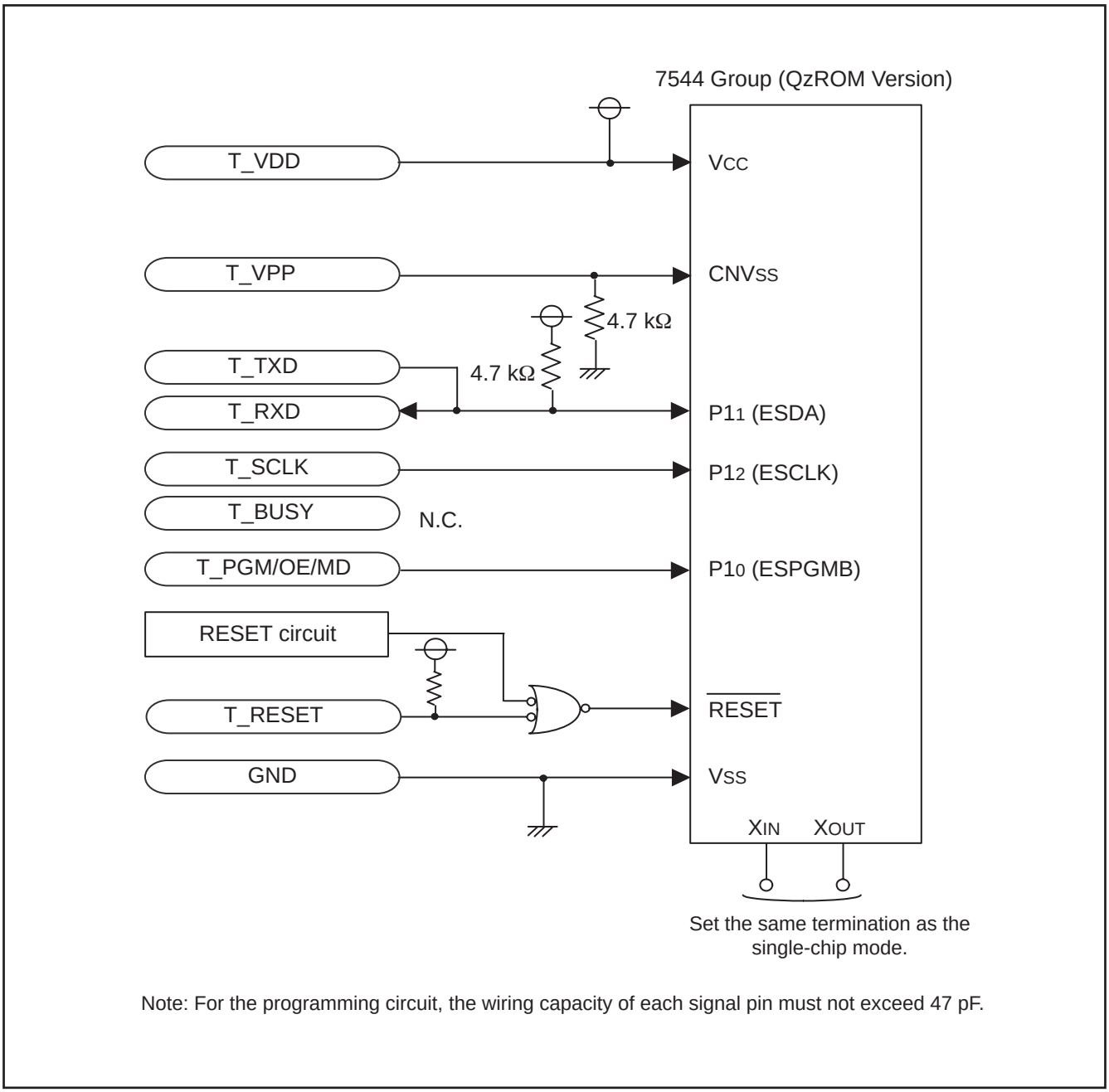


Fig. 53 When using E8 programmer, connection example

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is “1”. After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations. Initialize these flags at beginning of the program.

Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

Decimal Calculations

• For calculations in decimal notation, set the decimal mode flag D to “1”, then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.

• In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

Ports

• The values of the port direction registers cannot be read.

That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is “1”, addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.

It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.

For setting direction registers, use the LDM instruction, STA instruction, etc.

A/D Conversion

Do not execute the STP instruction during A/D conversion.

Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the machine-language instruction table.

The frequency of the internal clock ϕ is the same as that of the X_{IN} in double-speed mode, twice the X_{IN} cycle in high-speed mode and 8 times the X_{IN} cycle in middle-speed mode.

CPU Mode Register

The oscillation mode selection bit and processor mode bits can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit. (Emulator MCU is excluded.)

When a ceramic / quartz-crystal oscillation is selected, a double-speed mode of the clock division ratio selection bits can be used. Do not use it when an RC oscillation is selected.

State transition

Do not stop the clock selected as the operation clock because of setting of CM3, 4.

NOTES ON HARDWARE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μF to 0.1 μF is recommended.

Handling of CNVss Pin

The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (V_{PP} pin) as well.

To improve the noise reduction, connect a track between CNVss pin and Vss pin with 1 to 10 kΩ resistance.

NOTES ON USE

Countermeasures against noise

1. Shortest wiring length

(1) Package

Select the smallest possible package to make the total wiring length short.

<Reason>

The wiring length depends on a microcomputer package. Use of a small package, for example QFP and not DIP, makes the total wiring length short to reduce influence of noise.

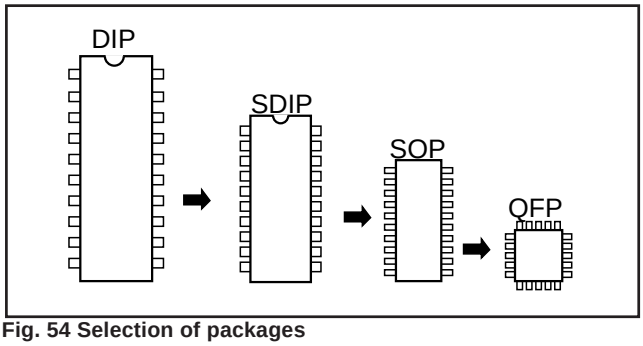


Fig. 54 Selection of packages

(2) Wiring for $\overline{\text{RESET}}$ pin

Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the Vss pin with the shortest possible wiring (within 20 mm).

<Reason>

The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

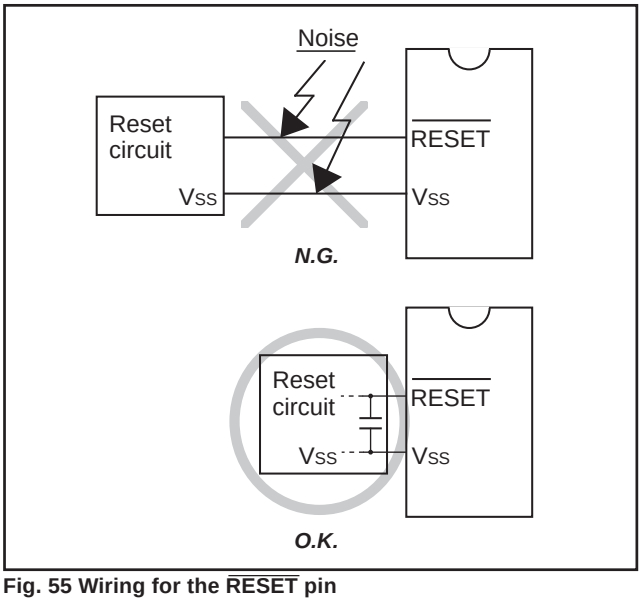


Fig. 55 Wiring for the $\overline{\text{RESET}}$ pin

(3) Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

<Reason>

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

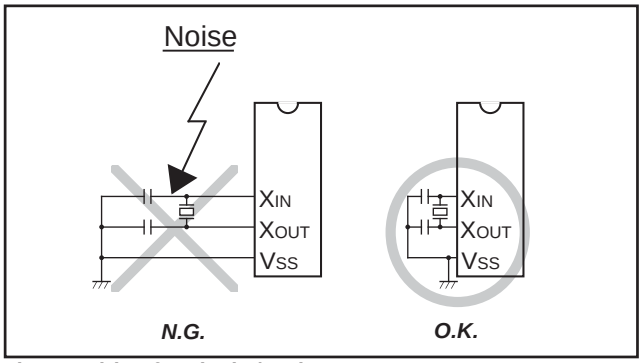


Fig. 56 Wiring for clock I/O pins

(4) Wiring to CNVss pin

Connect CNVss pin to a GND pattern at the shortest distance. The GND pattern is required to be as close as possible to the GND supplied to Vss.

In order to improve the noise reduction, to connect a 5 kΩ resistor serially to the CNVss pin - GND line may be valid.

As well as the above-mentioned, in this case, connect to a GND pattern at the shortest distance. The GND pattern is required to be as close as possible to the GND supplied to Vss.

<Reason>

The CNVss pin of the QzROM is the power source input pin for the built-in QzROM. When programming in the built-in QzROM, the impedance of the CNVss pin is low to allow the electric current for writing flow into the QzROM. Because of this, noise can enter easily. If noise enters the CNVss pin, abnormal instruction codes or data are read from the built-in QzROM, which may cause a program runaway.

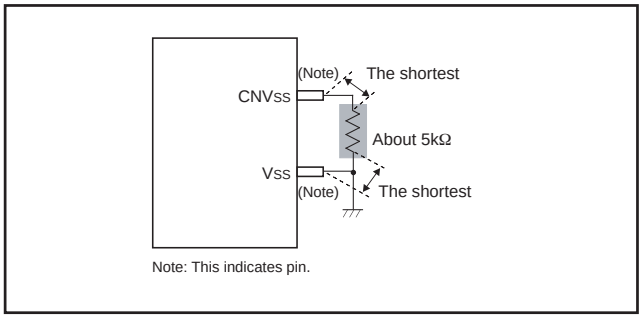


Fig. 57 Wiring for the CNVss pin of the QzROM

2. Connection of bypass capacitor across Vss line and Vcc line

Connect an approximately 0.1 μF bypass capacitor across the Vss line and the Vcc line as follows:

- Connect a bypass capacitor across the Vss pin and the Vcc pin at equal length.
- Connect a bypass capacitor across the Vss pin and the Vcc pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for Vss line and Vcc line.
- Connect the power source wiring via a bypass capacitor to the Vss pin and the Vcc pin.

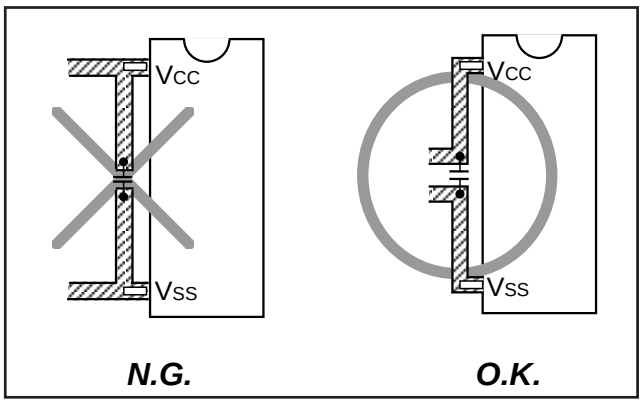


Fig. 58 Bypass capacitor across the Vss line and the Vcc line

3. Wiring to analog input pins

- Connect an approximately 100 Ω to 1 kΩ resistor to an analog signal line which is connected to an analog input pin in series. Besides, connect the resistor to the microcomputer as close as possible.
- Connect an approximately 1000 pF capacitor across the Vss pin and the analog input pin. Besides, connect the capacitor to the Vss pin as close as possible. Also, connect the capacitor across the analog input pin and the Vss pin at equal length.

<Reason>

Signals which is input in an analog input pin (such as an A/D converter/comparator input pin) are usually output signals from sensor. The sensor which detects a change of event is installed far from the printed circuit board with a microcomputer, the wiring to an analog input pin is longer necessarily. This long wiring functions as an antenna which feeds noise into the microcomputer, which causes noise to an analog input pin.

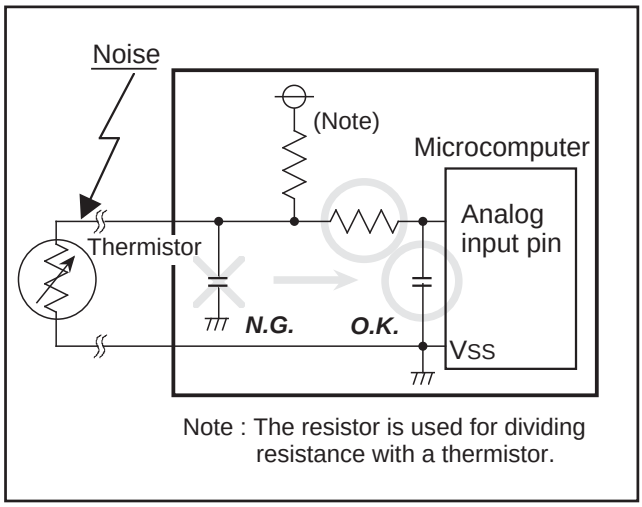


Fig. 59 Analog signal line and a resistor and a capacitor

- The analog input pin is connected to the capacitor of a voltage comparator. Accordingly, sufficient accuracy may not be obtained by the charge/discharge current at the time of A/D conversion when the analog signal source of high-impedance is connected to an analog input pin. In order to obtain the A/D conversion result stabilized more, please lower the impedance of an analog signal source, or add the smoothing capacitor to an analog input pin.

4. Oscillator concerns

So that the product obtains the stabilized operation clock on the user system and its condition, contact the resonator manufacturer and select the resonator and oscillation circuit constants.

Be careful especially when range of voltage and temperature is wide.

Take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

(1) Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

<Reason>

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

(2) Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

<Reason>

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

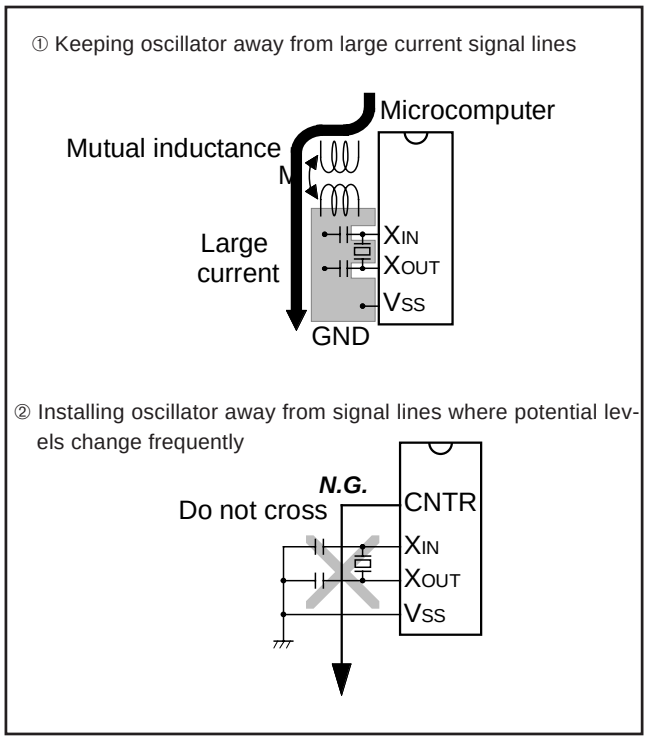


Fig. 60 Wiring for a large current signal line/Writing of signal lines where potential levels change frequently

(3) Oscillator protection using Vss pattern

As for a two-sided printed circuit board, print a Vss pattern on the underside (soldering side) of the position (on the component side) where an oscillator is mounted.

Connect the Vss pattern to the microcomputer Vss pin with the shortest possible wiring. Besides, separate this Vss pattern from other Vss patterns.

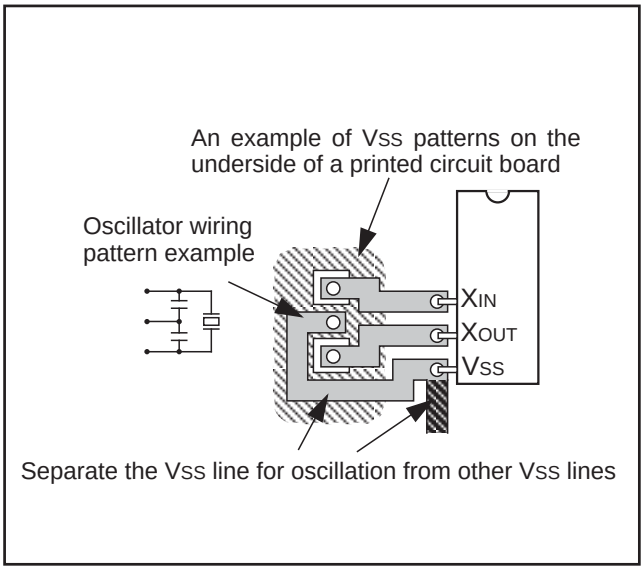


Fig. 61 Vss pattern on the underside of an oscillator

5. Setup for I/O ports
Setup I/O ports using hardware and software as follows:

<Hardware>
• Connect a resistor of 100 Ω or more to an I/O port in series.

<Software>
• As for an input port, read data several times by a program for checking whether input levels are equal or not.
• As for an output port, since the output data may reverse because of noise, rewrite data to its port latch at fixed periods.
• Rewrite data to direction registers and pull-up control registers at fixed periods.

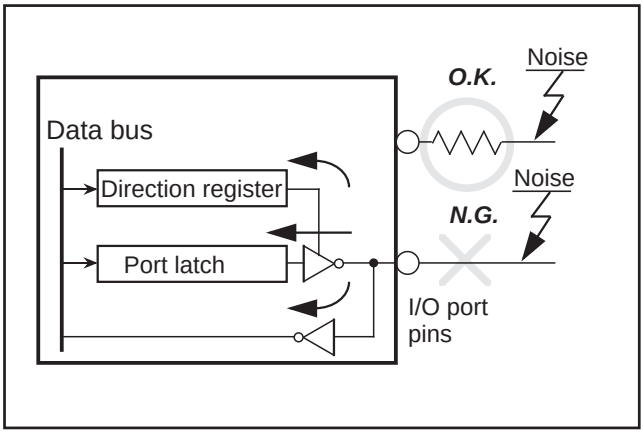


Fig. 62 Setup for I/O ports

6. Providing of watchdog timer function by software
If a microcomputer runs away because of noise or others, it can be detected by a software watchdog timer and the microcomputer can be reset to normal operation. This is equal to or more effective than program runaway detection by a hardware watchdog timer. The following shows an example of a watchdog timer provided by software.
In the following example, to reset a microcomputer to normal operation, the main routine detects errors of the interrupt processing routine and the interrupt processing routine detects errors of the main routine.
This example assumes that interrupt processing is repeated multiple times in a single main routine processing.

<The main routine>
• Assigns a single byte of RAM to a software watchdog timer (SWDT) and writes the initial value N in the SWDT once at each execution of the main routine. The initial value N should satisfy the following condition:
N+1 ≥ (Counts of interrupt processing executed in each main routine)
As the main routine execution cycle may change because of an interrupt processing or others, the initial value N should have a margin.
• Watches the operation of the interrupt processing routine by comparing the SWDT contents with counts of interrupt processing after the initial value N has been set.
• Detects that the interrupt processing routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
If the SWDT contents do not change after interrupt processing.

<The interrupt processing routine>
• Decrements the SWDT contents by 1 at each interrupt processing.
• Determines that the main routine operates normally when the SWDT contents are reset to the initial value N at almost fixed cycles (at the fixed interrupt processing count).
• Detects that the main routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
If the SWDT contents are not initialized to the initial value N but continued to decrement and if they reach 0 or less.

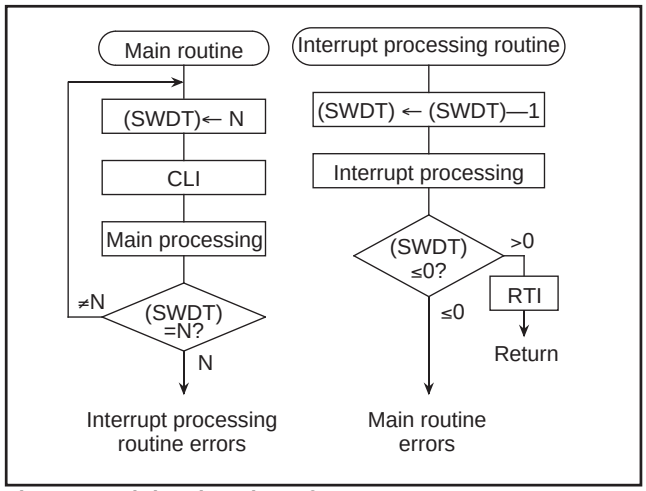


Fig. 63 Watchdog timer by software

NOTES ON QzROM

Product shipped in blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur.
Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

Precautions Regarding Overvoltage

Make sure that voltage exceeding the V_{CC} pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in Figure below does not occur for CNV_{SS} pin (V_{PP} power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.

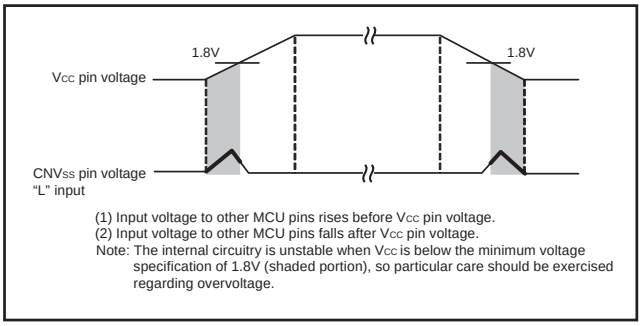


Fig. 64 Timing Diagram (bold-lined periods are applicable)

Notes On QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .msk) which is made by the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "00_{16}" and "FF_{16}" can not be accepted.
- Set "FF_{16}" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF_{16}" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

Data Required For QzROM Writing Orders

The following are necessary when ordering a QzROM product shipped after writing:

1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).
Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

ELECTRICAL CHARACTERISTICS (QzROM version)

1.7544Group (QzROM version)

Applied to: M37544G2A-XXXSP/GP, M37544G2ASP/GP

Absolute Maximum Ratings

Table 10 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. When an input voltage is measured, output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$,$P3_7$, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$,$P3_7$, X_{OUT}		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	Ta = 25°C	200	mW
T_{opr}	Operating temperature	–	–20 to 85	°C
T_{stg}	Storage temperature	–	–40 to 125	°C

Recommended Operating Conditions

Table 11 Recommended operating conditions (1) (Vcc = 1.8 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (ceramic)	f(X_{IN}) = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 2 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
		f(X_{IN}) = 8 MHz (Double-speed mode)	4.5	5.0	5.5	V
		f(X_{IN}) = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 1 MHz (Double-speed mode)	2.2	5.0	5.5	V
	Power source voltage (RC)	f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 1 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
	Power source voltage (On-chip oscillator)		1.8	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage		2.0		V_{CC}	V
V_{IH}	“H” input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$		0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage (TTL input level selected) $P1_0$, $P1_2$, $P3_4$, $P3_7$		2.0		V_{CC}	V
V_{IH}	“H” input voltage $\overline{RESET}$, X_{IN}		0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$		0		0.3V_{CC}	V
V_{IL}	“L” input voltage (TTL input level selected) $P1_0$, $P1_2$, $P3_4$, $P3_7$		0		0.8	V
V_{IL}	“L” input voltage $\overline{RESET}$, CNV_{SS}		0		0.2V_{CC}	V
V_{IL}	“L” input voltage X_{IN}		0		0.16V_{CC}	V
$\sum I_{OH(peak)}$	“H” total peak output current (**Note**) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$				–80	mA
$\sum I_{OL(peak)}$	“L” total peak output current (**Note**) $P1_0$–$P1_4$, $P2_0$–$P2_5$				80	mA
$\sum I_{OL(peak)}$	“L” total peak output current (**Note**) $P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$				60	mA
$\sum I_{OH(avg)}$	“H” total average output current (**Note**) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$				–40	mA
$\sum I_{OL(avg)}$	“L” total average output current (**Note**) $P1_0$–$P1_4$, $P2_0$–$P2_5$				40	mA
$\sum I_{OL(avg)}$	“L” total average output current (**Note**) $P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$				30	mA

Note : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Recommended Operating Conditions (continued)

Table 12 Recommended operating conditions (2) (V_{CC} = 1.8 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current (**Note 1**) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$				–10	mA
$I_{OL(peak)}$	"L" peak output current (**Note 1**) $P1_0$–$P1_4$, $P2_0$–$P2_5$				10	mA
$I_{OL(peak)}$	"L" peak output current (**Note 1**) $P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$				30	mA
$I_{OH(avg)}$	"H" average output current (**Note 2**) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$				–5	mA
$I_{OL(avg)}$	"L" average output current (**Note 2**) $P1_0$–$P1_4$, $P2_0$–$P2_5$				5	mA
$I_{OL(avg)}$	"L" average output current (**Note 2**) $P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$				15	mA
$f(X_{IN})$	Internal clock oscillation frequency (**Note 3**) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Internal clock oscillation frequency (**Note 3**) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (**Note 3**) at RC oscillation	V_{CC} = 2.2 to 5.5 V High-, Middle-speed mode			2	MHz
	Internal clock oscillation frequency (**Note 3**) at ceramic oscillation or external clock input	V_{CC} = 4.5 to 5.5 V Double-speed mode			8	MHz
	Internal clock oscillation frequency (**Note 3**) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V Double-speed mode			4	MHz
	Internal clock oscillation frequency (**Note 3**) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V Double-speed mode			2	MHz
	Internal clock oscillation frequency (**Note 3**) at ceramic oscillation or external clock input	V_{CC} = 2.2 to 5.5 V Double-speed mode			1	MHz
	Internal clock oscillation frequency (**Note 3**) at RC oscillation	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (**Note 3**) at RC oscillation	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			2	MHz
	Internal clock oscillation frequency (**Note 3**) at RC oscillation	V_{CC} = 2.2 to 5.5 V High-, Middle-speed mode			1	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50 %.

Electrical Characteristics

Table 13 Electrical characteristics (1) (V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$ (**Note 1**)	I_{OH} = –5 mA V_{CC} = 4.0 to 5.5 V	V_{CC}–1.5			V
		I_{OH} = –1.0 mA V_{CC} = 1.8 to 5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P1_0$–$P1_4$, $P2_0$–$P2_5$	I_{OL} = 5 mA V_{CC} = 4.0 to 5.5 V			1.5	V
		I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
		I_{OL} = 1.0 mA V_{CC} = 1.8 to 5.5 V			1.0	V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$	I_{OL} = 15 mA V_{CC} = 4.0 to 5.5 V			2.0	V
		I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
		I_{OL} = 10 mA V_{CC} = 1.8 to 5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis $CNTR_0$, $CNTR_1$, INT_0, INT_1 (**Note 2**) $P0_0$–$P0_7$ (**Note 3**)			0.4		V
V_{T+}–V_{T-}	Hysteresis RxD, SCLK (**Note 2**)			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.9		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$	V_I = V_{CC} (Pin floating. Pull up transistors "off")			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$	V_I = V_{SS} (Pin floating. Pull up transistors "off")			–5.0	µA
I_{IL}	"L" input current $\overline{RESET}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$	V_I = V_{SS} (Pull up transistors "on")		–0.2	–0.5	mA
V_{RAM}	RAM hold voltage	When clock stopped	1.6		5.5	V
ROSC	On-chip oscillator oscillation frequency	V_{CC} = 5.0 V, Ta = 25 °C	1000	2000	3000	kHz
DOSC	Oscillation stop detection circuit detection frequency	V_{CC} = 5.0 V, Ta = 25 °C	62.5	125	187.5	kHz

Notes 1: $P1_1$ is measured when the $P1_1$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: RxD, SCLK, INT_0, and INT_1 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake up.

Electrical Characteristics (continued)

Table 14 Electrical characteristics (2) (V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	High-speed mode, f(X_{IN}) = 8 MHz Output transistors “off”			3.3	8.0	mA
		High-speed mode, V_{CC} = 2.2 V, f(X_{IN}) = 2 MHz Output transistors “off”			0.3	1.5	mA
		Double-speed mode, f(X_{IN}) = 8 MHz Output transistors “off”			4.8	10.0	mA
		Middle-speed mode, f(X_{IN}) = 8 MHz Output transistors “off”			1.8	5.0	mA
		On-chip oscillator operation mode, V_{CC} = 5.0 V Output transistors “off”			250	900	µA
		f(X_{IN}) = 8 MHz (in WIT state), functions except timer 1 disabled, Output transistors “off”			1.3	3.2	mA
		f(X_{IN}) = 2 MHz, V_{CC} = 2.2 V (in WIT state), functions except timer 1 disabled, Output transistors “off”			0.2		mA
		On-chip oscillator operation mode (in WIT state), V_{CC} = 5.0 V functions except timer 1 disabled, Output transistors “off”			120	450	µA
		Increment when A/D conversion is executed f(X_{IN}) = 8 MHz, V_{CC} = 5.0 V			0.45		mA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10.0	µA

A/D Converter Characteristics

Table 15 A/D Converter characteristics (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
ABS	Absolute accuracy (quantification error excluded)	Ta = –20 to 85 °C, Vcc = VREF			±3	LSB
tCONV	Conversion time				109	tc(XIN)
RLADDER	Ladder resistor			37		kΩ
IVREF	Reference power source input current	VREF = 5.0 V	50	135	200	μA
		VREF = 3.0 V	30	80	120	
II(AD)	A/D port input current				5.0	μA

Note: As for AD translation accuracy, on the following operating conditions, accuracy may become low.

(1) Since the analog circuit inside a microcomputer becomes sensitive to noise when VREF voltage is set up lower than Vcc voltage, accuracy may become low rather than the case where VREF voltage and Vcc voltage are set up to the same value..

(2) When VREF voltage is less than [3.0V], the accuracy at the time of low temperature may become extremely low compared with the time of room temperature. The use beyond VREF=3.0V is recommended in the system the use by the side of low temperature is assumed to be.

Timing Requirements

Table 16 Timing requirements (Vcc = 1.8 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tW($\overline{\text{RESET}}$)	Reset input “L” pulse width	2			μs
tC(XIN)	External clock input cycle time	125			ns
tWH(XIN)	External clock input “H” pulse width	50			ns
tWL(XIN)	External clock input “L” pulse width	50			ns
tC(CNTR0)	CNTR0 input cycle time	200			ns
tWH(CNTR0)	CNTR0, INT0, INT1, input “H” pulse width	80			ns
tWL(CNTR0)	CNTR0, INT0, INT1, input “L” pulse width	80			ns
tC(CNTR1)	CNTR1 input cycle time	2000			ns
tWH(CNTR1)	CNTR1 input “H” pulse width	800			ns
tWL(CNTR1)	CNTR1 input “L” pulse width	800			ns
tC(SCLK)	Serial I/O clock input cycle time (Note)	800			ns
tWH(SCLK)	Serial I/O clock input “H” pulse width (Note)	370			ns
tWL(SCLK)	Serial I/O clock input “L” pulse width (Note)	370			ns
tsu(RxD–SCLK)	Serial I/O input set up time	220			ns
th(SCLK–RxD)	Serial I/O input hold time	100			ns

Note: In this time, bit 6 of the serial I/O control register (address 001A16) is set to “1” (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.

Switching Characteristics

Table 17 Switching characteristics (V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O clock output “H” pulse width	$t_{C(SCLK)}$/2–30			ns
$t_{WL(SCLK)}$	Serial I/O clock output “L” pulse width	$t_{C(SCLK)}$/2–30			ns
$t_{d(SCLK–TxD)}$	Serial I/O output delay time			140	ns
$t_{v(SCLK–TxD)}$	Serial I/O output valid time	–30			ns
$t_{r(SCLK)}$	Serial I/O clock output rising time			30	ns
$t_{f(SCLK)}$	Serial I/O clock output falling time			30	ns
$t_{r(CMOS)}$	CMOS output rising time (**Note**)		10	30	ns
$t_{f(CMOS)}$	CMOS output falling time (**Note**)		10	30	ns

Note : Pin X_{OUT} is excluded.

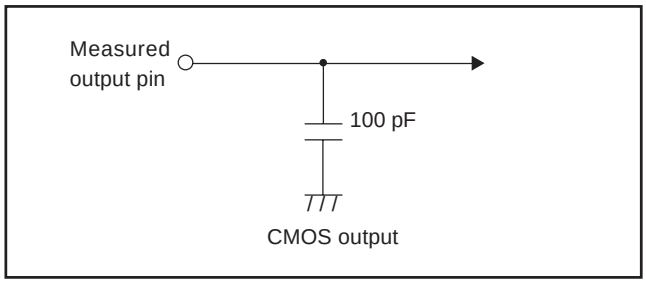


Fig. 65 Switching characteristics measurement circuit diagram

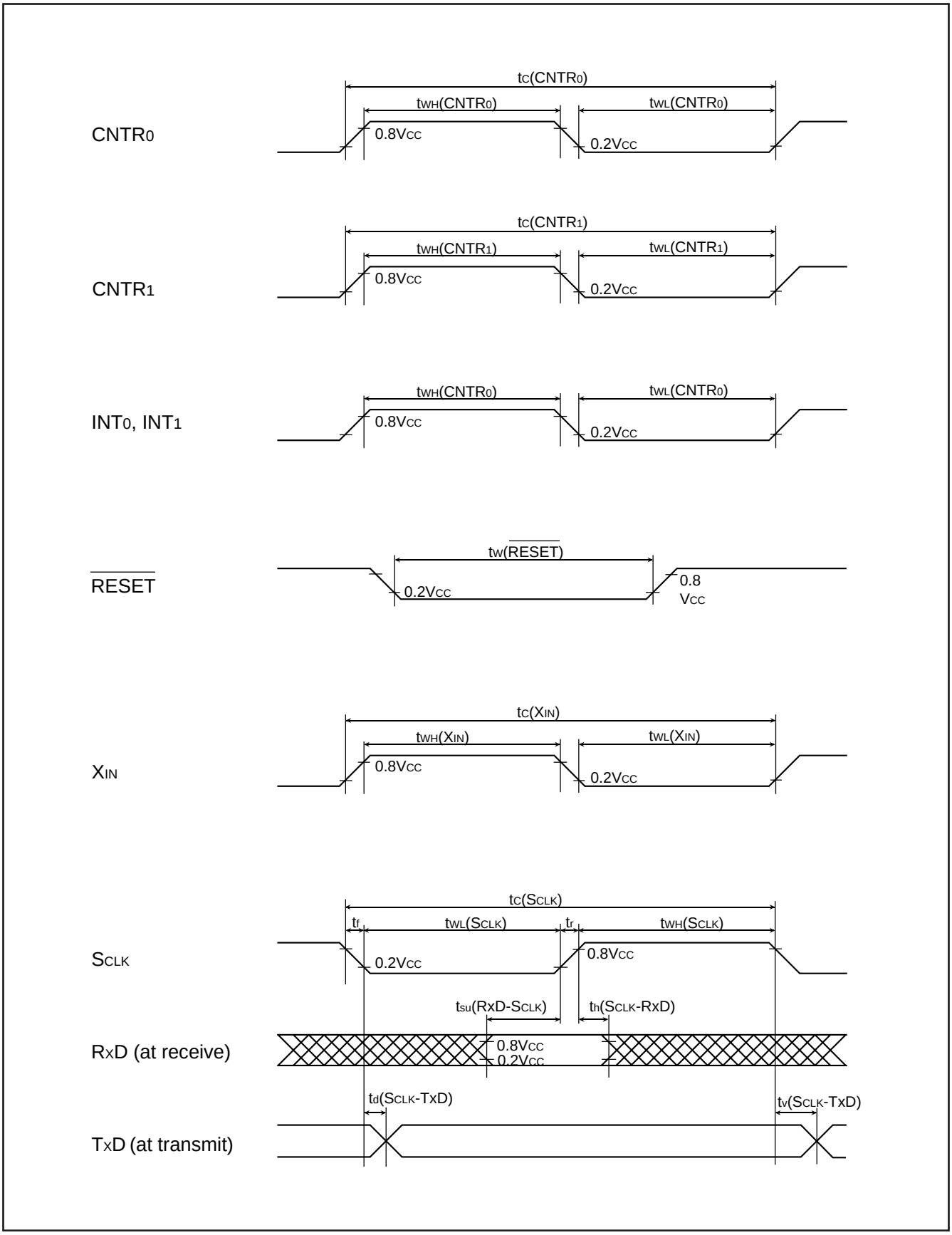
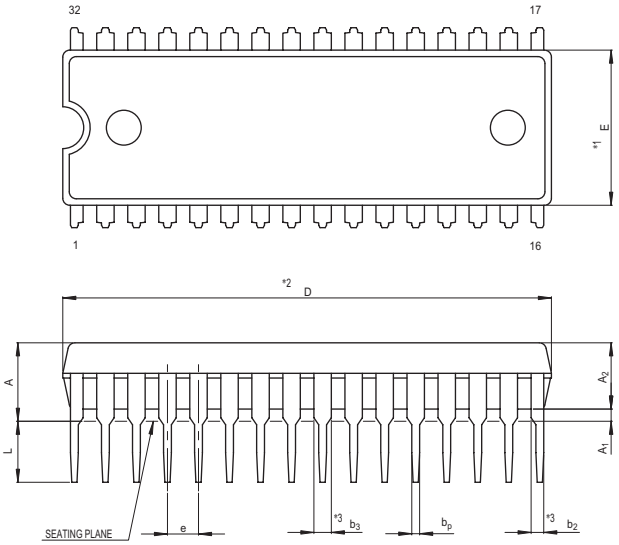


Fig. 66 Timing chart

PACKAGE OUTLINE

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

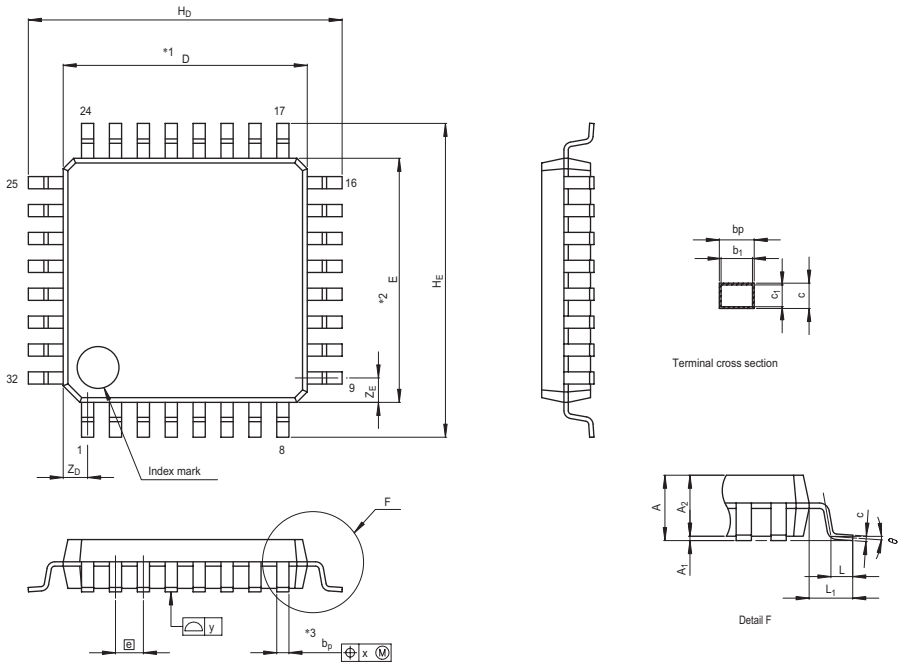
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SDIP32-8.9x28-1.78	PRDP0032BA-A	32P4B	2.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e1	9.86	10.16	10.46
D	27.8	28.0	28.2
E	8.75	8.9	9.05
A	——	——	5.08
A_1	0.51	——	——
A_2	——	3.8	——
b_p	0.35	0.45	0.55
b_2	0.63	0.73	1.03
b_3	0.9	1.0	1.3
c	0.22	0.27	0.34
θ	0°	——	15°
e	1.528	1.778	2.028
L	3.0	——	——

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	——	1.4	——
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	——	——	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	——	0.35	——
c	0.09	0.145	0.20
c_1	——	0.125	——
θ	0°	——	8°
e	——	0.8	——
x	——	——	0.20
y	——	——	0.10
Z_D	——	0.7	——
Z_E	——	0.7	——
L	0.3	0.5	0.7
L_1	——	1.0	——

APPENDIX

NOTES ON PROGRAMMING

1. Processor Status Register

(1) Initializing of processor status register

Flags which affect program execution must be initialized after a reset.

In particular, it is essential to initialize the T and D flags because they have an important effect on calculations. Initialize these flags at beginning of the program.

<Reason>

After a reset, the contents of the processor status register (PS) are undefined except for the I flag which is “1”.

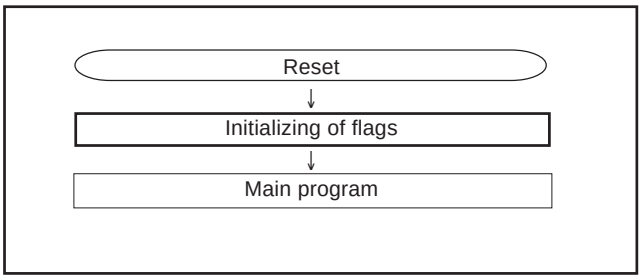


Fig. 1 Initialization of processor status register

(2) How to reference the processor status register

To reference the contents of the processor status register (PS), execute the **PHP** instruction once then read the contents of (S+1). If necessary, execute the **PLP** instruction to return the PS to its original status.

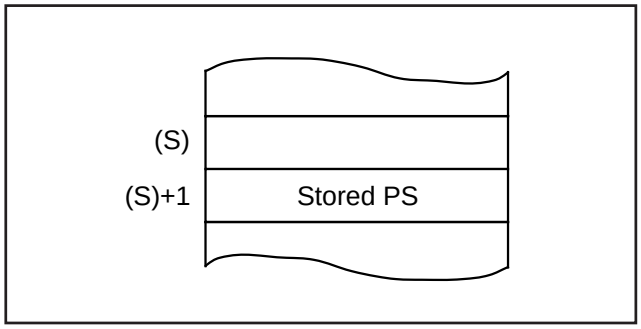


Fig. 2 Stack memory contents after PHP instruction execution

2. Decimal calculations

(1) Execution of decimal calculations

The **ADC** and **SBC** are the only instructions which will yield proper decimal notation, set the decimal mode flag (D) to “1” with the **SED** instruction. After executing the **ADC** or **SBC** instruction, execute another instruction before executing the **SEC**, **CLC**, or **CLD** instruction.

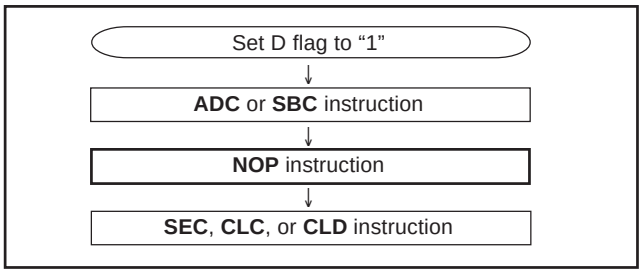


Fig. 3 Instructions for decimal calculations

(2) Notes on status flag in decimal mode

When decimal mode is selected, the values of three of the flags in the status register (the N, V, and Z flags) are invalid after a **ADC** or **SBC** instruction is executed.

The carry flag (C) is set to “1” if a carry is generated as a result of the calculation, or is cleared to “0” if a borrow is generated. To determine whether a calculation has generated a carry, the C flag must be initialized to “0” before each calculation. To check for a borrow, the C flag must be initialized to “1” before each calculation.

3. JMP instruction

When using the **JMP** instruction in indirect addressing mode, do not specify the last address on a page as an indirect address.

4. BRK instruction

(1) Interrupt priority level

When the BRK instruction is executed with the following conditions satisfied, the interrupt execution is started from the address of interrupt vector which has the highest priority.

- Interrupt request bit and interrupt enable bit are set to “1”.
- Interrupt disable flag (I) is set to “1” to disable interrupt.

5. Multiplication and Division Instructions

(1) The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.

(2) The execution of these instructions does not change the contents of the processor status register.

6. Read-modify-write instruction
Do not execute a read-modify-write instruction to the read invalid address (SFR).
The read-modify-write instruction operates in the following sequence: read one-byte of data from memory, modify the data, write the data back to original memory. The following instructions are classified as the read-modify-write instructions in the 740 Family.
(1) Bit management instructions: CLB, SEB
(2) Shift and rotate instructions: ASL, LSR, ROL, ROR, RRF
(3) Add and subtract instructions: DEC, INC
(4) Logical operation instructions (1's complement): COM

Add and subtract/logical operation instructions (ADC, SBC, AND, EOR, and ORA) when T flag = "1" operate in the way as the read-modify-write instruction. Do not execute the read invalid SFR.
<Reason>
When the read-modify-write instruction is executed to read invalid SFR, the instruction may cause the following consequence: the instruction reads unspecified data from the area due to the read invalid condition. Then the instruction modifies this unspecified data and writes the data to the area. The result will be random data written to the area or some unexpected event.

NOTES ON PERIPHERAL FUNCTIONS
Notes on I/O Ports

1. Pull-up control register
When using each port which built in pull-up resistor as an output port, the pull-up control bit of corresponding port becomes invalid, and pull-up resistor is not connected.
<Reason>
Pull-up control is effective only when each direction register is set to the input mode.

2. Notes in stand-by state
In stand-by state*1 for low-power dissipation, do not make input levels of an input port and an I/O port "undefined".
Pull-up (connect the port to Vcc) or pull-down (connect the port to Vss) these ports through a resistor.
When determining a resistance value, note the following points:
• External circuit
• Variation of output levels during the ordinary operation
When using a built-in pull-up resistor, note on varied current values:
• When setting as an input port : Fix its input level
• When setting as an output port : Prevent current from flowing out to external.
<Reason>
The output transistor becomes the OFF state, which causes the ports to be the high-impedance state. Note that the level becomes "undefined" depending on external circuits.
Accordingly, the potential which is input to the input buffer in a microcomputer is unstable in the state that input levels of an input port and an I/O port are "undefined". This may cause power source current.

*1 stand-by state : the stop mode by executing the **STP** instruction

3. Modifying output data with bit handling instruction
When the port latch of an I/O port is modified with the bit handling instruction*1, the value of an unspecified bit may change.
<Reason>
I/O ports can be set to input mode or output mode in byte units. When the port register is read or written, the following will be operated:
• Port as input mode
Read: Read the pin level
Write: Write to the port latch
• Port as output mode
Read: Read the port latch or peripheral function output
(specifications vary depending on the port)
Write: Write to the port latch
(output the content of the port latch from the pin)

Meanwhile, the bit handling instructions are the read-modifywrite instructions*2. Executing the bit handling instruction to the port register allows reading and writing a bit unspecified with the instruction at the same time.
If an unspecified bit is set to input mode, the pin level is read and the value is written to the port latch. At this time, if the original content of the port latch and the pin level do not match, the content of the port latch changes.
If an unspecified bit is set to output mode, the port latch is normally read, but the peripheral function output is read in some ports and the value is written to the port latch. At this time, if the original content of the port latch and the peripheral function output do not match, the content of the port latch changes.

*1 Bit handling instructions: CLB, SEB
*2 Read-modify-write instruction: Reads 1-byte of data from memory, modifies the data, and writes 1-byte of the data to the original memory.

4. Direction register
The values of the port direction registers cannot be read.
That is, it is impossible to use the **LDA** instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as **BBC** and **BBS**.
It is also impossible to use bit operation instructions such as **CLB** and **SEB** and read-modify-write instructions of direction registers for calculations such as **ROR**.
For setting direction registers, use the **LDM** instruction, **STA** instruction, etc.

Termination of Unused Pins

1. Terminate unused pins

Perform the following wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

(1) I/O ports

Set the I/O ports for the input mode and connect each pin to V_{CC} or V_{SS} through each resistor of 1 kΩ to 10 kΩ. The port which can select a built-in pull-up resistor can also use the built-in pull-up resistor.

When using the I/O ports as the output mode, open them at "L" or "H".

- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

2. Termination remarks

(1) I/O ports setting as input mode

[1] Do not open in the input mode.

<Reason>

- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination (1) shown on the above "1. Terminate unused pins".

[2] Do not connect to V_{CC} or V_{SS} directly.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur.

[3] Do not connect multiple ports in a lump to V_{CC} or V_{SS} through a resistor.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

Notes on Interrupts

1. Change of relevant register settings

When not requiring for the interrupt occurrence synchronous with the following case, take the sequence shown in Figure 4.

- When switching external interrupt active edge
- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated

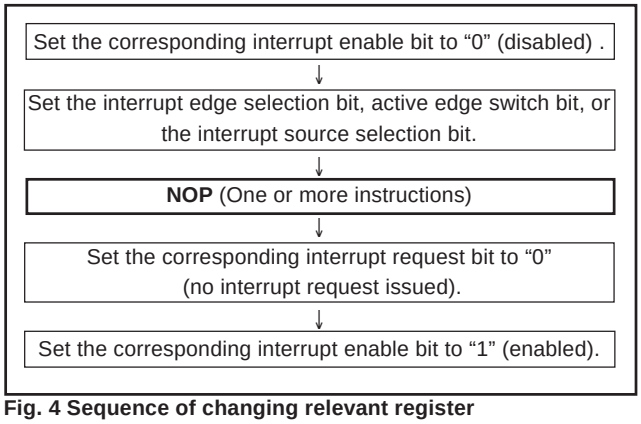


Fig. 4 Sequence of changing relevant register

<Reason>

When setting the followings, the interrupt request bit of the corresponding interrupt may be set to "1".

- When switching external interrupt active edge
  - INT_0 interrupt edge selection bit
    (bit 0 of Interrupt edge selection register (address $003A_{16}$))
  - INT_1 interrupt edge selection bit
    (bit 1 of Interrupt edge selection register)
  - $CNTR_0$ active edge switch bit
    (bit 2 of timer X mode register (address $002B_{16}$))
  - $CNTR_1$ active edge switch bit
    (bit 6 of timer A mode register (address $001D_{16}$))

2. Check of interrupt request bit

When executing the **BBC** or **BBS** instruction to determine an interrupt request bit immediately after this bit is set to "0", take the following sequence.

<Reason>

If the BBC or BBS instruction is executed immediately after an interrupt request bit is cleared to "0", the value of the interrupt request bit before being cleared to "0" is read.

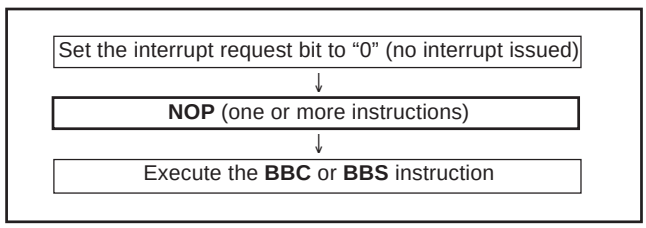


Fig. 5 Sequence of check of interrupt request bit

Notes on Timers

1. When n (0 to 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

2. When a count source of timer X is switched, stop a count of the timer.

Notes on Timer 1

1. Timer 1 count source

The “on-chip oscillator output” of timer 1 count source selection bits (bits 1 and 0 of timer count source set register 2 (address $002F_{16}$)) can be selected while the on-chip oscillator oscillation control bit (bit 3 of CPU mode register (address $003B_{16}$)) is “0” (on-chip oscillator oscillation enabled).

Notes on Timer A

1. $CNTR_1$ interrupt active edge selection

$CNTR_1$ interrupt active edge depends on the $CNTR_1$ active edge switch bit (bit 6 of timer A mode register (address $001D_{16}$)).
When this bit is “0”, the $CNTR_1$ interrupt request bit goes to “1” at the falling edge of the $CNTR_1$ pin input signal. When this bit is “1”, the $CNTR_1$ interrupt request bit goes to “1” at the rising edge of the $CNTR_1$ pin input signal.
However, in the pulse width HL continuously measurement mode, $CNTR_1$ interrupt request is generated at both rising and falling edges of $CNTR_1$ pin input signal regardless of the setting of $CNTR_1$ active edge switch bit.

2. Period measurement mode, event counter mode and pulse width HL continuously measurement mode

Set the direction register of port $P0_0$, which is also used as $CNTR_1$ pin, to input.
Set the key-on wakeup function of $P0_0$, which is also used as $CNTR_1$ pin, to be disabled by setting the $P0_0$ key-on wakeup selection bit (bit 7 of interrupt edge selection register (address $003A_{16}$)) to “1”.

3. Timer A count source

The “on-chip oscillator output” of timer A count source selection bits (bits 3 and 2 of timer count source set register 2 (address $002F_{16}$)) can be selected while the on-chip oscillator oscillation control bit (bit 3 of CPU mode register (address $003B_{16}$)) is “0” (on-chip oscillator oscillation enabled).

Notes on Timer X

1. $CNTR_0$ interrupt active edge selection

$CNTR_0$ interrupt active edge depends on the $CNTR_0$ active edge switch bit (bit 2 of timer X mode register (address $002B_{16}$)).
When this bit is “0”, the $CNTR_0$ interrupt request bit goes to “1” at the falling edge of $CNTR_0$ pin input signal. When this bit is “1”, the $CNTR_0$ interrupt request bit goes to “1” at the rising edge of $CNTR_0$ pin input signal.

2. Timer X count source selection

The f(X_{IN}) (frequency not divided) can be selected by the timer X count source selection bits (bits 1 and 0 of timer count source set register 1 (address $002E_{16}$)) only when the ceramic oscillation or the on-chip oscillator is selected.
Do not select it for the timer X count source at the RC oscillation.

3. Pulse output mode

Set the direction register of port $P1_4$, which is also used as $CNTR_0$ pin, to output.
When the TX_{OUT} pin is used, set the direction register of port $P0_3$, which is also used as TX_{OUT} pin, to output.

4. Pulse width measurement mode

Set the direction register of port $P1_4$, which is also used as $CNTR_0$ pin, to input.

Notes on Serial Interface

1. Clock synchronous serial I/O

(1) When the transmit operation is stopped, clear the serial I/O enable bit (bit 7) and the transmit enable bit (bit 4 of serial I/O control register (address 001A16)) to “0” (serial I/O and transmit disabled).

<Reason>

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O enable bit is cleared to “0” (serial I/O disabled), the internal transmission is running (in this case, since pins TxD, RxD, SCLK, and $\overline{\text{SRDY}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O enable bit is set to “1” at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

(2) When the receive operation is stopped, clear the receive enable bit (bit 5) to “0” (receive disabled), or clear the serial I/O enable bit (bit 7 of serial I/O control register (address 001A16)) to “0” (serial I/O disabled).

(3) When the transmit/receive operation is stopped, clear both the transmit enable bit and receive enable bit to “0” (transmit and receive disabled) simultaneously. (any one of data transmission and reception cannot be stopped.)

<Reason>

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception.

If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized. In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to “0” (transmit disabled). Also, the transmission circuit cannot be initialized even if the serial I/O enable bit is cleared to “0” (serial I/O disabled) (same as (1)).

(4) When signals are output from the $\overline{\text{SRDY}}$ pin on the reception side by using an external clock, set all of the receive enable bit (bit 5), the $\overline{\text{SRDY}}$ output enable bit (bit 2 of serial I/O control register (address 001A16)), and the transmit enable bit to “1”.

(5) When the $\overline{\text{SRDY}}$ signal input is used, set the using pin to the input mode before data is written to the transmit/receive buffer register.

2. UART

When the transmit operation is stopped, clear the transmit enable bit to “0” (transmit disabled).

<Reason>

Same as (1) shown on the above “1. Clock synchronous serial I/O“.

When the receive operation is stopped, clear the receive enable bit to “0” (receive disabled).

When the transmit/receive operation is stopped, clear the transmit enable bit to “0” (transmit disabled) and receive enable bit to “0” (receive disabled).

3. Notes common to clock synchronous serial I/O and UART

(1) Set the serial I/O control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to “0.”

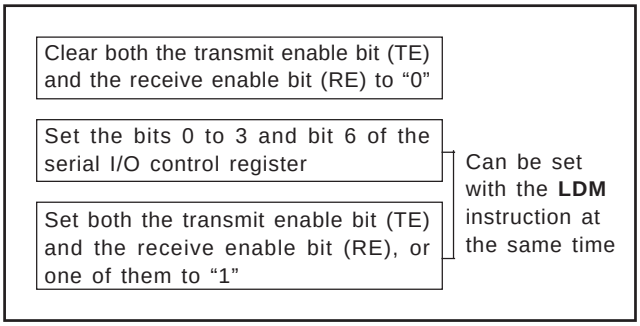


Fig. 6 Sequence of setting serial I/O control register again

(2) The transmit shift completion flag (bit 2 of serial I/O status register (address 001916)) changes from “1” to “0” with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

(3) When data transmission is executed at the state that an external clock input is selected as the synchronous clock, set “1” to the transmit enable bit while the SCLK is “H” state. Also, write to the transmit buffer register while the SCLK is “H” state.

(4) When the transmit interrupt is used, set as the following sequence.

① Serial I/O transmit interrupt enable bit is set to “0” (disabled).

② Serial I/O transmit enable bit is set to “1”.

③ Serial I/O transmit interrupt request bit (bit 1 of interrupt request register 1 (address 003C16)) is set to “0” after 1 or more instructions have been executed.

④ Serial I/O transmit interrupt enable bit (bit 1 of interrupt control register 1 (address 003E16)) is set to “1” (enabled).

<Reason>

When the transmit enable bit is set to “1”, the transmit buffer empty flag (bit 0) and transmit shift completion flag (bit 2 of serial I/O status register (address 001916)) are set to “1”.

Accordingly, even if the timing when any of the above flags is set to “1” is selected for the transmit interrupt source, interrupt request occurs and the transmit interrupt request bit is set.

(5) Write to the baud rate generator (BRG) while the transmit/receive operation is stopped.

4. I/O pin function when serial I/O is enabled.
The pin functions of P12/SCLK and P13/$\overline{\text{SRDY}}$ are switched to as follows according to the setting values of a serial I/O mode selection bit (bit 6 of serial I/O control register (address 001A16)) and a serial I/O synchronous clock selection bit (bit 1 of serial I/O control register).
(1) Serial I/O mode selection bit → "1" :
Clock synchronous type serial I/O is selected.
• Setup of a serial I/O synchronous clock selection bit
"0" : P12 pin turns into an output pin of a synchronous clock.
"1" : P12 pin turns into an input pin of a synchronous clock.
• Setup of a $\overline{\text{SRDY}}$ output enable bit (SRDY)
"0" : P13 pin can be used as a normal I/O pin.
"1" : P13 pin turns into a $\overline{\text{SRDY}}$ output pin.

(2) Serial I/O mode selection bit → "0" :
Clock asynchronous (UART) type serial I/O is selected.
• Setup of a serial I/O synchronous clock selection bit
"0": P12 pin can be used as a normal I/O pin.
"1": P12 pin turns into an input pin of an external clock.
• When clock asynchronous (UART) type serial I/O is selected, it functions P13 pin. It can be used as a normal I/O pin.

Notes on A/D conversion

1. Analog input pin
Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01μF to 1μF. Further, be sure to verify the operation of application products on the user side.
<Reason>
An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A/D conversion/comparison precision to be worse.

2. Clock frequency during A/D conversion
The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. This may cause the A/D conversion precision to be worse. Accordingly, set f(XIN) in order that the A/D conversion clock is 500 kHz or over during A/D conversion.

3. A/D conversion accuracy
As for AD translation accuracy, on the following operating conditions, accuracy may become low.
(1) Since the analog circuit inside a microcomputer becomes sensitive to noise when VREF voltage is set up lower than Vcc voltage, accuracy may become low rather than the case where VREF voltage and Vcc voltage are set up to the same value.
(2) When VREF voltage is lower than [3.0 V], the accuracy at the low temperature may become extremely low compared with that at room temperature. When the system would be used at low temperature, the use at VREF=3.0 V or more is recommended.

Notes on Watchdog Timer

1. The watchdog timer is operating during the wait mode. Write data to the watchdog timer control register to prevent timer underflow.

2. The watchdog timer stops during the stop mode. However, the watchdog timer is running during the oscillation stabilizing time after the **STP** instruction is released. In order to avoid the underflow of the watchdog timer, the watchdog timer count source selection bit (bit 7 of watchdog timer control register (address 003916)) before executing the **STP** instruction.

3. The **STP** instruction function selection bit (bit 6 of watchdog timer control register (address 003916)) can be rewritten only once after releasing reset. After rewriting it is disable to write any data to this bit.

Notes on RESET pin

1. Connecting capacitor
In case where the $\overline{\text{RESET}}$ signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and the Vss pin. And use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following :
• Make the length of the wiring which is connected to a capacitor as short as possible.
• Be sure to verify the operation of application products on the user side.
<Reason>
If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

Notes on Clock Generating Circuit

1. Switch of ceramic/quartz-crystal oscillation and RC oscillation
After releasing reset, the oscillation mode selection bit (bit 5 of CPU mode register (address 003B16)) is “0” (ceramic/quartz-crystal oscillation selected). When the RC oscillation is used, after releasing reset, set this bit to “1”.

2. Double-speed mode
The double-speed mode can be used only when a ceramic oscillation is selected. Do not use it when an RC oscillation is selected.

3. CPU mode register
Oscillation mode selection bit (bit 5), processor mode bits (bits 1 and 0) of CPU mode register (address 003B16) are used to select oscillation mode and to control operation modes of the microcomputer. In order to prevent the dead-lock by erroneously writing (ex. program run-away), these bits can be rewritten only once after releasing reset. After rewriting, it is disabled to write any data to the bit. (The emulator MCU “M37542RSS” is excluded.)
Also, when the read-modify-write instructions (SEB, CLB, etc.) are executed to bits 2 to 4, 6 and 7, bits 5, 1 and 0 are locked.

4. Clock division ratio, XIN oscillation control, on-chip oscillator control
The state transition shown in Fig. 49 can be performed by setting the clock division ratio selection bits (bits 7 and 6), XIN oscillation control bit (bit 4), on-chip oscillator oscillation control bit (bit 3) of CPU mode register. Be careful of notes on use in Fig. 49.

5. On-chip oscillator operation
When the MCU operates by the on-chip oscillator for the main clock, connect XIN pin to VCC through a 1 kΩ to 10 kΩ resistor and leave XOUT pin open.
The clock frequency of the on-chip oscillator depends on the supply voltage and the operation temperature range.
Be careful that this margin of frequencies when designing application products.

6. Ceramic resonator
When the ceramic resonator/quartz-crystal oscillation is used for the main clock, connect the ceramic resonator and the external circuit to pins XIN and XOUT at the shortest distance. A feedback resistor is built-in.

7. RC oscillation
When the RC oscillation is used for the main clock, connect the XIN pin and XOUT pin to the external circuit of resistor R and the capacitor C at the shortest distance.
The frequency is affected by a capacitor, a resistor and a microcomputer.
So, set the constants within the range of the frequency limits.

8. External clock
When the external signal clock is used for the main clock, connect the XIN pin to the clock source and leave XOUT pin open.
Select “0” (ceramic oscillation) to oscillation mode selection bit.

9. Count source (Timer 1, Timer A, Timer X, Serial I/O, A/D converter, Watchdog timer)
The count sources of these functions are affected by the clock division selection bit of the CPU mode register.
The f(XIN) clock is supplied to the watchdog timer when selecting f(XIN) as the CPU clock.
The on-chip oscillator output is supplied to these functions when selecting the on-chip oscillator output as the CPU clock.

Notes on Oscillation Control

1. Oscillation stop detection circuit
(1) When the stop mode is used, set the oscillation stop detection function to “invalid”.

(2) When the ceramic or RC oscillation is stopped (bit 4 of CPU mode register (address 003B16)), set the oscillation stop detection function to “invalid”.

(3) The oscillation stop detection circuit is not included in the emulator MCU “M37542RSS”.

2. Stop mode
(1) When the stop mode is used, set the oscillation stop detection function to “invalid”.

(2) When the stop mode is used, set “0” to the **STP** instruction function selection bit of the watchdog timer control register (bit 6 of watchdog timer control register (address 003916)).

(3) The oscillation stabilizing time after release of **STP** instruction can be selected from “set automatically”/“not set automatically” by the oscillation stabilizing time set bit after release of the **STP** instruction (bit 0 of MISRG (address 003816)). When “0” is set to this bit, “0116” is set to timer 1 and “FF16” is set to prescaler 1 automatically at the execution of the STP instruction. When “1” is set to this bit, set the wait time to timer 1 and prescaler 1 according to the oscillation stabilizing time of the oscillation. Also, when timer 1 is used, set values again to timer 1 and prescaler 1 after system is returned from the stop mode.

(4) The STP instruction cannot be used when the on-chip oscillator is selected by the clock division ratio selection bits (bits 7 and 6 of CPU mode register (address 003B16)).

(5) When the stop mode is used, set the on-chip oscillator oscillation control bit (bit 3 of CPU mode register (address 003B16)) to “1” (on-chip oscillator oscillation stop).

(6) Do not execute the **STP** instruction during the A/D conversion.

Notes on Oscillation Stop Detection Circuit

1. Oscillation stop detection status bit is initialized by the following operation.
(1) External reset
(2) Write "0" data to the ceramic or RC oscillation stop detection function active bit.

2. The oscillation stop detection circuit is not included in the emulator MCU "M37544RSS".

Note on Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.
In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the supply voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

NOTES ON HARDWARE

1. Handling of Power Source Pin
In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μF to 0.1 μF is recommended.

2. Handling of CNVss Pin
The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (V_{PP} pin) as well.
To improve the noise reduction, connect a track between CNVss pin and Vss pin with 1 to 10 kΩ resistance.

NOTES ON QzROM

Product shipped in blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur.
Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

Precautions Regarding Overvoltage

Make sure that voltage exceeding the V_{CC} pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in Figure below does not occur for CNV_{SS} pin (V_{PP} power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.

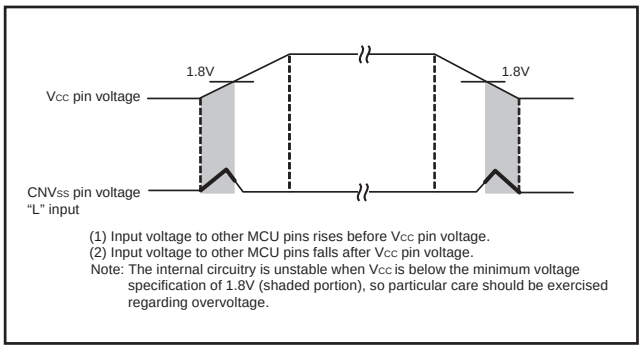


Fig. 7 Timing Diagram (bold-lined periods are applicable)

Notes on QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .msk) which is made by the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "00_{16}" and "FF_{16}" can not be accepted.
- Set "FF_{16}" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF_{16}" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

DATA REQUIRED FOR QzROM WRITING ORDERS

The following are necessary when ordering a QzROM product shipped after writing:
1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file
* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).
Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

REVISION HISTORY	7544 Group (QzROM version) Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Oct 26, 2004	–	First edition issued
1.01	Nov 24, 2004	46 48-50	Table 12 Electrical characteristics: Minimum value of V_{RAM} revised. The followings are added; - A/D Converter characteristics - Timing requirements - Switching Characteristics - Timing chart
1.02	Jul 20, 2005	All pages 2, 4, 5, 7 3 7 12 18 41 45 53 61	Delete the following: "PRELIMINARY". Package names are revised. Table 1 Performance overview is added. Table 2 is deleted. ROM code protect is added. Fig.10 is partly revised. Termination of unused pins is added. (4)Wiring to CNV_{SS} pin is deleted. (4)Wiring to V_{PP} pin is revised. Fig.49 is partly revised. Table 8 is partly revised. PACKAGE OUTLINE is revised. Product shipped in blank, NOTES ON QzROM, DATA REQUIRED FOR QzROM WRITING ORDERS are added.
1.03	Mar 31, 2009	3,8 13 17 18 19 20-25 36, 70, 71 36 37 41 45-49 50 51 54 55 65 66 70	42S1M package added Fig. 11 Memory map diagram revised Fig. 15 (5)Port $P1_1$ revised Fig. 16 (8)Port $P1_4$ revised Table 7 X_{IN}, X_{OUT} added “Interrupts” revised Operation of STP instruction disable bit → Operation of STP instruction function selection bit Watchdog Timer “Operation of watchdog timer H count source selection bit” revised “Operation of STP instruction function selection bit” revised “Notes on watchdog timer” added -Fig. 36 Block diagram of watchdog timer revised -Fig. 37 Structure of watchdog timer control register revised “-Clock division ratio, X_{IN} oscillation control, on-chip oscillator control” added “QzROM Writing Mode”added “Processor Status Register”revised Fig. 57 V_{PP} → CNV_{SS} 5. Setup for I/O ports “Note” deleted “NOTES ON QzROM” added -“1. Processor Status Register”revised APPENDIX “Fig. 2 Sequence of PLP Instruction execution deleted. -Figure title of Fig. 3 revised “3. Modifying output data with bit managing instruction” revised Notes on A/D conversion 1. Analog input pin revised Notes on Watchdog Timer revised

REVISION HISTORY	7544 Group (QzROM version) Data Sheet

Rev.	Date	Description	
		Page	Summary
1.03	Mar 31, 2009	71 72	Notes on Clock Generation Circuit “9. Count source” added “NOTES ON QzROM” revised

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