

To our customers,

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## 1. Overview

The M16C/28 Group (M16C/28 and M16C/28B) MCU are single-chip control MCU, fabricated using high-performance silicon gate CMOS technology with the M16C/60 series CPU core. The M16C/28 Group (M16C/28 and M16C/28B) are housed in 64-pin and 80-pin plastic molded LQFP packages and also in 85-pin plastic molded TFLGA (Thin Fine Pitch Land Grid Array) package. With a 1-Mbyte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed. It includes a multiplier and DMAC adequate for office automation, communication devices and other high-speed processing applications.

The M16C/28 has Normal-ver., T-ver., and V-ver.. The M16C/28B has Normal-ver. only.

This hardware manual describes the Normal-ver. only. Please contact Renesas Technology Corp. for T-ver./V-ver. information.

### 1.1 Applications

Audio, cameras, office equipment, communication equipment, portable equipment, home appliances (inverter solution), motor control, industrial equipment, etc.

## 1.2 Performance Overview

Table 1.1 and 1.2 outline performance overview of the M16C/28 Group (M16C/28, M16C/28B).

**Table 1.1 M16C/28 Group (M16C/28, M16C/28) Performance (80/85-Pin Package)**

	Item	Performance
CPU	Number of basic instructions	91 instructions
	Minimum instruction execution time	41.7 ns (f(BCLK) = 24 MHz, V <sub>CC</sub> = 4.2 V to 5.5 V) (M16C/28B) 50 ns (f(BCLK) = 20 MHz, V <sub>CC</sub> = 3.0 V to 5.5 V) (M16C/28, M16C/28B) 100 ns (f(BCLK) = 10 MHz, V <sub>CC</sub> = 2.7 V to 5.5 V) (M16C/28, M16C/28B)
	Operation mode	Single chip mode
	Address space	1M bytes
	Memory capacity	See <b>Table 1.3</b>
Peripheral Function	I/O port	Input/Output : 71 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
	Serial I/O	2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I <sup>2</sup> C bus <sup>(1)</sup> , or IEBus <sup>(2)</sup> 2 channels (SI/O3, SI/O4) Clock synchronous 1 channel (Multi-Master I <sup>2</sup> C bus <sup>(1)</sup> )
	A/D converter	10 bits x 24 channels
	DMAC	2 channels
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	25 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits • Main clock (*) • Sub-clock (*) • On-chip oscillator • PLL frequency synthesizer (* ) Equipped with a built-in feedback resistor
	Oscillation Stop Detect Function	Main clock oscillation stop, re-oscillation detect function
	Voltage detection circuit	Available
Electrical Characteristics	Power supply voltage	V <sub>CC</sub> = 4.2 V to 5.5 V (f(BCLK) = 24 MHz) (M16C/28B) V <sub>CC</sub> = 3.0 V to 5.5 V (f(BCLK) = 20 MHz) (M16C/28, M16C/28B) V <sub>CC</sub> = 2.7 V to 5.5 V (f(BCLK) = 10 MHz) (M16C/28, M16C/28B)
	Power consumption	16 mA (V <sub>CC</sub> = 5V, f(BCLK) = 20 MHz) 25 μA (f(XCIN) = 32 KHz on RAM) 3.0 μA (V <sub>CC</sub> = 3V, f(XCIN) = 32 KHz, in wait mode) 0.7 μA (V <sub>CC</sub> = 3V, in stop mode)
Flash Memory	Program/erase supply voltage	2.7 V to 5.5 V
	Program and erase endurance	100 times (all space) or 1,000 times (Blocks 0 to 5) /10,000 times (Block A, Block B <sup>(3)</sup> )
Operating Ambient Temperature		-20 to 85°C/-40 to 85°C <sup>(3)</sup>
Package		80-pin plastic mold LQFP, 85-pin plastic mold TFLGA

NOTES:

- I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.
- IEBus is a trademark of NEC Electronics Corporation.
- Refer to **Table 1.5** to **1.7** for number of program/erase.
- Use PLL frequency synthesizer to use M16C/28B at f(BCLK) = 24 MHz.

**Table 1.2 M16C/28 Group (M16C/28, M16C/28B) (64-Pin Package)**

	Item	Performance
CPU	Number of basic instructions	91 instructions
	Minimum instruction execution time	41.7 ns (f(BCLK) = 24 MHz, VCC = 4.2 V to 5.5 V) (M16C/28B) 50 ns (f(BCLK) = 20 MHz, VCC = 3.0V to 5.5V) (M16C/28, M16C/28B) 100 ns (f(BCLK) = 10 MHz, VCC = 2.7V to 5.5V) (M16C/28, M16C/28B)
	Operation mode	Single chip mode
	Address space	1M bytes
	Memory capacity	See <b>Table 1.3</b>
Peripheral Function	I/O Port	Input/Output : 55 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels )
	Serial I/O	2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I <sup>2</sup> C bus <sup>(1)</sup> , or IEBus <sup>(2)</sup> 1 channels (SI/O3, SI/O4) Clock synchronous 1 channel (Multi-Master I <sup>2</sup> C bus <sup>(1)</sup> )
	A/D converter	10 bits x 13 channels
	DMAC	2 channels
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	24 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits • Main clock(*) • Sub-clock(*) • On-chip oscillator • PLL frequency synthesizer (*) Equipped with a built-in feedback resistor
	Oscillation Stop Detect Function	Main clock oscillation stop, re-oscillation detect function
	Voltage detection circuit	Available
Electrical Characteristics	Power supply voltage	VCC = 4.2 V to 5.5 V (f(BCLK) = 24 MHz) (M16C/28) VCC = 3.0 V to 5.5 V (f(BCLK) = 20 MHz) (M16C/28, M16C/28B) VCC = 2.7 V to 5.5 V (f(BCLK) = 10 MHz) (M16C/28, M16C/28B)
	Power consumption	16 mA (VCC = 5 V, f(BCLK) = 20 MHz) 25 $\mu$ A (f(XCIN) = 32 KHz on RAM) 3.0 $\mu$ A (VCC = 3 V, f(XCIN) = 32 KHz, in wait mode) 0.7 $\mu$ A (VCC = 3 V, in stop mode)
Flash Memory	Program/erase supply voltage	2.7 V to 5.5 V
	Program and erase endurance	100 times (all space) or 1,000 times (Blocks 0 to 5) /10,000 times (Block A, Block B <sup>(3)</sup> )
Operating Ambient Temperature		-20 to 85C°/-40 to 85C° <sup>(3)</sup>
Package		64-pin plastic mold LQFP

## NOTES:

1. I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. Refer to **Table 1.5 to 1.7** for number of program/erase.
4. Use PLL frequency synthesizer to use M16C/28B at f(BCLK) = 24 MHz.

### 1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 80-pin and 85-pin package.  
 Figure 1.2 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 64-pin package.

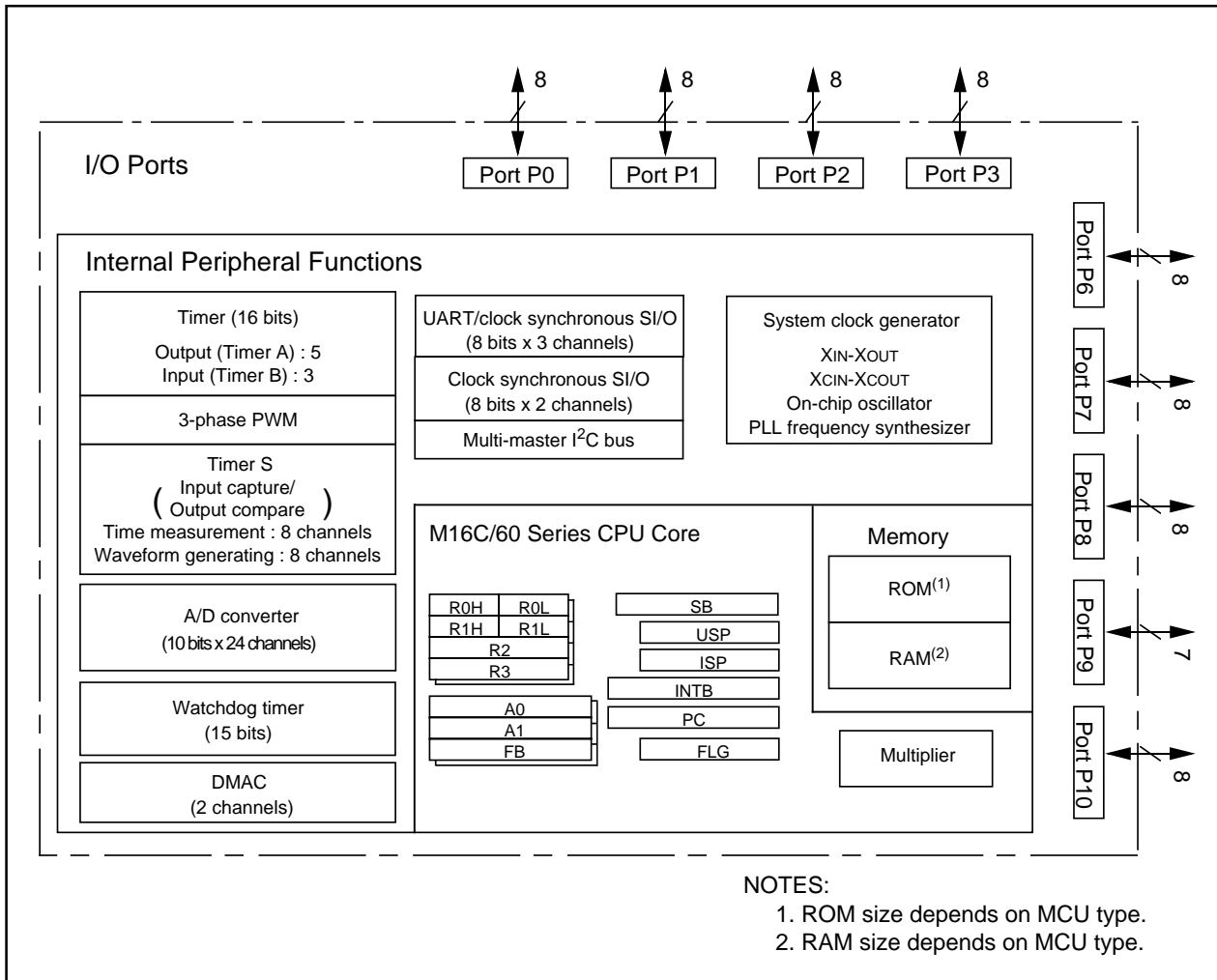


Figure 1.1 M16C/28 Group (M16C/28, M16C/28B), 80-Pin/85-Pin Block Diagram

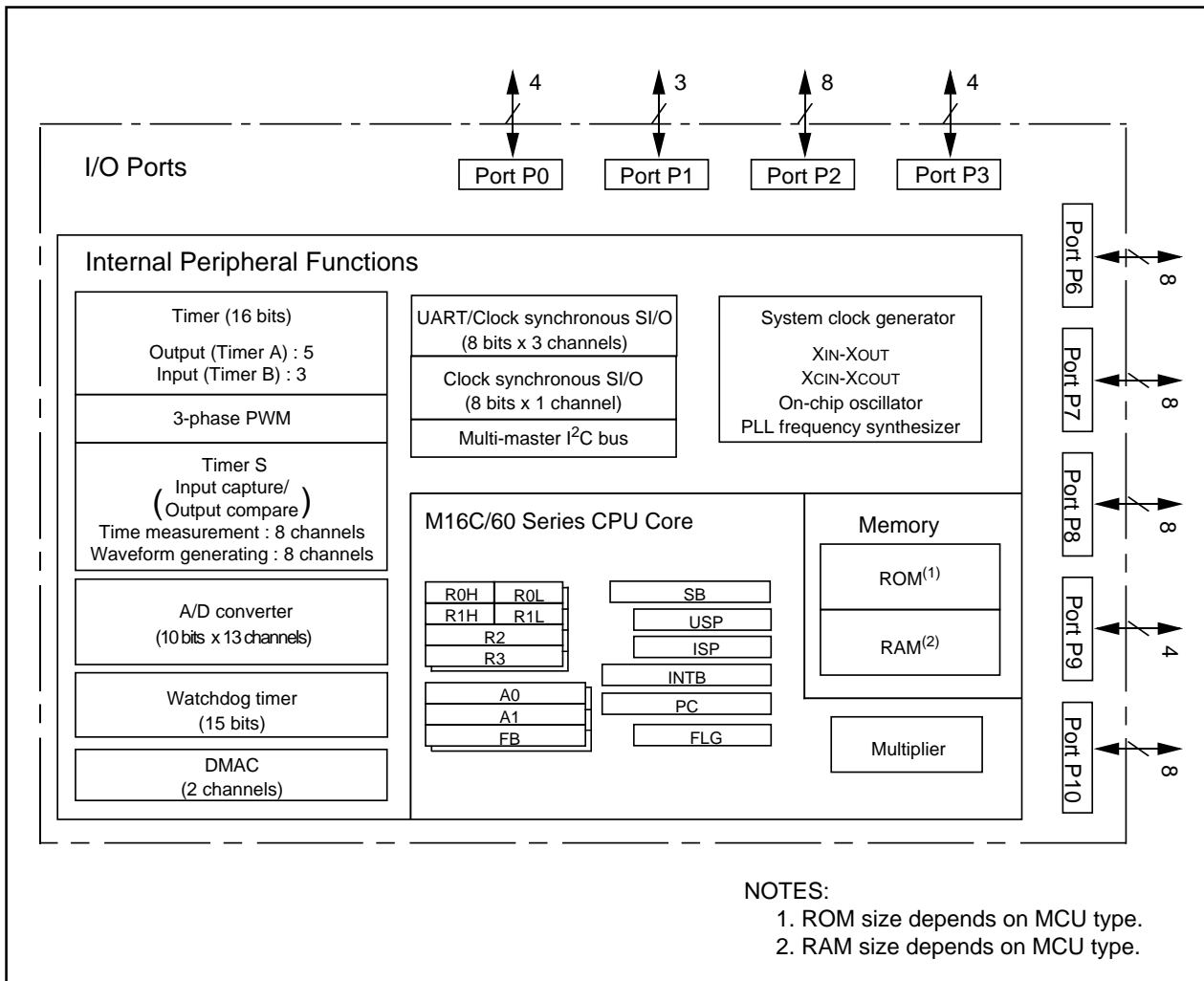


Figure 1.2 M16C/28 Group (M16C/28, M16C/28B), 64-Pin Block Diagram

## 1.4 Product Information

Tables 1.3 and 1.4 list the M16C/28 Group product information and Figure 1.3 shows the product numbering system. The specifications are partially different between normal-ver. and T/ V-ver..

**Table 1.3 M16C/28 Product List -Normal-ver.**

**As of September, 2006**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code		
M30280F6WG (N)	48 K + 4 K	4 K	PTLG0085JB-A (85F0G)	Flash Memory	U3, U5, U7, U9		
M30280F8WG (N)	64 K + 4 K	4 K					
M30280FAWG (N)	96 K + 4 K	8 K					
M30280F6HP (N)	48 K + 4 K	4 K	PLQP0080KB-A (80P6Q-A)				
M30280F8HP (N)	64 K + 4 K	4 K					
M30280FAHP (N)	96 K + 4 K	8 K					
M30280FCHP (N)	128 K + 4 K	12 K	PLQP0064KB-A (64P6Q-A)				
M30281F6HP (N)	48 K + 4 K	4 K					
M30281F8HP (N)	64 K + 4 K	4 K					
M30281FAHP (N)	96 K + 4 K	8 K					
M30281FCHP (N)	128 K + 4 K	12 K	PLQP0080KB-A (80P6Q-A)			Mask ROM	U3, U5
M30280M8-XXXHP (N)	64 K	4 K					
M30280MA-XXXHP (N)	96 K	8 K					
M30280MC-XXXHP (N)	128 K	12 K					
M30281M8-XXXHP (N)	64 K	4 K					
M30281MA-XXXHP (N)	96 K	8 K					
M30281MC-XXXHP (N)	128 K	12 K	PLQP0064KB-A (64P6Q-A)				

(N): New

**Table 1.4 M16C/28B Product List -Normal-ver.**

**As of September, 2006**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280FCBHP (D)	128 K + 4 K	12 K	PLQP0080KB-A (80P6Q-A)	Flash memory	U7
M30281FCBHP (D)	128 K + 4 K	12 K	PLQP0064KB-A (64P6Q-A)		

(D): Under development

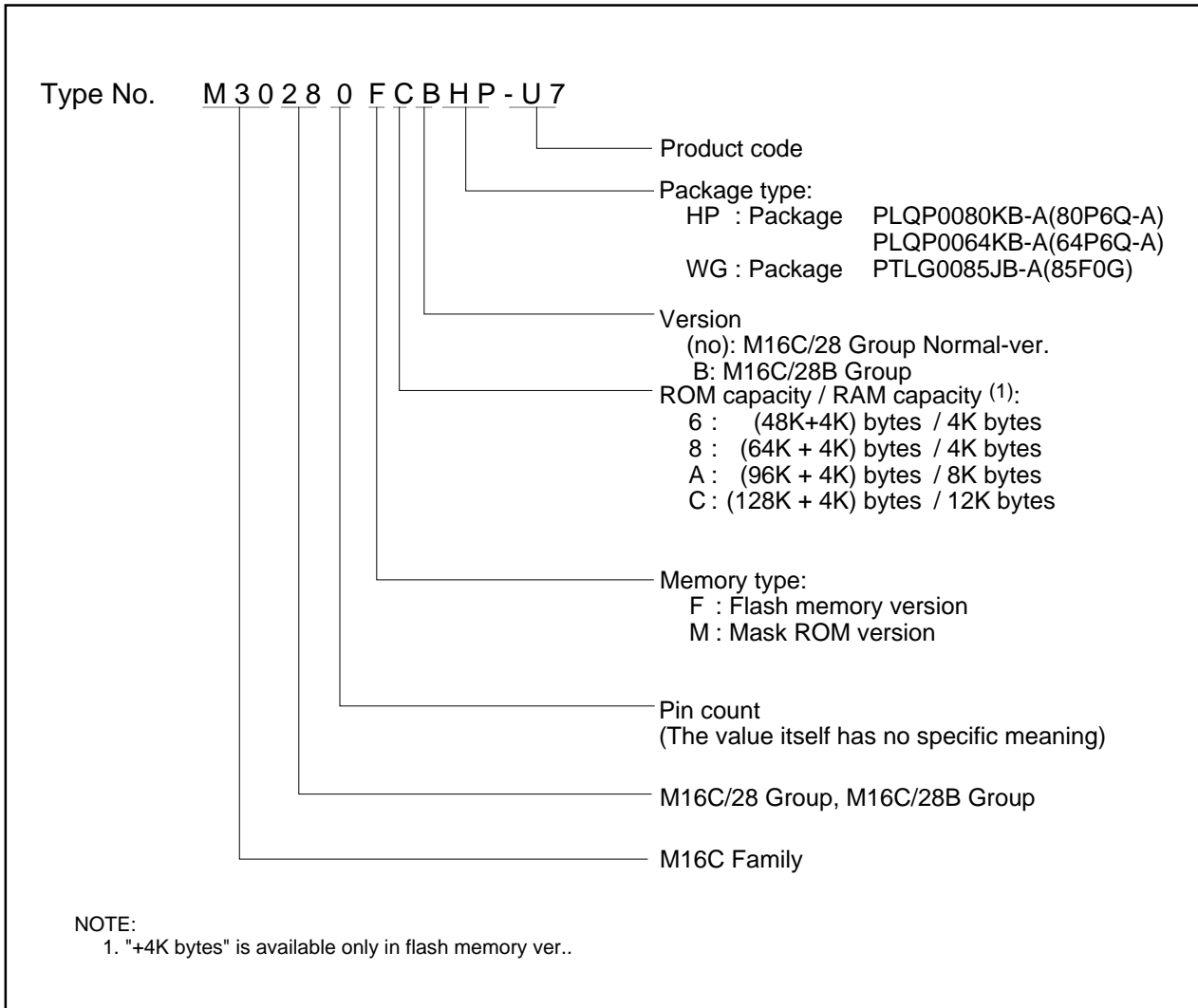


Figure 1.3 Product Numbering System

**Table 1.5 Product Code (Flash Memory-ver.) - M16C/28 Normal-ver., 64-Pin<sup>(1)</sup>/80-Pin<sup>(1)</sup>/85-Pin Package**

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead free	100	0 to 60°C	100	0 to 60°C	-40 to 85°C
U5					-20 to 85°C	
U7		1,000		10,000	-40 to 85°C	-40 to 85°C
U9				-20 to 85°C	-20 to 85°C	

## NOTE:

- The lead contained products, D3, D5, D7 and D9, are put together with U3, U5, U7 and U9 respectively. Lead-free (Sn-Ag-Cu plating) products can be mounted by both conventional Sn-Pb paste and Lead-free paste.

**Table 1.6 Product Code (Flash Memory-ver.) - M16C/28B Normal-ver., 64-Pin/85-Pin Package**

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U7	Lead-free	1,000	0 to 60°C	10,000	-40 to 85°C	-40 to 85°C

**Table 1.7 Product Code (Mask ROM ver.) - M16C/28B Normal-ver., 64-Pin/80-Pin/85-Pin Package**

Product Code	Package	Operating Ambient Temperature
U3	Lead-free	-40 to 85°C
U5		-20 to 85°C

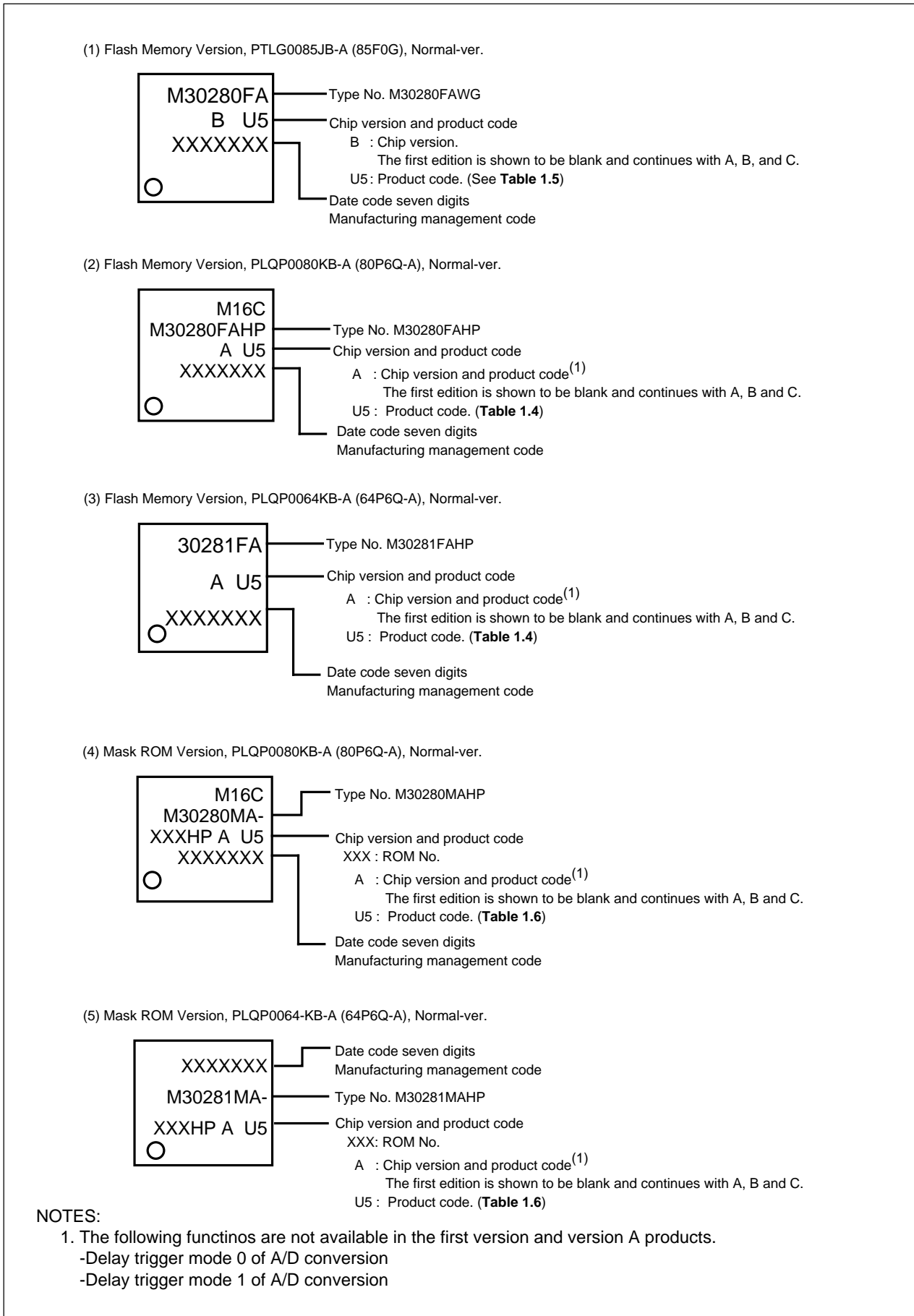
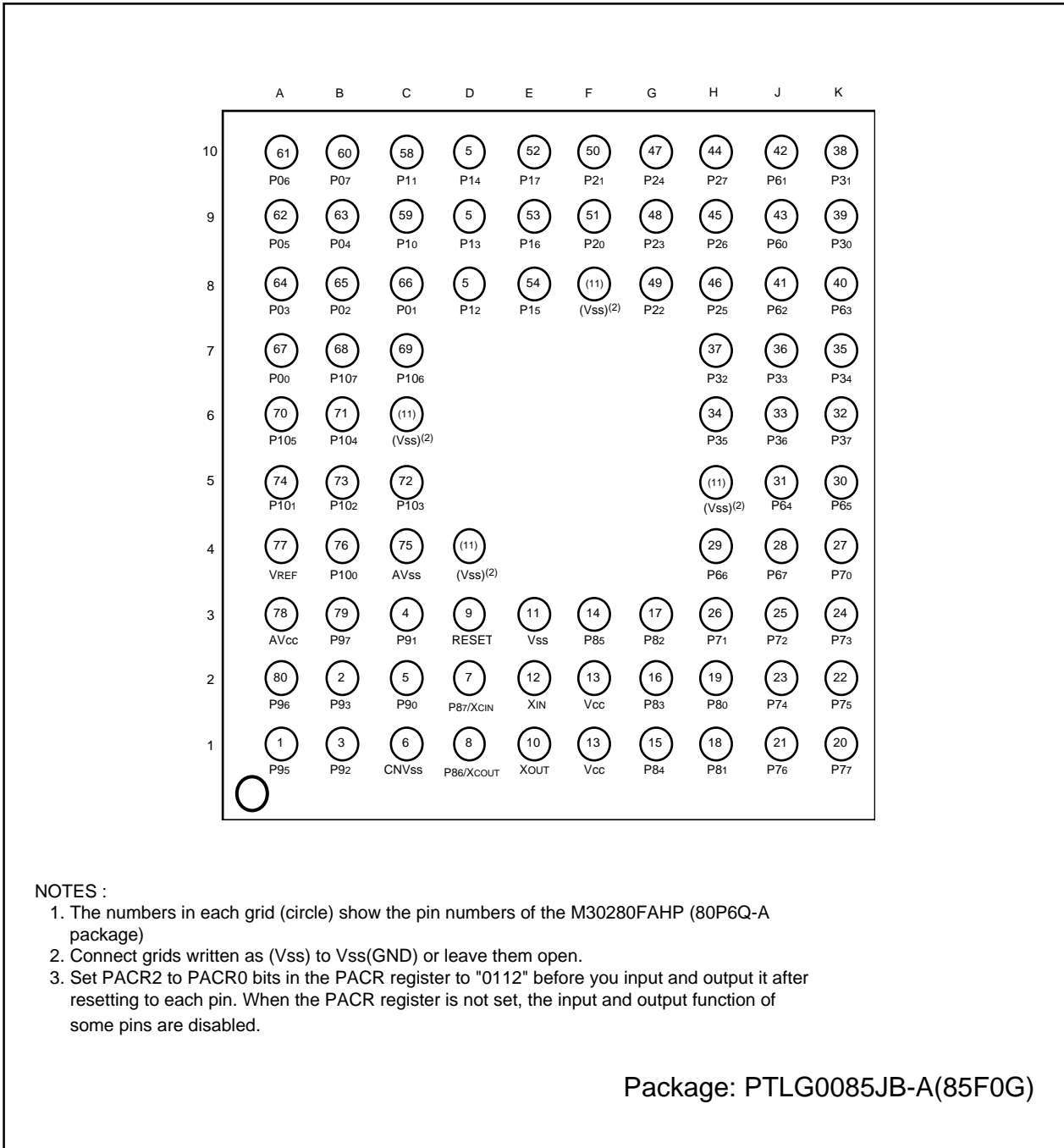


Figure 1.4 Marking Diagram-M16C/28 Normal-ver.

### 1.5 Pin Assignment

Figures 1.5 to 1.7 show the pin Assignments (top view).



NOTES :

1. The numbers in each grid (circle) show the pin numbers of the M30280FAHP (80P6Q-A package)
2. Connect grids written as (Vss) to Vss(GND) or leave them open.
3. Set PACR2 to PACR0 bits in the PACR register to "0112" before you input and output it after resetting to each pin. When the PACR register is not set, the input and output function of some pins are disabled.

Package: PTLG0085JB-A(85F0G)

Figure 1.5 Pin Assignment (Top View) of 85-pin Package

**Table 1.8 Pin Characteristics for 85-pin Package**

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I <sup>2</sup> C bus Pin	Analog Pin	PLQP0080KB-A Pin Number
A1		P95				CLK4		AN25	1
A2		P96				SOUT4		AN26	80
A3	AVcc								78
A4	VREF								77
A5		P101						AN1	74
A6		P105	$\overline{KI1}$					AN5	70
A7		P00						AN00	67
A8		P03						AN03	64
A9		P05						AN05	62
A10		P06						AN06	61
B1		P92		TB2IN					3
B2		P93						AN24	2
B3		P97				SIN4		AN27	79
B4		P100						AN0	76
B5		P102						AN2	73
B6		P104	$\overline{KI0}$					AN4	71
B7		P107	$\overline{KI3}$					AN7	68
B8		P02						AN02	65
B9		P04						AN04	63
B10		P07						AN07	60
C1	CNVss								6
C2		P90		TB0IN					5
C3		P91		TB1IN					4
C4	AVss								75
C5		P103						AN3	72
C6	Vss <sup>(1)</sup>								(11)
C7		P106	$\overline{KI2}$					AN6	69
C8		P01						AN01	66
C9		P10						AN20	59
C10		P11						AN21	58
D1	XCOUT	P86							8
D2	XCIN	P87							7
D3	$\overline{RESET}$								9
D4	Vss <sup>(1)</sup>								(11)
D8		P12						AN22	57
D9		P13						AN23	56
D10		P14							55
E1	XOUT								10
E2	XIN								12
E3	Vss								11

Table 1.8 Pin Characteristics for 85-pin Package (continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I <sup>2</sup> C bus Pin	Analog Pin	PLQP0080KB-A Pin Number
E8		P15	$\overline{\text{INT}}_3$	IDV				ADTRG	54
E9		P16	$\overline{\text{INT}}_4$	IDW					53
E10		P17	$\overline{\text{INT}}_5$	IDU	INPC17				52
F1	Vcc								13
F2	Vcc								13
F3		P85	$\overline{\text{NMI}}$	$\overline{\text{SD}}$					14
F8	Vss <sup>(1)</sup>								(11)
F9		P20			OUTC10 / INPC10		SDAMM		51
F10		P21			OUTC11 / INPC11		SCLMM		50
G1		P84	$\overline{\text{INT}}_2$	ZP					15
G2		P83	$\overline{\text{INT}}_1$						16
G3		P82	$\overline{\text{INT}}_0$						17
G8		P22			OUTC12 / INPC12				49
G9		P23			OUTC13 / INPC13				48
G10		P24			OUTC14 / INPC14				47
H1		P81		TA4IN / $\overline{\text{U}}$					18
H2		P80		TA4OUT / U					19
H3		P71		TA0IN		RxD2 / SCL2 / CLK1			26
H4		P66				RxD1			29
H5	Vss <sup>(1)</sup>								(11)
H6		P35							34
H7		P32				SOUT3			37
H8		P25			OUTC15 / INPC15				46
H9		P26			OUTC16 / INPC16				45
H10		P27			OUTC17 / INPC17				44
J1		P76		TA3OUT					21
J2		P74		TA2OUT / W					23
J3		P72		TA1OUT / V		CLK2 / RxD1			25
J4		P67				TxD1			28
J5		P64				RTS1 / CTS1 / CTS0 / CLKS1			31
J6		P36							33
J7		P33							36
J8		P62				RxD0			41
J9		P60				$\overline{\text{RTS}}_0 / \overline{\text{CTS}}_0$			43
J10		P61				CLK0			42
K1		P77		TA3IN					20
K2		P75		TA2IN / $\overline{\text{W}}$					22
K3		P73		TA1IN / $\overline{\text{V}}$		$\overline{\text{CTS}}_2 / \overline{\text{RTS}}_2 / \overline{\text{TXD}}_1$			24
K4		P70		TA0OUT		TxD2 / SDA2 / RTS1 / CTS1 / CTS0 / CLKS1			27
K5		P65				CLK1			30
K6		P37							32
K7		P34							35
K8		P63				TxD0			40
K9		P30				CLK3			39
K10		P31				SIN3			38

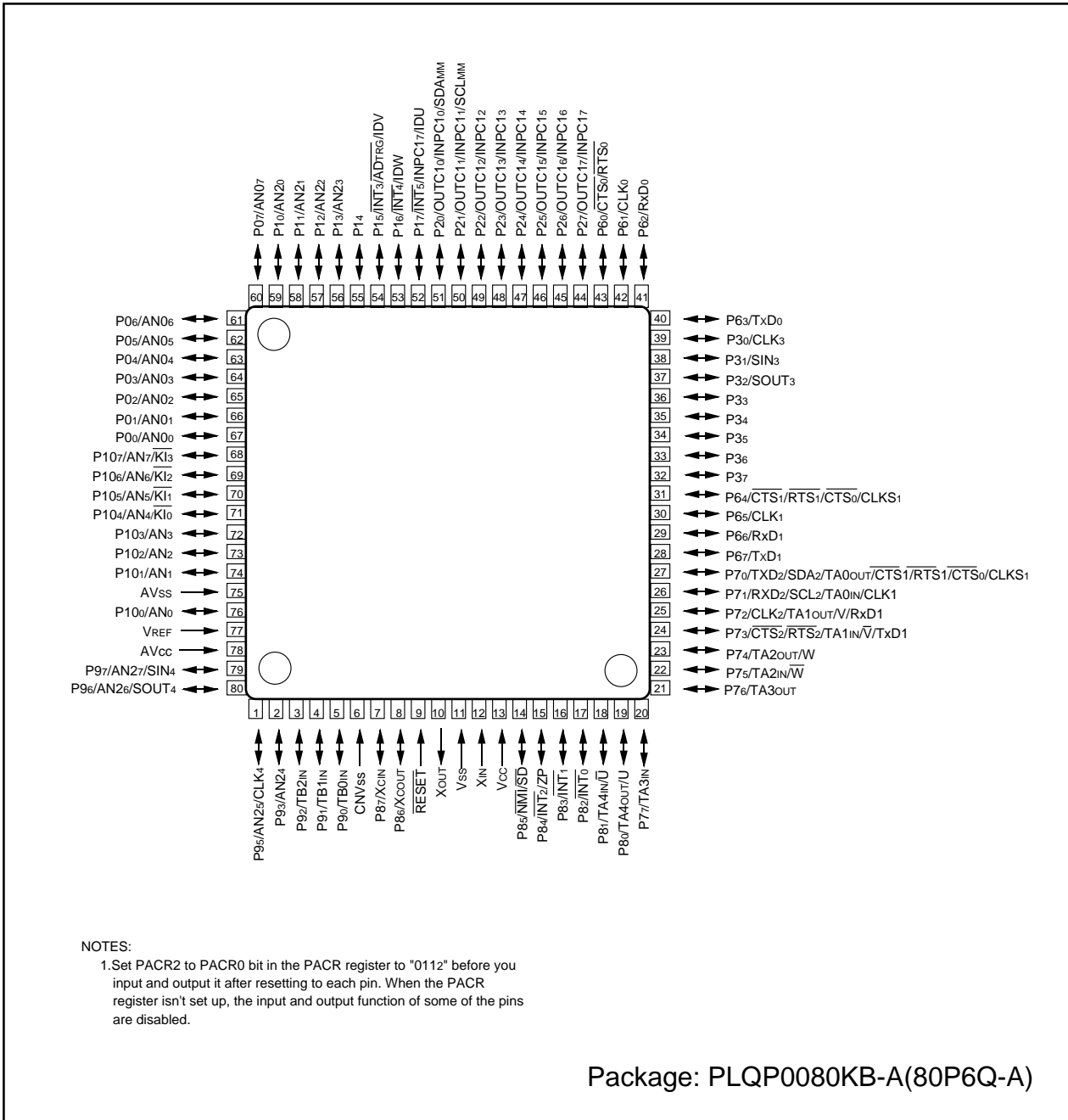


Figure 1.5 Pin Assignment (Top View) of 80-Pin Package

NOTES:

1. Set PACR2 to PACR0 bit in the PACR register to "0112" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Table 1.9 Pin Characteristics for 80-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I <sup>2</sup> C bus Pin	Analog Pin
1		P95				CLK4		AN25
2		P93						AN24
3		P92		TB2IN				
4		P91		TB1IN				
5		P90		TB0IN				
6	CNVss							
7	XCIN	P87						
8	XCOUT	P86						
9	RESET							
10	XOUT							
11	Vss							
12	XIN							
13	Vcc							
14		P85	NMI	SD				
15		P84	INT <sub>2</sub>	ZP				
16		P83	INT <sub>1</sub>					
17		P82	INT <sub>0</sub>					
18		P81		TA4IN / $\bar{U}$				
19		P80		TA4OUT / U				
20		P77		TA3IN				
21		P76		TA3OUT				
22		P75		TA2IN / $\bar{W}$				
23		P74		TA2OUT / W				
24		P73		TA1IN / $\bar{V}$		CTS <sub>2</sub> / RTS <sub>2</sub> / TxD <sub>1</sub>		
25		P72		TA1OUT / V		CLK <sub>2</sub> / RxD <sub>1</sub>		
26		P71		TA0IN		RxD <sub>2</sub> / SCL <sub>2</sub> / CLK <sub>1</sub>		
27		P70		TA0OUT		TxD <sub>2</sub> / SDA <sub>2</sub> / RTS <sub>1</sub> / CTS <sub>1</sub> / CTS <sub>0</sub> / CLKS <sub>1</sub>		
28		P67				TxD <sub>1</sub>		
29		P66				RxD <sub>1</sub>		
30		P65				CLK <sub>1</sub>		
31		P64				RTS <sub>1</sub> / CTS <sub>1</sub> / CTS <sub>0</sub> / CLKS <sub>1</sub>		
32		P37						
33		P36						
34		P35						
35		P34						
36		P33						
37		P32				SOUT <sub>3</sub>		
38		P31				SIN <sub>3</sub>		
39		P30				CLK <sub>3</sub>		
40		P63				TxD <sub>0</sub>		

**Table 1.9 Pin Characteristics for 80-Pin Package (Continued)**

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I <sup>2</sup> C bus Pin	Analog Pin
41		P62				RxD0		
42		P61				CLK0		
43		P60				$\overline{\text{RTS}}_0 / \overline{\text{CTS}}_0$		
44		P27			OUTC17 / INPC17			
45		P26			OUTC16 / INPC16			
46		P25			OUTC15 / INPC15			
47		P24			OUTC14 / INPC14			
48		P23			OUTC13 / INPC13			
49		P22			OUTC12 / INPC12			
50		P21			OUTC11 / INPC11		SCLMM	
51		P20			OUTC10 / INPC10		SDAMM	
52		P17	$\overline{\text{INT}}_5$	IDU	INPC17			
53		P16	$\overline{\text{INT}}_4$	IDW				
54		P15	$\overline{\text{INT}}_3$	IDV				$\overline{\text{ADTRG}}$
55		P14						
56		P13						AN23
57		P12						AN22
58		P11						AN21
59		P10						AN20
60		P07						AN07
61		P06						AN06
62		P05						AN05
63		P04						AN04
64		P03						AN03
65		P02						AN02
66		P01						AN01
67		P00						AN00
68		P107	$\overline{\text{KI}}_3$					AN7
69		P106	$\overline{\text{KI}}_2$					AN6
70		P105	$\overline{\text{KI}}_1$					AN5
71		P104	$\overline{\text{KI}}_0$					AN4
72		P103						AN3
73		P102						AN2
74		P101						AN1
75	AVss							
76		P100						AN0
77	VREF							
78	AVcc							
79		P97				SIN4		AN27
80		P96				SOUT4		AN26

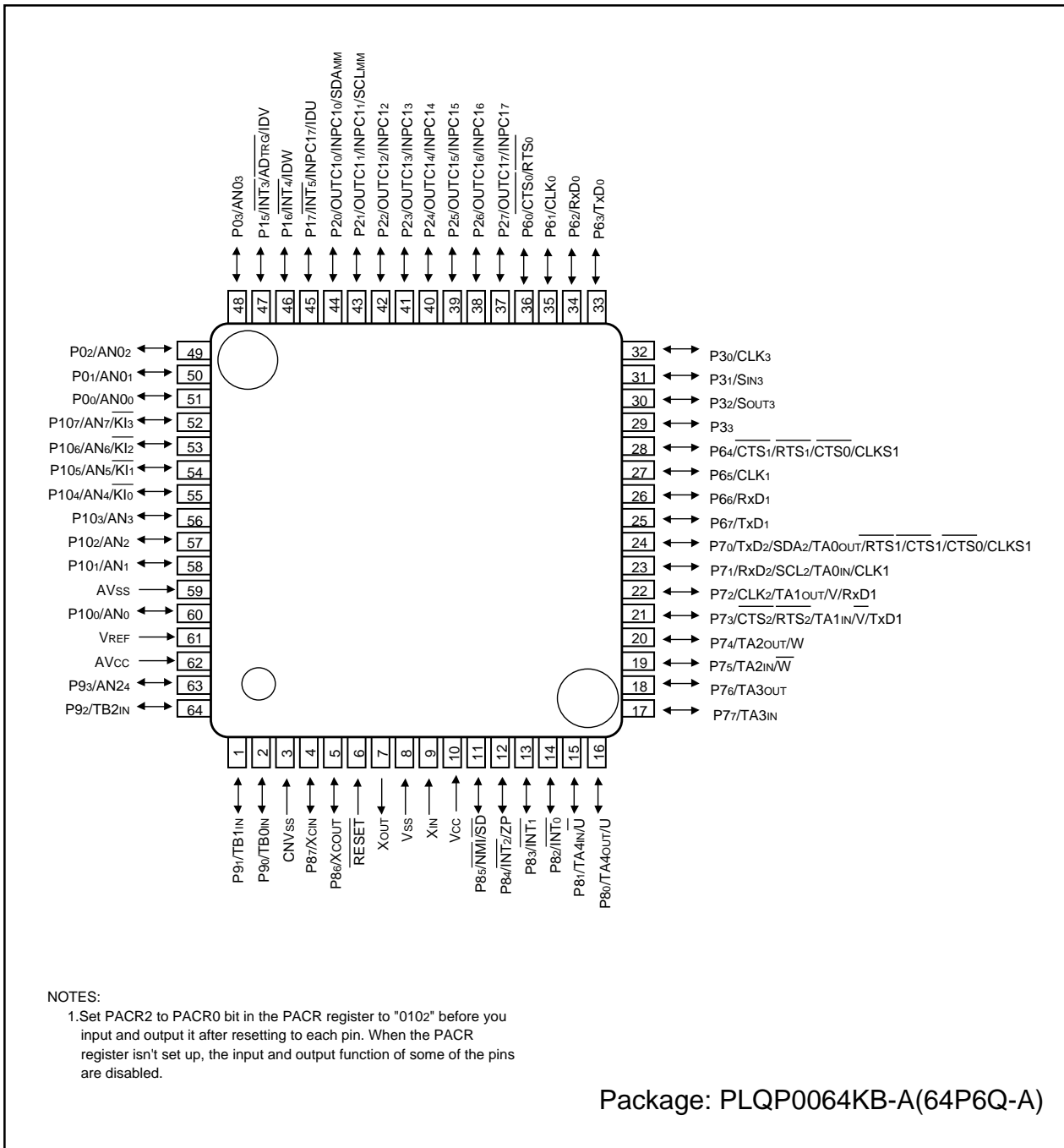


Figure 1.6 Pin Assignment (Top View) of 64-Pin Package

**Table 1.10 Pin Characteristics for 64-Pin Package**

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I <sup>2</sup> C bus Pin	Analog Pin
1		P91		TA1IN				
2		P90		TB0IN				
3	CNVss							
4	XCIN	P87						
5	XcOUT	P86						
6	RESET							
7	XOUT							
8	Vss							
9	XIN							
10	Vcc							
11		P85	NMI	SD				
12		P84	INT <sub>2</sub>	ZP				
13		P83	INT <sub>1</sub>					
14		P82	INT <sub>0</sub>					
15		P81		TA4IN / $\bar{U}$				
16		P80		TA4OUT / U				
17		P77		TA3IN				
18		P76		TA3OUT				
19		P75		TA2IN / $\bar{W}$				
20		P74		TA2OUT / W				
21		P73		TA1IN / $\bar{V}$		CTS <sub>2</sub> / $\bar{RTS}_2$ / TxD <sub>1</sub>		
22		P72		TA1OUT / V		CLK <sub>2</sub> / RxD <sub>1</sub>		
23		P71		TA0IN		RxD <sub>2</sub> / SCL <sub>2</sub> / CLK <sub>1</sub>		
24		P70		TA0OUT		TxD <sub>2</sub> / SDA <sub>2</sub> / $\bar{RTS}_1$ / CTS <sub>1</sub> / $\bar{CTS}_0$ / CLKS <sub>1</sub>		
25		P67				TxD <sub>1</sub>		
26		P66				RxD <sub>1</sub>		
27		P65				CLK <sub>1</sub>		
28		P64				RTS <sub>1</sub> / CTS <sub>1</sub> / $\bar{CTS}_0$ / CLKS <sub>1</sub>		
29		P33						
30		P32				SOUT <sub>3</sub>		
31		P31				SIN <sub>3</sub>		
32		P30				CLK <sub>3</sub>		
33		P63				TxD <sub>0</sub>		
34		P62				RxD <sub>0</sub>		
35		P61				CLK <sub>0</sub>		
36		P60				$\bar{RTS}_0$ / $\bar{CTS}_0$		
37		P27			OUTC <sub>17</sub> / INPC <sub>17</sub>			
38		P26			OUTC <sub>16</sub> / INPC <sub>16</sub>			
39		P25			OUTC <sub>15</sub> / INPC <sub>15</sub>			
40		P24			OUTC <sub>14</sub> / INPC <sub>14</sub>			

**Table 10 Pin Characteristics for 64-Pin Package (Continued)**

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I <sup>2</sup> C bus Pin	Analog Pin
41		P23			OUTC13 / INPC13			
42		P22			OUTC12 / INPC12			
43		P21			OUTC11 / INPC11		SCLMM	
44		P20			OUTC10 / INPC10		SDAMM	
45		P17	$\overline{\text{INT}}_5$	IDU	INPC17			
46		P16	$\overline{\text{INT}}_4$	IDW				
47		P15	$\overline{\text{INT}}_3$	IDV				$\overline{\text{ADTRG}}$
48		P03						AN03
49		P02						AN02
50		P01						AN01
51		P00						AN00
52		P107	$\overline{\text{KI}}_3$					AN7
53		P106	$\overline{\text{KI}}_2$					AN6
54		P105	$\overline{\text{KI}}_1$					AN5
55		P104	$\overline{\text{KI}}_0$					AN4
56		P103						AN3
57		P102						AN2
58		P101						AN1
59	AVss							
60		P100						AN0
61	VREF							
62	AVcc							
63		P93						AN24
64		P92		TB2IN				

## 1.6 Pin Description

**Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages)**

Classification	Symbol	I/O Type	Function
Power Supply	VCC, VSS	I	Apply 2.7 to 5.5V to the VCC pin. Apply 0V to the VSS pin.
Analog Power Supply	AVCC AVSS	I	Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS.
Reset Input	RESET	I	The MCU is in a reset state when "L" is applied to the RESET pin
CNVSS	CNVSS	I	Connect the CNVSS pin to VSS.
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open. If XIN is not used (for external oscillator or external clock) connect XIN pin to VCC and leave XOUT open.
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XOUT.
Sub Clock Output	XOUT	O	
INT Interrupt Input	INT0 to INT5	I	Input pins for the INT interrupt. INT2 can be used for Timer A Z-phase function.
NMI Interrupt Input	NMI	I	Input pin for the NMI interrupt. NMI cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to NMI after setting it's direction register to "0" when the three-phase motor control is enabled.
Key Input Interrupt	KI0 to KI3	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
	ZP	I	Input pin for Z-phase
Timer B	TB0IN to TB2IN	I	Input pins for the timer B0 to B2
Three-phase Motor Control Timer Output	U, $\bar{U}$ , V, $\bar{V}$ , W, $\bar{W}$	O	Output pins for the three-phase motor control timer
	IDU, IDW, IDV, SD	I/O	Input and output pins for the three-phase motor control timer
Serial I/O	CTS0 to CTS2	I	Input pins for data transmission control
	RTS0 to RTS2	O	Output pins for data reception control
	CLK0 to CLK3	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD2	I	Inputs serial data
	TxD0 to TxD2	O	Outputs serial data
	CLKS1	O	Output pin for transfer clock
I <sup>2</sup> C Mode	SDA2	I/O	Inputs and outputs serial data
	SCL2		Inputs and outputs the transfer clock
Multi-master I <sup>2</sup> C bus	SDAMM	I/O	Inputs and outputs serial data
	SCLMM		Inputs and outputs the transfer clock
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter
A/D Converter	AN0 to AN7 AN00 to AN03 AN24	I	Analog input pins for the A/D converter
	ADTRG		Input pin for an external A/D trigger

I : Input    O : Output    I/O : Input and output

**Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages) (Continued)**

Classification	Symbol	I/O Type	Function
Timer S	INPC10 to INPC17	I	Input pins for the time measurement function
	OUTC10 to OUTC17	O	Output pins for the waveform generating function
I/O Ports	P00 to P03 P15 to P17 P20 to P27 P30 to P33 P60 to P67 P70 to P77 P80 to P87 P100 to P107	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units
	P90 to P93	I/O	I/O ports having equivalent functions to P0

I : Input    O : Output    I/O : Input and output

**Table 1.10 Pin Description (80-Pin and 85-Pin Packages only) (Continued)**

Classification	Symbol	I/O Type	Function
Serial I/O	CLK4	I/O	Inputs and outputs the transfer clock
	SIN4	I	Inputs serial data
	SOUT4	O	Outputs serial data
A/D Converter	AN04 to AN07 AN20 to AN23 AN25 to AN27	I	Analog input pins for the A/D converter
I/O Ports	P04 to P07 P10 to P14 P34 to P37	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units
	P95 to P97	I/O	I/O ports having equivalent functions to P0

I : Input    O : Output    I/O : Input and output

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The register bank is comprised of 7 registers (R0, R1, R2, R3, A0, A1 and FB) out of 13 CPU registers. Two sets of register banks are provided.

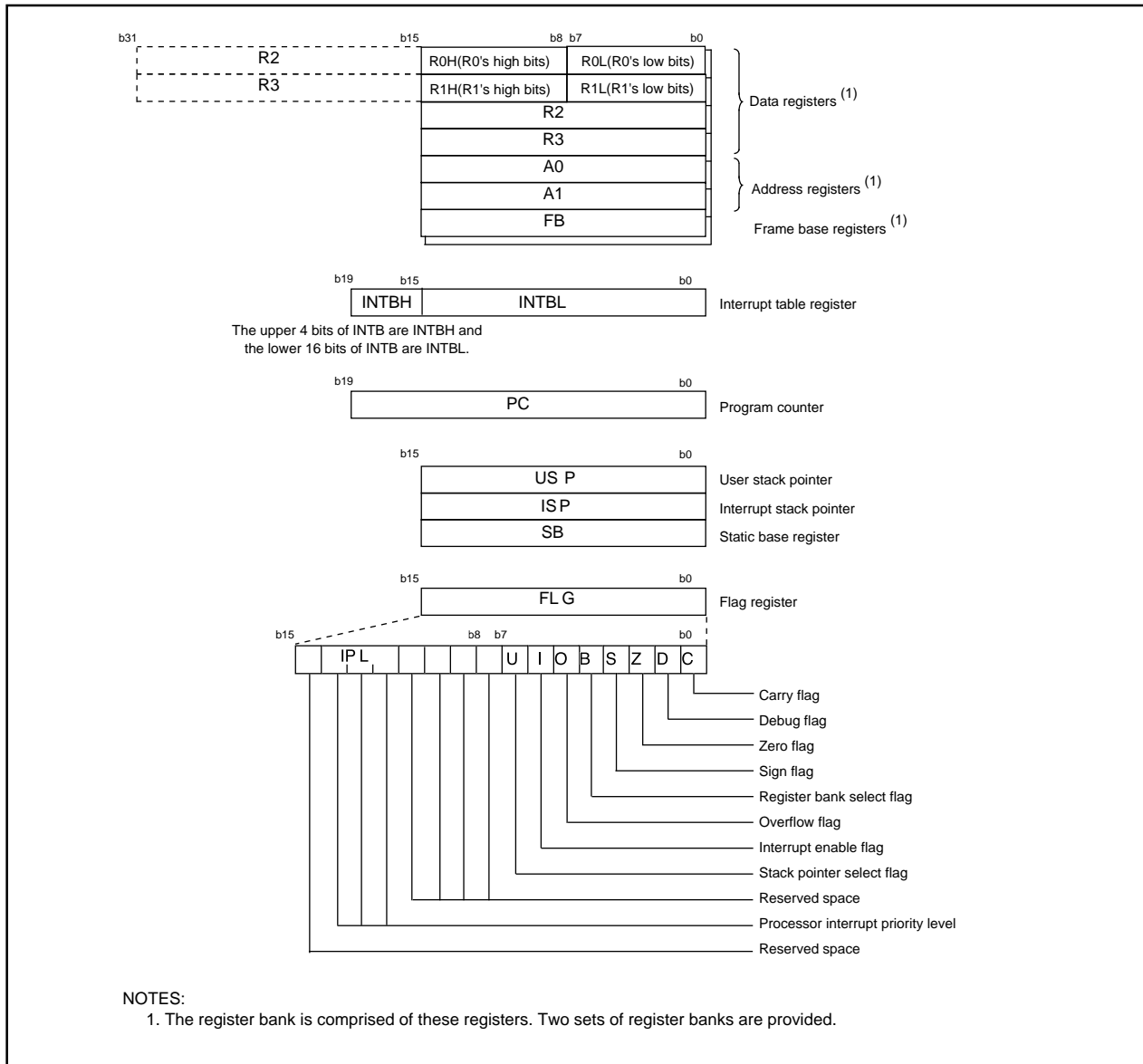


Figure 2.1 Central Processing Unit Register

### 2.1 Data Registers (R0, R1, R2 and R3)

The R0, R1, R2 and R3 registers are 16 bit registers for transfer and arithmetic/logic operations.

The R0 and R1 registers can be split into high-order bits(R0H, R1H) and low-order bits (R0L, R1L) to be used separately as 8-bit data registers. Conversely, R2 and R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R2.

### 2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0. In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

## 2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

### 2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

### 2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to 0.

### 2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

### 2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

### 2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0 ; register bank 1 is selected when this flag is 1.

### 2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

### 2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is cleared to 0 when the interrupt request is accepted.

### 2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is cleared to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

### 2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is indeterminate.

### 3. Memory

**Figure 3.1** is a memory map of the M16C/28 Group (M16C/28, M16C/28B). M16C/28 Group provides 1-Mbyte address space from addresses 00000<sub>16</sub> to FFFFF<sub>16</sub>. The internal ROM is allocated lower addresses beginning with address FFFFF<sub>16</sub>. For example, 64 Kbytes internal ROM is allocated addresses F0000<sub>16</sub> to FFFFF<sub>16</sub>.

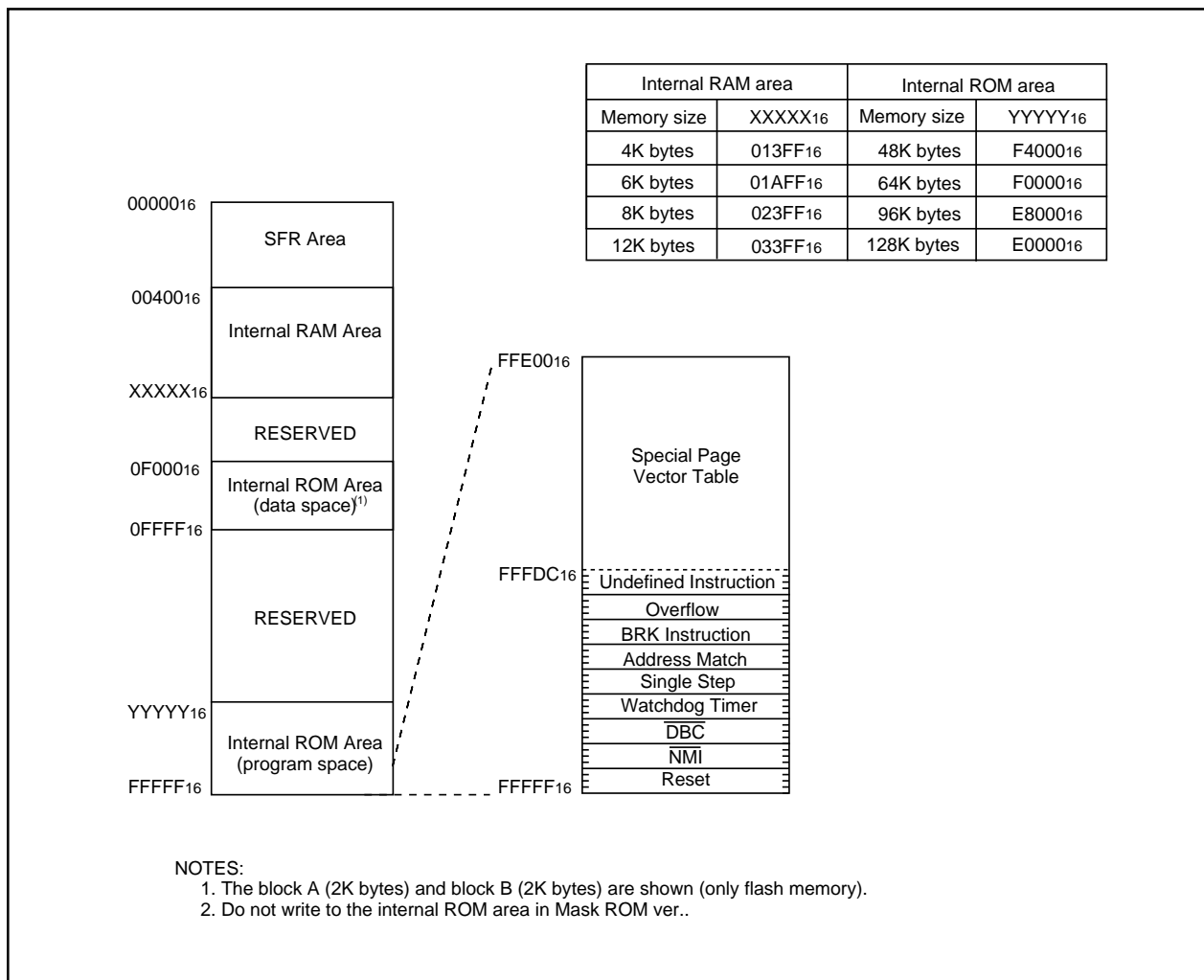
Two 2-Kbyte internal ROM areas, block A and block B, are available in the flash memory version. The blocks are allocated addresses F000<sub>16</sub> to FFFF<sub>16</sub>.

The fixed interrupt vector tables are allocated addresses FFFDC<sub>16</sub> to FFFFF<sub>16</sub>. It stores the starting address of each interrupt routine. See the section on interrupts for details.

The internal RAM is allocated higher addresses beginning with address 00400<sub>16</sub>. For example, 4-Kbytes internal RAM is allocated addresses 00400<sub>16</sub> to 013FF<sub>16</sub>. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, timers is allocated addresses 00000<sub>16</sub> to 003FF<sub>16</sub>. All blank spaces within SFR are reserved and cannot be accessed by users.

The special page vector table is allocated to the addresses FFE00<sub>16</sub> to FFFDB<sub>16</sub>. This vector is used by the JMPS or JSRS instruction. For details, refer to the **M16C/60 and M16C/20 Series Software Manual**.



**Figure 3.1 Memory Map**

## 4. Special Function Register (SFR)

SFR (Special Function Register) is the control register of peripheral functions. **Tables 4.1 to 4.7** list the SFR information.

**Table 4.1 SFR Information(1)(1)**

Address	Register	Symbol	After Reset
0000 <sub>16</sub>			
0001 <sub>16</sub>			
0002 <sub>16</sub>			
0003 <sub>16</sub>			
0004 <sub>16</sub>	Processor mode register 0	PM0	0016
0005 <sub>16</sub>	Processor mode register 1	PM1	000010002
0006 <sub>16</sub>	System clock control register 0	CM0	010010002
0007 <sub>16</sub>	System clock control register 1	CM1	001000002
0008 <sub>16</sub>			
0009 <sub>16</sub>	Address match interrupt enable register	AIER	XXXXXX002
000A <sub>16</sub>	Protect register	PRCR	XX0000002
000B <sub>16</sub>			
000C <sub>16</sub>	Oscillation stop detection register <sup>(2)</sup>	CM2	0X0000102
000D <sub>16</sub>			
000E <sub>16</sub>	Watchdog timer start register	WDTS	XX16
000F <sub>16</sub>	Watchdog timer control register	WDC	00XXXXXX2
0010 <sub>16</sub>	Address match interrupt register 0	RMAD0	0016
0011 <sub>16</sub>			0016
0012 <sub>16</sub>			X016
0013 <sub>16</sub>			
0014 <sub>16</sub>	Address match interrupt register 1	RMAD1	0016
0015 <sub>16</sub>			0016
0016 <sub>16</sub>			X016
0017 <sub>16</sub>			
0018 <sub>16</sub>			
0019 <sub>16</sub>	Voltage detection register 1 <sup>(3)</sup>	VCR1	000010002
001A <sub>16</sub>	Voltage detection register 2 <sup>(3)</sup>	VCR2	0016
001B <sub>16</sub>			
001C <sub>16</sub>	PLL control register 0	PLC0	0001X0102
001D <sub>16</sub>			
001E <sub>16</sub>	Processor mode register 2	PM2	XXX000002
001F <sub>16</sub>	Low voltage detection interrupt register	D4INT	0016
0020 <sub>16</sub>	DMA0 source pointer	SAR0	XX16
0021 <sub>16</sub>			XX16
0022 <sub>16</sub>			XX16
0023 <sub>16</sub>			
0024 <sub>16</sub>	DMA0 destination pointer	DAR0	XX16
0025 <sub>16</sub>			XX16
0026 <sub>16</sub>			XX16
0027 <sub>16</sub>			
0028 <sub>16</sub>	DMA0 transfer counter	TCR0	XX16
0029 <sub>16</sub>			XX16
002A <sub>16</sub>			
002B <sub>16</sub>			
002C <sub>16</sub>	DMA0 control register	DM0CON	00000X002
002D <sub>16</sub>			
002E <sub>16</sub>			
002F <sub>16</sub>			
0030 <sub>16</sub>	DMA1 source pointer	SAR1	XX16
0031 <sub>16</sub>			XX16
0032 <sub>16</sub>			XX16
0033 <sub>16</sub>			
0034 <sub>16</sub>	DMA1 destination pointer	DAR1	XX16
0035 <sub>16</sub>			XX16
0036 <sub>16</sub>			XX16
0037 <sub>16</sub>			
0038 <sub>16</sub>	DMA1 transfer counter	TCR1	XX16
0039 <sub>16</sub>			XX16
003A <sub>16</sub>			
003B <sub>16</sub>			
003C <sub>16</sub>	DMA1 control register	DM1CON	00000X002
003D <sub>16</sub>			
003E <sub>16</sub>			
003F <sub>16</sub>			

**NOTES:**

1. The blank spaces are reserved. No access is allowed.
2. The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
3. This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.

X : Undefined

Table 4.2 SFR Information(2)<sup>(1)</sup>

Address	Register	Symbol	After Reset
0040 <sub>16</sub>			
0041 <sub>16</sub>			
0042 <sub>16</sub>			
0043 <sub>16</sub>			
0044 <sub>16</sub>	INT3 interrupt control register	INT3IC	XX00X0002
0045 <sub>16</sub>	IC/OC 0 interrupt control register	ICOC0IC	XXXXX0002
0046 <sub>16</sub>	IC/OC 1 interrupt control register, I <sup>2</sup> C bus interface interrupt control register	ICOC1IC, IICIC	XXXXX0002
0047 <sub>16</sub>	IC/OC base timer interrupt control register, SCLSDA interrupt control register	BTIC, SCLDAIC	XXXXX0002
0048 <sub>16</sub>	SI/O4 interrupt control register, INT5 interrupt control register	S4IC, INT5IC	XX00X0002
0049 <sub>16</sub>	SI/O3 interrupt control register, INT4 interrupt control register	S3IC, INT4IC	XX00X0002
004A <sub>16</sub>	UART2 Bus collision detection interrupt control register	BCNIC	XXXXX0002
004B <sub>16</sub>	DMA0 interrupt control register	DM0IC	XXXXX0002
004C <sub>16</sub>	DMA1 interrupt control register	DM1IC	XXXXX0002
004D <sub>16</sub>	Key input interrupt control register	KUPIC	XXXXX0002
004E <sub>16</sub>	A/D conversion interrupt control register	ADIC	XXXXX0002
004F <sub>16</sub>	UART2 transmit interrupt control register	S2TIC	XXXXX0002
0050 <sub>16</sub>	UART2 receive interrupt control register	S2RIC	XXXXX0002
0051 <sub>16</sub>	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052 <sub>16</sub>	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053 <sub>16</sub>	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054 <sub>16</sub>	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055 <sub>16</sub>	Timer A0 interrupt control register	TA0IC	XXXXX0002
0056 <sub>16</sub>	Timer A1 interrupt control register	TA1IC	XXXXX0002
0057 <sub>16</sub>	Timer A2 interrupt control register	TA2IC	XXXXX0002
0058 <sub>16</sub>	Timer A3 interrupt control register	TA3IC	XXXXX0002
0059 <sub>16</sub>	Timer A4 interrupt control register	TA4IC	XXXXX0002
005A <sub>16</sub>	Timer B0 interrupt control register	TB0IC	XXXXX0002
005B <sub>16</sub>	Timer B1 interrupt control register	TB1IC	XXXXX0002
005C <sub>16</sub>	Timer B2 interrupt control register	TB2IC	XXXXX0002
005D <sub>16</sub>	INT0 interrupt control register	INT0IC	XX00X0002
005E <sub>16</sub>	INT1 interrupt control register	INT1IC	XX00X0002
005F <sub>16</sub>	INT2 interrupt control register	INT2IC	XX00X0002
0060 <sub>16</sub>			
0061 <sub>16</sub>			
0062 <sub>16</sub>			
0063 <sub>16</sub>			
0064 <sub>16</sub>			
0065 <sub>16</sub>			
0066 <sub>16</sub>			
0067 <sub>16</sub>			
0068 <sub>16</sub>			
0069 <sub>16</sub>			
006A <sub>16</sub>			
006B <sub>16</sub>			
006C <sub>16</sub>			
006D <sub>16</sub>			
006E <sub>16</sub>			
006F <sub>16</sub>			
0070 <sub>16</sub>			
0071 <sub>16</sub>			
0072 <sub>16</sub>			
0073 <sub>16</sub>			
0074 <sub>16</sub>			
0075 <sub>16</sub>			
0076 <sub>16</sub>			
0077 <sub>16</sub>			
0078 <sub>16</sub>			
0079 <sub>16</sub>			
007A <sub>16</sub>			
007B <sub>16</sub>			
007C <sub>16</sub>			
007D <sub>16</sub>			
007E <sub>16</sub>			
007F <sub>16</sub>			

Note 1: The blank spaces are reserved. No access is allowed.

X : Undefined

**Table 4.3 SFR Information(3)<sup>(1)</sup>**

Address	Register	Symbol	After Reset
01B0 <sub>16</sub>			
01B1 <sub>16</sub>			
01B2 <sub>16</sub>			
01B3 <sub>16</sub>	Flash memory control register 4 <sup>(2)</sup>	FMR4	01000002
01B4 <sub>16</sub>			
01B5 <sub>16</sub>	Flash memory control register 1 <sup>(2)</sup>	FMR1	000XX0X2
01B6 <sub>16</sub>			
01B7 <sub>16</sub>	Flash memory control register 0 <sup>(2)</sup>	FMR0	00000012
01B8 <sub>16</sub>			
01B9 <sub>16</sub>			
0210 <sub>16</sub>	Low-power Consumption Control 0	LPCC0	X0000012
0211 <sub>16</sub>			
0212 <sub>16</sub>			
0213 <sub>16</sub>			
0214 <sub>16</sub>			
0215 <sub>16</sub>			
0216 <sub>16</sub>			
0217 <sub>16</sub>			
0218 <sub>16</sub>			
0219 <sub>16</sub>			
0250 <sub>16</sub>			
0251 <sub>16</sub>			
0252 <sub>16</sub>			
0253 <sub>16</sub>			
0254 <sub>16</sub>			
0255 <sub>16</sub>			
0256 <sub>16</sub>			
0257 <sub>16</sub>			
0258 <sub>16</sub>			
0259 <sub>16</sub>			
025A <sub>16</sub>			
025B <sub>16</sub>			
025C <sub>16</sub>	On-chip oscillator control register	ROCR	X00001012
025D <sub>16</sub>	Pin assignment control register	PACR	0016
025E <sub>16</sub>	Peripheral clock select register	PCLKR	000000112
025F <sub>16</sub>	Low-power Consumption Control 1	LPCC1	0016
02E0 <sub>16</sub>	I <sup>2</sup> C0 data shift register	S00	XX16
02E1 <sub>16</sub>			
02E2 <sub>16</sub>	I <sup>2</sup> C0 address register	S0D0	0016
02E3 <sub>16</sub>	I <sup>2</sup> C0 control register 0	S1D0	0016
02E4 <sub>16</sub>	I <sup>2</sup> C0 clock control register	S20	0016
02E5 <sub>16</sub>	I <sup>2</sup> C0 start/stop condition control register	S2D0	000110102
02E6 <sub>16</sub>	I <sup>2</sup> C0 control register 1	S3D0	001100002
02E7 <sub>16</sub>	I <sup>2</sup> C0 control register 2	S4D0	0016
02E8 <sub>16</sub>	I <sup>2</sup> C0 status register	S10	0001000X2
02E9 <sub>16</sub>			
02EA <sub>16</sub>			
02FE <sub>16</sub>			
02FF <sub>16</sub>			

Note 1: The blank spaces are reserved. No access is allowed.

Note 2: This register is included in the flash memory version.

X : Undefined

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After Reset
0300 <sub>16</sub> 0301 <sub>16</sub>	TM, WG register 0	G1TM0, G1PO0	XX <sub>16</sub> XX <sub>16</sub>
0302 <sub>16</sub> 0303 <sub>16</sub>	TM, WG register 1	G1TM1, G1PO1	XX <sub>16</sub> XX <sub>16</sub>
0304 <sub>16</sub> 0305 <sub>16</sub>	TM, WG register 2	G1TM2, G1PO2	XX <sub>16</sub> XX <sub>16</sub>
0306 <sub>16</sub> 0307 <sub>16</sub>	TM, WG register 3	G1TM3, G1PO3	XX <sub>16</sub> XX <sub>16</sub>
0308 <sub>16</sub> 0309 <sub>16</sub>	TM, WG register 4	G1TM4, G1PO4	XX <sub>16</sub> XX <sub>16</sub>
030A <sub>16</sub> 030B <sub>16</sub>	TM, WG register 5	G1TM5, G1PO5	XX <sub>16</sub> XX <sub>16</sub>
030C <sub>16</sub> 030D <sub>16</sub>	TM, WG register 6	G1TM6, G1PO6	XX <sub>16</sub> XX <sub>16</sub>
030E <sub>16</sub> 030F <sub>16</sub>	TM, WG register 7	G1TM7, G1PO7	XX <sub>16</sub> XX <sub>16</sub>
0310 <sub>16</sub>	WG control register 0	G1POCR0	0X00XX00 <sub>2</sub>
0311 <sub>16</sub>	WG control register 1	G1POCR1	0X00XX00 <sub>2</sub>
0312 <sub>16</sub>	WG control register 2	G1POCR2	0X00XX00 <sub>2</sub>
0313 <sub>16</sub>	WG control register 3	G1POCR3	0X00XX00 <sub>2</sub>
0314 <sub>16</sub>	WG control register 4	G1POCR4	0X00XX00 <sub>2</sub>
0315 <sub>16</sub>	WG control register 5	G1POCR5	0X00XX00 <sub>2</sub>
0316 <sub>16</sub>	WG control register 6	G1POCR6	0X00XX00 <sub>2</sub>
0317 <sub>16</sub>	WG control register 7	G1POCR7	0X00XX00 <sub>2</sub>
0318 <sub>16</sub>	TM control register 0	G1TMCR0	00 <sub>16</sub>
0319 <sub>16</sub>	TM control register 1	G1TMCR1	00 <sub>16</sub>
031A <sub>16</sub>	TM control register 2	G1TMCR2	00 <sub>16</sub>
031B <sub>16</sub>	TM control register 3	G1TMCR3	00 <sub>16</sub>
031C <sub>16</sub>	TM control register 4	G1TMCR4	00 <sub>16</sub>
031D <sub>16</sub>	TM control register 5	G1TMCR5	00 <sub>16</sub>
031E <sub>16</sub>	TM control register 6	G1TMCR6	00 <sub>16</sub>
031F <sub>16</sub>	TM control register 7	G1TMCR7	00 <sub>16</sub>
0320 <sub>16</sub> 0321 <sub>16</sub>	Base timer register	G1BT	XX <sub>16</sub> XX <sub>16</sub>
0322 <sub>16</sub>	Base timer control register 0	G1BCR0	00 <sub>16</sub>
0323 <sub>16</sub>	Base timer control register 1	G1BCR1	00 <sub>16</sub>
0324 <sub>16</sub>	TM prescale register 6	G1TPR6	00 <sub>16</sub>
0325 <sub>16</sub>	TM prescale register 7	G1TPR7	00 <sub>16</sub>
0326 <sub>16</sub>	Function enable register	G1FE	00 <sub>16</sub>
0327 <sub>16</sub>	Function select register	G1FS	00 <sub>16</sub>
0328 <sub>16</sub> 0329 <sub>16</sub>	Base timer reset register	G1BTRR	XX <sub>16</sub> XX <sub>16</sub>
032A <sub>16</sub> 032B <sub>16</sub> 032C <sub>16</sub> 032D <sub>16</sub> 032E <sub>16</sub> 032F <sub>16</sub>	Divider register	G1DV	00 <sub>16</sub>
0330 <sub>16</sub>	Interrupt request register	G1IR	XX <sub>16</sub>
0331 <sub>16</sub>	Interrupt enable register 0	G1IE0	00 <sub>16</sub>
0332 <sub>16</sub>	Interrupt enable register 1	G1IE1	00 <sub>16</sub>
0333 <sub>16</sub>			
0334 <sub>16</sub>			
0335 <sub>16</sub>			
0336 <sub>16</sub>			
0337 <sub>16</sub>			
0338 <sub>16</sub>			
0339 <sub>16</sub>			
033A <sub>16</sub>			
033B <sub>16</sub>			
033C <sub>16</sub>			
033D <sub>16</sub>			
033E <sub>16</sub>	NMI digital debounce register	NDDR	FF <sub>16</sub>
033F <sub>16</sub>	P17 digital debounce register	P17DDR	FF <sub>16</sub>

Note 1: The blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.5 SFR Information(5)(1)

Address	Register	Symbol	After Reset
0340 <sub>16</sub>			
0341 <sub>16</sub>			
0342 <sub>16</sub>	Timer A1-1 register	TA11	XX <sub>16</sub>
0343 <sub>16</sub>			XX <sub>16</sub>
0344 <sub>16</sub>	Timer A2-1 register	TA21	XX <sub>16</sub>
0345 <sub>16</sub>			XX <sub>16</sub>
0346 <sub>16</sub>	Timer A4-1 register	TA41	XX <sub>16</sub>
0347 <sub>16</sub>			XX <sub>16</sub>
0348 <sub>16</sub>	Three-phase PWM control register 0	INVC0	00 <sub>16</sub>
0349 <sub>16</sub>	Three-phase PWM control register 1	INVC1	00 <sub>16</sub>
034A <sub>16</sub>	Three-phase output buffer register 0	IDB0	00111111 <sub>2</sub>
034B <sub>16</sub>	Three-phase output buffer register 1	IDB1	00111111 <sub>2</sub>
034C <sub>16</sub>	Dead time timer	DTT	XX <sub>16</sub>
034D <sub>16</sub>	Timer B2 interrupt occurrence frequency set counter	ICTB2	XX <sub>16</sub>
034E <sub>16</sub>	Position-data-retain function control register	PDRF	XXXX0000 <sub>2</sub>
034F <sub>16</sub>			
0350 <sub>16</sub>			
0351 <sub>16</sub>			
0352 <sub>16</sub>			
0353 <sub>16</sub>			
0354 <sub>16</sub>			
0355 <sub>16</sub>			
0356 <sub>16</sub>			
0357 <sub>16</sub>			
0358 <sub>16</sub>			
0359 <sub>16</sub>			
035A <sub>16</sub>			
035B <sub>16</sub>			
035C <sub>16</sub>			
035D <sub>16</sub>			
035E <sub>16</sub>	Interrupt request cause select register 2	IFSR2A	00XXXXX0 <sub>2</sub> (2)
035F <sub>16</sub>	Interrupt request cause select register	IFSR	00 <sub>16</sub>
0360 <sub>16</sub>	SI/O3 transmit/receive register	S3TRR	XX <sub>16</sub>
0361 <sub>16</sub>			
0362 <sub>16</sub>	SI/O3 control register	S3C	01000000 <sub>2</sub>
0363 <sub>16</sub>	SI/O3 bit rate generator	S3BRG	XX <sub>16</sub>
0364 <sub>16</sub>	SI/O4 transmit/receive register	S4TRR	XX <sub>16</sub>
0365 <sub>16</sub>			
0366 <sub>16</sub>	SI/O4 control register	S4C	01000000 <sub>2</sub>
0367 <sub>16</sub>	SI/O4 bit rate generator	S4BRG	XX <sub>16</sub>
0368 <sub>16</sub>			
0369 <sub>16</sub>			
036A <sub>16</sub>			
036B <sub>16</sub>			
036C <sub>16</sub>			
036D <sub>16</sub>			
036E <sub>16</sub>			
036F <sub>16</sub>			
0370 <sub>16</sub>			
0371 <sub>16</sub>			
0372 <sub>16</sub>			
0373 <sub>16</sub>			
0374 <sub>16</sub>	UART2 special mode register 4	U2SMR4	00 <sub>16</sub>
0375 <sub>16</sub>	UART2 special mode register 3	U2SMR3	000X0X0X <sub>2</sub>
0376 <sub>16</sub>	UART2 special mode register 2	U2SMR2	X0000000 <sub>2</sub>
0377 <sub>16</sub>	UART2 special mode register	U2SMR	X0000000 <sub>2</sub>
0378 <sub>16</sub>	UART2 transmit/receive mode register	U2MR	00 <sub>16</sub>
0379 <sub>16</sub>	UART2 bit rate generator	U2BRG	XX <sub>16</sub>
037A <sub>16</sub>	UART2 transmit buffer register	U2TB	XX <sub>16</sub>
037B <sub>16</sub>			XX <sub>16</sub>
037C <sub>16</sub>	UART2 transmit/receive control register 0	U2C0	00001000 <sub>2</sub>
037D <sub>16</sub>	UART2 transmit/receive control register 1	U2C1	00000010 <sub>2</sub>
037E <sub>16</sub>	UART2 receive buffer register	U2RB	XX <sub>16</sub>
037F <sub>16</sub>			XX <sub>16</sub>

Note 1: The blank spaces are reserved. No access is allowed.

Note 2: Write 1 to bit 0 after reset.

X : Undefined

Table 4.6 SFR Information(6)<sup>(1)</sup>

Address	Register	Symbol	After Reset
0380 <sub>16</sub>	Count start flag	TABSR	0016
0381 <sub>16</sub>	Clock prescaler reset flag	CPSRF	0XXXXXX2
0382 <sub>16</sub>	One-shot start flag	ONSF	0016
0383 <sub>16</sub>	Trigger select register	TRGSR	0016
0384 <sub>16</sub>	Up-down flag	UDF	0016
0385 <sub>16</sub>			
0386 <sub>16</sub> 0387 <sub>16</sub>	Timer A0 register	TA0	XX16 XX16
0388 <sub>16</sub> 0389 <sub>16</sub>	Timer A1 register	TA1	XX16 XX16
038A <sub>16</sub> 038B <sub>16</sub>	Timer A2 register	TA2	XX16 XX16
038C <sub>16</sub> 038D <sub>16</sub>	Timer A3 register	TA3	XX16 XX16
038E <sub>16</sub> 038F <sub>16</sub>	Timer A4 register	TA4	XX16 XX16
0390 <sub>16</sub> 0391 <sub>16</sub>	Timer B0 register	TB0	XX16 XX16
0392 <sub>16</sub> 0393 <sub>16</sub>	Timer B1 register	TB1	XX16 XX16
0394 <sub>16</sub> 0395 <sub>16</sub>	Timer B2 register	TB2	XX16 XX16
0396 <sub>16</sub>	Timer A0 mode register	TA0MR	0016
0397 <sub>16</sub>	Timer A1 mode register	TA1MR	0016
0398 <sub>16</sub>	Timer A2 mode register	TA2MR	0016
0399 <sub>16</sub>	Timer A3 mode register	TA3MR	0016
039A <sub>16</sub>	Timer A4 mode register	TA4MR	0016
039B <sub>16</sub>	Timer B0 mode register	TB0MR	00XX00002
039C <sub>16</sub>	Timer B1 mode register	TB1MR	00XX00002
039D <sub>16</sub>	Timer B2 mode register	TB2MR	00XX00002
039E <sub>16</sub>	Timer B2 special mode register	TB2SC	X00000002
039F <sub>16</sub>			
03A0 <sub>16</sub>	UART0 transmit/receive mode register	U0MR	0016
03A1 <sub>16</sub>	UART0 bit rate generator	U0BRG	XX16
03A2 <sub>16</sub> 03A3 <sub>16</sub>	UART0 transmit buffer register	U0TB	XX16 XX16
03A4 <sub>16</sub>	UART0 transmit/receive control register 0	U0C0	000010002
03A5 <sub>16</sub>	UART0 transmit/receive control register 1	U0C1	000000102
03A6 <sub>16</sub> 03A7 <sub>16</sub>	UART0 receive buffer register	U0RB	XX16 XX16
03A8 <sub>16</sub>	UART1 transmit/receive mode register	U1MR	0016
03A9 <sub>16</sub>	UART1 bit rate generator	U1BRG	XX16
03AA <sub>16</sub> 03AB <sub>16</sub>	UART1 transmit buffer register	U1TB	XX16 XX16
03AC <sub>16</sub>	UART1 transmit/receive control register 0	U1C0	000010002
03AD <sub>16</sub>	UART1 transmit/receive control register 1	U1C1	000000102
03AE <sub>16</sub> 03AF <sub>16</sub>	UART1 receive buffer register	U1RB	XX16 XX16
03B0 <sub>16</sub>	UART transmit/receive control register 2	UCON	X00000002
03B1 <sub>16</sub>			
03B2 <sub>16</sub>			
03B3 <sub>16</sub>			
03B4 <sub>16</sub>			
03B5 <sub>16</sub>			
03B6 <sub>16</sub>			
03B7 <sub>16</sub>			
03B8 <sub>16</sub> 03B9 <sub>16</sub>	DMA0 request cause select register	DM0SL	0016
03BA <sub>16</sub> 03BB <sub>16</sub>	DMA1 request cause select register	DM1SL	0016
03BC <sub>16</sub>			
03BD <sub>16</sub>			
03BE <sub>16</sub>			
03BF <sub>16</sub>			

Note 1: The blank spaces are reserved. No access is allowed.

X : Undefined

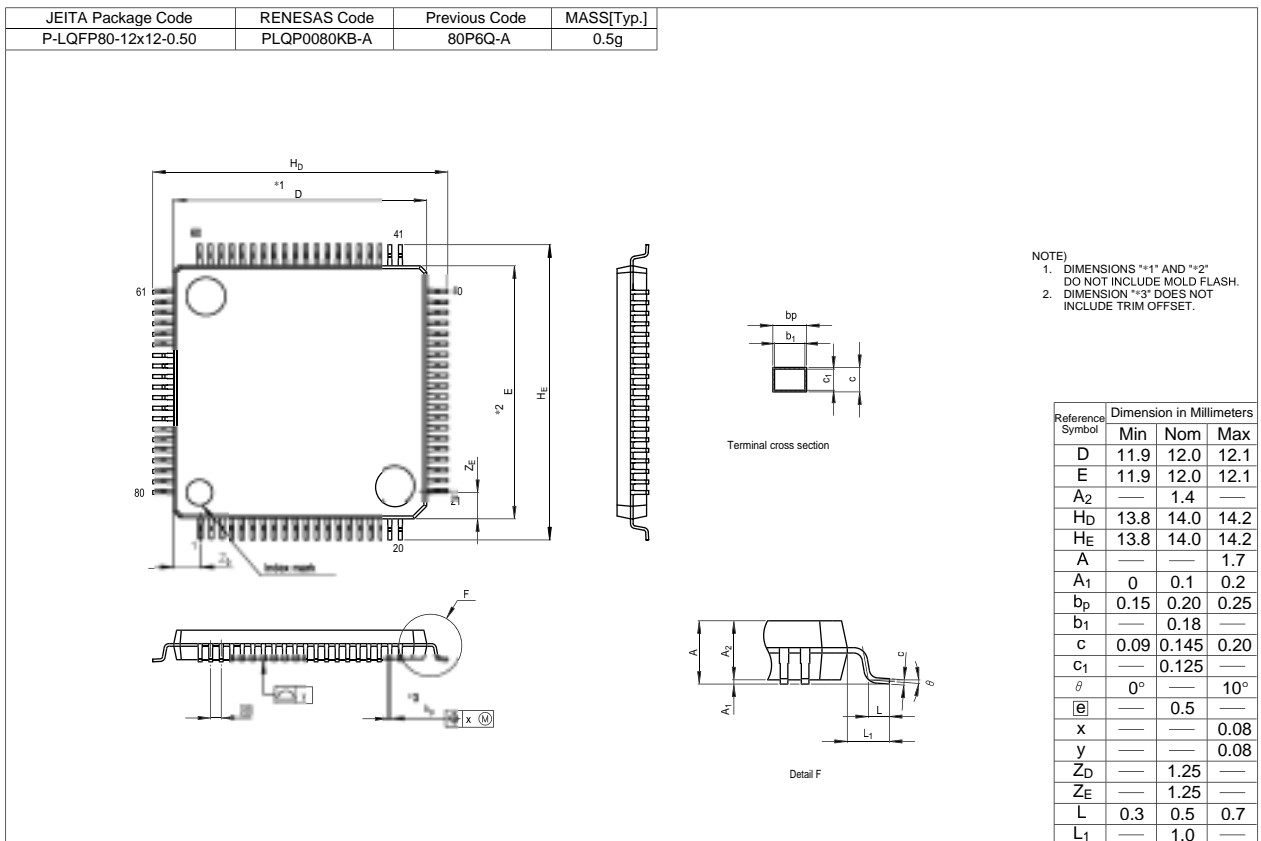
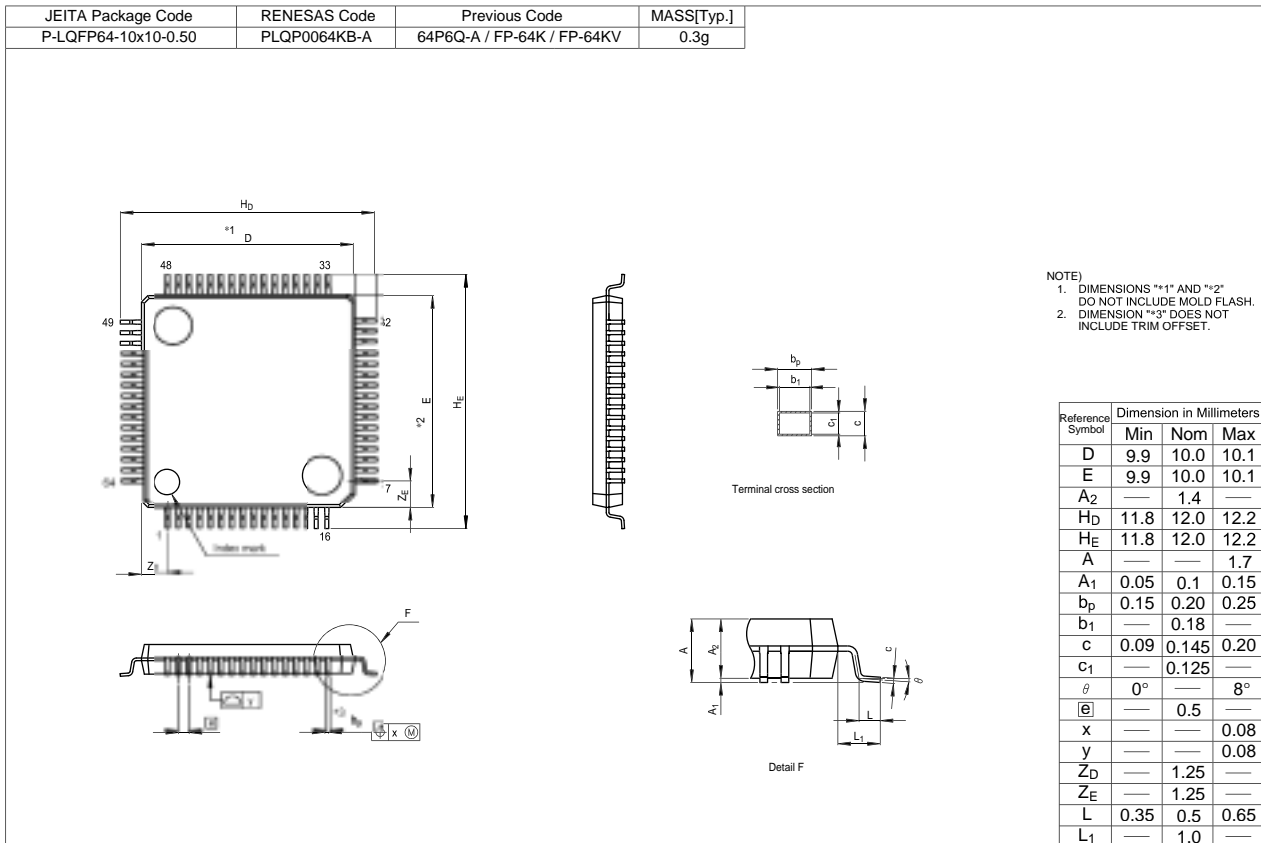
Table 4.7 SFR Information(7)(1)

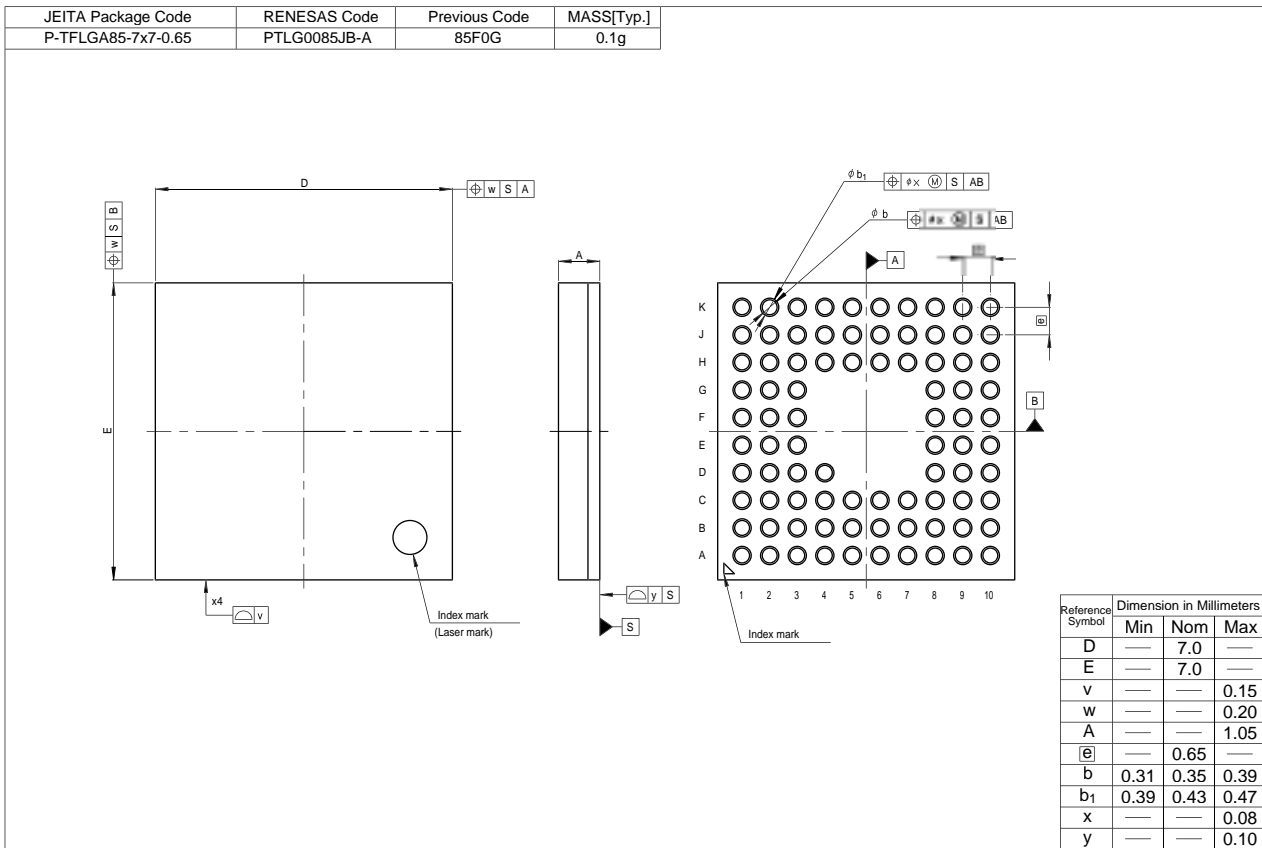
Address	Register	Symbol	After Reset
03C0 <sub>16</sub> 03C1 <sub>16</sub>	A/D register 0	AD0	XX <sub>16</sub> XX <sub>16</sub>
03C2 <sub>16</sub> 03C3 <sub>16</sub>	A/D register 1	AD1	XX <sub>16</sub> XX <sub>16</sub>
03C4 <sub>16</sub> 03C5 <sub>16</sub>	A/D register 2	AD2	XX <sub>16</sub> XX <sub>16</sub>
03C6 <sub>16</sub> 03C7 <sub>16</sub>	A/D register 3	AD3	XX <sub>16</sub> XX <sub>16</sub>
03C8 <sub>16</sub> 03C9 <sub>16</sub>	A/D register 4	AD4	XX <sub>16</sub> XX <sub>16</sub>
03CA <sub>16</sub> 03CB <sub>16</sub>	A/D register 5	AD5	XX <sub>16</sub> XX <sub>16</sub>
03CC <sub>16</sub> 03CD <sub>16</sub>	A/D register 6	AD6	XX <sub>16</sub> XX <sub>16</sub>
03CE <sub>16</sub> 03CF <sub>16</sub>	A/D register 7	AD7	XX <sub>16</sub> XX <sub>16</sub>
03D0 <sub>16</sub> 03D1 <sub>16</sub>			
03D2 <sub>16</sub>	A/D trigger control register	ADTRGCON	00 <sub>16</sub>
03D3 <sub>16</sub>	A/D convert status register 0	ADSTAT0	00000X00 <sub>2</sub>
03D4 <sub>16</sub> 03D5 <sub>16</sub>	A/D control register 2	ADCON2	00 <sub>16</sub>
03D6 <sub>16</sub>	A/D control register 0	ADCON0	00000XXX <sub>2</sub>
03D7 <sub>16</sub> 03D8 <sub>16</sub>	A/D control register 1	ADCON1	00 <sub>16</sub>
03D9 <sub>16</sub> 03DA <sub>16</sub>			
03DB <sub>16</sub> 03DC <sub>16</sub>			
03DD <sub>16</sub> 03DE <sub>16</sub>			
03DF <sub>16</sub>			
03E0 <sub>16</sub>	Port P0 register	P0	XX <sub>16</sub>
03E1 <sub>16</sub>	Port P1 register	P1	XX <sub>16</sub>
03E2 <sub>16</sub>	Port P0 direction register	PD0	00 <sub>16</sub>
03E3 <sub>16</sub>	Port P1 direction register	PD1	00 <sub>16</sub>
03E4 <sub>16</sub>	Port P2 register	P2	XX <sub>16</sub>
03E5 <sub>16</sub>	Port P3 register	P3	XX <sub>16</sub>
03E6 <sub>16</sub>	Port P2 direction register	PD2	00 <sub>16</sub>
03E7 <sub>16</sub>	Port P3 direction register	PD3	00 <sub>16</sub>
03E8 <sub>16</sub> 03E9 <sub>16</sub>			
03EA <sub>16</sub> 03EB <sub>16</sub>			
03EC <sub>16</sub>	Port P6 register	P6	XX <sub>16</sub>
03ED <sub>16</sub>	Port P7 register	P7	XX <sub>16</sub>
03EE <sub>16</sub>	Port P6 direction register	PD6	00 <sub>16</sub>
03EF <sub>16</sub>	Port P7 direction register	PD7	00 <sub>16</sub>
03F0 <sub>16</sub>	Port P8 register	P8	XX <sub>16</sub>
03F1 <sub>16</sub>	Port P9 register	P9	XX <sub>16</sub>
03F2 <sub>16</sub>	Port P8 direction register	PD8	00 <sub>16</sub>
03F3 <sub>16</sub>	Port P9 direction register	PD9	000X0000 <sub>2</sub>
03F4 <sub>16</sub> 03F5 <sub>16</sub>	Port P10 register	P10	XX <sub>16</sub>
03F6 <sub>16</sub>	Port P10 direction register	PD10	00 <sub>16</sub>
03F7 <sub>16</sub> 03F8 <sub>16</sub>			
03F9 <sub>16</sub> 03FA <sub>16</sub>			
03FB <sub>16</sub>			
03FC <sub>16</sub>	Pull-up control register 0	PUR0	00 <sub>16</sub>
03FD <sub>16</sub>	Pull-up control register 1	PUR1	00 <sub>16</sub>
03FE <sub>16</sub>	Pull-up control register 2	PUR2	00 <sub>16</sub>
03FF <sub>16</sub>	Port control register	PCR	00 <sub>16</sub>

Note 1: The blank spaces are reserved. No access is allowed.

X : Undefined

# Appendix 1. Package Dimensions





<b>REVISION HISTORY</b>	M16C/28 Group (M16C/28, M16C/28B) Shortsheet
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Rev.	Date	Description	
		Page	Summary
0.50	09/15/06	-	First edition

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