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April 1st, 2010
Renesas Electronics Corporation

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1. Overview

The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) is a single-chip control MCU, fabricated using high-performance silicon gate CMOS technology, embedding the M16C/60 Series CPU core. The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) is housed in 42-pin and 48-pin plastic molded packages. With a 1M byte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed. The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) has a multiplier and DMAC adequate for office automation, communication devices and industrial equipment, and other high-speed processing applications.

1.1 Applications

Audio, cameras, office/communications/portable/ equipment, air-conditioning equipment, home appliances, etc.

1.2 Performance Outline

Table 1.1 and **1.2** outline performance overview of the M16C/26A Group (M16C/26A, M16C/26B, M16C/26T).

Table 1.1. M16C/26A Group(M16C/26A, M16C/26B, M16C/26T) Performance (48-Pin Package)

Item		Specification
CPU	Basic instructions	91 instructions
	Minimum instruction execution time	41.7 ns (f(BCLK) = 24MHz ⁽⁴⁾ , Vcc = 4.2 to 5.5 V) (M16C/26B)
		50 ns (f(BCLK) = 20MHz, Vcc = 3.0 to 5.5 V) (M16C/26A, M16C/26B, M16C/26T(T-ver.))
		100 ns (f(BCLK) = 10MHz, Vcc = 2.7 to 5.5 V) (M16C/26A, M16C/26B)
		50 ns (f(BCLK) = 20MHz, Vcc = 4.2 to 5.5 V -40 to 105°C) (M16C/26T(V-ver.))
		62.5 ns (f(BCLK) = 16MHz, Vcc = 4.2 to 5.5 V -40 to 125°C) (M16C/26T(V-ver.))
Operating mode	Single-chip mode	
Address space	1 Mbyte	
Memory capacity	See 1.4 Product Information	
Peripheral Function	I/O ports	39 I/O pins
	Multifunction timers	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase motor control timer
	Serial I/O	2 channels (UART, clock synchronous serial I/O) 1 channel (UART, clock synchronous, I ² C bus ⁽¹⁾ , or IEBus ⁽²⁾)
	A/D converter	10 bit A/D Converter : 1 circuit, 12 channels
	DMAC	2 channels
	CRC calculation circuit	1 circuit (CRC-CCITT and CRC-16) with MSB/LSB selectable
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupts	20 internal and 8 external sources, 4 software sources, Interrupt priority level: 7
	Clock generation circuit	4 circuits Main clock oscillation circuit(*), Sub-clock oscillation circuit(*) On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor.
	Oscillation stop detection	Main clock oscillation stop, re-oscillation detection function
	Voltage detection circuit	On-chip (M16C/26A, M16C/26B), not on-chip (M16C/26T)
Electrical Characteristics	Power supply voltage	Vcc = 4.2 to 5.5 V (f(BCLK) = 24 MHz) ⁽⁴⁾ (M16C/26B)
		Vcc = 3.0 to 5.5 V (f(BCLK) = 20 MHz) (M16C/26A, M16C/26B)
		Vcc = 2.7 to 5.5 V (f(BCLK) = 10 MHz)
		Vcc = 3.0 to 5.5 V (M16C/26T(T-ver.))
	Vcc = 4.2 to 5.5 V (M16C/26T(V-ver.))	
Power consumption	16 mA (Vcc = 5 V, f(BCLK) = 20 MHz) 25 μ A (f(XCIN) = 32 KHz on RAM) 3 μ A (Vcc = 3 V, f(XCIN) = 32 KHz, in wait mode) 0.7 μ A (Vcc = 3 V, in stop mode)	
Flash Memory Version	Programming /erasure voltage	2.7 to 5.5 V (M16C/26A, M16C/26B) 3.0 to 5.5 V (M16C/26T(T-ver.)) 4.2 to 5.5 V (M16C/26T(V-ver.))
	Programming /erasure endurance	100 times (all area) or 1,000 times (block 0 to 3) / 10,000 times (block A, block B) ⁽³⁾
Operating Ambient Temperature		-20 to 85°C / -40 to 85°C ⁽³⁾ (M16C/26A, M16C/26B)
		-40 to 85°C (M16C/26T(T-ver.))
		-40 to 105°C / -40 to 125°C (M16C/26T(V-ver.))
Package	48-pin plastic molded QFP	

NOTES:

- I²C bus is a trademark of Koninklijke Philips Electronics N. V.
- IEBus is a trademark of NEC Electronics Corporation.
- See **Table 1.7 Product Code** for the program and erase endurance, and operating ambient temperature.
- The PLL frequency synthesizer is used to run the M16C/26B at f(BCLK) = 24 MHz.

Table 1.2. Performance outline of M16C/26A group (M16C/26A, M16C/26B) (42-pin device)

	Item	Performance
CPU	Basic instructions	91 instructions
	Minimum instruction execution time	41.7 ns (f(BCLK) = 24 MHz ⁽⁴⁾ , VCC = 4.2 to 5.5 V) (M16C/26B)
		50 ns (f(BCLK) = 20 MHz, VCC = 3.0 to 5.5 V) (M16C/26A, M16C/26B)
		100 ns (f(BCLK) = 10 MHz, VCC = 2.7 to 5.5 V) (M16C/26A, M16C/26B)
	Operation mode	Single-chip mode
Address space	1M byte	
Memory capacity	See 1.4 Product Information	
Peripheral function	Port	33 I/O pins
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 3 channels Three-phase motor control timer
	Serial I/O	1 channel (UART, clock synchronous serial I/O)
		1 channel (UART, clock synchronous, I ² C bus ⁽¹⁾ , or IEBus ⁽²⁾)
	A/D converter	10 bit A/D converter: 1 circuit, 10 channels
	DMAC	2 channels
	CRC calculation circuit	1 circuits (CRC-CCITT and CRC-16) with MSB/LSB selectable
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	18 internal and 8 external sources, 4 software sources, Interrupt priority level: 7
	Clock generation circuit	4 circuits Main clock(*), Sub-clock(*) On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor.
Oscillation stop detection		Main clock oscillation stop, re-oscillation detection function
Voltage detection circuit	On-chip	
Electrical Characteristics	Supply voltage	VCC = 4.2 to 5.5 V (f(BCLK) = 24 MHz) ⁽⁴⁾ (M16C/26B)
		VCC = 3.0 to 5.5 V (f(BCLK) = 20 MHz) (M16C/26A, M16C/26B)
VCC = 2.7 to 5.5 V (f(BCLK) = 10 MHz)		
Power Consumption	16 mA (VCC = 5 V, f(BCLK) = 20 MHz)	
	25 μ A (f(XCIN) = 32 KHz on RAM)	
	3 μ A (VCC = 3 V, f(XCIN) = 32 KHz, in wait mode)	
	0.7 μ A (VCC = 3 V, in stop mode)	
Flash memory	Programming/erasure voltage	2.7 to 5.5 V
	Programming/erasure endurance	100 times (all area) or 1,000 times (block 0 to 3) / 10,000 times (block A, block B) ⁽³⁾
Operating Ambient Temperature		-20 to 85°C / -40 to 85°C ⁽³⁾
Package		42-pin plastic molded SSOP

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. See **Table 1.7 Product Code** for the program and erase endurance, and operating ambient temperature.
4. The PLL frequency synthesizer is used to run the M16C/26B at f(BCLK) = 24 MHz.

1.3 Block Diagram

Figure 1.1 and 1.2 show block diagrams of the M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) 48-pin package and 42-pin package.

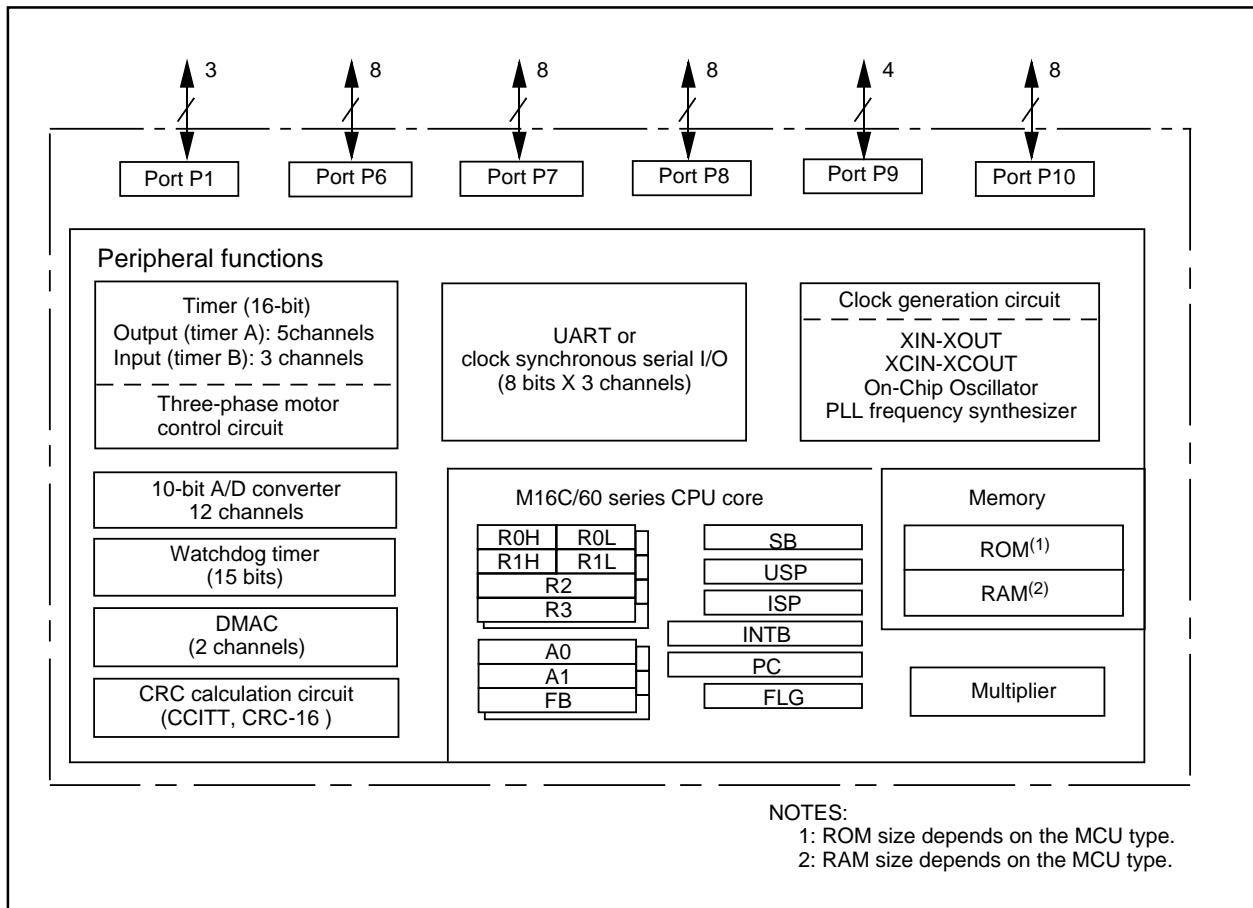


Figure 1.1 Block Diagram(48-pin Package)

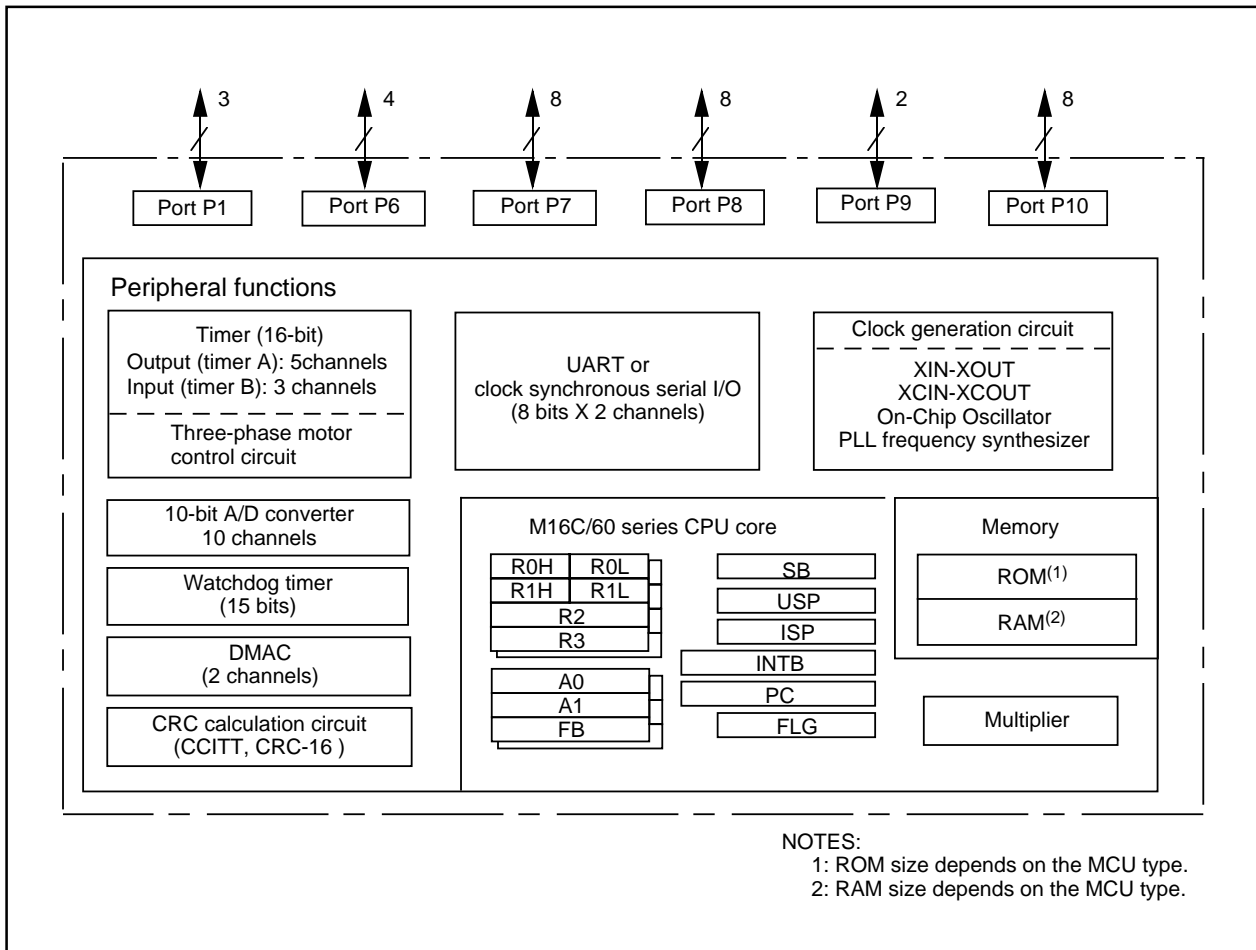


Figure 1.2 Block Diagram(42-pin Package)

1.4 Product List

Tables 1.3 to 1.6 lists product information, Figure 1.3 shows a product numbering system, Table 1.7 lists the product code, and Figure 1.4 shows the marking.

Table 1.3 M16C/26A

Current as of Jul., 2006

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30260F3AGP (N)	24K + 4K	1K	PLQP0048KB-A (48P6Q-A)	Flash memory	U3, U5, U7, U9
M30260F6AGP (N)	48K + 4K	2K			
M30260F8AGP (N)	64K + 4K	2K			
M30263F3AFP (N)	24K + 4K	1K	PRSP0042GA-B (42P2R)		U5, U9
M30263F6AFP (N)	48K + 4K	2K			
M30263F8AFP (N)	64K + 4K	2K			
M30260M3A-XXXGP (N)	24K	1K	PLQP0048KB-A (48P6Q-A)	Mask ROM	U3, U5
M30260M6A-XXXGP (N)	48K	2K			
M30260M8A-XXXGP (N)	64K	2K			
M30263M3A-XXXFP (N)	24K	1K	PRSP0042GA-B (42P2R)		U5
M30263M6A-XXXFP (N)	48K	2K			
M30263M8A-XXXFP (N)	64K	2K			

(N): New

Table 1.4 M16C/26B

Current as of Jul., 2006

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30260F8BGP (D)	64K + 4K	2K	PLQP0048KB-A (48P6Q-A)	Flash memory	U7
M30263F8BFP (D)	64K + 4K	2K	PRSP0042GA-B (42P2R)		U9

(D): Under development

Table 1.5 M16C/26T T-ver.

Current as of Jul., 2006

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30260F3TGP	24K + 4K	1K	PLQP0048KB-A (48P6Q-A)	Flash memory	U3, U7
M30260F6TGP	48K + 4K	2K			
M30260F8TGP	64K + 4K	2K			

NOTE:

1. Please contact Renesas Technology Corp. for details on Mask ROM version.

Table 1.6 M16C/26T V-ver.

Current as of Jul., 2006

Type Number	ROM Capacity	RAM Capacity	Package	Remarks	Product Code
M30260F3VGP	24K + 4K	1K	PLQP0048KB-A (48P6Q-A)	Flash memory	U3, U7
M30260F6VGP	48K + 4K	2K			
M30260F8VGP	64K + 4K	2K			

NOTE:

1. Please contact Renesas Technology Corp. for details on Mask ROM version.

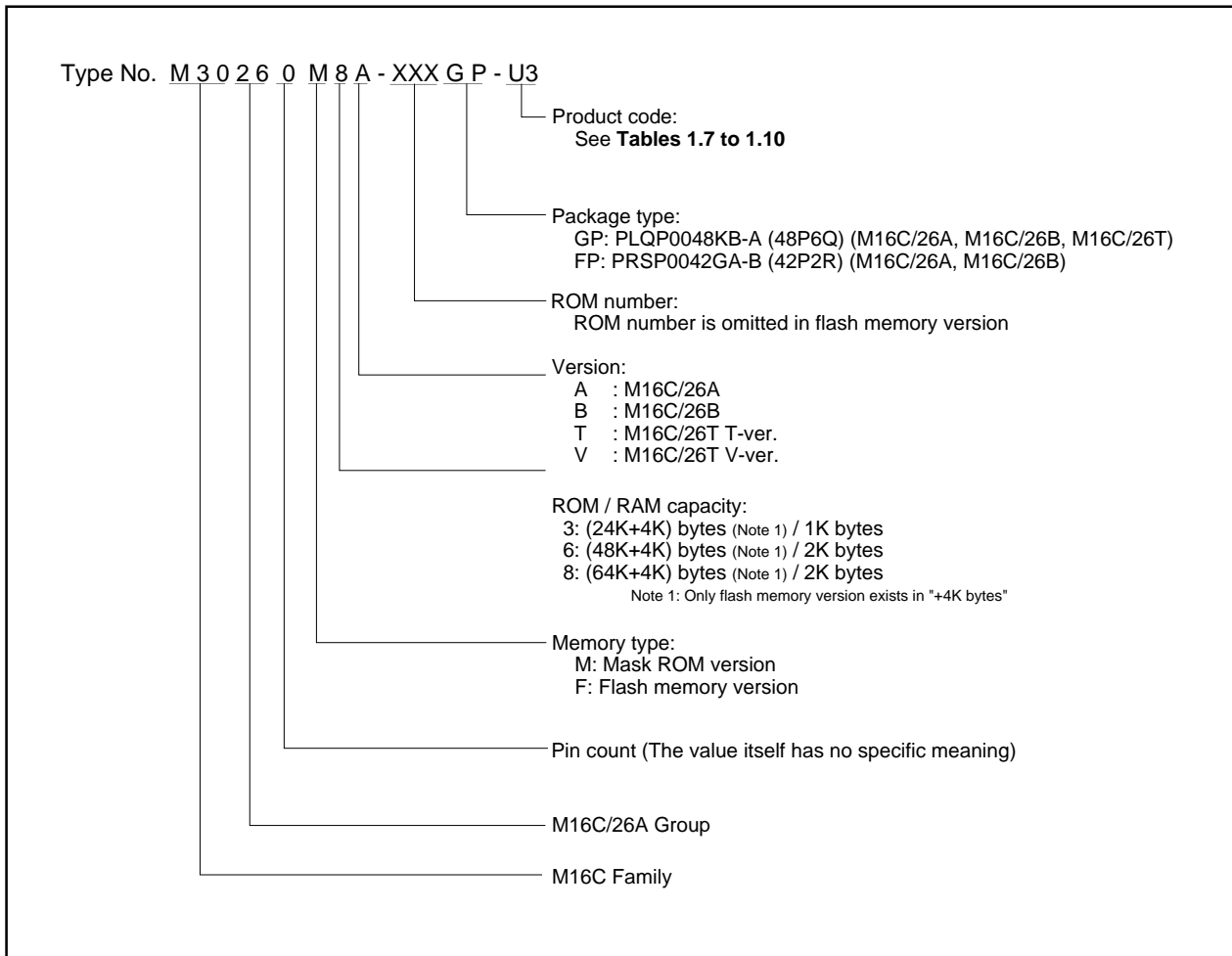


Figure 1.3 Product Numbering System

Table 1.7 Product Code (Flash Memory Version) - M16C/26A, M16C/26B

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead free	100	0 to 60°C	100	0 to 60°C	-40 to 85°C
U5						-20 to 85°C
U7		1,000		10,000	-40 to 85°C	-40 to 85°C
U9					-20 to 85°C	-20 to 85°C

Table 1.8 Product Code (Mask ROM Version - M16C/26A)

Product Code	Package	Operating Ambient Temperature
U3	Lead free	-40°C to 85°C
U5		-20°C to 85°C

NOTE:

- The lead contained products, D3, D5, D7, and D9 are put together with U3, U5, U7, and U9 respectively. Lead-free products can be mounted by both conventional Sn-Pb paste and Lead-free paste (Sn-Ag-Cu plating).

Table 1.9 Product Code (Flash Memory Version) - M16C/26T T-ver.

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Programming and erasure endurance	Temperature range	Programming and erasure endurance	Temperature range	
U3	Lead free	100	0°C to 60°C	100	-40°C to 85°C	-40°C to 85°C
U7		1,000		10,000		

Table 1.10 Product Code (Flash Memory Version) - M16C/26T V-ver.

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Programming and erasure endurance	Temperature range	Programming and erasure endurance	Temperature range	
U3	Lead free	100	0°C to 60°C	100	-40°C to 125°C	-40°C to 125°C
U7		1,000		10,000		

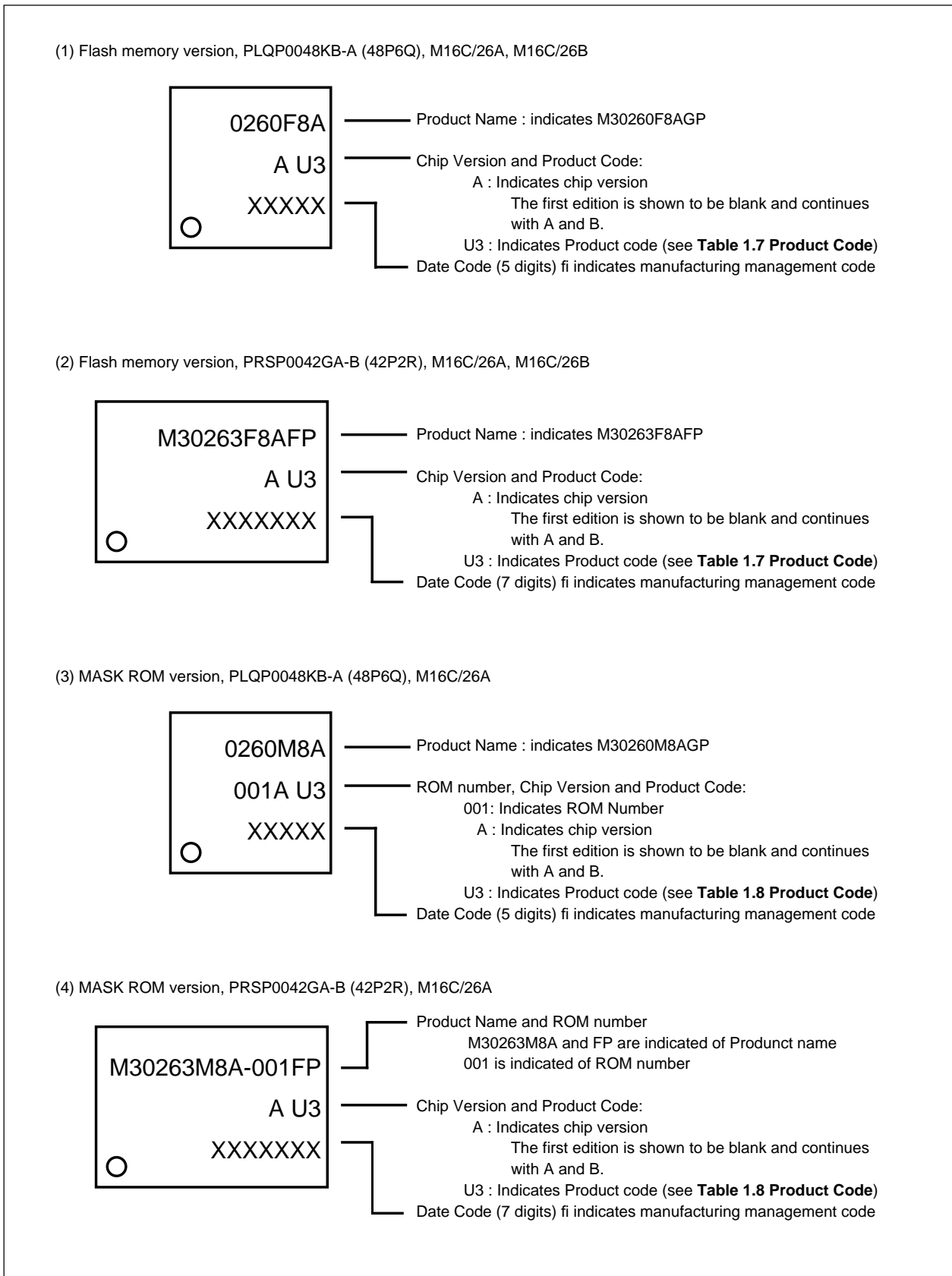


Figure 1.4 Marking Diagram (M16C/26A , M16C/26B)

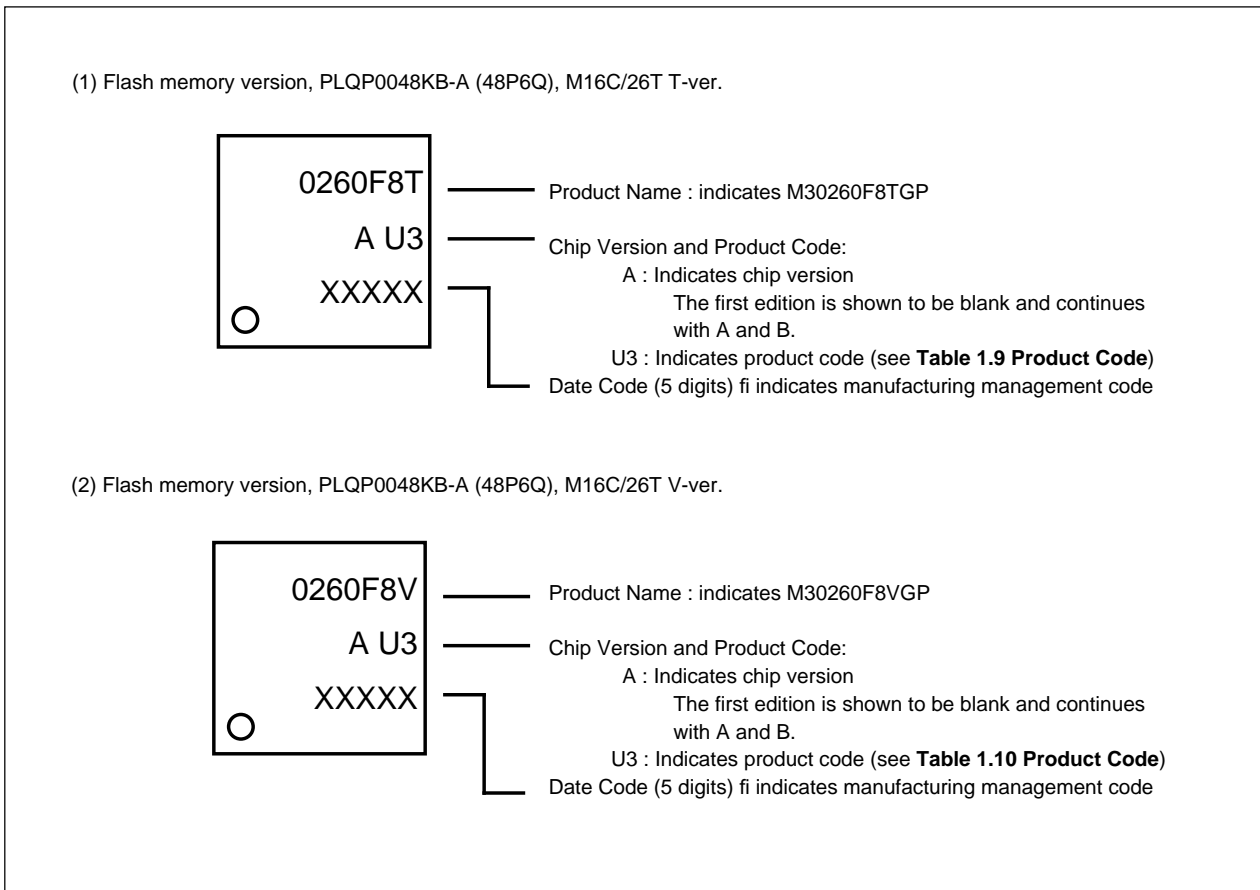


Figure 1.5 Marking Diagram (M16C/26T)

1.5 Pin Assignments

Figures 1.6 and 1.7 show the Pin Assignments (top view).

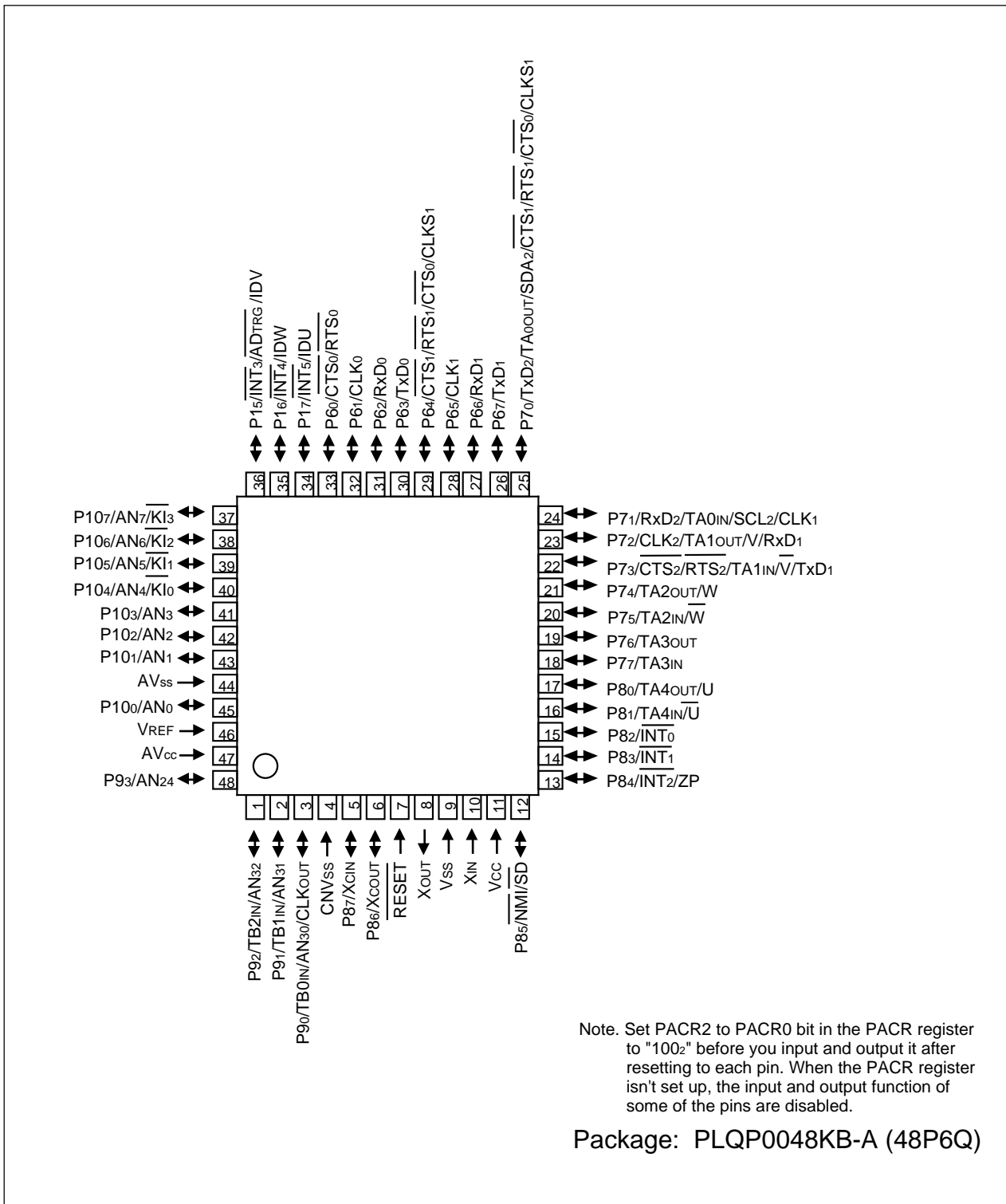


Figure 1.6 Pin Assignment for 48-Pin Package (Top View)

Table 1.11 Pin Characteristics for 48-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin
1		P92		TB2IN		AN32
2		P91		TB1IN		AN31
3		P90		TB0IN	CLKOUT	AN30
4	CNVss					
5	XCIN	P87				
6	XcOUT	P86				
7	RESET					
8	XOUT					
9	Vss					
10	XIN					
11	Vcc					
12		P85	$\overline{\text{NMI}}$	$\overline{\text{SD}}$		
13		P84	$\overline{\text{INT}}_2$	ZP		
14		P83	$\overline{\text{INT}}_1$			
15		P82	$\overline{\text{INT}}_0$			
16		P81		TA4IN / $\overline{\text{U}}$		
17		P80		TA4OUT / U		
18		P77		TA3IN		
19		P76		TA3OUT		
20		P75		TA2IN / $\overline{\text{W}}$		
21		P74		TA2OUT / W		
22		P73		TA1IN / $\overline{\text{V}}$	$\overline{\text{CTS}}_2 / \overline{\text{RTS}}_2 / \text{TxD}_1$	
23		P72		TA1OUT / V	CLK2 / RxD1	
24		P71		TA0IN	RxD2 / SCL2 / CLK1	
25		P70		TA0OUT	TxD2 / SDA2 / $\overline{\text{RTS}}_1 / \overline{\text{CTS}}_1 / \overline{\text{CTS}}_0 / \text{CLKS}_1$	
26		P67			TxD1	
27		P66			RxD1	
28		P65			CLK1	
29		P64			$\overline{\text{RTS}}_1 / \overline{\text{CTS}}_1 / \overline{\text{CTS}}_0 / \text{CLKS}_1$	
30		P63			TxD0	
31		P62			RxD0	
32		P61			CLK0	
33		P60			$\overline{\text{RTS}}_0 / \overline{\text{CTS}}_0$	
34		P17	$\overline{\text{INT}}_5$	IDU		
35		P16	$\overline{\text{INT}}_4$	IDW		
36		P15	$\overline{\text{INT}}_3$	IDV		ADTRG
37		P107	$\overline{\text{KI}}_3$			AN7
38		P106	$\overline{\text{KI}}_2$			AN6
39		P105	$\overline{\text{KI}}_1$			AN5
40		P104	$\overline{\text{KI}}_0$			AN4
41		P103				AN3
42		P102				AN2
43		P101				AN1
44	AVss					
45		P100				AN0
46	VREF					
47	AVcc					
48		P93				AN24

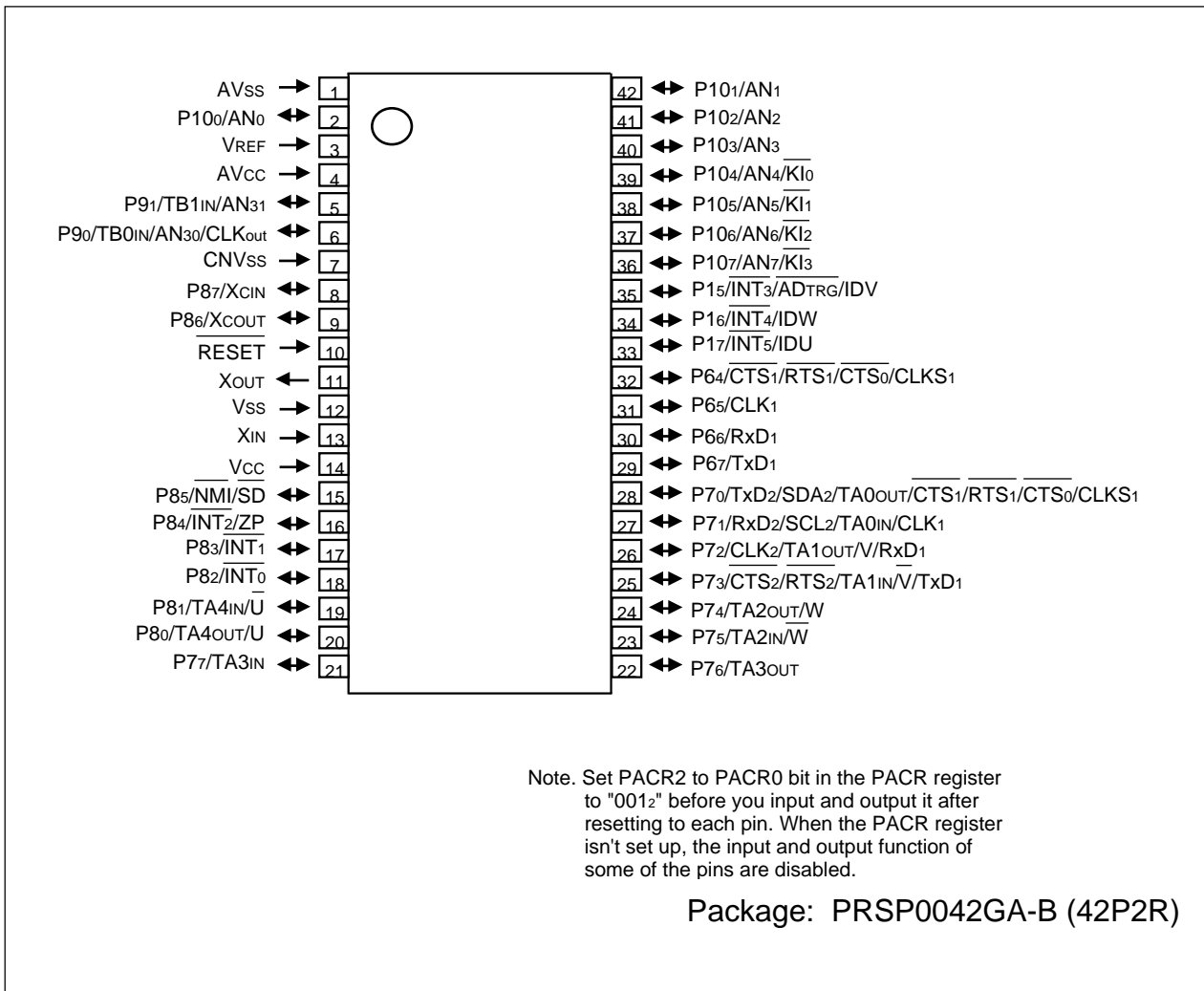


Figure 1.7 Pin Assignment for 42-Pin Package (Top View)

Table 1.12 Pin Characteristics for 42-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin
1	AVss					
2		P100				AN0
3	VREF					
4	AVCC					
5		P91		TB1IN		AN31
6		P90		TB0IN	CLKOUT	AN30
7	CNVss					
8	XCIN	P87				
9	XCOUT	P86				
10	RESET					
11	XOUT					
12	Vss					
13	XIN					
14	VCC					
15		P85	NMI	SD		
16		P84	INT2	ZP		
17		P83	INT1			
18		P82	INT0			
19		P81		TA4IN / U		
20		P80		TA4OUT / U		
21		P77		TA3IN		
22		P76		TA3OUT		
23		P75		TA2IN / W		
24		P74		TA2OUT / W		
25		P73		TA1IN / V	CTS2 / RTS2 / TxD1	
26		P72		TA1OUT / V	CLK2 / RxD1	
27		P71		TA0IN	RxD2 / SCL2 / CLK1	
28		P70		TA0OUT	TxD2 / SDA2 / RTS1 / CTS1 / CTS0 / CLKS1	
29		P67			TxD1	
30		P66			RxD1	
31		P65			CLK1	
32		P64			RTS1 / CTS1 / CTS0 / CLKS1	
33		P17	INT5	IDU		
34		P16	INT4	IDW		
35		P15	INT3	IDV		ADTRG
36		P107	KI3			AN7
37		P106	KI2			AN6
38		P105	KI1			AN5
39		P104	KI0			AN4
40		P103				AN3
41		P102				AN2
42		P101				AN1

1.6 Pin Description

Table 1.13 Pin Description (48-Pin and 42-Pin Packages)

Classification	Pin Name	I/O Type	Description
Power Supply	Vcc, Vss	I	Apply 0V to the Vss pin. Apply following voltage to the Vcc pin. 2.7 to 5.5 V (M16C/26A, M16C/26B), 3.0 to 5.5 V (M16C/26T T-ver.), 4.2 to 5.5 V (M16C/26T V-ver.)
Analog Power Supply	AVcc AVss	I	Supplies power to the A/D converter. Connect the AVcc pin to Vcc and the AVss pin to Vss
Reset Input	RESET	I	The MCU is in a reset state when "L" is applied to the RESET pin
CNVSS	CNVss	I	Connect the CNVss pin to Vss
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open. If XIN is not used (for external oscillator or external clock), connect XIN pin to Vcc and leave XOUT open
Main Clock Output	XOUT	O	
Sub Clock Input	Xcin	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between Xcin and Xcout
Sub Clock Output	Xcout	O	
Clock Output	CLKOUT	O	Outputs the clock having the same frequency as f1, f8, f32, or fc
INT Interrupt Input	INT0 to INT5	I	Input pins for the INT interrupt. INT2 can be used for Timer A Z-phase function
NMI Interrupt Input	NMI	I	NMI interrupt input pin. NMI cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $\overline{\text{NMI}}$ after setting it's direction register to "0" when the three-phase motor control is enabled
Key Input Interrupt	KI0 to KI3	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
	ZP	I	Input pin for Z-phase
Timer B	TB0IN to TB1IN	I	Timer B0 to B1 input pins
Three-Phase Motor Control Timer Output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	Output pins for the three-phase motor control timer
	IDU, IDW, IDV, $\overline{\text{SD}}$	I/O	I/O pins for the three-phase motor control timer
Serial I/O	CTS1 to CTS2	I	Input pins to control data transmission
	RTS1 to RTS2	O	Output pins to control data reception
	CLK1 to CLK2	I/O	Inputs and outputs the transfer clock
	RxD1 to RxD2	I	Inputs serial data
	TxD1 to TxD2	O	Outputs serial data
	CLKS1	O	Output pin for transfer clock
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter
A/D Converter	AN0 to AN7 AN30 to AN31	I	Analog input pins for the A/D converter
	ADTRG	I	Input pin for an external A/D trigger
I/O Ports	P15 to P17	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 3-bit units
	P64 to P67 P70 to P77 P80 to P87 P100 to P107 P90 to P91	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units

I : Input O : Output I/O : Input and output

Table 1.13 Pin Description (48-pin packages only) (Continued)

Classification	Pin Name	I/O Type	Description
Serial I/O	CTS0	I	Inputs pin to control data transmission
	RTS0	O	Output pin to control data reception
	CLK0	I/O	Inputs and outputs the transfer clock
	RxD0	I	Inputs serial data
	TxD0	O	Outputs serial data
Timer B	TB2IN	I	Timer B2 input pin
A/D Converter	AN24 AN32	I	Analog input pins for the A/D converter
I/O Ports	P60 to P63 P92 to P93	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The register bank is comprised of seven registers (R0, R1, R2, R3, A0, A1 and FB) out of 13 registers. There are two sets of register bank.

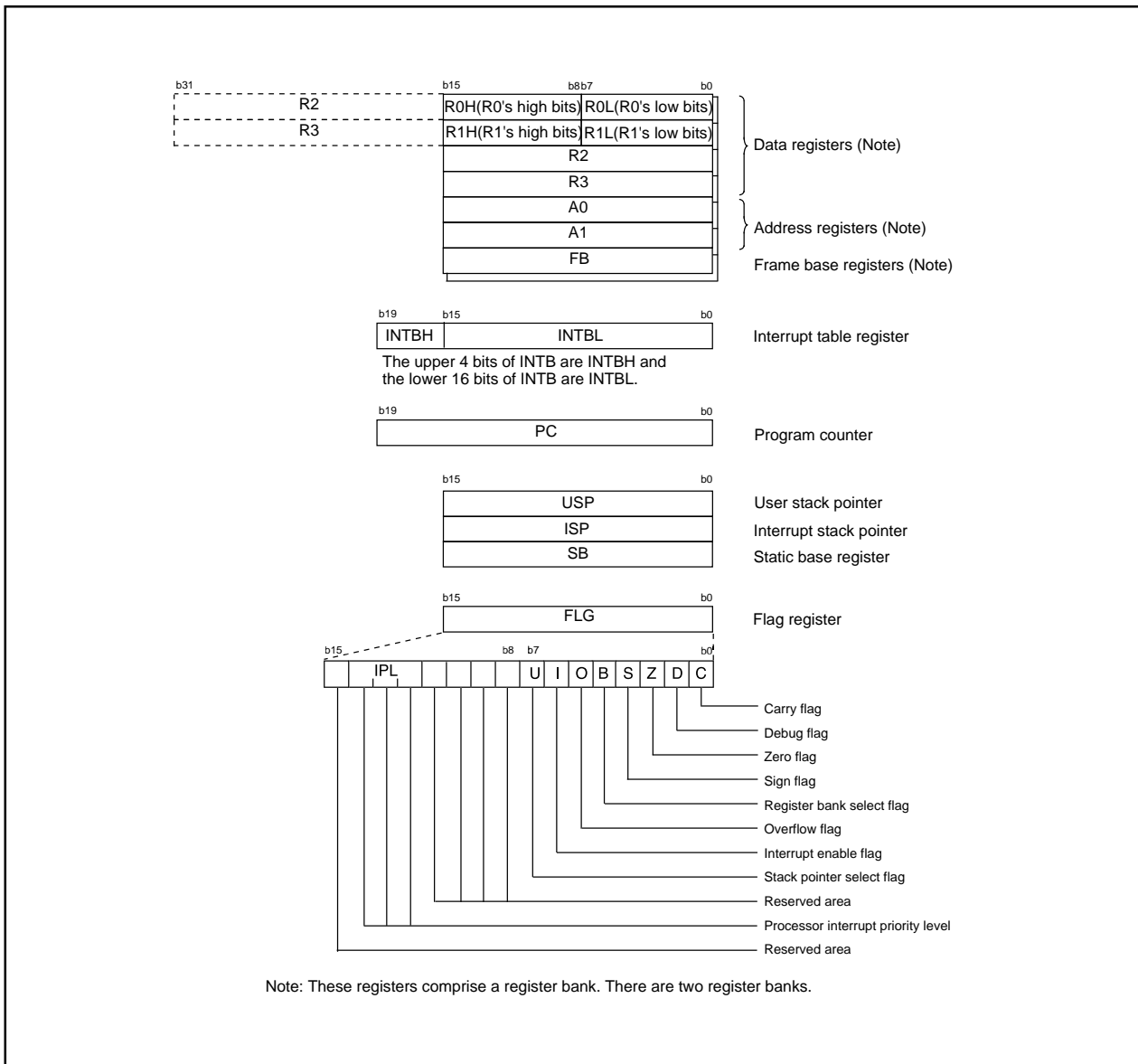


Figure 2.1. CPU Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to 0.

2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0; register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1.

The I flag is cleared to 0 when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is cleared to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is undefined.

3. Memory

Figure 3.1 is a memory map of the M16C/26A Group (M16C/26A, M16C/26B, M16C/26T). The M16C/26A Group provides 1-Mbyte address space addresses 00000₁₆ to FFFFF₁₆.

The internal ROM is allocated lower address, beginning with address FFFFF₁₆. For example, a 64-Kbyte internal ROM area is allocated in addresses F0000₁₆ to FFFFF₁₆. The flash memory version has two sets of 2-Kbyte internal ROM area, block A and block B, for data space. These blocks are allocated addresses F000₁₆ to FFFF₁₆.

The fixed interrupt vectors are allocated addresses FFFDC₁₆ to FFFFF₁₆ and they store the start address of each interrupt routine.

The internal RAM is allocated higher addresses, beginning with address 00400₁₆. For example, a 1-Kbyte internal RAM area is allocated in addresses 00400₁₆ to 007FF₁₆. The internal RAM is used for temporarily storing data. The area is also used as stacks when subroutines are called or interrupt requests are acknowledged.

The SFR is allocated addresses 00000₁₆ to 003FF₁₆. The peripheral function control registers are allocated here. All blank spaces within SFR location are reserved and cannot be accessed by users.

The special page vectors are allocated addresses FFE00₁₆ to FFFDB₁₆. They are used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M16C/60 and M16C/20 Series Software Manual** for details.

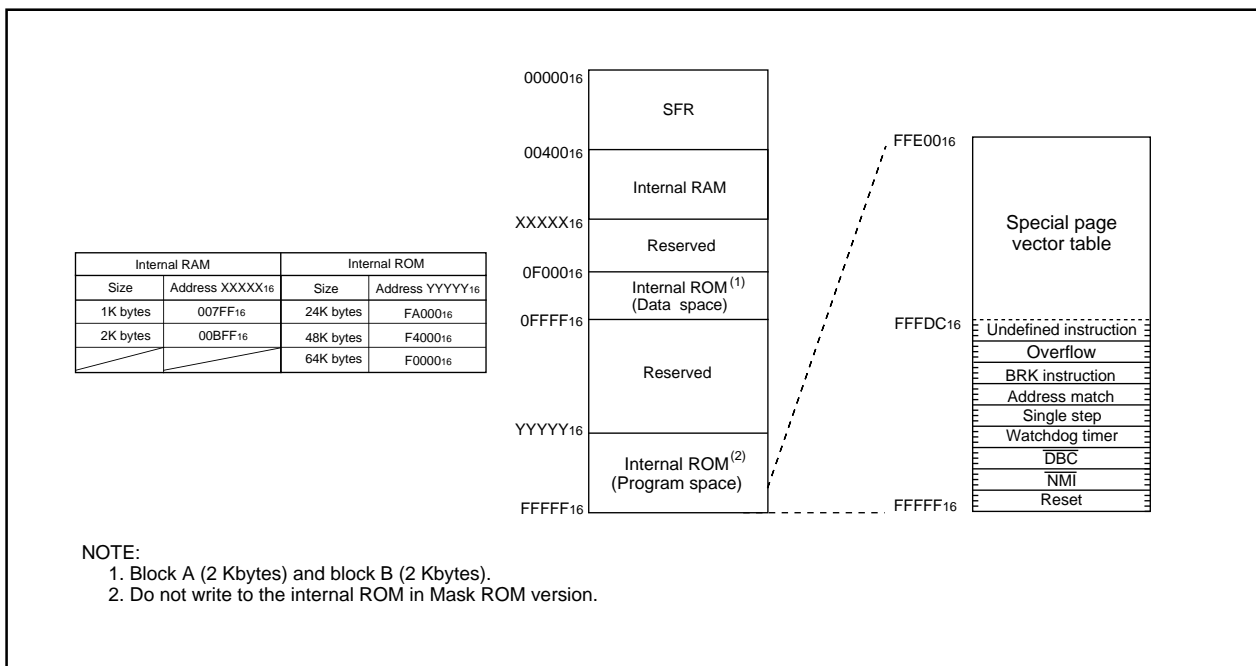


Figure 3.1 Memory Map

4. Special Function Register (SFR)

Table 4.1 SFR Information(1)(1)

Address	Register	Symbol	After reset
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0	PM0	00 ₁₆
0005 ₁₆	Processor mode register 1	PM1	00001000 ₂
0006 ₁₆	System clock control register 0	CM0	01001000 ₂ (M16C/26A) 01101000 ₂ (M16C/26T)
0007 ₁₆	System clock control register 1	CM1	00100000 ₂
0008 ₁₆			
0009 ₁₆	Address match interrupt enable register	AIER	XXXXXX00 ₂
000A ₁₆	Protect register	PRCR	XX000000 ₂
000B ₁₆			
000C ₁₆	Oscillation stop detection register ⁽²⁾	CM2	0X000000 ₂
000D ₁₆			
000E ₁₆	Watchdog timer start register	WDTS	XX ₁₆
000F ₁₆	Watchdog timer control register	WDC	00XXXXXX ₂ ⁽³⁾
0010 ₁₆	Address match interrupt register 0	RMAD0	00 ₁₆
0011 ₁₆			00 ₁₆
0012 ₁₆			X0 ₁₆
0013 ₁₆			
0014 ₁₆	Address match interrupt register 1	RMAD1	00 ₁₆
0015 ₁₆			00 ₁₆
0016 ₁₆			X0 ₁₆
0017 ₁₆			
0018 ₁₆			
0019 ₁₆	Voltage detection register 1 ^(4, 5)	VCR1	00001000 ₂
001A ₁₆	Voltage detection register 2 ^(4, 5)	VCR2	00 ₁₆
001B ₁₆			
001C ₁₆	PLL control register 0	PLC0	0001X010 ₂
001D ₁₆			
001E ₁₆	Processor mode register 2	PM2	XXX00000 ₂
001F ₁₆	Low voltage detection interrupt register ⁽⁵⁾	D4INT	00 ₁₆
0020 ₁₆	DMA0 source pointer	SAR0	XX ₁₆
0021 ₁₆			XX ₁₆
0022 ₁₆			XX ₁₆
0023 ₁₆			
0024 ₁₆	DMA0 destination pointer	DAR0	XX ₁₆
0025 ₁₆			XX ₁₆
0026 ₁₆			XX ₁₆
0027 ₁₆			
0028 ₁₆	DMA0 transfer counter	TCR0	XX ₁₆
0029 ₁₆			XX ₁₆
002A ₁₆			
002B ₁₆			
002C ₁₆	DMA0 control register	DM0CON	00000X00 ₂
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆	DMA1 source pointer	SAR1	XX ₁₆
0031 ₁₆			XX ₁₆
0032 ₁₆			XX ₁₆
0033 ₁₆			XX ₁₆
0034 ₁₆	DMA1 destination pointer	DAR1	XX ₁₆
0035 ₁₆			XX ₁₆
0036 ₁₆			XX ₁₆
0037 ₁₆			
0038 ₁₆	DMA1 transfer counter	TCR1	XX ₁₆
0039 ₁₆			XX ₁₆
003A ₁₆			
003B ₁₆			
003C ₁₆	DMA1 control register	DM1CON	00000X00 ₂
003D ₁₆			
003E ₁₆			
003F ₁₆			

NOTES:

1. The blank spaces are reserved. No access is allowed.
2. Bits CM27, CM21, and CM20 do not change at oscillation stop detection reset.
3. The WDC5 bit is 0 (cold start) immediately after power-on. It can only be set to 1 by program. The WDC5 bit cannot be used in M16C/26T.
4. The VCR1 and VCR2 registers do not change at software reset, watchdog timer reset, and oscillation stop detection reset.
5. Registers VCR1, VCR2, and D4INT cannot be used in M16C/26T.

X : Undefined

Table 4.2 SFR Information(2)⁽¹⁾

Address	Register	Symbol	After reset
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆	INT3 interrupt control register	INT3IC	XX00X000 ₂
0045 ₁₆			
0046 ₁₆			
0047 ₁₆			
0048 ₁₆	INT5 interrupt control register	INT5IC	XX00X000 ₂
0049 ₁₆	INT4 interrupt control register	INT4IC	XX00X000 ₂
004A ₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXXX000 ₂
004B ₁₆	DMA0 interrupt control register	DM0IC	XXXXX000 ₂
004C ₁₆	DMA1 interrupt control register	DM1IC	XXXXX000 ₂
004D ₁₆	Key input interrupt control register	KUPIC	XXXXX000 ₂
004E ₁₆	A/D conversion interrupt control register	ADIC	XXXXX000 ₂
004F ₁₆	UART2 transmit interrupt control register	S2TIC	XXXXX000 ₂
0050 ₁₆	UART2 receive interrupt control register	S2RIC	XXXXX000 ₂
0051 ₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX000 ₂
0052 ₁₆	UART0 receive interrupt control register	S0RIC	XXXXX000 ₂
0053 ₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX000 ₂
0054 ₁₆	UART1 receive interrupt control register	S1RIC	XXXXX000 ₂
0055 ₁₆	TimerA0 interrupt control register	TA0IC	XXXXX000 ₂
0056 ₁₆	TimerA1 interrupt control register	TA1IC	XXXXX000 ₂
0057 ₁₆	TimerA2 interrupt control register	TA2IC	XXXXX000 ₂
0058 ₁₆	TimerA3 interrupt control register	TA3IC	XXXXX000 ₂
0059 ₁₆	TimerA4 interrupt control register	TA4IC	XXXXX000 ₂
005A ₁₆	TimerB0 interrupt control register	TB0IC	XXXXX000 ₂
005B ₁₆	TimerB1 interrupt control register	TB1IC	XXXXX000 ₂
005C ₁₆	TimerB2 interrupt control register	TB2IC	XXXXX000 ₂
005D ₁₆	INT0 interrupt control register	INT0IC	XX00X000 ₂
005E ₁₆	INT1 interrupt control register	INT1IC	XX00X000 ₂
005F ₁₆	INT2 interrupt control register	INT2IC	XX00X000 ₂
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆			
0069 ₁₆			
006A ₁₆			
006B ₁₆			
006C ₁₆			
006D ₁₆			
006E ₁₆			
006F ₁₆			
0070 ₁₆			
0071 ₁₆			
0072 ₁₆			
0073 ₁₆			
0074 ₁₆			
0075 ₁₆			
0076 ₁₆			
0077 ₁₆			
0078 ₁₆			
0079 ₁₆			
007A ₁₆			
007B ₁₆			
007C ₁₆			
007D ₁₆			
007E ₁₆			
007F ₁₆			

NOTE:

1. Blank spaces are reserved. No access is allowed.

X: Undefined

Table 4.3 SFR Information(3)⁽¹⁾

Address	Register	Symbol	After reset
0080 ₁₆			
0081 ₁₆			
0082 ₁₆			
0083 ₁₆			
0084 ₁₆			
0085 ₁₆			
0086 ₁₆			
01B0 ₁₆			
01B1 ₁₆			
01B2 ₁₆			
01B3 ₁₆	Flash memory control register 4 (Note 2)	FMR4	01000000 ₂
01B4 ₁₆			
01B5 ₁₆	Flash memory control register 1 (Note 2)	FMR1	000XXX0X ₂
01B6 ₁₆			
01B7 ₁₆	Flash memory control register 0 (Note 2)	FMR0	01 ₁₆
01B8 ₁₆			
01B9 ₁₆			
01BA ₁₆			
01BB ₁₆			
01BC ₁₆			
01BD ₁₆			
01BE ₁₆			
01BF ₁₆			
0250 ₁₆			
0251 ₁₆			
0252 ₁₆			
0253 ₁₆			
0254 ₁₆			
0255 ₁₆			
0256 ₁₆			
0257 ₁₆			
0258 ₁₆			
0259 ₁₆			
025A ₁₆	Three phase protect control register	TPRC	00 ₁₆
025B ₁₆			
025C ₁₆	On-chip oscillator control register	ROCR	00000101 ₂
025D ₁₆	Pin assignment control register	PACR	00 ₁₆
025E ₁₆	Peripheral clock select register	PCLKR	00000011 ₂
025F ₁₆			
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆			
0335 ₁₆			
0336 ₁₆			
0337 ₁₆			
0338 ₁₆			
0339 ₁₆			
033A ₁₆			
033B ₁₆			
033C ₁₆			
033D ₁₆			
033E ₁₆	NMI digital debounce register	NDDR	FF ₁₆
033F ₁₆	Port17 digital debounce register	P17DDR	FF ₁₆

NOTES:

- Blank spaces are reserved. No access is allowed.
- This register is included in the flash memory version.

X: Undefined

Table 4.4 SFR Information(4)⁽¹⁾

Address	Register	Symbol	After reset
0340 ₁₆			
0341 ₁₆			
0342 ₁₆	Timer A1-1 register	TA11	XX ₁₆
0343 ₁₆			XX ₁₆
0344 ₁₆	Timer A2-1 register	TA21	XX ₁₆
0345 ₁₆			XX ₁₆
0346 ₁₆	Timer A4-1 register	TA41	XX ₁₆
0347 ₁₆			XX ₁₆
0348 ₁₆	Three phase PWM control register 0	INVC0	00 ₁₆
0349 ₁₆	Three phase PWM control register 1	INVC1	00 ₁₆
034A ₁₆	Three phase output buffer register 0	IDB0	3F ₁₆
034B ₁₆	Three phase output buffer register 1	IDB1	3F ₁₆
034C ₁₆	Dead time timer	DTT	XX ₁₆
034D ₁₆	Timer B2 Interrupt occurrence frequency set counter	ICTB2	XX ₁₆
034E ₁₆	Position-data-retain function control register	PDRF	XXXX0000 ₂
034F ₁₆			
0350 ₁₆			
0351 ₁₆			
0352 ₁₆			
0353 ₁₆			
0354 ₁₆			
0355 ₁₆			
0356 ₁₆			
0357 ₁₆			
0358 ₁₆	Port function control register	PFCR	00111111 ₂
0359 ₁₆			
035A ₁₆			
035B ₁₆			
035C ₁₆			
035D ₁₆			
035E ₁₆	Interrupt request cause select register 2	IFSR2A	XXXXXXXX ₂
035F ₁₆	Interrupt request cause select register	IFSR	00 ₁₆
0360 ₁₆			
0361 ₁₆			
0362 ₁₆			
0363 ₁₆			
0364 ₁₆			
0365 ₁₆			
0366 ₁₆			
0367 ₁₆			
0368 ₁₆			
0369 ₁₆			
036A ₁₆			
036B ₁₆			
036C ₁₆			
036D ₁₆			
036E ₁₆			
036F ₁₆			
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆	UART2 special mode register 4	U2SMR4	00 ₁₆
0375 ₁₆	UART2 special mode register 3	U2SMR3	00X0X0X ₂
0376 ₁₆	UART2 special mode register 2	U2SMR2	X0000000 ₂
0377 ₁₆	UART2 special mode register	U2SMR	X0000000 ₂
0378 ₁₆	UART2 transmit/receive mode register	U2MR	00 ₁₆
0379 ₁₆	UART2 bit rate register	U2BRG	XX ₁₆
037A ₁₆	UART2 transmit buffer register	U2TB	XXXXXXXX ₂
037B ₁₆			XXXXXXXX ₂
037C ₁₆	UART2 transmit/receive control register 0	U2C0	00001000 ₂
037D ₁₆	UART2 transmit/receive control register 1	U2C1	00000010 ₂
037E ₁₆	UART2 receive buffer register	U2RB	XXXXXXXX ₂
037F ₁₆			XXXXXXXX ₂

NOTE:

1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.5 SFR Information(5)⁽¹⁾

Address	Register	Symbol	After reset
0380 ₁₆	Count start flag	TABSR	00 ₁₆
0381 ₁₆	Clock prescaler reset flag	CPSRF	0XXXXXXX ₂
0382 ₁₆	One-shot start flag	ONSF	00 ₁₆
0383 ₁₆	Trigger select register	TRGSR	00 ₁₆
0384 ₁₆	Up-downm flag	UDF	00 ₁₆
0385 ₁₆			
0386 ₁₆ 0387 ₁₆	Timer A0 register	TA0	XX ₁₆ XX ₁₆
0388 ₁₆ 0389 ₁₆	Timer A1 register	TA1	XX ₁₆ XX ₁₆
038A ₁₆ 038B ₁₆	Timer A2 register	TA2	XX ₁₆ XX ₁₆
038C ₁₆ 038D ₁₆	Timer A3 register	TA3	XX ₁₆ XX ₁₆
038E ₁₆ 038F ₁₆	Timer A4 register	TA4	XX ₁₆ XX ₁₆
0390 ₁₆ 0391 ₁₆	Timer B0 register	TB0	XX ₁₆ XX ₁₆
0392 ₁₆ 0393 ₁₆	Timer B1 register	TB1	XX ₁₆ XX ₁₆
0394 ₁₆ 0395 ₁₆	Timer B2 register	TB2	XX ₁₆ XX ₁₆
0396 ₁₆	Timer A0 mode register	TA0MR	00 ₁₆
0397 ₁₆	Timer A1 mode register	TA1MR	00 ₁₆
0398 ₁₆	Timer A2 mode register	TA2MR	00 ₁₆
0399 ₁₆	Timer A3 mode register	TA3MR	00 ₁₆
039A ₁₆	Timer A4 mode register	TA4MR	00 ₁₆
039B ₁₆	Timer B0 mode register	TB0MR	00XX0000 ₂
039C ₁₆	Timer B1 mode register	TB1MR	00XX0000 ₂
039D ₁₆	Timer B2 mode register	TB2MR	00XX0000 ₂
039E ₁₆ 039F ₁₆	Timer B2 special mode register	TB2SC	X0000000 ₂
03A0 ₁₆	UART0 transmit/receive mode register	U0MR	00 ₁₆
03A1 ₁₆	UART0 bit rate register	U0BRG	XX ₁₆
03A2 ₁₆ 03A3 ₁₆	UART0 transmit buffer register	U0TB	XXXXXXXX ₂ XXXXXXXX ₂
03A4 ₁₆	UART0 transmit/receive control register 0	U0C0	00001000 ₂
03A5 ₁₆	UART0 transmit/receive control register 1	U0C1	00000010 ₂
03A6 ₁₆ 03A7 ₁₆	UART0 receive buffer register	U0RB	XXXXXXXX ₂ XXXXXXXX ₂
03A8 ₁₆	UART1 transmit/receive mode register	U1MR	00 ₁₆
03A9 ₁₆	UART1 bit rate register	U1BRG	XX ₁₆
03AA ₁₆ 03AB ₁₆	UART1 transmit buffer register	U1TB	XXXXXXXX ₂ XXXXXXXX ₂
03AC ₁₆	UART1 transmit/receive control register 0	U1C0	00001000 ₂
03AD ₁₆	UART1 transmit/receive control register 1	U1C1	00000010 ₂
03AE ₁₆ 03AF ₁₆	UART1 receive buffer register	U1RB	XXXXXXXX ₂ XXXXXXXX ₂
03B0 ₁₆ 03B1 ₁₆ 03B2 ₁₆ 03B3 ₁₆	UART transmit/receive control register 2	UCON	X0000000 ₂
03B4 ₁₆ 03B5 ₁₆	CRC snoop address register	CRCSAR	XX ₁₆ 00XXXXXXXX ₂
03B6 ₁₆ 03B7 ₁₆	CRC mode register	CRCMR	0XXXXXXXX0 ₂
03B8 ₁₆ 03B9 ₁₆	DMA0 request cause select register	DM0SL	00 ₁₆
03BA ₁₆ 03BB ₁₆	DMA1 request cause select register	DM1SL	00 ₁₆
03BC ₁₆ 03BD ₁₆	CRC data register	CRCD	XX ₁₆ XX ₁₆
03BE ₁₆ 03BF ₁₆	CRC input register	CRCIN	XX ₁₆

NOTE:

1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.6 SFR Information(6)⁽¹⁾

Address	Register	Symbol	After Reset
03C0 ₁₆ 03C1 ₁₆	A/D register 0	AD0	XXXXXXXX ₂ XXXXXXXX ₂
03C2 ₁₆ 03C3 ₁₆	A/D register 1	AD1	XXXXXXXX ₂ XXXXXXXX ₂
03C4 ₁₆ 03C5 ₁₆	A/D register 2	AD2	XXXXXXXX ₂ XXXXXXXX ₂
03C6 ₁₆ 03C7 ₁₆	A/D register 3	AD3	XXXXXXXX ₂ XXXXXXXX ₂
03C8 ₁₆ 03C9 ₁₆	A/D register 4	AD4	XXXXXXXX ₂ XXXXXXXX ₂
03CA ₁₆ 03CB ₁₆	A/D register 5	AD5	XXXXXXXX ₂ XXXXXXXX ₂
03CC ₁₆ 03CD ₁₆	A/D register 6	AD6	XXXXXXXX ₂ XXXXXXXX ₂
03CE ₁₆ 03CF ₁₆	A/D register 7	AD7	XXXXXXXX ₂ XXXXXXXX ₂
03D0 ₁₆			
03D1 ₁₆			
03D2 ₁₆	A/D trigger control register	ADTRGCON	00 ₁₆
03D3 ₁₆	A/D status register 0	ADSTAT0	0000X00 ₂
03D4 ₁₆ 03D5 ₁₆	A/D control register 2	ADCON2	00 ₁₆
03D6 ₁₆	A/D control register 0	ADCON0	0000XXX ₂
03D7 ₁₆ 03D8 ₁₆	A/D control register 1	ADCON1	00 ₁₆
03D9 ₁₆			
03DA ₁₆			
03DB ₁₆			
03DC ₁₆			
03DD ₁₆			
03DE ₁₆			
03DF ₁₆			
03E0 ₁₆			
03E1 ₁₆ 03E2 ₁₆	Port P1 register	P1	XX ₁₆
03E3 ₁₆ 03E4 ₁₆	Port P1 direction register	PD1	00 ₁₆
03E5 ₁₆			
03E6 ₁₆			
03E7 ₁₆			
03E8 ₁₆			
03E9 ₁₆			
03EA ₁₆			
03EB ₁₆			
03EC ₁₆	Port P6 register	P6	XX ₁₆
03ED ₁₆	Port P7 register	P7	XX ₁₆
03EE ₁₆	Port P6 direction register	PD6	00 ₁₆
03EF ₁₆	Port P7 direction register	PD7	00 ₁₆
03F0 ₁₆	Port P8 register	P8	XX ₁₆
03F1 ₁₆	Port P9 register	P9	XXXXXXXX ₂
03F2 ₁₆	Port P8 direction register	PD8	00 ₁₆
03F3 ₁₆	Port P9 direction register	PD9	XXXX0000 ₂
03F4 ₁₆ 03F5 ₁₆	Port P10 register	P10	XX ₁₆
03F6 ₁₆	Port P10 direction register	PD10	00 ₁₆
03F7 ₁₆			
03F8 ₁₆			
03F9 ₁₆			
03FA ₁₆			
03FB ₁₆			
03FC ₁₆	Pull-up control register 0	PUR0	00 ₁₆
03FD ₁₆	Pull-up control register 1	PUR1	00 ₁₆
03FE ₁₆	Pull-up control register 2	PUR2	00 ₁₆
03FF ₁₆	Port control register	PCR	00 ₁₆

NOTE:

1. Blank spaces are reserved. No access is allowed.

X: Undefined

Package

JEITA Package Code	RENEASAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g

NOTE)

1. DIMENSIONS *1* AND *2* DO NOT INCLUDE MOLD FLASH.
2. DIMENSION *3* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A ₂	—	1.4	—
H _D	8.8	9.0	9.2
H _E	8.8	9.0	9.2
A	—	—	1.7
A ₁	0	0.1	0.2
b _D	0.17	0.22	0.27
b ₁	—	0.20	—
c	0.09	0.145	0.20
c ₁	—	0.125	—
β	0°	—	8°
ⓐ	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z _D	—	0.75	—
Z _E	—	0.75	—
L	0.35	0.5	0.65
L ₁	—	1.0	—

JEITA Package Code	RENEASAS Code	Previous Code	MASS[Typ.]
P-SSOP42-8.4x17.5-0.80	PRSP0042GA-B	42P2R-E	0.6g

NOTE)

1. DIMENSIONS *1* AND *2* DO NOT INCLUDE MOLD FLASH.
2. DIMENSION *3* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	17.3	17.5	17.7
E	8.2	8.4	8.6
A ₂	—	2.0	—
A	—	—	2.4
A ₁	0.05	—	—
b _D	0.25	0.3	0.4
c	0.13	0.15	0.2
β	0°	—	10°
H _E	11.63	11.93	12.23
e	0.65	0.8	0.95
y	—	—	0.15
L	0.3	0.5	0.7

REVISION HISTORY	M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) Shortsheet
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Rev.	Date	Description	
		Page	Summary
0.51	07/25/06	-	First edition

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