THE DATASHEET OF

M21218G-42

M21208/M21218

SD and HD/SD-SDI Digital Video Cable Drivers

Rev V4

Applications

- Serial Routing Switchers, Production/Master Control Switchers
- Distribution Amplifiers
- Video Tape Recorders, ENG Edit decks, Cameras
- Broadcast video applications
- NLE's, MPEG Encoders/Decoders, format convertors etc.

Standards Compliance

- SMPTE 292M, 259M, 344M

Features

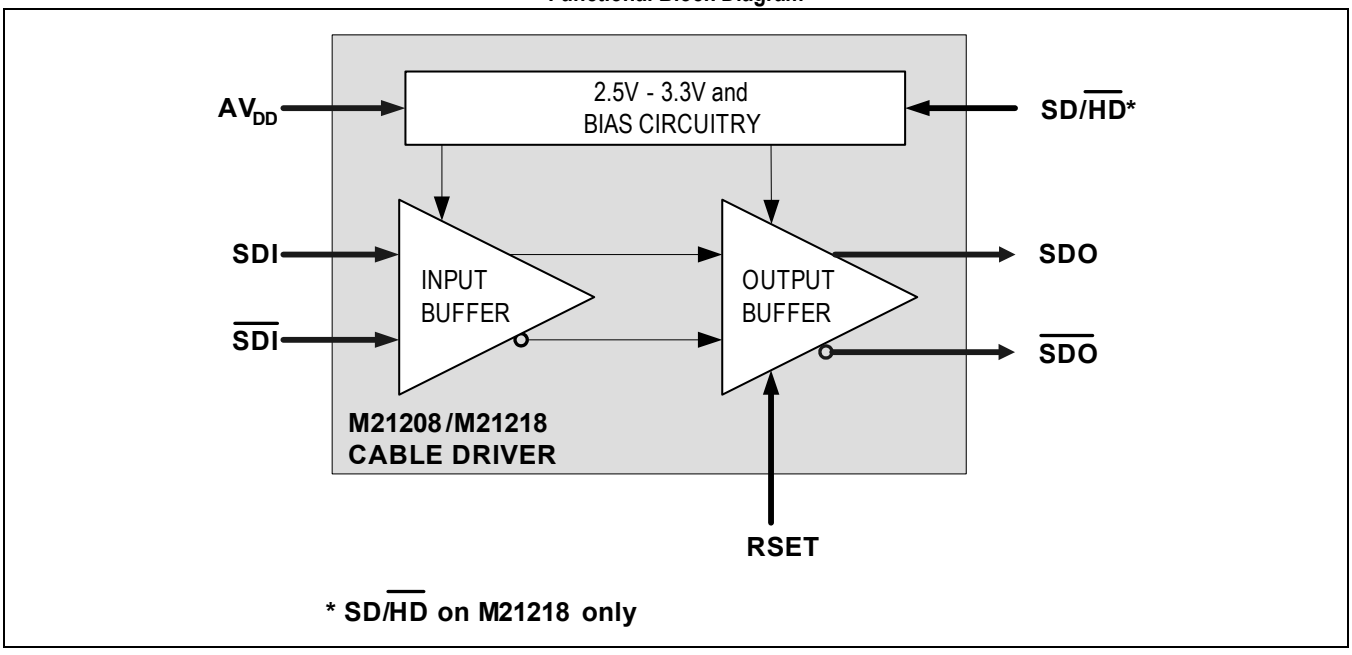
- HD and SD operation (M21218)
- SD operation (M21208)
- Pin compatible to GS9068/9068A (M21208)
- Pin compatible to GS1528/1528A (M21218)
- 800 mVp–p single ended output swing (typical)
- 1600 mVp–p maximum single ended output swing
- SD/HD Slew Rate control (M21218)
- 2.5V or 3.3V supply
- Low P_{DISS} (122 mW @ 2.5V, 144 mW @ 3.3V)
- Extended temperature range: -10 °C to 85 °C
- RoHS package

The M21208 and M21218 are high-speed, low-power, low-jitter cable drivers. They are designed to drive serial digital video data through 75Ω coaxial cable typically used in SMPTE and DVB-ASI video applications. The M21218 cable driver is optimized for performance from 143 Mbps up to 1485 Mbps, it has selectable slew rate for SD-SDI and HD-SDI applications. The M21208 cable driver is optimized for performance from 143 Mbps up to 540 Mbps with SD-SDI slew rates.

The typical output rise/fall time of the M21218 is 100 ps for HD rates. Both devices have a typical set slew rate of 600 ps at SD rates. The default output voltage swing is compliant with SMPTE 292M, 259M and 344M using a 750Ω ±1% resistor. The M21208 and M21218 are pin compatible, with the exception that the M21208 has no SD/HD control pin. M21208/M21218 support a maximum single ended output swing of 1600 mVp–p, when configured appropriately.

Both devices are available in a small outline RoHS compliant package, which is backwards compatible with standard JEDEC SnPb processes. The M21208 is pin compatible with the GS9068/9068A devices, and the M21218 is pin compatible with the GS1528/1528A, both support 2.5V and 3.3V operation.

Functional Block Diagram



Ordering Information

Part Number	Data Rates Supported	Package	Operating Temperature
M21208G-xx*	143–540 Mbps	SOIC—8 pin	-10 °C to 85 °C
M21218G-xx*	143–1485 Mbps	SOIC—8 pin	-10 °C to 85 °C

* Consult the MACOM price list for exact part number when ordering.

* The letter “G” designator after the part number indicates that the device is RoHS-compliant. This device is backward compatible with existing 225 °C reflow profiles.

Revision History

Revision	Level	Date	Description
V4	Release	May 2015	Updated logos and page layout. No content changes.
C (V3)	Release	July 2009	Revised AV_{DD} maximum rating in Table 1-1. Revised 2.5V to 3.3V minimum termination voltage.
B (V2)	Release	April 2007	Updated ordering information. Modified text in Section 2.2.2 to indicate that RSET must be used. SD/HD changed to pull-up in Table 2-2. DCD figure changed in Table 1-6 and Table 1-7.
A (V1)	Release	February 2007	Production Release. Combined M21208 and M21218 data sheets (21208-DSH-001-A and 21218-DSH-002-A). Changed maximum output swing to 1600 mV. Removed 1.8V operation. Updated Tables 2-1, 1-2, 1-3, and 1-7.

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1.0 Product Specification

1.1 Absolute Maximum Ratings

Table 1-1. Absolute Maximum Ratings (1)

Symbol	Parameter	Minimum	Maximum	Units
AV_{DD}	I/O Power	AV_{SS} - 0.5	3.6	V
V_{IOAM}	Voltage on any I/O Pin	AV_{SS} - 0.5	AV_{DD} + 0.5	V
T_{STORE}	Storage Temperature	-65	+150	°C
ESD_{HBML}	Human Body Model (low-speed)	2000	—	V
ESD_{HBMH}	Human Body Model (high-speed)	2000	—	V
ESD_{CDM}	Charge Device Model	500	—	V

NOTE:

1. Absolute Maximum is the limit beyond which the device life cannot be guaranteed. These limits shall not be construed to imply operational limits. Please refer to recommended operating conditions when evaluation device performance and functionality.

1.2 Recommended Operating Conditions

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
AV_{DD}	Device Power	1	—	2.5/3.3	—	V
AV_{SS}	Device Ground	—	—	0	—	V
T_A	Ambient Temperature	—	-10	—	+85	°C
θ_{JA}	Junction to ambient Thermal Resistance	—	—	110	—	°C/W
AV_{DDTERM}	75Ω Output Termination Voltage	—	See Table 2-1			V

NOTE:

1. ±5% is allowed from nominal supply.

1.3 DC Electrical Specifications

Table 1-3. Power DC Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
I_{DD}	Supply Current	1, 2	—	27	—	mA
I_{DDTERM}	Current in external termination resistors	1, 2, 3	—	22	—	mA
$P_{DISSINT}$	Power dissipation (AV_{DD} = 2.5V, AV_{DDTERM} = 3.3V)	1, 2, 5	—	122	—	mW
$P_{DISSINT}$	Power dissipation (AV_{DD} = 2.5V, AV_{DDTERM} = 5.0V)	1, 2, 5	—	159	—	mW
$P_{DISSINT}$	Power dissipation (AV_{DD} = 3.3V, AV_{DDTERM} = 3.3V)	1, 2, 5	—	144	—	mW
$P_{DISSINT}$	Power dissipation (AV_{DD} = 3.3V, AV_{DDTERM} = 5.0V)	1, 2, 5	—	181	—	mW
$P_{DISSTOT}$	Power dissipation (AV_{DD} = 2.5V, AV_{DDTERM} = 3.3V)	1, 2, 4	—	140	—	mW
$P_{DISSTOT}$	Power dissipation (AV_{DD} = 2.5V, AV_{DDTERM} = 5.0V)	1, 2, 4	—	177	—	mW
$P_{DISSTOT}$	Power dissipation (AV_{DD} = 3.3V, AV_{DDTERM} = 3.3V)	1, 2, 4	—	162	—	mW
$P_{DISSTOT}$	Power dissipation (AV_{DD} = 3.3V, AV_{DDTERM} = 5.0V)	1, 2, 4	—	199	—	mW

NOTES:

1. Recommended operating conditions—see Table 1-2.
2. 800 mV standard SMPTE swing, terminated as in Figure 1-3.
3. A portion of the power will be dissipated in the external 75OΩ termination ($P_{EXT} = V_{OD} \times I_{TERM}$).
4. $P_{DISSTOT} = AV_{DD} \times I_{DD} + AV_{DDTERM} \times I_{TERM}$.
5. $P_{DISSINT} = P_{DISSTOT} - P_{EXT}$.

1.4 Input/Output Level Specifications

Table 1-4. CMOS Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
V_{IH}	Input Logic High Voltage	1	0.75 x AV_{DD}	—	AV_{DD} + 0.3	V
V_{IL}	Input Logic Low Voltage	1	0	—	0.25 x AV_{DD}	V
I_{IH}	Input Current (logic High)	1	-100	—	100	µA
I_{IL}	Input Current (logic Low)	1	-100	—	100	µA

NOTES:

1. Specified at recommended operating condition—see Table 1-2.

Table 1-5. High-Speed Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Unit
DR_{IN}	Input Bit Rate (M21208)	1, 3	0	—	540	Mbps
DR_{IN}	Input Bit Rate (M21218)	1, 3	0	—	1485	Mbps
V_{ID}	Input Differential Voltage (peak to peak)	1, 4, 5	100	—	2000	mV
V_{CM}	Input Common-Mode Voltage	1, 2	1200	AV_{DD}	—	mV
V_{IH}	Maximum Input High Voltage	1	—	—	AV_{DD} + 400	mV
V_{IL}	Minimum Input Low Voltage	1	1200	—	—	mV
R_{IN}	Single-ended input impedance	1	—	13.33	20	kΩ

NOTES:

1. Specified at recommended operation conditions—see Table 1-2.
2. Part is DC coupled from input to output.
3. Example 1200 mV_{pp} differential = 600 mV_{pp} for each single-ended terminal.
4. Minimum input level defined as error free operation at 1 x 10^{-12} BER.

Table 1-6. Cable Driver Output Electrical Specifications M21208 (SD only)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Unit
DR_{OUT}	Output Bit Rates	1, 5	—	—	540	Mbps
t_r/t_f	SD Rise/Fall Time (20–80%)	1, 3	400	600	800	ps
t_r/t_{fMM}	Rise/fall mismatch	1, 2	—	40	100	ps
V_{OD}	Single-ended voltage swing range (sw) p–p	1, 2, 4, 5	500	800	1600	mV
V_{ODTOL}	Swing Level output variation at 800 mVp–p [**RSET** = 750Ω ±1%] (Single-Ended)	1, 2, 3	-7	—	+7	%
V_{OS}	Overshoot/Undershoot	1, 2	-8	—	+8	%
JAO_{PP}	Additive Output Jitter	1, 8	—	40	60	ps
DCD	Duty Cycle Distortion	1, 2, 6, 8	—	20	70	ps
S_{22}	Output Return Loss (5 MHz to 600MHz)	1, 2, 7	15	—	—	dB

NOTES:

Entire table tested with a 400 mVp–p differential input.

1. Specified at recommended operating condition—see Table 1-2.
2. Specification verified at 800 mVpp output with 1m cable.
3. Rated at nominal SMPTE 800 mV output swing level (using a 750Ω ±1% resistor at RSET).
4. Output stage is an open collector differential pair, actual swing dependant on IC supply voltage and external termination voltage.
5. Into 75Ω back termination and 75Ω load and appropriate external termination voltage.
6. Duty Cycle Distortion (DCD) is defined as the difference in the intrinsic jitter at the 50% voltage level and the intrinsic jitter at the rising/falling edge crossing point. If the rising/falling edge crossing point is at the 50% voltage level, then DCD = 0.
7. Measured under DC conditions that simulate AC coupling, V_T = 3.3V.
8. Measured using a “1010” data pattern.

Table 1-7. Cable Driver Output Electrical Specifications M21218 (SD/HD) (1 of 2)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Unit
DR_{OUT}	Output Bit Rates	1	—	—	1485	Mbps
t_r/t_f	SD Rise/Fall Time (20–80%)	1, 3	400	600	800	ps
	HD Rise/Fall Time (20–80%)	1, 3	—	100	180	ps
t_r/t_{fMM}	Rise/fall mismatch (HD Rate)	1, 2	—	10	30	ps
	Rise/fall mismatch (SD Rate)	1, 2	—	40	100	ps
V_{OD}	Single-ended voltage swing range (sw) p–p	1, 2, 4, 5	500	800	1600	mV
V_{ODTOL}	Swing Level output variation at 800 mVp–p [**RSET** = 750Ω ±1%] (Single-Ended)	1, 2, 3	-7	—	+7	%
V_{OS}	Overshoot/Undershoot	1, 2	-8	—	+8	%
JAO_{PP}	Additive Output Jitter (HD rate 1010 pattern)	1, 8	—	20	30	ps
	Additive Output Jitter (SD rate 1010 pattern)	1, 8	—	40	60	ps

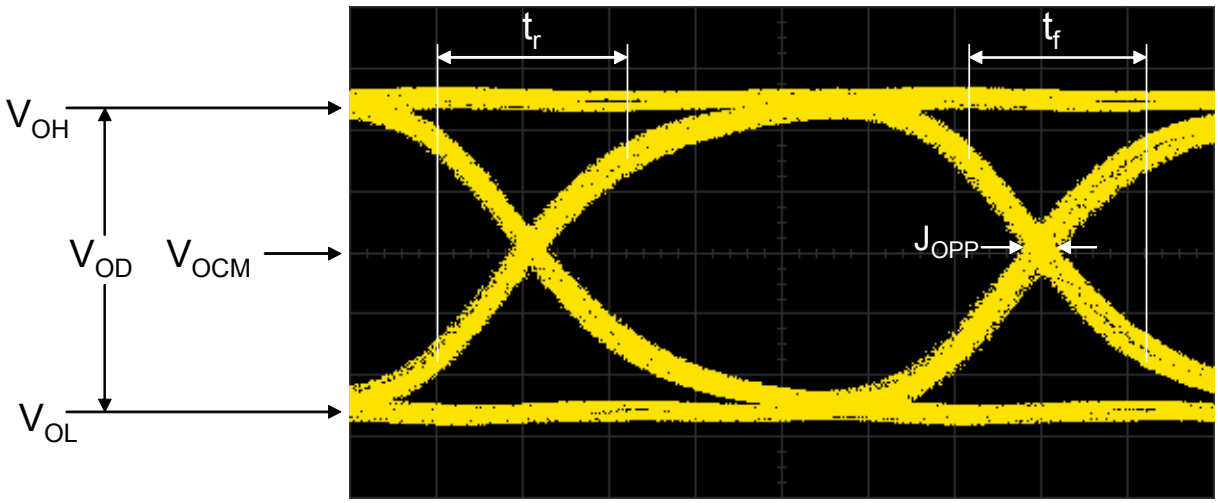
Table 1-7. Cable Driver Output Electrical Specifications M21218 (SD/HD) (2 of 2)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Unit
DCD_O	Duty Cycle Distortion (HD Rate)	1, 2, 6, 8	—	15	30	ps
	Duty Cycle Distortion (SD Rate)	1, 2, 6, 8	—	20	70	ps
S_{22}	Output Return Loss (5 MHz to 1.5 GHz)	1, 2, 7	15	—	—	dB

NOTES:

1. Entire table specified at recommended operating condition with 400 mVp–p differential input—see Table 1-2.
2. Specification verified at 800 mVpp output with 1m cable on MACOM test board. System results may vary.
3. Rated at nominal SMPTE 800 mV output swing level (using a 750Ω ±1% resistor at RSET).
4. Output stage is an open collector differential pair, actual swing dependant on IC supply voltage and external termination voltage.
5. Into 75Ω back termination and 75Ω load and appropriate external termination voltage.
6. Duty Cycle Distortion (DCD) is defined as the difference in the intrinsic jitter at the 50% voltage level and the intrinsic jitter at the rising/falling edge crossing point. If the rising/falling edge crossing point is at the 50% voltage level, then DCD = 0.
7. Measured under DC conditions that simulate AC coupling, V_T = 3.3V.
8. Measured using a “1010” data pattern.

Figure 1-1. Output Symbols Definition



V_{OH}: Average voltage high level
V_{OL}: Average voltage low level
V_{OD}: (VOH) – (VOL)
V_{OCM}: Common Mode Voltage
J_{OPP}: Output Jitter Peak-Peak
t_r: 20-80% Rise Time
t_f: 80-20% Fall Time

NOTE: Waveform above is differential.

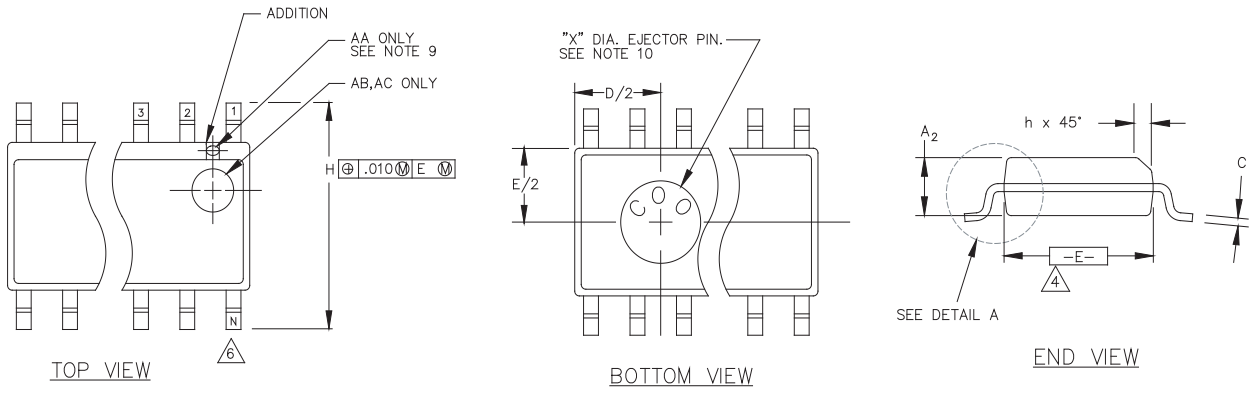
1.5 Package Specification

1.5.1 Mechanical Description

1.5.1.1 Package Information

The M21218 is available in a 8 pin, RoHS compliant, SOIC package. The package drawing is shown in Figure 1-2.

Figure 1-2. Package Drawing



NOTES:
1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M – 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES AT END AND .010 INCHES AT WINDOW
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.
10. COUNTRY OF ORIGIN LOCATION ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. CONTROLLING DIMENSION: INCHES.
12. THIS PART IS COMPLIANT WITH JEDEC STANDARD MS-012, VARIATION AA, AB & AC.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.061	.064	.068		AA	.189	.194	.196	8
A_1	.004	.006	.0098		AB	.337	.342	.344	14
A_2	.055	.058	.061		AC	.386	.391	.393	16
B	.0138	.016	.0192						
C	.0075	.008	.0098						
D	SEE VARIATIONS			3					
E	.150	.155	.157						
e	.050 BSC								
H	.230	.236	.244						
h	.010	.013	.016						
L	.016	.025	.035						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	1.55	1.63	1.73		AA	4.80	4.93	4.98	8
A_1	0.127	0.15	0.25		AB	8.58	8.69	8.74	14
A_2	1.40	1.47	1.55		AC	9.80	9.93	9.98	16
B	0.35	0.41	0.49						
C	0.19	0.20	0.25						
D	SEE VARIATIONS			3					
E	3.81	3.94	3.99						
e	1.27 BSC								
H	5.84	5.99	6.20						
h	0.25	0.33	0.41						
L	0.41	0.64	0.89						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						

2.0 Functional Description

2.1 General Nomenclature

Through out this data sheet, physical pins will be denoted in **BOLD** print.

2.2 Features

2.2.1 HD-SDI and SD-SDI Slew-rate Selection

The output slew rate of the M21218 is selectable to conform with the different SD-SDI and HD-SDI specifications. With **SD/HD** = Low, the high-definition (1485 Mbps) slew rate is typically 100 ps. The slew rate will vary depending on the output matching network and BNC connector used.

With **SD/$\overline{\text{HD}}$** = High, for standard definition (143 to 540 Mbps) applications, the slew rate is typically 600 ps, which is compliant with SMPTE 259M and SMPTE 344M. The M21208 has no control over slew rate; this is set at the SD requirement.

2.2.2 Output Amplitude Adjustment

For SMPTE compliance, an external 750Ω ±1% resistor at **RSET** to $\mathbf{AV_{DD}}$ is recommended for a swing level of 800 mV within a tolerance that is less than ±7%. The output amplitude can also be adjusted to range from 500 to 1600 mV using the following formula:

Output Swing = (600 / **RSET)** mVp–p [**RSET** in kΩ] (in mVpp, single-ended)

The actual swing is set as a function of the IC supply voltage and external termination voltage as shown in Table 2-1. For a 3.3V minimum termination voltage, the IC can be SMPTE compliant for all supply voltages. In applications where a lossy matching or splitting networks are used, the M21208/M21218 offers additional gain for up to 1600 mV output swings, so the output after the lossy network can be SMPTE compliant. For single-supply 3.3V operation, the swing range is compatible with the GS9068/GS9068A and GS1528/1528A.

Table 2-1. Output Swing vs. Supply and Termination Voltage

AV_{DD} (V)	AV_{DDTERM} (V)*	Maximum Swing (Single-ended mVp–p)	Minimum Swing (Single-ended mVp–p)
2.5–3.3V	3.3V	1200 mV	500 mV
2.5–3.3V	5.0V	1600 mV	500 mV
* ±5% tolerance allowed for AV_{DDTERM}.			

2.3 Pin Definitions

2.3.1 High-speed Inputs

The M21208/M21218 are designed to be operated with input signals as low as 100 mV or up to 2000 mV differential peak to peak. The M21218 requires external termination resistors to minimize high-speed reflections. The M21208 and M21218 are designed as pin compatible replacements to the GS9068/9068A and GS1528/1528A cable drivers, respectively, and the recommended input circuits are shown in Figure 2-1 and 2-2.

Figure 2-1. Typical Input Circuit—AC Coupled

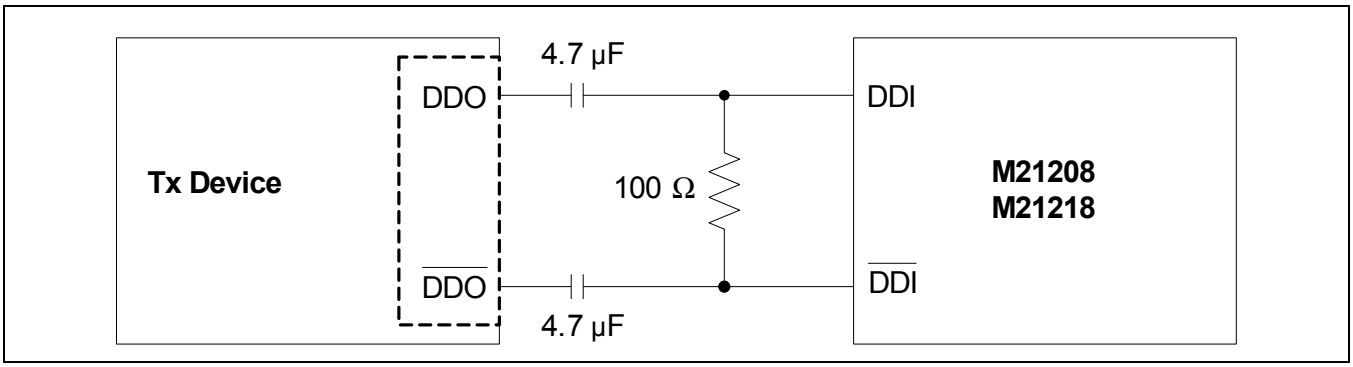
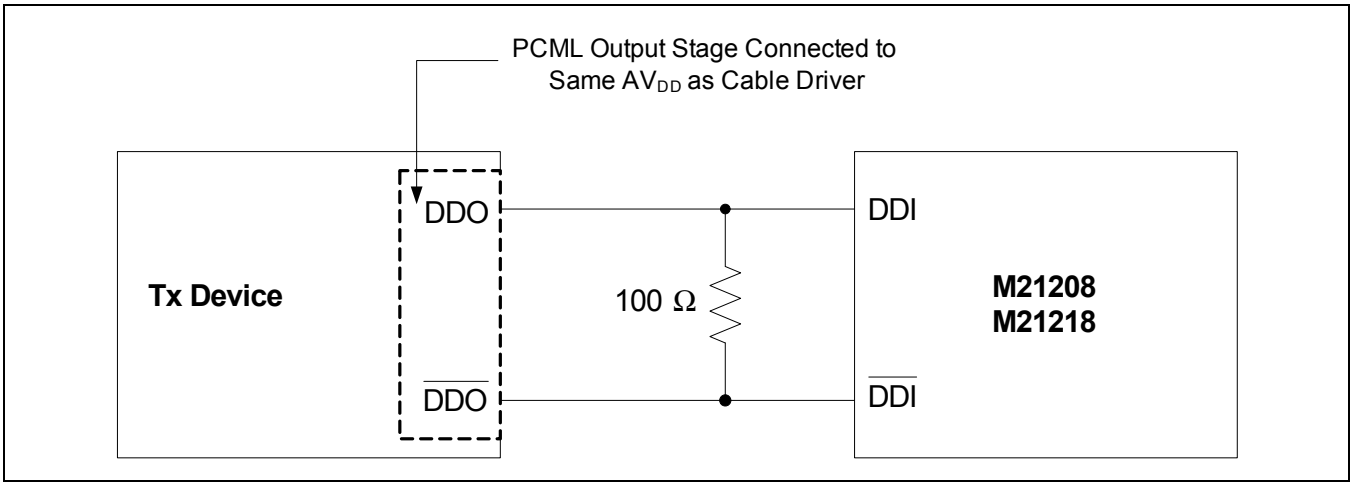


Figure 2-2. Typical Input Circuit—DC Coupled

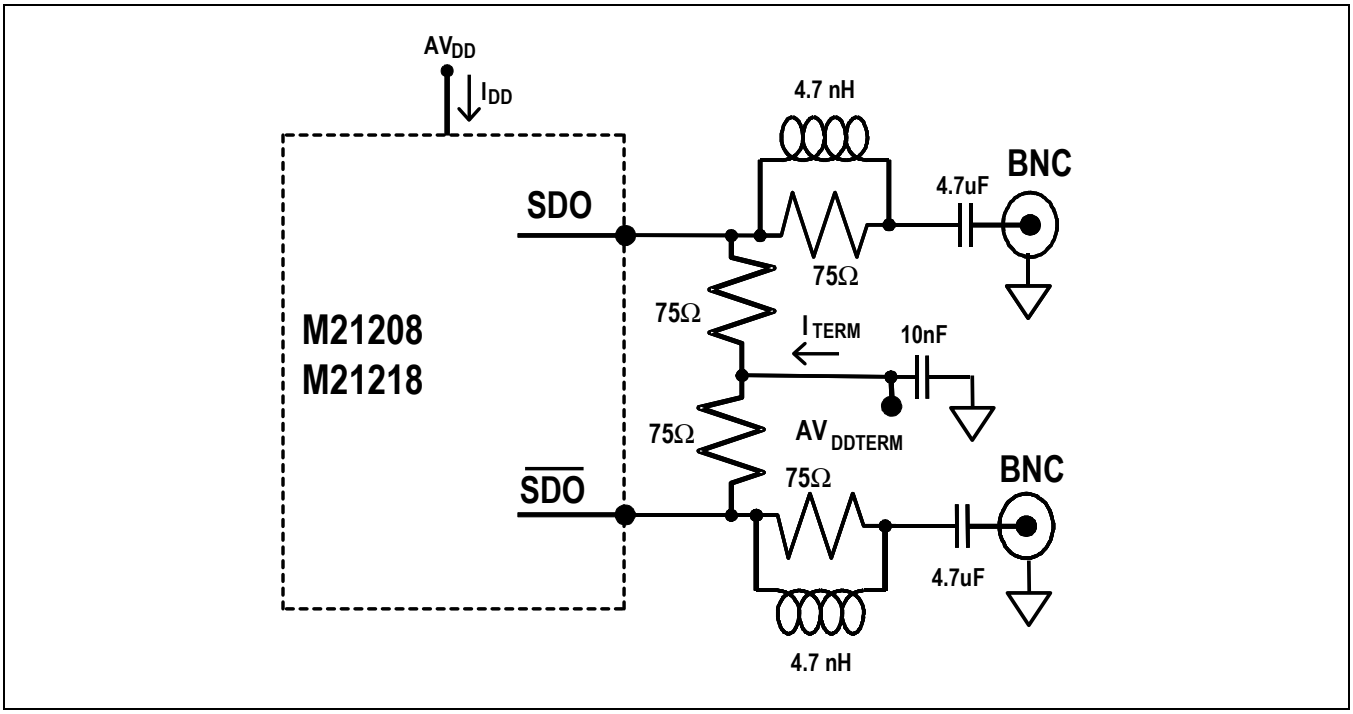


2.3.2 High-speed Outputs

The M21208/M21218 output buffer is an open collector buffer that is designed for typical return loss of 15dB using standard through-hole BNC connectors as typically employed with the GS9068/GS1528 series recommended back-termination and matching circuit as shown in Figure 2-3. The Output Return Loss (ORL) may be further optimized by using a different output matching network or component values and may vary with PCB layout or component selection. The output return loss of the M21208/M21218 is measured while forcing the outputs to a DC high or low state. Under normal operating conditions, the outputs of the M21208/M21218 will not be held to a static high or low state, so the measured output return loss will not represent the actual output return loss under normal operating conditions. To estimate the output return loss performance under typical operating conditions, an interpolation can be performed on the measured values for the output high condition and output low condition. The equations used for the interpolation are as follows:

RcH = RmH - (RmH - RmL) / 4 and
RcL = RmL + (RmH - RmL) / 4
RcH = Corrected ORL with output high
RcL = Corrected ORL with output low
RmH = Measured ORL with output stuck high
RmL = Measured ORL with output stuck low

Figure 2-3. Typical Output Matching/Back-termination circuit



2.3.3 M21208/M21218 Pin List

Table 2-2. Interface Pins

Pin Name	Function	Default	Type
SD/$\overline{\text{HD}}$ (M21218 only)	Input control signal to change the output slew rate. **SD/$\overline{\text{HD}}$** = High: Slow output slew rate for SD-SDI rate (143–540 Mbps). **SD/$\overline{\text{HD}}$** = Low: Fast output slew rate for HD-SDI rate (1485 Mbps) [Default].	Pull-up	I—CMOS
RSET	Input control signal for setting the single-ended output swing amplitude. Terminal floating results in 800 mVpp ± 15% swing. Higher output swing levels or reduced variations with a ±1% tolerance external resistor. For 800 mVpp single-ended, a 750Ω ±1% resistor to AV_{DD} is recommended.	—	Analog Input
NOTE: Internal pull-down is 100 kΩ.			

Table 2-3. Power Pins

Pin Name	Function	Type
AV_{SS}	Chip Ground	Power
AV_{DD}	Positive Supply	Power

Table 2-4. High-speed Signal Pins

Pin Name	Function	Default	Type
SDI/$\overline{\text{SDI}}$	Non-inverting and Inverting serial unterminated inputs.	—	I—High-speed
SDO/$\overline{\text{SDO}}$	Non-inverting and inverting serial unterminated data outputs to coaxial cable.	—	O—High-speed

Figure 2-4. M21208 Pin Out

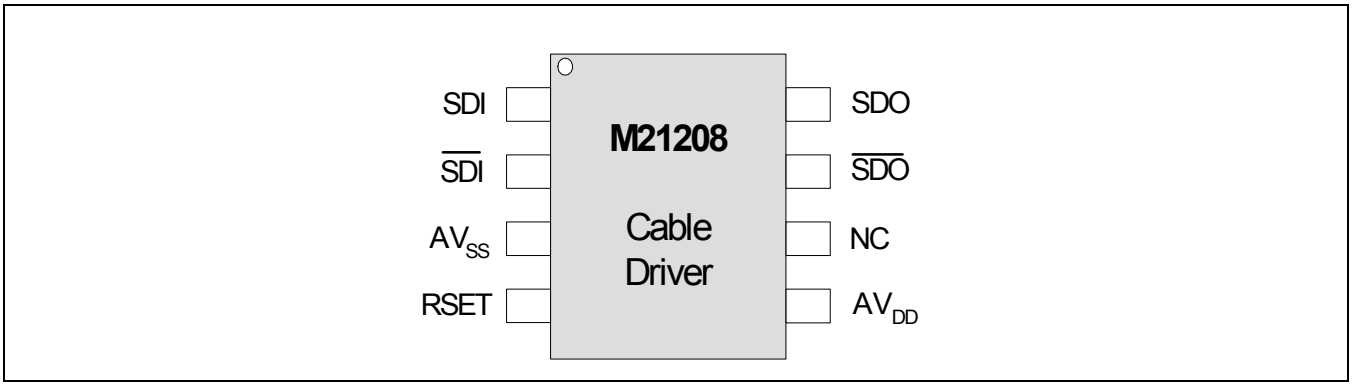
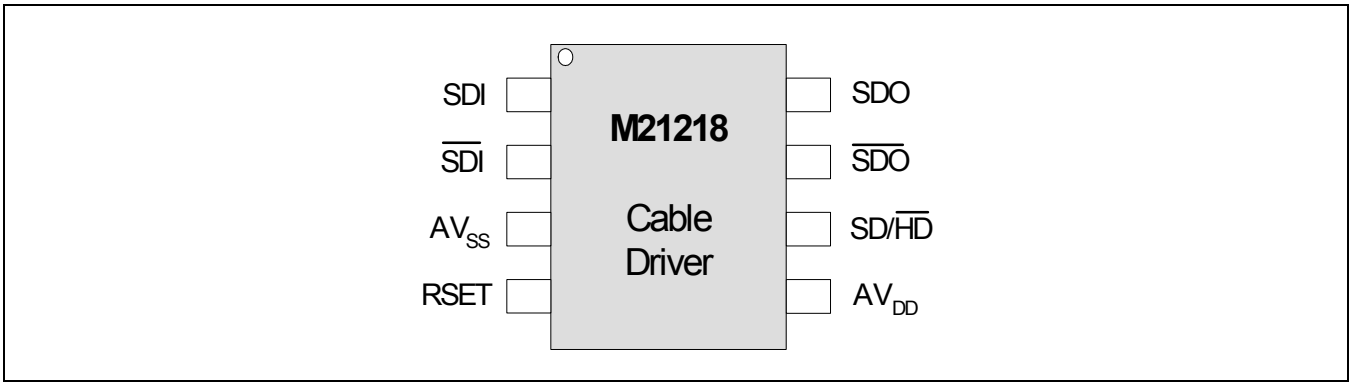


Figure 2-5. M21218 Pin Out



Appendix

A.1 Glossary of Terms/Acronyms

Table A-1. Glossary and Acronyms

DTV	Digital Television
DVB	Digital Video Broadcast
EQ	Equalizer or Equalization
HD	High Definition
SD	Standard Definition
SDI	Serial Digital Interface
SMPTE	Society of Motion Picture and Television Engineers

A.2 Reference Documents

A.2.1 External

Society of Motion Picture and Television Engineers

SMPTE 292M Bit—Serial Digital Interface for High-Definition Television Systems

SMPTE 259M 10—Bit 4:2:2 Component and 4f_{SC} Composite Digital Signals—Serial Digital Interface

SMPTE 344M 540Mb/s Serial Digital Interface

DVB Digital Video Broadcast (ASI)

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