THE DATASHEET OF

M02096G-12

M02095/6

3.3/5V Laser Driver / Limiting Amplifier for Operation to 2.5 Gbps

The M02095 and M02096 are integrated laser drivers and limiting amplifiers for applications to 1.25 Gbps and 2.5 Gbps, respectively. The laser driver modulation output can be AC or DC coupled to an FP/DFB laser. The devices can operate from a 3.3V or 5V supply.

The devices include monitors for bias and laser power. Integrated safety circuitry provides latched bias and modulation current shutdown if a fault condition is detected and provides an internal V_{CC} switch.

The limiting amplifier also includes a programmable signal-level detector, allowing the user to set thresholds at which the logic outputs are enabled. PECL or CML outputs are available on the limiting amplifier.

Configuration logic provides flexibility in setting data path polarity, safety logic configuration, and LOS behavior.

Applications

- 2.5 Gbps STM-16/OC-48 SDH/SONET (M02096)
- 1.06 and 2.12 Gbps Fibre Channel (M02095/6)
- 1.25 Gbps Ethernet (M02095/6)
- 1.25 Gbps SDH/SONET (M02095/6)
- 2.67 Gbps SDH/SONET with FEC (M02096)
- SDH/SONET 155 Mbps Transceivers
- FTTx and Media Converters

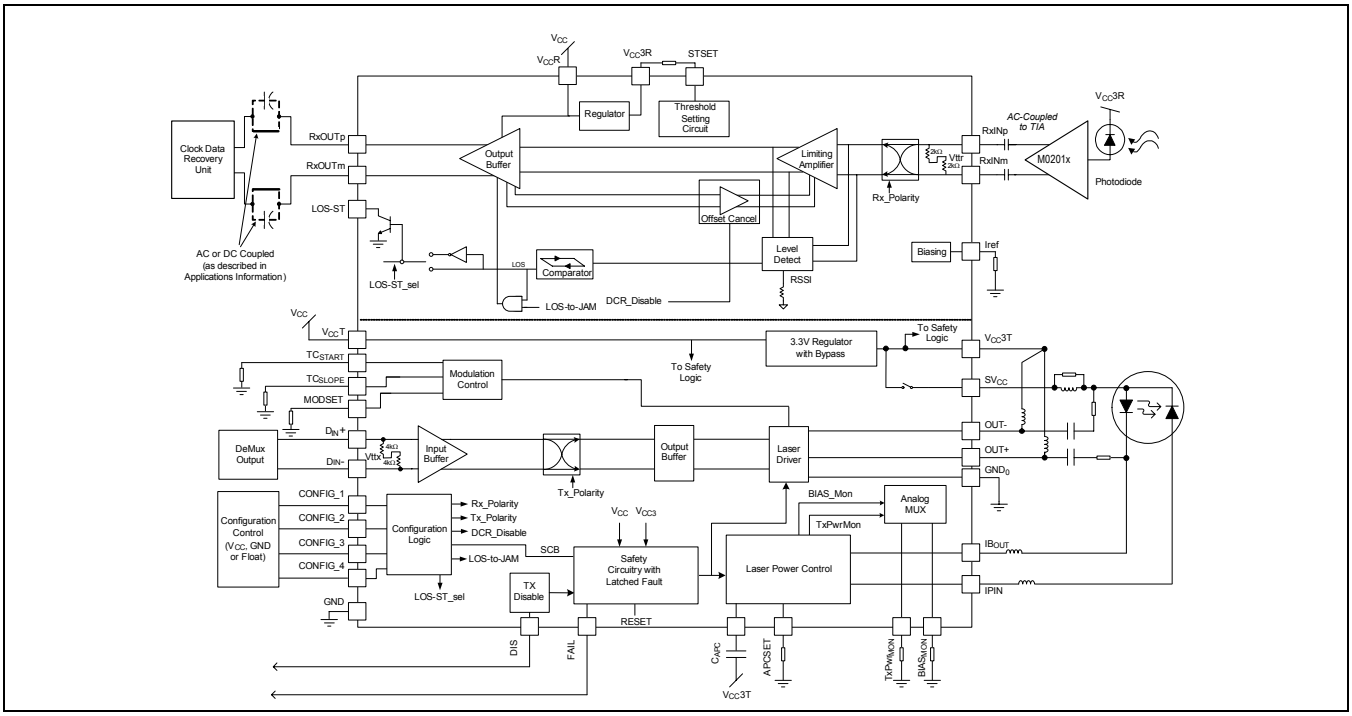
Features

- High speed operation; suitable for applications to 2.5 Gbps. 55 ps typical rise/fall time into 25Ω
- Independently programmable bias and modulation currents Modulation current to 85 mA and bias current to 100 mA

Features (con't)

- Integrated power supply switch for redundant shutdown under a fault condition
- Temperature compensation for modulation current
- Automatic Power Control
- SFP compliant safety circuitry (configurable)
- 3.3 mV typical input limiting amp sensitivity at 2.5 Gbps
- CML or PECL limiting amplifier outputs
- Limiting amplifier includes integrated DC offset cancellation circuit
- Polarity Control for both the driver and limiting amplifier data paths
- Operates with 3.3V or 5V supply with an internal auto-sensing regulator that enables with 5V supplies and is bypassed with 3.3V supplies
- Powers 3.3V ROSAs from its Receiver Regulator output enabling true 3.3/5V designs using all 3.3V Mindspeed TIAs

M02095/6 Typical Applications Diagram



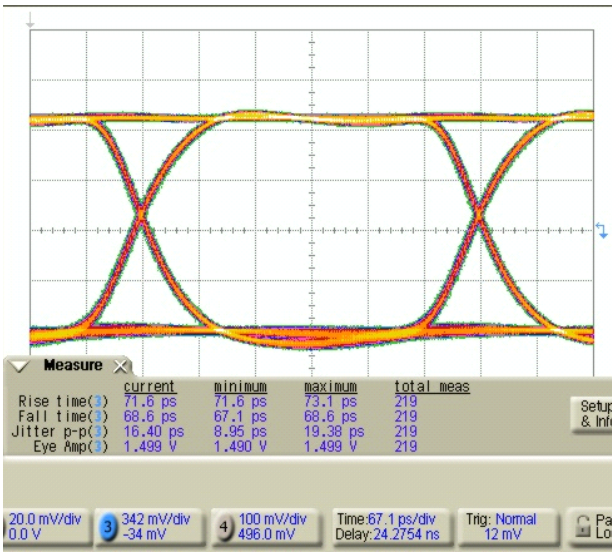
Ordering Information

Part Number	Package	Operating Temperature
M02095G-XX*	QFN32	–40°C to 95°C
M02096G-XX*	QFN32	–40°C to 95°C
* The letter “G” designator after the part number indicates that the device is RoHS-compliant. Refer to www.mindspeed.com for additional information.		

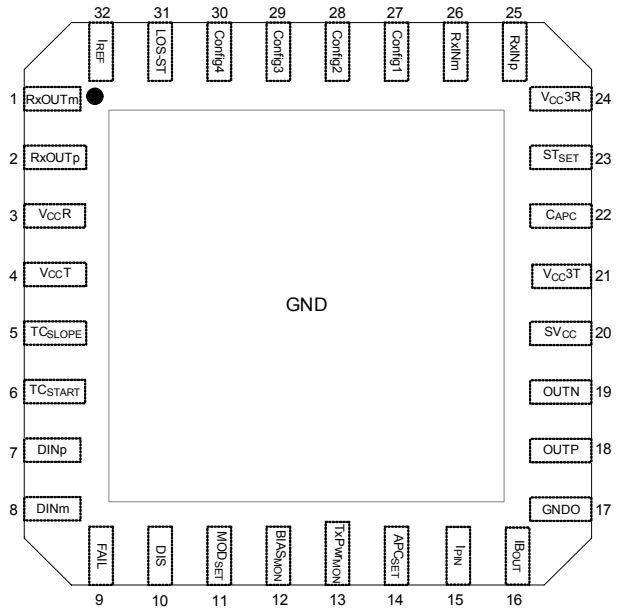
Revision History

Revision	Level	Date	ASIC Revision	Description
E	Release	August 2007	-12	Finalize limiting amplifier jitter specifications, combine laser driver and limiting amplifier supply current together in Table 1-3.
D	Preliminary	May 2007	-12	Add TxPwrMon and $BIAS_{MON}$ pins to device. Update DC specifications, Functional Description and Applications Information.
C	Preliminary	November 2006	-11	Reflect current device pinout.
B	Advance	August 2006	-11	Update several specifications based on initial device evaluation.
A	Advance	June 2006	NA	Initial Release.

M02096 2.5 Gbps Laser Driver Eye Diagram



M02095/6 Pin Configuration



1.0 Product Specification

1.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage	-0.4 to +6.0	V
$V_{CC}3$	3.3V power supply voltage (when $V_{CC}3$ is connected to V_{CC})	-0.4 to +4.0	V
T_{STG}	Storage temperature	-65 to +150	°C
IB_{OUT_MAX}	Maximum bias output current at IB_{OUT}	140	mA
I_{MOD_MAX}	Maximum modulation current	120	mA

1.2 Recommended Operating Conditions

Table 1-2. Recommended Operating Conditions

Parameter	Rating	Units
Power supply: (V_{CC}-GND) (apply no potential to $V_{CC}3$) or ($V_{CC}3$-GND) (connect V_{CC} to same potential as $V_{CC}3$)	+4.7 to 5.5V or +3.3V ± 7.5%	V
Junction temperature	-40 to +125	°C
Operating ambient	-40 to +95	°C

1.3 DC Characteristics

1.3.1 Device Power

V_{CC} = 3.05 to 3.55V or 4.7 to 5.5V, T_A = -40°C to +95°C, unless otherwise noted.
Typical values are V_{CC} = 3.3V, IB_{OUT} = 20 mA, I_{MOD} = 30 mA.

Table 1-3. Device Power

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{CC}	V_{CC} (sum of $V_{CC}T$ and $V_{CC}R$) supply current	Using external 3.3V supply V_{CC} = 3.3V (1) With CML Outputs (M02096)	–	68	96	mA
		With PECL Outputs (M02095 - includes PECL load)	–	93	108	
		Additional current when operating from 5V supply (2)	–	4	–	

NOTES:

1. Excludes bias and modulation currents delivered to the laser. Maximum supply current based on maximum settings for bias and modulation.
2. Bias and modulation currents add directly to power supply current in 5V applications; additional supply current noted excludes these currents.

1.3.2 DC Electrical Characteristics - Laser Driver

V_{CC} = 3.05 to 3.55V or 4.7 to 5.5V, T_A = -40°C to +95°C, unless otherwise noted.
Typical values are V_{CC} = 3.3V, IB_{OUT} = 20 mA, I_{MOD} = 30 mA.

Table 1-4. DC Electrical Characteristics - Laser Driver

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{CC}3THL$	3.3V supply detection (low voltage) threshold (1)		2.5	2.8	3.05	V
$V_{CC}3HH$	3.3V supply detection (high voltage) threshold (1)		3.65	3.95	4.2	V
$V_{CC}5THL$	5V supply detection (low voltage) threshold		3.9	4.35	4.7	V
$V_{CC}5THH$	5V supply detection (high voltage) threshold		5.5	–	–	V
V_{MODSET}	Modulation current ref.	Voltage reference for MOD_{SET}	1.1	1.25	1.4	V
V_{APCSET}	Automatic power control loop voltage reference	Voltage at APC_{SET} with APC loop operational	0.90	1.20	1.4	V
V_{FAULTL}	Low fault voltage detection threshold (IB_{OUT}, OUTP, C_{APC}, IPIN, MOD_{SET}, APC_{SET})	Fault condition occurs when voltage drops below this level	–	100	200	mV
V_{FAULTH}	High fault voltage detection threshold (IPIN)	Fault condition occurs when voltage goes above this level (2)	$V_{CC}3T$ - 0.2	$V_{CC}3T$ - 0.1	–	V
V_{SELFL}	Self-biased voltage for IB_{OUT} and OUTP	During disable condition	0.5	1.65	2.0	V

Table 1-4. DC Electrical Characteristics - Laser Driver

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{BIAS}	Bias current adjust range	At IB_{OUT}. V_{IBOUT} > 0.7V	1	–	100	mA
$I_{BIAS(OFF)}$	Bias current with output disabled	DIS = high $V_{IBOUT} = V_{CC}3$	–	–	150	µA
	Ratio of bias output current to APC_{SET} current	= I_{BIAS} / I_{APCSET} in open loop operation	–	90	–	A/A
	Ratio of bias current to $BIAS_{MON}$ current	= I_{BIAS} / $I_{BIASMON}$	79	89	99	A/A
V_{MD}	Monitor diode reverse bias voltage		1.5	2	–	V
I_{MD}	Monitor diode current adjustment range	For stable APC loop operation in closed loop mode	10	–	1500	µA
	Ratio of $TxPwr_{MON}$ current to monitor diode current	Across range of I_{MD}	0.8	1	1.2	A/A
C_{MDMAX}	Maximum monitor photodiode capacitance	For loop stability; includes any additional parasitic capacitance	–	–	100	pF
VIH_DIS	TTL/CMOS input high voltage (DIS)		2.0	–	–	V
VIL_DIS	TTL/CMOS input low voltage (DIS)		–	–	0.8	V
VIH_CFG	Configuration logic input high voltage (Config1 - 4) (2)		$V_{CC}3T$ - 0.5	–	–	V
VIL_CFG	Configuration logic input low voltage (Config1 - 4) (2)		–	–	0.5	V
VOH_FAIL	Logic output high voltage (FAIL)	With external 10 kΩ pull-up to V_{CC}	V_{CC} - 0.6	–	–	V
VOL_FAIL	Logic output low voltage (FAIL)	I_{OL} = 0.8 mA	–	–	0.4	V
R_{IN}	Differential input resistance	Transmitter Data inputs	–	7.5	–	kΩ
V_{CMSELF}	Self-biased common mode input voltage	Data inputs floating	–	$V_{CC}3T$ - 1.3	–	V
V_{INCM}	Common-mode input compliance voltage	Transmitter Data inputs	$V_{CC}3T$ - 1.5	–	$V_{CC}3T$ - $V_{IN(Diff)}/4$	V
$V_{IN(Diff)}$	Differential input voltage	= 2*($DINp_{HIGH}$ – $DINp_{LOW}$)	200	–	2400	mV

NOTES:

1. $V_{CC}3$ supply okay circuitry monitors internally regulated voltage when only the +5V supply is used (V_{CC} = 5V).
2. Input is 3.3V tolerant logic.

1.3.3 DC Electrical Characteristics - Limiting Amplifier

$V_{CC}R$ = 3.05 to 3.55V or 4.7 to 5.5V, T_A = -40°C to +95°C, unless otherwise noted.
Typical values are V_{CC} = 3.3V, 25°C.

Table 1-5. DC Electrical Characteristics - Limiting Amplifier

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{AMP_CML}	CML Output Amplitude	Single ended, 50Ω load to V_{CC}; 10 mV_{PP} input (M02096)	280	500	–	mV_{PP}
$V_{OUTL}PECL$ (1)	PECL Output Low Voltage (RxOUTm, RxOUTp)	Single ended; 50Ω load to V_{CC} - 2V (M02095)	V_{CC} - 1.88	V_{CC} - 1.71	V_{CC} - 1.60	V
$V_{OUTH}PECL$ (1)	PECL Output High Voltage (RxOUTm, RxOUTp)	Single ended; 50Ω load to V_{CC} - 2V (M02095)	V_{CC} - 1.09	V_{CC} - 0.95	V_{CC} - 0.88	V
V_{AMP_PECL}	PECL Output Amplitude	Single ended; 50Ω load to V_{CC} - 2V (M02095)	–	740	–	mV_{PP}
R_{IN}_DIFF	Differential Input Resistance		–	4.5	–	kΩ
R_{OUT}_DIFF	Differential Output Resistance	CML Outputs (M02096)	170	200	230	Ω
$V_{OUTL}LOS$	LOS Output High Voltage	Open collector, 4.7 - 10 kΩ pull up to V_{CC}	2.4	–	V_{CC}	V
$V_{OUTH}LOS$	LOS Output Low Voltage	I_{OL} = 0.8 mA	–	–	0.4	V

NOTES:

1. PECL level requirements apply from 0°C to 95°C.

1.4 AC Characteristics

1.4.1 AC Electrical Characteristics - Laser Driver

$V_{CC}T$ = 3.05 to 3.55V or 4.7 to 5.5V, T_A = -40°C to +95°C, unless otherwise noted.
Typical values are V_{CC} = 3.3V, IB_{OUT} = 20 mA, I_{MOD} = 30 mA.

Table 1-6. AC Electrical Characteristics - Laser Driver

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{MOD}	Modulation current adjust range	To meet AC specifications (1, 2)	8	–	85	mA_{PP}
$I_{MOD(OFF)}$	Modulation current with output disabled	DIS = high	–	–	150	µA
	Ratio of modulation current to MOD_{MON} current (3)		–	75	–	A/A
	Ratio of modulation current to MOD_{SET} current		–	110	–	A/A
I_{MOD-TC}	Programmable range for modulation current temperature coefficient	Adjustable using TC_{SLOPE}	0	–	10^4	ppm/°C
T_{TCSTRT}	Programmable temperature range at which modulation current TC compensation enables	Based on value set for TC_{START}	–	0 (4) - 95	–	°C

Table 1-6. AC Electrical Characteristics - Laser Driver

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
t_R / t_F	Modulation output rise / fall times	20% to 80% into 25Ω load. Measured using alternating 1111-0000 pattern at 2.5 Gbps M02095; 25Ω load M02096; 25Ω load	 – –	 72 65	 95 85	ps
OS	Overshoot of modulation output	Into 25Ω load, off direction	–	3	–	%
		Into 25Ω load, on direction	–	7	–	
RJ	Random jitter		–	1.0	–	ps_{RMS}
DJ	Modulation output deterministic jitter	into 25Ω load (includes pulse width distortion) K28.5 pattern at 1.25 Gbps (M02095) 2^{23} - 1 PRBS at 2.7 Gbps (M02096))	 – –	 22 15	 40 30	ps_{PP}

NOTES:

1. Minimum voltage at OUTP > 0.7 V; laser forward voltage and total series resistance must be considered if output is DC coupled to laser.
2. AC specifications apply across this range of mod current.
3. MOD_{MON} is accessible using Special Configuration 3 (SC3), see Table 4-3.
4. Default if TC_{START} is floating.

1.4.2 AC Electrical Characteristics - Limiting Amplifier

$V_{CC}R$ = 3.05 to 3.55V or 4.7 to 5.5V, T_A = -40°C to +95°C, unless otherwise noted.

Table 1-7. AC Electrical Characteristics - Limiting Amplifier

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{IN(MIN)}$	Minimum Differential Input Sensitivity	BER < 10^{-12} at 2.5 Gbps with 2^{23}-1 PRBS (M02096)	–	3.3	6	mV_{PP}
		BER < 10^{-12} at 1.25 Gbps with K28.5 pattern (M02095)	–	2	4	
$V_{I(MAX)}$	Input Overload	BER < 10^{-12}, differential input	1200	–	–	mV_{PP}
		BER < 10^{-12}, single-ended input	600	–	–	
V_N	RMS Input Referred Noise	M02096	–	–	425	μV_{RMS}
		M02095	–	–	285	
V_{LOS}	LOS Programmable Range	Differential inputs, 6.04 kΩ ≤ R_{STSET} ≤ 8.06 kΩ (M02096) 6.04 kΩ ≤ R_{STSET} ≤ 8.25 kΩ (M02095)	–	 8 - 60 7 - 60	–	mV
HYS	Signal Detect Hysteresis	(electrical); signal detect level set to 20 mV_{PP}	2	4	6	dB
RSSIpp	Peak-to-peak received signal strength indicator range		4	–	100	mV
BW_{LF}	Small-Signal -3dB Low Frequency Cutoff.	Excluding AC coupling capacitors	–	4	–	kHz
DJ	Deterministic Jitter	Differential, 10 mV_{PP} input, 2^{15}-1 PRBS 2.5 Gbps (M02096) 1.25 Gbps (M02095)	 – –	 20 20	 48 70	ps

Table 1-7. AC Electrical Characteristics - Limiting Amplifier

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
RJ	Random Jitter	10 mV_{PP} input	–	3.8	–	ps_{RMS}
t_r / $t_{f2.5G}$	Data Output Rise and Fall Times	M02096 20% to 80%; outputs terminated into 50Ω; 10 mV_{PP} input	–	90	150	ps
t_r / $t_{f1.25G}$	Data Output Rise and Fall Times	M02095 20% to 80%; outputs terminated into 50Ω; 10 mV_{PP} input	–	160	250	ps
T_{LOS_ON}	Time from LOS state until LOS output is asserted	LOS assert time after 1 V_{PP} input signal is turned off; signal detect level set to 10 mV	2.3	–	80	µs
T_{LOS_OFF}	Time from non-LOS state until LOS is deasserted	LOS deassert time after input crosses signal detect level; signal detect set to 10 mV with applied input signal of 20 mV_{PP}	2.3	–	80	µs

1.5 Safety Logic Timing

V_{CC} = 3.05 to 3.55V or 4.7 to 5.5V, T_A = -40°C to +95°C, unless otherwise noted.
Typical values are V_{CC} = 3.3V, IB_{OUT} = 20 mA, I_{MOD} = 30 mA.

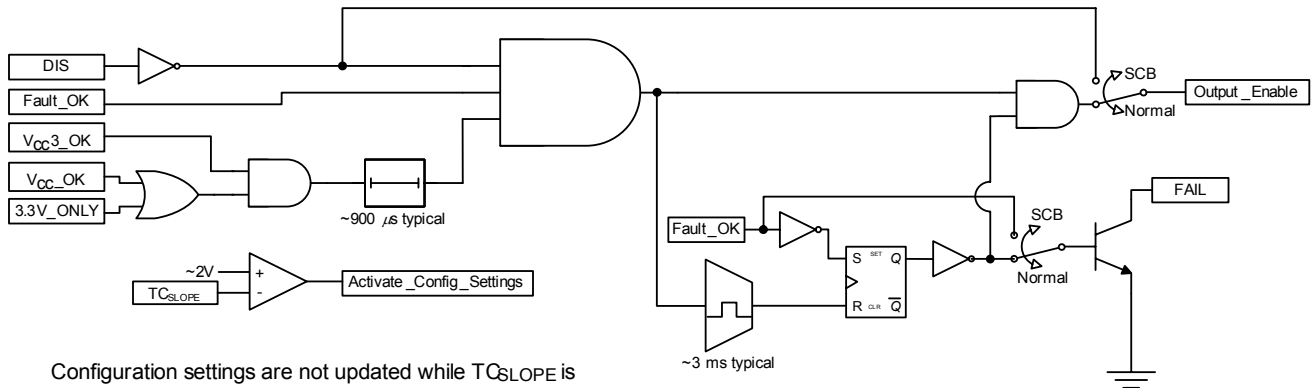
Table 1-8. Safety Logic Timing

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
t_off	DIS assert time	Rising edge of DIS to fall of output signal below 10% of nominal (1)	–	1	10	µs
t_on	DIS negate time	Falling edge of DIS to rise of output signal above 90% of nominal (1)	–	0.4	1	ms
t_init	Time to initialize	Includes reset of FAIL; from power on after Supply_OK or from negation of DIS during reset of FAIL condition	–	4	300	ms
t_wc	Window comparator hold-off time	Time during which the status of the fault detect comparators is ignored.	2	3	–	ms
t_fault	Laser fault time -- from fault condition to assertion of FAIL	From occurrence of fault condition or when Supply_OK is beyond specified range	–	16	100	µs
t_reset	DIS time to start reset	DIS pulse width required to initialize safety circuitry or reset a latched fault	–	–	10	µs
t_{VCC-OK}	Supply okay delay time	Delay between supply_OK condition and when outputs are enabled	–	900	–	µs

NOTE:

1. With C_{APC} = 47 nF.

Figure 1-1. Safety Logic Simplified Block Diagram



Configuration settings are not updated while TC_{SLOPE} is pulled high, but are updated when TC_{SLOPE} is at normal level

* Fault_OK indicates that no fault is detected at any of the fault sense nodes

Table 1-9. Circuit Response to Single-Point Fault Conditions on Driver Pins

Pin Name	Circuit Response to Over-voltage Condition or Short to V_{CC}	Circuit Response to Under-Voltage Condition or Short to Ground
Config1-4	Does not affect output power (some conditions can selectively enable/disable driver output).	Does not affect output power (some conditions can selectively enable/disable driver output).
V_{CC}	Outputs are disabled if V_{CC} exceeds the V_{CC}_okay (high level) threshold. If so, FAIL will be asserted. (1)	Outputs are disabled if V_{CC} voltage is below the V_{CC}_okay (low level) threshold. If so, FAIL will be asserted. (1)
$V_{CC}3T$	Outputs are disabled if $V_{CC}3$ exceeds the $V_{CC}3$_okay (high level) threshold. If so, FAIL will be asserted. (1)	Outputs are disabled if $V_{CC}3$ voltage is below the $V_{CC}3$_okay (low level) threshold. If so, FAIL will be asserted. (1)
DINp, DINm	The APC loop will attempt to compensate for the change in output power. If the APC loop can not maintain the set average power, a fault state occurs. (2,3)	The APC loop will attempt to compensate for the change in output power. If the APC loop can not maintain the set average power, a fault state occurs. (2,3)
C_{APC}	A fault state occurs.(2)	Laser bias current will be shut off, then a fault state occurs. (2)
FAIL	Does not affect laser operation.	Does not affect laser operation.
DIS	Bias and modulation outputs are disabled and SV_{CC} is opened.	Does not affect laser power (normal condition for circuit operation).
MOD_{SET}	No modulation current. APC loop will adjust output power if DC coupled to laser.	A fault state occurs. (2)
APC_{SET}	Laser output power is reduced (if the modulation outputs DC coupled to laser) or turned off (if the modulation outputs AC coupled to laser). A fault state may occur. (2)	A fault state occurs. (2)
TC_{START}	Modulation current may increase depending on operating temperature and TC_{SLOPE} setting. APC loop will adjust for change in output power if modulation outputs are DC coupled to laser.	Modulation current may decrease depending on operating temperature and TC_{SLOPE} setting. APC loop will adjust for change in output power if modulation outputs are DC coupled to laser.
TC_{SLOPE}	Modulation current may decrease depending on operating temperature and TC_{START} setting. APC loop will adjust for change in output power if modulation outputs are DC coupled to laser.	Modulation current may increase depending on operating temperature and TC_{START} setting. APC loop will adjust for change in output power if modulation outputs are DC coupled to laser.

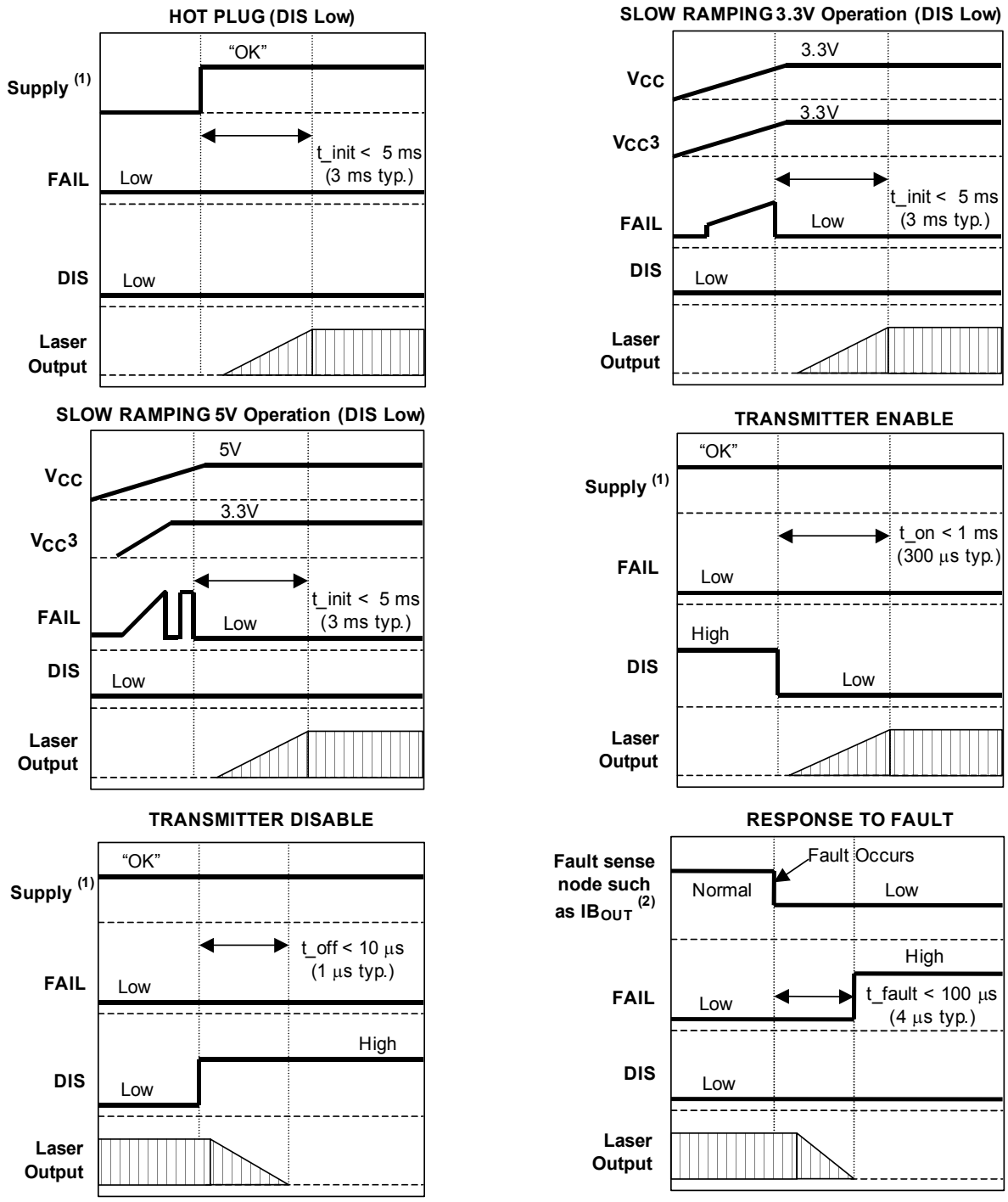
Table 1-9. Circuit Response to Single-Point Fault Conditions on Driver Pins

Pin Name	Circuit Response to Over-voltage Condition or Short to V_{CC}	Circuit Response to Under-Voltage Condition or Short to Ground
$BIAS_{MON}$, $TxPwr_{MON}$	Does not affect laser operation.	Does not affect laser operation.
I_{PIN}	A fault state occurs. (2,4)	A fault state occurs. (2,4)
IB_{OUT}	The laser is turned off and a fault state may occur. (2)	A fault state occurs. (2)
OUTP	Laser modulation is prevented; the APC loop will increase bias current to compensate for the drop in laser power. If the set output power can not be obtained, a fault state occurs. (2,3)	A fault state occurs. (2)
OUTN	Does not affect laser operation.	Does not affect laser operation.
GNDO	Laser modulation is prevented and a fault state may occur. (2)	Does not affect laser power.
SV_{CC}	Does not affect laser operation.	The laser is turned off and a fault state occurs. (2)

NOTES:

1. In this case a fault state will assert the FAIL output, but it is not latched. While the fault condition remains, the bias and modulation outputs are disabled and the switch at SV_{CC} is open. No fault occurs if in Safety Circuit Bypass (SCB).
2. In this case a fault state will assert and latch the FAIL output, disable bias and modulation outputs and open the switch at SV_{CC}. No fault occurs if in Safety Circuit Bypass (SCB).
3. Does not affect laser power when the modulation output is AC coupled to the laser.
4. Does not affect laser power in open loop mode or when "Ignore I_{PIN}" is selected.

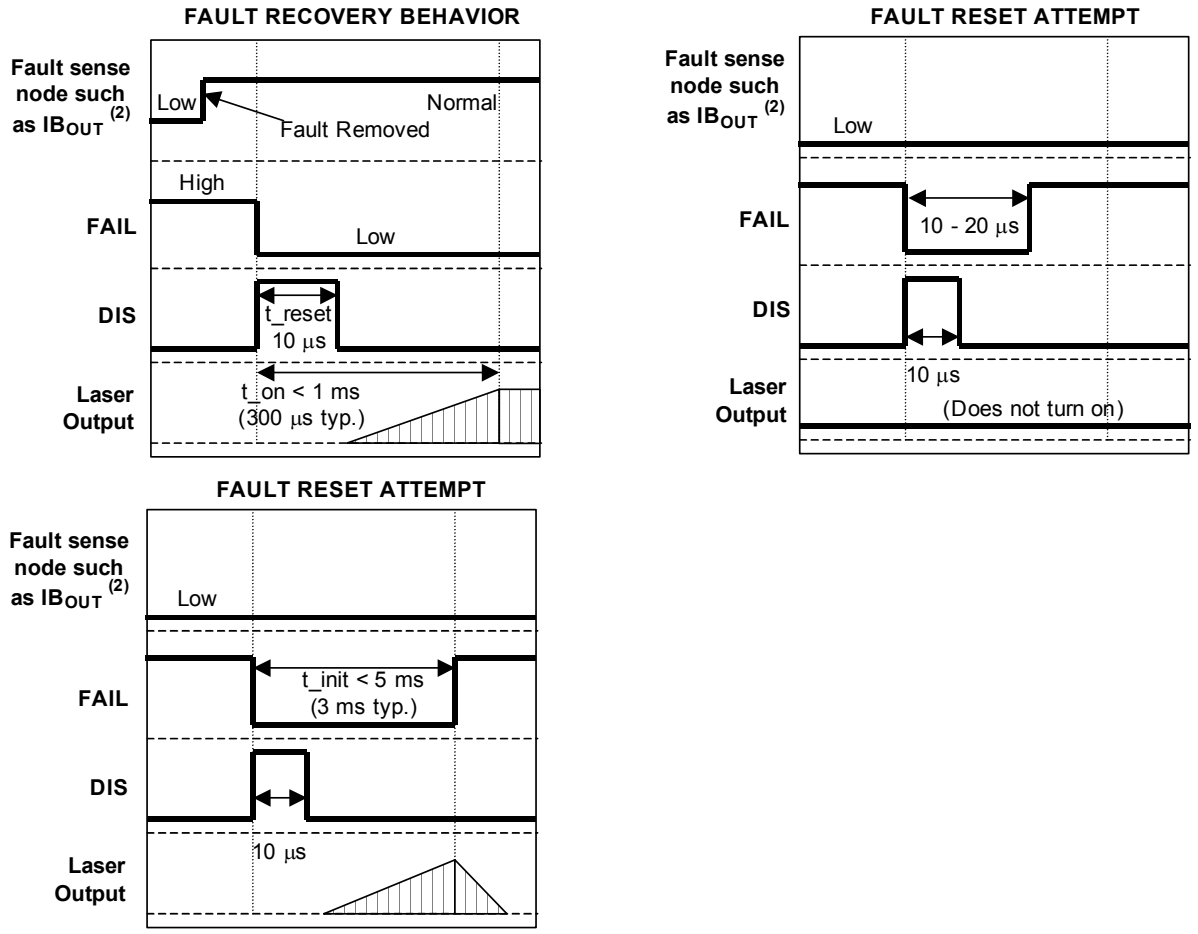
Figure 1-2. M02095/6 Safety Logic Timing Characteristics



1. Supply "OK" means both V_{CC} and $V_{CC}3$ are within their defined operating windows.
2. A fault occurs when I_{PIN} goes high or low; a fault at I_{PIN} does not apply when "Ignore I_{PIN}" configuration is selected.

NOTE: "Laser Output" is equivalent to bias current plus modulation current.

Figure 1-3. M02095/6 Safety Logic Timing Characteristics (Continued)



1. Supply "OK" means both V_{CC} and $V_{CC}3$ are within their defined operating windows.
2. A fault occurs when I_{PIN} goes high or low; a fault at I_{PIN} does not apply when "Ignore I_{PIN}" configuration is selected.

NOTE: "Laser Output" is equivalent to bias current plus modulation current.

2.0 Pin Definitions

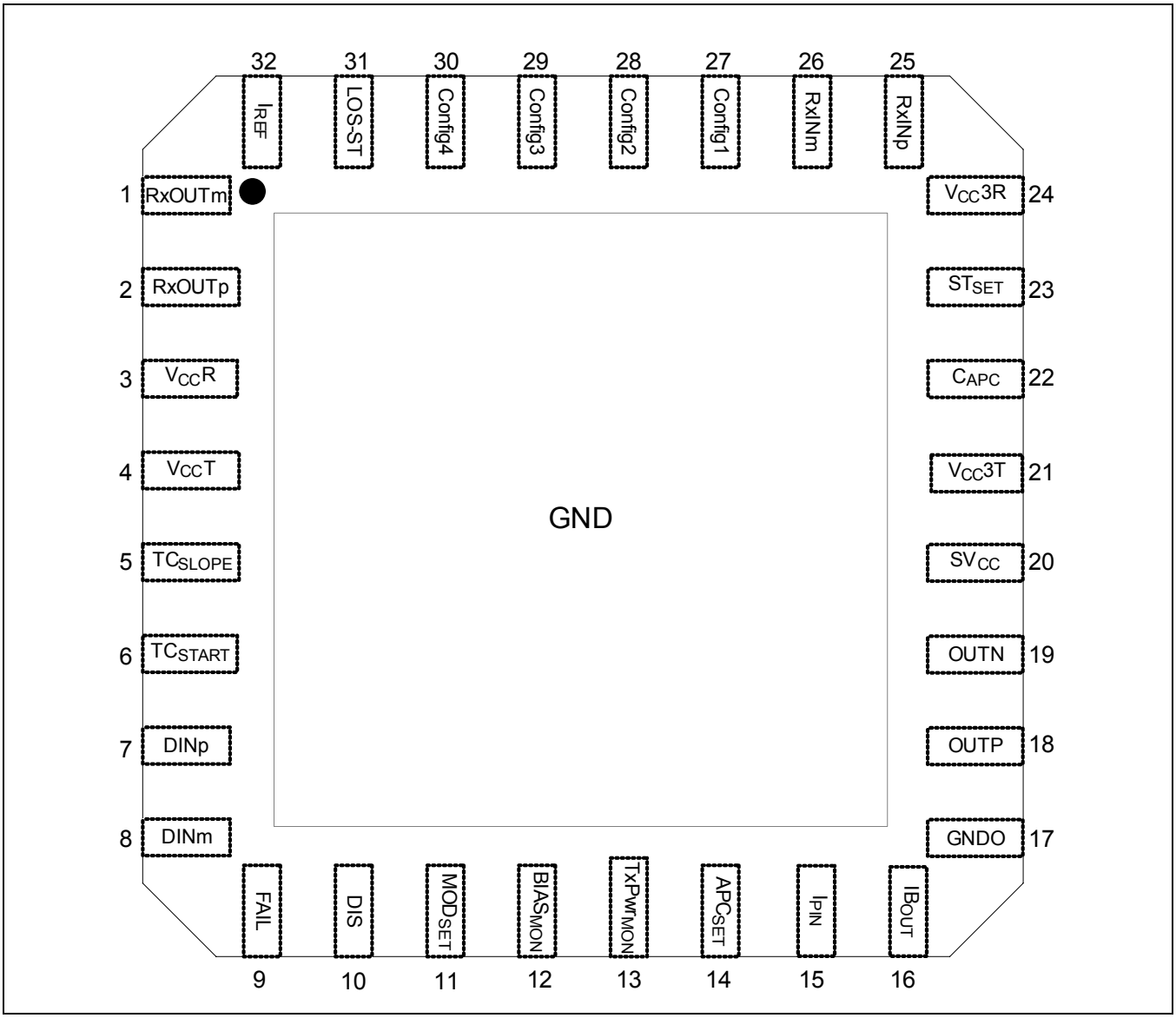
Table 2-1. M02095/6 Pin Descriptions (1 of 2)

QFN Pin Number	Pin Name	Function
1	RxOUTm	Limiting amplifier inverting data output (M02095 - PECL, M02096 - CML). Either output type is referenced to the Rx supply input ($V_{CC}R$).
2	RxOUTp	Limiting amplifier non-inverting data output (M02095 - PECL, M02096 - CML). Either output type is referenced to the Rx supply input ($V_{CC}R$).
3	$V_{CC}R$	Power supply input for limiting amplifier circuitry (3.3V or 5V).
4	$V_{CC}T$	Power supply input for laser driver circuitry (3.3V or 5V).
5	TC_{SLOPE}	Modulation temperature compensation slope. A resistor to ground sets the level of temperature compensation for the modulation current. Forcing this pin high (to 3.3V) causes the configuration logic to ignore configuration logic settings until this pin is released to its normal level (~1.25V). Temperature compensation is disabled if this pin is floating.
6	TC_{START}	A resistor to ground at this pin sets the temperature at which the modulation temperature compensation slope becomes active. Letting this pin float results in a start temperature of ~0°C. Grounding this pin disables temperature compensation.
7	DINp	Transmitter positive Data Input. Internally terminated with 4 kΩ to self-bias voltage of approximately $V_{CC}3T$ - 0.65V. Can be AC coupled.
8	DINm	Transmitter negative Data Input. Internally terminated with 4 kΩ to self-bias voltage of approximately $V_{CC}3T$ - 0.65V. Can be AC coupled.
9	FAIL	Safety circuit fault indicator. Goes high when a safety logic fault is detected. The FAIL output is low when DIS is high. Open collector; 4.7 kΩ to 10 kΩ external pull-up required. 5V compatible when using a 5V supply.
10	DIS	Disable control (TTL compatible). When high or left floating, the bias and modulation outputs are disabled. Set low for normal operation. 7 kΩ internal pull-up to $V_{CC}T$.
11	MOD_{SET}	Modulation Current Adjust. Connect a resistor between this pin and ground to set laser modulation current.
12	$BIAS_{MON}$	Bias output current monitor. Terminate with a resistor to ground to set the desired full-scale voltage at maximum bias current. Some internal functions can be muxed to this pin via the configuration logic. See configuration logic table for more detail.
13	$TxPwr_{MON}$	Transmit power monitor. Provides a 1:1 mirror of the monitor photodiode current. Terminate with a resistor to ground to set the desired full-scale voltage at maximum photodiode current.
14	APC_{SET}	A resistor connected from this pin to ground sets laser output power.
15	I_{PIN}	Monitor photodiode input. Connect this input to the monitor photodiode anode for automatic power control. The monitor photodiode cathode should be connected to SV_{CC} or $V_{CC}3T$.
16	IB_{OUT}	Laser bias current output. Connect to laser cathode through a ferrite.
17	GNDO	Ground for modulation output stage. Connect directly to ground or can connect to ground through an inductor.

Table 2-1. M02095/6 Pin Descriptions (2 of 2)

QFN Pin Number	Pin Name	Function
18	OUTP	Transmitter positive modulation output. Draws current when DINp is high. Referenced to the SV_{CC} (transmitter regulator output) voltage.
19	OUTN	Transmitter negative modulation output. Draws current when DINp is low. Referenced to the SV_{CC} (transmitter regulator output) voltage.
20	SV_{CC}	Internal power supply switch for laser. Provides redundant shutdown during a disable or fault condition.
21	$V_{CC}3T$	Internally regulated voltage for laser driver circuitry in 5V applications. Connect directly to supply to allow wider power supply tolerance in 3.3V-only applications (internal regulator not in use). Do not connect to power supply if V_{CC} = 5V.
22	C_{APC}	A capacitor at this pin sets the dominant pole for automatic power control. Connect a capacitor between this pin and $V_{CC}3$ if automatic power control is used. Can leave floating if using open loop configuration.
23	ST_{SET}	Loss of signal threshold setting input. Connect a resistor between this pin and $V_{CC}3R$ to set loss of signal or signal detect threshold.
24	$V_{CC}3R$	Internally regulated voltage for limiting amplifier circuitry in 5V applications. Connect directly to supply to allow wider power supply tolerance in 3.3V-only applications (internal regulator not in use). Do not connect to power supply if V_{CC} = 5V.
25	RxINp	Non-inverting limiting amplifier data input. Internally terminated with 2 kΩ to self-bias voltage of approximately $V_{CC}3R$ - 0.5V.
26	RxINm	Inverting limiting amplifier data input. Internally terminated with 2 kΩ to self-bias voltage of approximately $V_{CC}3R$ - 0.5V.
27	Config1	Configuration logic input. These pins select laser driver and limiting amplifier configurations and test modes. Refer to Configuration Logic table (Table 4-3) for more information. Three level logic where nominal level is mid-range ($V_{CC}3T$ / 2) when floating.
28	Config2	
29	Config3	
30	Config4	
31	LOS-ST	Limiting amplifier LOS or ST (signal detect) output. Configuration logic selects whether output is to be LOS or ST. 5V compatible when using a 5V supply.
32	I_{REF}	Internal reference current. Must be connected to ground through a 12.4 kΩ 1% resistor.

Figure 2-1. M02095/6 Package Pin-out (5x5mm MLF)



3.0 Functional Description

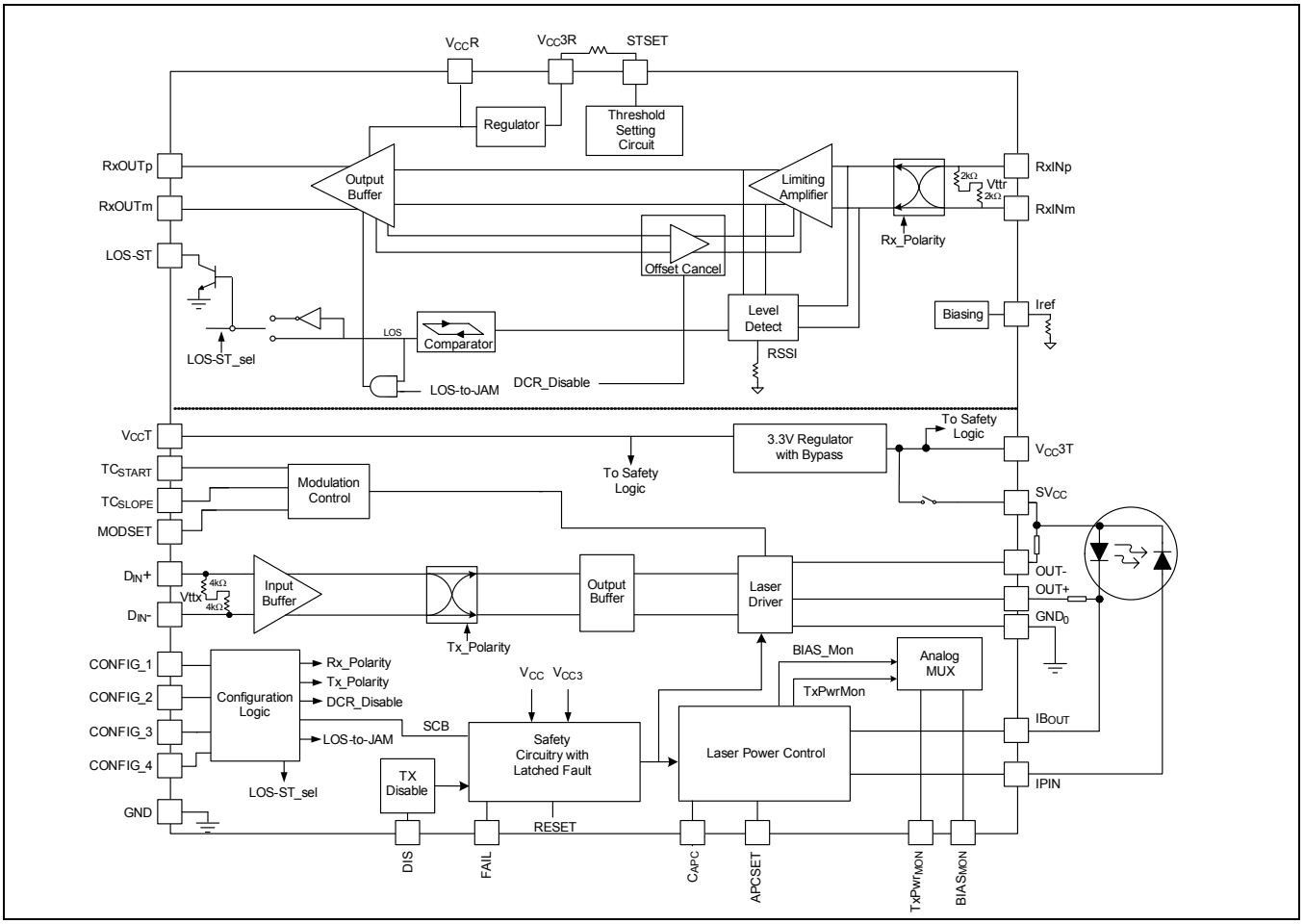
3.1 Overview

The M02095/6 devices are a highly integrated combined laser driver and limiting amplifier intended for applications to 2.5 Gbps, depending on device type. The parts can be operated from a single 3.3V or 5V supply.

Many features are user-adjustable, including the APC loop bias control (via a monitor photodiode), modulation current, temperature compensation control of modulation current, loss of signal threshold, using jam or not on the Rx path and the Rx and Tx polarity.

Safety circuitry is also included to provide a latched shut-down of laser bias and modulation current if a fault condition occurs. An internal V_{CC} switch provides redundant shutdown of the laser current under a fault condition.

Figure 3-1. M02095/6 Block Diagram



3.2 General Description

The M02095 and M02096 integrate a laser driver and limiting amplifier in one highly configurable device for applications to 1.25 Gbps and 2.5 Gbps respectively. The Tx and Rx paths are independently operated and configurable using four three state configuration inputs allowing more than 80 user variations.

The laser driver supplies the bias and modulation current required to drive an edge emitting laser and incorporates automatic power control, a power supply switch for redundant shutdown during a fault, user settable temperature compensation of modulation current and SFP compliant safety circuitry. The limiting amplifier includes user settable input signal level detection circuit and a fully integrated DC-offset cancellation loop that does not require any external components.

Using the configuration logic, the limiting amplifier output can be jammed when loss of signal occurs and polarity control is available for both the driver and limiting amplifier data paths. Finally, using an internal self selecting regulator, the devices can operate from either a 3.3V or 5V supply with no changes to its configuration.

3.2.1 Internal Regulator

The M02095/96 contain an internal 3.3V regulator so high bit rate performance can be achieved with either a 5V or 3.3V power supply.

When operating from a 5V supply (V_{CC} connected to +5V), an internal regulator provides a voltage of approximately 3.3V to the majority of the on-chip circuitry. The on-chip regulator is internally compensated, requiring no external components. When a 3.3V supply is used (V_{CC} connected to 3.3V, or both V_{CC} and $V_{CC}3$ connected to 3.3V), internal logic configures the device for 3.3V operation and the regulator is switched to a low-resistance mode. The device decides whether or not the internal regulator is enabled using internal sensing logic, the sensing logic also determines whether the device safety circuitry needs to monitor for proper +5V supply voltage.

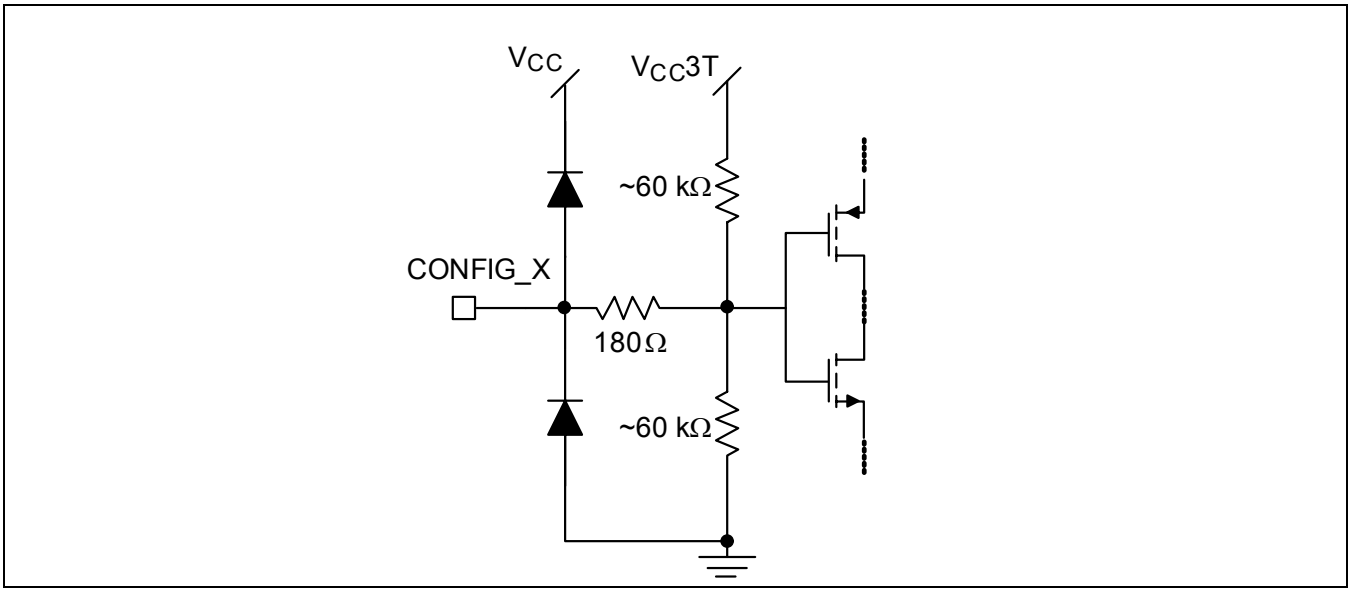
3.2.2 Configuration Logic

The four configuration pins allow the user to select over 80 configurations for the M02095/96. Each input has three states: tied high, tied low or floating. When floating, the respective configuration pin internally is brought to ~V_{CC}3T/2 and this is decoded separately from either a high or low state. See Figure 3-2.

Table 3-1. M02095/6 Configuration Logic Selections

Function	Function
DIS/EN:	The laser driver DIS pin is either active high “Tx_Disable” or active high “Tx_Enable”. Note that the DIS pin has an active high pull-up regardless of its function.
SCB	Safety Circuit Bypass. If SCB is selected, a Tx Fault condition will not be latched and the safety circuitry will not disable the bias and modulation outputs. Fail will be asserted only while the fault is present.
LOS/ST	Defines the limiting amplifier LOS-ST pin as either ST (goes high with signal detect) or LOS (goes high with LOS).
LOS=JAM / NO_JAM	When “LOS=Jam” the limiting amplifier outputs are jammed when a loss of signal occurs. This is separate from whether the LOS/ST pin is defined to be either LOS or ST.
TxPOL	Defines the relationship between D_{IN}+ and OUT+ in the Tx path.
RxPOL	Defines the relationship between RxINp and RxOUTp in the Rx path.
Special Config	Enables multiple specific configurations modes for the user. See Table 4-4 in Section 4.4 of this datasheet.

Figure 3-2. Configuration Pin Input



3.3 Laser Driver Description

3.3.1 Driver Inputs

Inputs to the laser driver data buffer are self-biased through 4 kΩ resistors to an internal reference of approximately $V_{CC}3T$ - 1.3V (Figure 3-3). ($V_{CC}3T$ is the internally regulated voltage for laser driver circuitry in 5V applications or is the bypassed regulator output in 3.3V applications). Both CML and PECL input signals can be AC coupled to the M02095/6.

In most applications the data inputs are AC coupled with controlled impedance pcb traces which will need to be terminated externally with a 100Ω resistor between the D_{IN}+ and D_{IN}- inputs. AC coupling is recommended when using the internal regulator (V_{CC} = 5V), though external level-shifting may be used if DC coupling is desired with a 5V supply.

It is possible to invert the polarity of the driver inputs using the configuration logic (Table 4-3).

Figure 3-3. Laser Driver Data Inputs

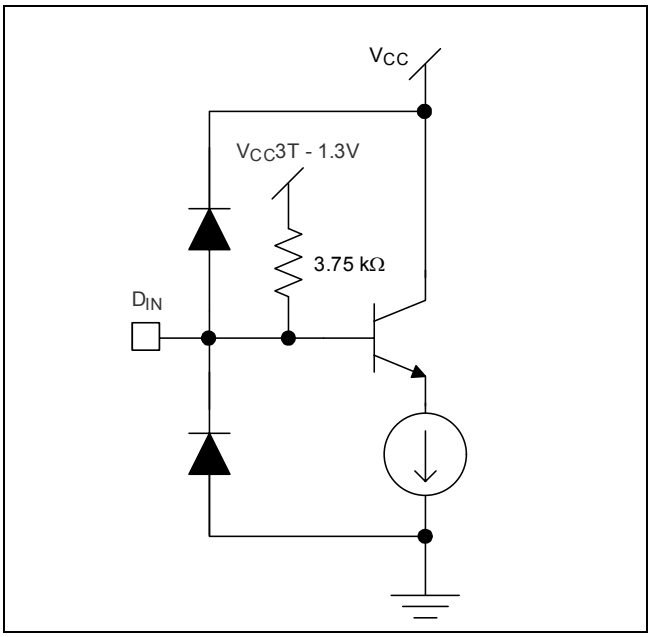
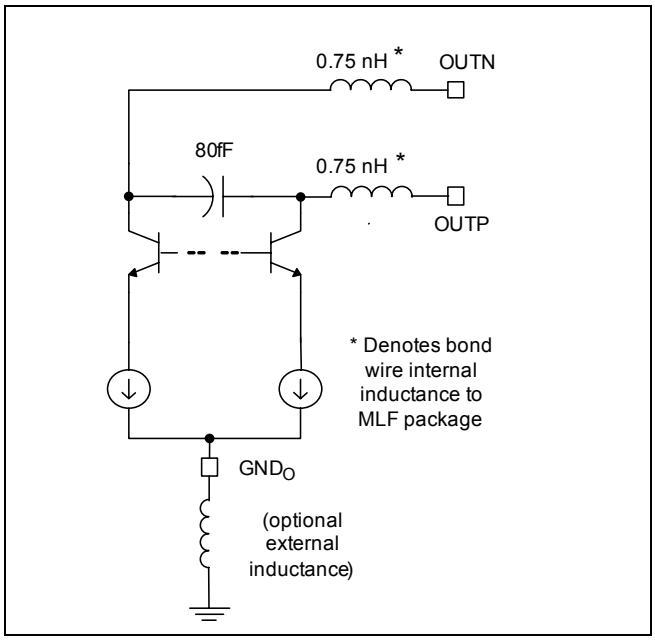


Figure 3-4. Modulator Outputs



3.3.2 Driver Output Stage

The laser driver output stage (Figure 3-4) incorporates feedback to maintain performance over the range of laser modulation current. The output stage is nominally configured to drive an approximate 25Ω output load. When DC coupled, OUTP should be connected through a series resistor to the laser such that the total impedance seen at the output is approximately 25Ω. This will result in the optimum pulse response while allowing the maximum modulation current to be achieved.

The output can also be AC coupled to the laser. When AC coupled the dynamic resistance seen by OUTP should still be 25Ω. In addition to a resistor in series with the laser, a capacitor is added in series and a ferrite is used to pull up the collector at OUTP to V_{CC}. When the laser is AC coupled, the OUTN pin is usually tied to the laser anode through an AC coupled series resistor which matches the impedance seen by the OUTP pad. Laser modulation current is controlled by adjusting current at MOD_{SET} (Figure 3-5).

The output stage also has a separate current path to GND labelled GNDO. This isolates the output switching currents from the rest of the device.

3.3.3 Modulation Control

The modulation current amplitude is controlled by the MOD_{SET} input pin. The modulation current can be temperature compensated by setting slope through the TC_{SLOPE} pin and TC_{START} (Figure 3-6) sets the temperature at which the temperature compensation begins to operate. The temperature compensation is independent of the modulation current setting.

Figure 3-5. APC_{SET}, MOD_{SET} and TC_{SLOPE} Input

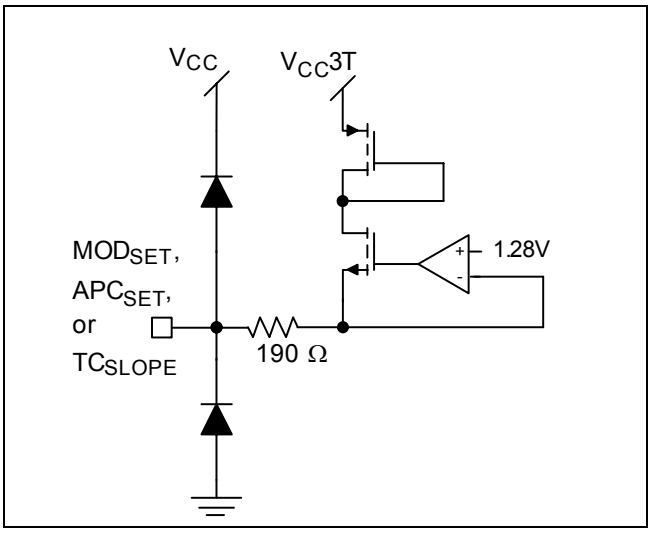
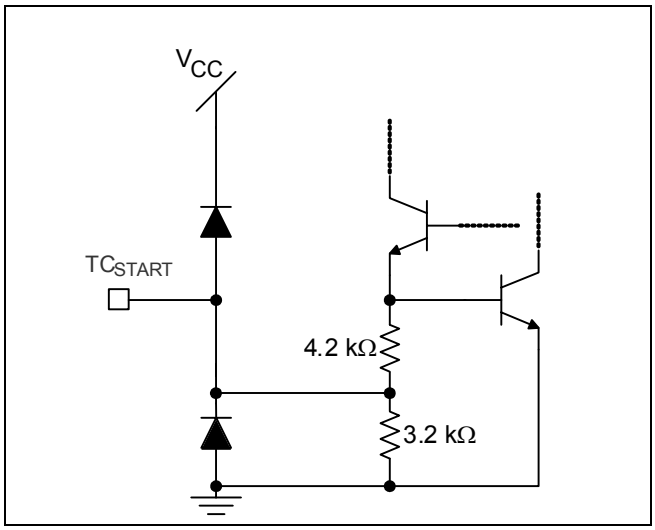


Figure 3-6. TC_{START} Input



3.3.4 Bias Current Generator (Figure 3-7) and Automatic Power Control

The M02095/6 include circuitry to automatically maintain laser average output power with use of a monitor photodiode. The monitor photodiode cathode is connected to $V_{CC}3$ (or SV_{CC}) and the anode is connected to I_{PIN} (Figure 3-8). A feedback loop maintains the monitor photodiode current set by the current at APC_{SET} (Figure 3-5).

The monitor diode photo current is mirrored and an equivalent current is sourced from TxPwrMON (Figure 3-9).

Figure 3-7. IBIAS$_{OUT}$

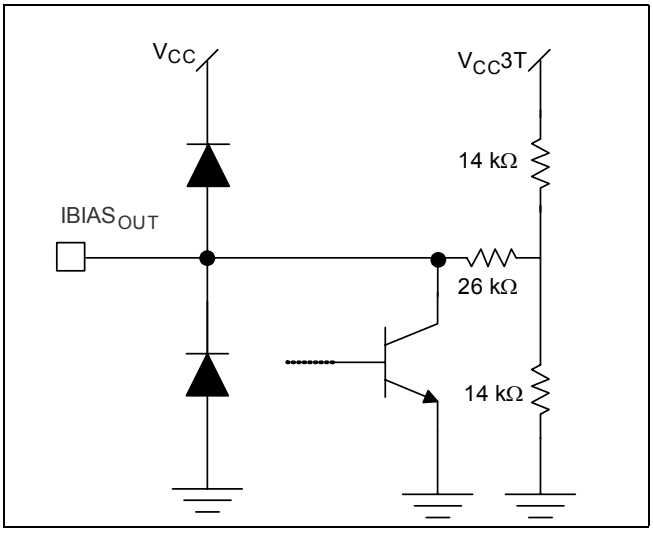
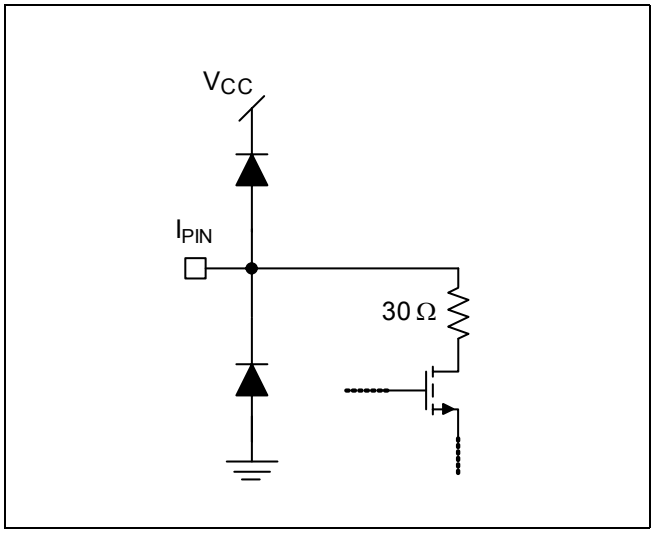


Figure 3-8. I_{PIN} Input



A capacitor between C_{APC} (Figure 3-10) and $V_{CC}3$ sets the dominant pole for APC loop stability.

The bias generator also includes a bias current monitor ($BIAS_{MON}$, Figure 3-9), whose output current is typically 1/90th of the bias current.

Figure 3-9. TxPwrMON and BIAS$_{MON}$ Outputs

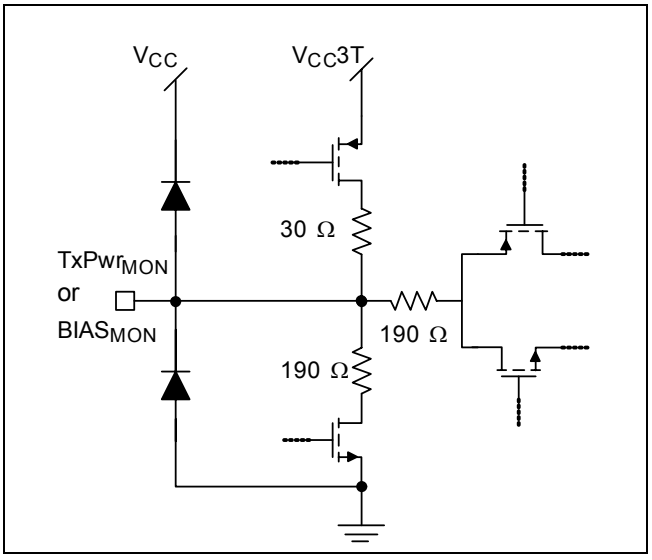
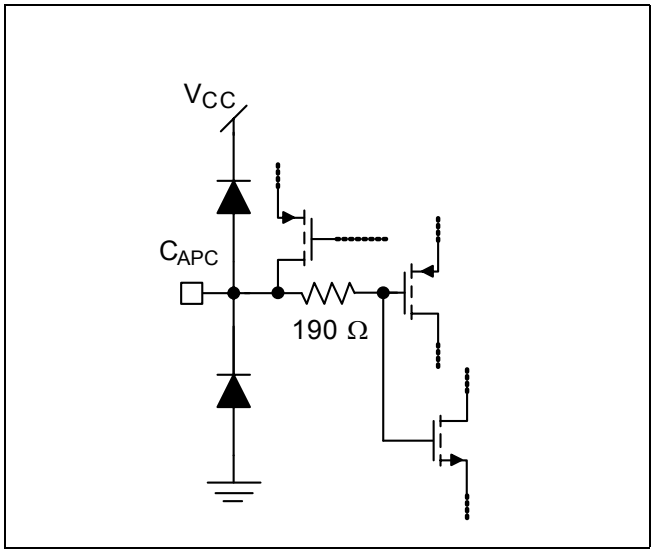


Figure 3-10. C_{APC} Input



3.3.5 Fail Output

The M02095/96 has an open collector FAIL alarm output (Figure 3-11) which is compatible with the TX_FAULT signalling requirements of common plugable module standards.

The Fail output is 5V compatible whether the M02095/96 is using a 5V or 3.3V supply. It requires an external 4.7kΩ to 10 kΩ pull-up resistor so if the M02095/96 loses power the pull-up will signal a fail condition. In a simple static protection scheme used by other ICs the protection diodes would clamp the FAIL signal to ground when the chip loses power.

3.3.6 Tx Disable Control

The DIS (Figure 3-12) pin is used to disable the transmit signal (both the modulation and bias current are disabled when DIS = high or is floating).

Depending on the configuration logic settings (Table 4-3), the DIS pin can redefined as an enable (EN) pin. In this case, both the modulation and bias current are enabled when EN = high or is floating).

The DIS input is compatible with TTL levels regardless of whether V_{CC} = 5V or V_{CC} = 3.3V. The external 4.7 kΩ to 10 kΩ pull-up resistor required by most interface standards is not needed because this pin has an internal 7 kΩ resistor to V_{CC}.

Figure 3-11. FAIL Output

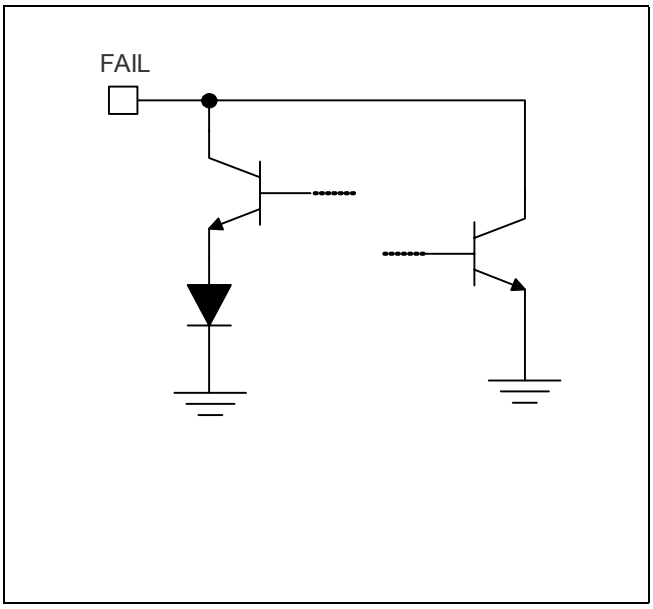
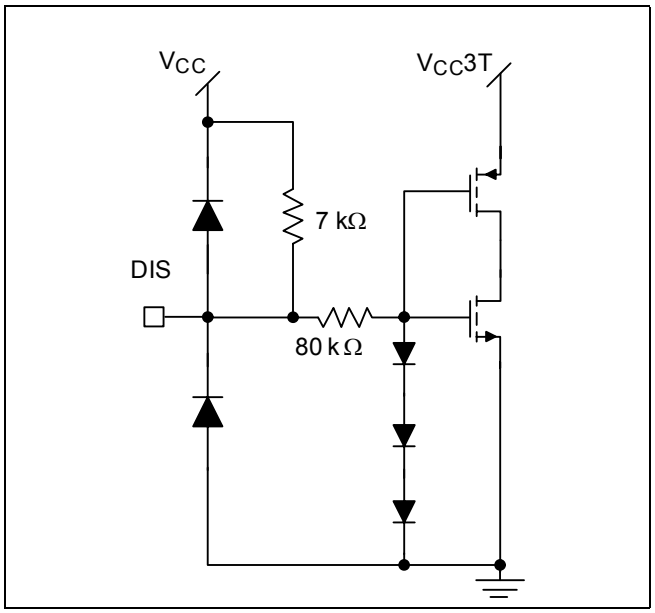


Figure 3-12. DIS (or EN) Input



3.3.7 Safety Circuitry

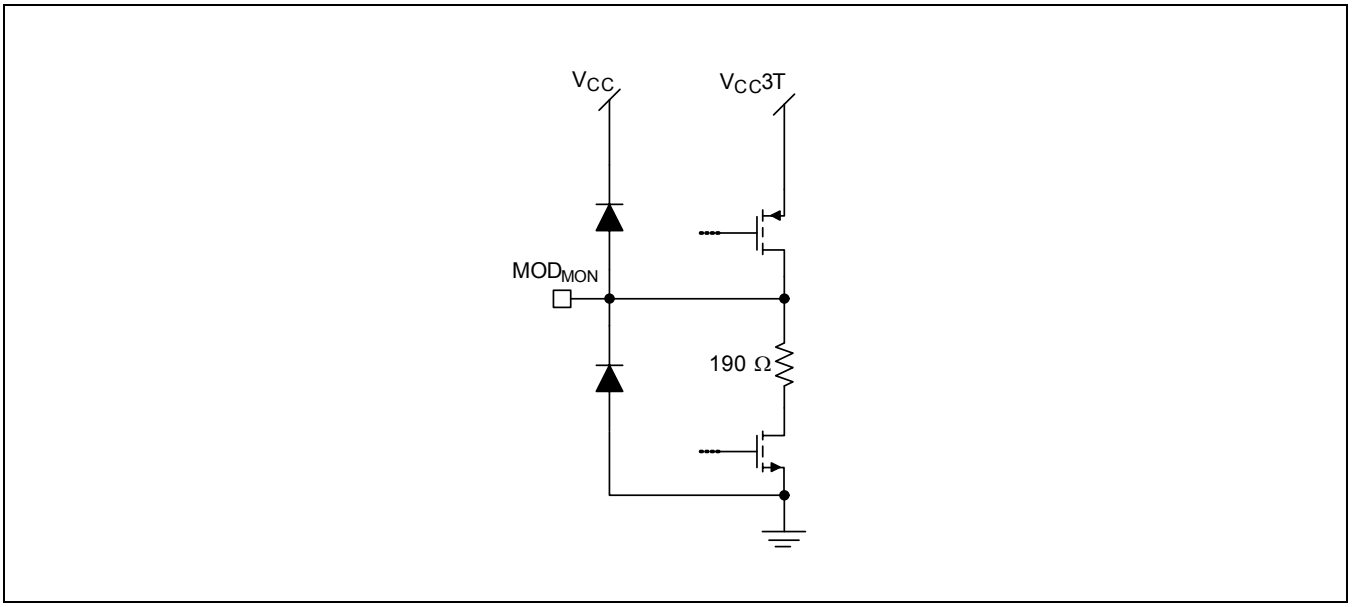
Comparators at APC_{SET}, MOD_{SET}, IB_{OUT}, I_{PIN}, OUTP, and C_{APC} will assert the FAIL (Figure 3-12) output, indicating that a fault condition has occurred (see Table 1-9). This condition is latched and requires DIS (Figure 3-11) to be toggled or power cycling before reset occurs. SV_{CC} is opened during a fault or disable condition.

By setting DIS high, the bias and modulation output currents are disabled. DIS will disable laser bias and modulation current if left floating. DIS must be forced to a low state to enable the outputs. When safety circuit bypass (SCB) mode is enabled, FAIL will indicate a fault condition but is not latched and the outputs will not be disabled. Only the DIS pin will shutdown the outputs when in SCB mode.

3.3.8 Current Monitors

Output monitors are provided for transmit power ($TxPwr_{MON}$) bias ($BIAS_{MON}$) and modulation current (MOD_{MON}). MOD_{MON} has limited availability through a configuration logic setting (Table 4-3) for the M02095/6. These monitors source current and should either feed into a current-input ADC or terminated with a resistor to ground that sets the desired full-scale voltage.

Figure 3-13. MOD_{MON} Output



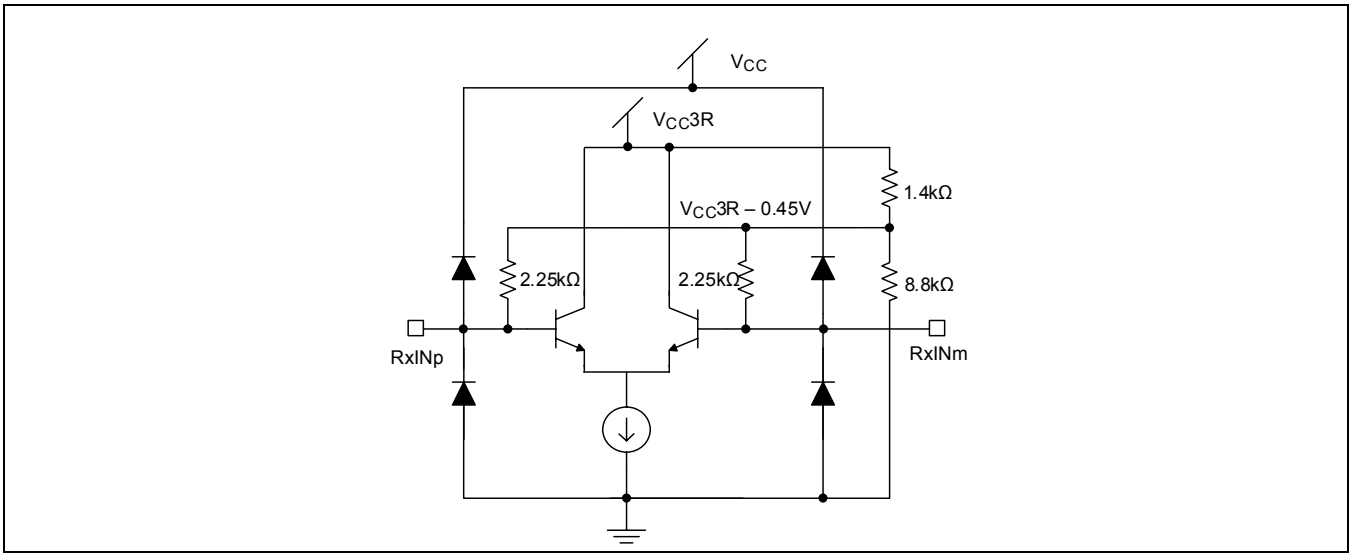
3.4 Limit Amp Description

3.4.1 Inputs

The data inputs are internally connected to V_{TTR} via 2 kΩ resistors and generally need to be AC coupled. Referring to Figure 3-14, the nominal V_{TTR} voltage is 2.85V because of the internal resistor divider to $V_{CC}3R$, which means this is the DC potential on the data inputs. See the applications information section for further details on choosing the AC-coupling capacitor.

It is possible to invert the polarity of the limit amp inputs using the configuration logic (Table 4-3).

Figure 3-14. CML Data Inputs



3.4.2 DC Offset Compensation

The M02095/96 contains an internal DC autozero circuit that can remove the effect of DC offsets without using external components. This circuit is configured such that the feedback is effective only at frequencies well below the lowest frequency of interest. The low frequency cut off is typically 4 kHz.

It is possible to reduce the DC servo cutoff frequency using an external capacitor or to disable the servo loop completely using the configuration logic (Table 4-3). This is described in more detail in the applications section.

3.4.3 CML Outputs

The M02096 CML output configuration is shown in Figure 3-15. The outputs are internally terminated to $V_{CC}3R$ through a 100Ω resistor and have a nominal amplitude of 260 mV_{PP}.

Figure 3-15. CML Data Outputs (M02096)

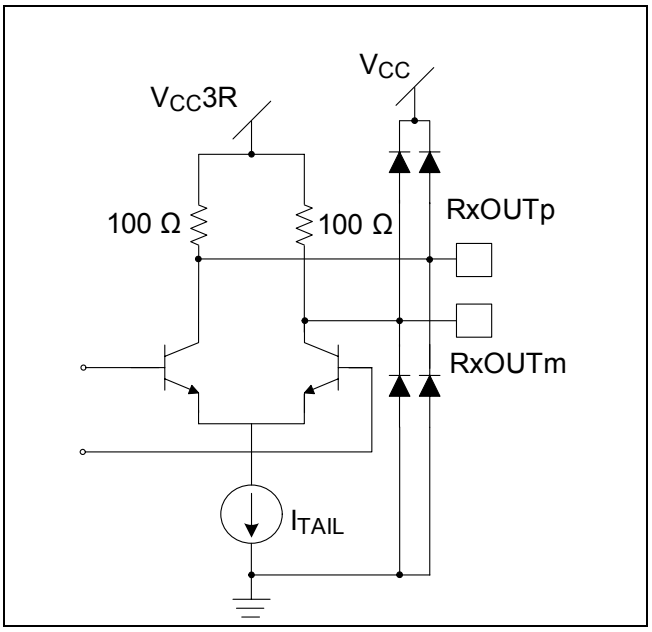
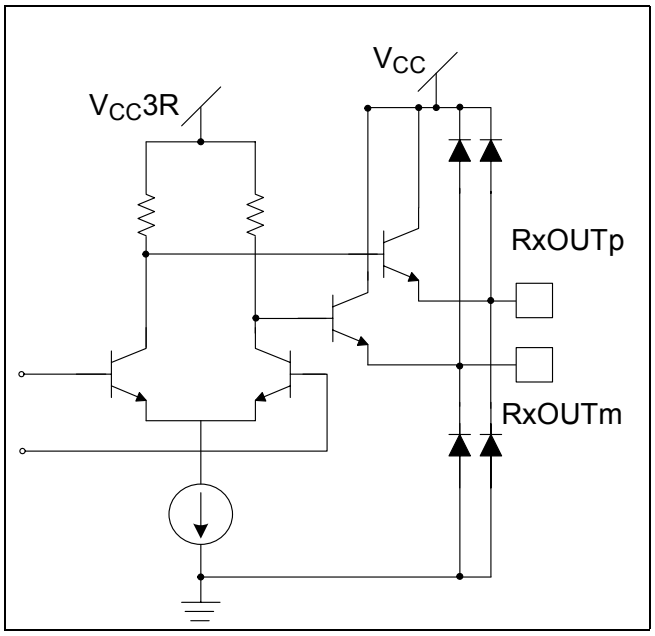


Figure 3-16. PECL Data Outputs (M02095)



3.4.4 PECL Outputs

The M02095 features 100k/300k PECL swing compatible outputs as shown in Figure 3-16 that are referenced to $V_{CC}3R$. The outputs may be terminated using any standard AC or DC-coupling PECL termination technique. AC-coupling is used in applications where the average DC content of the data is zero e.g. SONET. The advantage of this approach is lower power consumption, no susceptibility to DC drive and compatibility with non-PECL interfaces.

3.4.5 Loss of Signal/Signal Detect (LOS-ST)

The M02095/96 features input signal level detection over an extended range. Using an external resistor between pin ST_{SET} (Figure 3-18) and $V_{CC}3R$ the user can program the input signal threshold. This function can be programmed using the configuration logic (Table 4-3) to either represent signal detect (ST) or loss of signal (LOS). For a given R_{ST} resistor setting, the difference between the ST and LOS threshold is a fixed hysteresis. The signal detect status is indicated on the LOS-ST output pin shown in Figure 3-17. LOS is active when the signal is below the threshold value, ST is active when the signal is above the threshold value. The signal detection circuitry has the equivalent of 4 dB electrical hysteresis.

Figure 3-17. LOS-ST Output

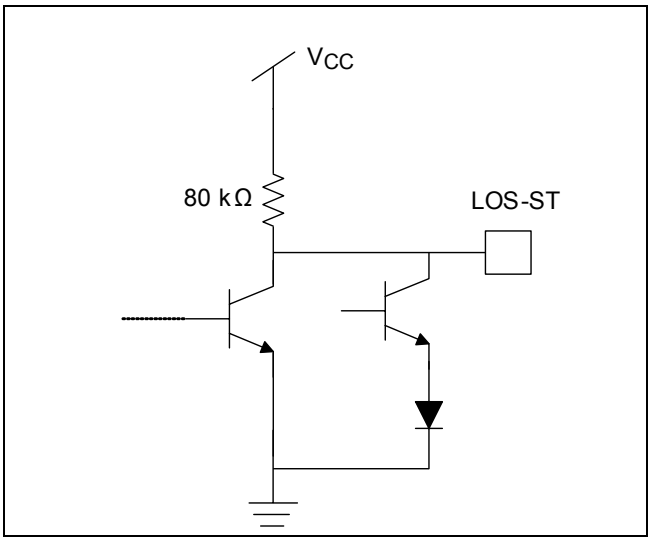
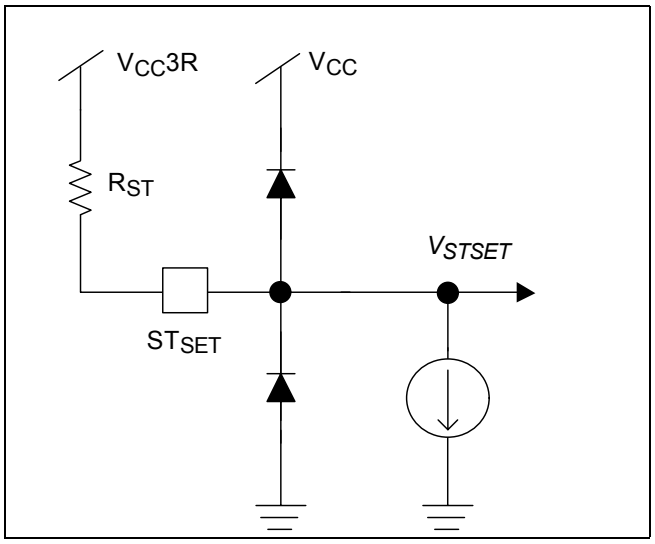


Figure 3-18. STSet Input



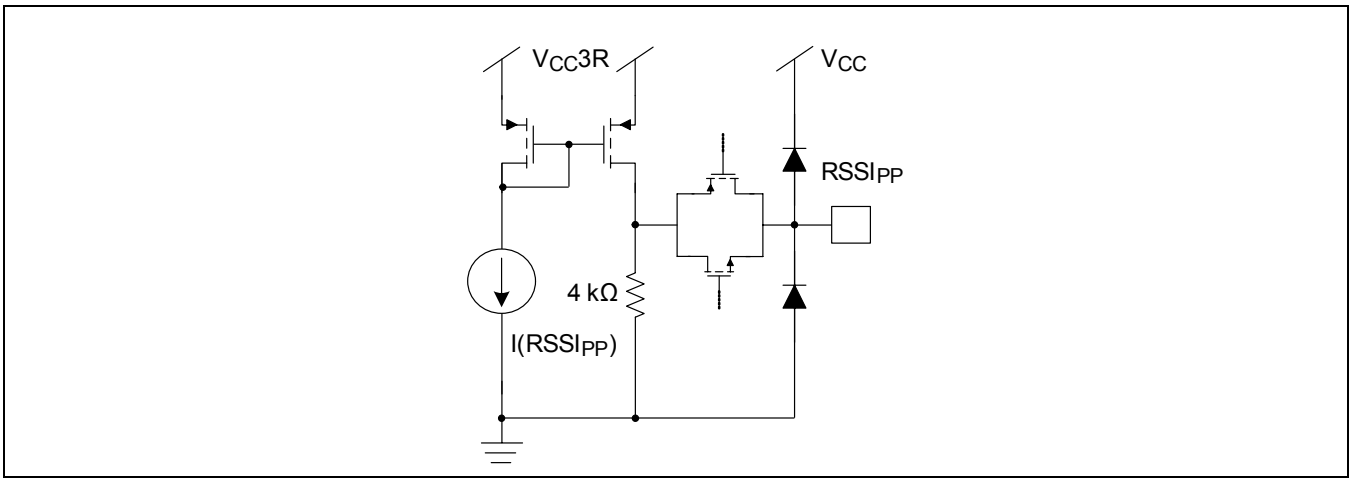
3.4.6 JAM Function (“Squelch”) (Special Configuration Mode)

When enabled through the configuration logic (Table 4-3), when LOS is asserted (ST is deasserted) an internal connection between LOS and the output buffer forces the data outputs to a logic “one” state. This ensures that no data is propagated through the system. The loss of signal detection circuit can be used to automatically force the data outputs to a high state when the input signal falls below the LOS threshold. The function is normally used to allow data to propagate only when the signal is above the user's bit-error-rate requirement. It therefore inhibits the data outputs toggling due to noise when there is no signal present.

3.4.7 Peak to Peak Received Signal Strength Indicator ($RSSI_{PP}$) (Special Configuration Mode)

When enabled through the configuration logic (Table 4-3), the $RSSI_{PP}$ output voltage is made available on the TxPwrMON output pin. the RSSI voltage is logarithmically proportional to the peak to peak level of the input signal. It is not necessary to connect an external capacitor to this output.

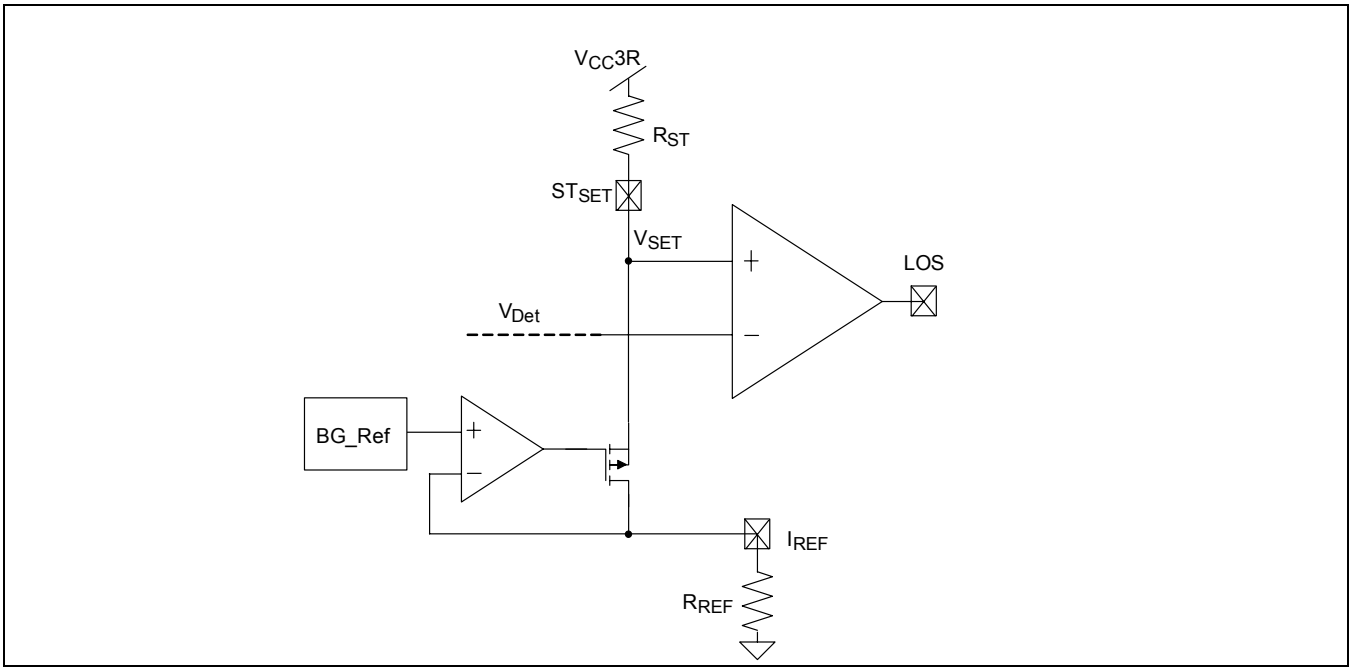
Figure 3-19. $RSSI_{PP}$ Output (when configured by the Configuration Logic)



3.4.8 Reference Current Generation

The M095/96 contains an accurate on-chip bias circuit that requires an external 12.4 kΩ 1% resistor, R_{REF}, from pin I_{REF} to ground to set the LOS-ST threshold voltage at ST_{SET} precisely.

Figure 3-20. Reference Current Generation

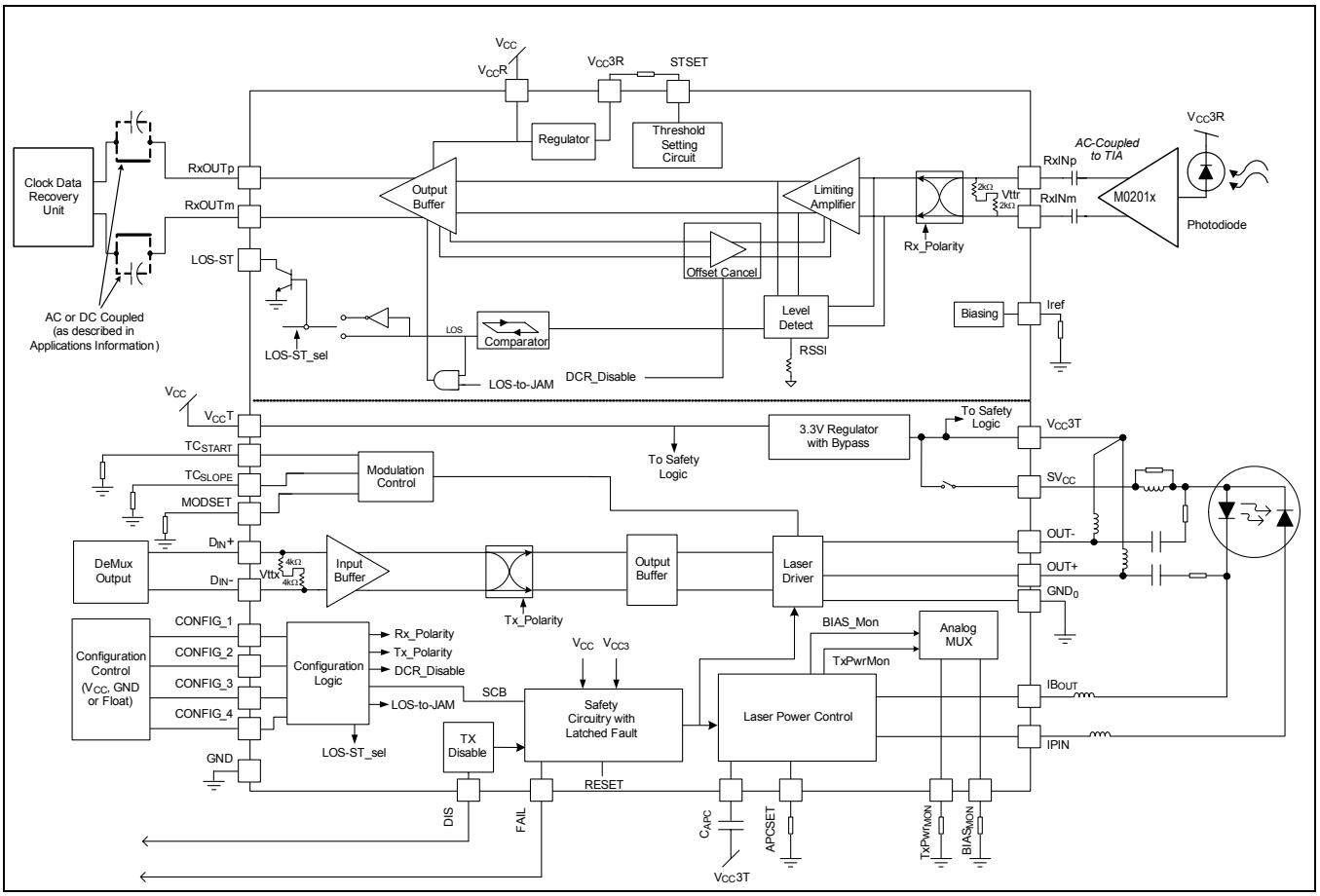


4.0 Applications Information

4.1 General

- 2.5 Gbps STM-16/OC-48 SDH/SONET (M02096)
- 1.06 and 2.12 Gbps Fibre Channel (M02095/6)
- 1.25 Gbps Ethernet (M02095/6)
- 1.25 Gbps SDH/SONET (M02095/6)
- 2.67 Gbps SDH/SONET with FEC (M02096)
- SDH/SONET 155 Mbps Transceivers
- FTTx and Media Converters

Figure 4-1. Application Diagram, Laser AC Coupled Example



4.2 Laser Driver Connections

4.2.1 Configuring the Laser Driver Output

The laser driver output configuration needs to be optimized for the device type and configuration. Figure 4-2 shows a typical schematic of the laser driver connections for both AC and DC coupling. Table 4-1 provides the recommended starting component values for the two configurations.

Figure 4-2. Laser Driver Output and Typical Component Values

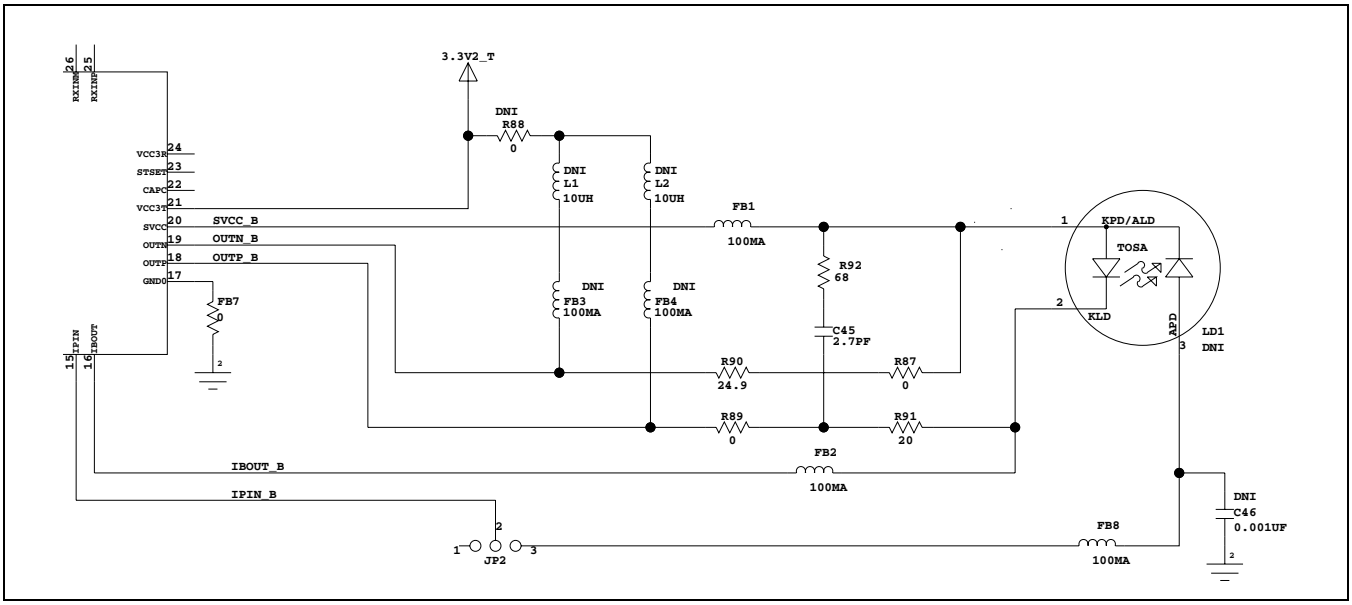


Table 4-1. Suggested Starting Component Values for Laser Driver Connections

Component	AC Coupled Laser	DC Coupled Laser
R88	0Ω	open
L1, 2	10 µH	open
FB3, 4	Ferrite (1)	open
FB1, 2, 8	Ferrite (1)	Ferrite (1)
R89, 90	100 nF	0Ω
R92 (2)	68Ω	68Ω
C45 (2)	2.7 pF	2.7 pF
R87	25Ω	25Ω
R91	20Ω	20Ω

Table 4-1. Suggested Starting Component Values for Laser Driver Connections

Component	AC Coupled Laser	DC Coupled Laser
C46	open	open
FB7	0Ω	0Ω

NOTES:

1. Ferrite bead, 600Ω, 100 MHz, 100 mA typical. Similar to Murata BLM18HD601SN1.
2. C45 and R92 are compensation components for the laser TO can inductance. Actual values are determined by experimentation but typically fall within 0 to 30 pF and 0 to 200Ω.

4.2.2 Modulation Control

There are programmable control lines for controlling the modulation current and its temperature compensation. These inputs can be programmed simply with a resistor to ground.

The modulation current amplitude is controlled by the MOD_{SET} input pin. The modulation current is temperature compensated by the TC_{SLOPE} inputs. The temperature compensation is independent of the setting.

If the temperature compensation at TC_{SLOPE} is disabled, the modulation output current is:
$I_{MOD} = 110 \times (1.25V / R_{MODSET})$

Where R_{MODSET} is the resistance from pin MOD_{SET} to ground.

4.2.2.1 Setting Modulation Temperature Compensation

Temperature compensation involves setting two parameters: the temperature at which the compensation starts TC_{START} (°C) and the slope TC_{SLOPE} (% compensation / °C).

Figure 4-3 graphically illustrates the selection of the resistor at the TC_{START} pin ($R_{TCSTART}$). For example, to have the temperature compensation start at 30°C, chose $R_{TCSTART}$ = 15 kΩ. With TC_{START} floating, the start temperature defaults to ~0°C.

The percent change per degree C is set by the selection of $R_{TCSLOPE}$ at the TC_{SLOPE} pin. The range varies from 0 to one percent of modulation current change per degree C. Note that the starting modulation current is the that set by R_{MODSET} when the temperature is below that of $R_{TCSTART}$. Figure 4-4 illustrates the behavior of the output modulation current as the temperature increases for a range of resistors at the TC_{SLOPE} pin. This is the most accurate method for selecting $R_{TCSLOPE}$.

However, you can also select $R_{TCSLOPE}$ using the following relationship:

$R_{TCSLOPE} = 19.5*(TC)^{-1.5}$, where TC is the desired slope of the modulation current from 25°C to 85°C in "%/°C" and $R_{TCSLOPE}$ is in kΩ. If no temperature compensation is desired, leave $R_{TCSLOPE}$ open.

In any case, $R_{TCSLOPE}$ will have negligible effect at M02095/6 ambient temperatures below the TC_{START} temperature. For example:

Given a laser with a desired modulation current at low temperatures of 30mA and a temperature coefficient of -0.5%/°C at high temperatures (which will require a laser driver temperature coefficient of +0.5%).

Choose $R_{MODSET} = 110 \times (1.25V / 30mA) = 4.6$ kΩ Choose $R_{TCSLOPE} = 19.5*(0.5)^{-1.5}$ kΩ = 55 kΩ.

Figure 4-3. Selecting $R_{TCSTART}$ for a Given Start Temperature

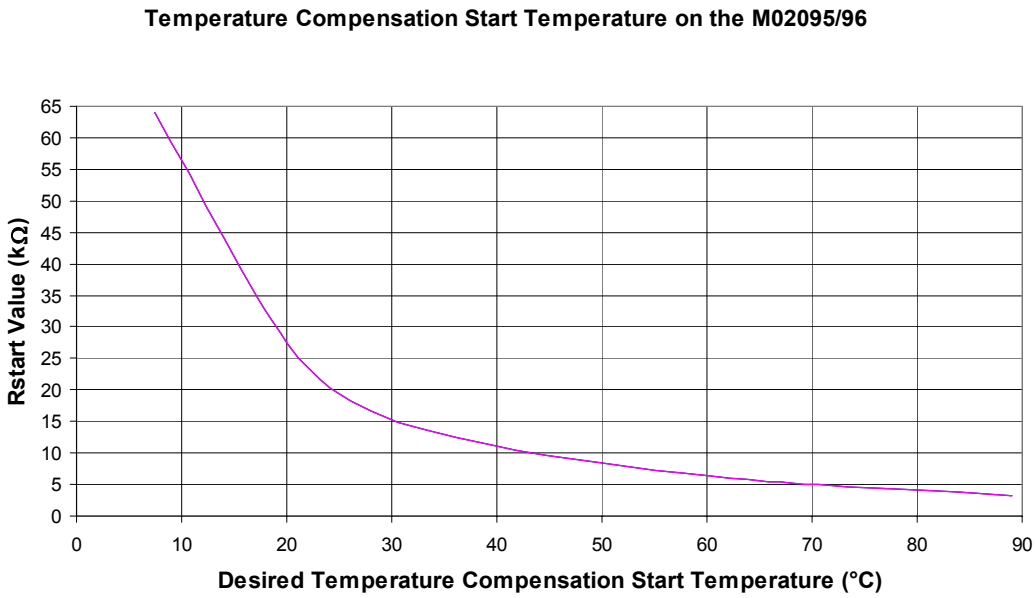
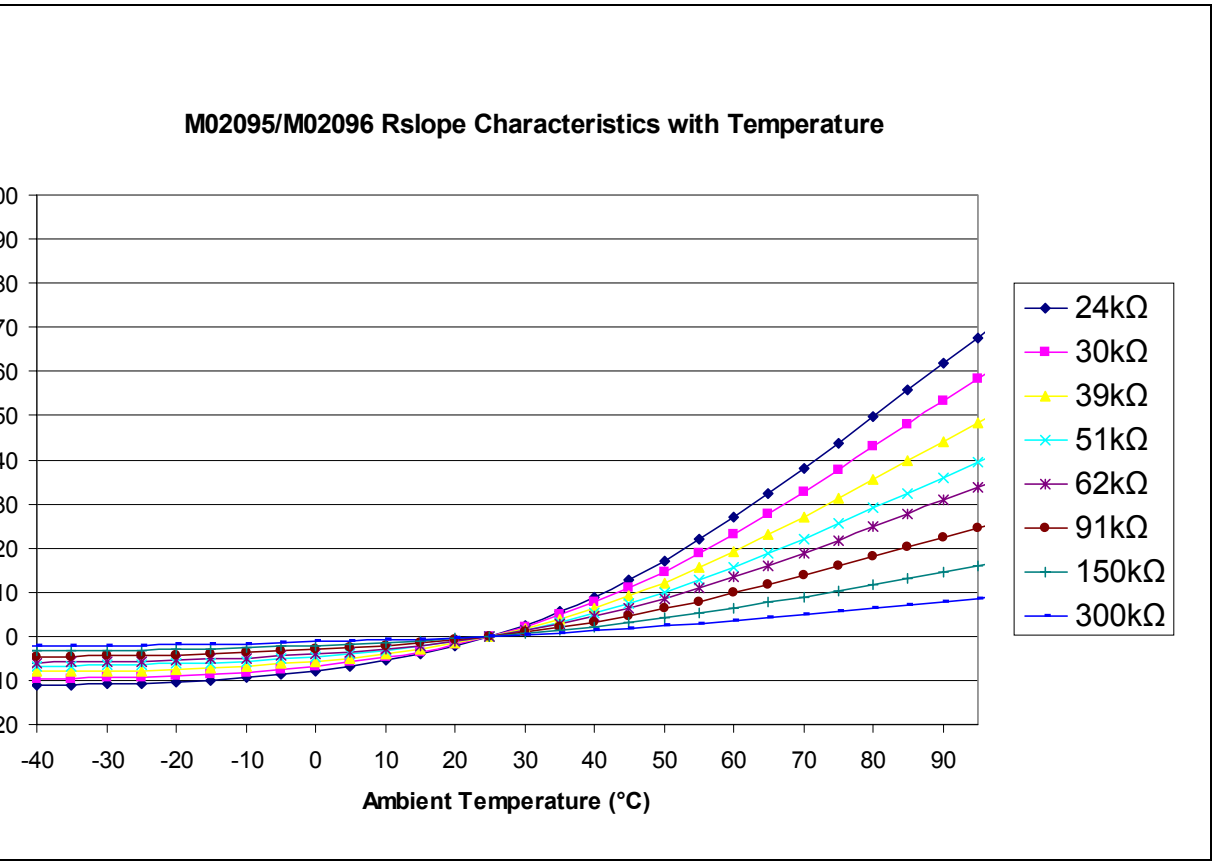


Figure 4-4. Effect of $R_{TCSLOPE}$ on I_{MOD} vs. Temperature for $R_{TCSTART}$ = 25°C (25kΩ)



4.2.3 Setting Automatic Power Control

To maintain laser average output power the laser monitor photodiode cathode is connected to $V_{CC}3$ (or SV_{CC}) and the anode is connected to I_{PIN}. The current from the monitor photo diode mounted in the laser package is sunk at I_{PIN}. The APC loop adjusts the laser bias current so that the current into I_{PIN} from the monitor photo diode equals the current set at APC_{SET} by the user selection of R_{APCSET}.

$R_{APCSET} = 1.25\ V / I_{PIN}$

An internal feedback loop maintains the monitor photodiode current set by the current at APC_{SET}. The resulting laser bias current is determined by the value of the external resistor R_{APCSET} (the external resistor connected between the APC_{SET} pin and ground) and the transfer efficiency between the laser and monitor photo diode.

The monitor diode photo current is mirrored and an equivalent current is sourced from TxPwrMON. TxPwrMON can be connected directly to a current input ADC or through a resistor to ground. If this function is not needed this pin can be left open.

A capacitor between C_{APC} and $V_{CC}3$ sets the dominant pole for APC loop stability. The APC loop includes circuitry allow for good t_on times, even with higher C_{APC} values. For example, a 47 nF capacitor can be used at C_{APC}, providing a low-frequency cutoff typically around 1 kHz while still achieving a t_on < 1 ms. This makes it easy to use the M02095/6 in low rate or multi-rate applications.

The bias current monitor ($BIAS_{MON}$) output current is typically 1/90th of the bias current. This pin can be connected directly to a current input ADC or through a resistor to ground. If this function is not needed this pin can be left open.

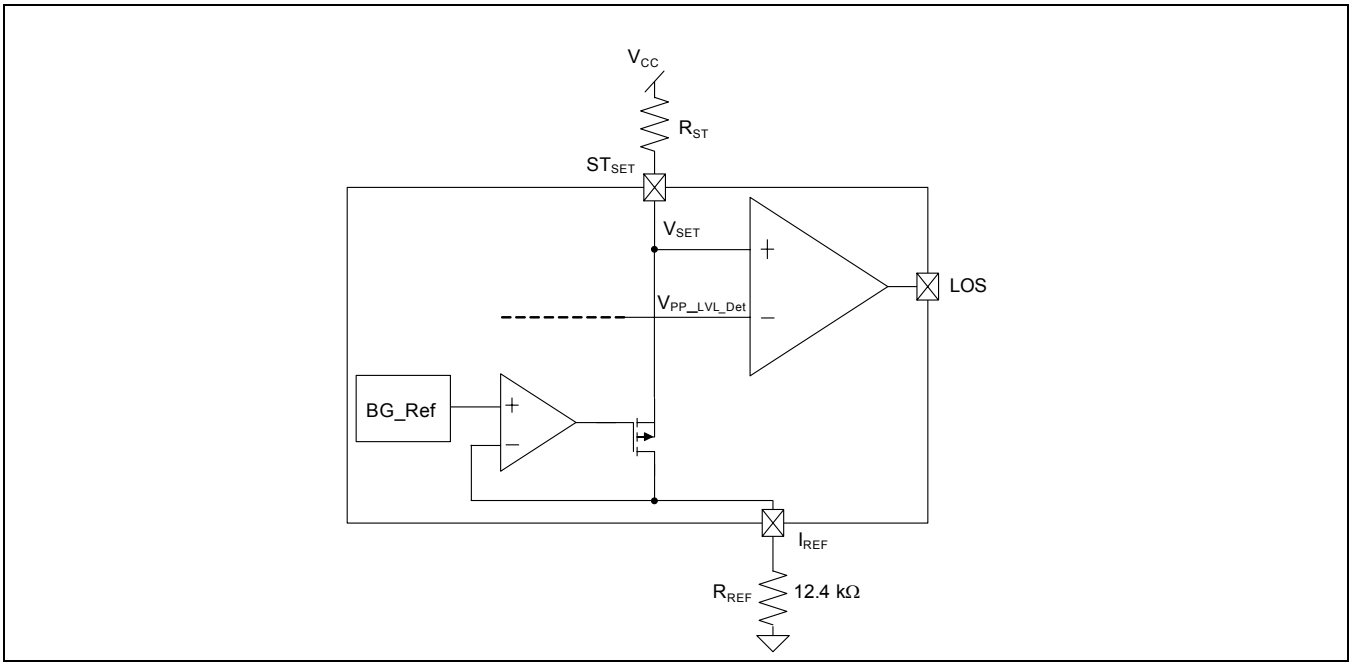
Open loop operation can also be achieved by connecting $BIAS_{MON}$ to I_{PIN}. The open loop bias current is set by adjusting R_{APCSET}. TxPwrMON effectively acts like a bias monitor (duplicate of $BIAS_{MON}$) in this configuration.

4.3 Limiting Amplifier Connections

4.3.1 Reference Current Generation

The M02095/96 contain an accurate on-chip bias circuit that requires an external 12.4 kΩ 1% resistor, R_{REF}, from pin I_{REF} to ground to set the LOS threshold voltage at ST_{SET} precisely.

Figure 4-5. Reference Current Generation



4.3.2 Input Matching and Choosing an Input AC-Coupling Capacitor

Depending on the intended data rate or data rates, the use of an 100Ω resistor in shunt across the limiting amplifier inputs may be used to achieve good high frequency matching between the TIA output and the limiting amplifier input. For applications above 1 Gbps, it is recommended that this resistor be used. The minimum value of AC coupling between the TIA and limit amp depends on whether the limit amp input has this external shunt matching resistance.

When AC-coupling the input the coupling capacitor should be of sufficient value to pass the lowest frequencies of interest, bearing in mind the number of consecutive identical bits, and the input resistance of the part. For SONET data, a good rule of thumb is to chose a coupling capacitor that has a cut-off frequency less than 1/(10,000) of the input data rate. For Ethernet or Fibre Channel, there are less consecutive bits in the data, and the recommended cut-off frequency is 1/(1,000) of the input data rate.

In all cases, a high quality coupling capacitor should be used as to pass undistorted the high frequency content of the input data stream.

4.3.2.1 Data Rates Greater than 1 Gbps

In this case a 100Ω resistor should be connected between RxINp and RxINm close to the limiting amplifier inputs to achieve good match with properly designed 50Ω Zo transmission lines to the input. The value for the AC coupling capacitor then depends on the actual datarate and whether the data is SONET or Ethernet/Fibre Channel based. For example, for 2.5 Gbps SONET data, the coupling capacitor should be chosen as:

$f_{CUTOFF} \leq (2.5x10^9 / 10x10^3) = 250x10^3$

The -3 dB cutoff frequency of the low pass filter at the input is found as (assuming the TIA output is 50Ω single ended):

$f_{3dB} = 1/ (2 \pi * 100\Omega * C_{AC})$

so solving for C where $f_{3dB} = f_{CUTOFF}$

$C_{AC} = 1/ (2 \pi * 100\Omega * f_{CUTOFF})$ EQ.1

and in this case the minimum capacitor is 6.4 nF.
For 1.25 Gbps SONET data, the minimum capacitor is twice this or 12.8 nF.

In all cases, a capacitor larger than calculated above results in a lower cutoff frequency due to the ac coupling between the TIA and the limiting amplifier inputs.

4.3.2.2 Applications below 1 Gbps

The M02095/96 limiting amplifier is ideally suited for low data rate operation because of its low DC servo cutoff frequency and high input resistance. The low servo cutoff frequency improves low data rate performance in the same way that having the AC coupling capacitor sized appropriately for the data rate and longest consecutive string of ones or zeros. The high input resistance means that the AC coupling capacitor need not be nearly as large as in the case of a device with a 50Ω input resistance. For 155 Mbps SONET data, the input coupling capacitor needs to be large enough to pass 15 kHz ($155x10^6$/10,000) resulting in a minimum capacitor value of 5 nF and for 100 Mbps ethernet, the minimum capacitor is even smaller. In either case, a simple choice is the widely available 10 nF capacitor.

4.3.3 Setting the Signal Detect Level

Based on the configuration logic setting (see Table 4-3), the LOS-ST output is either configured to either go high with signal detect (ST output) or to go high with the loss of signal (LOS). Figure 4-6 shows the relationship of the LOS-ST output when defined as LOS across the range of R_{ST} resistors. When configured as an ST output, the labels “Assert” and “Deassert” are interchanged. Table 4-2 lists the Assert and Deassert values for 1% resistors.

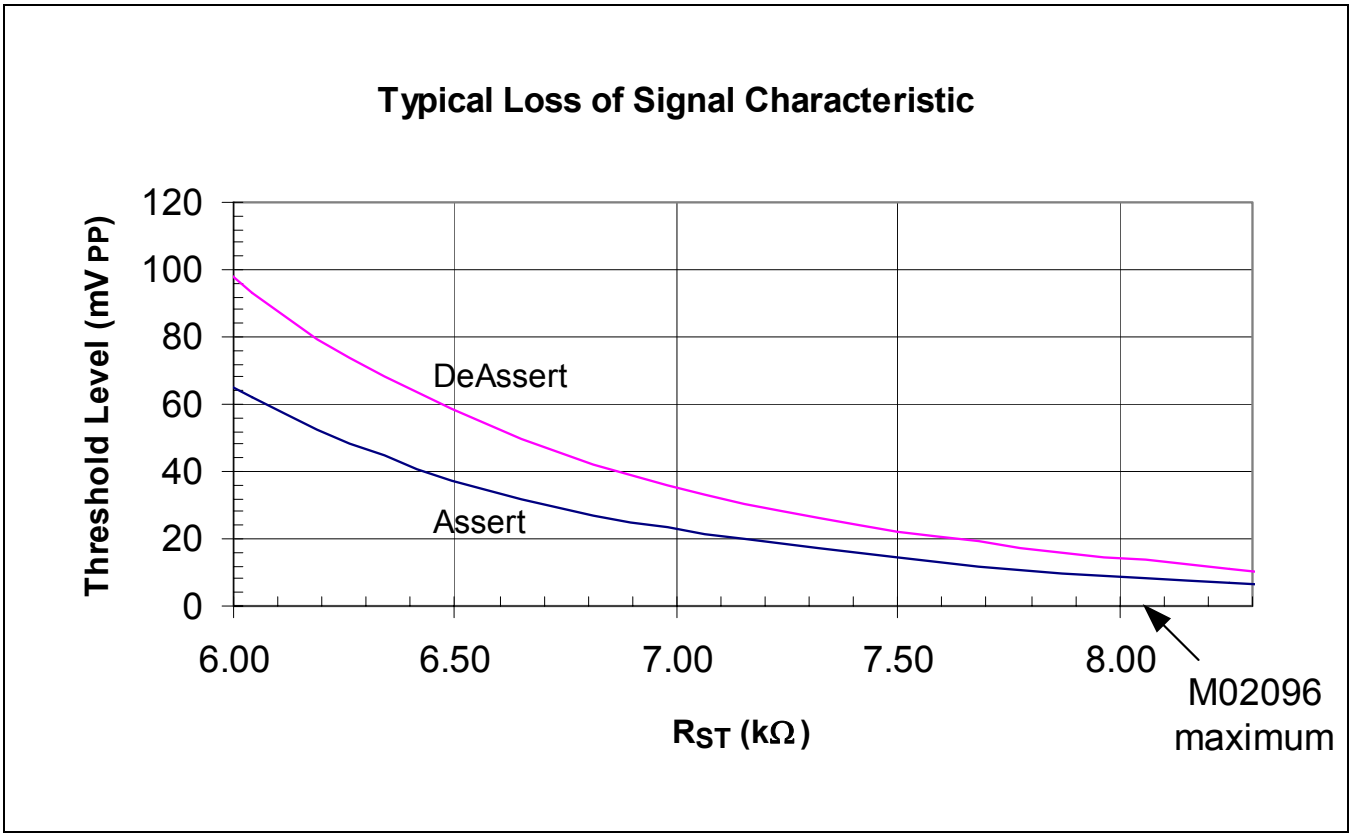
As shown in Figure 4-1, R_{ST} is connected between STSET and $V_{CC}3R$. To minimize LOS-ST variation, it is recommended that a 1% resistor be used for R_{ST}. And as shown in Figure 4-5, the tolerance of the 12.4 kΩ resistor at I_{REF} also affects the LOS-ST accuracy.

Table 4-2. Typical LOS Assert and De-assert Levels for Various 1% R_{ST} Resistor Values

R_{ST} (kΩ)	VIN (mV_{PP}) differential		R_{ST} (kΩ)	VIN (mV_{PP}) differential	
	LOS Assert/ST De-Assert	LOS De-Assert/ST Assert		LOS Assert/ST De-Assert	LOS De-Assert/ST Assert
6.04	62.0	93.0	7.15	20.0	30.2
6.19	52.6	79.1	7.32	17.4	26.2
6.34	44.6	68.1	7.50	14.4	22.4
6.49	37.3	58.8	7.68	11.9	19.3
6.65	31.6	49.6	7.87	10.0	16.2
6.81	27.2	42.0	8.06	8.2	13.6
6.98	23.6	35.6	8.25 (1)	6.9	11.3

NOTE:
1. M02095 Only.

Figure 4-6. Typical Loss of Signal Characteristic vs. R_{ST} (use 1% Resistor tolerance)



4.3.4 Using JAM

As shown in Figure 4-1, there is an optional internal connection between LOS and Jam. If this connection is enabled via the configuration logic (), when LOS asserts the Jam function sets the data outputs to a fixed “one” state (RxOUTp is held high and RxOUTm is held low). This is normally used to allow data to propagate only when the signal is above the users' bit error rate (BER) requirement. It prevents the outputs from toggling due to noise when no signal is present. The internal connection between LOS and Jam is independent of whether the LOS-ST output is configured as a LOS output or an ST output.

4.3.5 PECL Output Termination (2095 Only)

The data outputs of the M02095 are PECL compatible and any standard AC or DC-coupling termination technique can be used. Figure 4-7 and Figure 4-8 illustrate typical AC and DC terminations.

AC-coupling is used in applications where the limiting amplifier is connected to a non-PECL compatible load. In addition to level shifting the signal to the common mode range of the load, the load receives the full PECL peak to peak swing from the limiting amplifier.

DC-coupling can be used when driving PECL interfaces. In the case where the load does not contain PECL termination, Figure 4-8 shows the proper termination for the M02095 PECL outputs. A Thevenin termination may be substituted for the load when V_{CC}-2V is not available and is shown in Figure 4-9.

Figure 4-7. Most Common AC-Coupled PECL Termination (Non-PECL load)

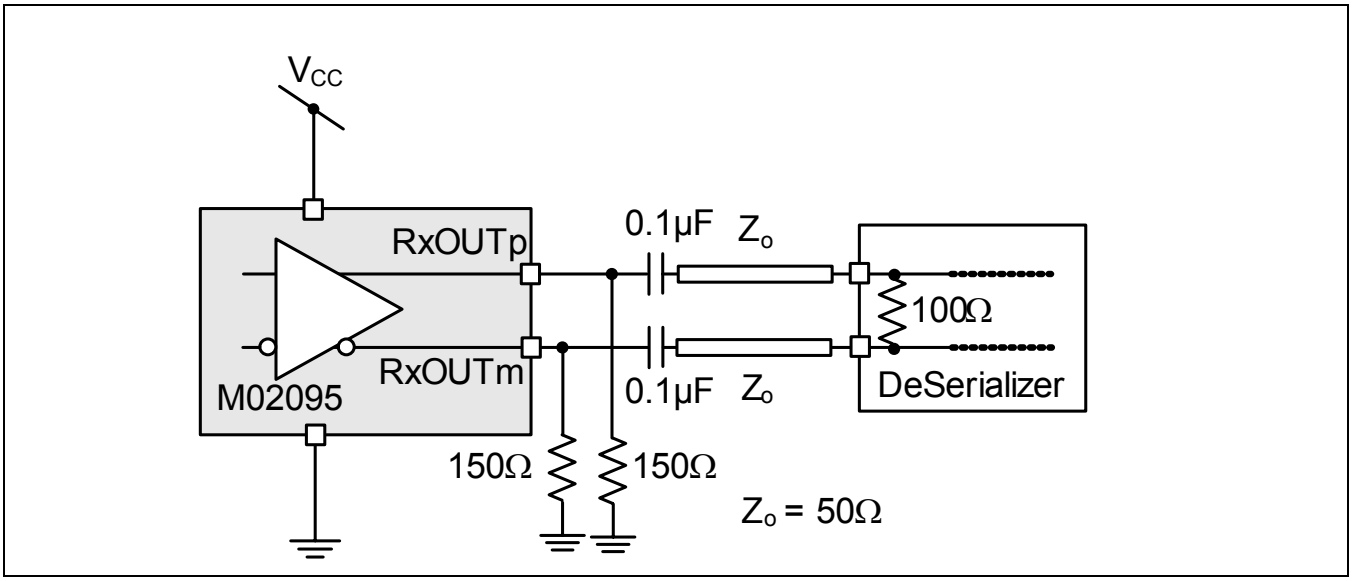


Figure 4-8. True PECL Termination (DC Coupled)

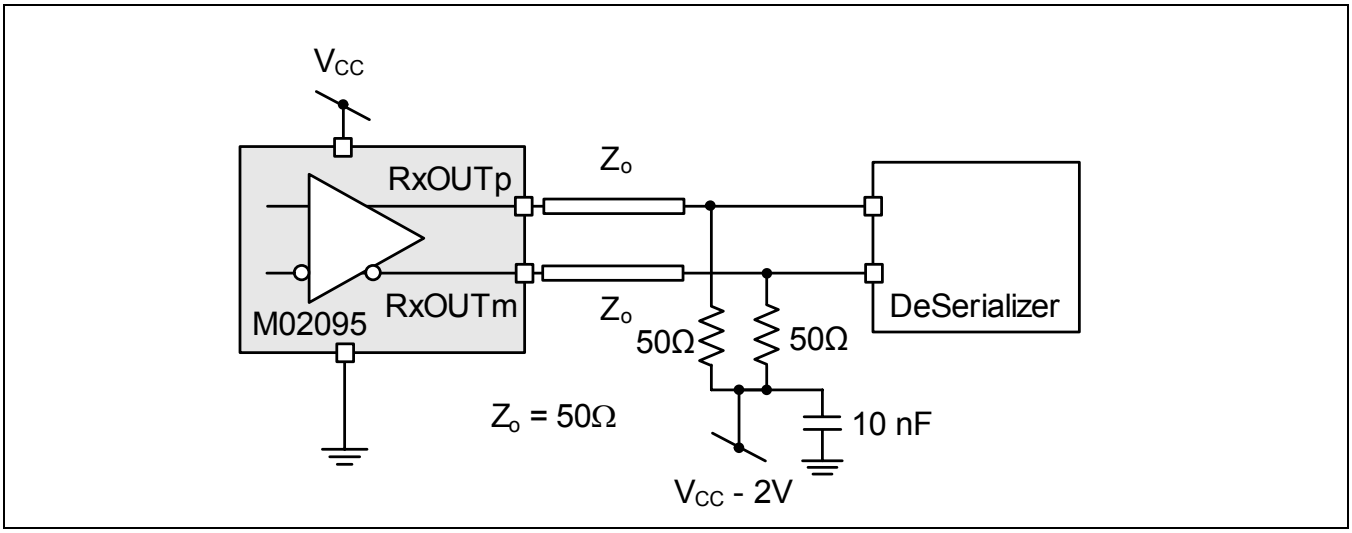
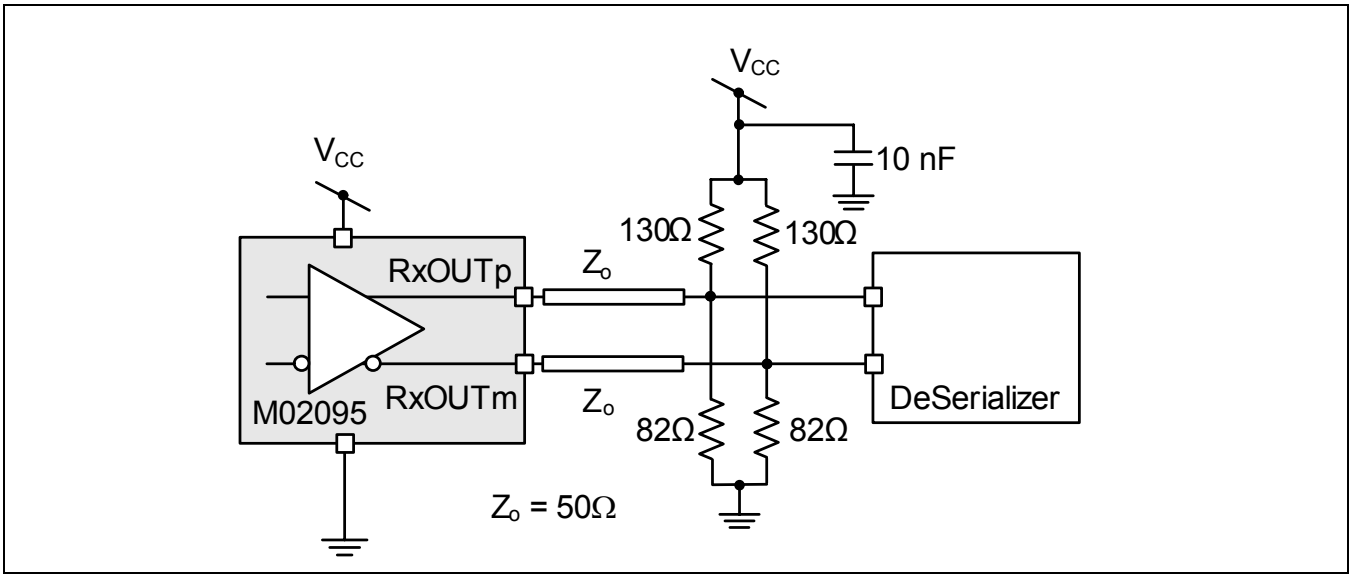


Figure 4-9. Thevenin Equivalent PECL Termination (DC Coupled)



4.4 M02095/6 Configuration Logic

Table 4-3. M02095/6 Configuration Logic

Config1	Config2	Config3	Config4	DIS/EN	LOS=JAM/ NO_JAM	LOS/ST	SCB	RxPOL	TxPOL	Special Config.
0	0	0	0	0	0	0	0	0	0	none
0	0	0	M	0	0	0	0	0	1	none
0	0	M	0	0	0	0	0	1	0	none
0	0	M	M	0	0	0	0	1	1	none
0	0	1	1	0	0	0	1	0	0	none
0	0	0	1	0	0	0	1	0	1	none
0	0	1	0	0	0	0	1	1	0	none
0	0	M	1	0	0	0	1	1	1	none
0	0	1	M	0	0	0	0	0	0	SC1
0	M	0	0	0	0	1	0	0	0	none
0	M	0	M	0	0	1	0	0	1	none
0	M	M	0	0	0	1	0	1	0	none
0	M	M	M	0	0	1	0	1	1	none
0	M	1	1	0	0	1	1	0	0	none
0	M	0	1	0	0	1	1	0	1	none
0	M	1	0	0	0	1	1	1	0	none
0	M	M	1	0	0	1	1	1	1	none
0	M	1	M	0	0	1	0	0	0	SC2
M	0	0	0	0	1	0	0	0	0	none
M	0	0	M	0	1	0	0	0	1	none
M	0	M	0	0	1	0	0	1	0	none
M	0	M	M	0	1	0	0	1	1	none
M	0	1	1	0	1	0	1	0	0	none
M	0	0	1	0	1	0	1	0	1	none
M	0	1	0	0	1	0	1	1	0	none
M	0	M	1	0	1	0	1	1	1	none
M	0	1	M	0	1	0	0	0	0	SC3
M	M	0	0	0	1	1	0	0	0	none
M	M	0	M	0	1	1	0	0	1	none
M	M	M	0	0	1	1	0	1	0	none
M	M	M	M	0	1	1	0	1	1	none
M	M	1	1	0	1	1	1	0	0	none
M	M	0	1	0	1	1	1	0	1	none

Table 4-3. M02095/6 Configuration Logic

Config1	Config2	Config3	Config4	DIS/EN	LOS=JAM/ NO_JAM	LOS/ST	SCB	RxPOL	TxPOL	Special Config.
M	M	1	0	0	1	1	1	1	0	none
M	M	M	1	0	1	1	1	1	1	none
M	M	1	M	0	1	1	0	0	0	SC4
1	1	0	0	1	0	0	0	0	0	none
1	1	0	M	1	0	0	0	0	1	none
1	1	M	0	1	0	0	0	1	0	none
1	1	M	M	1	0	0	0	1	1	none
1	1	1	1	1	0	0	1	0	0	none
1	1	0	1	1	0	0	1	0	1	none
1	1	1	0	1	0	0	1	1	0	none
1	1	M	1	1	0	0	1	1	1	none
1	1	1	M	1	0	0	0	0	0	SC5
0	1	0	0	1	0	1	0	0	0	none
0	1	0	M	1	0	1	0	0	1	none
0	1	M	0	1	0	1	0	1	0	none
0	1	M	M	1	0	1	0	1	1	none
0	1	1	1	1	0	1	1	0	0	none
0	1	0	1	1	0	1	1	0	1	none
0	1	1	0	1	0	1	1	1	0	none
0	1	M	1	1	0	1	1	1	1	none
0	1	1	M	1	0	1	0	0	0	SC5
1	0	0	0	1	1	0	0	0	0	none
1	0	0	M	1	1	0	0	0	1	none
1	0	M	0	1	1	0	0	1	0	none
1	0	M	M	1	1	0	0	1	1	none
1	0	1	1	1	1	0	1	0	0	none
1	0	0	1	1	1	0	1	0	1	none
1	0	1	0	1	1	0	1	1	0	none
1	0	M	1	1	1	0	1	1	1	none
1	0	1	M	1	1	0	0	0	0	SC6
M	1	0	0	1	1	1	0	0	0	none
1	M	0	0	1	1	1	0	0	0	SC7
M	1	0	M	1	1	1	0	0	1	none
1	M	0	M	1	1	1	0	0	1	SC8
M	1	M	0	1	1	1	0	1	0	none

Table 4-3. M02095/6 Configuration Logic

Config1	Config2	Config3	Config4	DIS/EN	LOS=JAM/ NO_JAM	LOS/ST	SCB	RxPOL	TxPOL	Special Config.
1	M	M	0	1	1	1	0	1	0	SC9
M	1	M	M	1	1	1	0	1	1	none
1	M	M	M	1	1	1	0	1	1	SC10
M	1	1	1	1	1	1	1	0	0	none
1	M	1	1	1	1	1	1	0	0	SC5
M	1	0	1	1	1	1	1	0	1	none
1	M	0	1	1	1	1	1	0	1	SC3
M	1	1	0	1	1	1	1	1	0	none
1	M	1	0	1	1	1	1	1	0	SC11
M	1	M	1	1	1	1	1	1	1	none
M	1	1	M	1	1	1	0	0	0	SC12
1	M	M	1	1	1	1	1	1	1	SC13
1	M	1	M	1	1	1	0	0	0	SC14

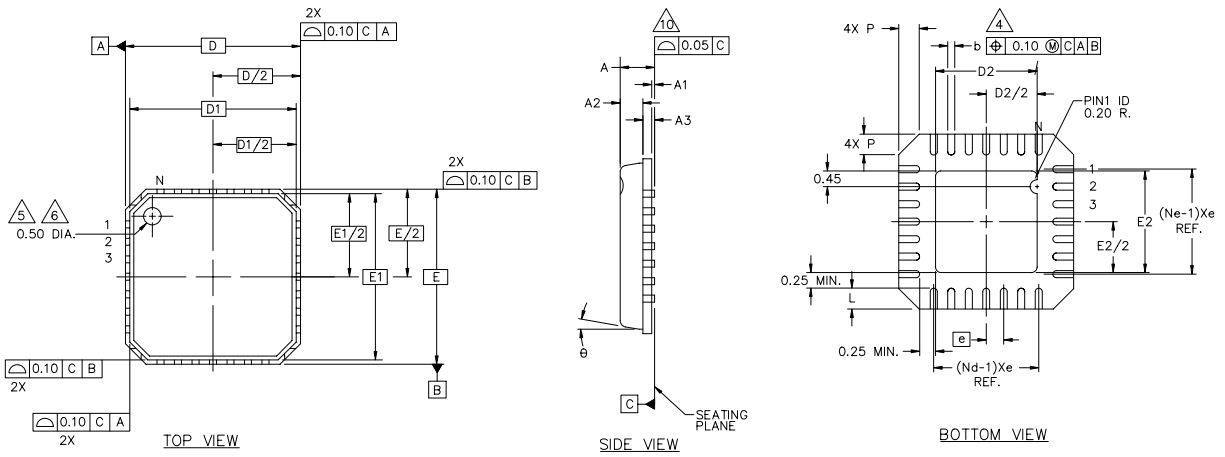
KEY:
0, 1, M:0 = Logic low; 1 = Logic high; M = pin floating (pin goes to intermediate “mid-range” self-biased voltage
DIS/EN:0 = DIS pin acts as Tx_Disable; 1 = DIS pin becomes Tx_Enable
LOS=JAM / NO_JAM:0 = Jam outputs upon LOS; 1 = Do not jam outputs upon LOS
LOS/ST:0 = LOS-ST pin is ST (goes high with signal detect); 1 = LOS-ST pin is high with LOS
SCB:0=latched fault; 1=safety circuit bypass mode
TxPOL and RxPOL:0 = default polarity; 1 = inverted polarity
Special Config.:Refer to Special Configurations table for definition of special configuration modes
If Special Config = “none”, $BIAS_{MON}$, $TxPwr_{MON}$ and other functions operate as defined in the specification.

Table 4-4. M02095/6 Special Configurations

Special Config. #	Special Config. Name	Definition
SC1	Ignore_Ipin	Safety logic ignores high/low faults on IPIN
SC2	Vdet-RSSI	Vdet node in limiting amp is muxed to $BIAS_{MON}$; $RSSI_{PP}$ node of limiting amp is muxed to $TxPwr_{MON}$
SC3	ModMon	$TxPwr_{MON}$ output becomes MOD_{MON} output
SC4	Faultbits6	$BIAS_{MON}$ output acts as fault status at V_{CC}THL; $TxPwr_{MON}$ output acts as fault status at V_{CC}THH
SC5	DCR_Filter (C_{AZ})	The DC restore lowpass filter nodes are muxed to $BIAS_{MON}$ and $TxPwr_{MON}$; can add capacitance between these nodes to reduce the LF cutoff of the limiting amplifier
SC6	Faultbits5	$BIAS_{MON}$ output acts as fault status at V_{CC}3THL; $TxPwr_{MON}$ output acts as fault status at V_{CC}3THH
SC7	Faultbits1	$BIAS_{MON}$ output acts as fault status at OUTP; $TxPwr_{MON}$ output acts as fault status at IB_{OUT}
SC8	Faultbits2	$BIAS_{MON}$ output acts as fault status at APC_{SET}; $TxPwr_{MON}$ output acts as fault status at MOD_{SET}
SC9	Faultbits3	$BIAS_{MON}$ output acts as fault status at C_{APC}; $TxPwr_{MON}$ is undefined status bit
SC10	Faultbits4	$BIAS_{MON}$ output acts as fault status at Ipin_hi; $TxPwr_{MON}$ output acts as fault status at Ipin_lo
SC11	Test Mode 1	Internal Use Only; do not use
SC12	DCRDIS	Disables the DC restore in the limiting amplifier. Can pass DC signal through limiting amp, but offset at limiting amplifier input passes through to outputs.
SC13	Test Mode 2	Internal Use Only; do not use
SC14	Test Mode 3	Internal Use Only; do not use

5.0 Package Specification

Figure 5-1. QFN32 Package Information



Note: View is for a 28 pin package. All dimensions in the tables apply for the 32 pin package

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
Q	0.00	0.20	0.45	
D2	3.15	3.30	3.45	
E2	3.15	3.30	3.45	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	-	0.85	0.90	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.70	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	

NOTES:

2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.

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Newport Beach, CA 92660

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