THE DATASHEET OF

LTM8023IV#PBF

2A, 36V DC/DC Step-Down µModule Regulator

FEATURES

- **Complete Step-Down Switch Mode Power Supply**
- **Wide Input Voltage Range: 3.6V to 36V**
- **2A Output Current**
- **0.8V to 10V Output Voltage**
- **Selectable Switching Frequency: 200kHz to 2.4MHz**
- Current Mode Control
- Programmable Soft-Start
- SnPb (BGA) or RoHS Compliant (LGA and BGA) Finish
- Tiny, Low Profile, Surface Mount LGA (9mm × 11.25mm × 2.82mm) and BGA (9mm × 11.25mm × 3.42mm) Packages

APPLICATIONS

- Automotive Battery Regulation
- Power for Portable Products
- Distributed Supply Regulation
- Industrial Supplies
- Wall Transformer Regulation

DESCRIPTION

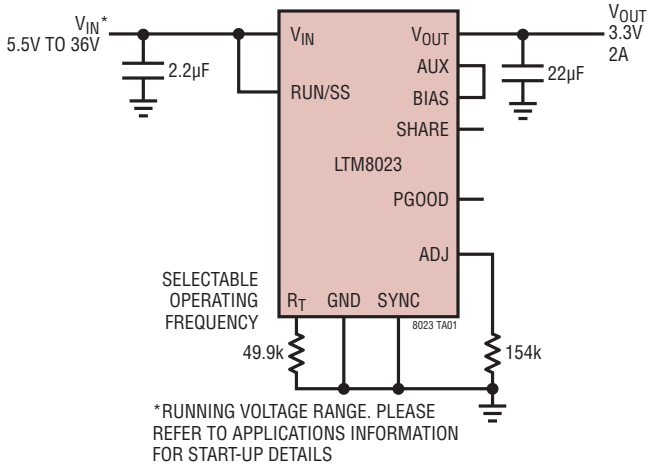
The LTM®8023 is a complete 2A, DC/DC step-down power supply. Included in the package are the switching controller, power switches, inductor, and all support components. Operating over an input voltage range of 3.6V to 36V, the LTM8023 supports an output voltage range of 0.8V to 10V, and a switching frequency range of 200kHz to 2.4MHz, each set by a single resistor. Only the bulk input and output filter capacitors are needed to finish the design.

The low profile package enables utilization of unused space on the bottom of PC boards for high density point of load regulation.

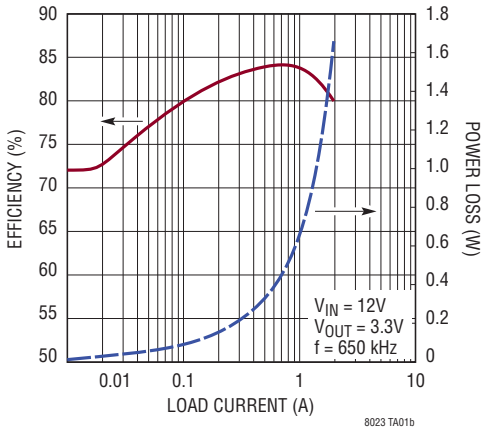
The LTM8023 is packaged in a thermally enhanced, compact and low profile over-molded land grid array (LGA) and ball grid array (BGA) packages suitable for automated assembly by standard surface mount equipment. The LTM8023 is available with SnPb (BGA) or RoHS compliant terminal finish.

TYPICAL APPLICATION

5.5V_{IN} to 36V_{IN}, 3.3V/2A DC/DC µModule® Converter



Efficiency and Power Loss

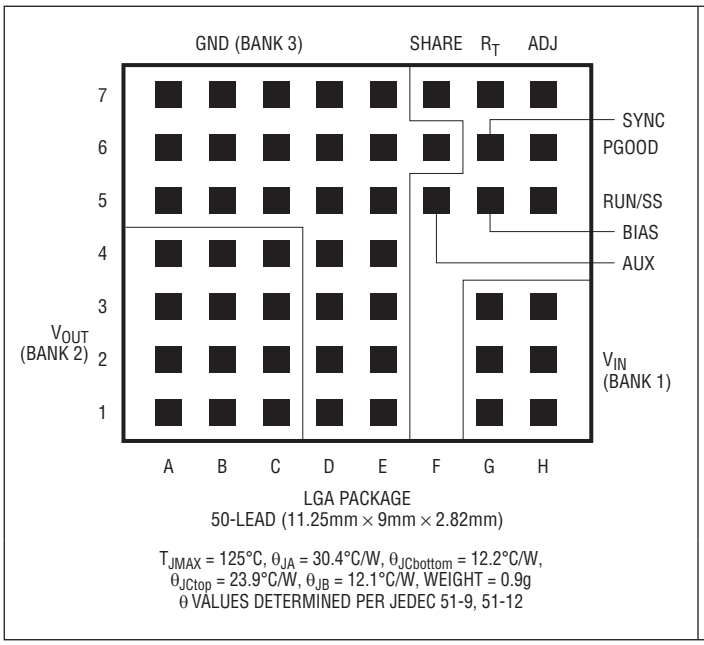


ABSOLUTE MAXIMUM RATINGS

(Note 1)

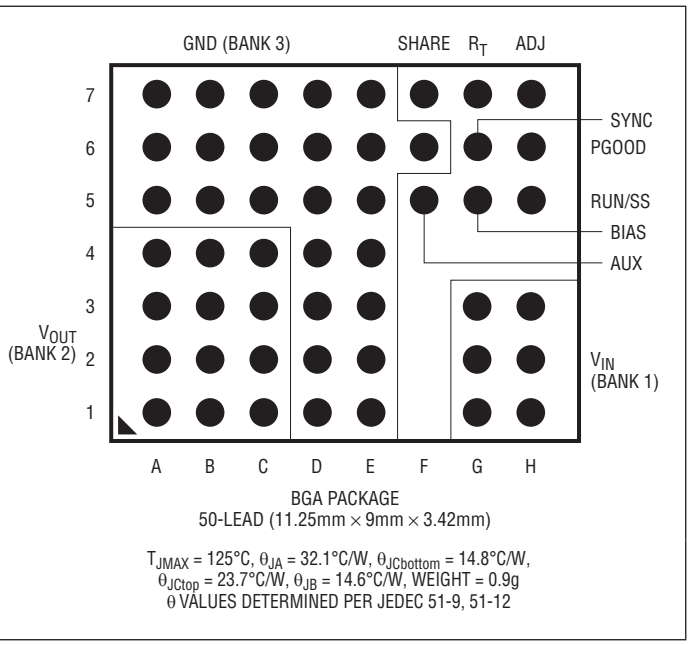
V_{IN}, RUN/SS Voltage.....40V
ADJ, R_T, SHARE Voltage.....5V
V_{OUT}, AUX.....10V
PGOOD, SYNC.....30V
BIAS.....16V
V_{IN} + BIAS.....56V
Internal Operating Temperature
(Note 2).....–40°C to 125°C
Storage Temperature.....–55°C to 125°C
Solder Temperature.....250°C

PIN CONFIGURATION



LGA PACKAGE
50-LEAD (11.25mm × 9mm × 2.82mm)

T_{JMAX} = 125°C, θ_{JA} = 30.4°C/W, $\theta_{JCbottom}$ = 12.2°C/W,
θ_{JCtop} = 23.9°C/W, θ_{JB} = 12.1°C/W, WEIGHT = 0.9g
θ VALUES DETERMINED PER JEDEC 51-9, 51-12



BGA PACKAGE
50-LEAD (11.25mm × 9mm × 3.42mm)

T_{JMAX} = 125°C, θ_{JA} = 32.1°C/W, $\theta_{JCbottom}$ = 14.8°C/W,
θ_{JCtop} = 23.7°C/W, θ_{JB} = 14.6°C/W, WEIGHT = 0.9g
θ VALUES DETERMINED PER JEDEC 51-9, 51-12

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM8023EV#PBF	Au (RoHS)	LTM8023V	e4	LGA	3	–40°C to 85°C
LTM8023IV#PBF	Au (RoHS)	LTM8023V	e4	LGA	3	–40°C to 85°C
LTM8023MPV#PBF	Au (RoHS)	LTM8023MPV	e4	LGA	3	–55°C to 125°C
LTM8023EY#PBF	SAC305 (RoHS)	LTM8023Y	e1	BGA	3	–40°C to 85°C
LTM8023IY#PBF	SAC305 (RoHS)	LTM8023Y	e1	BGA	3	–40°C to 85°C
LTM8023IY	SnPb (63/37)	LTM8023Y	e0	BGA	3	–40°C to 85°C
LTM8023MPY#PBF	SAC305 (RoHS)	LTM8023Y	e1	BGA	3	–55°C to 125°C
LTM8023MPY	SnPb (63/37)	LTM8023Y	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Marking:
  www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures:
  www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings:
  www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, $V_{RUN/SS}$ = 10V, V_{BIAS} = 3V, R_T = 60.4k, C_{OUT} = 4.7µF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	3.6		36	V
V_{OUT}	Output DC Voltage	0A < I_{OUT} ≤ 2A, R_{ADJ} Open, C_{OUT} = 51µF (Note 3) 0A < I_{OUT} ≤ 2A, R_{ADJ} = 43.2k, C_{OUT} = 51µF (Note 3)			0.8 10		V V
$R_{ADJ(MIN)}$	Minimum Allowable R_{ADJ}	(Note 4)		42.2			kΩ
I_{OUT}	Continuous Output DC Current	4 ≤ V_{IN} ≤ 36, C_{OUT} = 51µF		0		2	A
IQ_{VIN}	V_{IN} Quiescent Current	$V_{RUN/SS}$ = 0.2V, R_T = 174k V_{BIAS} = 3V, Not Switching, R_T = 174k (E, I) V_{BIAS} = 3V, Not Switching, R_T = 174k (MP) V_{BIAS} = 0V, Not Switching, R_T = 174k	 ● ● 		0.1 25 25 85	0.5 60 350 120	µA µA µA µA
IQ_{BIAS}	BIAS Quiescent Current	$V_{RUN/SS}$ = 0.2V, R_T = 174k V_{BIAS} = 3V, Not Switching, R_T = 174k (E, I) V_{BIAS} = 3V, Not Switching, R_T = 174k (MP) V_{BIAS} = 0V, Not Switching, R_T = 174k	 ● ● 		0.03 50 50 1	0.5 120 200 5	µA µA µA µA
$\Delta V_{OUT}/V_{OUT}$	Line Regulation	5 ≤ V_{IN} ≤ 36, I_{OUT} = 1A, V_{OUT} = 3.3V, C_{OUT} = 51µF			0.1		%
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	V_{IN} = 24V, 0 ≤ I_{OUT} ≤ 2A, V_{OUT} = 3.3V, C_{OUT} = 51µF			0.4		%
$V_{OUT(AC\_RMS)}$	Output Ripple (RMS)	V_{IN} = 24V, I_{OUT} = 2A, V_{OUT} = 3.3V, C_{OUT} = 51µF			10		mV
f_{SW}	Switching Frequency	R_T = 113k, C_{OUT} = 51µF			325		kHz
$I_{SC(OUT)}$	Output Short Circuit Current	V_{IN} = 36V, V_{OUT} = 0V (Note 5)			2.9		A
V_{ADJ}	Voltage at ADJ Pin	C_{OUT} = 51µF	●	765	790	805	mV
$V_{BIAS(MIN)}$	Minimum BIAS Voltage for Proper Operation				2.3	2.8	V
I_{ADJ}	Current Out of ADJ Pin	ADJ = 1V, C_{OUT} = 51µF			2		µA
$I_{RUN/SS}$	RUN/SS Pin Current	$V_{RUN/SS}$ = 2.5V			5	10	µA
$V_{IH(RUN/SS)}$	RUN/SS Input High Voltage	C_{OUT} = 51µF		2.5			V
$V_{IL(RUN/SS)}$	RUN/SS Input Low Voltage	C_{OUT} = 51µF				0.2	V
$V_{PGOOD(TH)}$	PGOOD Threshold	V_{OUT} Rising			730		mV
$I_{PGOOD(O)}$	PGOOD Leakage	V_{PGOOD} = 30V			0.1	1	µA
$I_{PGOOD(SINK)}$	PGOOD Sink Current	V_{PGOOD} = 0.4V		200	800		µA
V_{SYNCIL}	SYNC Input Low Threshold	f_{SYNC} = 550kHz, C_{OUT} = 51µF				0.5	V
V_{SYNCIH}	SYNC Input High Threshold	f_{SYNC} = 550kHz, C_{OUT} = 51µF		0.7			V
$I_{SYNCBIAS}$	SYNC Pin Bias Current	V_{SYNC} = 0V			0.1		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM8023E is guaranteed to meet performance specifications from 0°C to 85°C ambient. Specifications over the full –40°C to 85°C ambient operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8023I is guaranteed to meet specifications over the full –40°C to 85°C ambient operating temperature range. The LTM8023MP is guaranteed to meet specifications over the full –55°C to 125°C temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

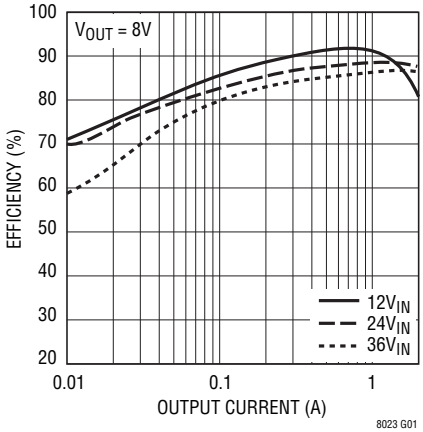
Note 3: C_{OUT} = 51µF is composed of a 4.7µF ceramic capacitor in parallel with a 47µF electrolytic.

Note 4: Guaranteed by design.

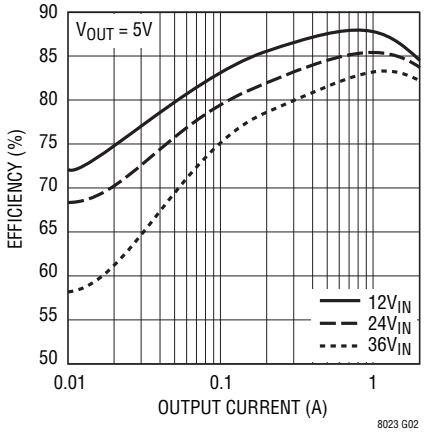
Note 5: Short circuit current at V_{IN} = 36V is guaranteed by characterization and correlation. 100% tested at V_{IN} = 10V

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

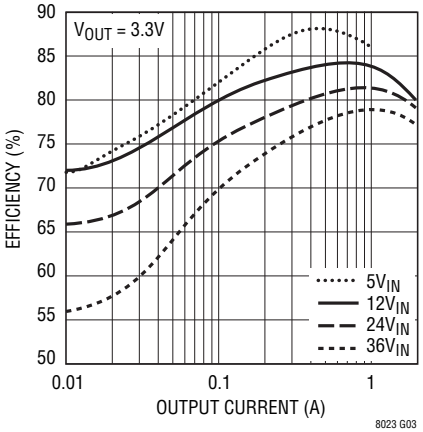
Efficiency ($8V_{OUT}$)



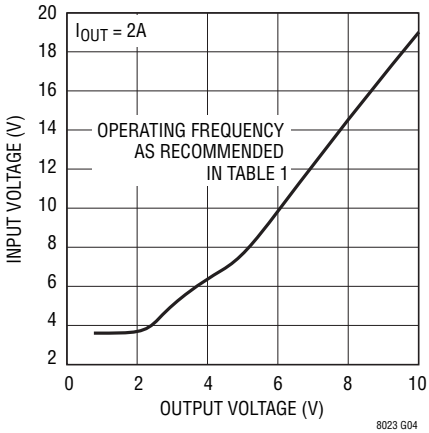
Efficiency ($5V_{OUT}$)



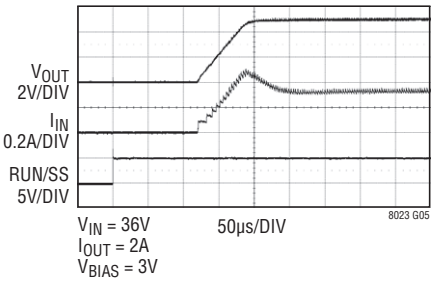
Efficiency ($3.3V_{OUT}$)



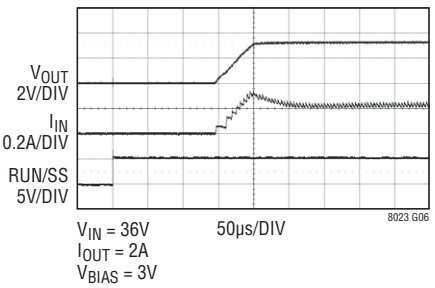
Minimum Required Input Voltage vs Output Voltage



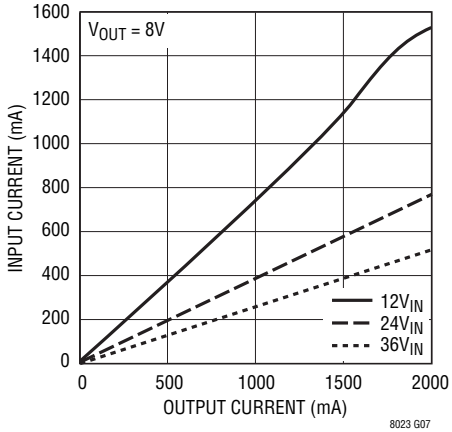
$36V_{IN}$ Start-Up Waveforms ($5V_{OUT}$)



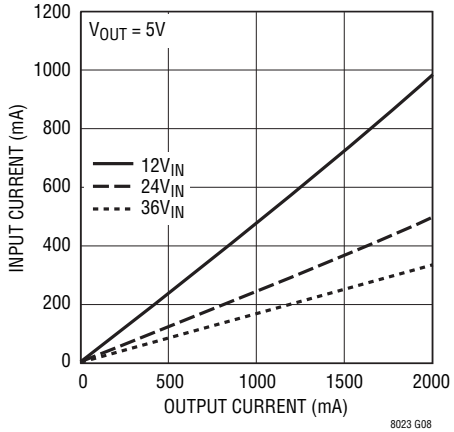
$36V_{IN}$ Start-Up Waveforms ($3.3V_{OUT}$)



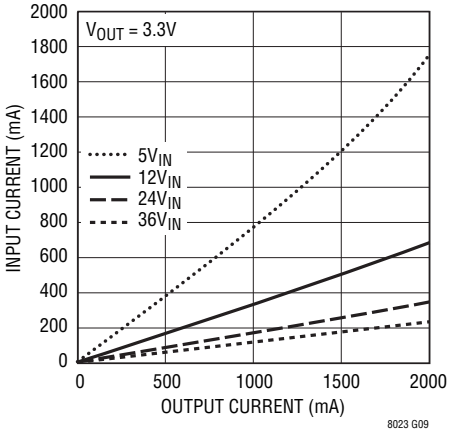
Input Current vs Output Current



Input Current vs Output Current

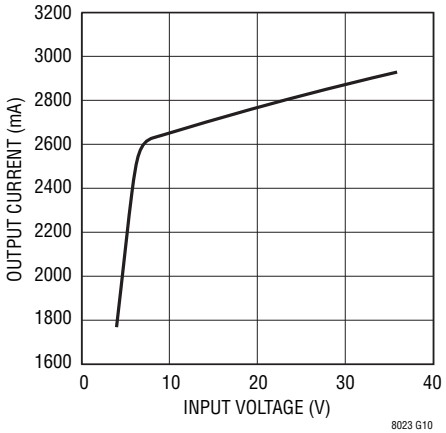


Input Current vs Output Current

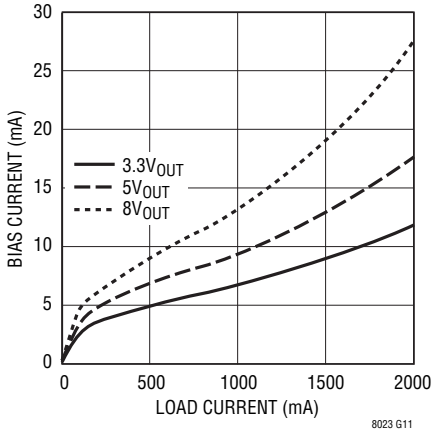


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

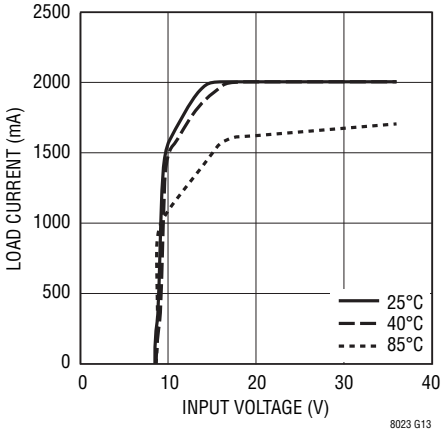
Output Short-Circuit Current vs Input Voltage



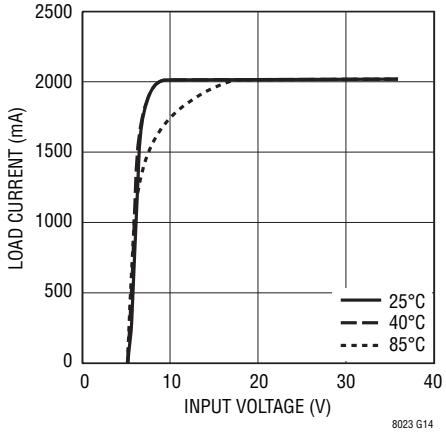
BIAS Current vs Load Current



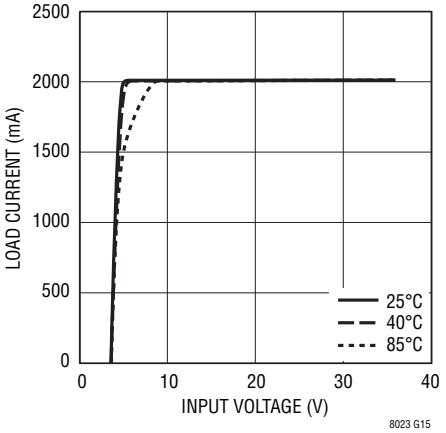
Maximum Load Current vs Input Voltage ($8V_{OUT}$, LGA)



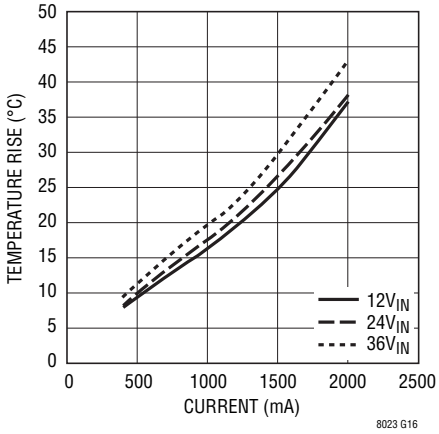
Load Current vs Input Voltage ($5V_{OUT}$, LGA)



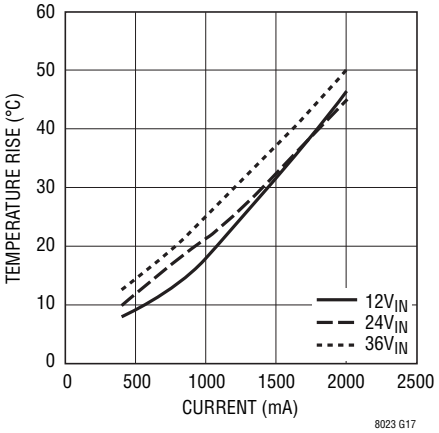
Load Current vs Input Voltage ($3.3V_{OUT}$, LGA)



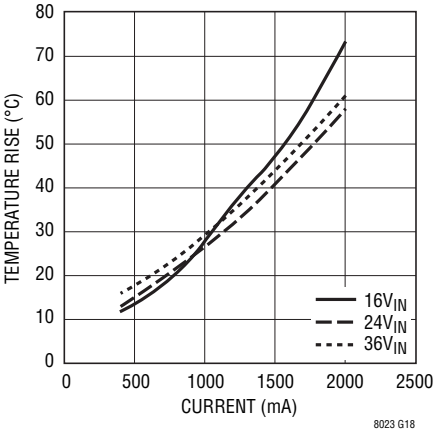
$3.3V_{OUT}$ Junction Temperature vs Load (LGA)



$5V_{OUT}$ Junction Temperature vs Load (LGA)

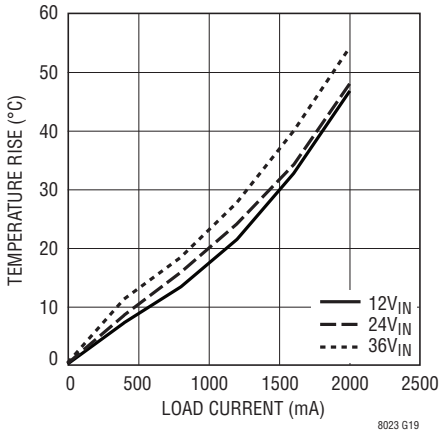


$8V_{OUT}$ Junction Temperature vs Load (LGA)

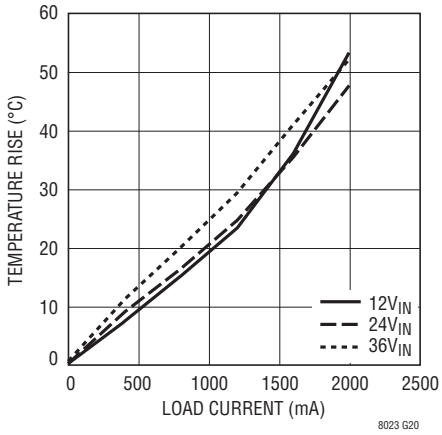


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

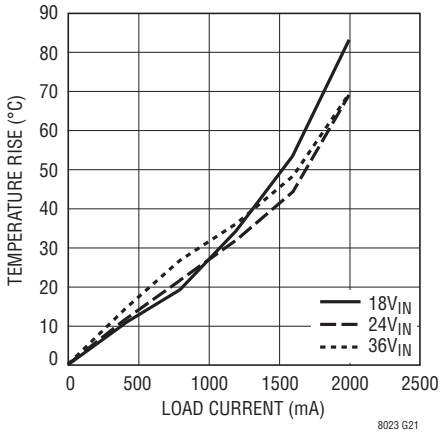
3.3V_{OUT} Temperature Rise vs Load Current (BGA)



5V_{OUT} Temperature Rise vs Load Current (BGA)



8V_{OUT} Temperature Rise vs Load Current (BGA)



PIN FUNCTIONS

V_{IN} (Bank 1): The V_{IN} pin supplies current to the LTM8023's internal regulator and to the internal power switch. This pin must be locally bypassed with an external, low ESR capacitor of at least 2.2µF.

V_{OUT} (Bank 2): Power Output Pins. Apply the output filter capacitor and the output load between these pins and GND pins.

AUX (Pin F5): Low Current Voltage Source for BIAS. The V_{AUX} pin is internally connected to V_{OUT} and is placed adjacent to the BIAS pin to ease printed circuit board routing. Although this pin is internally connected to V_{OUT}, do NOT connect this pin to the load. If this pin is not tied to BIAS, leave it floating.

BIAS (Pin G5): The BIAS pin connects to the internal power bus. Connect to a power source greater than 2.8V. If the output is greater than 2.8V, connect this pin there. If the output voltage is less, connect this to a voltage source between 2.8V and 16V. Also, make sure that BIAS + V_{IN} is less than 56V.

RUN/SS (Pin H5): Tie RUN/SS pin to ground to shut down the LTM8023. Tie to 2.5V or more for normal operation. If the shutdown feature is not used, tie this pin to the V_{IN} pin. RUN/SS also provides a soft-start function; see the Applications Information section.

GND (Bank 3): Tie these GND pins to a local ground plane below the LTM8023 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8023 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Consideration sections for more details. Return the feedback divider (R_{ADJ}) to this net.

R_T (Pin G7): The R_T pin is used to program the switching frequency of the LTM8023 by connecting a resistor from this pin to ground. The Applications Information section of the data sheet includes a table to determine the resistance value based on the desired switching frequency. Minimize capacitance at this pin.

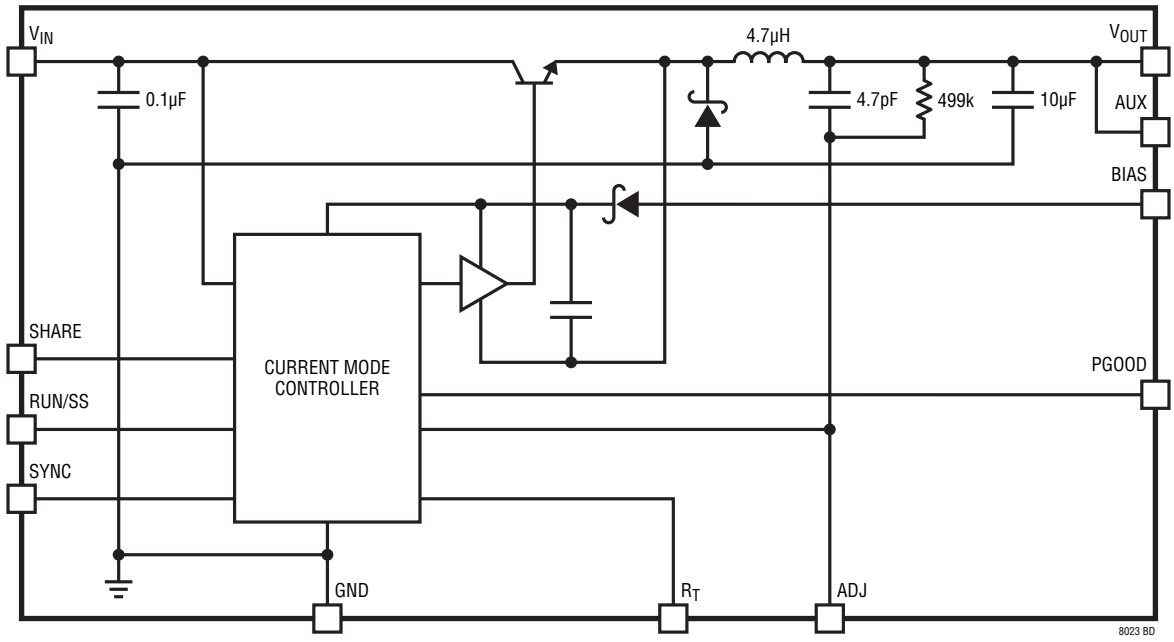
SHARE (Pin F7): Tie this to the SHARE pin of another LTM8023 when paralleling the outputs. Otherwise, do not connect (leave floating).

SYNC (Pin G6): This is the external clock synchronization input. Ground this pin for low ripple Burst Mode® operation at low output loads. Tie to a stable voltage source greater than 0.7V to disable Burst Mode operation. *Do not leave this pin floating*. Tie to a clock source for synchronization. Clock edges should have rise and fall times faster than 1µs. See synchronizing section in Applications Information.

PGOOD (Pin H6): The PGOOD pin is the open-collector output of an internal comparator. PG remains low until the ADJ pin is within 10% of the final regulation voltage. PG output is valid when V_{IN} is above 3.6V and RUN/SS is high. If this function is not used, leave this pin floating.

ADJ (Pin H7): The LTM8023 regulates its ADJ pin to 0.79V. Connect the adjust resistor from this pin to ground. The value of R_{ADJ} is given by the equation $R_{ADJ} = 394.21/(V_{OUT} – 0.79)$, where R_{ADJ} is in kΩ.

BLOCK DIAGRAM



OPERATION

The LTM8023 is a standalone nonisolated step-down switching DC/DC power supply. It can deliver up to 2A of DC output current with only bulk external input and output capacitors. This module provides a precisely regulated output voltage programmable via one external resistor from $0.8V_{DC}$ to $10V_{DC}$. The input voltage range is 3.6V to 36V. Given that the LTM8023 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current. A simplified Block Diagram is given on the previous page.

The LTM8023 contains a current mode controller, power switching element, power inductor, power Schottky diode and a modest amount of input and output capacitance.

The LTM8023 is a fixed frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor value from the R_T pin to GND.

An internal regulator provides power to the control circuitry. The bias regulator normally draws power from the V_{IN} pin, but if the BIAS pin is connected to an external voltage higher than 2.8V, bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency. The RUN/SS pin is used to place the LTM8023 in shutdown, disconnecting the output and reducing the input current to less than 1µA.

To further optimize efficiency, the LTM8023 automatically switches to Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to 50µA in a typical application. The oscillator reduces the LTM8023's operating frequency when the voltage at the ADJ pin is low. This frequency foldback helps to control the output current during start-up and overload.

The LTM8023 contains a power good comparator which trips when the ADJ pin is at 92% of its regulated value. The PGOOD output is an open-collector transistor that is off when the output is in regulation, allowing an external resistor to pull the PGOOD pin high. Power good is valid when the LTM8023 is enabled and V_{IN} is above 3.6V.

APPLICATIONS INFORMATION

For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{ADJ} and R_T values.
3. Connect BIAS as indicated.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

APPLICATIONS INFORMATION

Table 1. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN}	V_{OUT}	C_{IN}	C_{OUT}	R_{ADJ}	BIAS	$f_{OPTIMAL}$ (kHz)	$R_{T(OPTIMAL)}$	f_{MAX} (kHz)	$R_{T(MIN)}$
3.6V to 36V	0.82V	10µF	200µF 1206	13M	≥2.8V, <16V	250	150k	250	150k
3.6V to 36V	1.00V	10µF	147µF 1206	1.87M	≥2.8V, <16V	300	124k	300	124k
3.6V to 36V	1.20V	10µF	100µF 1206	953k	≥2.8V, <16V	350	105k	350	105k
3.6V to 36V	1.50V	10µF	100µF 1206	549k	≥2.8V, <16V	400	88.7k	400	88.7k
3.6V to 36V	1.80V	4.7µF	100µF 1206	383k	≥2.8V, <16V	450	79k	450	79k
3.6V to 36V	2.00V	2.2µF	68µF 1206	324k	≥2.8V, <16V	450	79k	500	69.8k
3.6V to 36V	2.20V	2.2µF	47µF 1206	274k	≥2.8V, <16V	500	69.8k	550	61.9k
4.1V to 36V	2.50V	2.2µF	47µF 1206	226k	≥2.8V, <16V	550	61.9k	615	54.9k
5.5V to 36V	3.30V	2.2µF	22µF 1206	154k	AUX	650	49.9k	750	42.2k
7.5V to 36V	5.00V	2.2µF	10µF 0805	93.1k	AUX	650	49.9k	890	34.8k
3.6V to 15V	0.82V	10µF	200µF 1206	13M	V_{IN}	350	105k	650	49.9k
3.6V to 15V	1.00V	10µF	147µF 1206	1.87M	V_{IN}	400	88.7k	725	43.2k
3.6V to 15V	1.20V	10µF	100µF 1206	953k	V_{IN}	450	79k	800	39.2k
3.6V to 15V	1.50V	10µF	100µF 1206	549k	V_{IN}	450	79k	1000	29.4k
3.6V to 15V	1.80V	4.7µF	100µF 1206	383k	V_{IN}	450	79k	1100	26.7k
3.6V to 15V	2.00V	2.2µF	68µF 1206	324k	V_{IN}	450	79k	1200	23.7k
3.6V to 15V	2.20V	2.2µF	47µF 1206	274k	V_{IN}	500	69.8k	1300	21.0k
3.6V to 15V	2.50V	2.2µF	47µF 1206	226k	V_{IN}	550	61.9k	1450	18.2k
5.5V to 15V	3.30V	2.2µF	22µF 1206	154k	AUX	650	49.9k	1400	19.6k
7.5V to 15V	5.00V	2.2µF	10µF 0805	93.1k	AUX	650	49.9k	1200	23.7k
9V to 24V	0.82V	10µF	200µF 1206	13M	≥2.8V, <16V	250	150k	250	150k
9V to 24V	1.00V	10µF	147µF 1206	1.87M	≥2.8V, <16V	300	124k	450	79k
9V to 24V	1.20V	2.2µF	100µF 1206	953k	≥2.8V, <16V	450	79k	500	69.8k
9V to 24V	1.50V	2.2µF	100µF 1206	549k	≥2.8V, <16V	450	79k	615	54.9k
9V to 24V	1.80V	2.2µF	100µF 1206	383k	≥2.8V, <16V	450	79k	700	44.2k
9V to 24V	2.00V	2.2µF	68µF 1206	324k	≥2.8V, <16V	450	79k	750	42.2k
9V to 24V	2.20V	2.2µF	47µF 1206	274k	≥2.8V, <16V	500	69.8k	800	39.2k
9V to 24V	2.50V	2.2µF	47µF 1206	226k	≥2.8V, <16V	550	61.9k	890	34.8k
9V to 24V	3.30V	2.2µF	22µF 1206	154k	AUX	650	49.9k	1150	25.5k
9V to 24V	5.00V	2.2µF	10µF 0805	93.1k	AUX	650	49.9k	1000	29.4k
14.5V to 24V	8.00V	2.2µF	10µF 0805	53.6k	AUX	650	49.9k	800	39.2k
18V to 36V	0.82V	10µF	200µF 1206	13M	≥2.8V, <16V	250	150k	250	150k
18V to 36V	1.00V	10µF	147µF 1206	1.87M	≥2.8V, <16V	300	124k	300	124k
18V to 36V	1.20V	2.2µF	100µF 1206	953k	≥2.8V, <16V	350	105k	350	105k
18V to 36V	1.50V	2.2µF	100µF 1206	549k	≥2.8V, <16V	400	88.7k	400	88.7k
18V to 36V	1.80V	2.2µF	100µF 1206	383k	≥2.8V, <16V	450	79k	450	79k
18V to 36V	2.00V	2.2µF	68µF 1206	324k	≥2.8V, <16V	450	79k	500	69.8k
18V to 36V	2.20V	2.2µF	47µF 1206	274k	≥2.8V, <16V	450	79k	550	61.9k
18V to 36V	2.50V	2.2µF	47µF 1206	226k	≥2.8V, <16V	500	69.8k	615	54.9k
18V to 36V	3.30V	2.2µF	22µF 1206	154k	AUX	650	49.9k	750	42.2k
18V to 36V	5.00V	2.2µF	10µF 0805	93.1k	AUX	800	39.2k	890	34.8k
18V to 36V	8.00V	2.2µF	10µF 0805	53.6k	AUX	650	49.9k	800	39.2k
20V to 36V	10.00V	2.2µF	10µF 0805	42.2k	AUX	615	54.9k	750	42.2k
4.75V to 32V	–3.30V	2.2µF	22µF 1206	154k	AUX	550	61.9k	800	39.2k
7V to 31V	–5.00V	2.2µF	10µF 0805	93.1k	AUX	800	39.2k	1100	26.7k
15V to 28V	–8.00V	2.2µF	10µF 0805	53.6k	AUX	800	39.2k	1600	15.8k

A bulk input capacitor is required.

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Ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8023's switching frequency depends on the load current, and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8023 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear.

If this audible noise is unacceptable, use a high performance electrolytic capacitor at the output. The input capacitor can be a parallel combination of a 2.2µF ceramic capacitor and a low cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8023. A ceramic input capacitor combined with trace or cable inductance forms a high Q (under damped) tank circuit. If the LTM8023 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Frequency Selection

The LTM8023 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 2.4MHz by using a resistor tied from the R_T pin to ground. Table 2 provides a list of R_T resistor values and their resultant frequencies.

Table 2. Switching Frequency vs R_T Value

SWITCHING FREQUENCY (MHz)	R_T VALUE (kΩ)
0.2	187
0.3	124
0.4	88.7
0.5	69.8
0.6	56.2
0.7	46.4
0.8	39.2
0.9	34.6
1.0	29.4
1.2	23.7
1.4	19.6
1.6	15.8
1.8	13.3
2.0	11.5
2.2	9.76
2.4	8.66

Operating Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8023 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8023 if the output is overloaded or short circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

The maximum frequency (and attendant R_T value) at which the LTM8023 should be allowed to switch is given in Table 1 in the $f_{(MAX)}$ column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the $f_{OPTIMAL}$ column.

There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

BIAS Pin Considerations

The BIAS pin is used to provide drive power for the internal power switching stage and operate internal circuitry. For proper operation, it must be powered by at least 2.8V. If the output voltage is programmed to be 2.8V or higher, simply tie BIAS to V_{OUT}. If V_{OUT} is less than 2.8V, BIAS can be tied to V_{IN} or some other voltage source. In all cases, ensure that the maximum voltage at the BIAS pin is both less than 16V and the sum of V_{IN} and BIAS is less than 56V. If BIAS power is applied from a remote or noisy voltage source, it may be necessary to apply a decoupling capacitor locally to the LTM8023.

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Load Sharing

Two or more LTM8023's may be paralleled to produce higher currents. To do this, tie the V_{IN}, ADJ, V_{OUT} and SHARE pins of all the paralleled LTM8023's together. To ensure that paralleled modules start up together, the RUN/SS pins may be tied together, as well. If the RUN/SS pins are not tied together, make sure that the same valued soft-start capacitors are used for each module. An example of two LTM8023 modules configured for load sharing is given in the Typical Applications section.

For current sharing applications using multiple LTM8023s, the ADJ pins for all regulators may be combined using one resistor to ground as determined by:

$$R_{ADJ} = \frac{\frac{394.21}{N}}{V_{OUT} - 0.79}$$

where N is the number of paralleled modules and R_{ADJ} is in kΩ.

Burst Mode Operation

To enhance efficiency at light loads, the LTM8023 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LTM8023 delivers single cycle bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. In addition, V_{IN} and BIAS quiescent currents are reduced to typically 25µA and 50µA respectively during the sleep time. As the load current decreases towards a no load condition, the percentage of time that the LTM8023 operates in sleep mode increases and the average input current is greatly reduced, resulting in higher efficiency.

Burst Mode operation is enabled by tying SYNC to GND. To disable Burst Mode operation, tie SYNC to a stable voltage above 0.7V or synchronize to an external clock. *Do not leave the SYNC pin floating.*

Minimum Input Voltage

The LTM8023 is a step-down converter, so a minimum amount of headroom is required to keep the output in regulation. In addition, the input voltage required to turn on is higher than that required to run, and depends upon whether the RUN/SS is used. As shown in Figure 2, it takes only about $3.5V_{IN}$ for the LTM8023 to run a 3.3V output at light load. If RUN/SS is tied to V_{IN}, a 5.5V input voltage is required to start. If V_{IN} is allowed to settle in the operating region first then the RUN/SS pin is enabled, the minimum input voltage to start at light load is lower, about 4.2V. A similar curve for $5V_{OUT}$ operation is also provided in Figure 2.

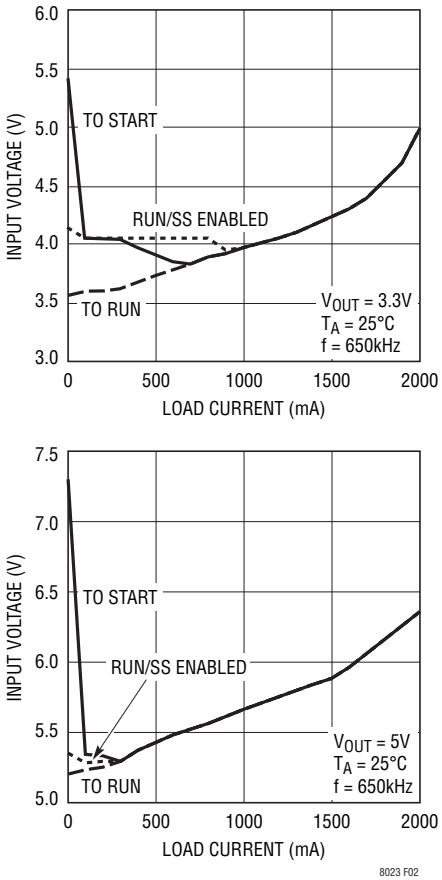

Figure 2. The LTM8023 Needs More Voltage to Start Than to Run

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Soft-Start

The RUN/SS pin can be used to soft-start the LTM8023, reducing the maximum input current during start-up. The RUN/SS pin is driven through an external RC filter to create a voltage ramp at this pin. Figure 3 shows the start-up and shutdown waveforms with the soft-start circuit. By choosing an appropriate RC time constant, the peak start-up current can be reduced to the current that is required to regulate the output, with no overshoot. Choose the value of the resistor so that it can supply at least 20µA when the RUN/SS pin reaches 2.5V.

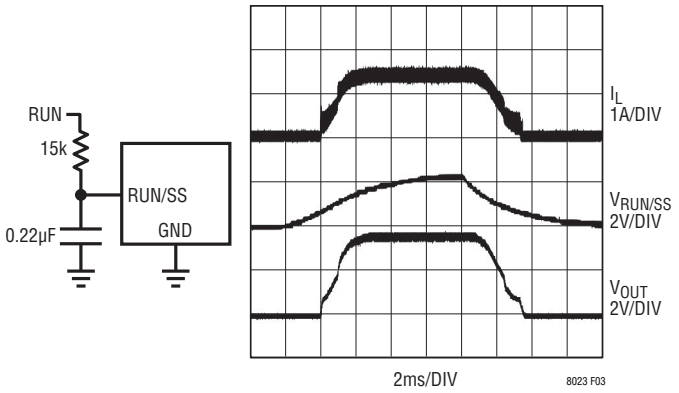

Figure 3. To Soft-Start the LTM8023, Add a Resistor and Capacitor to the RUN/SS Pin

Synchronization

The internal oscillator of the LTM8023 can be synchronized by applying an external 250kHz to 2MHz clock to the SYNC pin. *Do not leave this pin floating*. The resistor tied from the R_T pin to ground should be chosen such that the LTM8023 oscillates 20% lower than the intended synchronization frequency (see the Frequency Selection section).

The LTM8023 will not enter Burst Mode operation while synchronized to an external clock, but will instead skip pulses to maintain regulation.

Shorted Input Protection

Care needs to be taken in systems where the output will be held high when the input to the LTM8023 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR-ed with the LTM8023's output. If the V_{IN} pin is allowed to float and the RUN/SS pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LTM8023's internal circuitry will pull its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN/SS pin, the internal power switch current will drop to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LTM8023 can pull large currents from the output through the V_{IN} pin. Figure 4 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

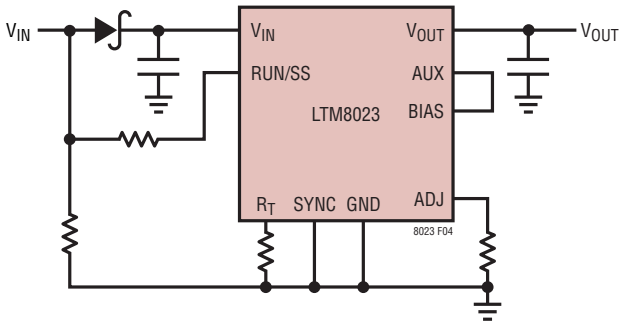

Figure 4. The Input Diode Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LTM8023 Runs Only When the Input is Present.

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PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8023. The LTM8023 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 5 for a suggested layout.

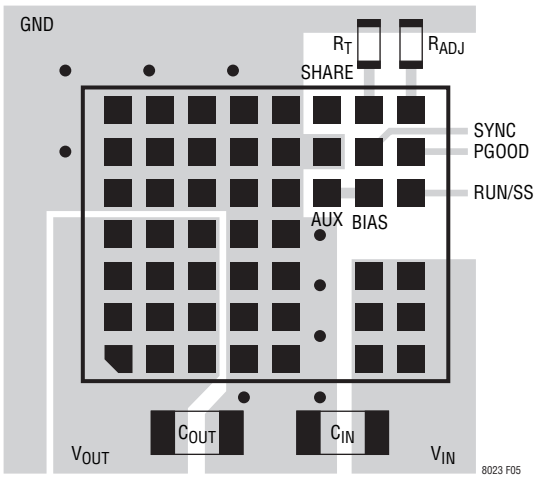

Figure 5. Layout Showing Suggested External Components, GND Plane and Thermal Vias

Ensure that the grounding and heatsinking are acceptable. A few rules to keep in mind are:

1. Place the R_{ADJ} and R_T resistors as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8023.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8023.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground current flow directly adjacent or underneath the LTM8023.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8023.
6. Use vias to connect the GND copper area to the boards internal ground plane. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board.

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8023. However, these capacitors can cause problems if the LTM8023 is plugged into a live supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8023 can ring to twice the nominal input voltage, possibly exceeding the LTM8023's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8023 into an energized supply, the input network should be designed to prevent this overshoot. Figure 6 shows the waveforms that result when an LTM8023 circuit is connected to a 24V supply through six feet of 24-gauge twisted pair. The first plot is the response with a 2.2µF ceramic capacitor at the input. The input voltage rings as high as 35V and the input current peaks at 20A. One method of damping the tank circuit is to add another capacitor with a series resistor to the circuit. In Figure 6c an aluminum electrolytic capacitor has been added. This capacitor's high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency

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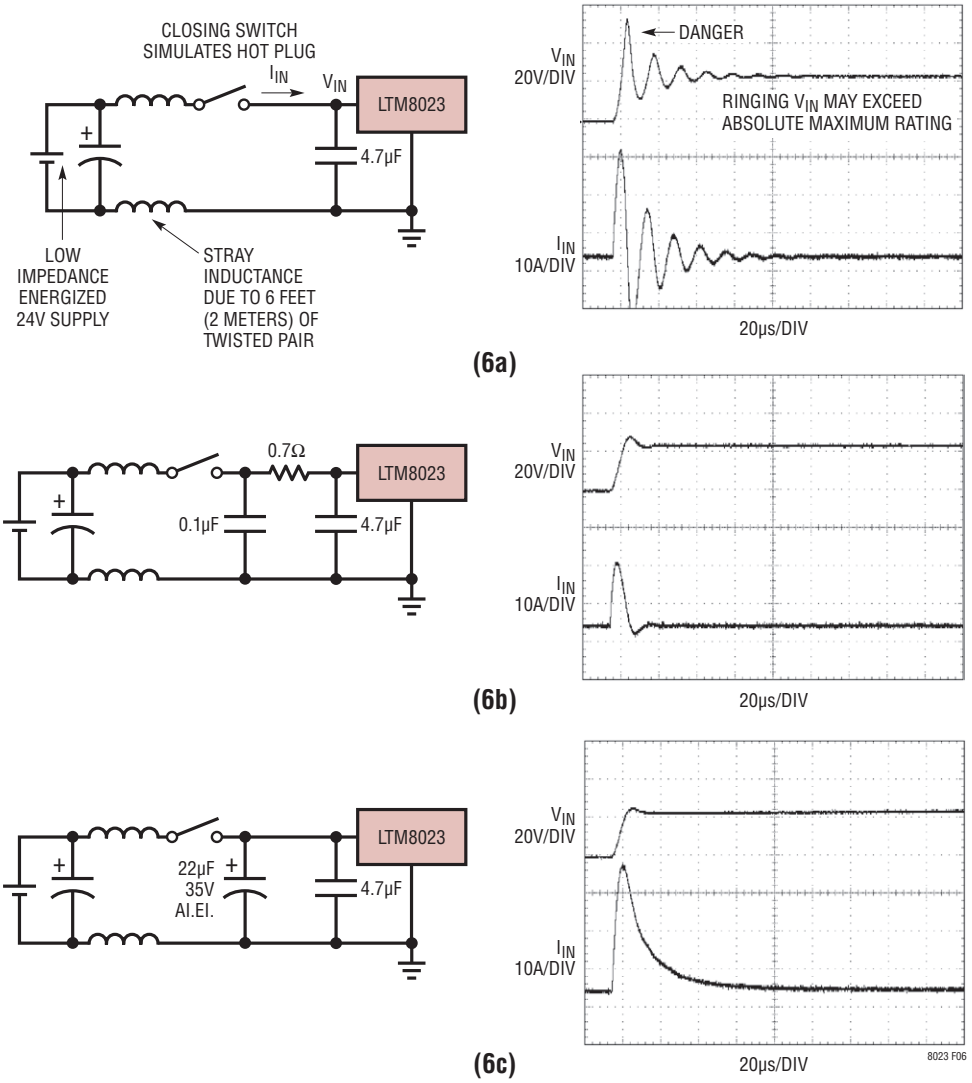

Figure 6. A Well Chosen Input Network Prevents Input Voltage Overshoot and Ensures Reliable Operation When the LTM8023 is Connected to a Live Supply

ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit. An alternative solution is shown in Figure 6b. A 0.7Ω resistor is added in series with the input to eliminate the voltage overshoot (it also reduces the peak input current). A 0.1µF capacitor improves high frequency filtering. This solution is smaller and less expensive than the electrolytic capacitor. For high input voltages its impact on efficiency is minor, reducing efficiency less than one-half percent for a 5V output at full load operating from 24V.

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Thermal Considerations

The LTM8023 output current may need to be derated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by an LTM8023 mounted to a 33cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

The thermal resistance numbers listed in the Pin Configuration are based on modeling the µModule package mounted on a test board specified per JESD51-9 "Test Boards for Area Array Surface Mount Package Thermal Measurements." The thermal coefficients provided in this page are based on JESD 51-12 "Guidelines for Reporting and Using Electronic Package Thermal Information."

For increased accuracy and fidelity to the actual application, many designers use FEA to predict thermal performance. To that end, the Pin Configuration typically gives four thermal coefficients:

- θ_{JA} – Thermal resistance from junction to ambient.
- $\theta_{JCbottom}$ – Thermal resistance from junction to the bottom of the product case.
- θ_{JCtop} – Thermal resistance from junction to top of the product case.
- θ_{JB} – Thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased in the following:

- θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
- $\theta_{JCbottom}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
- θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.
- θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

The most appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously. None of them can be individually used to accurately predict the thermal performance of the product, so it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature versus load graphs given in the LTM8023 data sheet.

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A graphical representation of these thermal resistances is given in Figure 7.

The blue resistances are contained within the µModule regulator, and the green are outside.

The die temperature of the LTM8023 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8023. The bulk of the heat flow out of the LTM8023 is through the bottom of the module and the LGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

Finally, be aware that at high ambient temperatures the internal Schottky diode will have significant leakage current increasing the quiescent current of the LTM8023.

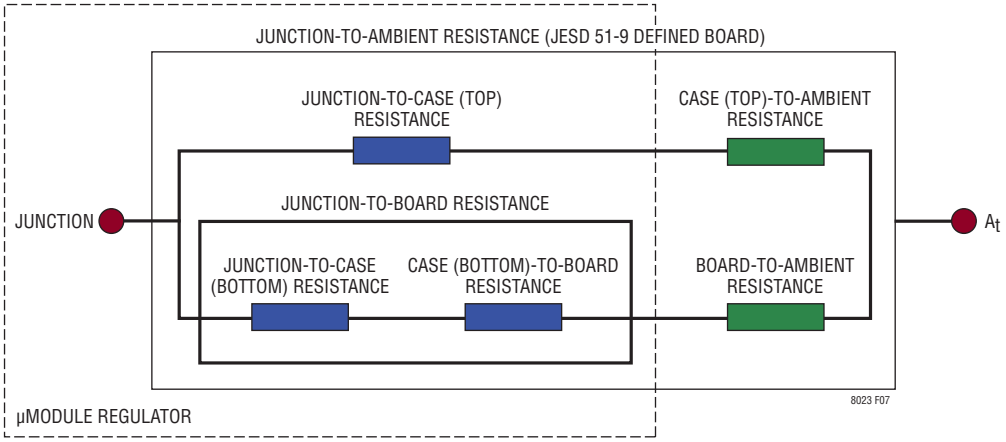
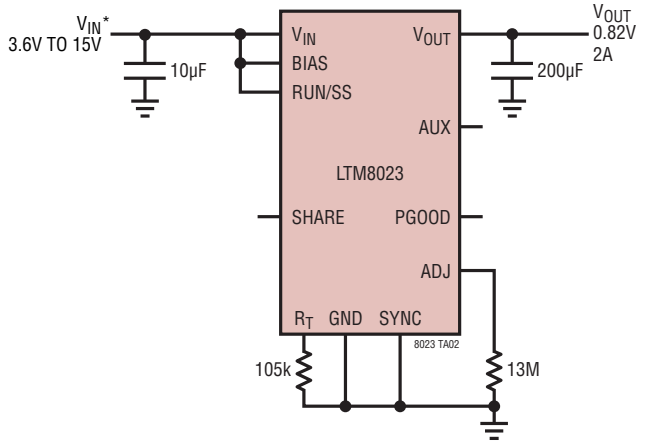


Figure 7

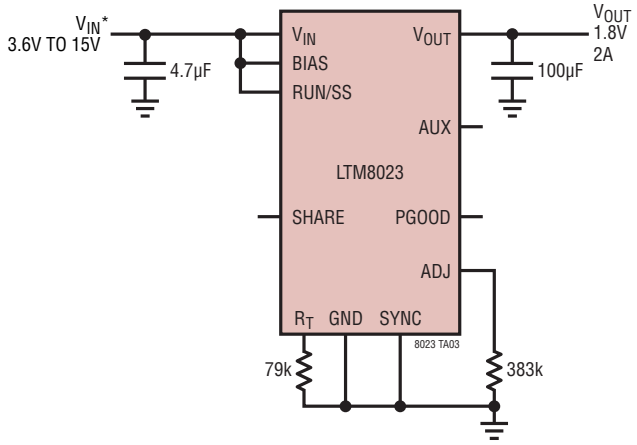
TYPICAL APPLICATIONS

0.82V Step-Down Converter



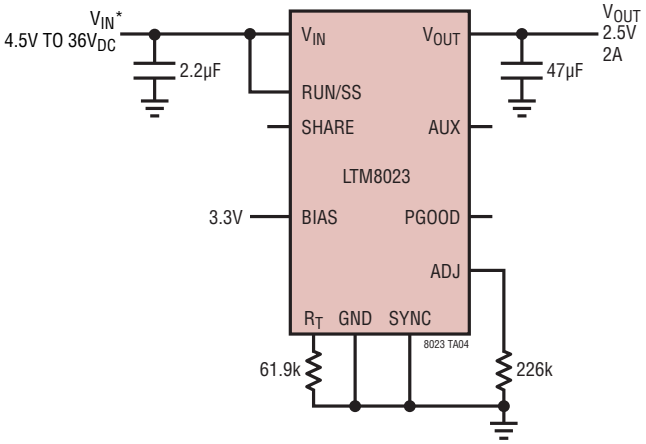
*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION FOR START-UP DETAILS

1.8V Step-Down Converter



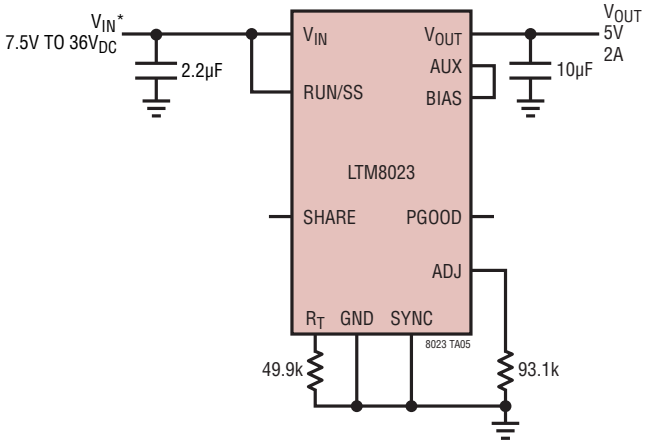
*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION FOR START-UP DETAILS

2.5V Step-Down Converter

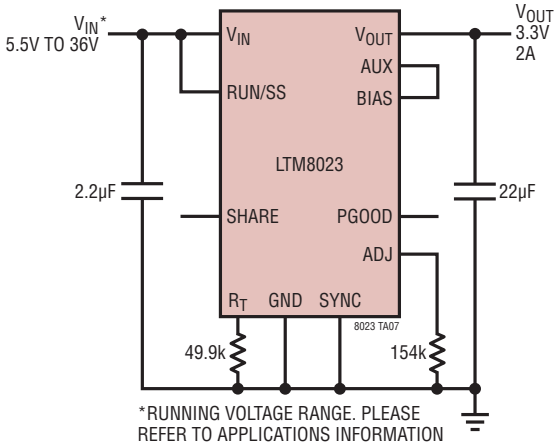


*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION FOR START-UP DETAILS

5V Step-Down Converter



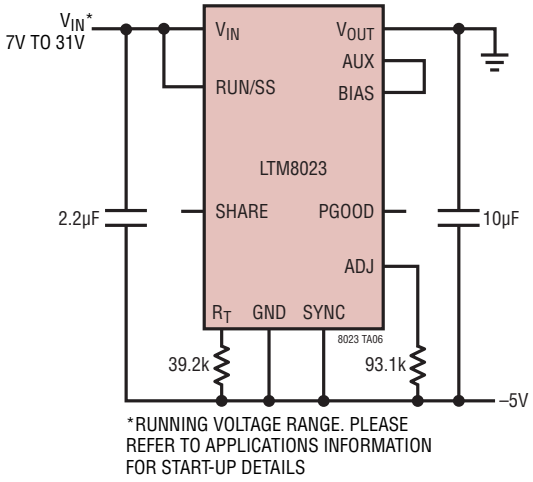
*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION FOR START-UP DETAILS



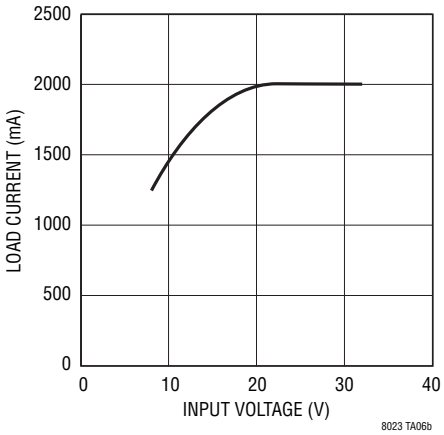
*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION FOR START-UP DETAILS

TYPICAL APPLICATIONS

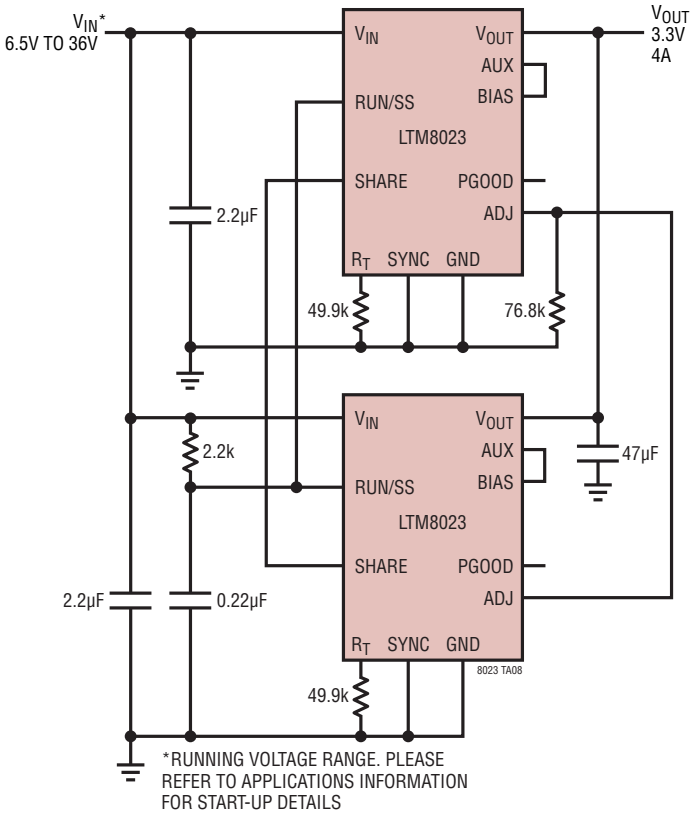
–5V Positive to Negative Converter



–5V Positive to Negative Converter Load Current vs Input Voltage

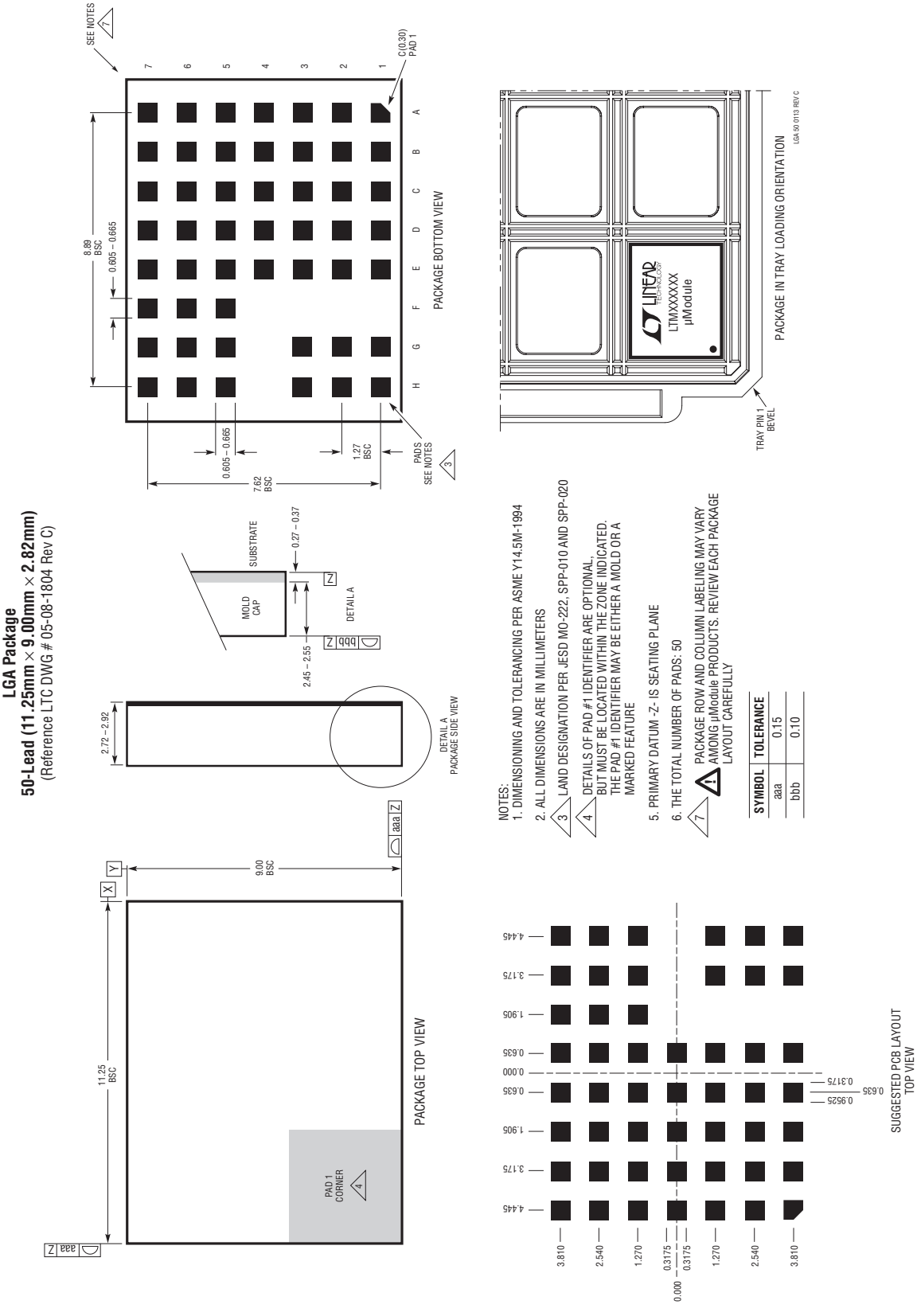


Two LTM8023's in Parallel, 3.3V at 4A



PACKAGE DESCRIPTION

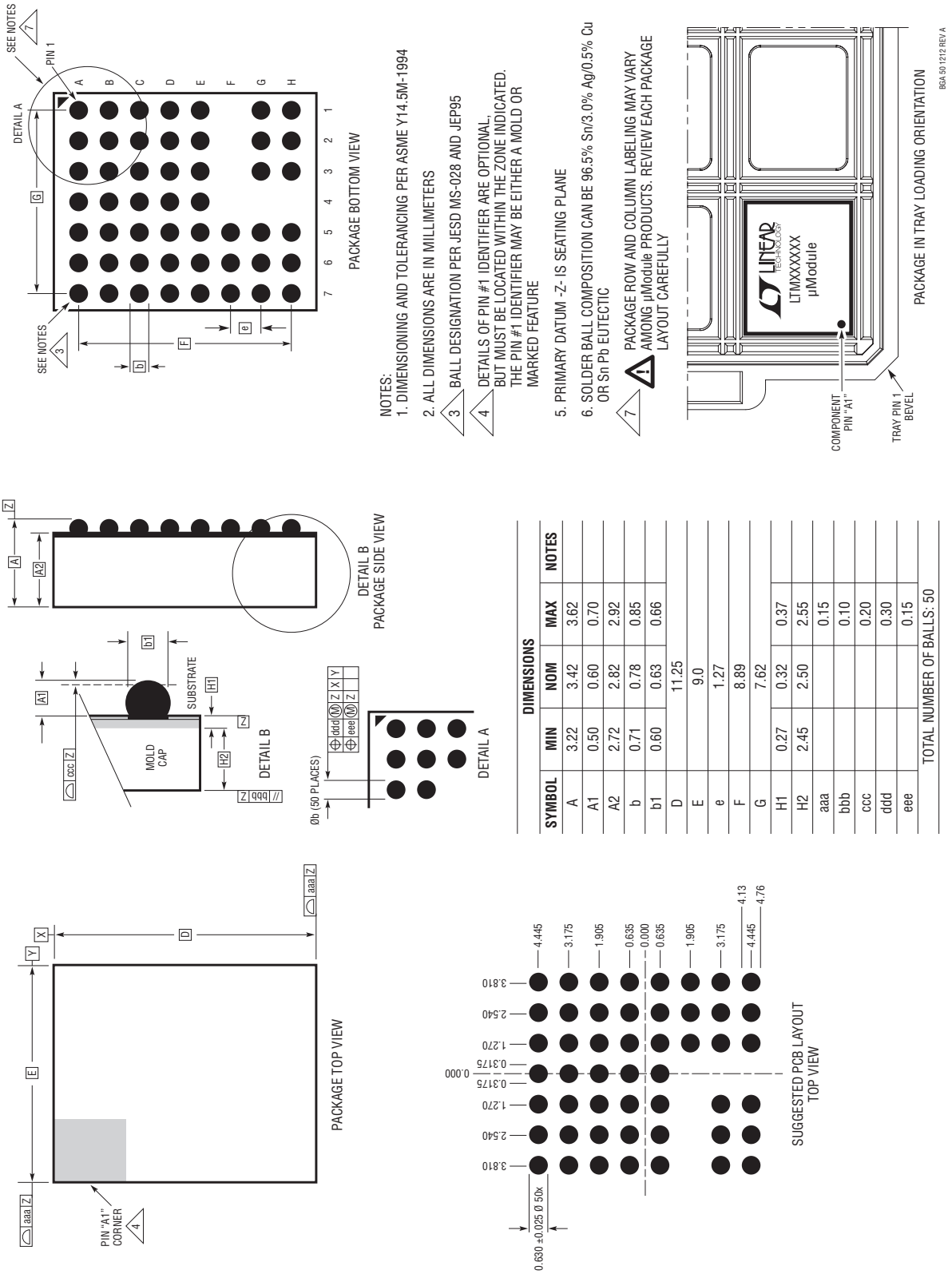
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

BGA Package
50-Lead (11.25mm × 9.00mm × 3.42mm)
(Reference LTC DWG # 05-08-1883 Rev A)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	3.22	3.42	3.62	
A1	0.50	0.60	0.70	
A2	2.72	2.82	2.92	
b	0.71	0.78	0.85	
b1	0.60	0.63	0.66	
D		11.25		
E		9.0		
e		1.27		
F		8.89		
G		7.62		
H1	0.27	0.32	0.37	
H2	2.45	2.50	2.55	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 50				

PACKAGE DESCRIPTION

Table 3. Pin Assignment (Sorted by Pin Number)

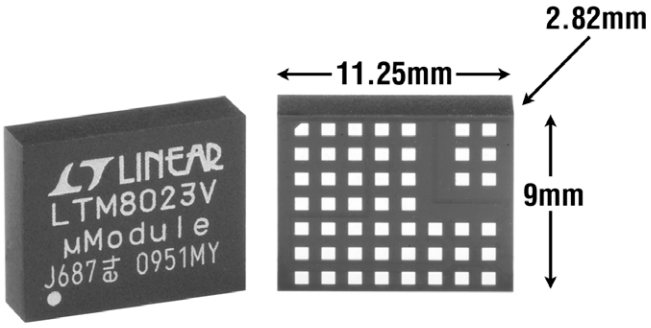
PIN	SIGNAL DESCRIPTION	PIN	SIGNAL DESCRIPTION
A1	V_{OUT}	D5	GND
A2	V_{OUT}	D6	GND
A3	V_{OUT}	D7	GND
A4	V_{OUT}	E1	GND
A5	GND	E2	GND
A6	GND	E3	GND
A7	GND	E4	GND
B1	V_{OUT}	E5	GND
B2	V_{OUT}	E6	GND
B3	V_{OUT}	E7	GND
B4	V_{OUT}	F5	AUX
B5	GND	F6	GND
B6	GND	F7	SHARE
B7	GND	G1	V_{IN}
C1	V_{OUT}	G2	V_{IN}
C2	V_{OUT}	G3	V_{IN}
C3	V_{OUT}	G5	BIAS
C4	V_{OUT}	G6	SYNC
C5	GND	G7	R_T
C6	GND	H1	V_{IN}
C7	GND	H2	V_{IN}
D1	GND	H3	V_{IN}
D2	GND	H5	RUN/SS
D3	GND	H6	PGOOD
D4	GND	H7	ADJ

REVISION HISTORY (Revision history begins at Rev F)

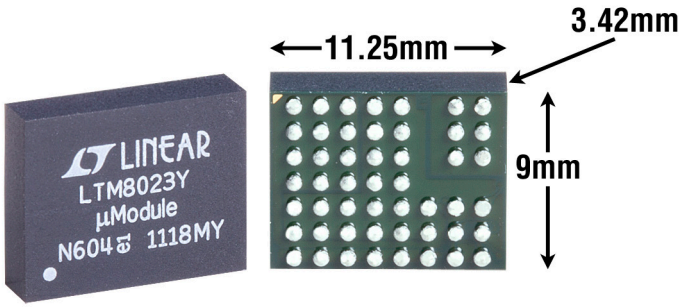
REV	DATE	DESCRIPTION	PAGE NUMBER
F	8/10	Added Note 5	3
G	8/11	Added BGA package. Changes reflected throughout the data sheet.	1 to 24
H	8/13	Changed output capacitor from 2.2µF to 22µF	1
I	2/14	Added SnPb BGA package option	1, 2
J	8/15	Updated thermal impedance values	2

PACKAGE PHOTOGRAPHS

LGA



BGA



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8022	36V, 1A Step-Down µModule Regulator	$0.8V \le V_{OUT} \le 10V$, Synchronizable, 9mm × 11.25mm × 2.8mm LGA
LTM8025	36V, 3A Step-Down µModule Regulator	$0.8V \le V_{OUT} \le 24V$, Synchronizable, 9mm × 15mm × 4.3mm LGA
LTM8027	60V, 4A Step-Down µModule Regulator	$2.5V \le V_{OUT} \le 24V$, Synchronizable, 15mm × 15mm × 4.3mm LGA
LTM4612	EN55022B Certified 36V, 5A Step-Down µModule Regulator	$3.3V \le V_{OUT} \le 15V$, Synchronizable, 15mm × 15mm × 2.8mm LGA
LTM4613	EN55022B Certified 36V, 8A Step-Down µModule Regulator	$3.3V \le V_{OUT} \le 15V$, Synchronizable, 15mm × 15mm × 4.3mm LGA
LTM8061	32V, 2A Li-Ion/Li-Polymer µModule Battery Charger	C/10 or Timer Termination, Auto-Recharge, Programmable Charge Current, 9mm × 15mm × 4.3mm LGA

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