THE DATASHEET OF

LTC4441IMSE#TRPBF

N-Channel MOSFET Gate Driver

FEATURES

- **6A Peak Output Current**
- **Wide V_{IN} Supply Range: 5V to 25V**
- **Adjustable Gate Drive Voltage: 5V to 8V**
- **Logic Input Can Be Driven Below Ground**
- 30ns Propagation Delay
- Supply Independent CMOS/TTL Input Thresholds
- Undervoltage Lockout
- Low Shutdown Current: <12µA
- Overtemperature Protection
- Adjustable Blanking Time for MOSFET's Current Sense Signal (LTC4441)
- Available in SO-8 and 10-Lead MSOP (Exposed Pad) Packages

APPLICATIONS

- Power Supplies
- Motor/Relay Control
- Line Drivers
- Charge Pumps

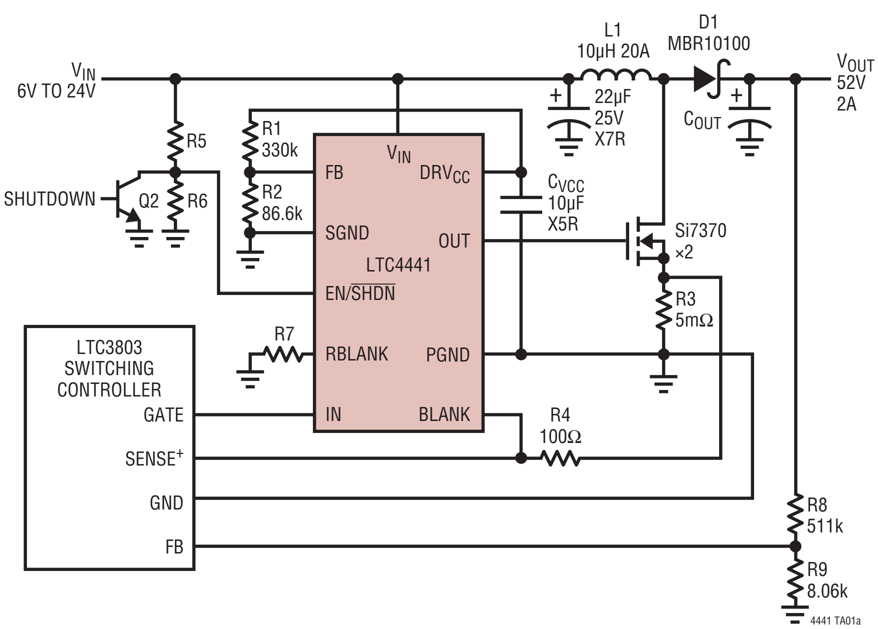
DESCRIPTION

The LTC®4441/LTC4441-1 is an N-channel MOSFET gate driver that can supply up to 6A of peak output current. The chip is designed to operate with a supply voltage of up to 25V and has an adjustable linear regulator for the gate drive. The gate drive voltage can be programmed between 5V and 8V.

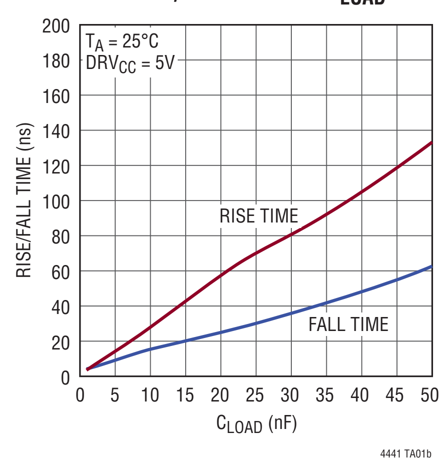
The LTC4441/LTC4441-1 features a logic threshold driver input. This input can be driven below ground or above the driver supply. A dual function control input is provided to disable the driver or to force the chip into shutdown mode with <12µA of supply current. Undervoltage lockout and overtemperature protection circuits will disable the driver output when activated. The LTC4441 also comes with an open-drain output that provides adjustable leading edge blanking to prevent ringing when sensing the source current of the power MOSFETs.

The LTC4441 is available in a thermally enhanced 10-lead MSOP package. The LTC4441-1 is the SO-8 version without the blanking function.

TYPICAL APPLICATION



RISE/FALL Time vs C_{LOAD}

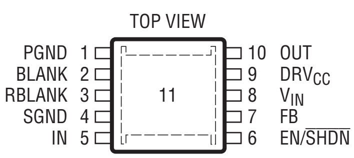


ABSOLUTE MAXIMUM RATINGS (Notes 1, 8)

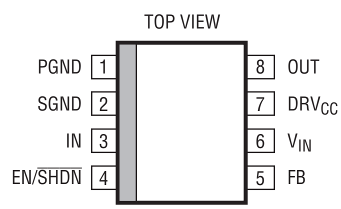
Supply Voltage
V_{IN} 28V
DRV_{CC} 9V
Input Voltage
IN ....–15V to 15V
FB, EN/$\overline{SHDN}$ ....–0.3V to DRV_{CC} + 0.3V
RBLANK, BLANK (LTC4441 Only)........... –0.3V to 5V

OUT Output Current 100mA
Operating Junction Temperature Range
(Note 2).. –55°C to 125°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec).................. 300°C

PIN CONFIGURATION



MSE PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 38°C/W (Note 3)
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4441EMSE#PBF	LTC4441EMSE#TRPBF	LTBJQ	10-Lead Plastic MSOP	–40°C to 125°C
LTC4441IMSE#PBF	LTC4441IMSE#TRPBF	LTBJP	10-Lead Plastic MSOP	–40°C to 125°C
LTC4441MPMSE#PBF	LTC4441MPMSE#TRPBF	LTBJP	10-Lead Plastic MSOP	–55°C to 125°C
LTC4441ES8-1#PBF	LTC4441ES8-1#TRPBF	44411	8-Lead Plastic SO	–40°C to 125°C
LTC4441IS8-1#PBF	LTC4441IS8-1#TRPBF	4441I1	8-Lead Plastic SO	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC4441EMSE	LTC4441EMSE#TR	LTBJQ	10-Lead Plastic MSOP	–40°C to 125°C
LTC4441IMSE	LTC4441IMSE#TR	LTBJP	10-Lead Plastic MSOP	–40°C to 125°C
LTC4441MPMSE	LTC4441MPMSE#TR	LTBJP	10-Lead Plastic MSOP	–55°C to 125°C
LTC4441ES8-1	LTC4441ES8-1#TR	44411	8-Lead Plastic SO	–40°C to 125°C
LTC4441IS8-1	LTC4441IS8-1#TR	4441I1	8-Lead Plastic SO	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 7.5V, DRV_{CC} = 5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DRVCC}	Driver Supply Programmable Range		●	5		8	V
I_{VIN}	V_{IN} Supply Current	EN/$\overline{\text{SHDN}}$ = 0V, IN = 0V EN/$\overline{\text{SHDN}}$ = 5V, IN = 0V f_{IN} = 100kHz, C_{OUT} = 4.7nF (Note 4)	● ●		5 250 3	12 500 6	µA µA mA
DRV_{CC} Regulator							
V_{FB}	Regulator Feedback Voltage	V_{IN} = 7.5V	●	1.11	1.21	1.31	V
$\Delta V_{DRVCC(LINE)}$	Regulator Line Regulation	V_{IN} = 7.5V to 25V			9	40	mV
$\Delta V_{DRVCC(LOAD)}$	Load Regulation	Load = 0mA to 40mA			–0.1		%
$V_{DROPOUT}$	Regulator Dropout Voltage	Load = 40mA			370		mV
V_{UVLO}	FB Pin UVLO Voltage	Rising Edge Falling Edge			1.09 0.97		V V
Input							
V_{IH}	IN Pin High Input Threshold	Rising Edge	●	2	2.4	2.8	V
V_{IL}	IN Pin Low Input Threshold	Falling Edge	●	1	1.4	1.8	V
V_{IH}-V_{IL}	IN Pin Input Voltage Hysteresis	Rising-Falling Edge			1		V
I_{INP}	IN Pin Input Current	V_{IN} = ±10V	●		±0.01	±10	µA
$I_{EN/\overline{SHDN}}$	EN/$\overline{\text{SHDN}}$ Pin Input Current	$V_{EN/\overline{SHDN}}$ = 9V	●		±0.01	±1	µA
$V_{\overline{SHDN}}$	EN/$\overline{\text{SHDN}}$ Pin Shutdown Threshold	Falling Edge			0.45		V
V_{EN}	EN/$\overline{\text{SHDN}}$ Pin Enable Threshold	Rising Edge Falling Edge	 ●	 1.036	1.21 1.09	 1.145	V V
$V_{EN(HYST)}$	EN/$\overline{\text{SHDN}}$ Pin Enable Hysteresis	Rising-Falling Edge			0.12		V
Output							
R_{ONL}	Driver Output Pull-Down Resistance	I_{OUT} = 100mA	●		0.35	0.8	Ω
I_{PU}	Driver Output Peak Pull-Up Current	DRV_{CC} = 8V			6		A
I_{PD}	Driver Output Peak Pull-Down Current	DRV_{CC} = 8V			6		A
$R_{ON(BLANK)}$	BLANK Pin Pull-Down Resistance	IN = 0V, I_{BLANK} = 100mA LTC4441 Only			11		Ω
V_{RBLANK}	RBLANK Pin Voltage	RBLANK = 200kΩ LTC4441 Only			1.3		V
Switching Timing							
t_{PHL}	Driver Output High-Low Propagation Delay	C_{OUT} = 4.7nF (Note 5)			30		ns
t_{PLH}	Driver Output Low-High Propagation Delay	C_{OUT} = 4.7nF (Note 5)			36		ns
t_r	Driver Output Rise Time	C_{OUT} = 4.7nF (Note 5)			13		ns
t_f	Driver Output Fall Time	C_{OUT} = 4.7nF (Note 5)			8		ns
t_{BLANK}	Driver Output High to BLANK Pin High	RBLANK = 200kΩ (Note 6)			200		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4441/LTC4441-1 are tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4441E/LTC4441E-1 are guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design characterization and correlation with statistical process controls. The LTC4441I/LTC4441I-1 grade are guaranteed over the –40°C to 125°C operating junction temperature range. The LTC4441MP is guaranteed and tested over the full –55°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

ELECTRICAL CHARACTERISTICS

Note 3: Failure to solder the Exposed Pad of the MSE package to the PC board will result in a thermal resistance much higher than 38°C/W.

Note 4: Supply current in normal operation is dominated by the current needed to charge and discharge the external power MOSFET gate. This current will vary with supply voltage, switching frequency and the external MOSFETs used.

Note 5: Rise and fall times are measured using 10% and 90% levels. Delay times are measured from 50% of input to 20%/80% levels at driver output.

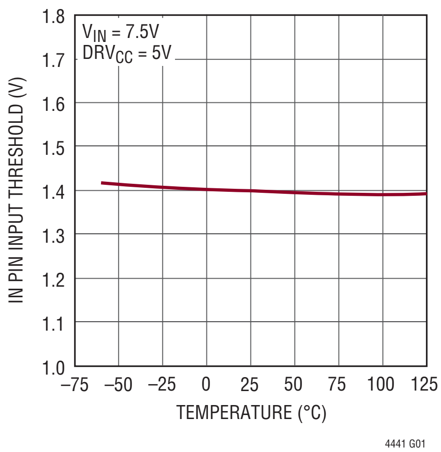
Note 6: Blanking time is measured from 50% of OUT leading edge to 10% of BLANK with a 1kΩ pull-up at BLANK pin. LTC4441 only.

Note 7: Guaranteed by design, not subject to test.

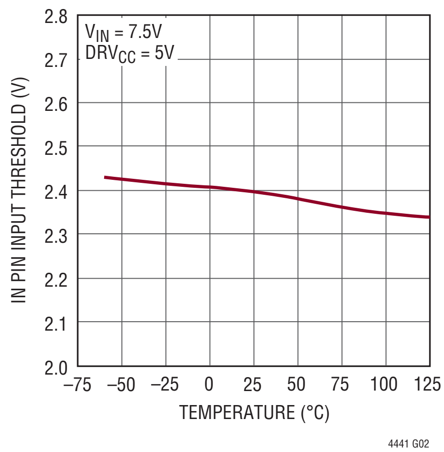
Note 8: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

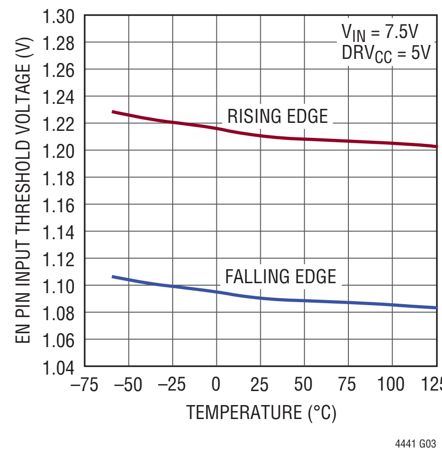
IN Pin Low Threshold Voltage vs Temperature



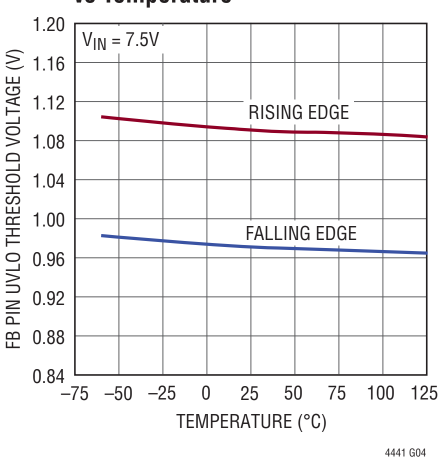
IN Pin High Threshold Voltage vs Temperature



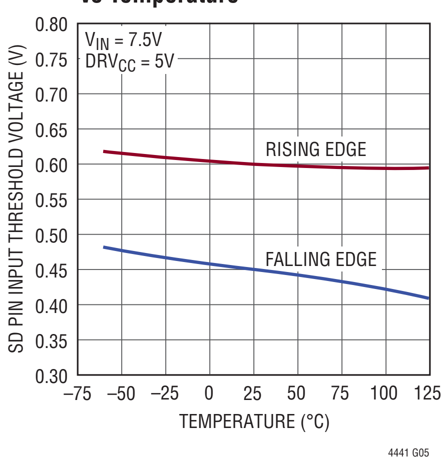
EN Pin Input Threshold Voltage vs Temperature



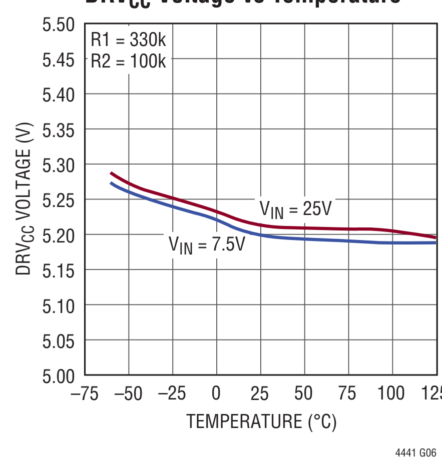
FB Pin UVLO Threshold vs Temperature



SD Pin Input Threshold Voltage vs Temperature

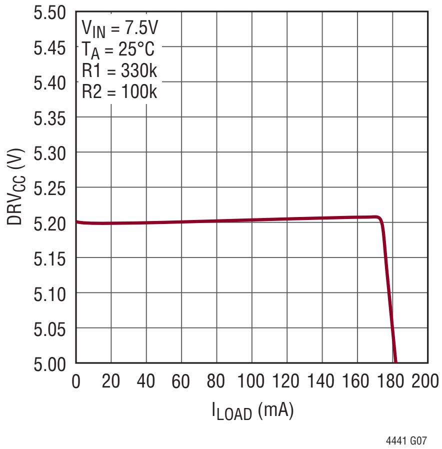


DRV_{CC} Voltage vs Temperature

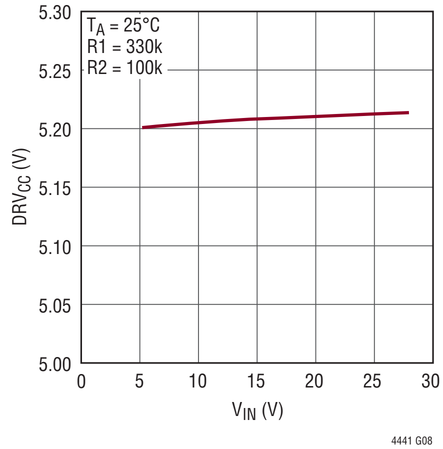


TYPICAL PERFORMANCE CHARACTERISTICS

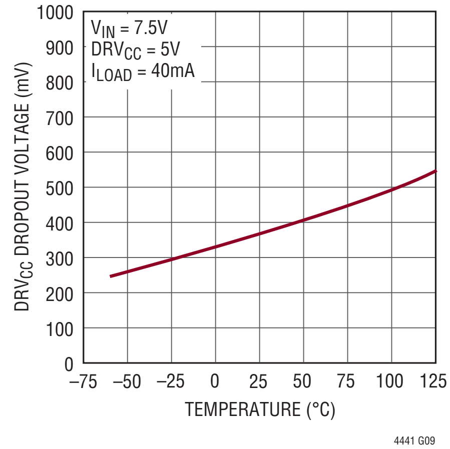
DRV_{CC} Load Regulation



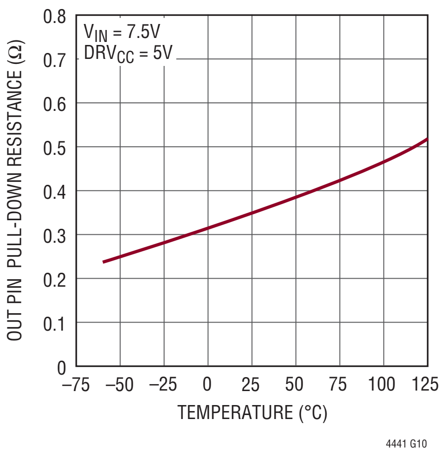
DRV_{CC} Line Regulation



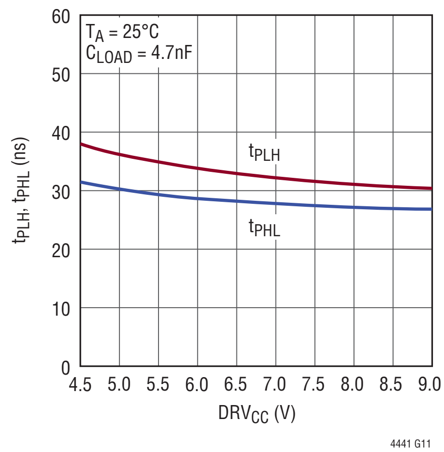
DRV_{CC} Dropout Voltage vs Temperature



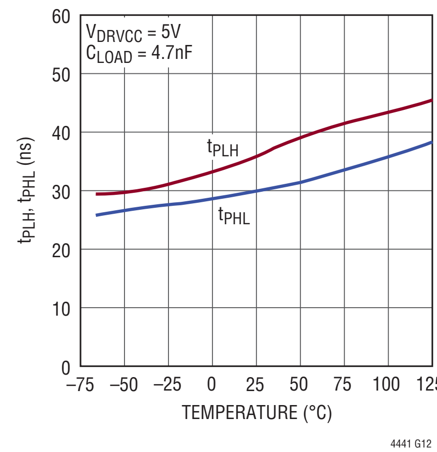
OUT Pin Pull-Down Resistance vs Temperature



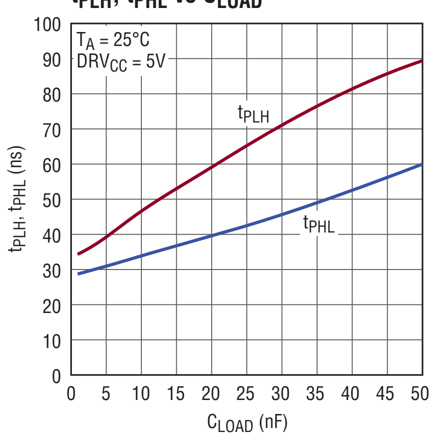
t_{PLH}, t_{PHL} vs DRV_{CC}



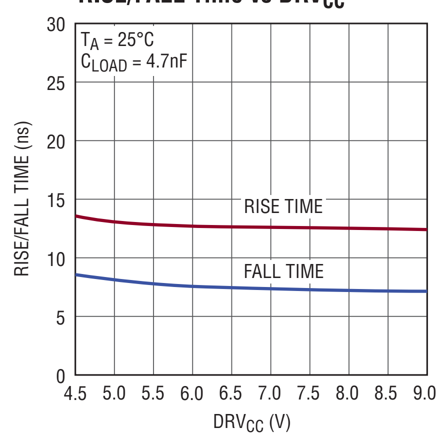
t_{PLH}, t_{PHL} vs Temperature



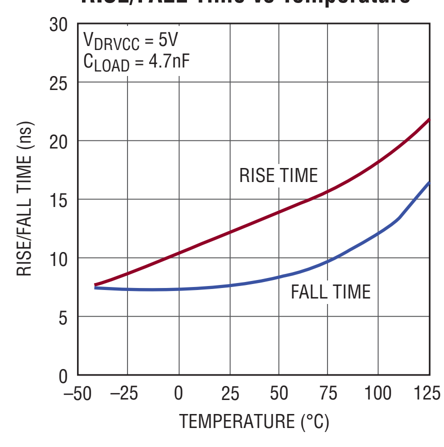
t_{PLH}, t_{PHL} vs C_{LOAD}



RISE/FALL Time vs DRV_{CC}

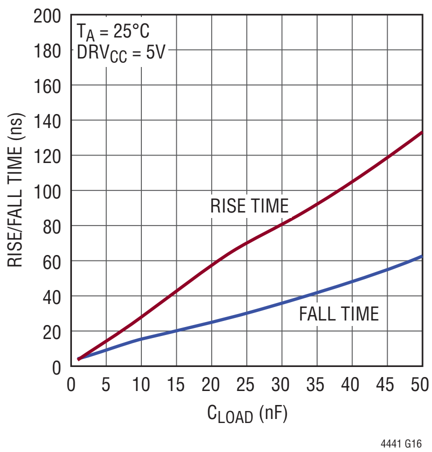


RISE/FALL Time vs Temperature

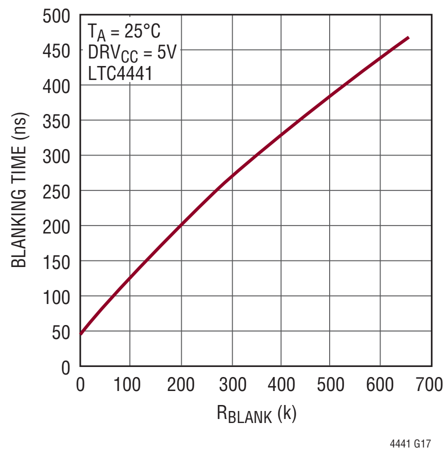


TYPICAL PERFORMANCE CHARACTERISTICS

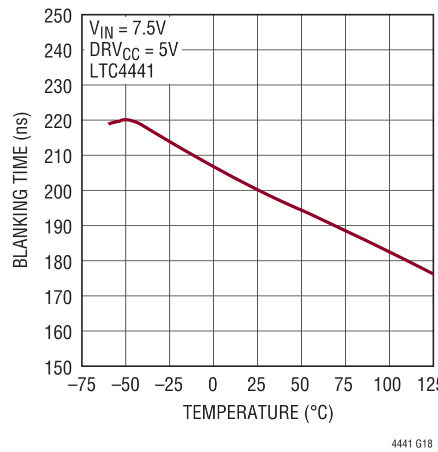
RISE/FALL Time vs C_{LOAD}



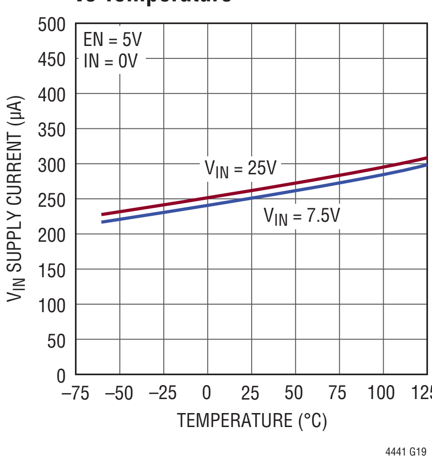
Blanking Time vs R_{BLANK}



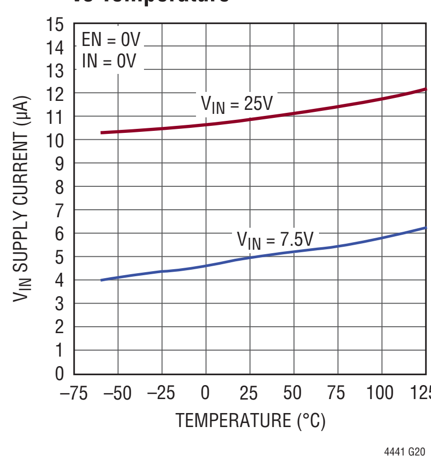
Blanking Time vs Temperature



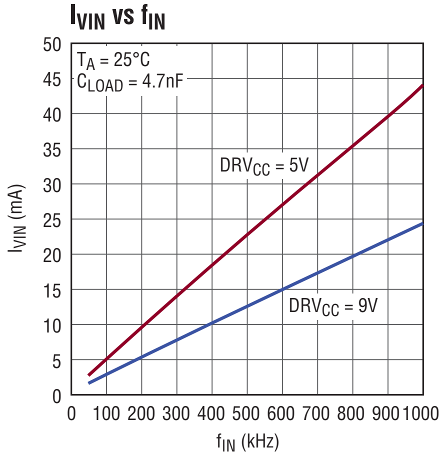
V_{IN} Operating Supply Current vs Temperature



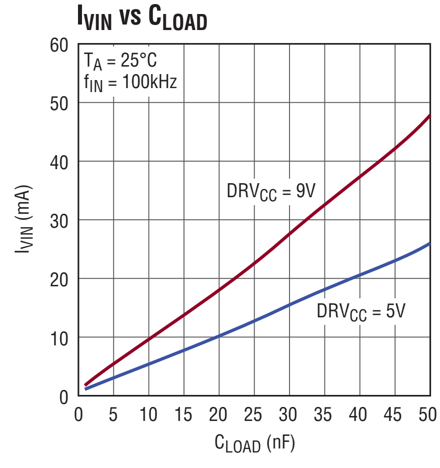
V_{IN} Standby Supply Current vs Temperature



I_{VIN} vs f_{IN}



I_{VIN} vs C_{LOAD}



PIN FUNCTIONS (MSOP/SO-8)

PGND (Pin 1/Pin 1): Driver Ground. Connect the DRV_{CC} bypass capacitor directly to this pin, as close as possible to the IC. In addition, connect the PGND and SGND pins together close to the IC, and then connect this node to the source of the power MOSFET (or current sense resistor) with as short and wide a PCB trace as possible.

BLANK (Pin 2/NA): Current Sense Blanking Output. Use this pin to assert a blanking time in the power MOSFET's source current sense signal. The LTC4441 pulls this open-drain output to SGND if the driver output is low. The output becomes high impedance after a programmable blanking time from the driver leading edge output. This blanking time can be adjusted with the RBLANK pin.*

RBLANK (Pin 3/NA): Blanking Time Adjust Input. Connect a resistor from this pin to SGND to set the blanking time. A small resistor value gives a shorter delay. Leave this pin floating if the BLANK pin is not used.*

SGND (Pin 4/Pin 2): Signal Ground. Ground return for the DRV_{CC} regulator and low power circuitry.

IN (Pin 5/Pin 3): Driver Logic Input. This is the noninverting driver input under normal operating conditions.

*Available only on the 10-lead version of the LTC4441.

EN/$\overline{\text{SHDN}}$ (Pin 6/Pin 4): Enable/$\overline{\text{Shutdown}}$ Input. Pulling this pin above 1.21V allows the driver to switch. Pulling this pin below 1.09V forces the driver output to go low. Pulling this pin below 0.45V forces the LTC4441/LTC4441-1 into shutdown mode; the DRV_{CC} regulator turns off and the supply current drops below 12µA.

FB (Pin 7/Pin 5): DRV_{CC} Regulator Feedback Input. Connect this pin to the center tap of an external resistive divider between DRV_{CC} and SGND to program the DRV_{CC} regulator output voltage. To ensure loop stability, use the value of 330kΩ for the top resistor, R1.

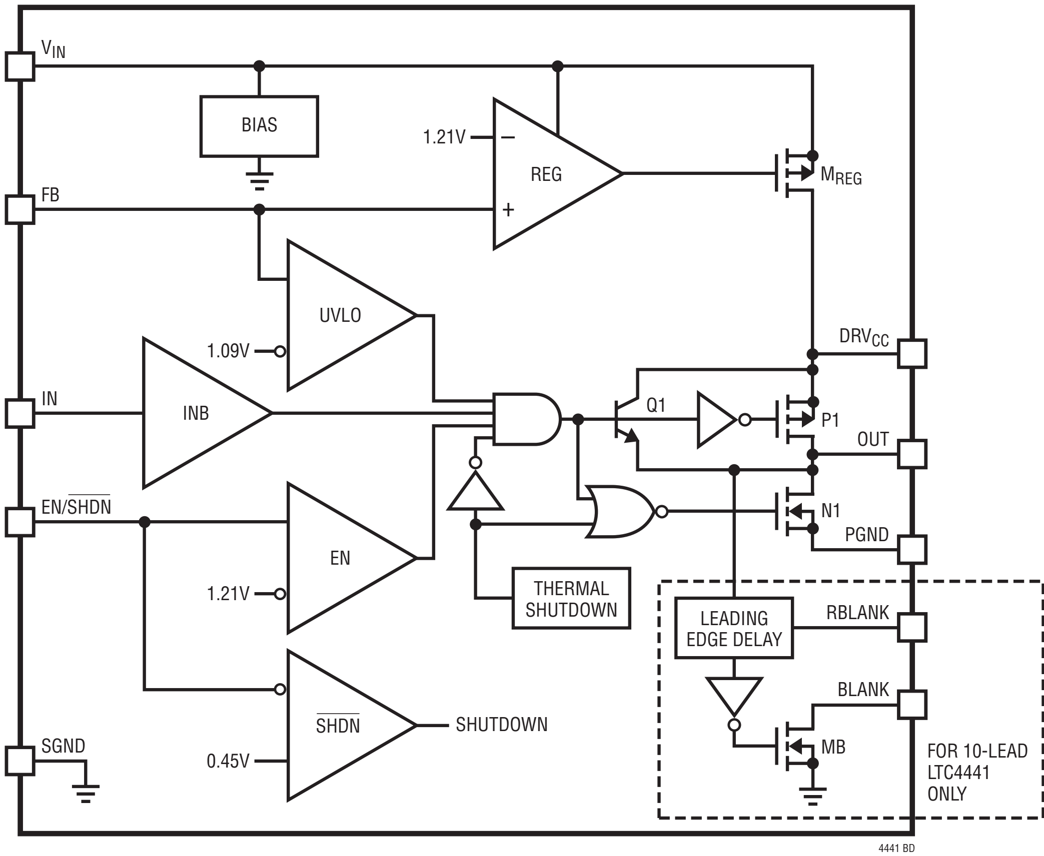
V_{IN} (Pin 8/Pin 6): Main Supply Input. This pin powers the DRV_{CC} linear regulator. Bypass this pin to SGND with a 1µF ceramic, tantalum or other low ESR capacitor in close proximity to the LTC4441/LTC4441-1.

DRV_{CC} (Pin 9/Pin 7): Linear Regulator Output. This output pin powers the driver and the control circuitry. Bypass this pin to PGND using a 10µF ceramic, low ESR (X5R or X7R) capacitor in close proximity to the LTC4441/LTC4441-1.

OUT (Pin 10/Pin 8): Driver Output.

GND (Exposed Pad Pin 11/NA): Ground. The exposed pad must be soldered to the PCB ground.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Overview

Power MOSFETs generally account for the majority of power lost in a converter. It is important to choose not only the type of MOSFET used, but also its gate drive circuitry. The LTC4441/LTC4441-1 is designed to drive an N-channel power MOSFET with little efficiency loss. The LTC4441/LTC4441-1 can deliver up to 6A of peak current using a combined NPN Bipolar and MOSFET output stage. This helps to turn the power MOSFET fully "on" or "off" with a very brief transition region.

The LTC4441/LTC4441-1 includes a programmable linear-regulator to regulate the gate drive voltage. This regulator provides the flexibility to use either standard threshold or logic level MOSFETs.

DRV_{CC} Regulator

An internal, P-channel low dropout linear regulator provides the DRV_{CC} supply to power the driver and the pre-driver logic circuitry as shown in Figure 1. The regulator output voltage can be programmed between 5V and 8V with an external resistive divider between DRV_{CC} and SGND and a center tap connected to the FB pin. The regulator needs an R1 value of around 330k to ensure loop stability; the value of R2 can be varied to achieve the required DRV_{CC} voltage:

$$R2 = \frac{406k}{DRV_{CC} - 1.21V}$$

The DRV_{CC} regulator can supply up to 100mA and is short-circuit protected. The output must be bypassed to the PGND pin in very close proximity to the IC pins with a minimum of 10µF ceramic, low ESR (X5R or X7R) capacitor. Good bypassing is necessary as high transient supply currents are required by the driver. If the input supply voltage, V_{IN}, is close to the required gate drive voltage, this regulator can be disabled by connecting the DRV_{CC} and FB pins to V_{IN}.

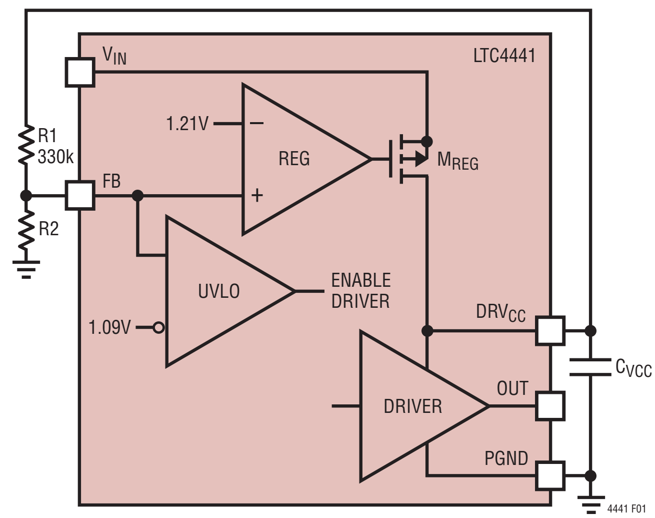


Figure 1. DRV_{CC} Regulator

The LTC4441/LTC4441-1 monitors the FB pin for DRV_{CC}'s UVLO condition (UVLO in Figure 1). During power-up, the driver output is held low until the DRV_{CC} voltage reaches 90% of the programmed value. Thereafter, if the DRV_{CC} voltage drops more than 20% below the programmed value, the driver output is forced low.

Logic Input Stage

The LTC4441/LTC4441-1 driver employs TTL/CMOS compatible input thresholds that allow a low voltage digital signal to drive standard power MOSFETs. The LTC4441/LTC4441-1 contains an internal voltage regulator that biases the input buffer, allowing the input thresholds (V_{IH} = 2.4V, V_{IL} = 1.4V) to be independent of the programmed-driver supply, DRV_{CC}, or the input supply, V_{IN}. The 1V hysteresis between V_{IH} and V_{IL} eliminates false triggering due to noise during switching transitions. However, care should be taken to isolate this pin from any noise pickup, especially in high frequency, high voltage applications.The LTC4441/LTC4441-1 input buffer has high input impedance and draws negligible input current, simplifying the drive circuitry required for the input. This input can withstand voltages up to 15V above and below ground. This makes the chip more tolerant to ringing on the input digital signal caused by parasitic inductance.

APPLICATIONS INFORMATION

Driver Output Stage

A simplified version of the LTC4441/LTC4441-1's driver-output stage is shown in Figure 2.

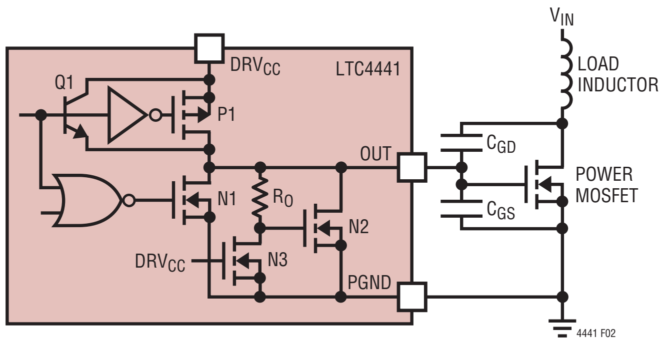


Figure 2. Driver Output Stage

The pull-up device is the combination of an NPN transistor, Q1, and a P-channel MOSFET, P1. This provides both the ability to swing to rail (DRV_{CC}) and deliver large peak charging currents.

The pull-down device is an N-channel MOSFET, N1, with a typical on resistance of 0.35Ω. The low impedance of N1 provides fast turn-off of the external power MOSFET and holds the power MOSFET's gate low when its drain voltage switches. When the power MOSFET's gate is pulled low (gate shorted to source through N1) by the LTC4441/LTC4441-1, its drain voltage is pulled high by its load (e.g., inductor or resistor). The slew rate of the drain voltage causes current to flow to the MOSFET's gate through its gate-to-drain capacitance. If the MOSFET driver does not have sufficient sink current capability (low output impedance), the current through the power MOSFET's C_{GD} can momentarily pull the gate high and turn the MOSFET back on.

A similar situation occurs during power-up when V_{IN} is ramping up with the DRV_{CC} regulator output still low. N1 is off and the driver output, OUT, may momentarily pull high through the power MOSFET's C_{GD}, turning on the power MOSFET. The N-channel MOSFETs N2 and N3,shown in Figure 2, prevent the driver output from going high in this situation. If DRV_{CC} is low, N3 is off. If OUT is pulled high through the power MOSFET's C_{GD}, the gate of N2 gets pulled high through RO. This turns N2 on, which then pulls OUT low. Once DRV_{CC} is >1V, N3 turns on to hold the N2 gate low, thus disabling N2.

The pre-driver that drives Q1, P1 and N1 uses an adaptive method to minimize cross-conduction currents. This is done with a 5ns nonoverlapping transition time. N1 is fully turned off before Q1 is turned on and vice-versa using this 5ns buffer time. This minimizes any cross-conduction currents while Q1 and N1 are switching on and off without affecting their rise and fall times.

Thermal Shutdown

The LTC4441/LTC4441-1 has a thermal detector that disables the DRV_{CC} regulator and pulls the driver output low when activated. If the junction temperature exceeds150°C, the driver pull-up devices, Q1 and P1, turn off while the pull-down device, N1, turns on briskly for 200ns to quickly pull the output low. The thermal shutdown circuit has 20°C of hysteresis.

Enable/$\overline{\text{Shutdown}}$ Input

The EN/$\overline{\text{SHDN}}$ pin serves two functions. Pulling this pin below 0.45V forces the LTC4441/LTC4441-1 into shutdown mode. In shutdown mode, the internal circuitry and the DRV_{CC} regulator are off and the supply current drops to <12μA. If the input voltage is between 0.45V and 1.21V, the DRV_{CC} regulator and internal circuit power up but the driver output stays low. If the input goes above 1.21V, the driver starts switching according to the input logic signal. The driver enable comparator has a small hysteresis of 120mV.

Blanking

In some switcher applications, a current sense resistor is placed between the low side power MOSFET's source terminal and ground to sense the current in the MOSFET. With this configuration, the switching controller must incorporate some timing interval to blank the ringing onthe current sense signal immediately after the MOSFET is turned on. This ringing is caused by the parasitic inductance and capacitance of the PCB trace and the MOSFET. The duration of the ringing is thus dependent on the PCB layout and the components used and can be longer than the blanking interval provided by the controller.

APPLICATIONS INFORMATION

The 10-Lead LTC4441 includes an open-drain output that can be used to extend this blanking interval. The 8-Lead LTC4441-1 does not have this blanking function. Figure 3 shows the BLANK pin connection. The BLANK pin is connected directly to the switching controller's SENSE+ input. Figure 4 shows the blanking waveforms. If the driver input is low, the external power MOSFET is off and MB turns on to hold SENSE+ low. If the driver input goes high, the power MOSFET turns on after the driver's propagation delay. MB remains on, attenuating the ringing seen by the controller's SENSE+ input. After the programmed blanking time, MB turns off to enable the current sense signal. MB is designed to turn on and turn off at a controlled slew rate. This is to prevent the gate switching noise from coupling into the current sense signal.

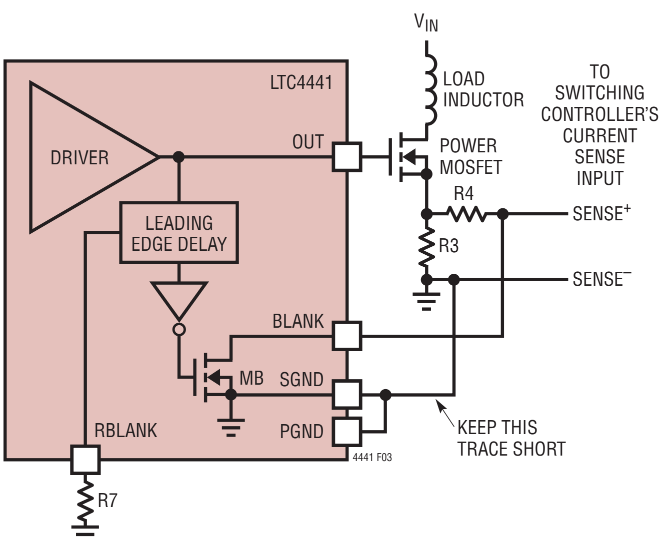


Figure 3. Blanking Circuit

The blanking interval can be adjusted using resistor R7 connected to the RBLANK pin. A small resistance value gives a shorter interval with a default minimum of 75ns.

The value of the resistor R4 and the on-resistance of MB (typically 11Ω) form a resistive divider attenuating the ringing. R4 needs to be large for effective blanking, but not so large as to cause delay to the sense signal. A resistance value of 1k to 10k is recommended.

For optimum performance, the LTC4441/LTC4441-1should be placed as close as possible to the powerMOSFET and current sense resistor, R3.

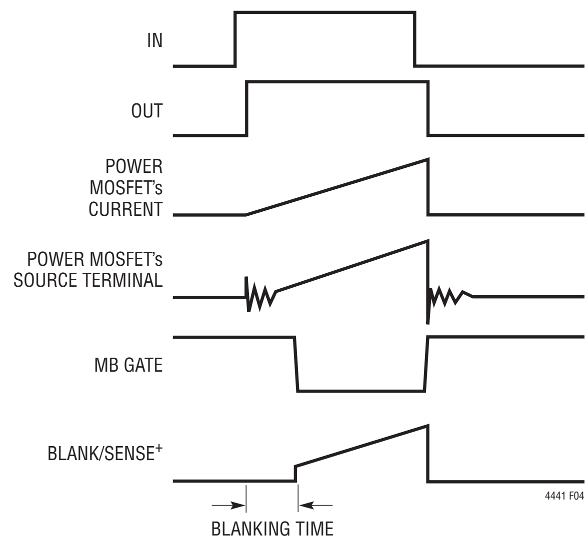


Figure 4. Blanking Waveforms

Power Dissipation

To ensure proper operation and long-term reliability, the LTC4441/LTC4441-1 must not operate beyond its maximum temperature rating. The junction temperature can be calculated by:

$$I_{Q(TOT)} = I_Q + f \bullet Q_G$$

$$P_D = V_{IN} \bullet (I_Q + f \bullet Q_G)$$

$$T_J = T_A + P_D \bullet \theta_{JA}$$

where:

I_Q = LTC4441/LTC4441-1 static quiescent current, typically 250µA

f = Logic input switching frequency

Q_G = Power MOSFET total gate charge at corresponding V_{GS} voltage equal to DRV_{CC}

V_{IN} = LTC4441/LTC4441-1 input supply voltage

T_J = Junction temperature

T_A = Ambient temperature

θ_{JA} = Junction-to-ambient thermal resistance. The 10-pin MSOP package has a thermal resistance of θ_{JA} = 38°C/W.

APPLICATIONS INFORMATION

The total supply current, $I_{Q(TOT)}$, consists of the LTC4441/LTC4441-1's static quiescent current, I_Q, and the current required to drive the gate of the power MOSFET, with thelatter usually much higher than the former. The dissipated power, P_D, includes the efficiency loss of the DRV_{CC} regulator. With a programmed DRV_{CC}, a high V_{IN} results in higher efficiency loss.

As an example, consider an application with V_{IN} = 12V. The switching frequency is 300kHz and the maximum ambient temperature is 70°C. The power MOSFET chosen is three pieces of IRFB31N20D, which has a maximum $R_{DS(ON)}$ of 82mΩ (at room temperature) and a typical total gatecharge of 70nC (the temperature coefficient of the gate charge is low).

$$I_{Q(TOT)} = 500\mu A + 210nC \cdot 300kHz = 63.5mA$$

$$P_{IC} = 12V \cdot 63.5mA = 0.762W$$

$$T_J = 70°C + 38°C/W \cdot 0.762W = 99°C$$

This demonstrates how significant the gate charge current can be when compared to the LTC4441/LTC4441-1's static quiescent current. To prevent the maximum junction temperature from being exceeded, the input supply current must be checked when switching at high V_{IN}. A tradeoff between the operating frequency and the size of the power MOSFET may be necessary to maintain areliable LTC4441/LTC4441-1 junction temperature. Prior to lowering the operating frequency, however, be sure to check with power MOSFET manufacturers for their innovations on low Q_G, low $R_{DS(ON)}$ devices. Power MOSFET manufacturing technologies are continually improving, with newer and better performing devices being introduced.

PC Board Layout Checklist

When laying out the printed circuit board, the following-checklist should be used to ensure proper operation of the LTC4441/LTC4441-1:

A. Mount the bypass capacitors as close as possible between the DRV_{CC} and PGND pins and between the V_{IN} and SGND pins. The PCB trace loop areas should be tightened as much as possible to reduce inductance.

B. Use a low inductance, low impedance ground plane to reduce any ground drop. Remember that the LTC4441/LTC4441-1 switches 6A peak current and any significant ground drop will degrade signal integrity.

C. Keep the PCB ground trace between the LTC4441/LTC4441-1 ground pins (PGND and SGND) and the external current sense resistor as short and wide as possible.

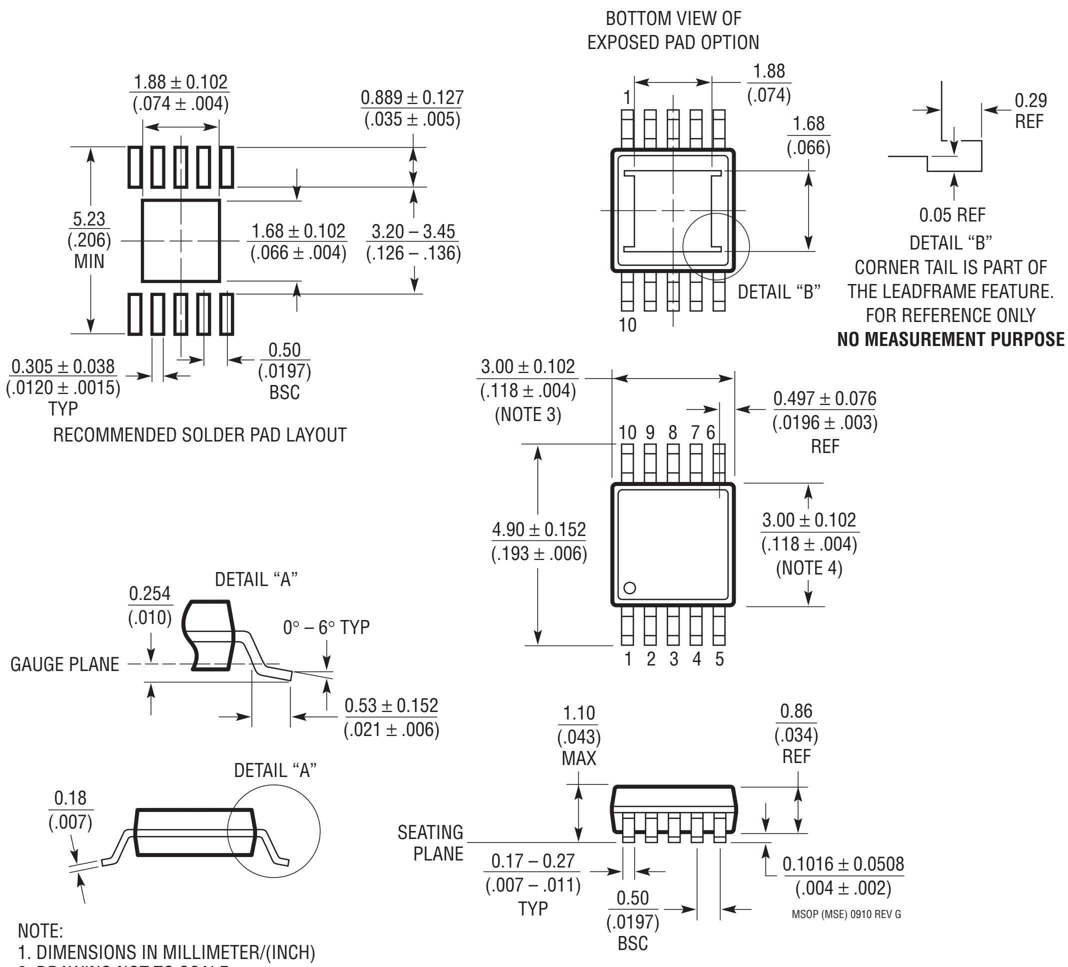
D. Plan the ground routing carefully. Know where the large load switching current paths are. Maintain separate ground return paths for the input pin and output pin to avoid sharing small-signal ground with large load ground return. Terminate these two ground traces only at the GND pin of the driver (STAR network).

E. Keep the copper trace between the driver output pin andthe load short and wide.

F. Place the small-signal components away from the high frequency switching nodes. These components include the resistive networks connected to the FB, RBLANK and EN/$\overline{SHDN}$ pins.

PACKAGE DESCRIPTION

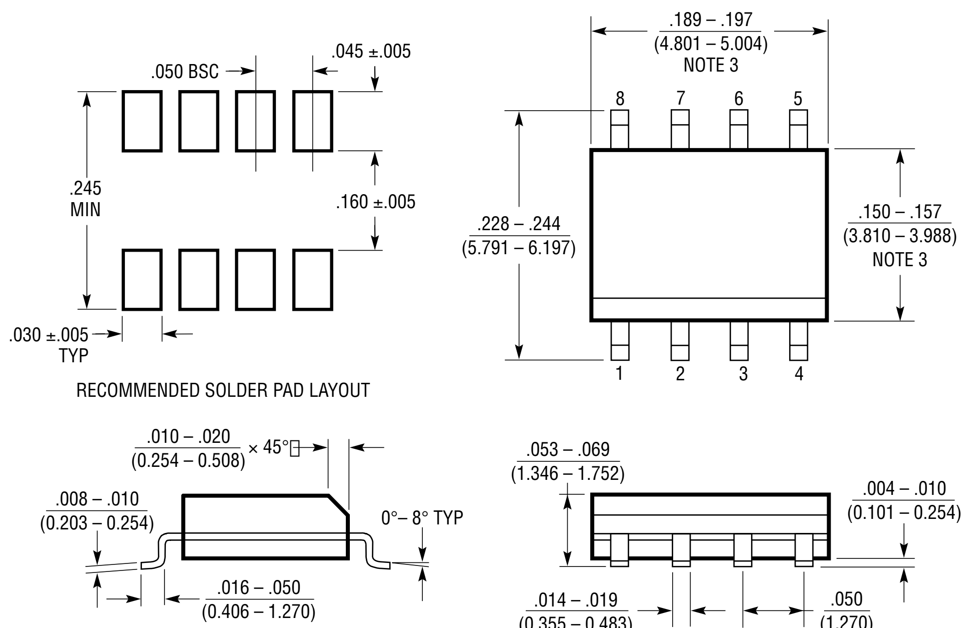
MSE Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1664 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/11	Added MP-grade part. Changes reflected throughout the data sheet.	1-16

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4440/ LTC4440-5	High Voltage, High Speed, High Side N-Channel Gate Driver	Up to 80V Supply Voltage, 8V ≤ V_{CC} ≤ 15V, 2.4A Peak Pull-Up/1.5Ω Peak Pull-Down
LTC4442	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, 6V ≤ V_{CC} ≤ 9.5V
LTC4449	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, 4.5V ≤ V_{CC} ≤ 6.5V
LTC4444/ LTC4444-5	High Voltage Synchronous N-Channel MOSFET Driver with Shoot Thru Protection	Up to 100V Supply Voltage, 4.5V/7.2V ≤ V_{CC} ≤ 13.5V, 3A Peak Pull-Up/0.55Ω Peak Pull-Down
LTC4446	High Voltage Synchronous N-Channel MOSFET Driver without Shoot Thru Protection	Up to 100V Supply Voltage, 7.2V ≤ V_{CC} ≤ 13.5V, 3A Peak Pull-Up/0.55Ω Peak Pull-Down
LTC1154	High Side Micropower MOSFET Driver	Up to 18V Supply Voltage, 85µA Quiescent Current, Internal Charge Pump

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