THE DATASHEET OF

LTC4260CUH#PBF

www.win-source.net 0086-755-83957316

Positive High Voltage Hot Swap Controller with I²C Compatible Monitoring

FEATURES

- **Allows Safe Board Insertion into Live Backplane**
- **8-Bit ADC Monitors Current and Voltage**
- **I²C™/SMBus Interface**
- **Wide Operating Voltage Range: 8.5V to 80V**
- High Side Drive for External N-Channel MOSFET
- Input Overvoltage/Undervoltage Protection
- Optional Latchoff or Autoretry After Faults
- Alerts Host After Faults
- Foldback Current Limiting
- Available in 24-Lead SO, 24-Lead Narrow SSOP and 32-Lead (5mm × 5mm) QFN Packages

APPLICATIONS

- Electronic Circuit Breakers
- Live Board Insertion
- Computers, Servers

DESCRIPTION

The LTC®4260 Hot Swap™ controller allows a board to be safely inserted and removed from a live backplane. Using an external N-channel pass transistor, the board supply voltage can be ramped up at an adjustable rate. An I²C interface and onboard ADC allow monitoring of board current, voltage and fault status.

The device features adjustable analog foldback current limit with latch off or automatic restart after the LTC4260 remains in current limit beyond an adjustable time-out delay.

The controller has additional features to interrupt the host when a fault has occurred, notify when output power is good, detect insertion of a load card and power-up in either the on or off state.

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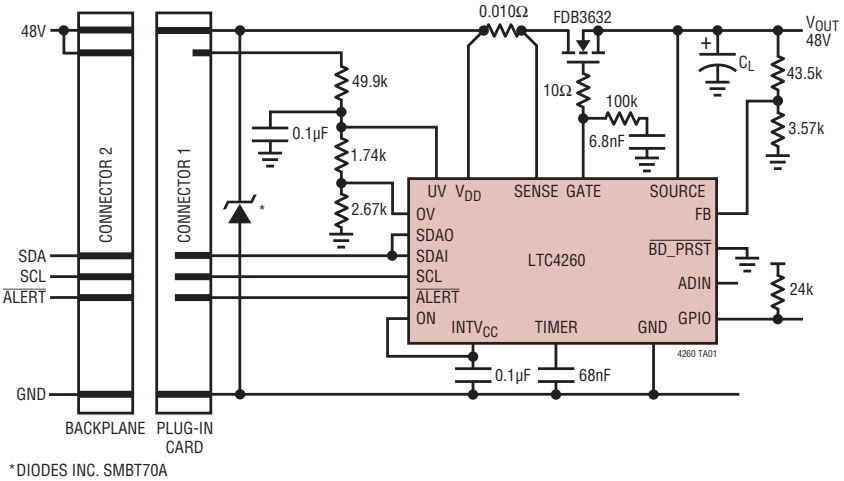
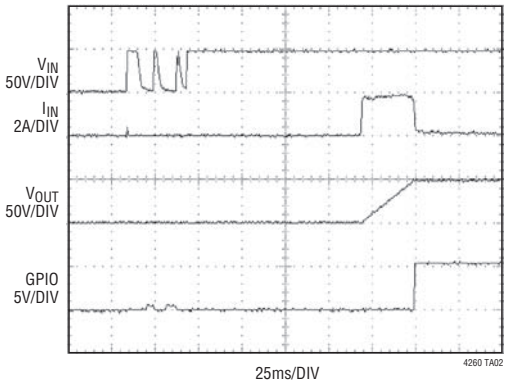
TYPICAL APPLICATION

3A, 48V Card Resident Application



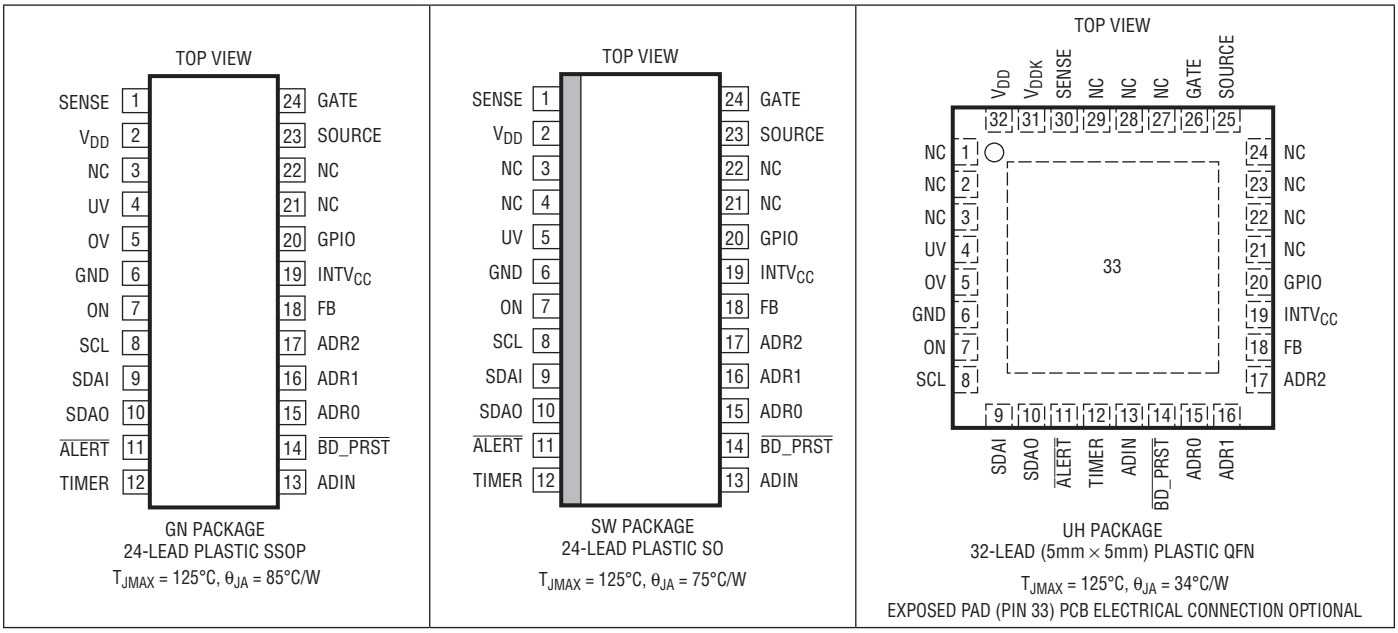
Power Up Waveforms



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltages (V_{DD}) ..... –0.3V to 100V
Input Voltages
SENSE ..... V_{DD} – 10V or –0.3V to V_{DD}
SOURCE..... GATE – 5V to GATE + 0.3V
$\overline{BD_PRST}$, FB, ON, OV, UV ..... –0.3V to 12V
ADR0-ADR2, TIMER, ADIN.....–0.3V to $INTV_{CC}$ + 0.3V
SCL, SDAI ..... –0.3V to 6.5V
Output Voltages
GPIO ..... –0.3V to 100V
GATE (Note 3) ..... –0.3V to 100V
$\overline{ALERT}$, SDAO..... –0.3V to 6.5V
Supply Voltage ($INTV_{CC}$) ..... –0.3V to 6.2V
Operating Temperature Range
LTC4260C ..... 0°C to 70°C
LTC4260I..... –40°C to 85°C
Storage Temperature Range
GN, SW Packages ..... –65°C to 150°C
UH Package ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
GN, SW Packages Only..... 300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4260CGN#PBF	LTC4260CGN#TRPBF	LTC4260CGN	24-Lead Plastic SSOP	0°C to 70°C
LTC4260IGN#PBF	LTC4260IGN#TRPBF	LTC4260IGN	24-Lead Plastic SSOP	–40°C to 85°C
LTC4260CSW#PBF	LTC4260CSW#TRPBF	LTC4260CSW	24-Lead Plastic SO	0°C to 70°C
LTC4260ISW#PBF	LTC4260ISW#TRPBF	LTC4260ISW	24-Lead Plastic SO	–40°C to 85°C
LTC4260CUH#PBF	LTC4260CUH#TRPBF	4260	32-Lead (5mm × 5mm) Plastic QFN	0°C to 70°C
LTC4260IUH#PBF	LTC4260IUH#TRPBF	4260	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 48V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
General							
V_{DD}	Input Supply Range		●	8.5		80	V
I_{DD}	Input Supply Current		●		2	5	mA
$V_{DD(UVL)}$	V_{DD} Supply Undervoltage Lockout	V_{DD} Falling	●	7	7.45	7.9	V
$INTV_{CC(UVL)}$	V_{CC} Supply Undervoltage Lockout	$INTV_{CC}$ Falling	●	3.4	3.8	4.2	V
$INTV_{CC}$	Internal Regulator Voltage		●	5	5.5	6	V
Gate Drive							
t_D	Turn-On Delay		●	50	100	150	ms
ΔV_{GATE}	External N-Channel Gate Drive ($V_{GATE} - V_{SOURCE}$)	V_{DD} = 20V to 80V V_{DD} = 8.5V to 20V	● ●	10 4.5	14 6	18 18	V V
$I_{GATE(UP)}$	External N-Channel Pull-Up Current	Gate Drive On, V_{GATE} = 0V	●	–14	–18	–22	µA
$I_{GATE(FST)}$	External N-Channel Fast Pull-Down	Fast Turn Off, V_{GATE} = 48V, V_{SOURCE} = 43V	●	300	600	1000	mA
$I_{GATE(DN)}$	External N-Channel Pull-Down Current	Gate Drive Off, V_{GATE} = 58V, V_{SOURCE} = 48V	●	0.7	1	1.4	mA
I_{SOURCE}	SOURCE Pin Input Current	SOURCE = 48V	●	200	400	600	µA
Input Pins							
$V_{ON(TH)}$	ON Pin Threshold Voltage	V_{ON} Rising	●	1.19	1.235	1.27	V
$\Delta V_{ON(HYST)}$	ON Pin Hysteresis		●	60	130	200	mV
$I_{ON(IN)}$	ON Pin Input Current	V_{ON} = 1.2V	●		0	±1	µA
$V_{OV(TH)}$	OV Pin Threshold Voltage	V_{OV} Rising	●	3.43	3.5	3.56	V
$\Delta V_{OV(HYST)}$	OV Pin Hysteresis		●	70	90	120	mV
$I_{OV(IN)}$	OV Pin Input Current	V_{OV} = 3.5V	●		0	±1	µA
$V_{UV(TH)}$	UV Pin Threshold Voltage	V_{UV} Rising	●	3.43	3.5	3.56	V
$\Delta V_{UV(HYST)}$	UV Pin Hysteresis		●	310	380	440	mV
$I_{UV(IN)}$	UV Pin Input Current	V_{UV} = 3.5V	●		0	±2	µA
$V_{UV(RTH)}$	UV Pin Reset Threshold Voltage	V_{UV} Falling	●	1.18	1.235	1.27	V
$\Delta V_{UV(RHYST)}$	UV Pin Reset Threshold Hysteresis		●	80	160	250	mV
$\Delta V_{SENSE(TH)}$	Current Limit Sense Voltage Threshold ($V_{DD} - V_{SENSE}$)	V_{FB} = 3.5V V_{FB} = 0V	● ●	45 10	50 20	55 30	mV mV
$I_{SENSE(IN)}$	SENSE Pin Input Current	V_{SENSE} = 48V	●	70	100	130	µA
V_{FB}	Foldback Pin Power Good Threshold	FB Rising	●	3.43	3.5	3.56	V
$\Delta V_{FB(HYST)}$	FB Pin Power Good Hysteresis		●	80	100	120	mV
I_{FB}	Foldback Pin Input Current	FB = 3.5V	●		0	±2	µA
$V_{\overline{BD_PRST}(TH)}$	$\overline{BD_PRST}$ Input Threshold	$V_{\overline{BD_PRST}}$ Rising	●	1.2	1.235	1.27	V
$\Delta V_{\overline{BD_PRST}(HYST)}$	$\overline{BD_PRST}$ Hysteresis		●	70	130	190	mV
$I_{\overline{BD_PRST}}$	$\overline{BD_PRST}$ Pullup Current	$\overline{BD_PRST}$ = 0V	●	–7	–10	–16	µA
$V_{GPIO(TH)}$	GPIO Pin Input Threshold	V_{GPIO} Rising	●	1.6	1.8	2	V
$\Delta V_{GPIO(HYST)}$	GPIO Pin Hysteresis				80		mV
$V_{GPIO(OL)}$	GPIO Pin Output Low Voltage	I_{GPIO} = 2mA	●		0.25	0.5	V
$I_{GPIO(IN)}$	GPIO Pin Input Leakage Current	V_{GPIO} = 80V	●		0	±10	µA
R_{ADIN}	ADIN Pin Input Resistance	V_{ADIN} = 1.28V	●	2	10		MΩ
I_{ADIN}	ADIN Pin Input Current	V_{ADIN} = 2.56V	●		0	±1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 48V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Timer							
$V_{TIMER(H)}$	TIMER Pin High Threshold	V_{TIMER} Rising	●	1.2	1.235	1.28	V
$V_{TIMER(L)}$	TIMER Pin Low Threshold	V_{TIMER} Falling	●	0.1	0.2	0.3	V
$I_{TIMER(UP)}$	TIMER Pin Pull-Up Current	V_{TIMER} = 0V	●	–80	–100	–120	µA
$I_{TIMER(DN)}$	TIMER Pin Pull-Down Current	V_{TIMER} = 1.3V	●	1.4	2	2.6	µA
$I_{TIMER(RATIO)}$	TIMER Pin Current Ratio $I_{TIMER(DN)}/I_{TIMER(UP)}$		●	1.6	2	2.7	%
AC Parameters							
$t_{PLH(GATE)}$	Input High (ON) to GATE High Propagation Delay	C_{GATE} = 1pF	●		1	3	µs
$t_{PHL(GATE)}$	Input High (OV, BD_PRST), Input Low (ON, UV) to GATE Low Propagation Delay	C_{GATE} = 1pF	●		0.5	3	µs
$t_{PHL(SENSE)}$	(V_{DD} – SENSE) High to GATE Low	V_{DD} – SENSE = 200mV, C_{GATE} = 10nF	●		0.4	1	µs
ADC							
	Resolution (No Missing Codes)	(Note 4)	●	8			Bits
	Integral Nonlinearity	V_{DD} – SENSE (Note 5) SOURCE ADIN	● ● ●		±0.5 ±0.5 ±0.5	±2 ±1.25 ±1.25	LSB LSB LSB
	Offset Error	V_{DD} – SENSE SOURCE ADIN	● ● ●			±1.5 ±1 ±1	LSB LSB LSB
	Full Scale Error	(Note 6)	●			±5	LSB
	Total Unadjusted Error	(Note 6)	●			±5	LSB
	Full Scale Voltage (Code 255)	V_{DD} – SENSE (Note 6) SOURCE ADIN	● ● ●	75 100 2.50	76.5 102 2.55	78 104 2.60	mV V V
	Conversion Rate				10		Hz
I^2C Interface							
$V_{ADR(H)}$	ADR0 to ADR2 Input High Voltage Threshold			$INTV_{CC}$ –0.6	$INTV_{CC}$ –0.45	$INTV_{CC}$ –0.25	V
$V_{ADR(L)}$	ADR0 to ADR2 Input Low Voltage Threshold			0.25	0.45	0.65	V
$I_{ADR(IN)}$	ADR0 to ADR2 Input Current	ADR0 to ADR2 = 0V, 5.5V	●	–80		80	µA
$V_{SDAI,SCL(TH)}$	SDAI, SCL Input Threshold		●	1.6	1.8	2	V
$I_{SDAI,SCL(IN)}$	SDAI, SCL Input Current	SCL, SDAI = 5V	●		0	±1	µA
$V_{SDAO(OL)}$	SDAO Output Low Voltage	I_{SDAO} = 5mA	●		0.2	0.4	V
$V_{\overline{ALERT}(OL)}$	$\overline{ALERT}$ Output Low Voltage	$I_{\overline{ALERT}}$ = 5mA	●		0.2	0.4	V
$I_{SDAO,ALERT(IN)}$	SDAO, $\overline{ALERT}$ Input Current	SDAO, $\overline{ALERT}$ = 5V	●		0	±1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 48V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I²C Interface Timing (Note 4)							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency	Operates with $f_{SCL} \le f_{SCL(MAX)}$		400			kHz
$t_{BUF(MIN)}$	Minimum Bus Free Time Between Stop/Start Condition				0.12	1.3	µs
$t_{SU,STA(MIN)}$	Minimum Repeated Start Condition Set-Up Time				30	600	ns
$t_{HD,STA(MIN)}$	Minimum Hold Time After (Repeated) Start Condition				140	600	ns
$t_{SU,STO(MIN)}$	Minimum Stop Condition Set-Up Time				30	600	ns
$t_{SU,DAT(MIN)}$	Minimum Data Set-Up Time Input				30	100	ns
$t_{HD,DATI(MIN)}$	Minimum Data Hold Time Input				–100	0	ns
$t_{HD,DATO(MIN)}$	Minimum Data Hold Time Output			300	500	900	ns
$t_{SP(MAX)}$	Maximum Suppressed Spike Pulse Width			50	110	250	ns
C_X	SCL, SDA Input Capacitance	SDAI Tied to SDAO			5	10	pF

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: Limits on maximum rating is defined as whichever limit occurs first. An internal clamp limits the GATE pin to a minimum of 10V above source. Driving this pin to voltages beyond the clamp may damage the device.

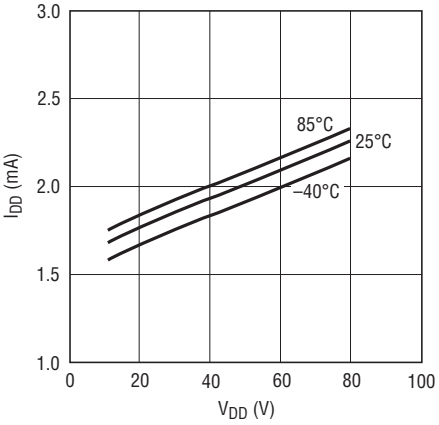
Note 4: Guaranteed by design and not subject to test.

Note 5: Integral nonlinearity is defined as the deviation of a code from a precise analog input voltage. Maximum specifications are limited by the LSB step size and the single shot measurement. Typical specifications are measured from the 1/4, 1/2 and 3/4 areas of the quantization band.

Note 6: For the V_{DD}-SENSE channel, full-scale is at code 255 but codes above 200 may be discarded by offset cancellation. Full scale error and total unadjusted error are evaluated over the 0-200 code range. Full scale voltage corresponds to the theoretical code 255, and is extrapolated from a code 200 measurement.

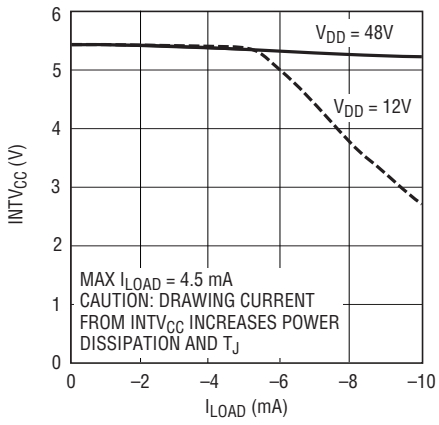
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{DD} = 48V unless otherwise noted.

I_{DD} vs V_{DD}



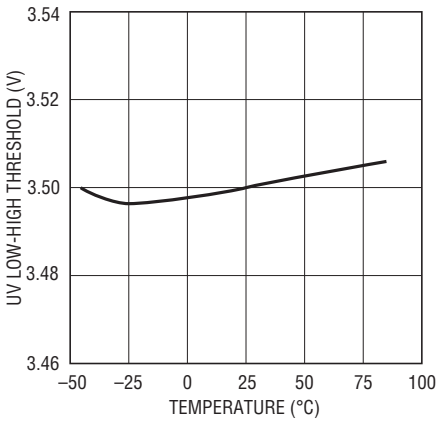
4260 G01

$INTV_{CC}$ vs I_{LOAD}



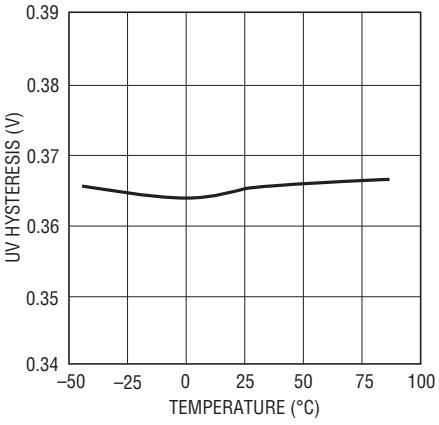
4260 G18

UV Low-High Threshold vs Temperature



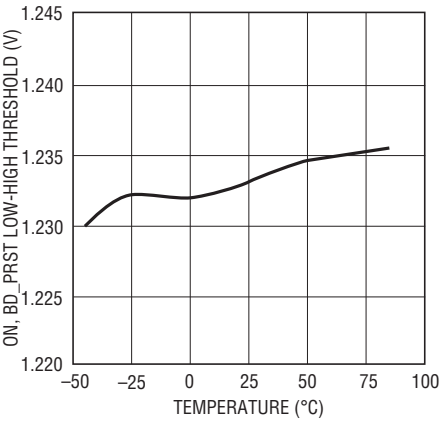
4260 G02

UV Hysteresis vs Temperature



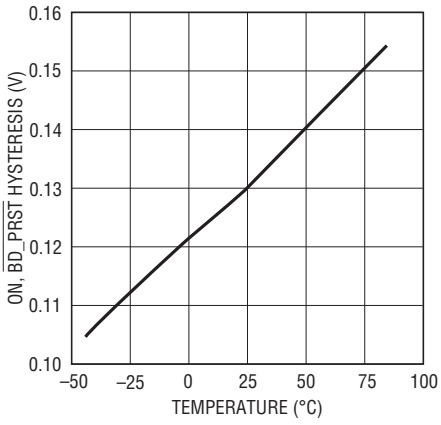
4260 G03

ON, $\overline{BD_PRST}$ Low-High Threshold vs Temperature



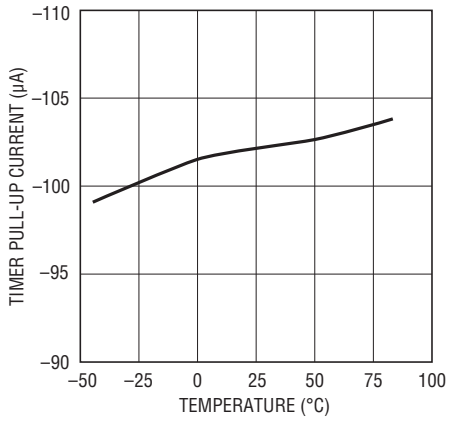
4260 G04

ON, $\overline{BD_PRST}$ Hysteresis vs Temperature



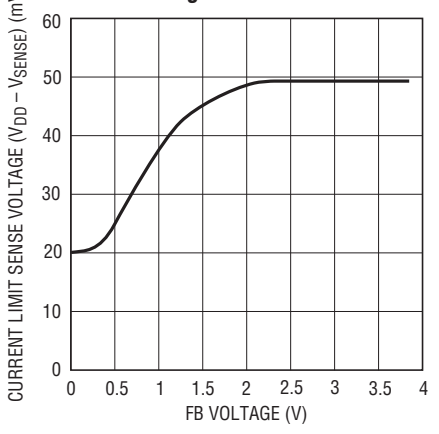
4260 G05

TIMER Pull-Up Current vs Temperature



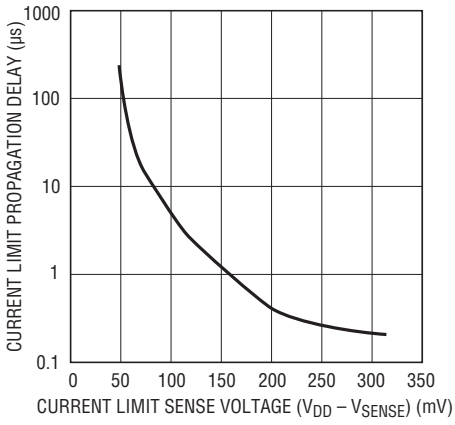
4260 G06

Current Limit Sense Voltage vs FB Voltage



4260 G07

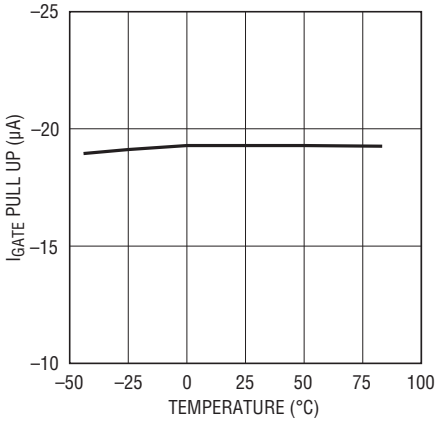
Current Limit Propagation Delay vs Sense Voltage



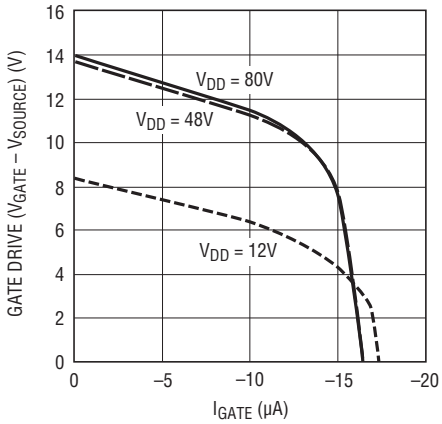
4260 G08

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{DD} = 48V unless otherwise noted.

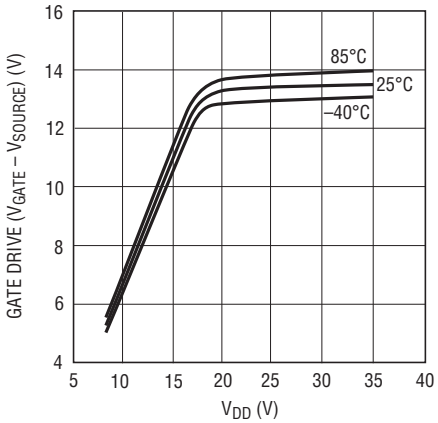
I_{GATE} Pull Up vs Temperature



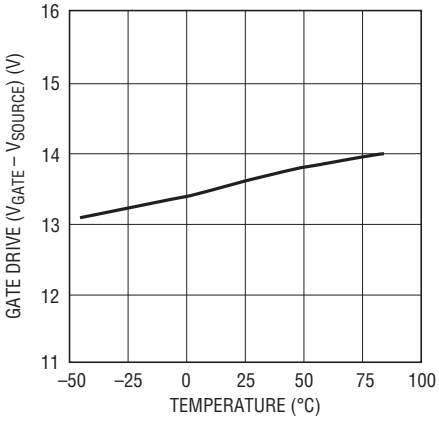
Gate Drive vs I_{GATE}



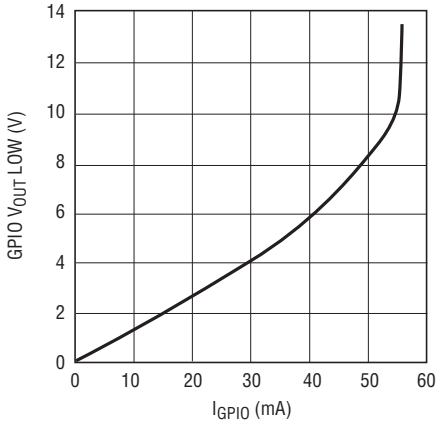
Gate Drive vs V_{DD}



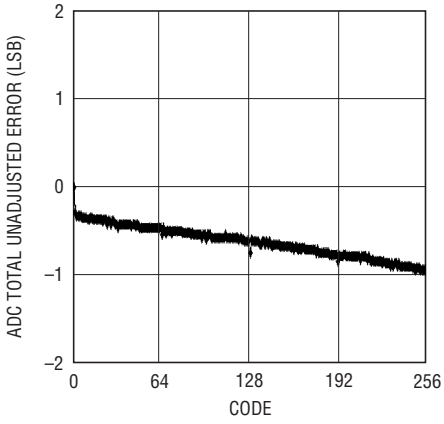
Gate Drive vs Temperature



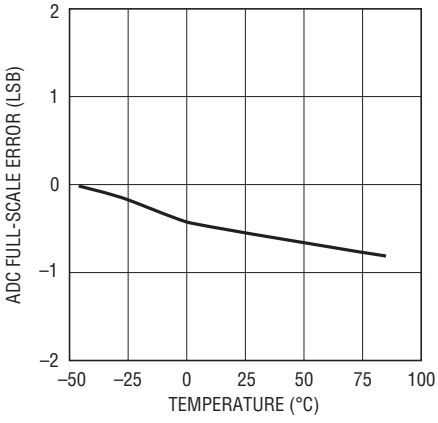
GPIO V_{OUT} Low vs I_{GPIO}



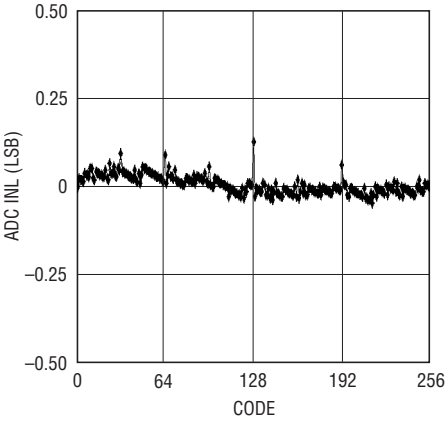
ADC Total Unadjusted Error vs Code (ADIN Pin)



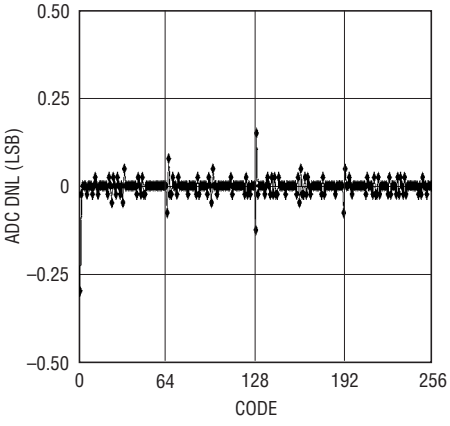
ADC Full-Scale Error vs Temperature (ADIN Pin)



ADC INL vs Code (ADIN Pin)



ADC DNL vs Code (ADIN Pin)



PIN FUNCTIONS

ADIN: ADC Input. A voltage between 0V and 2.56V applied to this pin can be measured by the onboard ADC. Tie to ground if unused.

ADR0 to ADR2: Serial Bus Address Inputs. Tying these pins to ground, open or $INTV_{CC}$ configures one of 27 possible addresses. See Table 1 in Applications Information.

$\overline{ALERT}$: Fault Alert Output. Open-drain logic output that can be pulled to ground when a fault occurs to alert the host controller. A fault alert is enabled by the ALERT register. This device is compatible with SMBus alert protocol. See Applications Information. Tie to ground if unused.

$\overline{BD_PRST}$: Board Present Input. Ground this pin to enable the N-channel FET to turn on after 100ms debounce delay. When this pin is high, the FET is off. An internal 10µA current source pulls up this pin. Transitions on this pin will be recorded in the FAULT register. A high-to-low transition activates the logic to read the state of the ON pin and clear Faults. See Applications Information.

Exposed Pad (Pin 33, UH Package): Exposed pad may be left open or connected to device ground.

FB: Foldback and Power Good Input. A resistive divider from the output voltage is tied to this pin. When the voltage at this pin drops below 3.41V, the output power is considered bad and the current limit is reduced. The power bad condition can be indicated with the GPIO pin and a power bad fault can be logged in this condition. See Applications Information.

GATE: Gate Drive for External N-Channel FET. An internal 18µA current source charges the gate of the external N-channel MOSFET. A resistor and capacitor network from this pin to ground sets the turn-on rate and compensates the active current limit. During turn-off there is a 1mA pull-down current. During a short circuit or undervoltage lockout (V_{DD} or $INTV_{CC}$), a 600mA pull-down current source between GATE and SOURCE is activated.

GND: Device Ground.

GPIO: General Purpose Input/Output. Open-drain logic output and logic input. Defaults to pull low to indicate power is bad. Configure according to Table 3.

$INTV_{CC}$: Internal Low Voltage Supply Decoupling Output. Connect a 0.1µF capacitor from this pin to ground. This pin can be used to drive the other pins to logic high and has an undervoltage lockout threshold of 3.8V.

NC: No Connect. Unconnected pins. These pins provide extra distance between high and low voltage pins.

ON: On Control Input. A rising edge turns on the external N-channel FET and a falling edge turns it off. This pin is also used to configure the state of the FET ON bit (and hence the external FET) at power up. For example if the ON pin is tied high, then the FET ON control bit (A3) will go high 100ms after power-up. Likewise if the ON pin is tied low then the part will remain off after power-up until the FET ON control bit is set high using the I^2C bus. A high-to-low transition on this pin will clear faults.

OV (GN/UH Packages): Overvoltage Comparator Input. Connect this pin to an external resistive divider from V_{DD}. If the voltage at this pin rises above 3.5V, an overvoltage fault is detected and the switch turns off. Tie to GND if unused.

SCL: Serial Bus Clock Input. Data at the SDA pin is shifted in or out on rising edges of SCL. This is a high impedance pin that is generally driven by an open-collector output from a master controller. An external pull-up resistor or current source is required.

SDAI: Serial Bus Data Input. A high impedance input used for shifting in address, command or data bits. Normally tied to SDAO to form the SDA line.

PIN FUNCTIONS

SDAO: Serial Bus Data Output. Open-drain output used for sending data back to the master controller or acknowledging a write operation. Normally tied to SDAI to form the SDA line. An external pull-up resistor or current source is required.

SENSE: Current Sense Input. Connect this pin to the output of the current sense resistor. The current limit circuit controls the GATE pin to limit the sense voltage between the V_{DD} and SENSE pins to 50mV or less depending on the voltage at the FB pin. This pin is used as an input to the 8-bit ADC.

SOURCE: N-Channel MOSFET Source Connection and ADC Input. Connect this pin to the source of the external N-channel MOSFET switch. This pin also serves as the ADC input to monitor output voltage. The pin provides a return for the gate pull-down circuit and as a supply for the charge pump circuit.

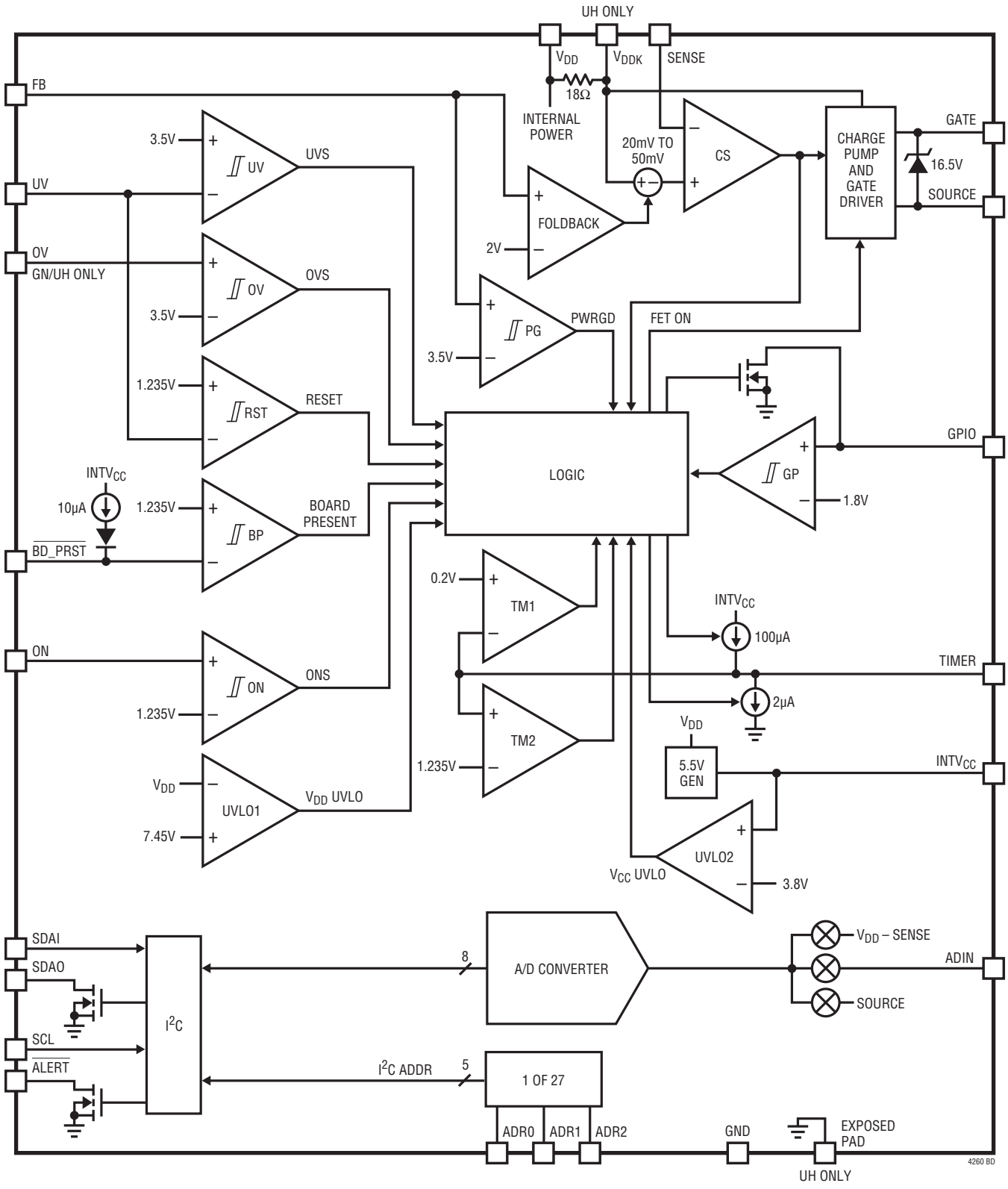
TIMER: Timer Input. Connect a capacitor between this pin and ground to set a 12ms/µF duration for current limit before the switch is turned off. The duration of the off time is 518ms/µF when autoretry during current limit is enabled. A minimum value of 0.1nF must be connected to this pin.

UV: Undervoltage Comparator Input. Connect this pin to an external resistive divider from V_{DD}. If the voltage at this pin falls below 3.12V, an undervoltage fault is detected and the switch turns off. Pulling this pin below 1.2V resets all faults and allows the switch to turn back on. Tie to $INTV_{CC}$ if unused.

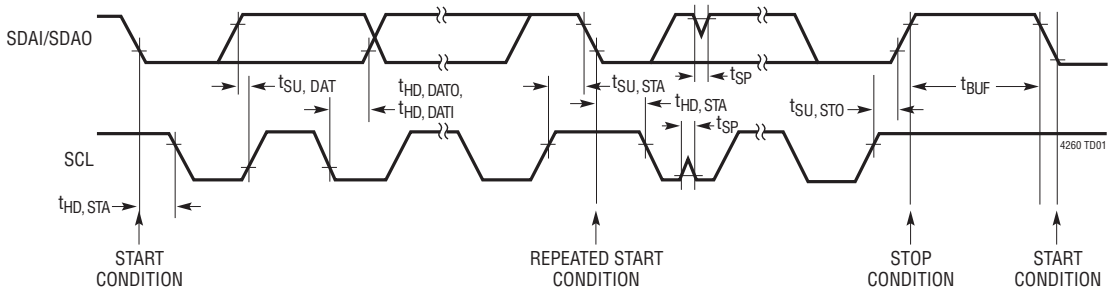
V_{DD}: Supply Voltage and Current Sense Input. This pin has an undervoltage lockout threshold of 7.45V.

V_{DDK} (UH Package): Same as V_{DD}. Connect this pin to V_{DD}. V_{DDK} tied to V_{DD} internally with 18Ω.

FUNCTIONAL DIAGRAM



TIMING DIAGRAM



OPERATION

The Functional Diagram displays the main functional areas of this device. The LTC4260 is designed to turn a board's supply voltage on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. During normal operation, the charge pump and gate driver turn on the external N-channel pass FET's gate to pass power to the load. The gate driver uses a charge pump that derives its power from the SOURCE pin. When the SOURCE pin is at ground, the charge pump is powered from an internal 12V supply derived from V_{DD}. This results in a 200µA current load on the SOURCE pin when the gate is up. Also included in the gate driver is an internal 15V gate-to-source clamp.

The current sense (CS) amplifier monitors the load current using the difference between the V_{DD} and SENSE pin voltage. The CS amplifier limits the current in the load by reducing the GATE-to-SOURCE voltage in an active control loop. The CS amplifier requires 100µA input bias current from both the V_{DD} and the SENSE pins.

A short circuit on the output to ground causes significant power dissipation during active current limiting. To limit this power, the foldback amplifier reduces the current limit value from 50mV to 20mV (referred to the V_{DD} minus SENSE voltage) in a linear manner as the FB pin drops below 2V (see Typical Performance curves).

If an overcurrent condition persists, the TIMER pin ramps up with a 100µA current source until the pin voltage exceeds 1.2V (comparator TM2). This indicates to the logic that it is time to turn off the pass FET to prevent overheating. At this point the TIMER pin ramps down using the 2µA current source until the voltage drops below 0.2V (comparator TM1) which tells the logic that the pass transistor has cooled and it is safe to turn it on again.

The output voltage is monitored using the FB pin and the PG comparator to determine if the power is available for the load. The power good condition is signalled by the GPIO pin using an open-drain pull-down transistor. The GPIO pin can also be used as a general purpose input (GP comparator) or output pin.

The Functional Diagram shows the monitoring blocks of the LTC4260. The group of comparators on the left side includes the UV, OV, RST, BP and ON comparators. These comparators are used to determine if the external conditions are valid prior to turning on the FET. But first the two undervoltage lockout circuits UVLO1 and UVLO2 must validate the input supply and the internally generated 5.5V supply ($INTV_{CC}$) and generate the power up initialization to the logic circuits.

Included in the LTC4260 is an 8-bit A/D converter. The converter has a 3-input mux to select between the ADIN pin, the SOURCE pin and the V_{DD} – SENSE voltage.

An I^2C interface is provided to read the A/D registers. It also allows the host to poll the device and determine if faults have occurred. If the $\overline{ALERT}$ line is used as an interrupt, the host can respond to a fault in real time. The typical SDA line is divided into an SDAI (input) and SDAO (output). This simplifies applications using an optoisolator driven directly from the SDAO output. The I^2C device address is decoded using the ADR0, ADR1 and ADR2 pins. These inputs have three states each that decode into a total of 27 device addresses.

APPLICATIONS INFORMATION

The typical LTC4260 application is in a high availability system that uses a positive voltage supply to distribute power to individual cards. The device measures card voltages and currents and records past and present fault conditions. The system queries each LTC4260 over the I^2C periodically and reads the stored information.

The basic LTC4260 application circuit is shown in Figure 1. External component selection is discussed in detail in the Design Example section.

Turn-On Sequence

The power supply on a board is controlled by placing an external N-channel pass transistor (Q1) in the power path. Note that sense resistor (R_S) detects current and capacitor C1 controls the GATE slew rate. Resistor R6 compensates the current control loop while R5 prevents high frequency oscillations in Q1. Resistors R1, R2 and R3 provide undervoltage and overvoltage sensing.

Several conditions must be present before the external switch can be turned on. First the external supply V_{DD} must exceed its undervoltage lockout level. Next the internally generated supply $INTV_{CC}$ must cross its 4.5V undervoltage threshold. This generates a 60µs to 120µs power-on-reset pulse. During reset the fault registers are cleared and the control registers are set or cleared as described in the register section.

After the power-on-reset pulse, the LTC4260 will go through the following turn-on sequence. First, the UV and OV pins must indicate that the input power is within the acceptable range and the $\overline{BD_PRST}$ pin must be pulled low. All of these conditions must be satisfied for duration of 100ms to ensure that any contact bounce during insertion has ended.

When these initial conditions are satisfied, the ON pin is checked. If it is high, the external switch turns on. If it is low, the external switch turns on when the ON pin is brought high or if a serial bus turn-on command is received.

The switch is turned on by charging up the GATE with a 18µA current source (Figure 2). The voltage at the GATE pin rises with a slope equal to 18µA/C1 and the supply inrush current is set at:

$$I_{INRUSH} = \frac{C_L}{C1} \bullet 18\mu A$$

When the GATE voltage reaches the FET threshold voltage, the switch begins to turn on and the SOURCE voltage follows the GATE voltage as it increases.

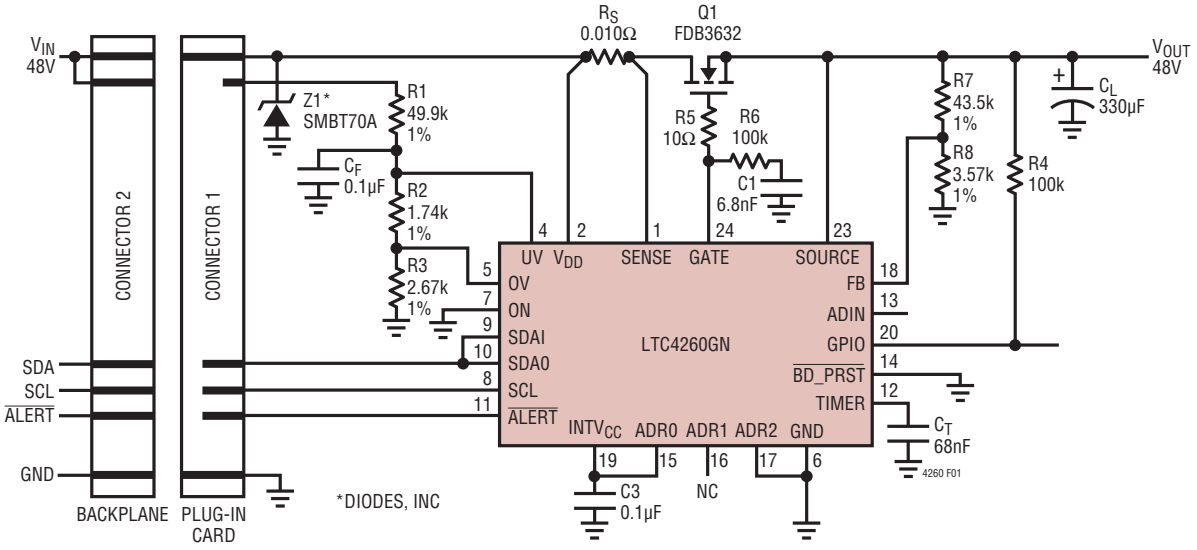


Figure 1. 5A, 48V Card Resident Application

APPLICATIONS INFORMATION

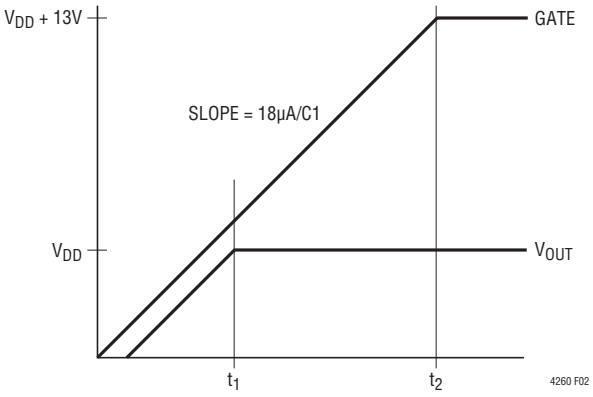


Figure 2. Supply Turn-On

As the SOURCE voltage rises, so will the FB pin which is monitoring it. If the voltage across the current sense resistor R_S gets too high, the inrush current will then be limited by the internal current limit circuitry. Once the FB pin crosses its 3.5V threshold, the GPIO pin, in its default configuration, will cease to pull low and indicate that the power is now good.

Turn-Off Sequence

The switch can be turned off by a variety of conditions. A normal turn-off is initiated by the ON pin going low or a serial bus turn-off command. Additionally, several fault conditions will turn off the switch. These include an input overvoltage (OV pin), input undervoltage (UV pin), overcurrent circuit breaker (SENSE pin) or $\overline{\text{BD_PRST}}$ going high. Writing a logic one into the UV, OV or overcurrent fault bits will also turn off the switch if their autoretry bits are set to false.

Normally the switch is turned off with a 1mA current pulling down the GATE pin to ground. With the switch turned off, the SOURCE voltage drops and when the FB pin crosses below its threshold, GPIO pulls low to indicate that the output power is no longer good.

If the V_{DD} pin falls below 7.5V for greater than 5µs or $INTV_{CC}$ drops below 3.8V for greater than 1µs, a fast shutdown of the switch is initiated. The GATE pin is pulled down with a 600mA current to the SOURCE pin.

Overcurrent Fault

The LTC4260 features an adjustable current limit with foldback that protects against short circuits or excessive load current. To protect against excessive power dissipation in the switch during active current limit, the available current is reduced as a function of the output voltage sensed by the FB pin. The device also features a variable overcurrent response time. A graph in the Typical Performance curves shows the delay from a voltage step at the SENSE pin until the GATE voltage starts falling, as a function of overdrive.

An overcurrent fault occurs when the current limit circuitry has been engaged for longer than the time-out delay set by the TIMER pin. Current limiting begins when the current sense voltage between the V_{DD} and SENSE pins reaches 20mV to 50mV (depending on the foldback). The GATE pin is then brought down with a 600mA GATE-to-SOURCE current. The voltage on the GATE is regulated in order to limit the current sense voltage to less than 50mV. At this point, a circuit breaker time delay starts by charging the external timing capacitor from the TIMER pin with a 100µA pull-up current. If the TIMER pin reaches its 1.2V threshold, the external switch turns off (with a 1mA current from GATE to ground). The overcurrent present bit, C2, and the overcurrent fault bit, D2, are set at this time.

The circuit breaker time delay is given by:

$$t_{CB} = C_T \bullet 12\ [ms/\mu F]$$

After the switch is turned off, the TIMER pin begins discharging the timing capacitor with a 2µA pull-down current. When the TIMER pin reaches its 0.2V threshold, the overcurrent present bit, C2, is cleared, and the switch will be allowed to turn on again if the overcurrent fault has been cleared. However, if the overcurrent autoretry bit, A2, has been set then the switch turns on again automatically (without resetting the overcurrent fault). Use a minimum value of 0.1nF for C_T.

The waveform in Figure 3 shows how the output latches off following a short circuit. The drop across the sense resistor is held at 20mV as the timer ramps up.

APPLICATIONS INFORMATION

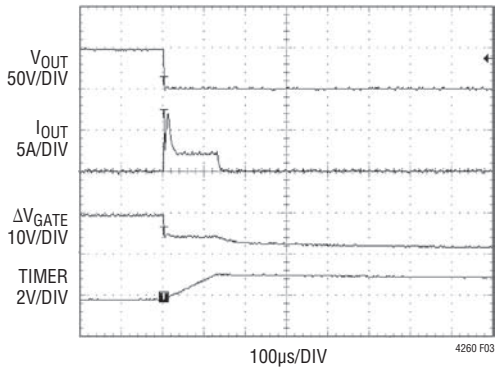


Figure 3. Short-Circuit Waveforms

During a short circuit, if the current limit sense voltage exceeds 150mV, the active current limit enters a high current protection mode that immediately turns off the output transistor by pulling the GATE-to-SOURCE voltage to zero. Current in the output transistor drops from tens of amps to zero in a few hundred nanoseconds. The input voltage will drop during the high current and then spike upwards due to parasitic inductances when the FET shuts off (see Supply Transients). Following this event, the part may turn on again after a delay (typically the 100ms normal turn-on delay if the input voltage drops below the UVLO threshold) and enters active current limit before shutting off.

Overvoltage Fault

An overvoltage fault occurs when the OV pin rises above its 3.5V threshold. This shuts off the switch immediately (with a 1mA current from GATE to ground) and sets the overvoltage present bit, C0, and the overvoltage fault bit D0. If the OV pin subsequently falls back below the threshold for 100ms, the switch will be allowed to turn on again unless the overvoltage autoretry has been disabled by clearing bit A0.

Undervoltage Fault

An undervoltage fault occurs when the UV pin falls below its 3.12V threshold. This turns off the switch immediately (with a 1mA current from GATE to ground) and sets the undervoltage present bit, C1, and the undervoltage fault bit D1. If the UV pin subsequently rises above the threshold for 100ms, the switch will turn on again unless the undervoltage autoretry has been disabled by clearing bit A1. When power is applied to the device, if UV is below its 3.12V threshold after $INTV_{CC}$ crosses its 4.5V undervoltage lockout threshold, an undervoltage fault will be logged in the fault register.

Board Present Change of State

Whenever the $\overline{BD_PRST}$ pin toggles, bit D4 is set to indicate a change of state. When the $\overline{BD_PRST}$ pin goes high, indicating board removal, the switch turns off immediately (with a 1mA current from GATE to ground) and clears the board present bit, C4. If the $\overline{BD_PRST}$ pin is pulled low, indicating a board insertion, all fault bits except D4 will be cleared and the board present bit, C4, is set. If the $\overline{BD_PRST}$ pin remains low for 100ms the state of the ON pin will be captured in the FET On Control bit A3. This turns the switch on if the ON pin is tied high. There is an internal 10µA pull-up current source on the $\overline{BD_PRST}$ pin.

If the system shuts down due to a fault, it may be desirable to restart the system simply by removing and reinserting a load card. In cases where the LTC4260 and the switch reside on a backplane or midplane and the load resides on a plug-in card, the $\overline{BD_PRST}$ pin can be used to detect when the plug-in card is removed (see Figure 4). Once the plug-in card is reinserted the fault register is cleared (except for D4). After 100ms the state of the ON pin is latched into bit A3 of the control register. At this point the system will start up again.

If a connection sense on the plug-in card is driving the $\overline{BD_PRST}$ pin, the insertion or removal of the card may cause the pin voltage to bounce. This will result in clearing the fault register when the card is removed. The pin can be debounced using a filter capacitor, $C_{\overline{BD_PRST}}$, on the $\overline{BD_PRST}$ pin as shown in Figure 4. The filter time is given by:

$$t_{FILTER} = C_{\overline{BD_PRST}} \bullet 123\ [ms/\mu F]$$

FET Short Fault

A FET short fault will be reported if the data converter measures a current sense voltage greater than or equal to 2mV while the FET is turned off. This condition sets the FET short present bit, C5, and the FET short fault bit D5.

APPLICATIONS INFORMATION

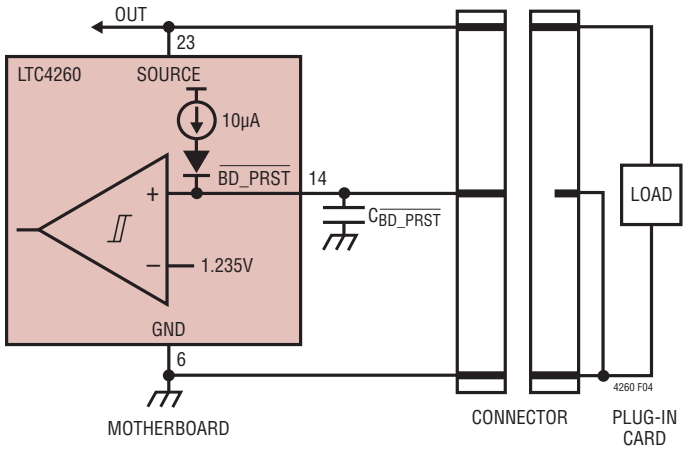


Figure 4. Plug-In Card Insertion/Removal

Power Bad Present/Power Bad Fault

When the FB pin drops below its 3.41V threshold the power bad present bit, C3, goes high. This pulls the GPIO pin low immediately when configured as PWRGD. If the FB pin subsequently rises back above the threshold, the GPIO pin will return to a high impedance state and bit C3 will be cleared.

The power bad fault bit, D3, is set when the GATE-to-SOURCE voltage is high and the power bad present C3 bit is high. This blanking with the gate voltage prevents false power bad faults during power-up or power-down.

Fault Alerts

When any of the fault bits in FAULT register D are set, an optional I^2C bus alert can be generated by setting the appropriate bit in the ALERT register B. This allows only selected faults to generate alerts. At power-up the default state is to not alert on faults. If an alert is enabled, the corresponding fault will cause the $\overline{\text{ALERT}}$ pin to pull low. After the bus master controller broadcasts the Alert Response Address, the LTC4260 responds with its address on the SDA line and releases $\overline{\text{ALERT}}$ as shown in Figure 11. If there is a collision between two LTC4260s responding with their addresses simultaneously, then the device with the lower address wins arbitration and responds first. The $\overline{\text{ALERT}}$ line will also be released if the device is addressed by the bus master.

Once the $\overline{\text{ALERT}}$ signal has been released for one fault, it will not be pulled low again until the FAULT register indicates a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults will not generate alerts until the associated FAULT register bit has been cleared.

Resetting Faults

Faults are reset with any of the following conditions. First, a serial bus command writing zeros to the FAULT register D will clear the associated faults. Second, the entire FAULT register is cleared when the switch is turned off by either the ON pin or bit A3 going from high to low, or if the UV pin is brought below its 1.23V reset threshold, or if $INTV_{CC}$ falls below its 3.8V undervoltage lockout threshold. Finally, when $\overline{\text{BD_PRST}}$ is brought from high to low, only FAULT bits D0-D3 and D5 are cleared, the bit D4 that indicates a $\overline{\text{BD_PRST}}$ change of state will be set. Faults that are still present (as indicated in the STATUS Register C) cannot be cleared.

The FAULT register will not be cleared when autoretrying. When autoretry is disabled the existence of a D0, D1 or D2 fault keeps the switch off. As soon as the fault is cleared, the switch will turn on. If autoretry is enabled, then a high value in C0, C1 or C2 will hold the switch off and the FAULT register is ignored. Subsequently, when the C0, C1 and C2 bits are cleared, the switch is allowed to turn on again.

Data Converter

The LTC4260 incorporates an 8-bit data converter that continuously monitors three different voltages. The ΔΣ architecture inherently averages signal noise during the measurement period. The SOURCE pin uses a 1/40 resistive divider to monitor a full-scale voltage of 102.4V with 0.4V resolution (divider converts 102.4V to 2.56V). The ADIN pin is monitored with a 2.56V full scale and 10mV resolution, and the voltage between the V_{DD} and SENSE pins is monitored with a 76.8mV full scale and 300µV resolution.

The results from each conversion are stored in registers E, F and G and are updated 10 times per second. Setting CONTROL register bit A5 invokes a test mode that halts the data converter updates so that registers E, F and G can be written to and read from for software testing.

APPLICATIONS INFORMATION

Gate Pin Voltage

A curve of gate drive vs V_{DD} is shown in the Typical Performance curves. At the minimum input supply voltage of 8.5V, the minimum gate drive voltage is 4.5V. When the input supply voltage is higher than 20V, the gate drive is at least 10V and a regular N-FET can be used. In applications over a 8.5V to 20V range, a logic level N-FET must be used to maintain adequate gate enhancement. The GATE pin is clamped at a typical value of 15V above the SOURCE pin.

Configuring the GPIO Pin

Table 3 describes the possible states of the GPIO pin using the control register bits A6 and A7. At power-up, the default state is for the GPIO pin to go high impedance when power is good (FB pin greater than 3.5V). Other uses for the GPIO pin are to pull down when power is good, a general purpose output and a general purpose input.

Compensating the Active Current Loop

The active current limit circuit is compensated using the resistor R6 and the slew rate capacitor C1. The value for C1 is calculated to limit the inrush current. The suggested value for R6 is 100k. This value should work for most pass FETs (Q1). If the gate capacitance of Q1 is very small then the best method to compensate the loop is to add a ≈10nF capacitor between the GATE and SOURCE terminals.The addition of 10Ω resistor (R5) prevents self-oscillation in Q1 by isolating trace capacitance from the FET's GATE Terminal. Locate the gate resistor at, or close to, the body of the MOSFET.

Supply Transients

The LTC4260 is designed to ride through supply transients caused by load steps. If there is a shorted load and the parasitic inductance back to the supply is greater than 0.5µH, there is a chance that the supply could collapse before the active current limit circuit brings down the GATE pin. In this case the undervoltage monitors turn off the pass FET. The undervoltage lockout circuit has a 5µs filter time after V_{DD} drops below 7.5V. The UV pin reacts in 2µs to shut the GATE off, but it is recommended to add a filter capacitor C_F to prevent unwanted shutdown caused by short transient. Eventually either the UV pin or the undervoltage lockout responds to bring the current under control before the supply completely collapses.

Supply Transient Protection

The LTC4260 is 100% tested and guaranteed to be safe from damage with supply voltages up to 100V. However, spikes above 100V may damage the part. During a short-circuit condition, the large change in currents flowing through the power supply traces can cause inductive voltage spikes which could exceed 100V. To minimize the spikes, the power trace inductance should be minimized by using wider traces or heavier trace plating. Adding a snubber circuit will dampen the voltage spikes. It is built using a 100Ω resistor in series with a 0.1µF capacitor between V_{DD} and GND. A surge suppressor, Z1 in Figure 1, at the input will clamp the voltage spikes.

Design Example

As a design example, take the following specifications: V_{IN} = 48V, I_{MAX} = 5A, I_{INRUSH} = 1A, C_L= 330µF, V_{UVON} = 43V, V_{UVOFF} = 38.5V, V_{OVOFF} = 70V, $V_{PWRGDUP}$ = 46V, $V_{PWRGDDN}$ = 45V and $I^2C_{ADDRESS}$ = 1010011. The selection of the sense resistor, R_S, is set by the overcurrent threshold of 50mV:

$$R_S = \frac{50mV}{I_{MAX}} = \frac{50mV}{5A} = 0.010\Omega$$

The FET should be sized to handle the power dissipation during the inrush charging of the output capacitor C_{OUT}. The method used to determine the power is the principle:

E_C = Energy in C_L= Energy in Q1

Thus:

$E_C = 1/2\ CV^2 = 1/2(0.33mF)(48V)^2 = 0.38J$

Calculate the time it takes to charge up C_{OUT}:

$$t_{CHARGUP} = \frac{C_L \bullet V_{IN}}{I_{INRUSH}} = \frac{330\mu F \bullet 48V}{1A} = 16ms$$

The average power dissipated in the FET:

$$P_{DISS} = \frac{E_C}{t_{CHARGUP}} = \frac{0.38J}{16ms} \cong 24W$$

APPLICATIONS INFORMATION

The SOA (safe operating area) curves of candidate FETs must be evaluated to ensure that the heat capacity of the package can stand 24W for 16ms. The SOA curves of the Fairchild FDB3632 provide for 1A at 50V (50W) for 10ms, satisfying the requirement.

The inrush current is set to 1A using C1:

$$C1 = C_L \frac{I_{GATE(UP)}}{I_{INRUSH}} = 0.33mF \frac{18\mu A}{1A} = 5.9nF$$

Default values of R5 = 10Ω and R6 = 100k are chosen as discussed previously.

The power dissipated in the FET during overcurrent must be limited. The active current limit uses a timer to prevent excessive energy dissipation in the FET. The worst-case power occurs when the voltage versus current profile of the foldback current limit is at the maximum. This occurs when the current is 5A and the voltage is 1/2 of the 48V or 24V. See the Current Limit Sense Voltage vs FB Voltage in the Typical Performance curves to view this profile. In order to survive 120W, the FET SOA curve dictates the maximum time at this power level. This particular FET allows 300W at 1ms or less. Therefore, it is acceptable to set the current limit timeout using C_T to be 0.81ms:

$$C_T = \frac{0.81ms}{12\ [ms/\mu F]} = 68nF$$

Note the minimum value for C_T is 0.1nF.

Choose R1, R2, R3, R7 and R8 for the UV, OV and PG threshold voltages:

$V_{OVRISING}$ = 71.2V, $V_{OVFALLING}$ = 69.44V (using $V_{OV(TH)}$ = 3.5V rising and 3.41V falling)

$V_{UVRISING}$ = 43V, $V_{UVFALLING}$ = 38.5V, (using $V_{UV(TH)}$ = 3.5V rising and 3.12V falling)

$V_{PGRISING}$ = 46.14V, $V_{PGFALLING}$ = 45V, (using V_{FB} = 3.5V rising and 3.411V falling)

In addition a 0.1µF ceramic bypass capacitor is placed on the $INTV_{CC}$ pin. The complete circuit is shown in Figure 1.

Layout Considerations

To achieve accurate current sensing, a Kelvin connection is recommended. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530µΩ/square. Small resistances add up quickly in high current applications. To improve noise immunity, put the resistive divider to the UV, OV and FB pins close to the device and keep traces to V_{DD} and GND short. It is also important to put C3, the bypass capacitor for the $INTV_{CC}$ pin, as close as possible between $INTV_{CC}$ and GND. A 0.1µF capacitor from the UV pin (and OV pin through resistor R2) to GND also helps reject supply noise. Figure 5 shows a layout that addresses these issues. Note that a surge suppressor, Z1, is placed between supply and ground using wide traces.

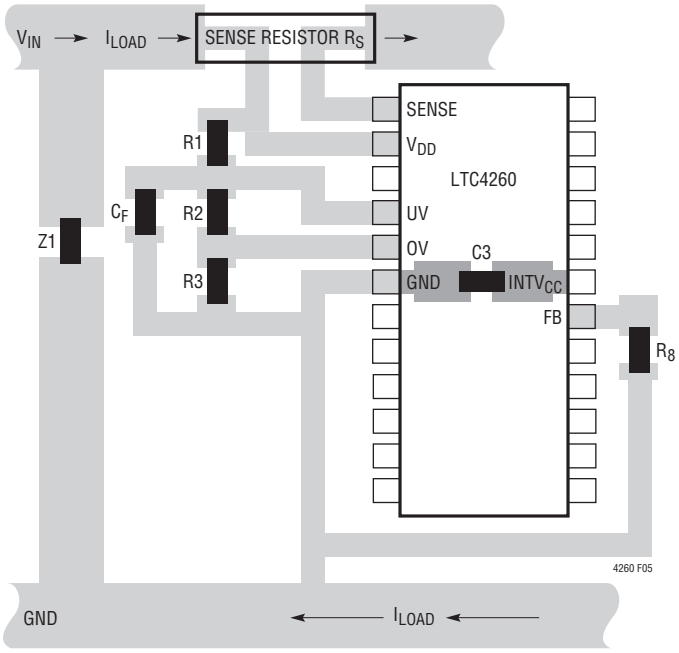


Figure 5. Recommended Layout for R1, R2, R3, R8, C_F, C3, Z1 and R_S

APPLICATIONS INFORMATION

Digital Interface

The LTC4260 communicates with a bus master using a 2-wire interface compatible with the I^2C bus and the SMBus, an I^2C extension for low power devices.

The LTC4260 is a read-write slave device and supports SMBus bus Read Byte, Write Byte, Read Word and Write Word commands. The second word in a Read Word command will be identical to the first word. The second word in a Write Word command is ignored. The data formats for these commands are shown in Figures 6 to 10.

Using Optoisolators with SDA

The LTC4260 separates the SDA line into SDAI and SDAO. If optoisolators are not used then tie SDAI and SDAO together to construct a normal SDA line. When using optoisolators connect the SDAI to the output of the incoming opto and connect the SDAO to the input of the outgoing opto (see Figure 13).

START and STOP Conditions

When the bus is idle, both SCL and SDA must be high (Figure 6). A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

I^2C Device Addressing

Twenty-seven distinct bus address are configurable using the three-state ADR0-ADR2 pins. Table 1 shows the correspondence between pin states and addresses. Note that address bits B7 and B6 are internally configured to 10. In addition, the LTC4260 will respond to two special addresses. Address (1011 111)b is a mass write used to write to all LTC4260, regardless of their individual address settings. The mass write can be masked by setting register bit A4 to zero. Address (0001 100)b is the SMBus Alert Response Address. If the LTC4260 is pulling low on the $\overline{\text{ALERT}}$ pin, it will acknowledge this address using the SMBus Alert Response Protocol.

Acknowledge

The acknowledge signal is used for handshaking between the transmitter and the receiver to indicate that the last byte of data was received. The transmitter always releases the SDA line during the acknowledge clock pulse. When the slave is the receiver, it must pull down the SDA line so that it remains LOW during this pulse to acknowledge receipt of the data. If the slave fails to acknowledge by leaving SDA HIGH, then the master can abort the transmission by generating a STOP condition. When the master is receiving data from the slave, the master must pull down the SDA line during the clock pulse to indicate receipt of the data. After the last byte has been received the master will leave the SDA line HIGH (not acknowledge) and issue a STOP condition to terminate the transmission.

Write Protocol

The master begins communication with a START condition followed by the seven bit slave address and the R/$\overline{\text{W}}$ bit set to zero (Figure 7). The addressed LTC4260 acknowledges this and then the master sends a command byte which indicates which internal register the master wishes to write. The LTC4260 acknowledges this and then latches the lower three bits of the command byte into its internal Register Address pointer. The master then delivers the data byte and the LTC4260 acknowledges once more and latches the data into its internal register. The transmission is ended when the master sends a STOP condition. If the master continues sending a second data byte, as in a Write Word command, the second data byte will be acknowledged by the LTC4260 but ignored (Figure 8).

Read Protocol

The master begins a read operation with a START condition followed by the seven bit slave address and the R/$\overline{\text{W}}$ bit set to zero (Figure 9). The addressed LTC4260 acknowledges this and then the master sends a command byte that indicates which internal register the master wishes to read. The LTC4260 acknowledges this and then latches the lower three bits of the command byte into its internal Register Address pointer. The master then sends a repeated START condition followed by the same seven bit address with the

APPLICATIONS INFORMATION

R/$\overline{W}$ bit now set to one. The LTC4260 acknowledges and sends the contents of the requested register. The transmission is ended when the master sends a STOP condition. If the master acknowledges the transmitted data byte, as in a Read Word command (Figure 12), the LTC4260 will repeat the requested register as the second data byte.

Note that the Register Address pointer is not cleared at the end of the transaction. Thus the Receive Byte protocol can be used to repeatedly read a specific register.

Alert Response Protocol

The LTC4260 implements the SMBus Alert Response Protocol as shown in Figure 11. If enabled to do so through the ALERT register B, the LTC4260 will respond to faults by pulling the $\overline{ALERT}$ pin low. Multiple LTC4260s can share a common $\overline{ALERT}$ line and the protocol allows a master to determine which LTC4260s are pulling the line low. The master begins by sending a START bit followed by the special Alert Response Address (0001 100)b with the R/$\overline{W}$ bit set to one. Any LTC4260 that is pulling its $\overline{ALERT}$ pin low will acknowledge and begin sending back its individual slave address.

An arbitration scheme ensures that the LTC4260 with the lowest address will have priority; all others will abort their response. The successful responder will then release its $\overline{ALERT}$ pin while any others will continue to hold their $\overline{ALERT}$ pins low. Polling may also be used to search for any LTC4260 that have detected faults. Any LTC4260 pulling its $\overline{ALERT}$ pin low will also release it if it is individually addressed during a read or write transaction.

The $\overline{ALERT}$ signal will not be pulled low again until the FAULT register indicates a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults will not generate alerts until the associated FAULT register bit has been cleared.

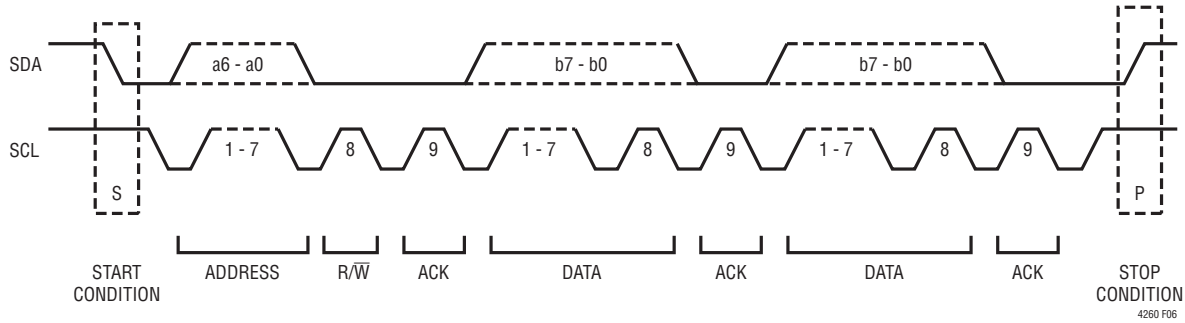


Figure 6. Data Transfer Over I^2C or SMBus

APPLICATIONS INFORMATION

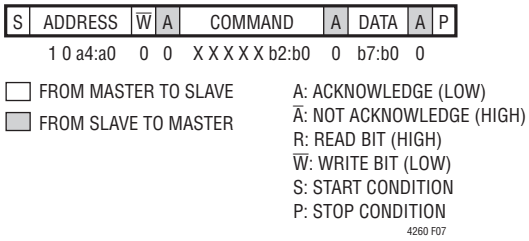


Figure 7. LTC4260 Serial Bus SDA Write Byte Protocol

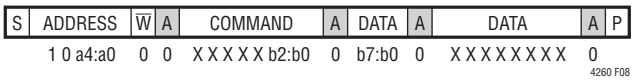


Figure 8. LTC4260 Serial Bus SDA Write Word Protocol

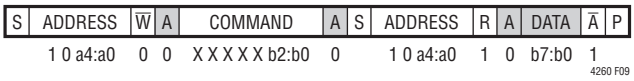


Figure 9. LTC4260 Serial Bus SDA Read Byte Protocol

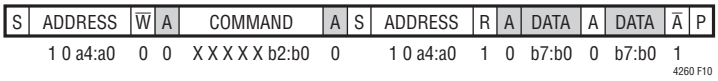


Figure 10. LTC4260 Serial Bus SDA Read Word Protocol

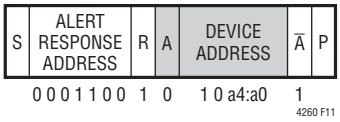


Figure 11. LTC4260 Serial Bus SDA Alert Response Protocol

APPLICATIONS INFORMATION

Table 1. LTC4260 I²C Device Addressing

DESCRIPTION	HEX DEVICE ADDRESS	BINARY DEVICE ADDRESS								LTC4260 ADDRESS PINS		
	h	6	5	4	3	2	1	0	R/$\overline{W}$	ADR2	ADR1	ADR0
Mass Write	BE	1	0	1	1	1	1	1	0	X	X	X
Alert Response	19	0	0	0	1	1	0	0	1	X	X	X
0	80	1	0	0	0	0	0	0	X	L	NC	L
1	82	1	0	0	0	0	0	1	X	L	H	NC
2	84	1	0	0	0	0	1	0	X	L	NC	NC
3	86	1	0	0	0	0	1	1	X	L	NC	H
4	88	1	0	0	0	1	0	0	X	L	L	L
5	8A	1	0	0	0	1	0	1	X	L	H	H
6	8C	1	0	0	0	1	1	0	X	L	L	NC
7	8E	1	0	0	0	1	1	1	X	L	L	H
8	90	1	0	0	1	0	0	0	X	NC	NC	L
9	92	1	0	0	1	0	0	1	X	NC	H	NC
10	94	1	0	0	1	0	1	0	X	NC	NC	NC
11	96	1	0	0	1	0	1	1	X	NC	NC	H
12	98	1	0	0	1	1	0	0	X	NC	L	L
13	9A	1	0	0	1	1	0	1	X	NC	H	H
14	9C	1	0	0	1	1	1	0	X	NC	L	NC
15	9E	1	0	0	1	1	1	1	X	NC	L	H
16	A0	1	0	1	0	0	0	0	X	H	NC	L
17	A2	1	0	1	0	0	0	1	X	H	H	NC
18	A4	1	0	1	0	0	1	0	X	H	NC	NC
19	A6	1	0	1	0	0	1	1	X	H	NC	H
20	A8	1	0	1	0	1	0	0	X	H	L	L
21	AA	1	0	1	0	1	0	1	X	H	H	H
22	AC	1	0	1	0	1	1	0	X	H	L	NC
23	AE	1	0	1	0	1	1	1	X	H	L	H
24	B0	1	0	1	1	0	0	0	X	L	H	L
25	B2	1	0	1	1	0	0	1	X	NC	H	L
26	B4	1	0	1	1	0	1	0	X	H	H	L

APPLICATIONS INFORMATION

Table 2. LTC4260 Register Addresses and Contents

REGISTER ADDRESS*	REGISTER NAME	READ/WRITE	DESCRIPTION
00h	CONTROL (A)	R/W	Controls Whether the Part Retries After Faults, Set the Switch State
01h	ALERT (B)	R/W	Controls Whether the ALERT Pin is Pulled Low After a Fault is Logged in the Fault Register
02h	STATUS (C)	R	System Status Information
03h	FAULT (D)	R/W	Fault Log
04h	SENSE (E)	R/W**	ADC Current Sense Voltage Data
05h	SOURCE (F)	R/W**	ADC SOURCE Voltage Data
06h, 07h	ADIN (G)	R/W**	ADC ADIN Voltage Data

*Register address MSBs b7-b3 are ignored.
**Writable if bit A5 set.

Table 3. CONTROL Register A (00h)—Read/Write

BIT	NAME	OPERATION
A7:6	GPIO Configure	Configures Behavior of GPIO Pin

FUNCTION	A6	A7	GPIO PIN
Power Good (Default)	0	0	GPIO = $\overline{C3}$
Power Bad	0	1	GPIO = C3
General Purpose Output	1	0	GPIO = B6
General Purpose Input	1	1	GPIO = Hi-Z

A5	Test Mode Enable	Test Mode Halts ADC Operation and Enables Writes to ADC Registers 1 = Enable Test Mode, 0 = Disable Test Mode (Default)
A4	Mass Write Enable	Enables Mass Write Using Address (1011 111)b 1 = Enable Mass Write (Default), 0 = Disable Mass Write
A3	FET On Control	Turns FET On and Off 1 = Turn FET On, 0 = Turn FET Off. Defaults to ON Pin State at End of Debounce Delay
A2	Overcurrent Autoretry	Enables Autoretry After an Overcurrent Fault 1 = Retry Enabled, 0 = Retry Disabled (Default)
A1	Undervoltage Autoretry	Enables Autoretry After an Undervoltage Fault 1 = Retry Enabled (Default), 0 = Retry Disabled
A0	Overvoltage Autoretry	Enables Autoretry After an Overvoltage Fault 1 = Retry Enabled (Default), 0 = Retry Disabled

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Table 4. ALERT Register B (01h)—Read/Write

BIT	NAME	OPERATION
B7	Reserved	Not Used
B6	GPIO Output	Output Data Bit to GPIO Pin When Configured as Output. Defaults to 0
B5	FET Short Alert	Enables Alert for FET Short Condition 1 = Enable Alert, 0 = Disable Alert (Default)
B4	$\overline{\text{BD_PRST}}$ State Change Alert	Enables Alert When $\overline{\text{BD_PRST}}$ Changes State 1 = Enable Alert, 0 = Disable Alert (Default)
B3	Power Bad Alert	Enables Alert when Output Power is Bad 1 = Enable Alert, 0 = Disable Alert (Default)
B2	Overcurrent Alert	Enables Alert for Overcurrent Condition 1 = Enable Alert, 0 = Disable Alert (Default)
B1	Undervoltage Alert	Enables Alert for Undervoltage Condition 1 = Enable Alert, 0 = Disable Alert (Default)
B0	Overvoltage Alert	Enables Alert for Overvoltage Condition 1 = Enable Alert, 0 = Disable Alert (Default)

Table 5. STATUS Register C (02h)—Read Only

BIT	NAME	OPERATION
C7	FET On	Indicates State of FET 1 = FET On, 0 = FET Off
C6	GPIO Input	State of the GPIO Pin 1 = GPIO High, 0 = GPIO Low
C5	FET Short Present	Indicates Potential FET Short if Current Sense Voltage Exceeds 2mV While FET is Off 1 = FET is Shorted, 0 = FET is Not Shorted
C4	Board Present	Indicates if a Board is Present When $\overline{\text{BD_PRST}}$ is Low 1 = $\overline{\text{BD_PRST}}$ Pin Low, 0 = $\overline{\text{BD_PRST}}$ Pin High
C3	Power Bad	Indicates Power is Bad When FB is Low 1 = FB Low, 0 = FB High
C2	Overcurrent	Indicates Overcurrent Condition During Cool Down Cycle 1 = Overcurrent, 0 = Not Overcurrent
C1	Undervoltage	Indicates Input Undervoltage When UV is Low 1 = UV Low, 0 = UV High
C0	Overvoltage	Indicates Input Overvoltage When OV is High 1 = OV High, 0 = OV Low

APPLICATIONS INFORMATION

Table 6. FAULT Register D (03h)—Read/Write

BIT	NAME	OPERATION
D7:6	Reserved	
D5	FET Short Fault Occurred	Indicates Potential FET Short was Detected When Measured Current Sense Voltage Exceeded 2mV (code 0000111) While FET was Off 1 = FET was Shorted, 0 = FET is Good
D4	Board Present Changes State	Indicates that a Board was Inserted or Extracted When $\overline{BD_PRST}$ Changed State 1 = $\overline{BD_PRST}$ Changed State, 0 = $\overline{BD_PRST}$ Unchanged
D3	Power Bad Fault Occurred	Indicates Power was Bad When FB Went Low (C3 = 1) While Gate-to-Source was High 1 = FB was Low and Gate was High, 0 = FB was Low and Gate was Low, or FB was High and Gate was High or Low
D2	Overcurrent Fault Occurred	Indicates Overcurrent Fault Occurred 1 = Overcurrent Fault Occurred, 0 = No Overcurrent Faults
D1	Undervoltage Fault Occurred	Indicates Input Undervoltage Fault Occurred When UV Went Low 1 = UV was Low, 0 = UV was High
D0	Overvoltage Fault Occurred	Indicates Input Overvoltage Fault Occurred When OV Went High 1 = OV was High, 0 = OV was Low

Table 7. SENSE Register E (04h)—Read/Write

BIT	NAME	OPERATION
E7:0	SENSE Voltage Data	V_{DD}-SENSE Current Sense Voltage Data. 8-Bit Data with 300µV LSB and 76.8mV Full Scale

Table 8. SOURCE Register F (05h)—Read/Write

BIT	NAME	OPERATION
F7:0	SOURCE Voltage Data	SOURCE Pin Voltage Data. 8-Bit Data with 400mV LSB and 102.4V Full Scale

Table 9. ADIN Register G (06h)—Read/Write

BIT	NAME	OPERATION
G7:0	ADIN Voltage Data	ADIN Pin Voltage Data. 8-Bit Data with 10mV LSB and 2.56V Full Scale

APPLICATIONS INFORMATION

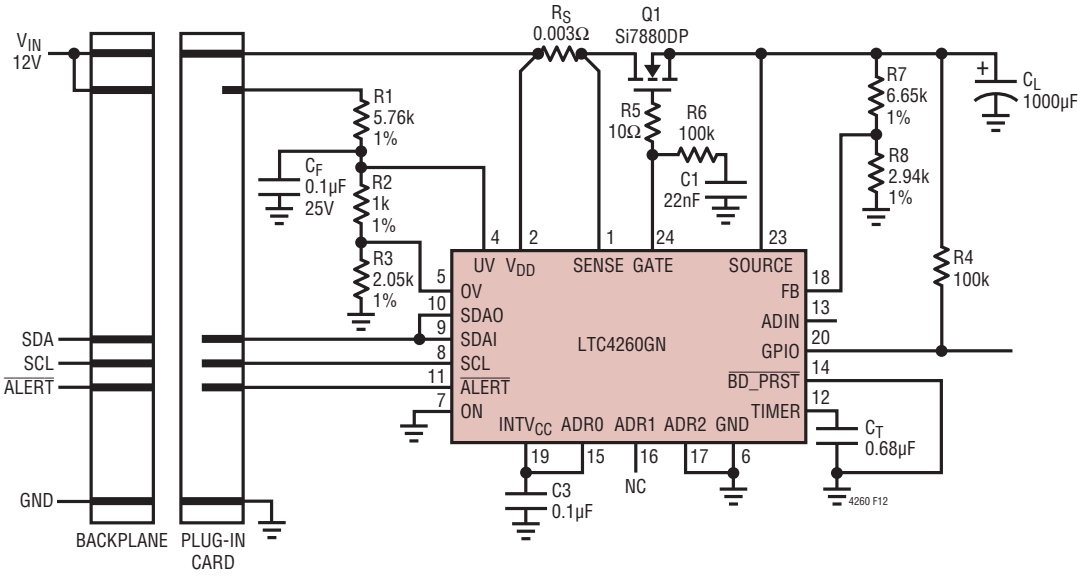


Figure 12. 12A, 12V Card Resident Application

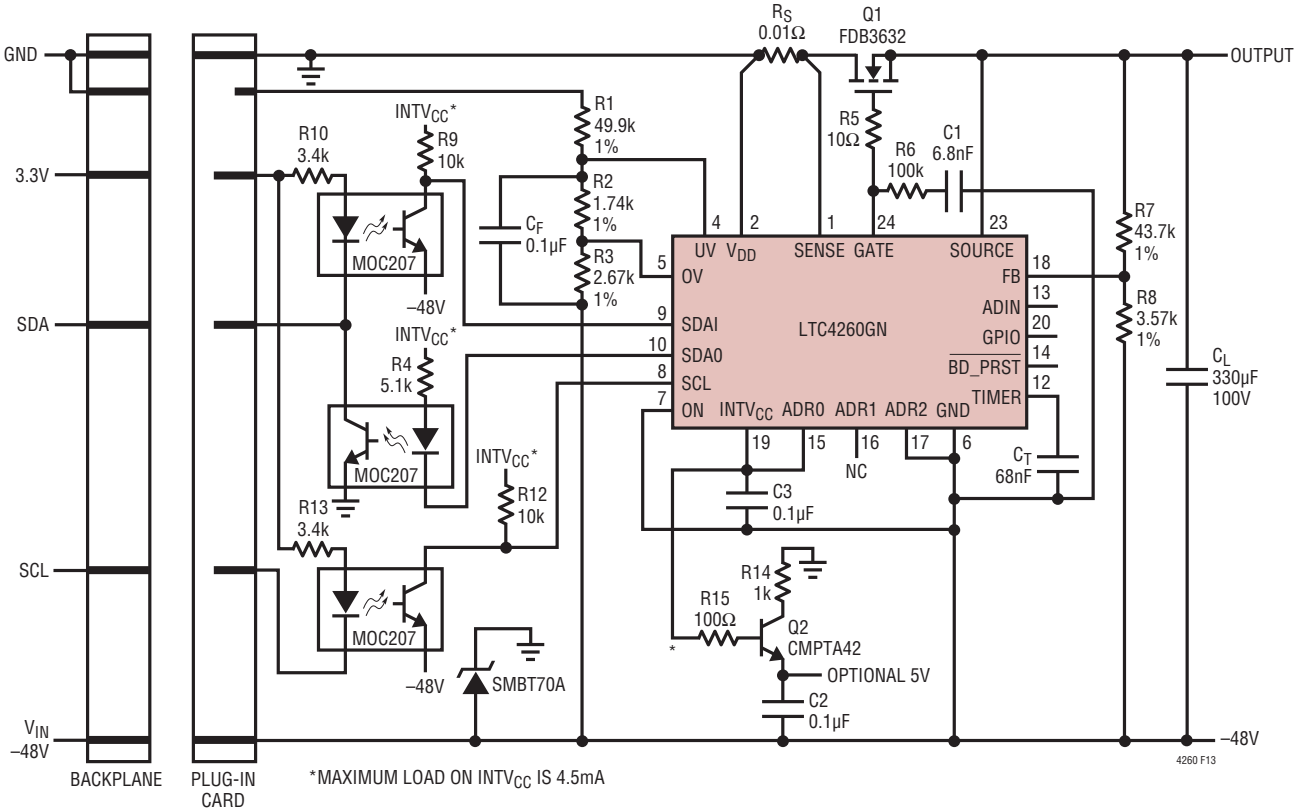
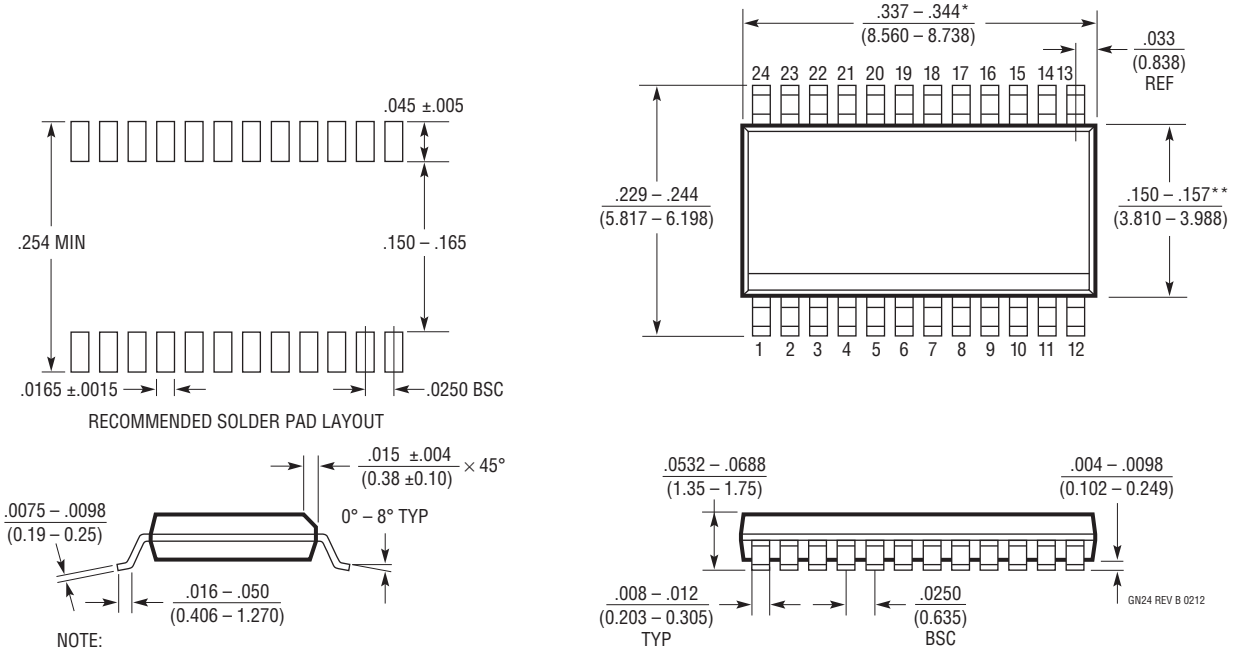


Figure 13. 3A, –48V Card Resident Application

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

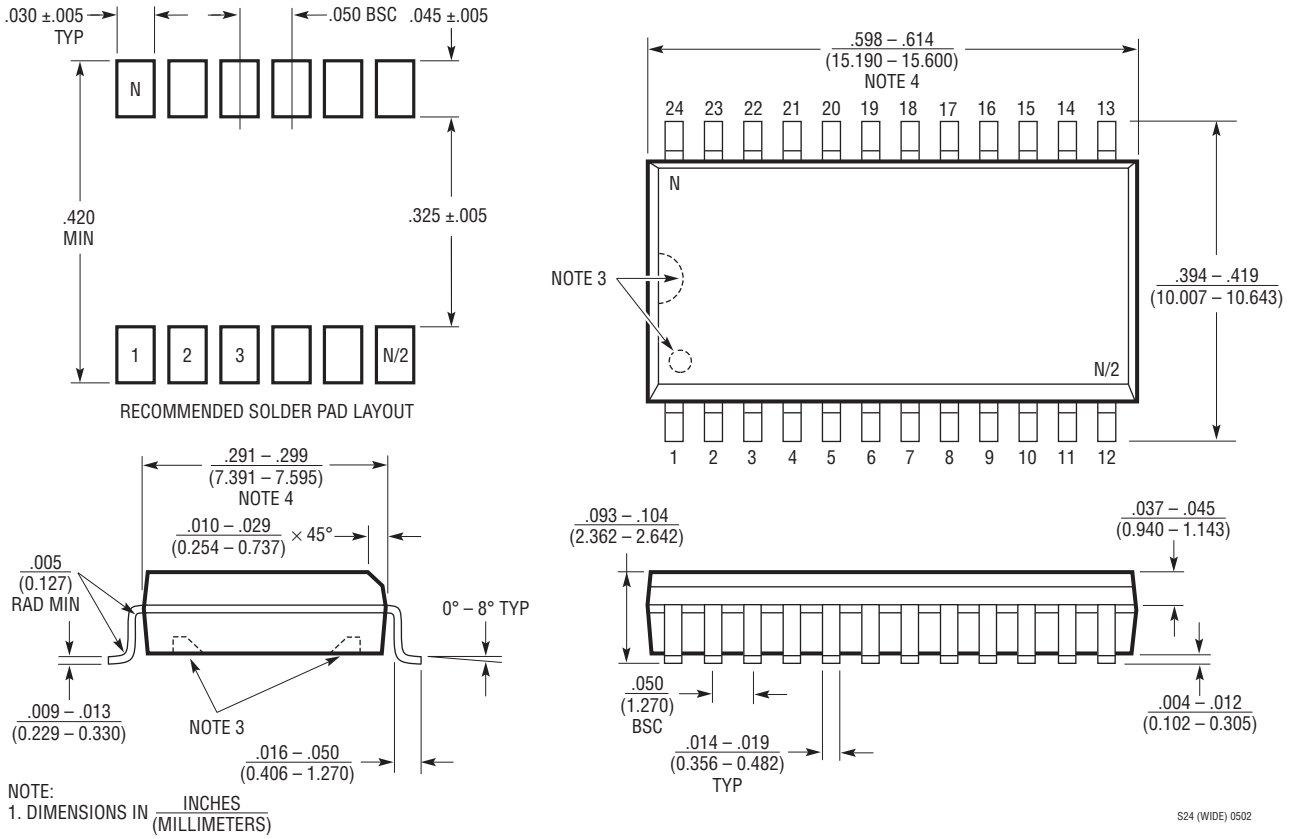
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

SW Package
24-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)

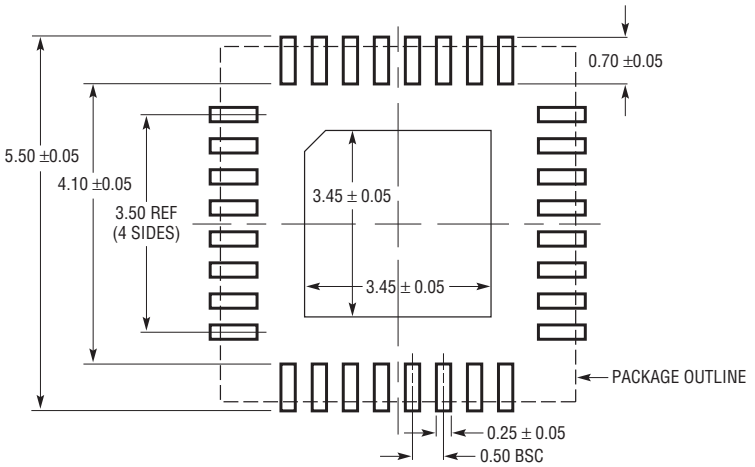


NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
   THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

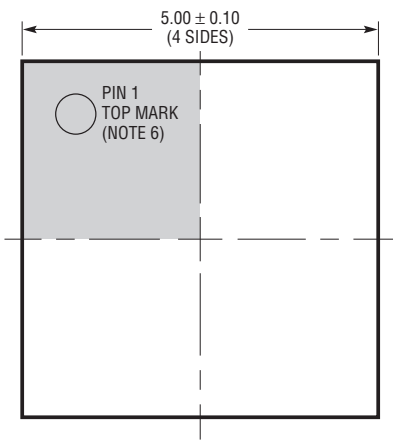
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

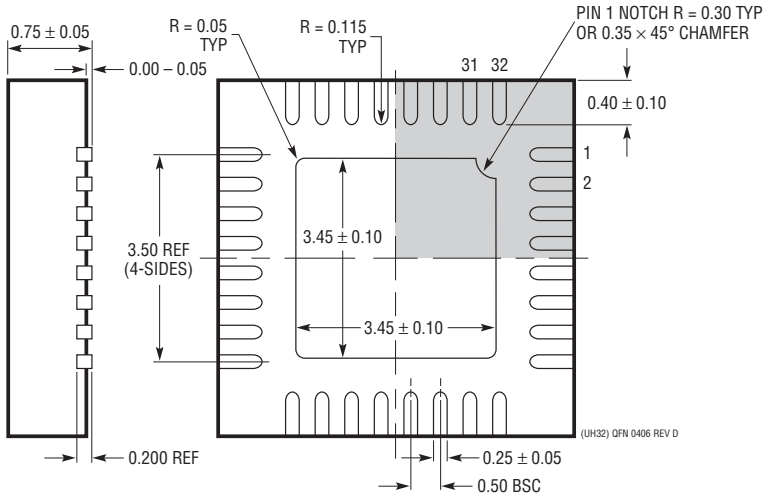
UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev B)

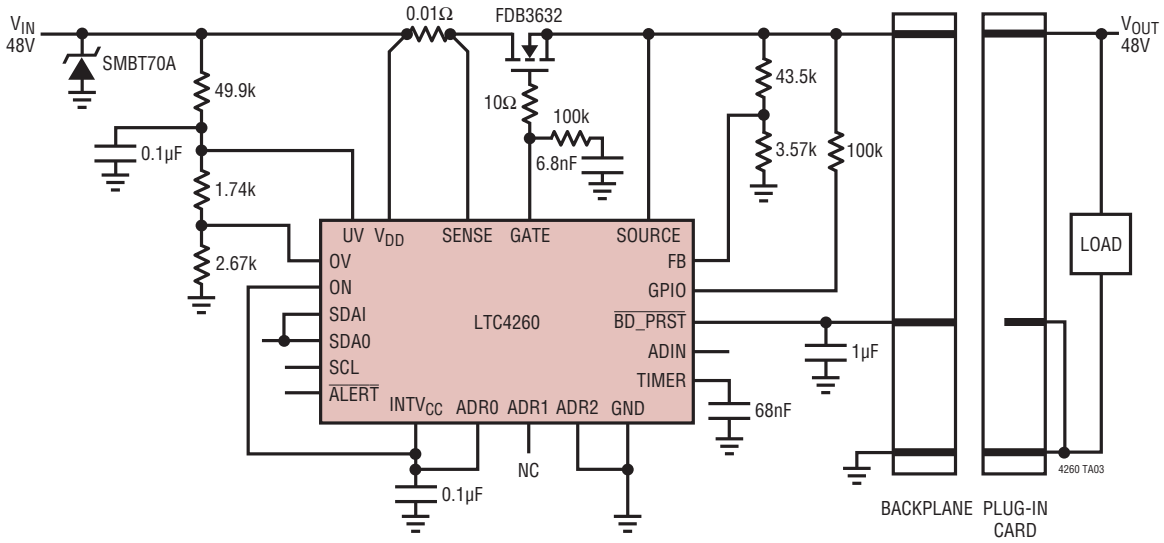
REV	DATE	DESCRIPTION	PAGE NUMBER
B	1/12	Revised Conditions and Min value for $I_{GATE(FST)}$	3
		Corrected typographical error in Layout Considerations section	17
C	5/13	Removed erroneous temperature dot from $\Delta V_{GPIO(TH)}$	3
		Corrected Full Scale Voltage of SOURCE to 102V	4
		Corrected I_{LOAD} to I_{GPIO} in G13	7
		Illustrated a 16.5V clamp between GATE and SOURCE pins	10
		Data Converter Section: Added a sentence describing noise averaging benefit of $\Delta\Sigma$ architecture	15
		Added SMBT70A clamp to V_{IN} line in Figure 13	25
		Changed SMAT70B to SMBT70A in the Typical Application	30

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

3A, 48V Backplane Resident Application with Insertion Activated Turn-On



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1641-1/LT1641-2	Positive High Voltage Hot Swap Controllers	Active Current Limiting, Supplies from 9V to 80V
LTC1921	Dual –48V Supply and Fuse Monitor	Withstands ±200V, Monitors Under-/Overvoltage and External Fuses
LTC2436	16-Bit, 2-Channel Delta-Sigma ADC	800nV$_{RMS}$ Noise, Two Differential Channels with Automatic Channel Selection
LTC4215	Hot Swap Controller with I^{2}C Compatible Monitoring	2.9V to 15V Supplies, 8-Bit ADC, I^{2}C/SMBus Interface
LTC4240	CompactPCI Hot Swap Controller with I^{2}C I/O	3.3V, 5V and ±12V Supplies, Control and Status over I^{2}C
LT4250	–48V Hot Swap Controller in SO-8	Active Current Limiting, Supplies from –20V to –80V
LTC4252	–48V Hot Swap Controller in MSOP	Fast Active Current Limiting with Drain Accelerated Response, Supplies from –15V
LT4256	Positive 48V Hot Swap Controller with Open-Circuit Detect	Foldback Current Limiting, Open-Circuit and Overcurrent Fault Output, Up to 80V Supply
LTC4300A	Hot Swappable 2-Wire Bus Buffer	Provides Capacitive Buffering, SDA and SCL Precharge and Level Shifting
LTC4301	Supply Independent Hot Swappable 2-Wire Bus Buffer	Provides Capacitive Buffering, SDA and SCL Precharge and Level Shifting
LTC4302	Addressable 2-Wire Bus Buffer	Provides Capacitive Buffering, SDA and SCL Precharge and Level Shifting, Enabled by 2-Wire Bus Commands
LTC4354	Negative Voltage Diode-OR Controller	8-Pin DFN and SO Package
LTC4357	Positive High Voltage Ideal Diode Controller	N-Channel, 9V to 80V, MSOP-8 and DFN-6 Packages

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