THE DATASHEET OF

LTC2274IUJ#TRPBF

16-Bit, 105Msps Serial Output ADC

FEATURES

- **High Speed Serial Interface (JESD204)**
- **Sample Rate: 105Msps**
- **77.7dBFS Noise Floor**
- **100dB SFDR**
- **SFDR >82dB at 250MHz (1.5V$_{P-P}$ Input Range)**
- **PGA Front End (2.25V$_{P-P}$ or 1.5V$_{P-P}$ Input Range)**
- **700MHz Full Power Bandwidth S/H**
- **Optional Internal Dither**
- Single 3.3V Supply
- Power Dissipation: 1300mW
- Clock Duty Cycle Stabilizer
- Pin Compatible Family
  - 105Msps: LTC2274
  - 80Msps: LTC2273
  - 65Msps: LTC2272
- 40-Pin 6mm × 6mm QFN Package

APPLICATIONS

- Telecommunications
- Receivers
- Cellular Base Stations
- Spectrum Analysis
- Imaging Systems
- ATE

DESCRIPTION

The LTC®2274 is a 105Msps, 16-bit A/D converter with a high speed serial interface. It is designed for digitizing high frequency, wide dynamic range signals with an input bandwidth of 700MHz. The input range of the ADC can be optimized using the PGA front end. The output data is serialized according to the JEDEC Serial Interface for Data Converters specification (JESD204).

The LTC2274 is perfect for demanding applications where it is desirable to isolate the sensitive analog circuits from the noisy digital logic. The AC performance includes a 77.7dB Noise Floor and 100dB spurious free dynamic range (SFDR). Ultra low internal jitter of 80fs RMS allows undersampling of high input frequencies with excellent noise performance. Maximum DC specs include ±4.5LSB INL and ±1LSB DNL (no missing codes) over temperature.

The encode clock inputs, ENC$^+$ and ENC$^-$, may be driven differentially or single-ended with a sine wave, PECL, LVDS, TTL or CMOS inputs. A clock duty cycle stabilizer allows high performance at full speed with a wide range of clock duty cycles.

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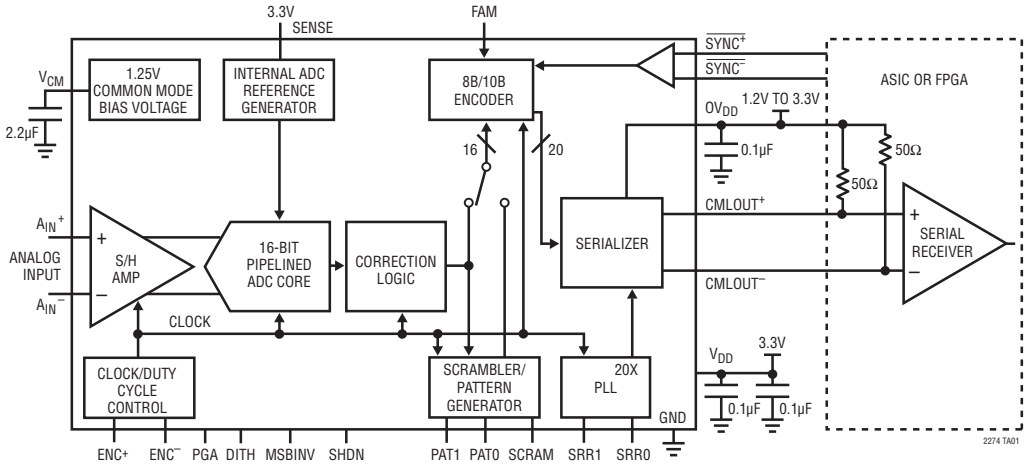
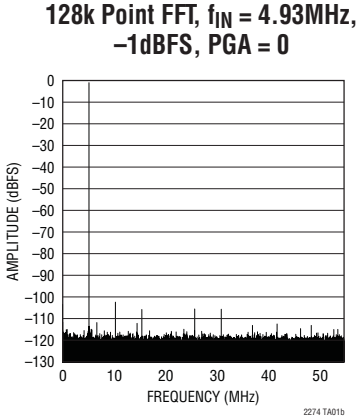
TYPICAL APPLICATION



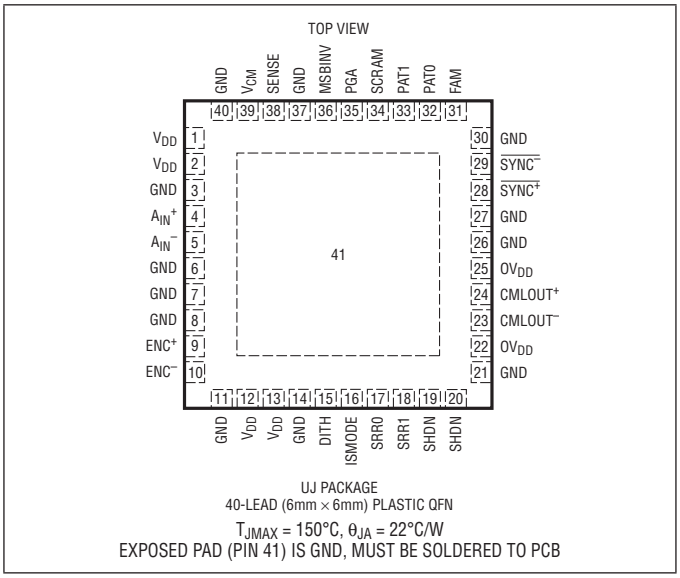


ABSOLUTE MAXIMUM RATINGS

OV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) ..... –0.3V to 4V
Analog Input Voltage (Note 3).....–0.3V to (V_{DD} + 0.3V)
Digital Input Voltage.....–0.3V to (V_{DD} + 0.3V)
Digital Output Voltage ..... –0.3V to (OV_{DD} + 0.3V)
Power Dissipation 2000mW
Operating Temperature Range
LTC2274C ..... 0°C to 70°C
LTC2274I..... –40°C to 85°C
Storage Temperature Range..... –65°C to 150°C
Digital Output Supply Voltage (OV_{DD}) ..... –0.3V to 4V

PIN CONFIGURATION



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 22°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2274CUJ#PBF	LTC2274CUJ#TRPBF	LTC2274UJ	40-Lead (6mm × 6mm) Plastic QFN	0°C to 70°C
LTC2274IUJ#PBF	LTC2274IUJ#TRPBF	LTC2274UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC2274CUJ	LTC2274CUJ#TR	LTC2274UJ	40-Lead (6mm × 6mm) Plastic QFN	0°C to 70°C
LTC2274IUJ	LTC2274IUJ#TR	LTC2274UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Integral Linearity Error	Differential Analog Input (Note 5) T_A = 25°C			±1.2	±4	LSB
Integral Linearity Error	Differential Analog Input (Note 5)	●		±1.5	±4.5	LSB
Differential Linearity Error	Differential Analog Input	●		±0.3	±1	LSB
Offset Error	(Note 6)	●		±1	±8.5	mV
Offset Drift				±10		µV/°C
Gain Error	External Reference	●		±0.2	±1.5	%FS
Full-Scale Drift	Internal Reference External Reference			±30 ±15		ppm/°C ppm/°C
Transition Noise				3		LSB_{RMS}

ANALOG INPUT

The ● denotes denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ - A_{IN}^-$)	3.135V ≤ V_{DD} ≤ 3.465V	●		1.5 or 2.25		V_{P-P}
$V_{IN, CM}$	Analog Input Common Mode	Differential Input (Note 7)	●	1	1.25	1.5	V
I_{IN}	Analog Input Leakage Current	0V ≤ A_{IN}^+, A_{IN}^- ≤ V_{DD} (Note 10)	●	–1		1	µA
I_{SENSE}	SENSE Input Leakage Current	0V ≤ SENSE ≤ V_{DD} (Note 11)		–3		3	µA
C_{IN}	Analog Input Capacitance	Sample Mode $ENC^+ < ENC^-$ Hold Mode $ENC^+ > ENC^-$			6.7 1.8		pF pF
t_{AP}	Sample-and-Hold Acquisition Delay Time				1		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Time Jitter				80		fs_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	1V < ($A_{IN}^+ = A_{IN}^-$) <1.5V			80		dB
BW-3dB	Full Power Bandwidth	R_S ≤ 25Ω			700		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	5MHz Input (2.25V Range, PGA = 0) 5MHz Input (1.5V Range, PGA = 1)			77.6 75.4		dBFS dBFS
		15MHz Input (2.25V Range, PGA = 0), T_A = 25°C 15MHz Input (2.25V Range, PGA = 0) 15MHz Input (1.5V Range, PGA = 1)	 ● 	76.5 76.2	77.5 77.2 75.3		dBFS dBFS dBFS
		70MHz Input (2.25V Range, PGA = 0) 70MHz Input (1.5V Range, PGA = 1)			77.2 75.1		dBFS dBFS
		140MHz Input (2.25V Range, PGA = 0) 140MHz Input (1.5V Range, PGA = 1), T_A = 25°C 140MHz Input (1.5V Range, PGA = 1)	 ●	 73.8 73.4	76.3 74.5 74.2		dBFS dBFS dBFS
		170MHz Input (2.25V Range, PGA = 0) 170MHz Input (1.5V Range, PGA = 1)			75.9 74.3		dBFS dBFS
SFDR	Spurious Free Dynamic Range 2^{nd} or 3^{rd} Harmonic	5MHz Input (2.25V Range, PGA = 0) 5MHz Input (1.5V Range, PGA = 1)			100 100		dBc dBc
		15MHz Input (2.25V Range, PGA = 0), T_A = 25°C 15MHz Input (2.25V Range, PGA = 0) 15MHz Input (1.5V Range, PGA = 1)	 ● 	85 84	95 95 100		dBc dBc dBc
		70MHz Input (2.25V Range, PGA = 0) 70MHz Input (1.5V Range, PGA = 1)			86 94		dBc dBc
		140MHz Input (2.25V Range, PGA = 0) 140MHz Input (1.5V Range, PGA = 1), T_A = 25°C 140MHz Input (1.5V Range, PGA = 1)	 ●	 81 80	85 90 89		dBc dBc dBc
		170MHz Input (2.25V Range, PGA = 0) 170MHz Input (1.5V Range, PGA = 1)			80 85		dBc dBc

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SFDR	Spurious Free Dynamic Range 4th Harmonic or Higher	5MHz Input (2.25V Range, PGA = 0) 5MHz Input (1.5V Range, PGA = 1)			100 100		dBc dBc
		15MHz Input (2.25V Range, PGA = 0) 15MHz Input (1.5V Range, PGA = 1)	● ●	90	100 100		dBc dBc
		70MHz Input (2.25V Range, PGA = 0) 70MHz Input (1.5V Range, PGA = 1)			100 100		dBc dBc
		140MHz Input (2.25V Range, PGA = 0) 140MHz Input (1.5V Range, PGA = 1)	 ●	 85	95 100		dBc dBc
		170MHz Input (2.25V Range, PGA = 0) 170MHz Input (1.5V Range, PGA = 1)			90 95		dBc dBc
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input (2.25V Range, PGA = 0) 5MHz Input (1.5V Range, PGA = 1)			77.5 75.3		dBFS dBFS
		15MHz Input (2.25V Range, PGA = 0), T_A = 25°C 15MHz Input (2.25V Range, PGA = 0 15MHz Input (1.5V Range, PGA = 1)	 ● 	76.3 75.9 	77.4 77 75.2		dBFS dBFS dBFS
		70MHz Input (2.25V Range, PGA = 0) 70MHz Input (1.5V Range, PGA = 1)			76.7 74.2		dBFS dBFS
		140MHz Input (2.25V Range, PGA = 0), T_A = 25°C 140MHz Input (1.5V Range, PGA = 1) 140MHz Input (1.5V Range, PGA = 1)	 ●	 73.6 73.2	75.3 74.3 74		dBFS dBFS dBFS
		170MHz Input (2.25V Range, PGA = 0) 170MHz Input (1.5V Range, PGA = 1)			73.4 73.4		dBFS dBFS
SFDR	Spurious Free Dynamic Range at –25dBFS Dither “OFF”	5MHz Input (2.25V Range, PGA = 0) 5MHz Input (1.5V Range, PGA = 1)			105 105		dBFS dBFS
		15MHz Input (2.25V Range, PGA = 0) 15MHz Input (1.5V Range, PGA = 1)			105 105		dBFS dBFS
		70MHz Input (2.25V Range, PGA = 0) 70MHz Input (1.5V Range, PGA = 1)			105 105		dBFS dBFS
		140MHz Input (2.25V Range, PGA = 0) 140MHz Input (1.5V Range, PGA = 1)			100 100		dBFS dBFS
		170MHz Input (2.25V Range, PGA = 0) 170MHz Input (1.5V Range, PGA = 1)			100 100		dBFS dBFS
SFDR	Spurious Free Dynamic Range at –25dBFS Dither “ON”	5MHz Input (2.25V Range, PGA = 0) 5MHz Input (1.5V Range, PGA = 1)			115 115		dBFS dBFS
		15MHz Input (2.25V Range, PGA = 0) 15MHz Input (1.5V Range, PGA = 1)	● 	97 	115 115		dBFS dBFS
		70MHz Input (2.25V Range, PGA = 0) 70MHz Input (1.5V Range, PGA = 1)			115 115		dBFS dBFS
		140MHz Input (2.25V Range, PGA = 0) 140MHz Input (1.5V Range, PGA = 1)			110 110		dBFS dBFS
		170MHz Input (2.25V Range, PGA = 0) 170MHz Input (1.5V Range, PGA = 1)			105 105		dBFS dBFS

COMMON MODE BIAS CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0		1.15	1.25	1.35	V
V_{CM} Output Tempco	I_{OUT} = 0	●		40		ppm/°C
V_{CM} Line Regulation	3.135V ≤ V_{DD} ≤ 3.465V	●		1		mV/V
V_{CM} Output Resistance	–1mA ≤ | I_{OUT} | ≤ 1mA	●		2		Ω

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Encode Inputs (ENC+, ENC–)							
V_{ID}	Differential Input Voltage	(Note 7)	●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 7)		 1.4	1.6	 3.0	V
R_{IN}	Input Resistance	(See Figure 2)			6		kΩ
C_{IN}	Input Capacitance				3		pF
$\overline{SYNC}$ Inputs ($\overline{SYNC}^+$, $\overline{SYNC}^-$)							
V_{SID}	$\overline{SYNC}$ Differential Input Voltage	(Note 7)	●	0.2			V
V_{SICM}	$\overline{SYNC}$ Common Mode Input Voltage	Internally Set Externally Set (Note 7)		 1.1	1.6	 2.2	V
R_{SIN}	$\overline{SYNC}$ Input Resistance				16.5		kΩ
C_{SIN}	$\overline{SYNC}$ Input Capacitance				3		pF
Logic Inputs (DITH, PGA, MSBINV, SCRAM, FAM, SHDN, SRR1, SRR0, ISMODE, PAT1, PAT0)							
V_{IH}	High Level Input Voltage	V_{DD} = 3.3V	●	2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 3.3V	●			0.8	V
I_{IN}	Input Current	V_{IN} = 0V to V_{DD}	●			±20	µA
C_{IN}	Input Capacitance				1.5		pF
High-Speed Serial Outputs (CMLOUT+, CMLOUT–)							
V_{OH}	Output High Level	Directly-Coupled 50Ω to OV_{DD} Directly-Coupled 100Ω Differential AC-Coupled			OV_{DD} OV_{DD} – 0.2 OV_{DD} – 0.2		V V V
V_{OL}	Output Low Level	Directly-Coupled 50Ω to OV_{DD} Directly-Coupled 100Ω Differential AC-Coupled			OV_{DD} – 0.4 OV_{DD} – 0.6 OV_{DD} – 0.6		V V V
V_{OCM}	Output Common Mode Voltage	Directly-Coupled 50Ω to OV_{DD} Directly-Coupled 100Ω Differential AC-Coupled			OV_{DD} – 0.2 OV_{DD} – 0.4 OV_{DD} – 0.4		V V V
R_{OUT}	Output Resistance	Single-Ended Differential	●	35	50 100	65	Ω Ω

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Analog Supply Voltage		●	3.135	3.3	3.465	V
P_{SHDN}	Shutdown Power	SHDN Pins = V_{DD}			5		mW
OV_{DD}	Output Supply Range	CMLOUT Directly-Coupled 50Ω to OV_{DD} (Note 7) CMLOUT Directly-Coupled 100Ω Differential (Note 7) CMLOUT AC-Coupled (Note 7)	● ● ●	1.2 1.4 1.4		V_{DD} V_{DD} V_{DD}	V V V
I_{VDD}	Analog Supply Current	DC Input	●		394	450	mA
I_{OVDD}	Output Supply Current	CMLOUT Directly-Coupled, 50Ω to $0V_{DD}$ CMLOUT Directly-Coupled 100Ω Differential CMLOUT AC-Coupled			8 16 16		mA mA mA
P_{DIS}	Power Dissipation	DC Input	●		1300	1485	mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency	(Note 9)	●	20		105	MHz
t_{CONV}	Conversion Period				$1/f_S$		s
t_L	ENC Clock Low Time	(Note 7)	●	3.1	4.762	25	ns
t_H	ENC Clock High Time	(Note 7)	●	3.1	4.762	25	ns
t_{AP}	Sample-and-Hold Aperture Delay				0.7		ns
t_{BIT}, UI	Period of a Serial Bit				$t_{CONV}/20$		s
t_{JIT}	Total Jitter of CMLOUT± (P-P)	BER = 1E–12 (Note 7)	●			0.35	UI
t_R, t_F	Differential Rise and Fall Time of CMLOUT± (20% to 80%)	R_{TERM} = 50Ω, C_L = 2pF (Note 7)	●	50	110		ps
t_{SU}	$\overline{SYNC}$ to ENC Clock Setup Time	(Note 7)	●	2			ns
t_{HD}	ENC Clock to $\overline{SYNC}$ Hold Time	(Note 7)	●	2.5			ns
t_{CS}	ENC Clock to $\overline{SYNC}$ Delay	(Note 7)	●	t_{HD}		$t_{CONV} – t_{SU}$	ns
LAT_P	Pipeline Latency				9		Cycles
LAT_{SC}	Latency from $\overline{SYNC}$ Active to COMMA Out				3		Cycles
LAT_{SD}	Latency from $\overline{SYNC}$ Release to DATA Out				2		Cycles

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: V_{DD} = 3.3V, f_{SAMPLE} = 105MHz differential $ENC^+/ENC^–$ = $2V_{P-P}$ sine wave with 1.6V common mode, input range = $2.25V_{P-P}$ with differential drive (PGA = 0), unless otherwise specified.

Note 5: Integral nonlinearity is defined as the deviation of a code from a "best fit straight line" to the transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Offset error is the offset voltage measured from –1/2LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111 in 2's complement output mode.

Note 7: Guaranteed by design, not subject to test.

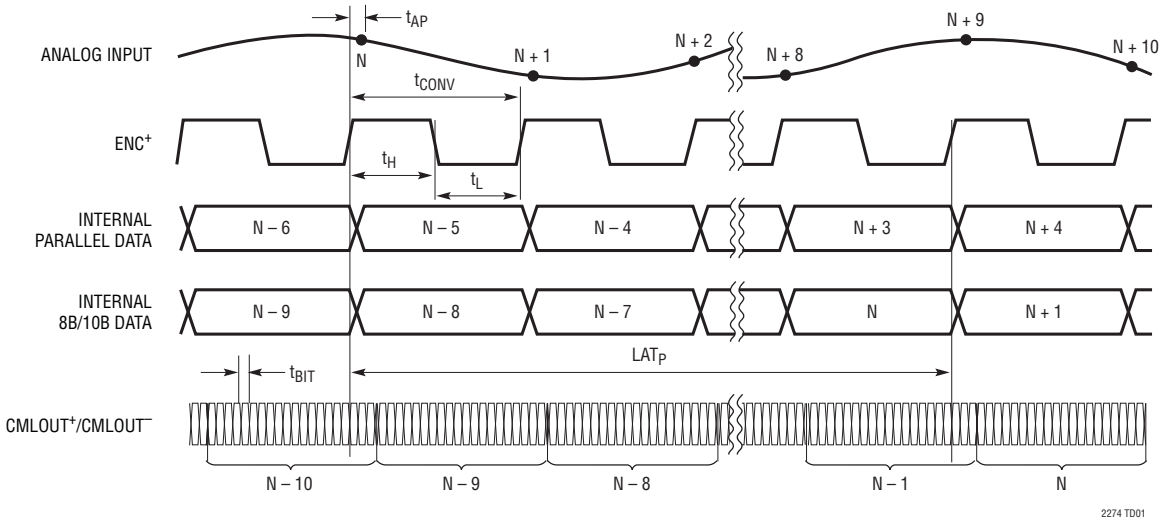
Note 8: V_{DD} = 3.3V, f_{SAMPLE} = 105MHz input range = $2.25V_{P-P}$ with differential drive.

Note 9: Recommended operating conditions.

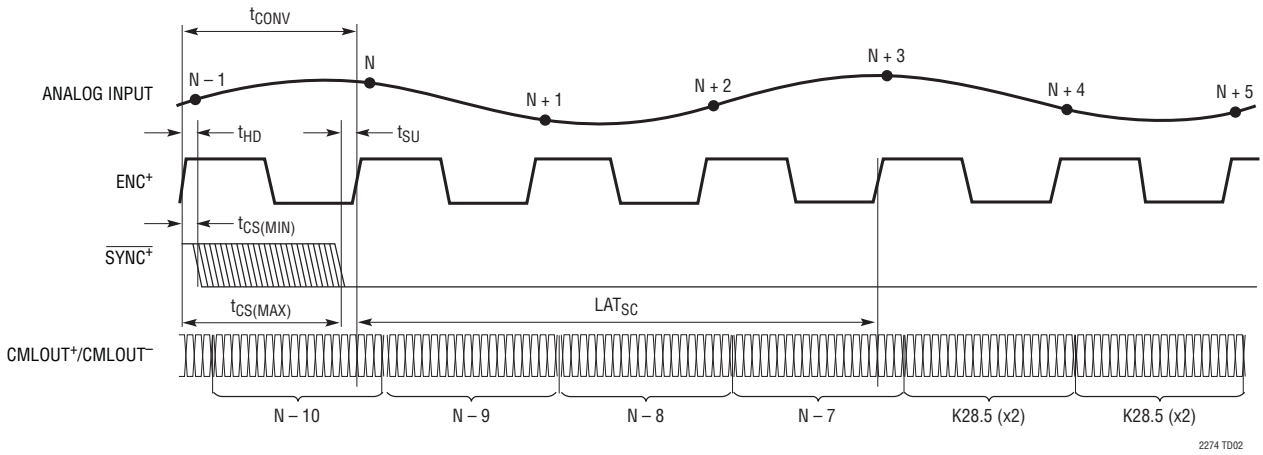
Note 10: The dynamic current of the switched capacitors analog inputs can be large compared to the leakage current and will vary with the sample rate.

Note 11: Leakage current will have higher transient current at power up. Keep drive resistance at or below 1k.

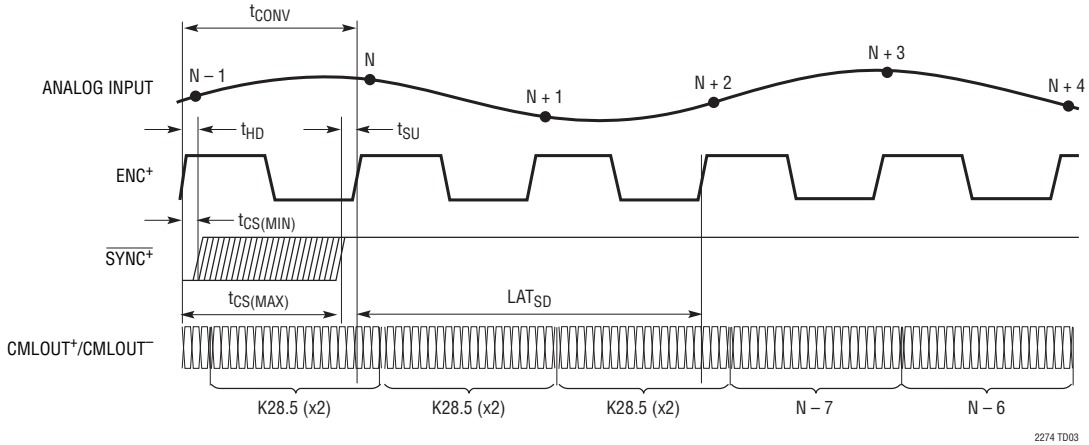
TIMING DIAGRAMS



Analog Input to Serial Data Out Timing



$\overline{\text{SYNC}}^+$ Falling Edge to Comma (K28.5) Timing

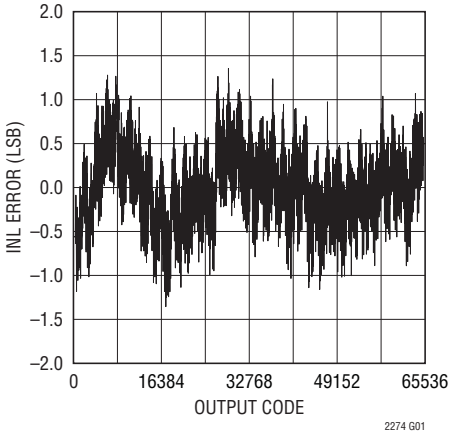


$\overline{\text{SYNC}}^+$ Rising Edge to Data Timing

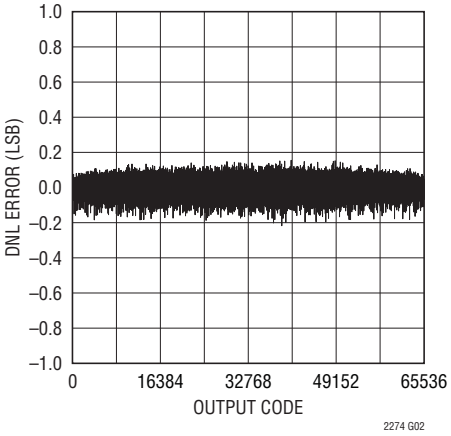
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3.3V, OV_{DD} = 1.5V, T_A = 25°C, F_S = 105Msps, unless otherwise noted.

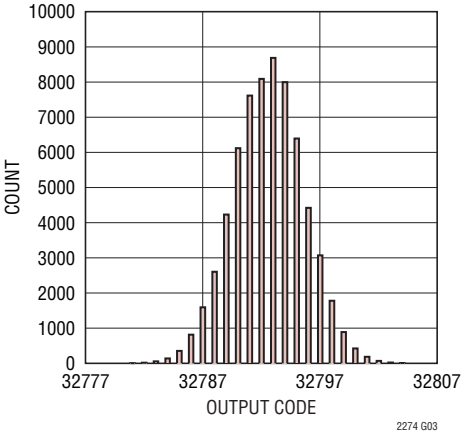
Integral Non-Linearity (INL) vs Output Code



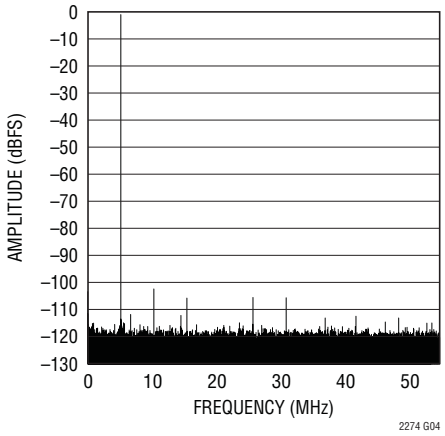
Differential Non-Linearity (DNL) vs Output Code



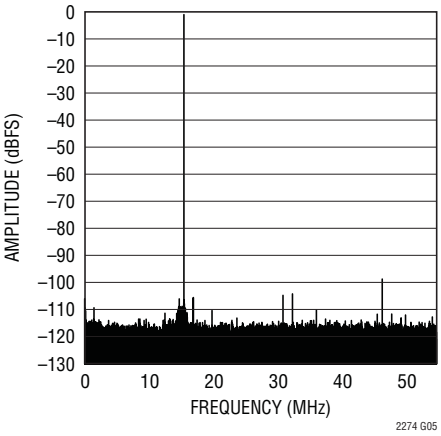
AC Grounded Input Histogram



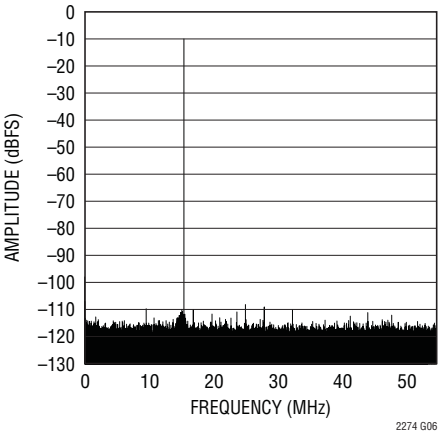
128k Point FFT, f_{IN} = 4.93MHz, –1dBFS, PGA = 0



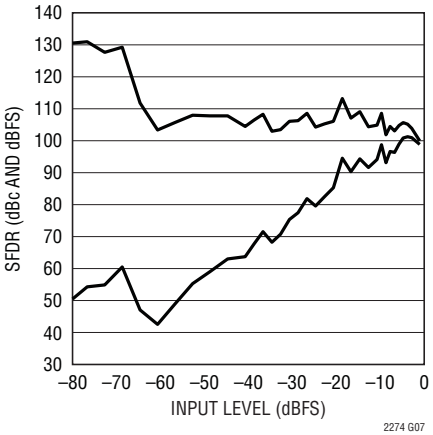
64k Point FFT, f_{IN} = 14.8MHz, –1dBFS, PGA = 0



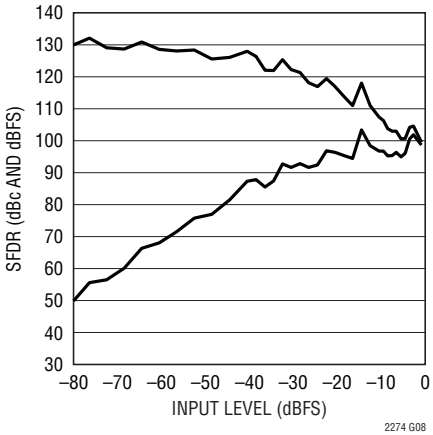
64k Point FFT, f_{IN} = 14.8MHz, –10dBFS, PGA = 0



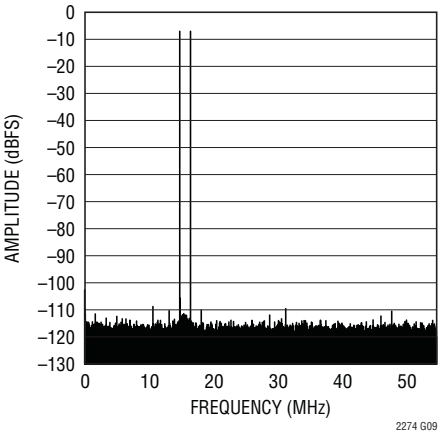
SFDR vs Input Level, f_{IN} = 15MHz, PGA = 0, Dither "Off"



SFDR vs Input Level, f_{IN} = 15MHz, PGA = 0, Dither "On"



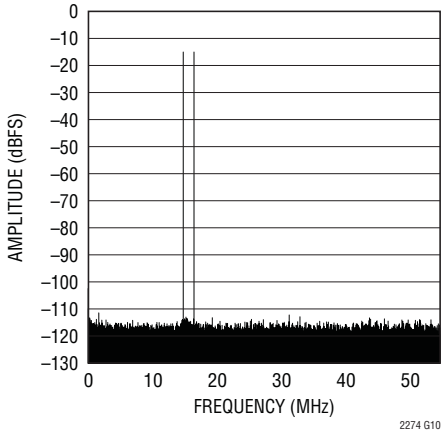
64k Point 2-Tone FFT, f_{IN} = 14.2MHz and 15.8MHz, –7dBFS, PGA = 0



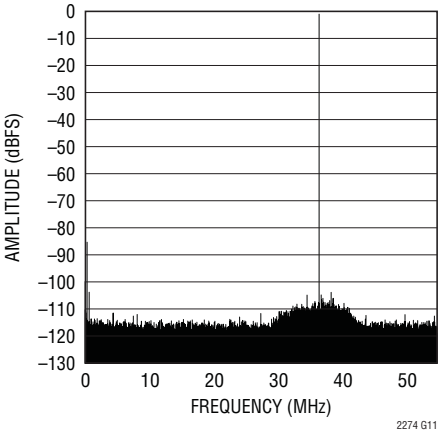
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3.3V, OV_{DD} = 1.5V, T_A = 25°C, F_S = 105Msps, unless otherwise noted.

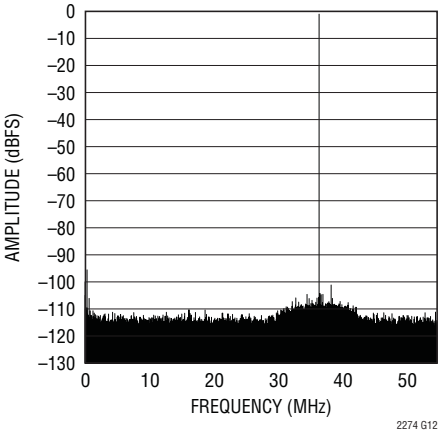
64k Point 2-Tone FFT, f_{IN} = 14.2MHz and 15.8MHz, –15dBFS, PGA = 0



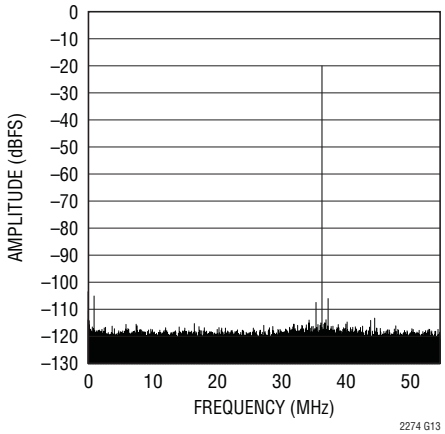
64k FFT, f_{IN} = 70.1MHz, –1dBFS, PGA = 0



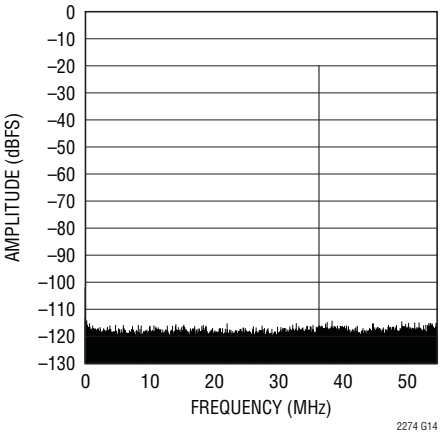
64k FFT, f_{IN} = 70.1MHz, –1dBFS, PGA = 1



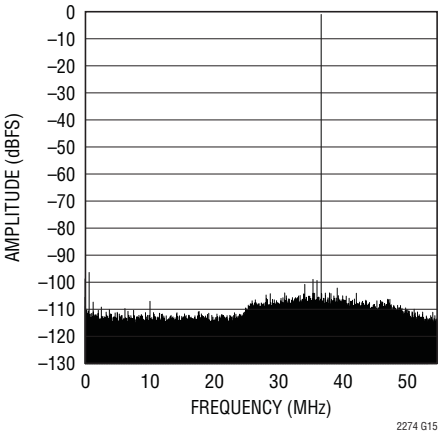
128k Point FFT, f_{IN} = 70.1MHz, –20dBFS, PGA = 0, Dither "Off"



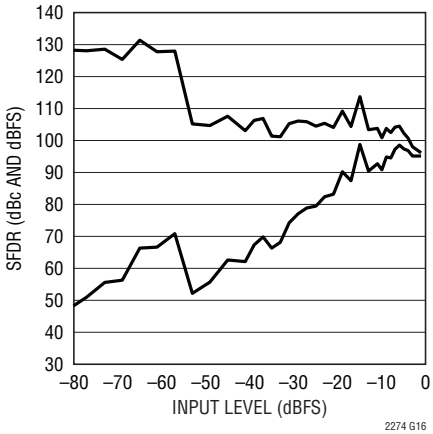
128k Point FFT, f_{IN} = 70.1MHz, –20dBFS, PGA = 0, Dither "On"



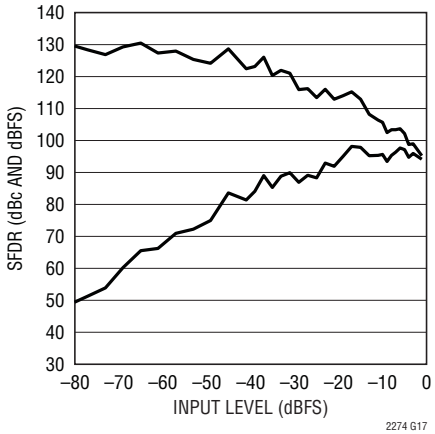
64k Point FFT, f_{IN} = 140.2MHz, –1dBFS, PGA = 1



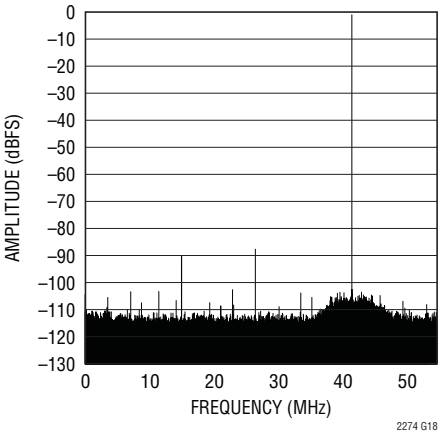
SFDR vs Input Level, f_{IN} = 140MHz, PGA = 1, Dither "Off"



SFDR vs Input Level, f_{IN} = 140MHz, PGA = 1, Dither "On"



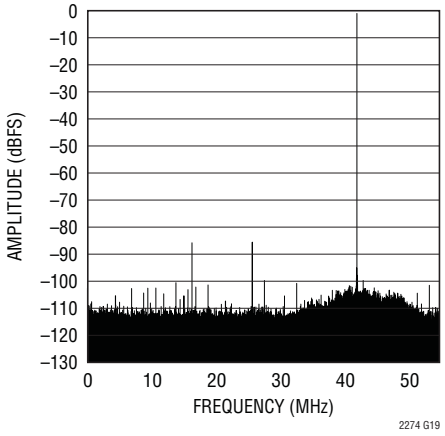
64k Point FFT, f_{IN} = 170.2MHz, –1dBFS, PGA = 1



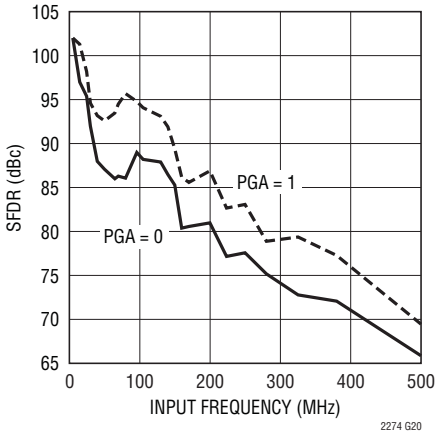
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3.3V, OV_{DD} = 1.5V, T_A = 25°C, F_S = 105Msps, unless otherwise noted.

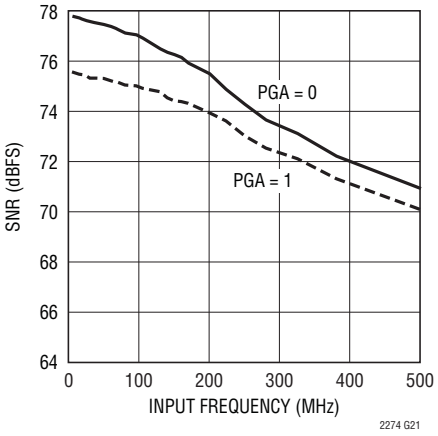
64k Point FFT, f_{IN} = 250.2MHz, –1dBFS, PGA = 1



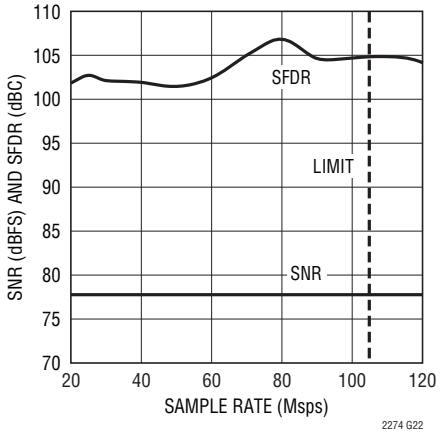
SFDR (HD2 and HD3) vs Input Frequency



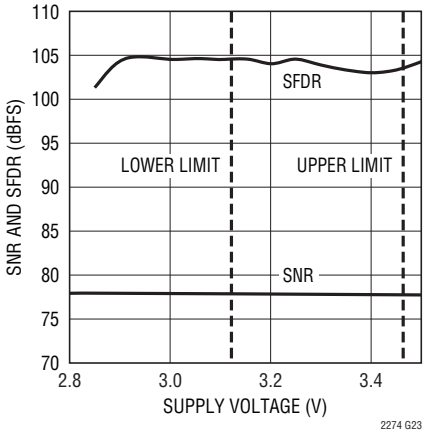
SNR vs Input Frequency



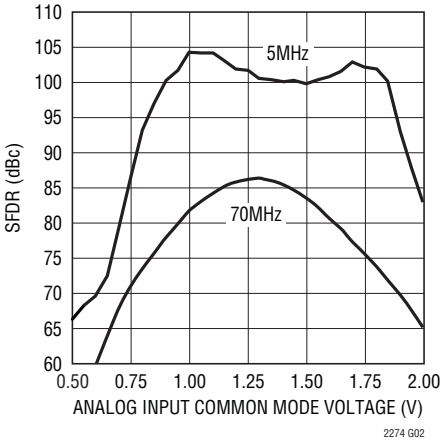
SNR and SFDR vs Sample Rate, f_{IN} = 5.1MHz



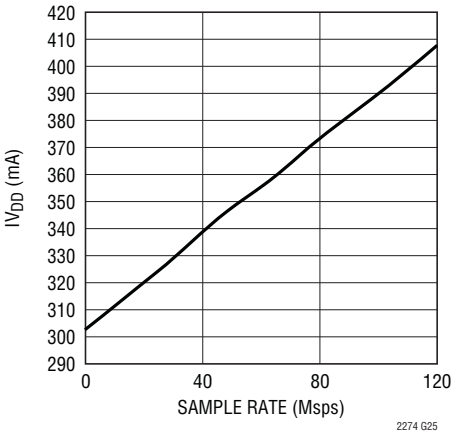
SNR and SFDR vs Supply Voltage (V_{DD}), f_{IN} = 5.2MHz



SFDR vs Analog Input Common Mode Voltage, 5MHz and 70MHz, –1dBFS



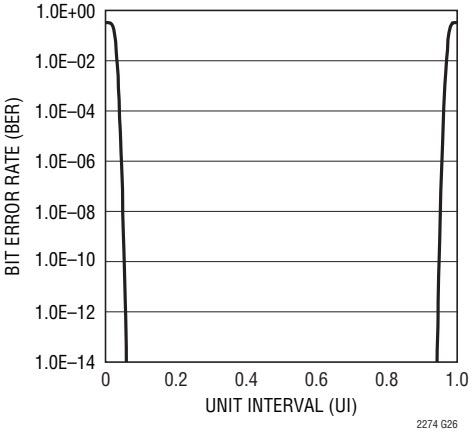
IV_{DD} vs Sample Rate, 5MHz Sine, –1dBFS



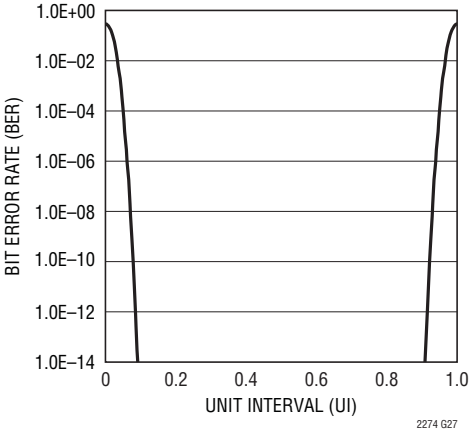
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3.3V, OV_{DD} = 1.5V, T_A = 25°C, F_S = 105Msps, unless otherwise noted.

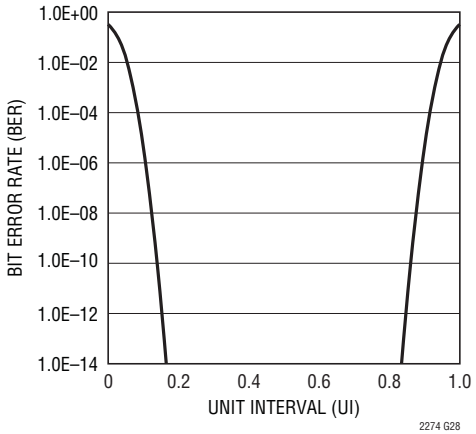
CMLOUT Dual-Dirac BER Bathtub Curve, 400Mbps



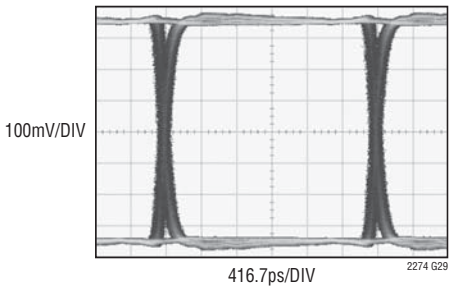
CMLOUT Dual-Dirac BER Bathtub Curve, 1.2Gbps



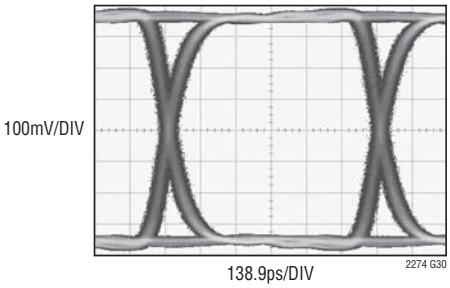
CMLOUT Dual-Dirac BER Bathtub Curve, 2.1Gbps



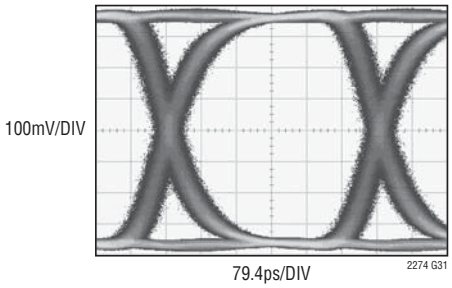
CMLOUT Eye Diagram 400Mbps



CMLOUT Eye Diagram 1.2Gbps



CMLOUT Eye Diagram 2.1Gbps



PIN FUNCTIONS

V_{DD} (Pins 1, 2, 12, 13): Analog 3.3V Supply. Bypass to GND with 0.1µF ceramic chip capacitors.

GND (Pins 3, 6, 7, 8, 11, 14, 21, 26, 27, 30, 37, 40): ADC Power Ground.

A_{IN}^+ (Pin 4): Positive Differential Analog Input.

A_{IN}^- (Pin 5): Negative Differential Analog Input.

ENC^+ (Pin 9): Positive Differential Encode Input. The sampled analog input is held on the rising edge of ENC^+. This pin is internally biased to 1.6V through a 6.2kΩ resistor. Output data can be latched on the falling edge of ENC^+.

ENC^- (Pin 10): Negative Differential Encode Input. The sampled analog input is held on the falling edge of ENC-. This pin is internally biased to 1.6V through a 6.2kΩ resistor. Bypass to ground with a 0.1uF capacitor for a single-ended Encode signal.

DITH (Pin 15): Internal Dither Enable Pin. DITH = low disables internal dither. DITH = high enables internal dither. Refer to Internal Dither section of this data sheet for details on dither operation.

ISMODE (Pin 16): Idle Synchronization mode. When ISMODE is not asserted, synchronization is performed with a series of COMMAS (K28.5). When ISMODE is asserted, a special Idle SYNC mode is enabled where synchronization is performed by sending a COMMA (K28.5) followed by the appropriate data code-group (D5.6 or D16.2) for establishing a negative running disparity for the first data code-group after synchronization.

SRR0 (Pin 17): Sample Rate Range Select Bit0. Used with the SRR1 pin to select the sample rate operating range.

SRR1 (Pin 18): Sample Rate Range Select Bit1. Used with the SRR0 pin to select the sample rate operating range.

SHDN (Pins 19, 20): Shutdown Pins. A high level on both pins will shut down the chip.

OV_{DD} (Pins 22, 25): Positive Supply for the Output Drivers. This supply range is 1.2V to V_{DD} for directly coupled CML outputs, or 1.4V to OV_{DD} for AC-coupled or differentially terminated CML outputs. Bypass to ground with 0.1µF ceramic chip capacitor.

$CMLOUT^-$ (Pin 23): Negative High-Speed CML Output.

$CMLOUT^+$ (Pin 24): Positive High-Speed CML Output.

$\overline{SYNC}^+$ (Pin 28): Sync Request Positive Input (Active Low for Compatibility with JESD204). A low level on this pin for at least two sample clock cycles will initiate frame synchronization.

$\overline{SYNC}^-$ (Pin 29): Sync Request Negative Input. A high level on this pin for at least two sample clock cycles will initiate frame synchronization. For single-ended operation, bypass to ground with a 0.1µF capacitor and use $\overline{SYNC}^+$ as the $\overline{SYNC}$ point.

FAM (Pin 31): Frame Alignment Monitor Enable. A high level enables the substitution of predetermined data at the end of the frame with a K28.7 symbol for frame alignment monitoring.

PAT0 (Pin 32): Pattern Select Bit0. Use with PAT1 to select a test pattern for the serial interface.

PAT1 (Pin 33): Pattern Select Bit1. Use with PAT0 to select a test pattern for the serial interface.

SCRAM (Pin 34): Enable Data Scrambling. A high level on this pin will apply the polynomial $1 + x^{14} + x^{15}$ in scrambling each ADC data sample. The scrambling takes place before the 8B/10B encoding.

PGA (Pin 35): Programmable Gain Amplifier Control Pin. Low selects a front-end gain of 1, input range of $2.25V_{P-P}$. High selects a front-end gain of 1.5, input range of $1.5V_{P-P}$.

MSBINV (Pin 36): Invert the MSB. A high level will invert the MSB to enable the 2's complement format.

PIN FUNCTIONS

SENSE (Pin 38): Reference Mode Select and External Reference Input. Tie SENSE to V_{DD} to select the internal 2.5V bandgap reference. An external reference of 2.5V or 1.25V may be used; both reference values will set a full scale ADC range of 2.25V (PGA = 0).

V_{CM} (Pin 39): 1.25V Output. Optimum voltage for input common mode. Must be bypassed to ground with a minimum of 2.2µF. Ceramic chip capacitors are recommended.

GND (Exposed Pad) (Pin 41): ADC Power Ground. The Exposed Pad on the bottom of the package needs to be soldered to ground.

BLOCK DIAGRAM

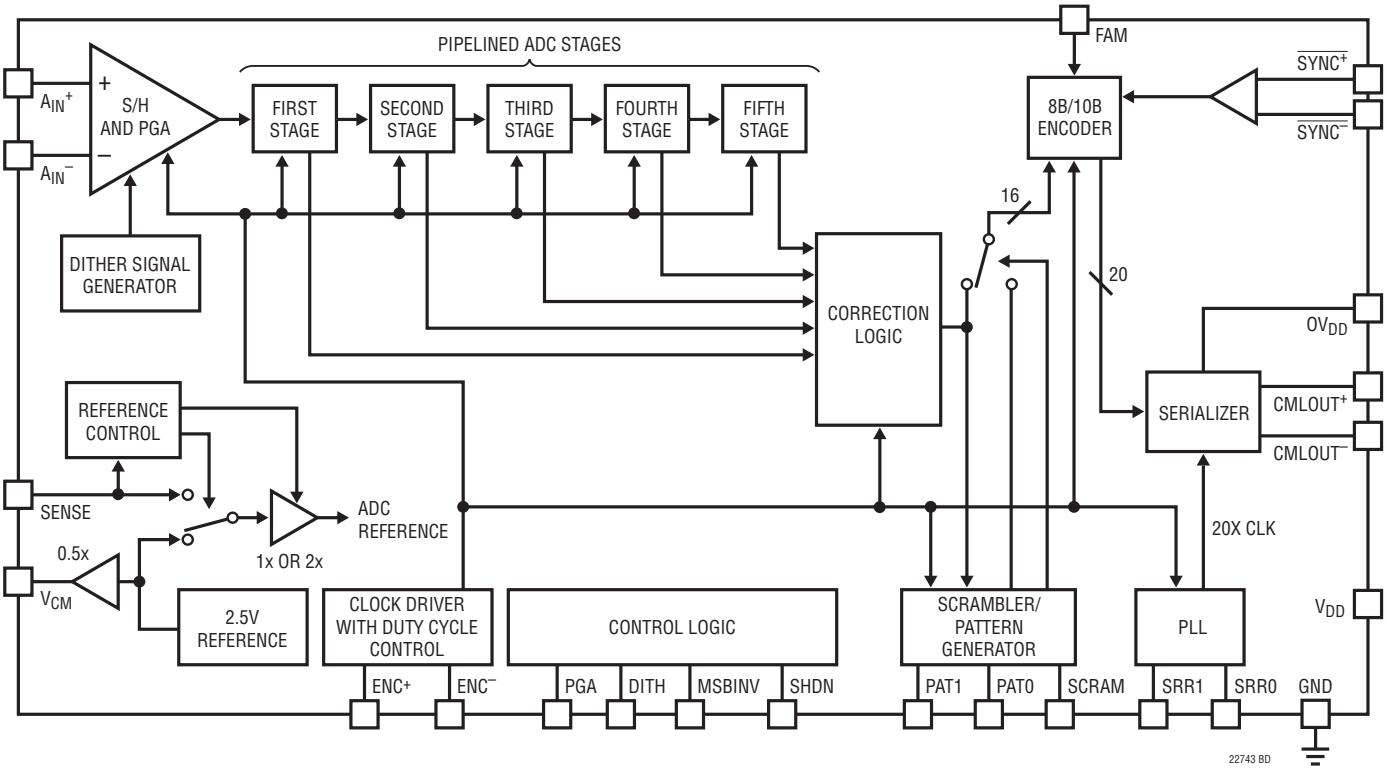


Figure 1. Functional Block Diagram

DEFINITIONS

DYNAMIC PERFORMANCE TERMS

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N+D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

Signal-to-Noise Ratio

The signal-to-noise (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components, except the first five harmonics.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = -20Log\ (\sqrt{(V_2^2 + V_3^2 + V_4^2 + ... V_N^2)}/V_1)$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through nth harmonics.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 3rd order IMD terms include (2fa + fb), (fa + 2fb), (2fa - fb) and (fa - 2fb). The 3rd order IMD is defined as the ratio of the RMS value of either input tone to the RMS value of the largest 3rd order IMD product.

Spurious Free Dynamic Range (SFDR)

The ratio of the RMS input signal amplitude to the RMS value of the peak spurious spectral component expressed in dBc. SFDR may also be calculated relative to full scale and expressed in dBFS.

Full Power Bandwidth

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

Aperture Delay Time

The time from when a rising ENC^+ equals the ENC^- voltage to the instant that the input signal is held by the sample-and-hold circuit.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20log\ (2\pi \bullet f_{IN} \bullet t_{JITTER})$$

SERIAL INTERFACE TERMS

8B/10B Encoding

A data encoding method designed to make an 8-bit data word (octet) more suitable for serial transmission. The resulting 10-bit word (code-group) has two fundamental strengths: 1) The receiver does not require a high-speed clock to capture the data. This is because the output code-groups are run-length limited, ensuring that there are enough transitions in the bit stream for the receiver to lock onto the data and recover the high-speed clock. 2) AC coupling is permitted because the code-groups are generated in a way that ensures the data stream is DC balanced (see Running Disparity).

A table of the 256 possible input octets with the resulting 10-bit code-groups is documented in IEEE Std 802.3-2002 part3 Table 36-1. The name associated with each of the 256 data code-groups is formatted Dx.y, with x ranging from 0 to 31 and y ranging from 0 to 7. Table 36-2 of

DEFINITIONS

the standard defines an additional set of 12 special code-groups for non-data characters such as commas. Special code-group names begin with K instead of D. A complete 8B/10B description is found in Clause 36.2 of IEEE Std 802.3-2002 part3.

Current Mode Logic (CML)

A technique used to implement differential high-speed logic. CML employs differential pairs (usually n-type) to steer current into resistive loads. It is possible to implement any logic function using CML. The output swing and offset is dependant on the bias current, the load resistance, and termination resistance.

This product family uses CML drivers to transmit high-speed serial data to the outside world. The output driver bias current is typically 16mA, generating a signal swing potential of $400mV_{P-P}$ ($800mV_{P-P}$ diff.) across the combined internal and external termination resistance of 25Ω on each output.

Code-Group

The 10-bit output from an 8B/10B encoder or the 10-bit input to the 8B/10B decoder.

Comma

A special 8B/10B code-group containing the binary sequence “0011111” or “1100000”. Commas are used for frame alignment and synchronization because a comma sequence cannot be generated by any combination of normal code-groups (unless a bit error occurs). There are three special code-groups that contain a comma, K28.1, K28.5, and K28.7.

For brevity, each of these three special code-groups are often called a comma, but in the strictest sense it is the first 7 bits of these code-groups that are designated a comma.

DC Balanced Signal

A specially conditioned signal that may be AC coupled with minimal degradation to the signal. DC balance is achieved when the average number of 1’s and 0’s are equal, eliminating the undesirable effects of DC wander on the receive side of the coupling capacitor. When 8B/10B coding is used, DC balance is achieved by following disparity rules (see Running Disparity).

De-Scrambler

A logic block that restores scrambled data to its pre-scrambled state. A self aligning de-scrambler is based on the same pseudo random bit sequence as the scrambler, so it requires no alignment signals. In this product family the scrambler is based on the $1 + x^{14} + x^{15}$ polynomial, and the self aligning process results in an initial loss of one ADC sample.

Frame

A group of octets or code-groups that make up one complete word. For this product family, a frame consists of two complete octets or code-groups, and constitutes one ADC sample.

Frame Alignment Monitoring (FAM)

After initial frame synchronization has been established, frame alignment monitoring enables the receiver to verify that code-group alignment is maintained without the loss of data. This is done by substituting a K28.7 comma for the last code-group of the frame when certain conditions are met. The receiver uses this comma as a position marker within the frame for alignment verification. After decoding the data, the receiver replaces the K28.7 comma with the original data.

Idle Frame Synchronization Mode (ISMODE)

A special synchronization mode where idle ordered sets are used to establish initial frame synchronization instead of K28.5 commas.

An Idle Ordered Set is defined in the IEEE Std 802.3-2002 part3, Clause 36.2.4.12. In general, it is a K28.5 comma followed by either a D5.6 or a D16.2. If the running disparity after the transmission of the K28.5 comma is positive,

DEFINITIONS

a D16.2 will be transmitted after the comma, otherwise a D5.6 will be transmitted. The result is that the ending disparity of an idle ordered set will always be negative.

Initial Frame Synchronization

The process of communicating frame synchronization information to the receiver upon the request of the receiver. For JESD204 compliance, K28.5 commas are transmitted as the preamble. Once the preamble has been detected the receiver terminates the synchronization request, and the preamble transmission continues until the end of the frame. The receiver designates the first normal data word after the preamble to be the start of the data frame.

Octet

The 8-bit input to an 8B/10B encoder, or the 8-bit output from an 8B/10B decoder.

Run-Length Limited (RLL)

The act of limiting the number of consecutive 1's or 0's in a data stream by encoding the data prior to serial transmission.

This process guarantees that there will be an adequate number of transitions in the serial data for the receiver to lock onto with a phase-locked loop and recover the high-speed clock.

Running Disparity

In order to maintain DC balance there are two possible 8B/10B output code-groups for each input octet. The running disparity is calculated to determine which of the two code-groups should be transmitted to maintain DC balance.

The disparity of a code-group is analyzed in two segments called sub-blocks. Sub-block1 consists of the first six bits of a code-group and sub-block2 consists of the last four bits of a code-group. When a sub-block is more heavily weighted with 1's the running disparity is positive, and when it is more heavily weighted with 0's the running disparity is negative. When the number of 1's and 0's are equal in a sub-block, the running disparity remains unchanged.

The polarity of the current running disparity determines which code-group should be transmitted to maintain DC balance. For a complete description of disparity rules, refer to IEEE Std 802.3-2002 part3, Clause 36.2.4.4.

Pseudo Random Bit Sequence (PRBS)

A data sequence having a random nature over a finite interval. The most commonly used PRBS test patterns may be described by a polynomial in the form of $1 + x^m + x^n$ and have a random nature for the length of up to $2^n - 1$ bits, where n indicates the order of the PRBS polynomial and m plays a role in maximizing the length of the random sequence.

Scrambler

A logic block that applies a pseudo random bit sequence to the input octets to minimize the tonal content of the high-speed serial bit stream.

APPLICATIONS INFORMATION

CONVERTER OPERATION

The core of the LTC2274 is a CMOS pipelined multi-step converter with a front-end PGA. As shown in Figure 1, the converter has five pipelined ADC stages. A sampled analog input will result in a digitized value nine clock cycles later (see the Timing Diagram section). The analog input (A_{IN}^+, A_{IN}^-) is differential for improved common mode noise immunity and to maximize the input range. Additionally, the differential input drive will reduce even order harmonics of the sample and hold circuit. The encode clock input (ENC^+, ENC^-) is also differential for improved common mode noise immunity.

Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC, and an error residue amplifier. The function of each stage is to produce a digital representation of its input voltage along with the resulting analog error residue. The ADC of each stage provides the quantization, and the residue is produced by taking the difference between the input voltage and the output of the reconstruction DAC. The residue is amplified by the residue amplifier and passed on to the next stage. The successive stages of the pipeline operate on alternating phases of the clock so that when odd stages are outputting their residue, the even stages are acquiring that residue and vice versa.

The pipelined ADC of the LTC2274 has two phases of operation determined by the state of the differential ENC^+/ENC^- input pins. For brevity, the text will refer to ENC^+ greater than ENC^- as ENC high and ENC^+ less than ENC^- as ENC low.

When ENC is low, the analog input is sampled differentially onto the input sample-and-hold capacitors, inside the "S/H & PGA" block of Figure 1. On the rising edge of ENC, the voltage on the sample capacitors is held. While ENC is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H amplifier during the high phase of ENC. On the falling edge of ENC, the first stage produces its residue which is acquired by the second stage. The process continues to the end of the pipeline.

Each ADC stage following the first has additional error correction range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally delayed such that the results can be properly combined in the correction logic before being encoded, serialized, and sent to the output buffer.

APPLICATIONS INFORMATION

SAMPLE/HOLD OPERATION AND INPUT DRIVE

Sample/Hold Operation

Figure 2 shows an equivalent circuit for the LTC2274 CMOS differential sample and hold. The differential analog inputs are sampled directly onto sampling capacitors (C_{SAMPLE}) through NMOS transistors. The capacitors shown attached to each input ($C_{PARASITIC}$) are the summation of all other capacitance associated with each input.

During the sample phase when ENC is low, the NMOS transistors connect the analog inputs to the sampling capacitors and they charge to, and track, the differential input voltage. On the rising edge of ENC, the sampled input voltage is held on the sampling capacitors. During the hold phase when ENC is high, the sampling capacitors are disconnected from the input and the held voltage is passed to the ADC core for processing. As ENC transitions for high to low, the inputs are reconnected to the sampling capacitors to acquire a new sample. Since the sampling capacitors still hold the previous sample, a charging glitch proportional to the change in voltage between samples will be seen at this time. If the change between the last sample and the new sample is small, the charging glitch seen at the input will be small. If the input change is large, such as the change seen with input frequencies near Nyquist, then a larger charging glitch will be seen.

Common Mode Bias

The ADC sample-and-hold circuit requires differential drive to achieve specified performance. Each input should swing ±0.5625V for the 2.25V range (PGA = 0) or ±0.375V for the 1.5V range (PGA = 1), around a common mode voltage of 1.25V. The V_{CM} output pin (Pin 39) is designed to provide the common mode bias level. V_{CM} can be tied directly to the center tap of a transformer to set the DC input level or as a reference level to an op amp differential driver circuit. The V_{CM} pin must be bypassed to ground close to the ADC with 2.2µF or greater.

Input Drive Impedance

As with all high performance, high speed ADCs the dynamic performance of the LTC2274 can be influenced by the input drive circuitry, particularly the second and third harmonics. Source impedance and input reactance can influence SFDR. At the falling edge of ENC the sample-and-hold circuit will connect the 4.9pF sampling capacitor to the input pin and start the sampling period. The sampling period ends when ENC rises, holding the sampled input on the sampling capacitor. Ideally, the input circuitry should be fast enough to fully charge the sampling capacitor during the sampling period $1/(2F_{ENCODE})$; however, this is not always possible and the incomplete settling may degrade the SFDR. The sampling glitch has been designed to be as linear as possible to minimize the effects of incomplete settling.

For the best performance it is recommended to have a source impedance of 100Ω or less for each input. The source impedance should be matched for the differential inputs. Poor matching will result in higher even order harmonics, especially the second.

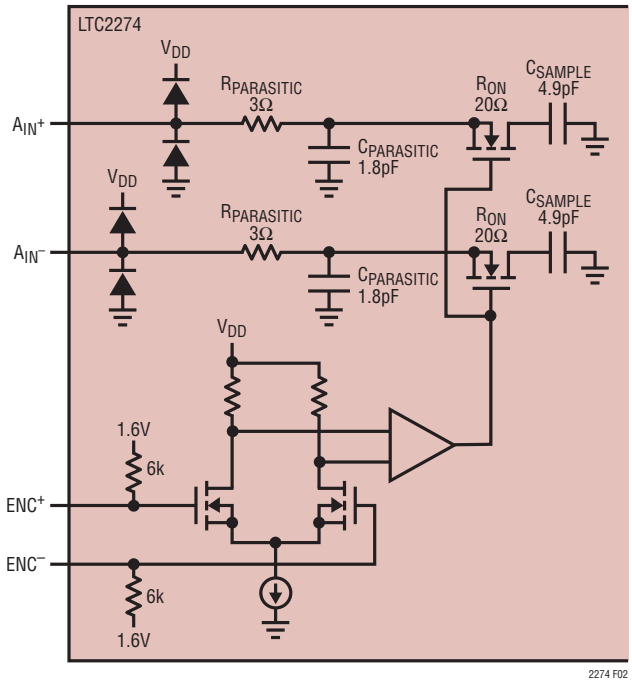


Figure 2. Equivalent Input Circuit

APPLICATIONS INFORMATION

INPUT DRIVE CIRCUITS

Input Filtering

A first order RC lowpass filter at the input of the ADC can serve two functions: limit the noise from input circuitry and provide isolation from ADC S/H switching. The LTC2274 has a very broadband S/H circuit, DC to 700MHz; it can be used in a wide range of applications; therefore, it is not possible to provide a single recommended RC filter.

Figures 3, 4a and 4b show three examples of input RC filtering at three ranges of input frequencies. In general it is desirable to make the capacitors as large as can be tolerated—this will help suppress random noise as well as noise coupled from the digital circuitry. The LTC2274 does not require any input filter to achieve data sheet specifications; however, no filtering will put more stringent noise requirements on the input drive circuitry.

Transformer Coupled Circuits

Figure 3 shows the LTC2274 being driven by an RF transformer with a center-tapped secondary. The secondary center tap is DC biased with V_{CM}, setting the ADC input signal at its optimum DC level. Figure 3 shows a 1:1 turns ratio transformer. Other turns ratios can be used; however, as the turns ratio increases so does the impedance seen by the ADC. Source impedance greater than 50Ω can reduce the input bandwidth and increase high frequency distortion. A disadvantage of using a transformer is the loss of low frequency response. Most small RF transformers have poor performance at frequencies below 1MHz.

Center-tapped transformers provide a convenient means of DC biasing the secondary; however, they often show poor balance at high input frequencies, resulting in large 2nd order harmonics.

Figure 4a shows transformer coupling using a transmission line balun transformer. This type of transformer has much better high frequency response and balance than flux coupled center tap transformers. Coupling capacitors are added at the ground and input primary terminals to allow the secondary terminals to be biased at 1.25V. Figure 4b shows the same circuit with components suitable for higher input frequencies.

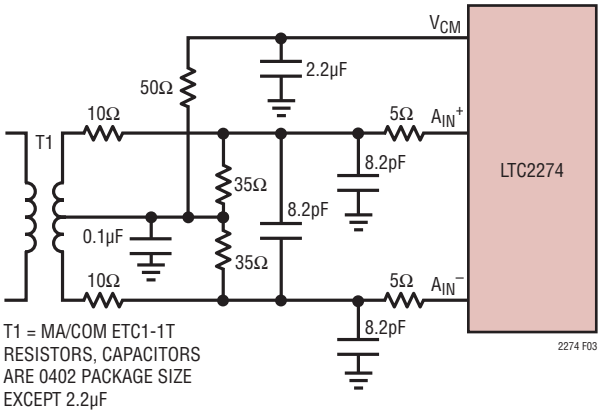


Figure 3. Single-Ended to Differential Conversion Using a Transformer. Recommended for Input Frequencies from 5MHz to 150MHz

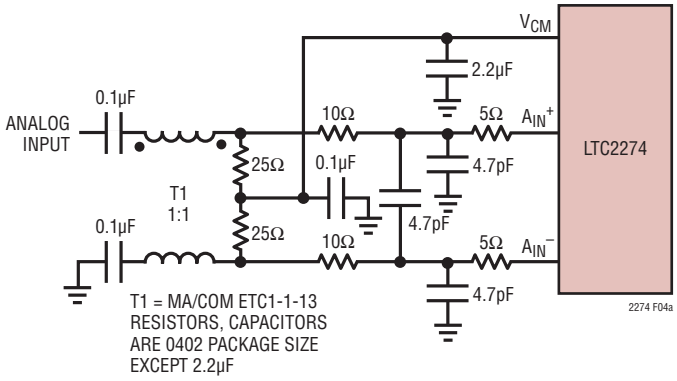


Figure 4a. Using a Transmission Line Balun Transformer. Recommended for Input Frequencies from 100MHz to 250MHz

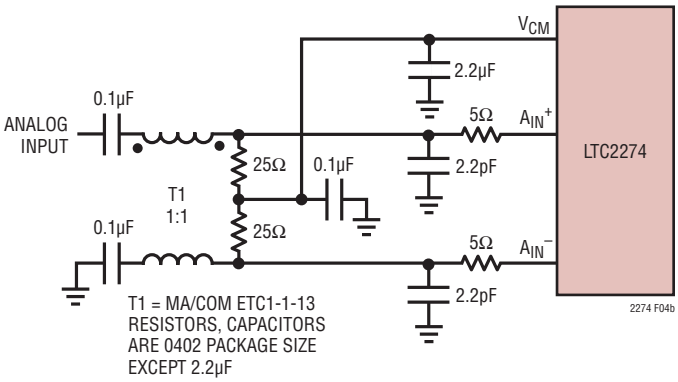


Figure 4b. Using a Transmission Line Balun Transformer. Recommended for Input Frequencies from 250MHz to 500MHz

APPLICATIONS INFORMATION

Direct Coupled Circuits

Figure 5 demonstrates the use of a differential amplifier to convert a single ended input signal into a differential input signal. The advantage of this method is that it provides low frequency input response; however, the limited gain bandwidth of any op amp or closed-loop amplifier will degrade the ADC SFDR at high input frequencies. Additionally, wideband op amps or differential amplifiers tend to have high noise. As a result, the SNR will be degraded unless the noise bandwidth is limited prior to the ADC input.

Reference Operation

Figure 6 shows the LTC2274 reference circuitry consisting of a 2.5V bandgap reference, a programmable gain amplifier and control circuit. The LTC2274 has three modes of reference operation: Internal Reference, 1.25V external reference or 2.5V external reference. To use the internal reference, tie the SENSE pin to V_{DD}. To use an external reference, simply apply either a 1.25V or 2.5V reference voltage to the SENSE input pin. Both 1.25V and 2.5V applied to SENSE will result in a full scale range of $2.25V_{P-P}$ (PGA = 0). A 1.25V output V_{CM} is provided for a common mode bias for input drive circuitry. An external bypass capacitor is required for the V_{CM} output. This provides a high frequency low impedance path to ground for internal and external circuitry. This is also the compensation capacitor for the reference; it will not be stable without this capacitor. The minimum value required for stability is 2.2µF.

The internal programmable gain amplifier provides the internal reference voltage for the ADC. This amplifier has very stringent settling requirements and is not accessible for external use.

The SENSE pin can be driven ±5% around the nominal 2.5V or 1.25V external reference inputs. This adjustment range can be used to trim the ADC gain error or other system gain errors. When selecting the internal reference, the SENSE pin should be tied to V_{DD} as close to the converter as possible. If the sense pin is driven externally it should be bypassed to ground as close to the device as possible with 1µF (or larger) ceramic capacitor.

PGA Pin

The PGA pin selects between two gain settings for the ADC front-end. PGA = 0 selects an input range of $2.25V_{P-P}$; PGA = 1 selects an input range of $1.5V_{P-P}$ The 2.25V input range has the best SNR; however, the distortion will be higher for input frequencies above 100MHz. For applications with high input frequencies, the low input range will have improved distortion; however, the SNR will be 2.4dB worse. See the Typical Performance Characteristics section of this datasheet.

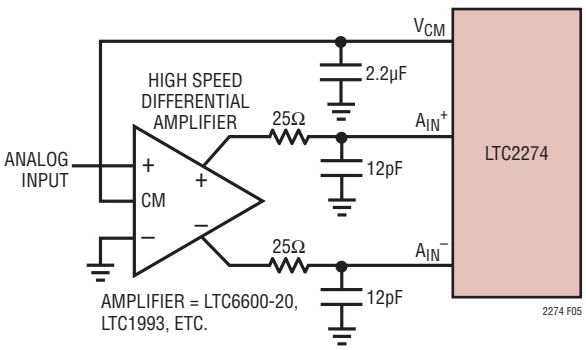


Figure 5. DC Coupled Input with Differential Amplifier

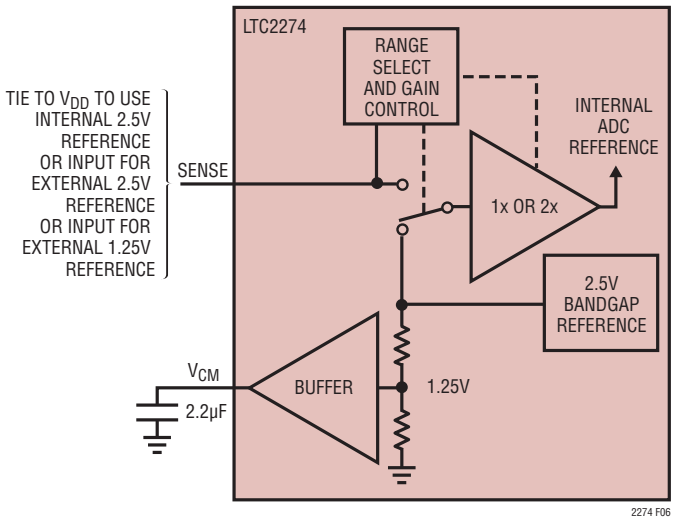


Figure 6. Reference Circuit

APPLICATIONS INFORMATION

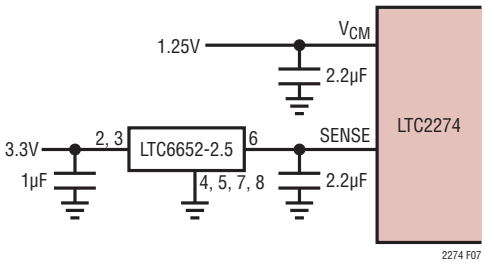


Figure 7. A 2.25V Range ADC with an External 2.5V Reference

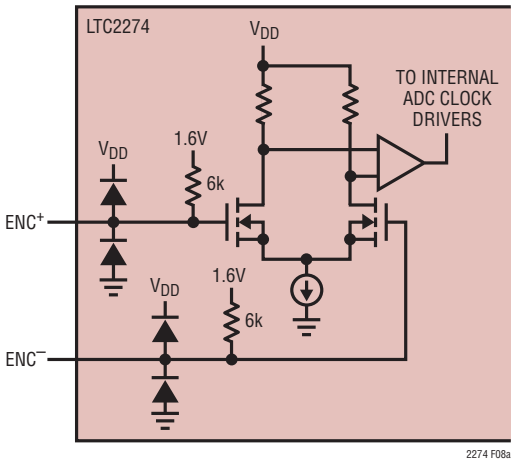
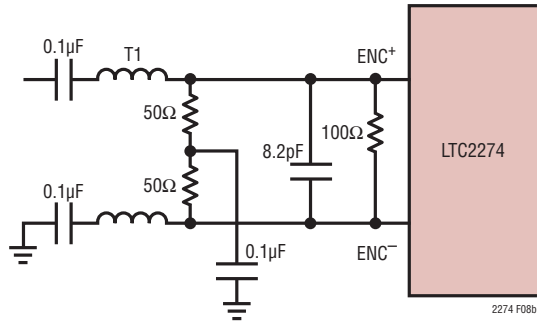


Figure 8a. Equivalent Encode Input Circuit



T1 = MA/COM ETC1-1-13
RESISTORS AND CAPACITORS
ARE 0402 PACKAGE SIZE

Figure 8b. Transformer Driven Encode

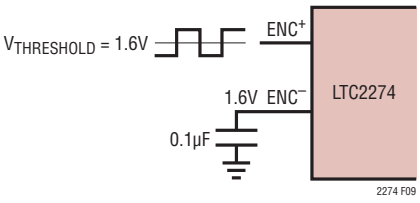


Figure 9. Single-Ended ENC Drive, Not Recommended for Low Jitter

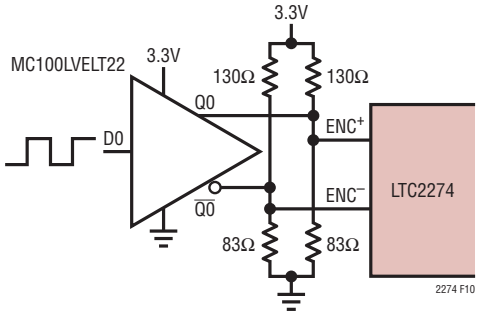


Figure 10. ENC Drive Using a CMOS to PECL Translator

APPLICATIONS INFORMATION

Driving the Encode Inputs

The noise performance of the LTC2274 can depend on the encode signal quality as much as for the analog input. The encode inputs are intended to be driven differentially, primarily for noise immunity from common mode noise sources. Each input is biased through a 6k resistor to a 1.6V bias. The bias resistors set the DC operating point for transformer coupled drive circuits and can set the logic threshold for single-ended drive circuits.

Any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical (high input frequencies), take the following into consideration:

1. Differential drive should be used.
2. Use as large an amplitude possible. If using transformer coupling, use a higher turns ratio to increase the amplitude.
3. If the ADC is clocked with a fixed frequency sinusoidal signal, filter the encode signal to reduce wideband noise.
4. Balance the capacitance and series resistance at both encode inputs such that any coupled noise will appear at both inputs as common mode noise.

The encode inputs have a common mode range of 1.2V to V_{DD}. Each input may be driven from ground to V_{DD} for single-ended drive.

Maximum and Minimum Conversion Rates

The maximum conversion rate is 105Msps for the LTC2274.

The lower limit of the LTC2274 sample rate is determined by the PLL minimum operating frequency of 20Msps.

For the ADC to operate properly, the internal CLK signal should have a 50% duty cycle. A duty cycle stabilizer circuit has been implemented on chip to facilitate non-50% ENC duty cycles.

Data Format

The MSBINV pin selects the ADC data format. A low level selects offset binary format (code 0 corresponds to –FS, and code 65535 corresponds to +FS). A high level on MSBINV selects 2's complement format (code –32768 corresponds to –FS and code 32767 corresponds to +FS.

Shutdown

A high level on both SHDN pins will shutdown the ADC and the serial interface and place the chip in a low current state.

Internal Dither

The LTC2274 is a 16-bit ADC with a very linear transfer function; however, at low input levels even slight imperfections in the transfer function will result in unwanted tones. Small errors in the transfer function are usually a result of ADC element mismatches. An optional internal dither mode can be enabled to randomize the input location on the ADC transfer curve, resulting in improved SFDR for low signal levels.

As shown in Figure 11, the output of the sample-and-hold amplifier is summed with the output of a dither DAC. The dither DAC is driven by a long sequence pseudo-random number generator; the random number fed to the dither DAC is also subtracted digitally from the ADC result. If the dither DAC is precisely calibrated to the ADC, very little of the dither signal will be seen at the output. The dither signal that does leak through will appear as white noise. The dither DAC is calibrated to result in less than 0.5dB elevation in the noise floor of the ADC, as compared to the noise floor with dither off.

APPLICATIONS INFORMATION

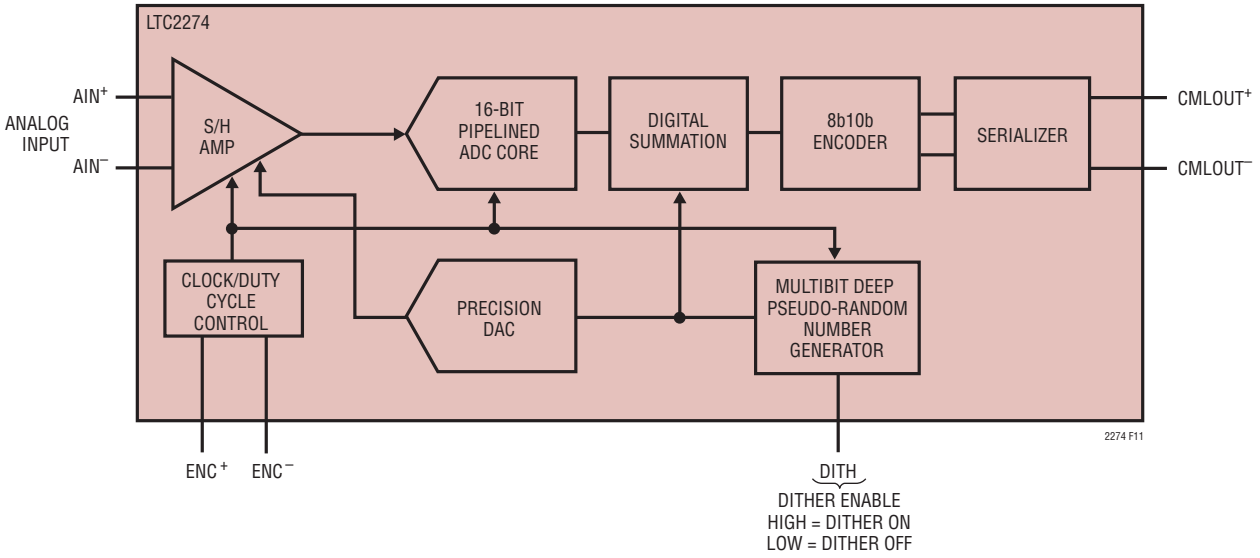


Figure 11. Functional Equivalent Block Diagram of Internal Dither Circuit

SERIALIZED DATA FRAME

Prior to serialization, the ADC data is encoded into the 8B/10B format, which is DC balanced, and run-length limited. The receiver is required to lock onto the data and recover the clock with the use of a PLL. The 8B/10B format requires that the ADC data be broken up into 8-bit blocks (octets), which is encoded into 10-bit code groups applying the 8B/10B rules (refer to IEEE Std 802.3-2002 Part 3, for a complete 8B/10B description).

Figure 12 illustrates the generation of one complete 8B/10B frame. The 8 most significant bits of the ADC are assigned to the first half of the frame, and the remaining 8 bits to the second half of the frame. Next, the two resulting octets are optionally scrambled and encoded into their corresponding 8B/10B code. Finally, the two 10-bit code groups are serialized and transmitted beginning with Bit 0 of code group 1.

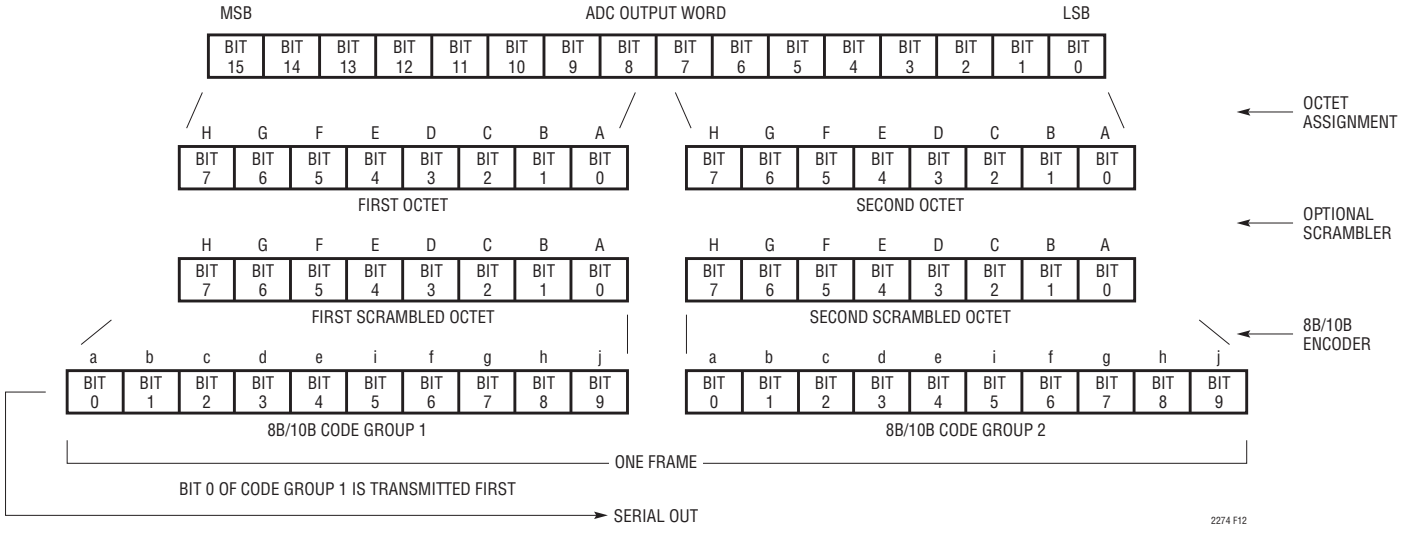


Figure 12. Evolution of One Transmitted Frame (Compare to IEEE Std 802.3-2002 Part 3, Figure 36-3)

APPLICATIONS INFORMATION

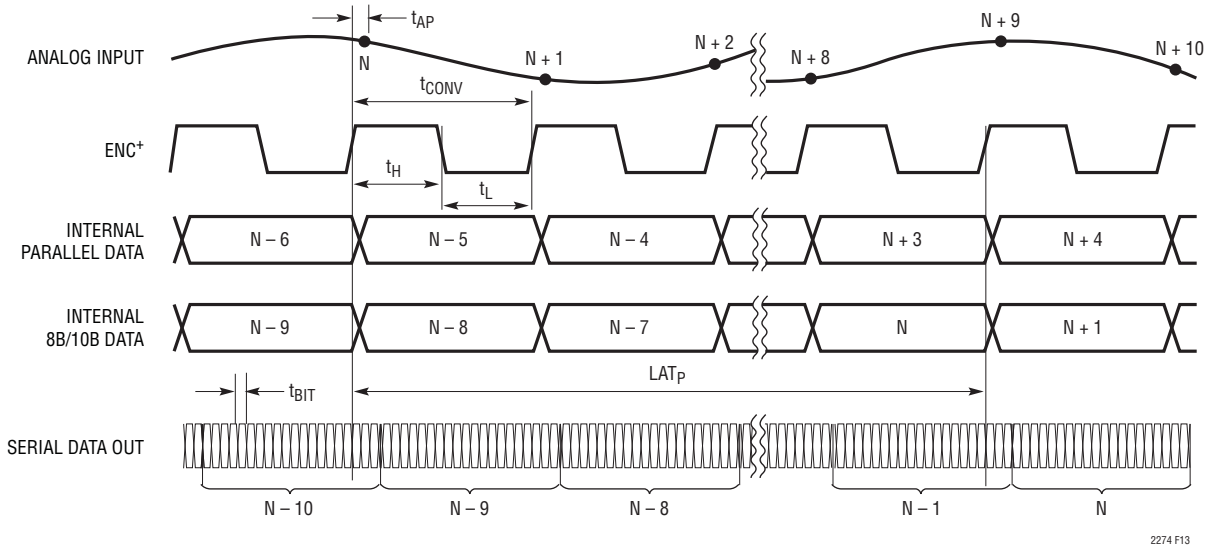


Figure 13. Timing Relationship of Analog Sample to Serial Data Out

Initial Frame Synchronization

In the absence of a frame clock, it is necessary to determine the start of each frame through a synchronization process. To establish frame synchronization, Figures 14 and 15 illustrate the following sequence:

- The receiver issues a synchronization request via the synchronization interface.
- If the synchronization request is active for more than one ENC clock cycle, the LTC2274 will transmit a synchronization preamble. When the ISMODE pin is low the transmitted preamble will consist of consecutive K28.5 comma symbols in conformance with the JESD204 specification. When the ISMODE pin is high, a series of idle ordered sets will be transmitted. The idle ordered sets consist of a K28.5 comma followed by either D5.6 or D16.2 as defined in IEEE Std 802.3-2002 part3, Clause 36.2.4.12.
- The receiver searches for the expected preamble and waits for the correct reception of an adequate number of preamble characters.
- The receiver deactivates the synchronization request.
- Upon detecting the deactivation of the synchronization request, the LTC2274 continues to transmit the synchronization preamble until the end of the frame.
- At the start of the next frame, the LTC2274 will begin transmitting data characters.
- The receiver designates the first data character received after the preamble transmission to be the start of the frame. The first octet of the frame contains the most significant byte of the ADC's output word.

APPLICATIONS INFORMATION

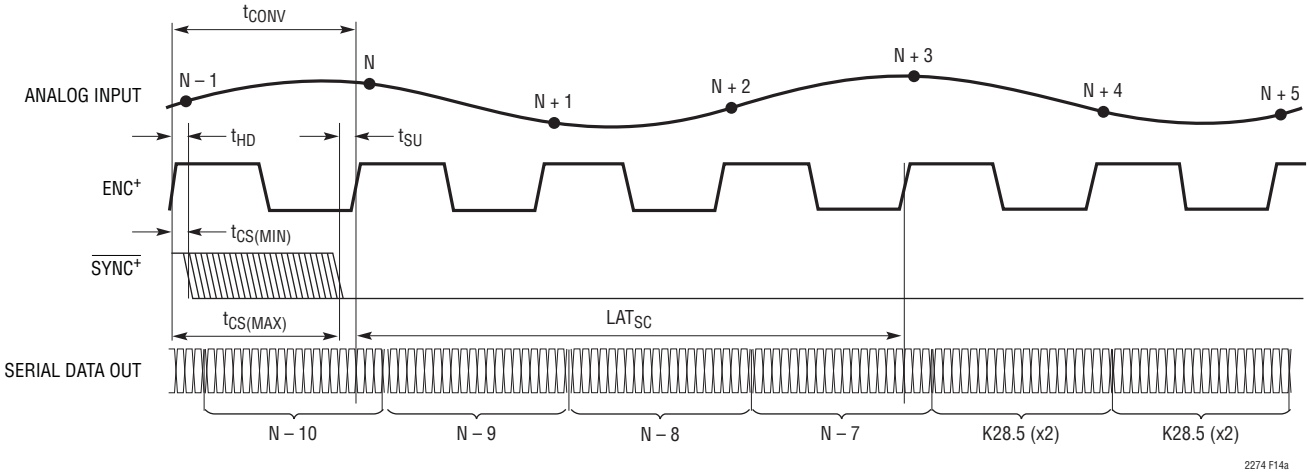


Figure 14a. $\overline{\text{SYNC}}^+$ Low Transition to Comma Output Timing (ISMODE is Low)

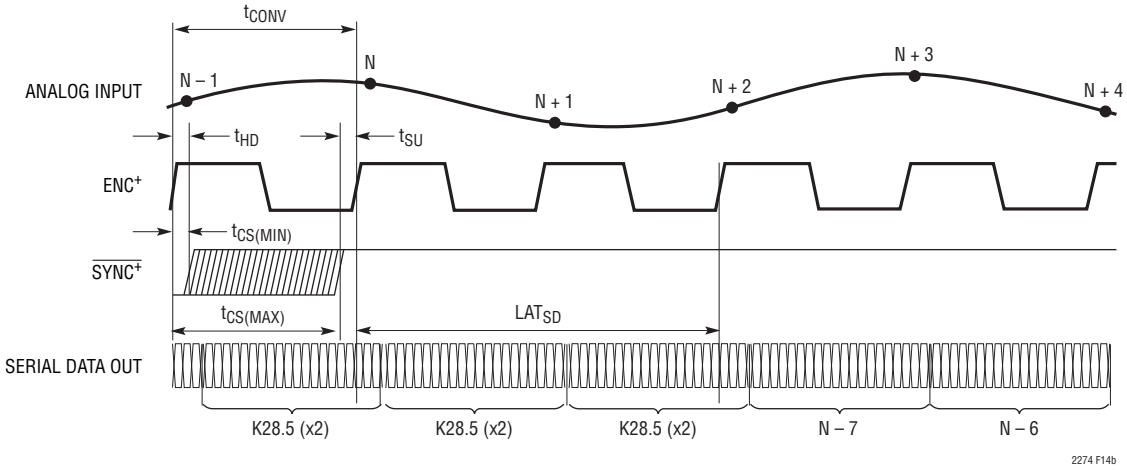


Figure 14b. $\overline{\text{SYNC}}^+$ High Transition to Data Output Timing (ISMODE is Low)

APPLICATIONS INFORMATION

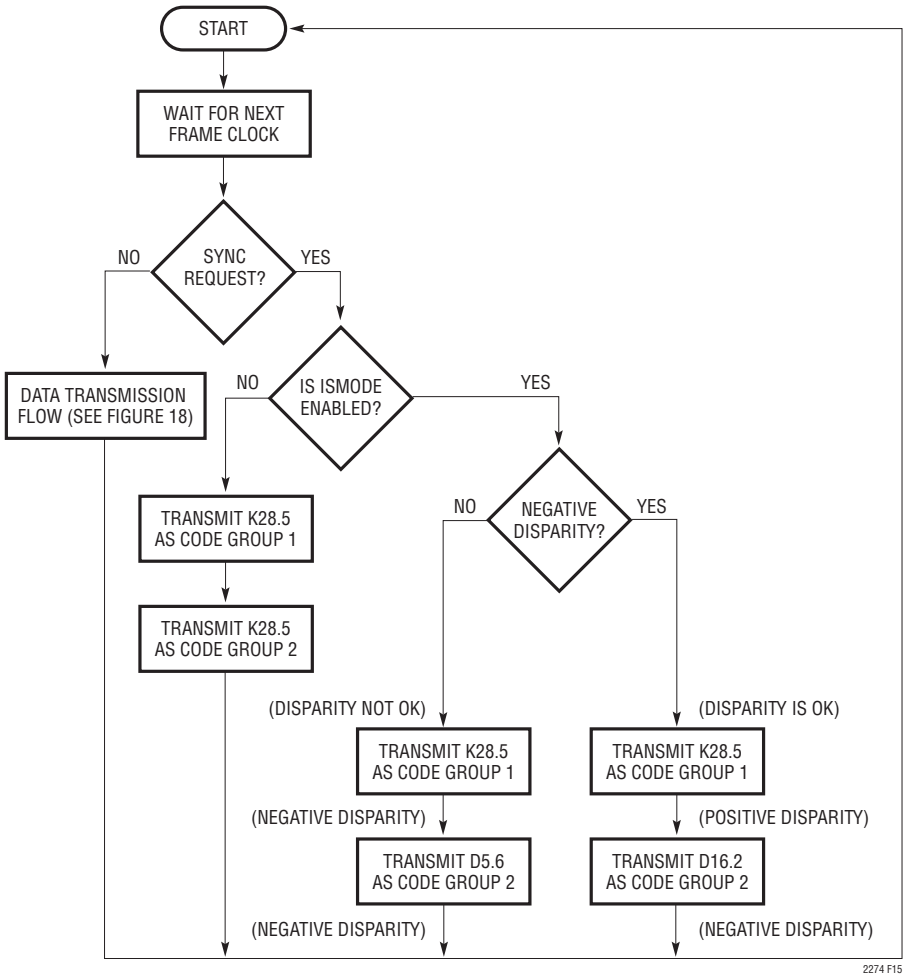


Figure 15. Initial Synchronization Flow Diagram

Scrambling

To avoid spectral interference from the serial data output, an optional data scrambler is added between the ADC data and the 8B/10B encoder to randomize the spectrum of the serial link. The scrambler is enabled by setting the SCRAM pin to a high logic level. The polynomial used for the scrambler is $1 + x^{14} + x^{15}$, which is a pseudo-random pattern repeating itself every $2^{15}–1$. Figure 16 illustrates the LTC2274 implementation of this polynomial in parallel form.

The scrambled data is converted into two valid 8B/10B code groups, constituting a complete frame. The 8B/10B code groups are then serialized and transmitted.

The receiver is required to deserialize the data, decode the code-groups into octets and descramble them back to the original octets using the self-aligning descrambler shown in Figure 17. This descrambler is shown in 16-bit parallel form, which is an efficient implementation of the $(1 + x^{14} + x^{15})$ polynomial, operating at the frame clock rate (ADC sample rate).

APPLICATIONS INFORMATION

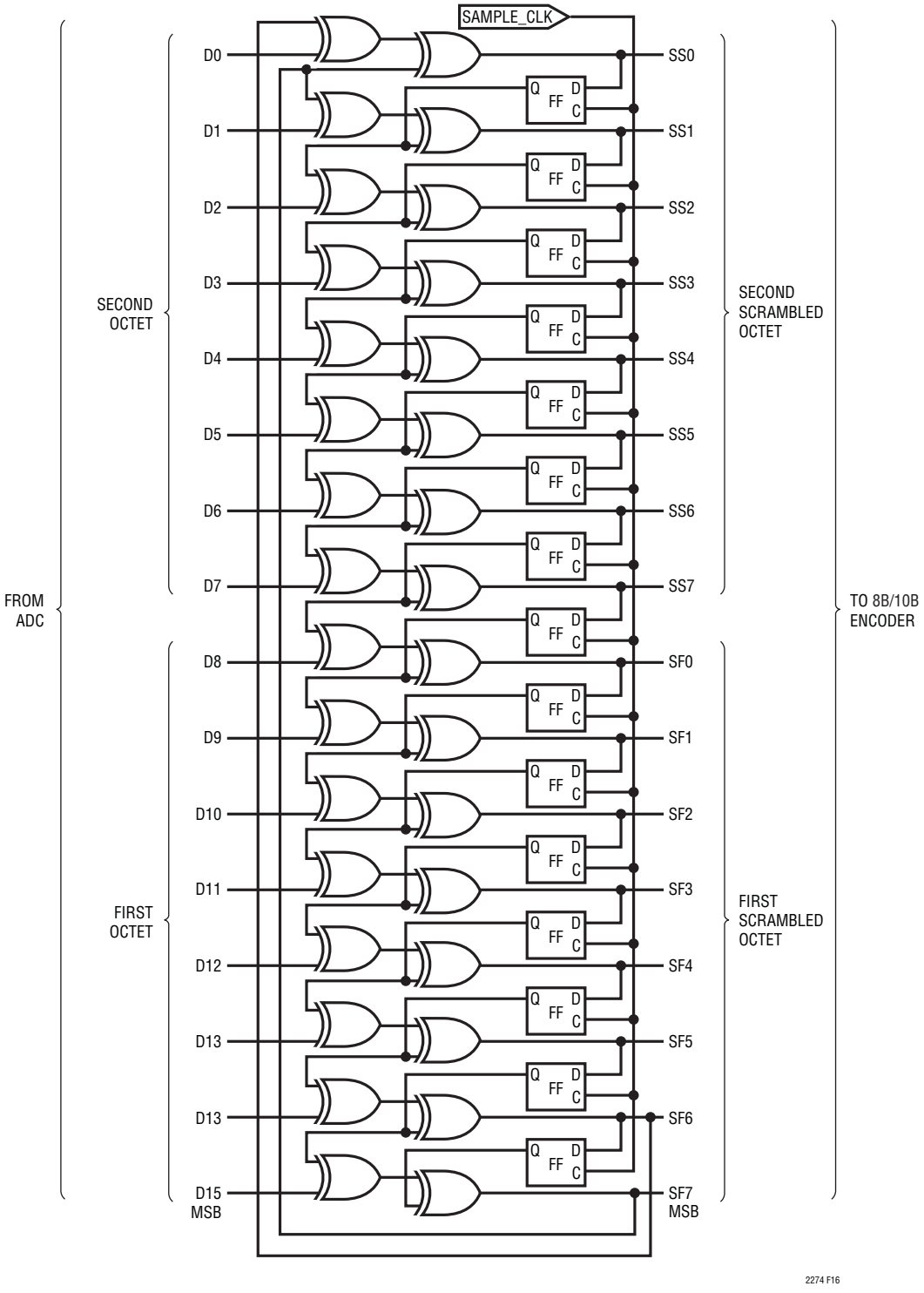


Figure 16. LTC2274 16-Bit 1 + x^{14} + x^{15} Parallel Scrambler

APPLICATIONS INFORMATION

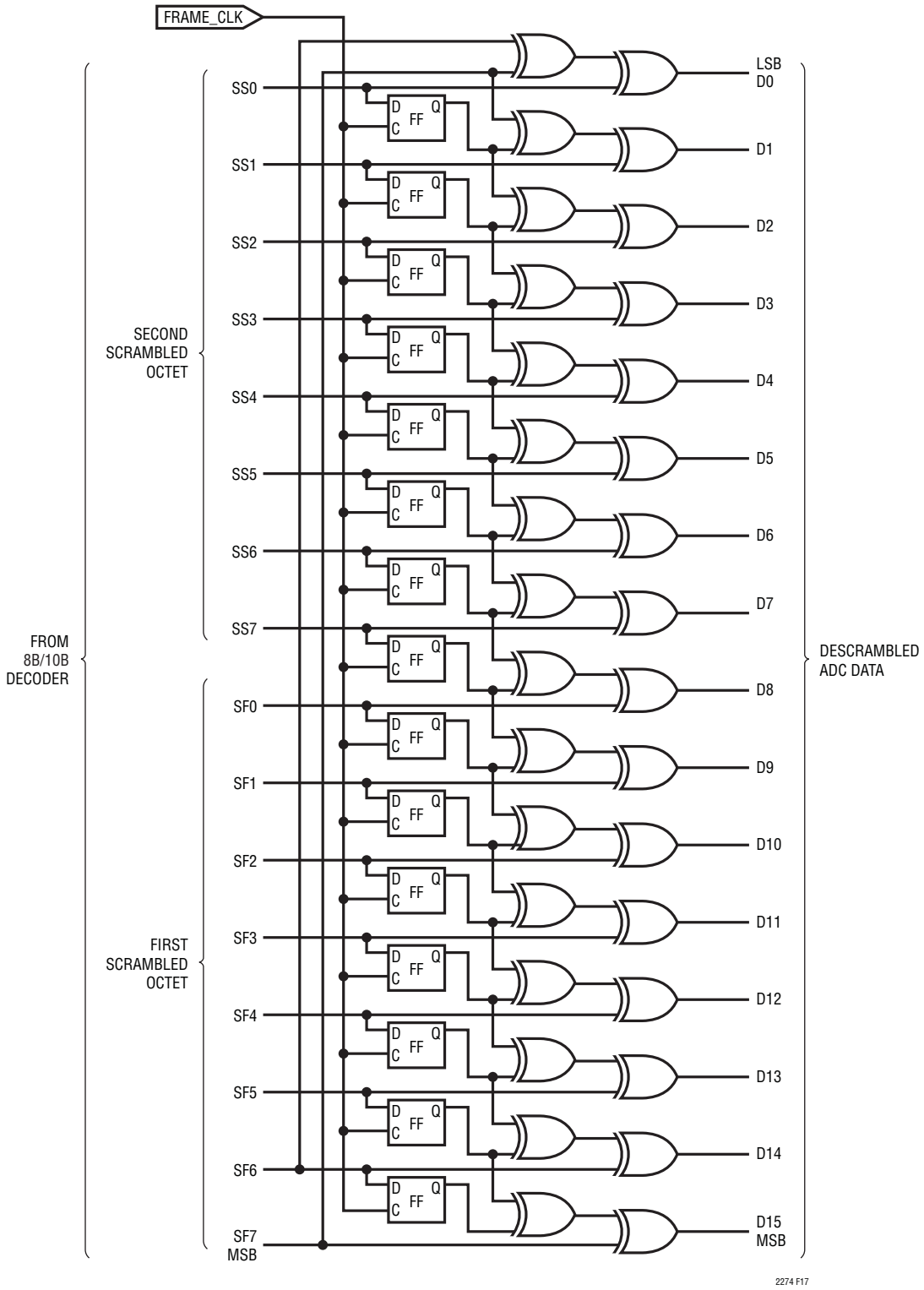


Figure 17. Required 16-Bit 1 + x^{14} + x^{15} Parallel Descrambler

APPLICATIONS INFORMATION

Frame Alignment Monitoring

After the initial synchronization has been established, it may be desirable to periodically verify that frame alignment is being maintained. The receiver may issue a synchronization request at any time, but data will be lost during the resynchronization interval.

To verify frame alignment without the loss of data, frame alignment monitoring is enabled by setting the FAM pin to a high level. In this mode, predetermined data in the second code group of the frame is substituted with the control character K28.7. The receiver is required to detect the K28.7 character and replace it with the original data. In this way, the second code group may be discerned from the first, and the receiver is able to periodically verify the frame alignment without the loss of data (refer to Table 1 and the flow diagram of Figure 18). There are two frame alignment monitoring modes summarized in Table 1.

FAM mode 1 is implemented when FAM is high, and SCRAM is low:

- When the data in the second code group of the current frame equals the data in the second code group of the previous frame, the LTC2274 will replace the second code group with the control character K28.7 before serialization. However, if a K28.7 symbol was already transmitted in the previous frame, the actual code group will be transmitted.
- Upon receiving a K28.7 symbol, the receiver is required to replace it with the data decoded at the same position of the previous frame.

FAM mode 2 is implemented when FAM is high and SCRAM is high:

- When the data in the second code group of the current frame equals D28.7, the LTC2274 will replace this data with K28.7 before serialization.
- Upon receiving a K28.7 symbol, the receiver is required to replace it with D28.7.

With FAM enabled the receiver is required to search for the presence of K28.7 symbols in the data stream. If two successive K28.7 symbols are detected at the same position other than the assumed end of frame, the receiver will realign its frame boundary to the new position.

Table 1. Frame Alignment Monitoring Modes

	SCRAM PIN	DDSYNC PIN	ACTION
FAM Mode 1	Low	High	The second code group is replaced with K28.7 if it is equal to the 2nd Code Group of the previous frame
FAM Mode 2	High	High	The second code group is replaced with K28.7 if it is equal to D28.7
FAM OFF	X	Low	No K28.7 substitutions will take place

APPLICATIONS INFORMATION

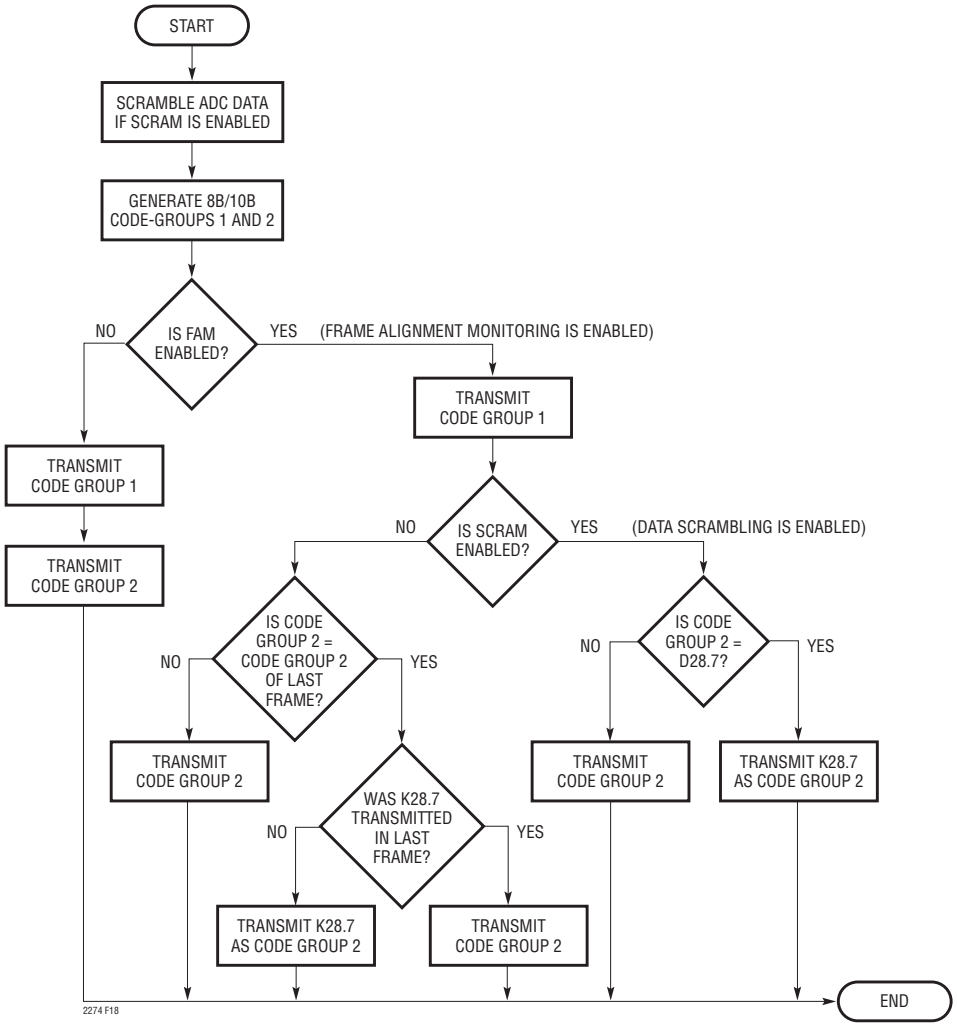


Figure 18. Data Transmission Flow Diagram

PLL Operation

The PLL has been designed to accommodate a wide range of sample rates. The SRR0 and SRR1 pins are used to configure the PLL for the intended sample rate range. Table 2 summarizes the sample clock ranges available to the user.

Table 2. Sample Rate Ranges

SRR1	SRR0	SAMPLE RATE RANGE
0	x	20Msps < FS ≤ 35Msps
1	0	30Msps < FS ≤ 65Msps
1	1	60Msps < FS ≤ 105Msps

Serial Test Patterns

To facilitate testing of the serial interface, three test patterns are selectable via pins PAT0 and PAT1. The available test patterns are described in Table 3. A K28.5 comma may be used as a fourth test pattern by requesting synchronization through the $\overline{SYNC^+}$/$\overline{SYNC^-}$ pins.

Table 3. Test Patterns

PAT1	PAT0	TEST PATTERNS
0	0	ADC Data
0	1	1010101010 Pattern (8B/10B Code Group D21.5)
1	0	$1+x^9+x^{11}$ Pseudo Random Pattern
1	1	$1+x^{14}+x^{15}$ Pseudo Random Pattern

APPLICATIONS INFORMATION

High Speed CML Outputs

The CML outputs must be terminated for proper operation. The OV_{DD} supply voltage and the termination voltage determine the common mode output level of the CML outputs. For proper operation of the CML driver, the output common mode voltage should be greater than 1V.

The directly-coupled termination mode of Figure 19a is recommended when the receiver termination voltage is within the range of 1.2V to 3.3V. When the CML outputs are directly-coupled to the 50Ω termination resistors, the OV_{DD} supply voltage serves as the receiver termination voltage, and the output common mode voltage will be approximately 200mV lower than OV_{DD}.

The directly-coupled differential termination of Figure 19b may be used in the absence of a receiver termination voltage within the required range. In this case, the common mode voltage is shifted down to approximately 400mV below OV_{DD}, requiring an OV_{DD} in the range of 1.4V to 3.3V.

If the serial receiver's common mode input requirements are not compatible with the directly-coupled termination modes, the DC balanced 8B/10B encoded data will permit the addition of DC blocking capacitors as shown in Figure 19c. In this AC-coupled mode, the termination voltage is determined by the receiver's requirements. The coupling capacitors should be selected appropriately for the intended operating bit-rate, usually between 1nF to 10nF. In the AC-coupled mode, the output common mode voltage will be approximately 400mV below OV_{DD}, so the OV_{DD} supply voltage should be in the range of 1.4V to 3.3V.

Grounding and Bypassing

The LTC2274 require a printed circuit board with a clean unbroken ground plane; a multilayer board with an internal ground plane is recommended. The pinout of the LTC2274 has been optimized for a flowthrough layout so that the interaction between inputs and digital outputs is minimized. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD}, V_{CM}, and OV_{DD} pins. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC2274 differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

Heat Transfer

Most of the heat generated by the LTC2274 is transferred from the die through the bottom-side exposed pad. For good electrical and thermal performance, the exposed pad must be soldered to a large grounded pad on the PC board. It is critical that the exposed pad and all ground pins are connected to a ground plane of sufficient area with as many vias as possible.

APPLICATIONS INFORMATION

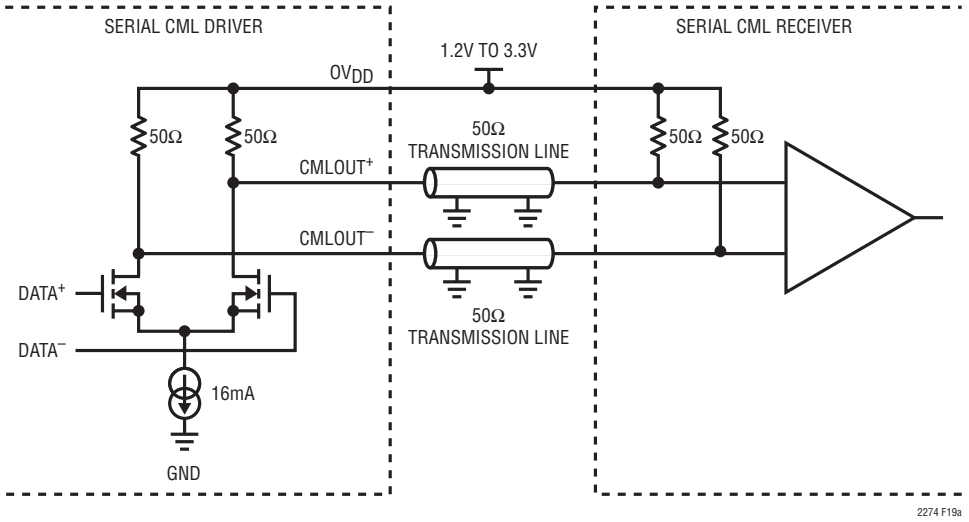


Figure 19a. CML Termination, Directly-Coupled Mode (Preferred)

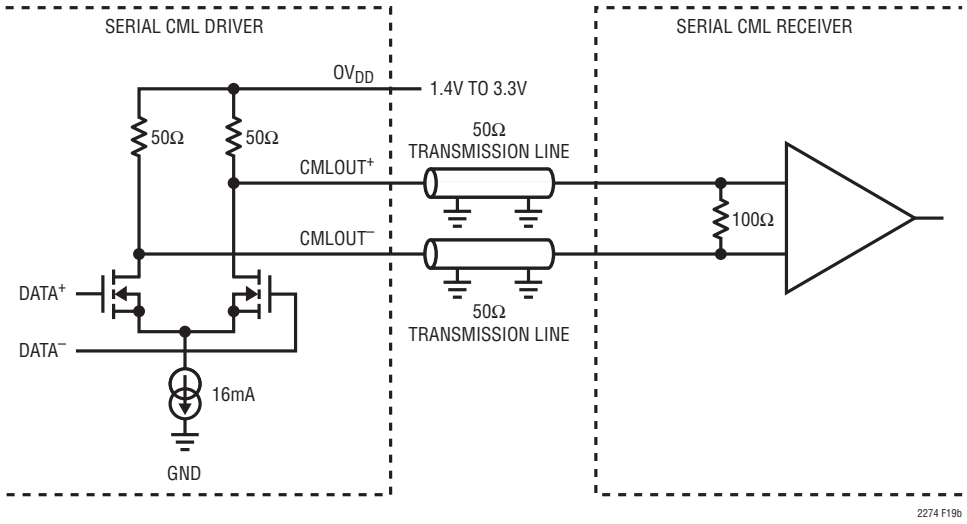


Figure 19b. CML Termination, Directly-Coupled Differential Mode

APPLICATIONS INFORMATION

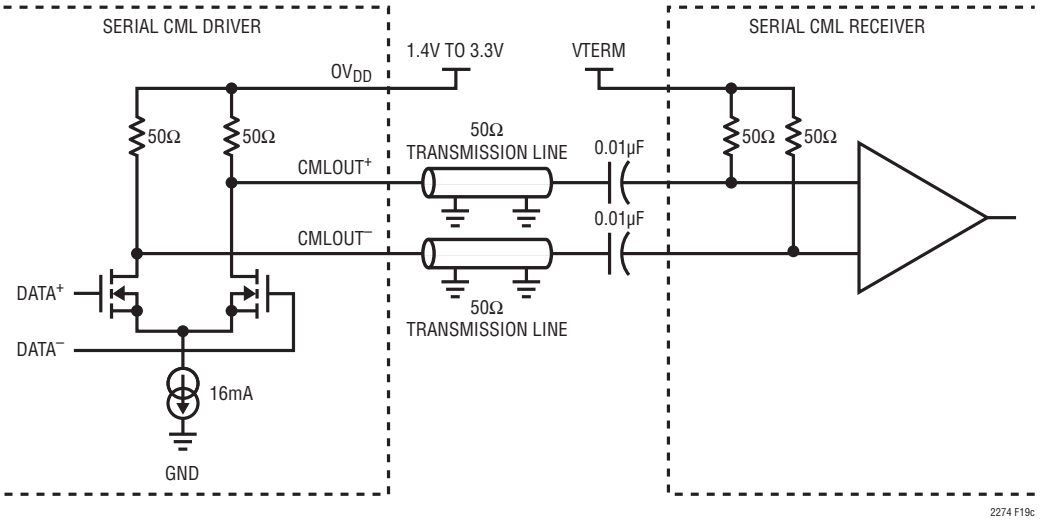
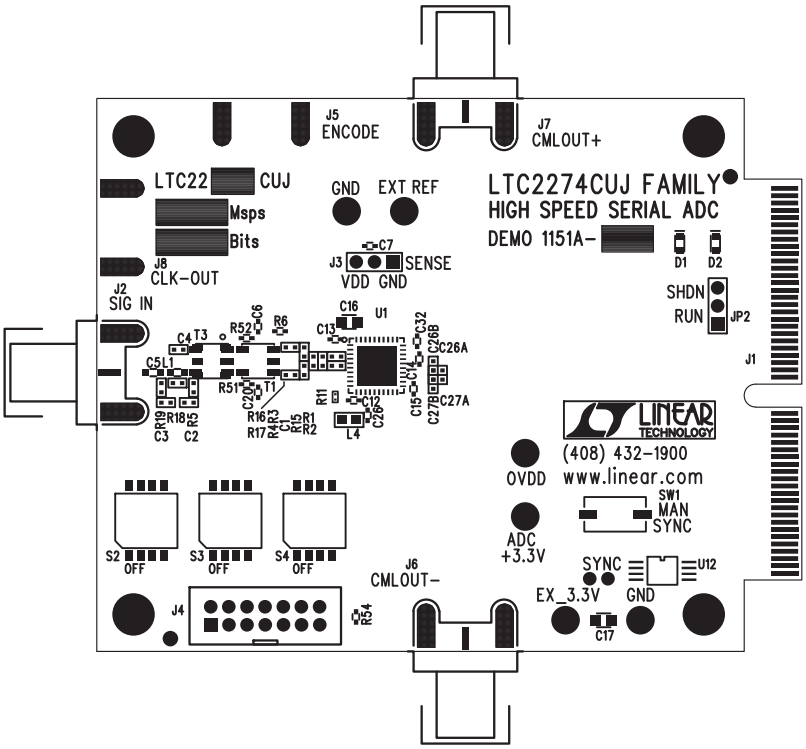


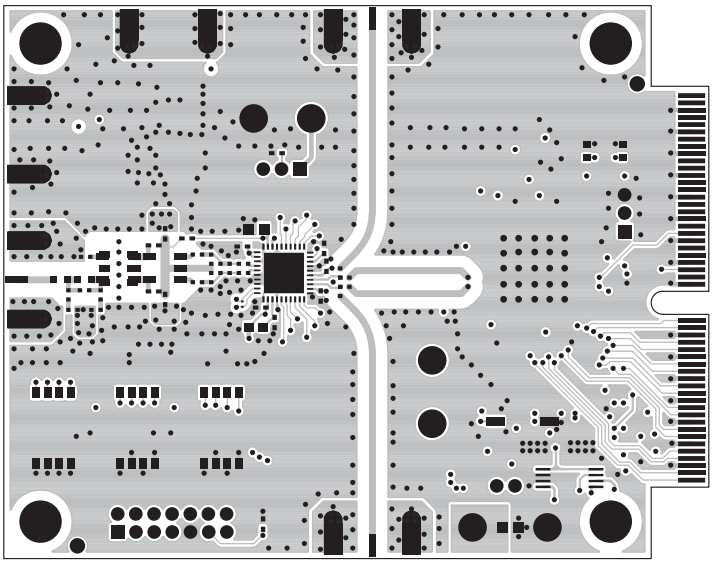
Figure 19c. CML Termination, AC-Coupled Mode

TYPICAL APPLICATIONS

Silkscreen Top

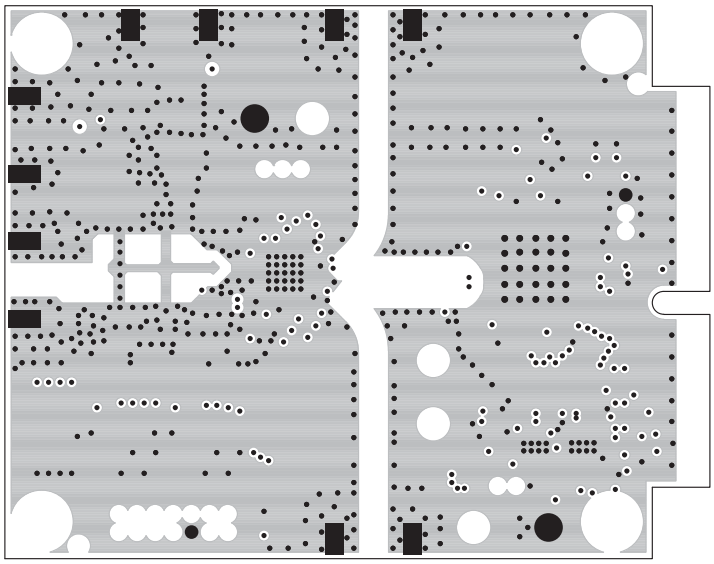


Top Side

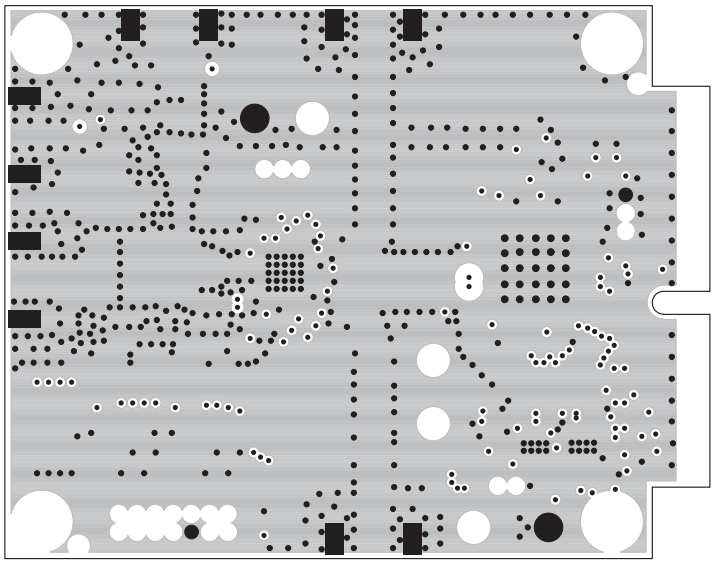


TYPICAL APPLICATIONS

Inner Layer 2

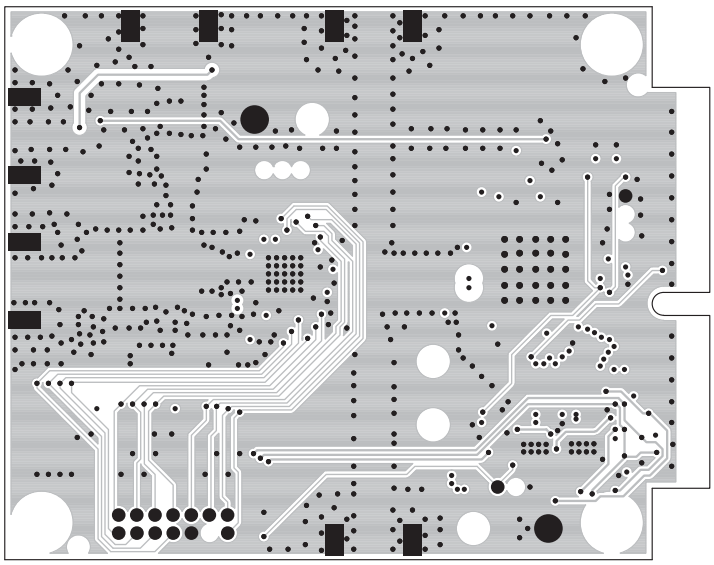


Inner Layer 3

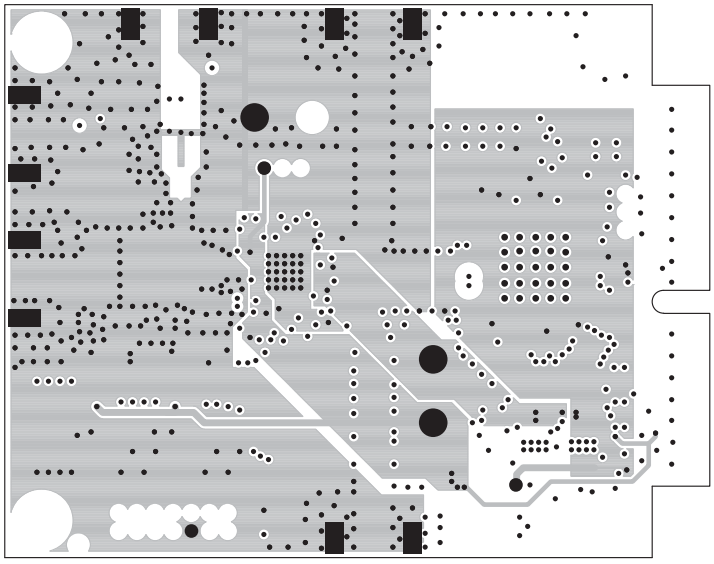


TYPICAL APPLICATIONS

Inner Layer 4

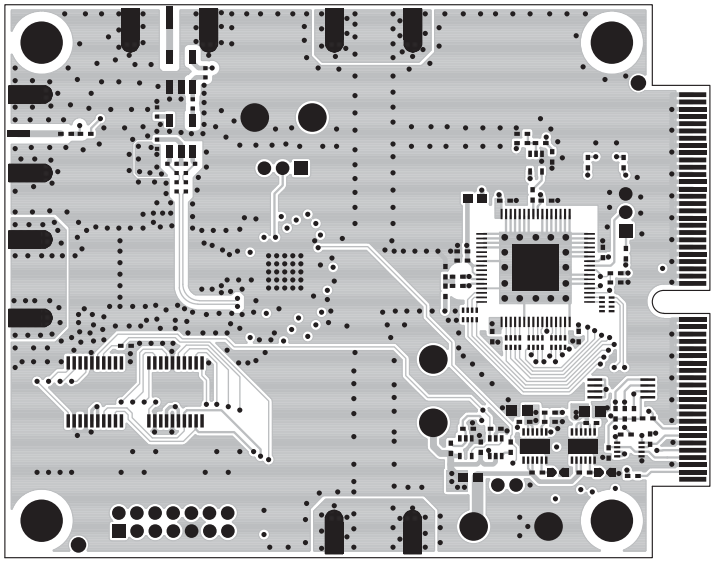


Inner Layer 5

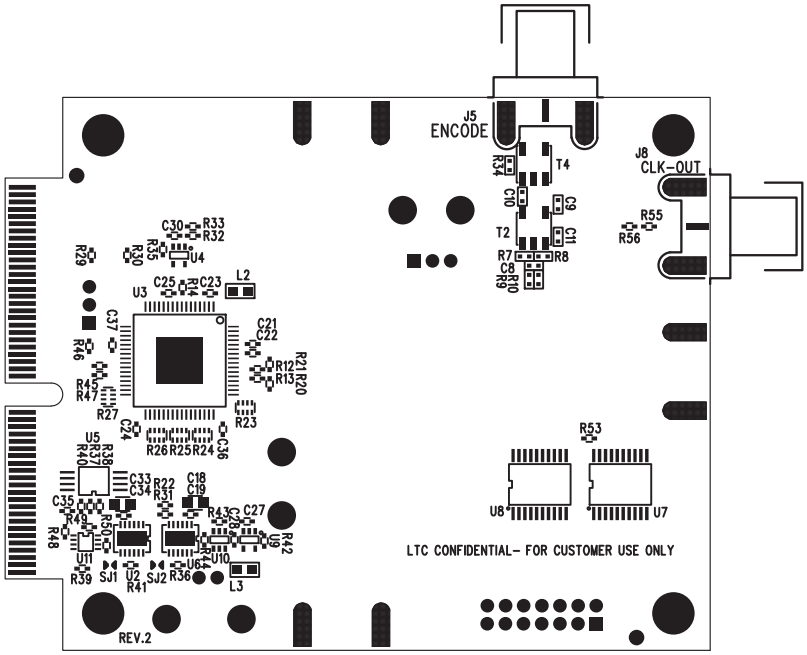


TYPICAL APPLICATIONS

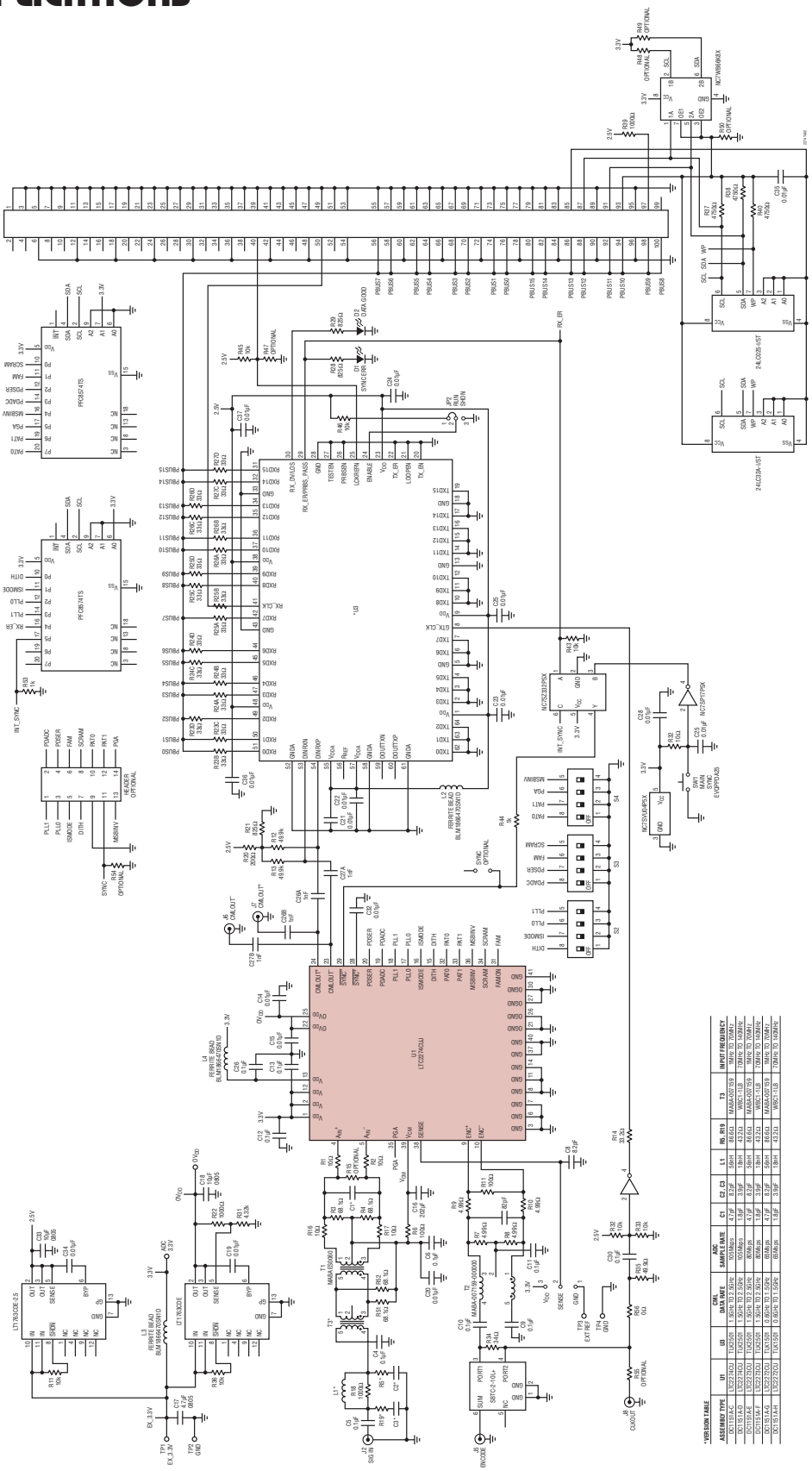
Bottom Side



Silkscreen Bottom



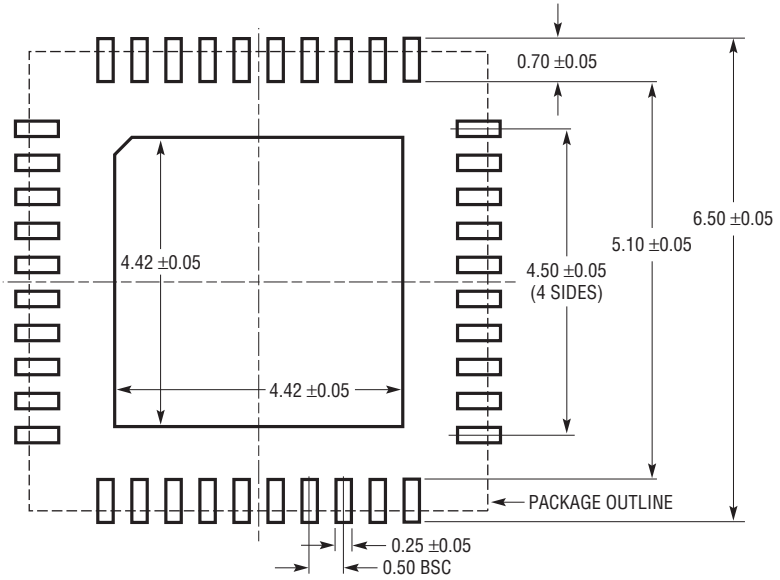
TYPICAL APPLICATIONS



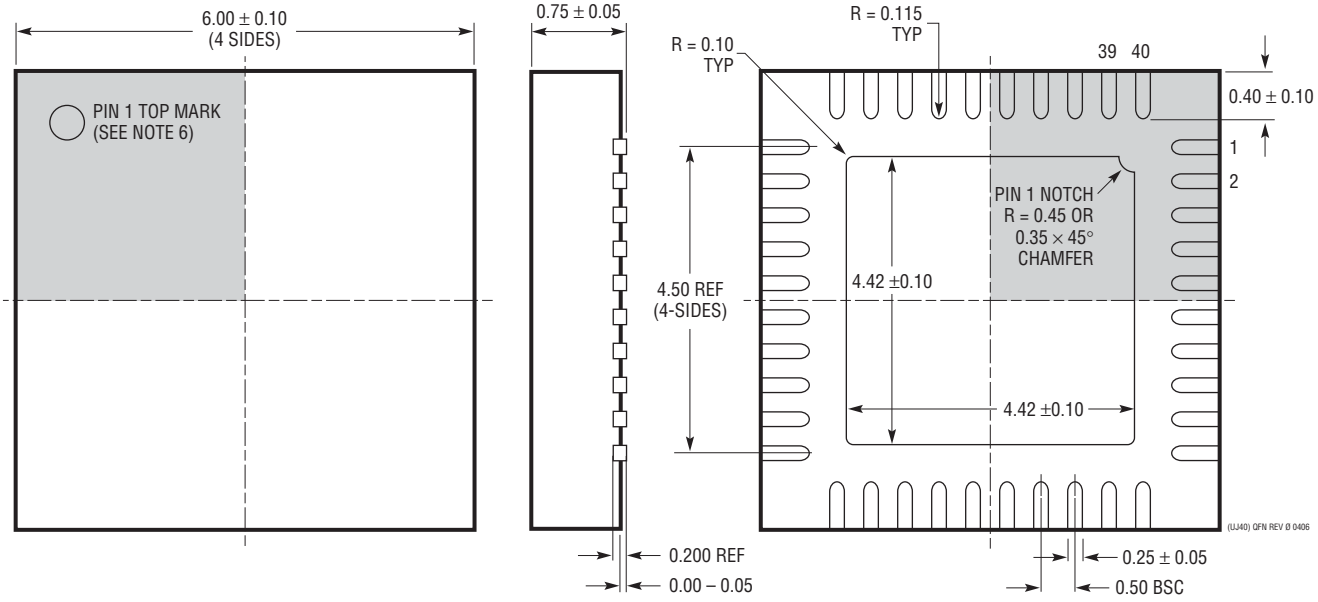
2274fb

PACKAGE DESCRIPTION

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1728 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1993-2	High Speed Differential Op Amp	800MHz BW, 70dBc Distortion at 70MHz, 6dB Gain
LTC1994	Low Noise, Low Distortion Fully Differential Input/ Output Amplifier/Driver	Low Distortion: –94dBc at 1MHz
LTC2215	16-Bit, 65Msps, Low Noise ADC	700mW, 81.5dB SNR, 100dB SFDR, 64-Pin QFN
LTC2216	16-Bit, 80Msps, Low Noise ADC	970mW, 81.3dB SNR, 100dB SFDR, 64-Pin QFN
LTC2217	16-Bit, 105Msps, Low Noise ADC	1190mW, 81.2dB SNR, 100dB SFDR, 64-Pin QFN
LTC2202	16-Bit, 10Msps, 3.3V ADC, Lowest Noise	140mW, 81.6dB SNR, 100dB SFDR, 48-Pin QFN
LTC2203	16-Bit, 25Msps, 3.3V ADC, Lowest Noise	220mW, 81.6dB SNR, 100dB SFDR, 48-Pin QFN
LTC2204	16-Bit, 40Msps, 3.3V ADC	480mW, 79dB SNR, 100dB SFDR, 48-Pin QFN
LTC2205	16-Bit, 65Msps, 3.3V ADC	590mW, 79dB SNR, 100dB SFDR, 48-Pin QFN
LTC2206	16-Bit, 80Msps, 3.3V ADC	725mW, 77.9dB SNR, 100dB SFDR, 48-Pin QFN
LTC2207	16-Bit, 105Msps, 3.3V ADC	900mW, 77.9dB SNR, 100dB SFDR, 48-Pin QFN
LTC2208	16-Bit, 130Msps, 3.3V ADC, LVDS Outputs	1250mW, 77.7dB SNR, 100dB SFDR, 64-Pin QFN
LTC2209	16-Bit, 160Msps, ADC, LVDS Outputs	1.45W, 77.1dB SNR, 100dB SFDR, 64-Pin QFN
LTC2220	12-Bit, 170Msps ADC	890mW, 67.5dB SNR, 9mm × 9mm QFN Package
LTC2220-1	12-Bit, 185Msps, 3.3V ADC, LVDS Outputs	910mW, 67.7dB SNR, 80dB SFDR, 64-Pin QFN
LTC2224	12-Bit, 135Msps, 3.3V ADC, High IF Sampling	630mW, 67.6dB SNR, 84dB SFDR, 48-Pin QFN
LTC2249	14-Bit, 80Msps ADC	230mW, 73dB SNR, 5mm × 5mm QFN Package
LTC2250	10-Bit, 105Msps ADC	320mW, 61.6dB SNR, 5mm × 5mm QFN Package
LTC2251	10-Bit, 125Msps ADC	395mW, 61.6dB SNR, 5mm × 5mm QFN Package
LTC2252	12-Bit, 105Msps ADC	320mW, 70.2dB SNR, 5mm × 5mm QFN Package
LTC2253	12-Bit, 125Msps ADC	395mW, 70.2dB SNR, 5mm × 5mm QFN Package
LTC2254	14-Bit, 105Msps ADC	320mW, 72.5dB SNR, 5mm × 5mm QFN Package
LTC2255	14-Bit, 125Msps, 3V ADC, Lowest Power	395mW, 72.5dB SNR, 88dB SFDR, 32-Pin QFN
LTC2284	14-Bit, Dual, 105Msps, 3V ADC, Low Crosstalk	540mW, 72.4dB SNR, 88dB SFDR, 64-Pin QFN
LTC2299	Dual 14-Bit, 80Msps ADC	230mW, 71.6dB SNR, 5mm x 5mm QFN Package
LTC5512	DC-3GHz High Signal Level Downconverting Mixer	DC to 3GHz, 21dBm IIP3, Integrated LO Buffer
LTC5515	1.5 GHz to 2.5GHz Direct Conversion Quadrature Demodulator	High IIP3: 20dBm at 1.9GHz, Integrated LO Quadrature Generator
LTC5516	800MHz to 1.5GHz Direct Conversion Quadrature Demodulator	High IIP3: 21.5dBm at 900MHz, Integrated LO Quadrature Generator
LTC5517	40MHz to 900MHz Direct Conversion Quadrature Demodulator	High IIP3: 21dBm at 800MHz, Integrated LO Quadrature Generator
LTC5522	600MHz to 2.7GHz High Linearity Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LTC5527	400MHz to 3.7GHz High Signal Level Downconverting Mixer	4.5V to 5.25V Supply, 23.5dBm IIP3 at 1900MHz, I_{CC} = 78mA, Conversion Gain = 2dB
LTC5579	1.5GHz to 3.8GHz High Linearity Upconverting Mixer	3.3V Supply, 27.3dBm OIP3 at 2.14GHz, Conversion Gain = 2.6dB at 2.14GHz
LTC6400-20	1.8GHz Low Noise, Low Distortion Differential ADC Driver for 300MHz IF	Fixed Gain 10V/V, 2.1nV$\sqrt{Hz}$ Total Input Noise, 3mm × 3mm QFN-16 Package

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