THE DATASHEET OF

LTC1929IG-PG#PBF

www.win-source.net 0086-755-83957316

2-Phase, High Efficiency, Synchronous Step-Down Switching Regulators

FEATURES

- 2-Phase Single Output Controller
- **Reduces Required Input Capacitance and Power Supply Induced Noise**
- **Current Mode Control Ensures Current Sharing**
- Phase-Lockable Fixed Frequency: 150kHz to 300kHz
- **True Remote Sensing Differential Amplifier**
- OPTI-LOOP™ Compensation Improves Transient Response
- **±1% Output Voltage Accuracy**
- **Power Good Output Voltage Monitor (LTC1929-PG)**
- Wide V_{IN} Range: 4V to 36V Operation
- Very Low Dropout Operation: 99% Duty Cycle
- Adjustable Soft-Start Current Ramping
- Internal Current Foldback
- Short-Circuit Shutdown Timer with Defeat Option
- Overvoltage Soft-Latch Eliminates Nuisance Trips
- Available in 28-Lead SSOP Package

APPLICATIONS

- Desktop Computers
- Internet/Network Servers
- Large Memory Arrays
- DC Power Distribution Systems

DESCRIPTION

The LTC®1929/LTC1929-PG are 2-phase, single output, synchronous step-down current mode switching regulator controllers that drive N-channel external power MOSFET stages in a phase-lockable fixed frequency architecture. The 2-phase controllers drive their two output stages out of phase at frequencies up to 300kHz to minimize the RMS ripple currents in both input and output capacitors. The 2-phase technique effectively multiplies the fundamental frequency by two, improving transient response while operating each channel at an optimum frequency for efficiency. Thermal design is also simplified.

An internal differential amplifier provides true remote sensing of the regulated supply's positive and negative output terminals as required by high current applications.

The RUN/SS pin provides soft-start and a defeatable, timed, latched short-circuit shutdown to shut down both channels. Internal foldback current limit provides protection for the external synchronous MOSFETs in the event of an output fault. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values.

LT, LTC and LT are registered trademarks of Linear Technology Corporation.
OPTI-LOOP is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

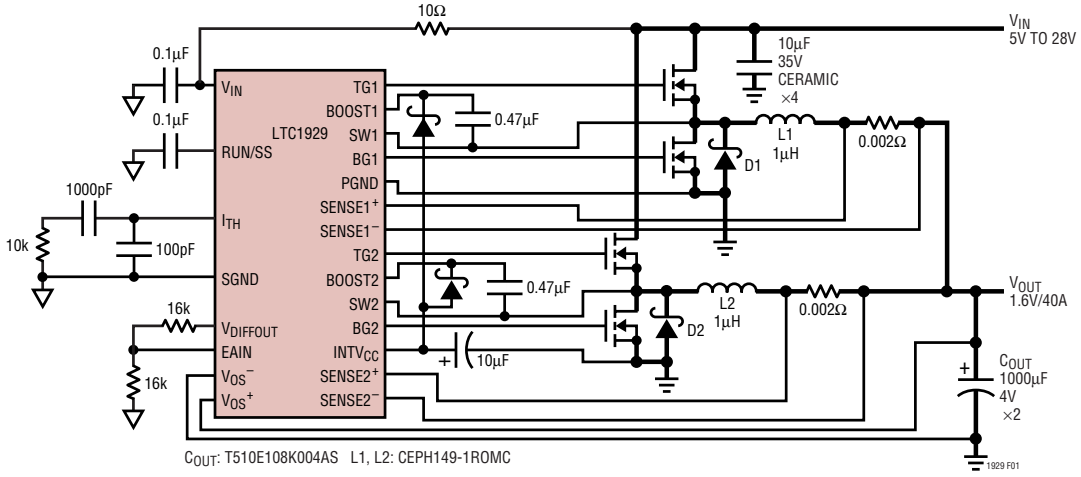


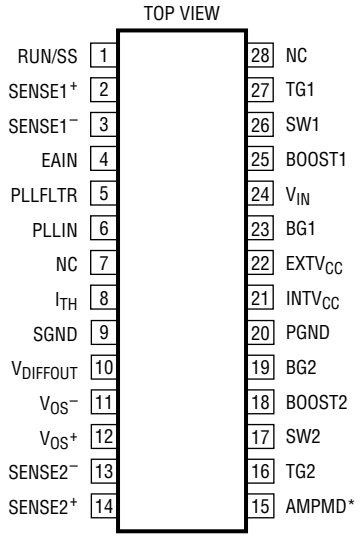
Figure 1. High Current 2-Phase Step-Down Converter

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... 36V to –0.3V
Topside Driver Voltages (BOOST1,2) ..... 42V to –0.3V
Switch Voltage (SW1, 2) ..... 36V to –5 V
SENSE1+, SENSE2+, SENSE1–,
SENSE2– Voltages ..... (1.1)$INTV_{CC}$ to –0.3V
EAIN, V_{OS}^+, V_{OS}^-, $EXTV_{CC}$, $INTV_{CC}$,
RUN/SS, AMPMD Voltages ..... 7V to –0.3V
Boosted Driver Voltage (BOOST-SW) ..... 7V to –0.3V
PLLFLTR, PLLIN, $V_{DIFFOUT}$ Voltages .... $INTV_{CC}$ to –0.3V
I_{TH} Voltage ..... 2.7V to –0.3V
Peak Output Current <1µs(TGL1,2, BG1,2) 3A
$INTV_{CC}$ RMS Output Current 50mA
Operating Ambient Temperature Range
LTC1929C ..... 0°C to 85°C
LTC1929I ..... –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP
*PGOOD ON LTC1929-PG

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER
LTC1929CG
LTC1929CG-PG
LTC1929IG
LTC1929IG-PG

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{EAIN}	Regulated Feedback Voltage	(Note 3); I_{TH} Voltage = 1.2V	●	0.792	0.800	0.808	V
$V_{SENSEMAX}$	Maximum Current Sense Threshold	V_{SENSE}^- = 5V $V_{SENSE1,\,2}$ = 5V, LTC1929 Only	●	62 65	75 75	88 85	mV mV
I_{INEAIN}	Feedback Current	(Note 3)			–5	–50	nA
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 3) Measured in Servo Loop; I_{TH} Voltage = 0.7V Measured in Servo Loop; I_{TH} Voltage = 2V	 ● ●		 0.05 –0.1	 0.5 –0.5	 % %
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 3.6V to 30V (Note 3)			0.002	0.02	%/V
V_{OVL}	Output Overvoltage Threshold	Measured at V_{EAIN}		0.84	0.86	0.88	V
UVLO	Undervoltage Lockout	V_{IN} Ramping Down		3	3.5	4	V
g_m	Transconductance Amplifier g_m	I_{TH} = 1.2V; Sink/Source 5µA; (Note 3)			3		mmho
g_{mOL}	Transconductance Amplifier Gain	I_{TH} = 1.2V; (g_mxZ_L; No Ext Load); (Note 3)			1.5		V/mV
I_Q	Input DC Supply Current Normal Mode Shutdown	(Note 4) $EXTV_{CC}$ Tied to V_{OUT}; V_{OUT} = 5V $V_{RUN/SS}$ = 0V			 470 20	 40	 µA µA
$I_{RUN/SS}$	Soft-Start Charge Current	$V_{RUN/SS}$ = 1.9V		–0.5	–1.2		µA
$V_{RUN/SS}$	RUN/SS Pin ON Threshold	$V_{RUN/SS}$ Rising		1.0	1.5	1.9	V
$V_{RUN/SSLO}$	RUN/SS Pin Latchoff Arming	$V_{RUN/SS}$ Rising from 3V			4.1	4.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SCL}	RUN/SS Discharge Current	Soft Short Condition V_{EAIN} = 0.5V; $V_{RUN/SS}$ = 4.5V		0.5	2.0	4.0	µA
I_{SDLHO}	Shutdown Latch Disable Current	V_{EAIN} = 0.5V			1.6	5	µA
I_{SENSE}	Total Sense Pins Source Current	Each Channel: $V_{SENSE1-,2-}$ = $V_{SENSE1+,2+}$ = 0V		–85	–60		µA
DF_{MAX}	Maximum Duty Factor	In Dropout		98	99.5		%
	Top Gate Transition Time:						
TG1, 2 t_r	Rise Time	C_{LOAD} = 3300pF			30	90	ns
TG1, 2 t_f	Fall Time	C_{LOAD} = 3300pF			40	90	ns
	Bottom Gate Transition Time:						
BG1, 2 t_r	Rise Time	C_{LOAD} = 3300pF			30	90	ns
BG1, 2 t_f	Fall Time	C_{LOAD} = 3300pF			20	90	ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			90		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			90		ns
$t_{ON(MIN)}$	Minimum On-Time	Tested with a Square Wave (Note 6)			180		ns
Internal V_{CC} Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 30V; V_{EXTVCC} = 4V		4.8	5.0	5.2	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0 to 20mA; V_{EXTVCC} = 4V			0.2	1.0	%
V_{LDO} EXT	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA; V_{EXTVCC} = 5V			120	240	mV
V_{LDO} EXT-PG	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA, V_{EXTVCC} = 5V, LTC1929-PG			80	160	mV
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{CC} = 20mA, $EXTV_{CC}$ Ramping Positive	●	4.5	4.7		V
V_{LDOHYS}	$EXTV_{CC}$ Switchover Hysteresis	I_{CC} = 20mA, $EXTV_{CC}$ Ramping Negative			0.2		V
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	$V_{PLLFLTR}$ = 1.2V		190	220	250	kHz
f_{LOW}	Lowest Frequency	$V_{PLLFLTR}$ = 0V		120	140	160	kHz
f_{HIGH}	Highest Frequency	$V_{PLLFLTR}$ ≥ 2.4V		280	310	360	kHz
R_{PLLIN}	PLLIN Input Resistance				50		kΩ
$I_{PLLFLTR}$	Phase Detector Output Current						
	Sinking Capability	f_{PLLIN} < f_{OSC}			–15		µA
	Sourcing Capability	f_{PLLIN} > f_{OSC}			15		µA
R_{RELPHS}	Controller 2-Controller 1 Phase				180		Deg
PGOOD Output (LTC1929-PG Only)							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
V_{PG}	PGOOD Trip Level	V_{EAIN} with Respect to Set Output Voltage					
		V_{EAIN} Ramping Negative		–6	–7.5	–9.5	%
		V_{EAIN} Ramping Positive		6	7.5	9.5	%
Differential Amplifier/Op Amp Gain Block (Note 5)							
A_{DA}	Gain	Differential Amp Mode		0.995	1	1.005	V/V
$CMRR_{DA}$	Common Mode Rejection Ratio	Differential Amp Mode; 0V < V_{CM} < 5V		46	55		dB
R_{IN}	Input Resistance	Differential Amp Mode; Measured at V_{OS}+ Input			80		kΩ
V_{OS}	Input Offset Voltage	Op Amp Mode; V_{CM} = 2.5V; $V_{DIFFOUT}$ = 5V; $I_{DIFFOUT}$ = 1mA (LTC1929 Only)				6	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_B	Input Bias Current	Op Amp Mode (LTC1929 Only)			30	200	nA
A_{OL}	Open Loop DC Gain	Op Amp Mode; 0.7V ≤ $V_{DIFFOUT}$ < 10V (LTC1929 Only)			5000		V/mV
V_{CM}	Common Mode Input Voltage Range	Op Amp Mode (LTC1929 Only)		0		3	V
$CMRR_{OA}$	Common Mode Rejection Ratio	Op Amp Mode; 0V < V_{CM} < 3V (LTC1929 Only)		70	90		dB
$PSRR_{OA}$	Power Supply Rejection Ratio	Op Amp Mode; 6V < V_{IN} < 30V (LTC1929 Only)		70	90		dB
I_{CL}	Maximum Output Current	Op Amp Mode; $V_{DIFFOUT}$ = 0V (LTC1929 Only)		10	35		mA
$V_{O(MAX)}$	Maximum Output Voltage	Op Amp Mode; $I_{DIFFOUT}$ = 1mA (LTC1929 Only)		10	11		V
GBW	Gain-Bandwidth Product	Op Amp Mode; $I_{DIFFOUT}$ = 1mA (LTC1929 Only)			2		MHz
SR	Slew Rate	Op Amp Mode; R_L = 2k (LTC1929 Only)			5		V/µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC1929CG: $T_J = T_A + (P_D \bullet 95°C/W)$

Note 3: The LTC1929 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{EAIN}.

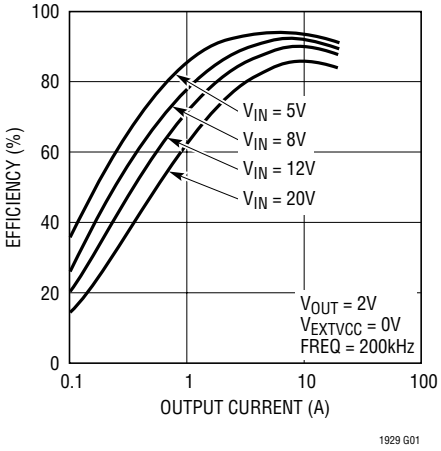
Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 5: When the AMPMD pin is high (default for the LTC1929-PG), the LTC1929 IC pins are connected directly to the internal op amp inputs. When the AMPMD pin is low, internal MOSFET switches connect four 40k resistors around the op amp to create a standard unity-gain differential amp.

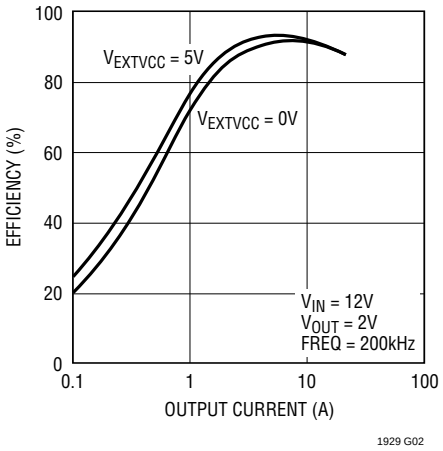
Note 6: Minimum on-time condition corresponds to the on inductor peak-to-peak ripple current ≥40% of I_{MAX} (see minimum on-time considerations in the Applications Information section).

TYPICAL PERFORMANCE CHARACTERISTICS

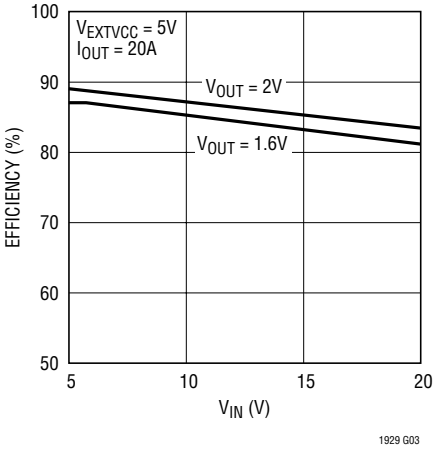
Efficiency vs Output Current (Figure 13)



Efficiency vs Output Current (Figure 13)

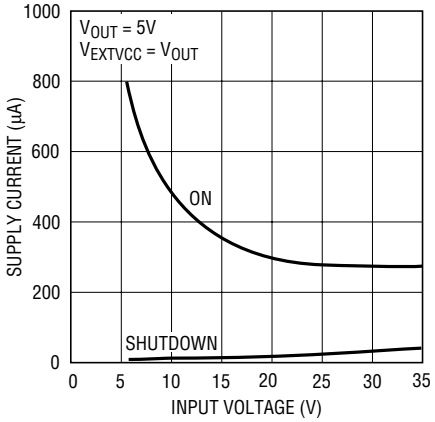


Efficiency vs V_{IN} (Figure 13)



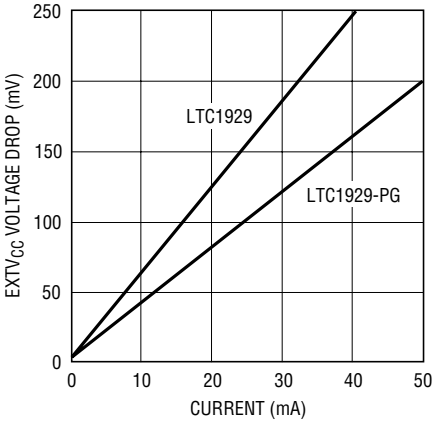
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Input Voltage and Mode



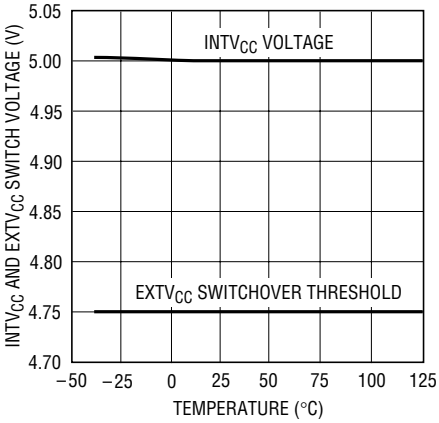
1929 G04

$EXTV_{CC}$ Voltage Drop



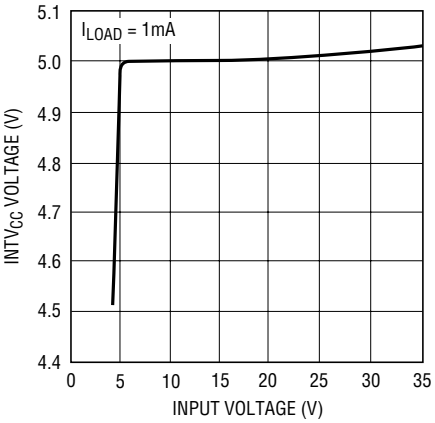
1929 G05

$INTV_{CC}$ and $EXTV_{CC}$ Switch Voltage vs Temperature



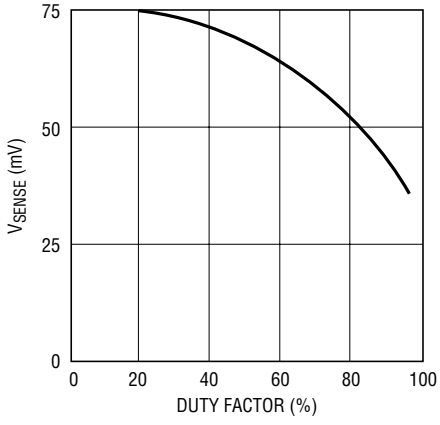
1929 G06

Internal 5V LDO Line Reg



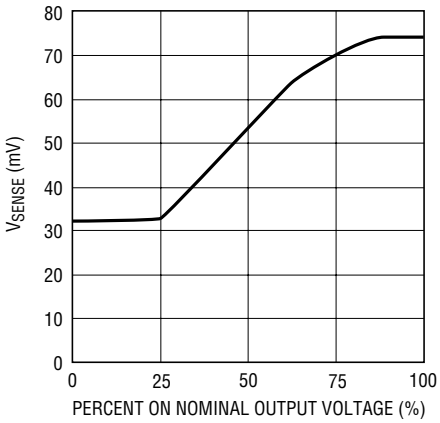
1929 G07

Maximum Current Sense Threshold vs Duty Factor



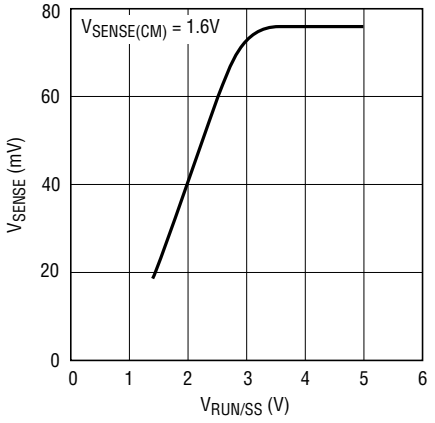
1929 G08

Maximum Current Sense Threshold vs Percent on Nominal Output Voltage (Foldback)



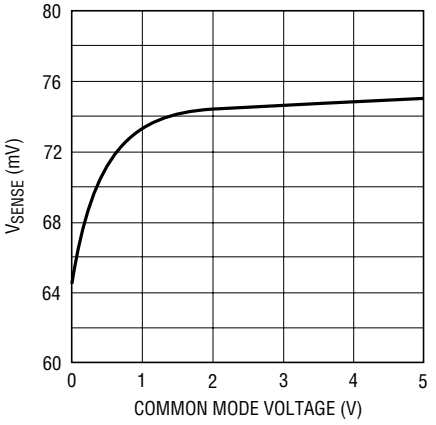
1929 G09

Maximum Current Sense Threshold vs $V_{RUN/SS}$ (Soft-Start)



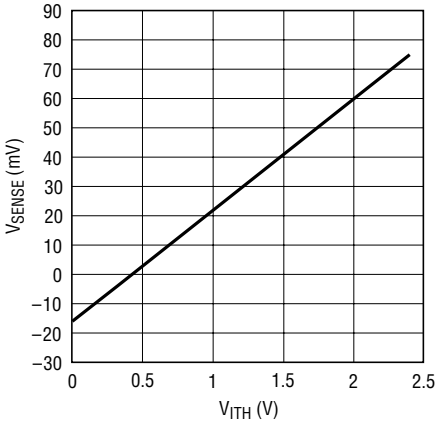
1929 G10

Maximum Current Sense Threshold vs Sense Common Mode Voltage



1929 G11

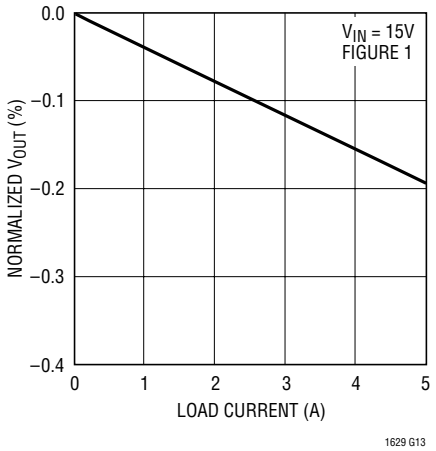
Current Sense Threshold vs I_{TH} Voltage



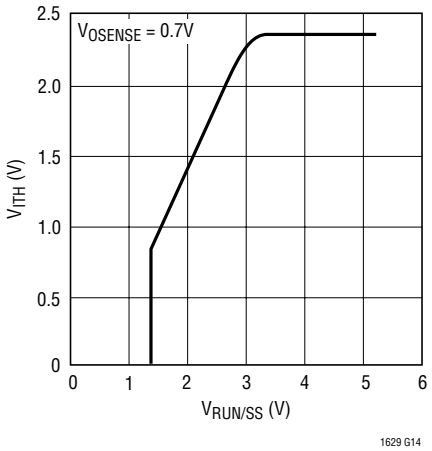
1929 G12

TYPICAL PERFORMANCE CHARACTERISTICS

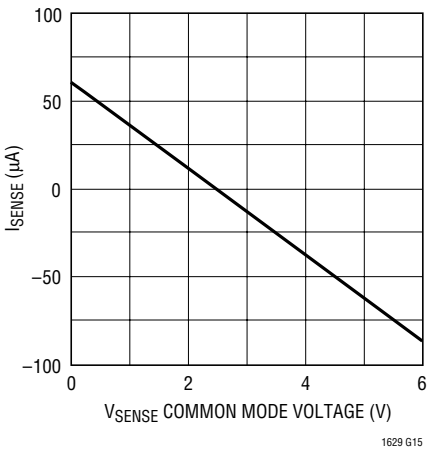
Load Regulation



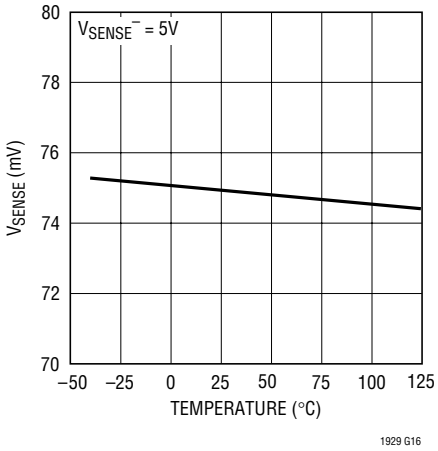
VITH vs VRUN/SS



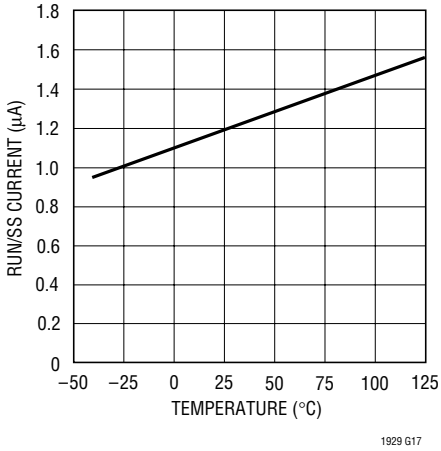
SENSE Pins Total Source Current



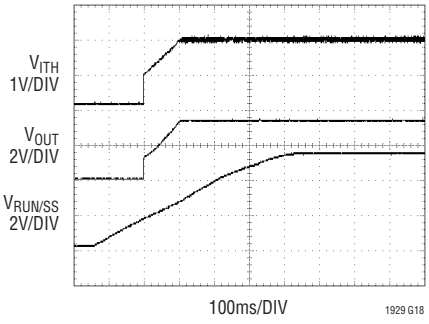
Maximum Current Sense Threshold vs Temperature



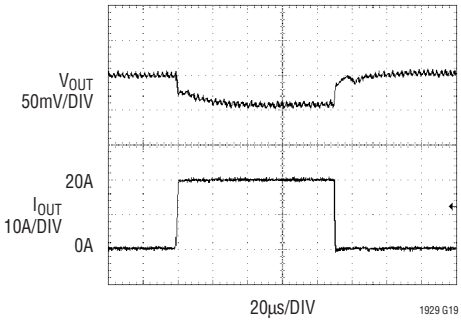
RUN/SS Current vs Temperature



Soft-Start (Figure 13)

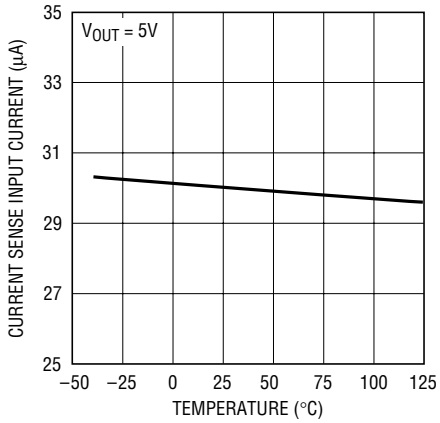


Load Step (Figure 13)

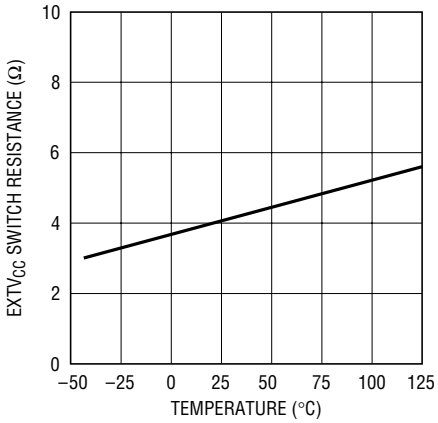


TYPICAL PERFORMANCE CHARACTERISTICS

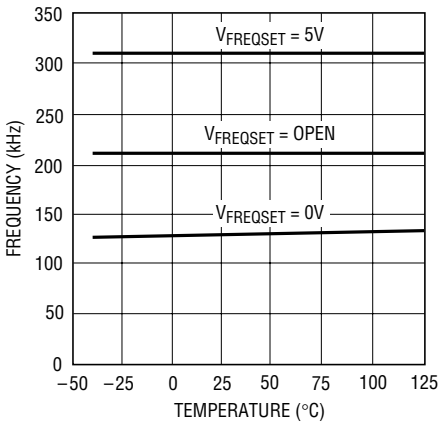
Current SENSE Pin Input Current vs Temperature



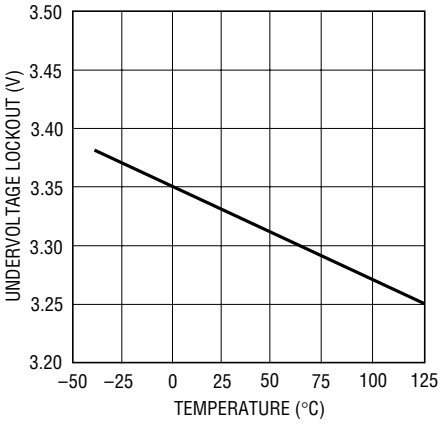
$EXTV_{CC}$ Switch Resistance vs Temperature



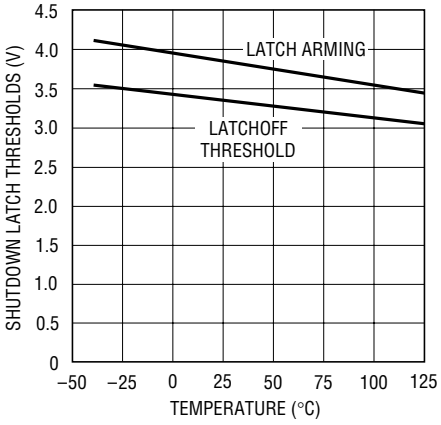
Oscillator Frequency vs Temperature



Undervoltage Lockout vs Temperature



$V_{RUN/SS}$ Shutdown Latch Thresholds vs Temperature



PIN FUNCTIONS

RUN/SS (Pin 1): Combination of Soft-Start, Run Control Input and Short-Circuit Detection Timer. A capacitor to ground at this pin sets the ramp time to full current output. Forcing this pin below 0.8V causes the IC to shut down all internal circuitry. All functions are disabled in shutdown.

SENSE1$^+$, SENSE2$^+$ (Pins 2,14): The (+) Input to the Differential Current Comparators. The I_{TH} pin voltage and built-in offsets between SENSE$^-$ and SENSE$^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

SENSE1$^-$, SENSE2$^-$ (Pins 3, 13): The (–) Input to the Differential Current Comparators.

EAIN (Pin 4): Input to the Error Amplifier that compares the feedback voltage to the internal 0.8V reference voltage. This pin is normally connected to a resistive divider from the output of the differential amplifier (DIFFOUT).

PLLFLTR (Pin 5): The Phase-Locked Loop's Low Pass Filter is tied to this pin. Alternatively, this pin can be driven with an AC or DC voltage source to vary the frequency of the internal oscillator.

PLLIN (Pin 6): External Synchronization Input to Phase Detector. This pin is internally terminated to SGND with 50kΩ. The phase-locked loop will force the rising top gate signal of controller 1 to be synchronized with the rising edge of the PLLIN signal.

NC (Pins 7, 28): Not connected.

I_{TH} (Pin 8): Error Amplifier Output and Switching Regulator Compensation Point. Both current comparator's thresholds increase with this control voltage. The normal voltage range of this pin is from 0V to 2.4V

SGND (Pin 9): Signal Ground, common to both controllers, must be routed separately from the input switched current ground path to the common (–) terminal(s) of the C_{OUT} capacitor(s).

$V_{DIFFOUT}$ (Pin 10): Output of a Differential Amplifier that provides true remote output voltage sensing. This pin normally drives an external resistive divider that sets the output voltage.

V_{OS}^-, V_{OS}^+ (Pins 11, 12): Inputs to an Operational Amplifier. Internal precision resistors capable of being electronically switched in or out can configure it as a differential amplifier (default for the LTC1929-PG) or an uncommitted Op Amp.

AMPMD (Pin 15): (LTC1929 Only) This Logic Input pin controls the connections of internal precision resistors that configure the operational amplifier as a unity-gain differential amplifier.

PGOOD (Pin 15): (LTC1929-PG Only) Open-Drain Logic Output. PGOOD is pulled to ground when the voltage on the EAIN pin is not within ±7.5% of its set point.

TG2, TG1 (Pins 16, 27): High Current Gate Drives for Top N-Channel MOSFETS. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW.

SW2, SW1 (Pins 17, 26): Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN}.

BOOST2, BOOST1 (Pins 18, 25): Bootstrapped Supplies to the Topside Floating Drivers. Capacitors are connected between the Boost and Switch pins, and Schottky diodes are tied between the Boost and $INTV_{CC}$ pins.

BG2, BG1 (Pins 19, 23): Voltage Swing High Current Gate Drives for Bottom Synchronous N-Channel MOSFETS. Voltage swing at these pins is from ground to $INTV_{CC}$.

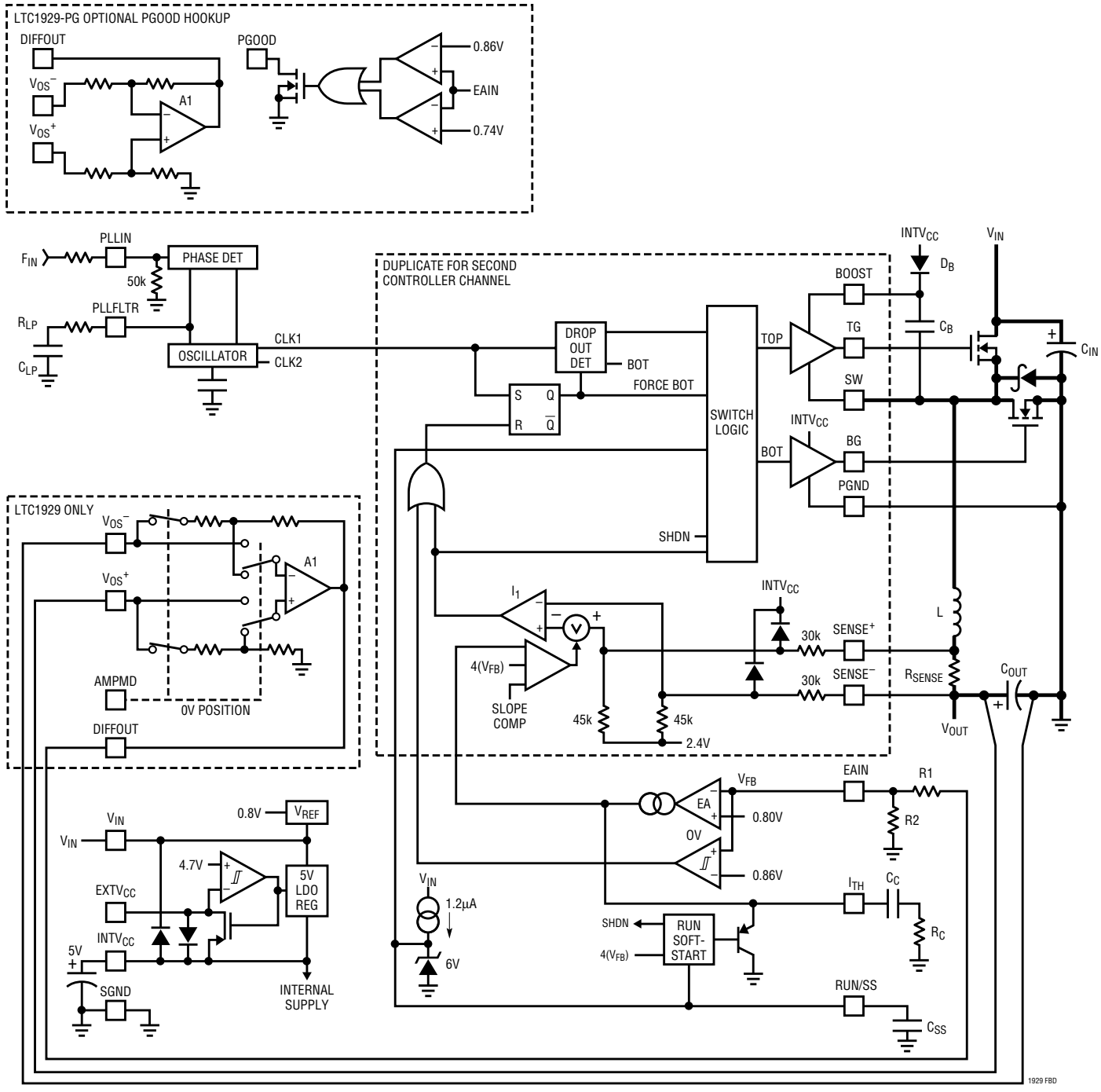
PGND (Pin 20): Driver Power Ground. Connects to sources of bottom N-channel MOSFETS and the (–) terminals of C_{IN}.

$INTV_{CC}$ (Pin 21): Output of the Internal 5V Linear Low Dropout Regulator and the $EXTV_{CC}$ Switch. The driver and control circuits are powered from this voltage source. Decouple to power ground with a 1µF ceramic capacitor placed directly adjacent to the IC and minimum of 4.7µF additional tantalum or other low ESR capacitor.

$EXTV_{CC}$ (Pin 22): External Power Input to an Internal Switch . This switch closes and supplies $INTV_{CC}$, bypassing the internal low dropout regulator whenever $EXTV_{CC}$ is higher than 4.7V. See $EXTV_{CC}$ Connection in the Applications Information section. Do not exceed 7V on this pin and ensure $V_{EXTVCC} \leq V_{IN}$.

V_{IN} (Pin 24): Main Supply Pin. Should be closely decoupled to the IC's signal ground pin.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC1929 uses a constant frequency, current mode step-down architecture with inherent current sharing. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the main current comparator, I_1, resets the RS latch. The peak inductor current at which I_1 resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier EA. The differential amplifier, A1, produces a signal equal to the differential voltage sensed across the output capacitor but re-references it to the internal signal ground (SGND) reference. The EAIN pin receives a portion of this voltage feedback signal at the DIFFOUT pin which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in the EAIN pin voltage relative to the 0.8V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on for the rest of the period.

The top MOSFET drivers are biased from floating bootstrap capacitor C_B, which normally is recharged during each off cycle through an external Schottky diode. When V_{IN} decreases to a voltage close to V_{OUT}, however, the loop may enter dropout and attempt to turn on the top MOSFET continuously. A dropout detector detects this condition and forces the top MOSFET to turn off for about 400ns every 10th cycle to recharge the bootstrap capacitor.

The main control loop is shut down by pulling Pin 1 (RUN/SS) low. Releasing RUN/SS allows an internal 1.2µA current source to charge soft-start capacitor C_{SS}. When C_{SS} reaches 1.5V, the main control loop is enabled with the I_{TH} voltage clamped at approximately 30% of its maximum value. As C_{SS} continues to charge, I_{TH} is gradually released allowing normal operation to resume. When the RUN/SS pin is low, all LTC1929 functions are shut down. If V_{OUT} has not reached 70% of its nominal value when C_{SS} has charged to 4.1V, an overcurrent latchoff can be invoked as described in the Applications Information section.

Low Current Operation

The LTC1929 operates in a continuous, PWM control mode. The resulting operation at low output currents optimizes transient response at the expense of substantial negative inductor current during the latter part of the period. The level of ripple current is determined by the inductor value, input voltage, output voltage, and frequency of operation.

Frequency Synchronization

The phase-locked loop allows the internal oscillator to be synchronized to an external source via the PLLIN pin. The output of the phase detector at the PLLFLTR pin is also the DC frequency control input of the oscillator that operates over a 140kHz to 310kHz range corresponding to a DC voltage input from 0V to 2.4V. When locked, the PLL aligns the turn on of the top MOSFET to the rising edge of the synchronizing signal. When PLLIN is left open, the PLLFLTR pin goes low, forcing the oscillator to minimum frequency.

Input capacitance ESR requirements and efficiency losses are substantially reduced because the peak current drawn from the input capacitor is effectively divided by two and power loss is proportional to the RMS current squared. A two stage, single output voltage implementation can reduce input path power loss by 75% and radically reduce the required RMS current rating of the input capacitor(s).

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most of the IC circuitry is derived from $INTV_{CC}$. When the $EXTV_{CC}$ pin is left open, an internal 5V low dropout regulator supplies $INTV_{CC}$ power. If the $EXTV_{CC}$ pin is taken above 4.7V, the 5V regulator is turned off and an internal switch is turned on connecting $EXTV_{CC}$ to $INTV_{CC}$. This allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as the output of the regulator itself or a secondary winding, as described in the Applications Information section. An external Schottky diode can be used to minimize the voltage drop from $EXTV_{CC}$ to $INTV_{CC}$ in applications requiring greater than the specified $INTV_{CC}$ current. Voltages up to 7V can be applied to $EXTV_{CC}$ for additional gate drive capability.

OPERATION (Refer to Functional Diagram)

Differential Amplifier

This amplifier provides true differential output voltage sensing. Sensing both V_{OUT}^+ and V_{OUT}^- benefits regulation in high current applications and/or applications having electrical interconnection losses. The AMPMD pin (LTC1929 only) allows selection of internal, precision feedback resistors for high common mode rejection differencing applications, or direct access to the actual amplifier inputs without these internal feedback resistors for other applications. The AMPMD pin is grounded to connect the internal precision resistors in a unity-gain differencing application (default for the LTC1929-PG), or tied to the $INTV_{CC}$ pin to bypass the internal resistors and make the amplifier inputs directly available. The amplifier is a unity-gain stable, 2MHz gain-bandwidth, >120dB open-loop gain design. The amplifier has an output slew rate of 5V/µs and is capable of driving capacitive loads with an output RMS current typically up to 25mA. The amplifier is not capable of sinking current and therefore must be resistively loaded to do so.

Power Good (PGOOD) Pin (LTC1929-PG Only)

The PGOOD pin is connected to an open drain of a MOSFET. The MOSFET turns on and pulls the pin low when the output is not within ±7.5% of its nominal output level as determined by its resistive feedback divider. When the output meets the ±7.5% requirement, the MOSFET is turned off within 10µs and the pin is allowed to be pulled up by an external source.

Short-Circuit Detection

The RUN/SS capacitor is used initially to limit the inrush current from the input power source. Once the controllers have been given time, as determined by the capacitor on the RUN/SS pin, to charge up the output capacitors and provide full load current, the RUN/SS capacitor is then used as a short-circuit timeout circuit. If the output voltage falls to less than 70% of its nominal output voltage the RUN/SS capacitor begins discharging assuming that the output is in a severe overcurrent and/or short-circuit condition. If the condition lasts for a long enough period as determined by the size of the RUN/SS capacitor, the controller will be shut down until the RUN/SS pin voltage is recycled. This built-in latchoff can be overidden by providing a current >5µA at a compliance of 5V to the RUN/SS pin. This current shortens the soft-start period but also prevents net discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit condition. Foldback current limiting is activated when the output voltage falls below 70% of its nominal level whether or not the short-circuit latchoff circuit is enabled.

APPLICATIONS INFORMATION

The basic LTC1929 application circuit is shown in Figure 1 on the first page. External component selection is driven by the load requirement, and begins with the selection of $R_{SENSE1, 2}$. Once $R_{SENSE1, 2}$ are known, L1 and L2 can be chosen. Next, the power MOSFETs and D1 and D2 are selected. The operating frequency and the inductor are chosen based mainly on the amount of ripple current. Finally, C_{IN} is selected for its ability to handle the input ripple current (that PolyPhase™ operation minimizes) and C_{OUT} is chosen with low enough ESR to meet the output ripple voltage and load step specifications (also minimized with PolyPhase). Current mode architecture provides inherent current sharing between output stages. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 28V (limited by the external MOSFETs).

R_{SENSE} Selection For Output Current

$R_{SENSE1, 2}$ are chosen based on the required output current. The LTC1929 current comparator has a maximum threshold of $75mV/R_{SENSE}$ and an input common mode range of SGND to 1.1($INTV_{CC}$). The current comparator threshold sets the peak inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Allowing a margin for variations in the LTC1929 and external component values yields:

$$R_{SENSE} = 2(50mV/I_{MAX})$$

PolyPhase is a trademark of Linear Technology Corporation.

APPLICATIONS INFORMATION

When using the controller in very low dropout conditions, the maximum output current level will be reduced due to internal compensation required to meet stability criterion for buck regulators operating at greater than 50% duty factor. A curve is provided to estimate this reduction in peak output current level depending upon the operating duty factor.

Operating Frequency

The LTC1929 uses a constant frequency, phase-lockable architecture with the frequency determined by an internal capacitor. This capacitor is charged by a fixed current plus an additional current which is proportional to the voltage applied to the PLLFLTR pin. Refer to Phase-Locked Loop and Frequency Synchronization in the Applications Information section for additional information.

A graph for the voltage applied to the PLLFLTR pin vs frequency is given in Figure 2. As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum switching frequency is approximately 310kHz.

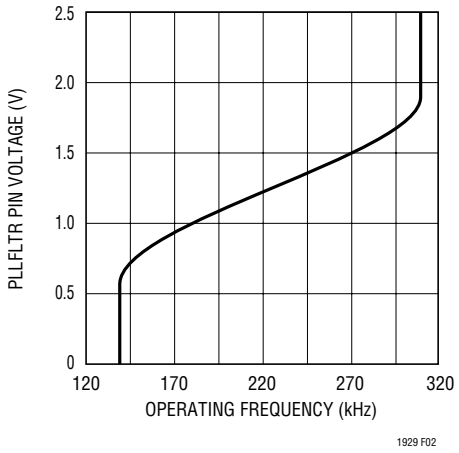


Figure 2. Operating Frequency vs $V_{PLLFLTR}$

Inductor Value Calculation and Output Ripple Current

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge and transition losses. In addition to this basic tradeoff, the effect of inductor value on ripple current and low current operation must also be considered. The PolyPhase approach reduces both input and output ripple currents while optimizing individual output stages to run at a lower fundamental frequency, enhancing efficiency.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L per individual section, N, decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{V_{OUT}}{fL}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

where f is the individual output stage operating frequency.

In a 2-phase converter, the net ripple current seen by the output capacitor is much smaller than the individual inductor ripple currents due to the ripple cancellation. The details on how to calculate the net output ripple current can be found in Application Note 77.

Figure 3 shows the net ripple current seen by the output capacitors for the 1- and 2-phase configurations. The output ripple current is plotted for a fixed output voltage as the duty factor is varied between 10% and 90% on the x-axis. The output ripple current is normalized against the inductor ripple current at zero duty factor. The graph can be used in place of tedious calculations, simplifying the design process.

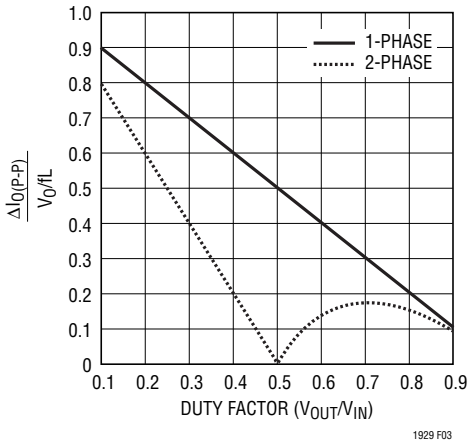


Figure 3. Normalized Output Ripple Current vs Duty Factor [$I_{RMS} \approx 0.3\ (\Delta I_{O(P-P)})$]

APPLICATIONS INFORMATION

Accepting larger values of ΔI_L allows the use of low inductances, but can result in higher output voltage ripple. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{OUT})/2$, where I_{OUT} is the total load current. Remember, the maximum ΔI_L occurs at the maximum input voltage. The individual inductor ripple currents are determined by the inductor, input and output voltages.

Inductor Core Selection

Once the values for L1 and L2 are known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. *Do not allow the core to saturate!*

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they lack a bobbin, mounting is more difficult. However, designs for surface mount are available which do not increase the height significantly.

Power MOSFET, D1 and D2 Selection

Two external power MOSFETs must be selected for each output stage with the LTC1929: One N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected ($V_{IN} < 5V$); then, sublogic-level threshold MOSFETs ($V_{GS(TH)} < 3V$) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage, and maximum output current. When the LTC1929 is operating in continuous mode the duty factors for the top and bottom MOSFETs of each output stage are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(\frac{I_{MAX}}{2}\right)^2(1+\delta)R_{DS(ON)} + k(V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(C_{RSS})(f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(\frac{I_{MAX}}{2}\right)^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current.

Both MOSFETs have I^2R losses but the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actual provides higher efficiency. The

Kool Mμ is a registered trademark of Magnetics, Inc.

APPLICATIONS INFORMATION

synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs. Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET characteristics. The constant k = 1.7 can be used to estimate the contributions of the two terms in the main switch dissipation equation.

The Schottky diodes, D1 and D2 shown in Figure 1 conduct during the dead-time between the conduction of the two large power MOSFETs. This helps prevent the body diode of the bottom MOSFET from turning on, storing charge during the dead-time, and requiring a reverse recovery period which would reduce efficiency. A 1A to 3A (depending on output current) Schottky diode is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of each top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. A low ESR input capacitor sized for the maximum RMS current must be used. The details of a close form equation can be found in Application Note 77. Figure 4 shows the input capacitor ripple current for a 2-phase configuration with the output voltage fixed and input voltage varied. The input ripple current is normalized against the DC output current. The graph can be used in place of tedious calculations. The minimum input ripple current can be achieved when the input voltage is twice the output voltage. The minimum is not quite zero due to inductor ripple current.

In the graph of Figure 4, the local maximum input RMS capacitor currents are reached when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{2k-1}{4} \qquad \text{where } k = 1, 2.$$

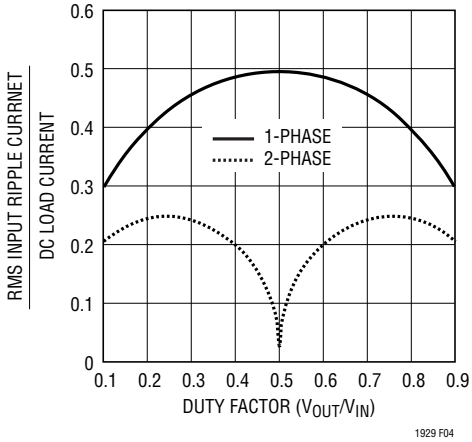


Figure 4. Normalized RMS Input Ripple Current vs Duty Factor for 1 and 2 Output Stages

These worst-case conditions are commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the capacitor manufacturer if there is any question.

It is important to note that the efficiency loss is proportional to the input RMS current *squared* and therefore a 2-stage implementation results in 75% less power loss when compared to a single phase design. Battery/input protection fuse resistance (if used), PC board trace and connector resistance losses are also reduced by the reduction of the input ripple current in a 2-phase system. The required amount of input capacitance is further reduced by the factor, 2, due to the effective increase in the frequency of the current pulses.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirements. The steady state output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_{RIPPLE}\left(ESR + \frac{1}{16fC_{OUT}}\right)$$

APPLICATIONS INFORMATION

Where f = operating frequency of each stage, C_{OUT} = output capacitance and ΔI_{RIPPLE} = combined inductor ripple currents.

The output ripple varies with input voltage since ΔI_L is a function of input voltage. The output ripple will be less than 50mV at max V_{IN} with $\Delta I_L = 0.4I_{OUT(MAX)}/2$ assuming:

C_{OUT} required ESR < $4(R_{SENSE})$ and

$C_{OUT} > 1/(16f)(R_{SENSE})$

The emergence of very low ESR capacitors in small, surface mount packages makes very physically small implementations possible. The ability to externally compensate the switching regulator loop using the I_{TH} pin (OPTI-LOOP compensation) allows a much wider selection of output capacitor types. OPTI-LOOP compensation effectively removes constraints on output capacitor ESR. The impedance characteristics of each capacitor type are significantly different than an ideal capacitor and therefore require accurate modeling or bench evaluation during design.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo and the Panasonic SP surface mount types have the lowest (ESR)(size) product of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON type capacitors is recommended to reduce the inductance effects.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent choices are the AVX TPS, AVX TPSV or the KEMET T510 series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, Nichicon PL series and Sprague 595D series. Consult the manufacturer for other specific recommendations. A combination of capacitors will often result in maximizing performance and minimizing overall cost and size.

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 5V at the $INTV_{CC}$ pin from the V_{IN} supply pin. The $INTV_{CC}$ regulator powers the drivers and internal circuitry of the LTC1929. The $INTV_{CC}$ pin regulator can supply up to 50mA peak and must be bypassed to power ground with a minimum of 4.7µF tantalum or electrolytic capacitor. An additional 1µF ceramic capacitor placed very close to the IC is recommended due to the extremely high instantaneous currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC1929 to be exceeded. The supply current is dominated by the gate charge supply current, in addition to the current drawn from the differential amplifier output. The gate charge is dependent on operating frequency as discussed in the Efficiency Considerations section. The supply current can either be supplied by the internal 5V regulator or via the $EXTV_{CC}$ pin. When the voltage applied to the $EXTV_{CC}$ pin is less than 4.7V, all of the $INTV_{CC}$ load current is supplied by the internal 5V linear regulator. Power dissipation for the IC is higher in this case by $(I_{IN})(V_{IN} - INTV_{CC})$ and efficiency is lowered. The junction temperature can be estimated by using the equations given in Note 1 of the Electrical Characteristics. For example, the LTC1929 V_{IN} current is limited to less than 24mA from a 24V supply:

$T_J = 70°C + (24mA)(24V)(95°C/W) = 125°C$

Use of the $EXTV_{CC}$ pin reduces the junction temperature to:

$T_J = 70°C + (24mA)(5V)(95°C/W) = 81.4°C$

The input supply current should be measured while the controller is operating in continuous mode at maximum V_{IN} and the power dissipation calculated in order to prevent the maximum junction temperature from being exceeded.

APPLICATIONS INFORMATION

$EXTV_{CC}$ Connection

The LTC1929 contains an internal P-channel MOSFET switch connected between the $EXTV_{CC}$ and $INTV_{CC}$ pins. When the voltage applied to $EXTV_{CC}$ rises above 4.7V, the internal regulator is turned off and the switch closes, connecting the $EXTV_{CC}$ pin to the $INTV_{CC}$ pin thereby supplying internal and MOSFET gate driving power. The switch remains closed as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. This allows the MOSFET driver and control power to be derived from the output during normal operation ($4.7V < V_{EXTVCC} < 7V$) and from the internal regulator when the output is out of regulation (start-up, short-circuit). Do not apply greater than 7V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} < V_{IN} + 0.3V$ when using the application circuits shown. If an external voltage source is applied to the $EXTV_{CC}$ pin when the V_{IN} supply is not present, a diode can be placed in series with the LTC1929's V_{IN} pin and a Schottky diode between the $EXTV_{CC}$ and the V_{IN} pin, to prevent current from backfeeding V_{IN}.

Significant efficiency gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by the ratio: (Duty Factor)/(Efficiency). For 5V regulators this means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. However, for 3.3V and other lower voltage regulators, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 5V regulator resulting in a significant efficiency penalty at high input voltages.

2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.

3. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5V to 7V range, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements.

4. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage which has been boosted to greater than 4.7V but less than 7V. This can be done with either the inductive boost winding as shown in Figure 5a or the capacitive charge pump shown in Figure 5b. The charge pump has the advantage of simple magnetics.

Topside MOSFET Driver Supply (C_B, D_B) (Refer to Functional Diagram)

External bootstrap capacitors C_{B1} and C_{B2} connected to the BOOST1 and BOOST2 pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged though diode D_B from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET turns on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage,

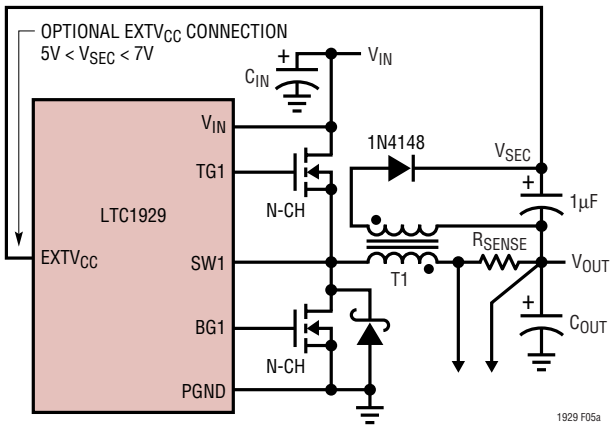


Figure 5a. Secondary Output Loop with $EXTV_{CC}$ Connection

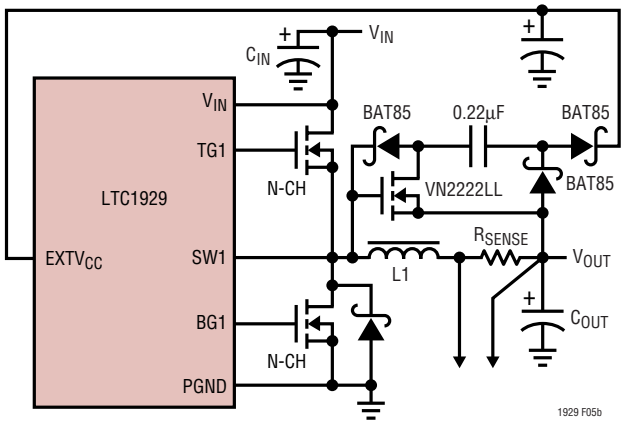


Figure 5b. Capacitive Charge Pump for $EXTV_{CC}$

APPLICATIONS INFORMATION

SW, rises to V_{IN} and the BOOST pin rises to $V_{IN} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 30 to 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of D_B must be greater than $V_{IN(MAX)}$.

The final arbiter when defining the best gate drive amplitude level will be the input supply current. If a change is made that decreases input current, the efficiency has improved. If the input current does not change then the efficiency has not changed either.

Output Voltage

The LTC1929 has a true remote voltage sense capability. The sensing connections should be returned from the load back to the differential amplifier's inputs through a common, tightly coupled pair of PC traces. The differential amplifier rejects common mode signals capacitively or inductively radiated into the feedback PC traces as well as ground loop disturbances. The differential amplifier output signal is divided down and compared with the internal precision 0.8V voltage reference by the error amplifier.

The differential amplifier can be used in either of two configurations according to the voltage applied to the AMPMD pin (LTC1929 only). The first configuration, with the connections illustrated in the Functional Diagram, utilizes a set of internal precision resistors to enable precision instrumentation-type measurement of the output voltage. This configuration is activated when the AMPMD pin is tied to ground and is the default for the LTC1929-PG. When the AMPMD pin is tied to $INTV_{CC}$, the resistors are disconnected and the amplifier inputs are made directly available. The amplifier can then be used as a general purpose op amp. The amplifier has a 0V to 3V common mode input range limitation due to the internal switching of its inputs. The output is an NPN emitter follower without any internal pull-down current. A DC resistive load to ground is required in order to sink current. The output will swing from 0V to 10V ($V_{IN} \geq V_{DIFFOUT} + 2V$).

Soft-Start/Run Function

The RUN/SS pin provides three functions: 1) Run/Shutdown, 2) soft-start and 3) a defeatable short-circuit latchoff timer. Soft-start reduces the input power sources' surge currents by gradually increasing the controller's current limit $I_{TH(MAX)}$. The latchoff timer prevents very short, extreme load transients from tripping the overcurrent latch. A small pull-up current (>5μA) supplied to the RUN/SS pin will prevent the overcurrent latch from operating. The following explanation describes how the functions operate.

An internal 1.2μA current source charges up the C_{SS} capacitor. When the voltage on RUN/SS reaches 1.5V, the controller is permitted to start operating. As the voltage on RUN/SS increases from 1.5V to 3.0V, the internal current limit is increased from $25mV/R_{SENSE}$ to $75mV/R_{SENSE}$. The output current limit ramps up slowly, taking an additional 1.4s/μF to reach full current. The output current thus ramps up slowly, reducing the starting surge current required from the input power supply. If RUN/SS has been pulled all the way to ground there is a delay before starting of approximately:

$$t_{DELAY} = \frac{1.5V}{1.2\mu A} C_{SS} = \left(1.25s / \mu F\right) C_{SS}$$

The time for the output current to ramp up is then:

$$t_{IRAMP} = \frac{3V - 1.5V}{1.2\mu A} C_{SS} = \left(1.25s / \mu F\right) C_{SS}$$

By pulling both RUN/SS controller pins below 0.8V the LTC1929 is put into low current shutdown ($I_Q < 40\mu A$). The RUN/SS pins can be driven directly from logic as shown in Figure 6. Diode D1 in Figure 6 reduces the start delay but allows C_{SS} to ramp up slowly providing the soft-start function. The RUN/SS pin has an internal 6V zener clamp (see Functional Diagram).

Fault Conditions: Overcurrent Latchoff

The RUN/SS pin also provides the ability to latch off the controllers when an overcurrent condition is detected. The RUN/SS capacitor, C_{SS}, is used initially to limit the inrush current of both controllers. After the controllers have been started and been given adequate time to charge up the output capacitors and provide full load current, the RUN/SS capacitor is used for a short-circuit timer. If the output voltage falls to less than 70% of its nominal value,

APPLICATIONS INFORMATION

after C_{SS} reaches 4.1V, C_{SS} begins discharging on the assumption that the output is in an overcurrent condition. If the condition lasts for a long enough period as determined by the size of C_{SS}, the controller will be shut down until the RUN/SS pin voltage is recycled. If the overload occurs during start-up, the time can be approximated by:

$$t_{LO1} \approx (C_{SS} \bullet 0.6V)/(1.2\mu A) = 5 \bullet 10^5 (C_{SS})$$

If the overload occurs after start-up the voltage on the RUN/SS capacitor will continue charging and will provide additional time before latching off:

$$t_{LO2} \approx (C_{SS} \bullet 3V)/(1.2\mu A) = 2.5 \bullet 10^6 (C_{SS})$$

This built-in overcurrent latchoff can be overridden by providing a pull-up resistor, R_{SS}, to the RUN/SS pin as shown in Figure 6. This resistance shortens the soft-start period and prevents the discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit condition. When deriving the 5µA current from V_{IN} as in the figure, current latchoff is always defeated. The diode connecting of this pull-up resistor to $INTV_{CC}$, as in Figure 6, eliminates any extra supply current during shutdown while eliminating the $INTV_{CC}$ loading from preventing controller start-up.

Why should you defeat current latchoff? During the prototyping stage of a design, there may be a problem with noise pickup or poor layout causing the protection circuit to latch off the controller. Defeating this feature allows troubleshooting of the circuit and PC layout. The internal short-circuit and foldback current limiting still remains active, thereby protecting the power supply system from failure. A decision can be made after the design is complete whether to rely solely on foldback current limiting or to enable the latchoff feature by removing the pull-up resistor.

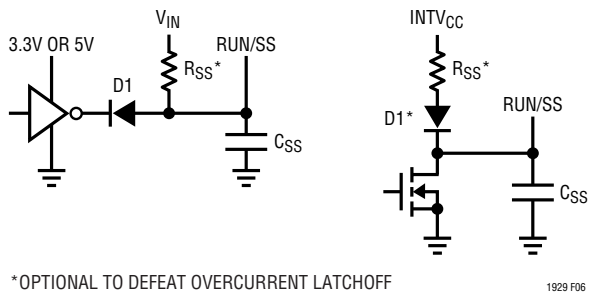


Figure 6. RUN/SS Pin Interfacing

The value of the soft-start capacitor C_{SS} may need to be scaled with output voltage, output capacitance and load current characteristics. The minimum soft-start capacitance is given by:

$$C_{SS} > (C_{OUT})(V_{OUT})(10^{-4})(R_{SENSE})$$

The minimum recommended soft-start capacitor of C_{SS} = 0.1µF will be sufficient for most applications.

Phase-Locked Loop and Frequency Synchronization

The LTC1929 has a phase-locked loop comprised of an internal voltage controlled oscillator and phase detector. This allows the top MOSFET turn-on to be locked to the rising edge of an external source. The frequency range of the voltage controlled oscillator is ±50% around the center frequency f_O. A voltage applied to the PLLFLTR pin of 1.2V corresponds to a frequency of approximately 220kHz. The nominal operating frequency range of the LTC1929 is 140kHz to 310kHz.

The phase detector used is an edge sensitive digital type which provides zero degrees phase shift between the external and internal oscillators. This type of phase detector will not lock up on input frequencies close to the harmonics of the VCO center frequency. The PLL hold-in range, Δf_H, is equal to the capture range, Δf_C:

$$\Delta f_H = \Delta f_C = \pm 0.5\ f_O\ (150kHz\text{-}300kHz)$$

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLLFLTR pin. A simplified block diagram is shown in Figure 7.

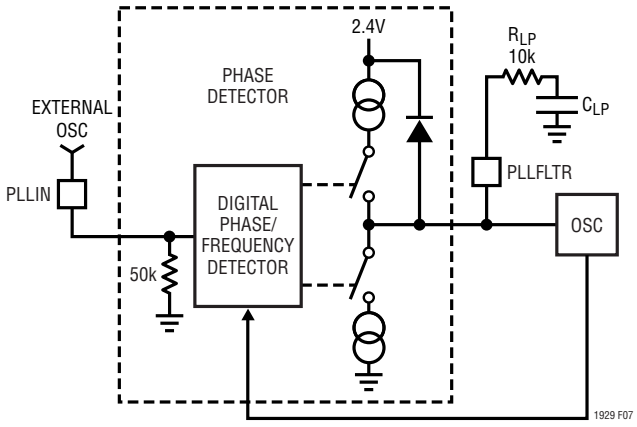


Figure 7. Phase-Locked Loop Block Diagram

APPLICATIONS INFORMATION

If the external frequency (f_{PLLIN}) is greater than the oscillator frequency f_{OSC}, current is sourced continuously, pulling up the PLLFLTR pin. When the external frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLFLTR pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus the voltage on the PLLFLTR pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point the phase comparator output is open and the filter capacitor C_{LP} holds the voltage. The LTC1929 PLLIN pin must be driven from a low impedance source such as a logic gate located close to the pin.

The loop filter components (C_{LP}, R_{LP}) smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} =10kΩ and C_{LP} is 0.01µF to 0.1µF.

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC1929 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC1929 will begin to skip cycles resulting in nonconstant frequency operation. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

The minimum on-time for the LTC1929 is generally less than 200ns. However, as the peak sense voltage decreases the minimum on-time gradually increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

If an application can operate close to the minimum on-time limit, an inductor must be chosen that has a low enough inductance to provide sufficient ripple amplitude to meet the minimum on-time requirement. *As a general rule, keep the inductor ripple current of each phase equal to or greater than 15% of $I_{OUT(MAX)}$ at $V_{IN(MAX)}$.*

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1929 circuits: 1) LTC1929 V_{IN} current (including loading on the differential amplifier output), 2) $INTV_{CC}$ regulator current, 3) I^2R losses and 4) Topside MOSFET transition losses.

1) The V_{IN} current has two components: the first is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents; the second is the current drawn from the differential amplifier output. V_{IN} current typically results in a small (<0.1%) loss.

2) $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = (Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

APPLICATIONS INFORMATION

Supplying $INTV_{CC}$ power through the $EXTV_{CC}$ switch input from an output-derived source will scale the V_{IN} current required for the driver and control circuits by the ratio (Duty Factor)/(Efficiency). For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 3mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3) I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses. For example, if each $R_{DS(ON)}$=10mΩ, R_L=10mΩ, and R_{SENSE}=5mΩ, then the total resistance is 25mΩ. This results in losses ranging from 2% to 8% as the output current increases from 3A to 15A per output stage for a 5V output, or a 3% to 12% loss per output stage for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4) Transition losses apply only to the topside MOSFET(s), and only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7)\ V_{IN}^2\ I_{O(MAX)}\ C_{RSS}\ f$$

Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and input fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and a very low ESR at the switching frequency. A 50W supply will typically require a minimum of 200µF to 300µF of output capacitance having a maximum of 10mΩ to 20mΩ of ESR. The LTC1929 2-phase architecture typically halves the input and output capacitance requirements over competing solutions. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD}(ESR), where ESR is the effective series resistance of C_{OUT}(ΔI_{LOAD}) also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. *The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time, and settling at this test point truly reflects the closed loop response.* Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Figure 1 circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.2 to 5 times their suggested values) to maximize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of <2µs will produce output voltage and I_{TH} pin waveforms

APPLICATIONS INFORMATION

that will give a sense of the overall loop stability without breaking the feedback loop. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the Ith pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main battery line in an automobile is the source of a number of nasty potential transients, including load-dump, reverse-battery, and double-battery.

Load-dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse-battery is just what it says, while double-battery is a consequence of tow truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 8 is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive battery line. The series diode prevents current from flowing during reverse-battery, while the transient suppressor clamps the input voltage during load-dump. Note that the transient suppressor should not conduct during double-battery operation, but must still clamp the input voltage below breakdown of the converter. Although the LT1929 has a maximum input voltage of 36V, most applications will be limited to 30V by the MOSFET BV_{DSS}.

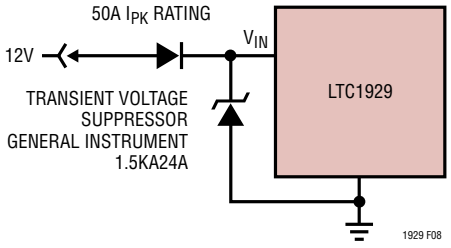


Figure 8. Automotive Application Protection

APPLICATIONS INFORMATION

Design Example

As a design example, assume V_{IN} = 5V (nominal), V_{IN} = 5.5V (max), V_{OUT} = 1.8V, I_{MAX} = 20A, T_A = 70°C and f = 300kHz.

The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Tie the FREQSET pin to the $INTV_{CC}$ pin for 300kHz operation. The minimum inductance for 30% ripple current is:

$$L \geq \frac{V_{OUT}}{f(\Delta I)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

$$\geq \frac{1.8V}{(300kHz)(30\%)(10A)}\left(1-\frac{1.8V}{5.5V}\right)$$

$$\geq 1.35\mu H$$

A 1.5µH inductor will produce 27% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 11.4A. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN}f} = \frac{1.8V}{(5.5V)(300kHz)} = 1.1\mu s$$

The R_{SENSE} resistors value can be calculated by using the maximum current sense voltage specification with some accomodation for tolerances:

$$R_{SENSE} = \frac{50mV}{11.4A} \approx 0.004\Omega$$

The power dissipation on the topside MOSFET can be easily estimated. Using a Siliconix Si4420DY for example; $R_{DS(ON)}$ = 0.013Ω, C_{RSS} = 300pF. At maximum input voltage with T_J (estimated) = 110°C at an elevated ambient temperature:

$$P_{MAIN} = \frac{1.8V}{5.5V}(10)^2\left[1+(0.005)(110°C-25°C)\right]$$

$$0.013\Omega + 1.7(5.5V)^2(10A)(300pF)$$

$$(300kHz) = 0.65W$$

The worst-case power disipated by the synchronous MOSFET under normal operating conditions at elevated ambient temperature and estimated 50°C junction temperature rise is:

$$P_{SYNC} = \frac{5.5V-1.8V}{5.5V}(10A)^2(1.48)(0.013\Omega)$$

$$= 1.29W$$

A short-circuit to ground will result in a folded back current of about:

$$I_{SC} = \frac{25mV}{0.004\Omega} + \frac{1}{2}\left[\frac{200ns(5.5V)}{1.5\mu H}\right] = 6.6A$$

The worst-case power disipated by the synchronous MOSFET under short-circuit conditions at elevated ambient temperature and estimated 50°C junction temperature rise is:

$$P_{SYNC} = \frac{5.5V-1.8V}{5.5V}(6.6A)^2(1.48)(0.013\Omega)$$

$$= 564mW$$

which is less than half of the normal, full-load dissipation. Incidentally, since the load no longer dissipates power in the shorted condition, total system power dissipation is decreased by over 99%.

The duty factor for this application is:

$$DF = \frac{V_O}{V_{IN}} = \frac{1.8V}{5V} = 0.36$$

Using Figure 4, the RMS ripple current will be:

I_{INRMS} = (20A)(0.23) = $4.6A_{RMS}$

An input capacitor(s) with a $4.6A_{RMS}$ ripple current rating is required.

The output capacitor ripple current is calculated by using the inductor ripple already calculated for each inductor and multiplying by the factor obtained from Figure 3 along with the calculated duty factor. The output ripple in

APPLICATIONS INFORMATION

continuous mode will be highest at the maximum input voltage since the duty factor is <50%. The maximum output current ripple is:

$$\Delta I_{COUT} = \frac{V_{OUT}}{fL}\left(0.3\right) \text{ at } 33\%\ DF$$

$$\Delta I_{COUTMAX} = \frac{1.8V}{\left(300kHz\right)\left(1.5\mu H\right)}0.3$$

$$= 1.2A_{RMS}$$

$$V_{OUTRIPPLE} = 20m\Omega\left(1.2A_{RMS}\right) = 24mV_{RMS}$$

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1929. These items are also illustrated graphically in the layout diagram of Figure 11. Check the following in your layout:

1) Are the signal and power grounds segregated? The LTC1929 signal ground pin should return to the (–) plate of C_{OUT} separately. The power ground returns to the sources of the bottom N-channel MOSFETs, anodes of the Schottky diodes, and (–) plates of C_{IN}, which should have as short lead lengths as possible.

2) Does the LTC1929 V_{OS}^+ pin connect to the (+) plate(s) of C_{OUT}? Does the LTC1929 V_{OS}^- pin connect to the (–) plate(s) of C_{OUT}? The resistive divider R1, R2 must be connected between the $V_{DIFFOUT}$ and signal ground and any feedforward capacitor across R1 should be as close as possible to the LTC1929.

3) Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The filter capacitors between SENSE$^+$ and SENSE$^-$ pin pairs should be as close as possible to the LTC1929. Ensure accurate current sensing with Kelvin connections.

4) Do the (+) plates of C_{IN} connect to the drains of the topside MOSFETs as closely as possible? This capacitor provides the AC current to the MOSFETs. Keep the input current path formed by the input capacitor, top and bottom MOSFETs, and the Schottky diode on the same side of the PC board in a tight loop to minimize conducted and radiated EMI.

5) Is the $INTV_{CC}$ 1µF ceramic decoupling capacitor connected closely between $INTV_{CC}$ and the power ground pin? This capacitor carries the MOSFET driver peak currents. A small value is used to allow placement immediately adjacent to the IC.

6) Keep the switching nodes, SW1 (SW2), away from sensitive small-signal nodes. Ideally the switch nodes should be placed at the furthest point from the LTC1929.

7) Use a low impedance source such as a logic gate to drive the PLLIN pin and keep the lead as short as possible.

The diagram in Figure 9 illustrates all branch currents in a 2-phase switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high-switching-current paths to a small physical size. High electric and magnetic fields will radiate from these "loops" just as radio stations transmit signals. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the "noise" generated by a switching regulator. The ground terminations of the synchronous MOSFETs and Schottky diodes should return to the bottom plate(s) of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. A separate isolated path from the bottom plate(s) of the input capacitor(s) should be used to tie in the IC power ground pin (PGND) and the signal ground pin (SGND). This technique keeps inherent signals generated by high current pulses from taking alternate current paths that have finite impedances during the total period of the switching regulator. External OPTI-LOOP compensation allows overcompensation for PC layouts which are not optimized but this is not the recommended design procedure.

APPLICATIONS INFORMATION

Simplified Visual Explanation of How a 2-Phase Controller Reduces Both Input and Output RMS Ripple Current

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is divided by, and the effective ripple frequency is multiplied up by the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by, and the effective ripple frequency is increased by the number of phases used. Figure 10 graphically illustrates the principle.

The worst-case RMS ripple current for a single stage design peaks at twice the value of the output voltage . The worst-case RMS ripple current for a two stage design results in peaks at 1/4 and 3/4 of input voltage. When the RMS current is calculated, higher effective duty factor results and the peak current levels are divided as long as the currents in each stage are balanced. Refer to Application Note 19 for a detailed description of how to calculate RMS current for the single stage switching regulator. Figures 3 and 4 illustrate how the input and output currents are reduced by using an additional phase. The input current peaks drop in half and the frequency is doubled for this 2-phase converter. The input capacity requirement is thus reduced theoretically by a factor of four! Ceramic input capacitors with their unbeatably low ESR characteristics can be used.

Figure 4 illustrates the RMS input current drawn from the input capacitance vs the duty cycle as determined by the ratio of input and output voltage. The peak input RMS current level of the single phase system is reduced by 50% in a 2-phase solution due to the current splitting between the two stages.

An interesting result of the 2-phase solution is that the V_{IN} which produces worst-case ripple current for the input capacitor, $V_{OUT} = V_{IN}/2$, in the single phase design produces zero input current ripple in the 2-phase design.

The output ripple current is reduced significantly when compared to the single phase solution using the same inductance value because the V_{OUT}/L discharge current term from the stage that has its bottom MOSFET on subtracts current from the $(V_{IN} - V_{OUT})/L$ charging current resulting from the stage which has its top MOSFET on. The output ripple current is:

$$\Delta I_{RIPPLE} = \frac{2V_{OUT}}{fL}\left[\frac{\left|1-2D\right|\left(1-D\right)}{\left|1-2D\right|+1}\right]$$

where D is duty factor.

The input and output ripple frequency is increased by the number of stages used, reducing the output capacity requirements. When V_{IN} is approximately equal to $2(V_{OUT})$ as illustrated in Figures 3 and 4, very low input and output ripple currents result.

APPLICATIONS INFORMATION

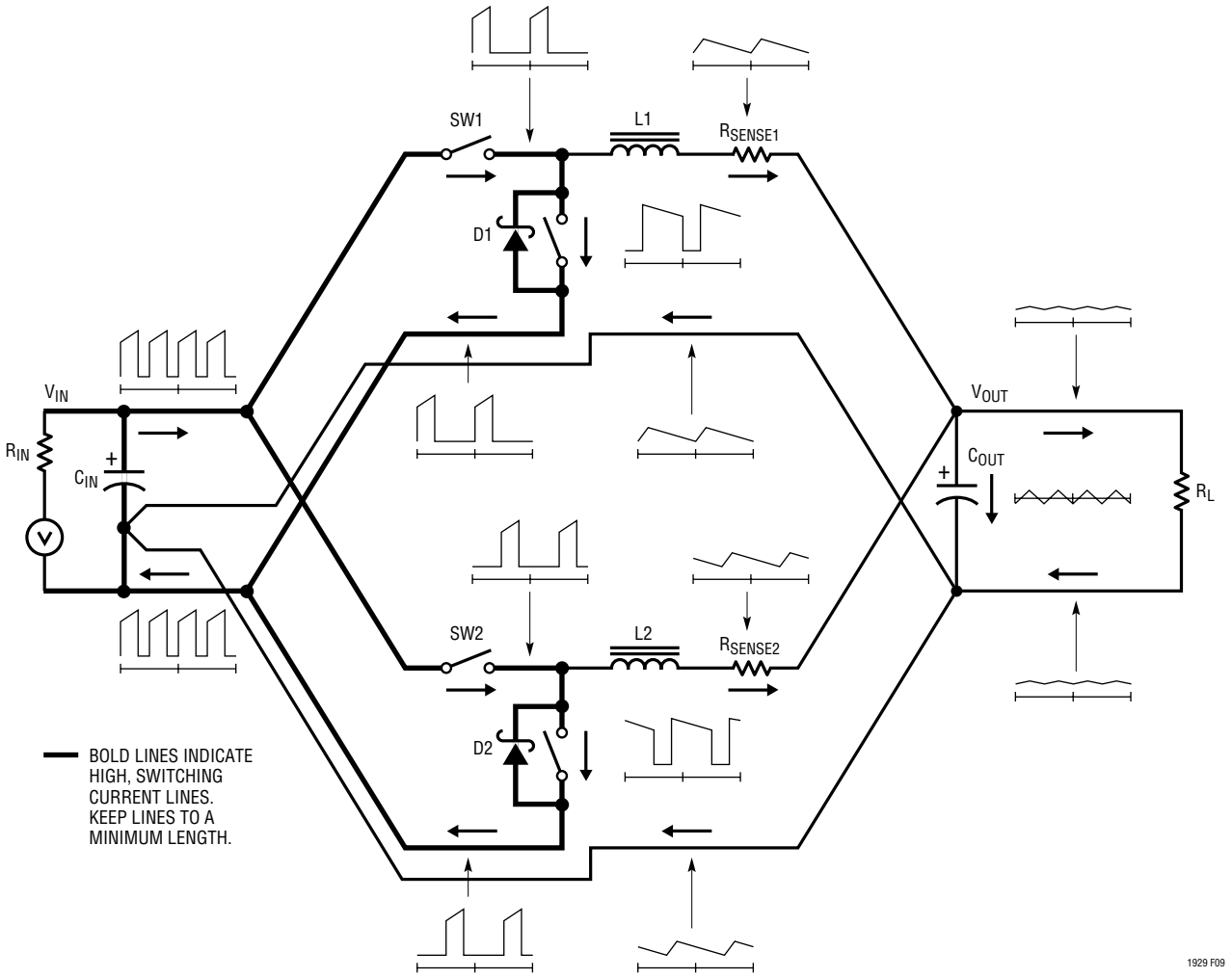


Figure 9. Instantaneous Current Path Flow in a Multiple Phase Switching Regulator

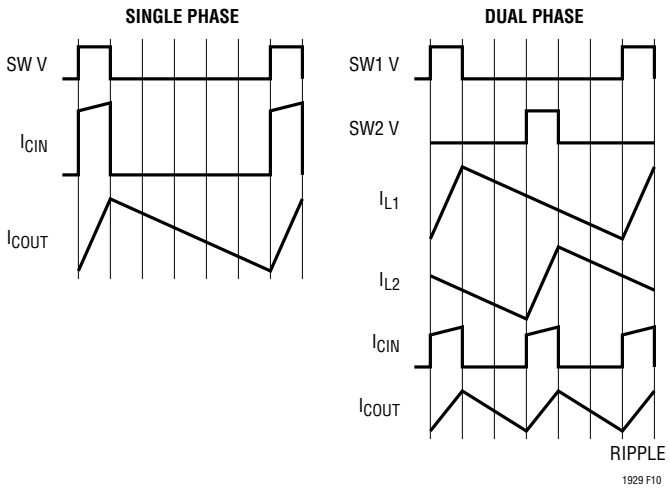


Figure 10. Single and 2-Phase Current Waveforms

TYPICAL APPLICATIONS

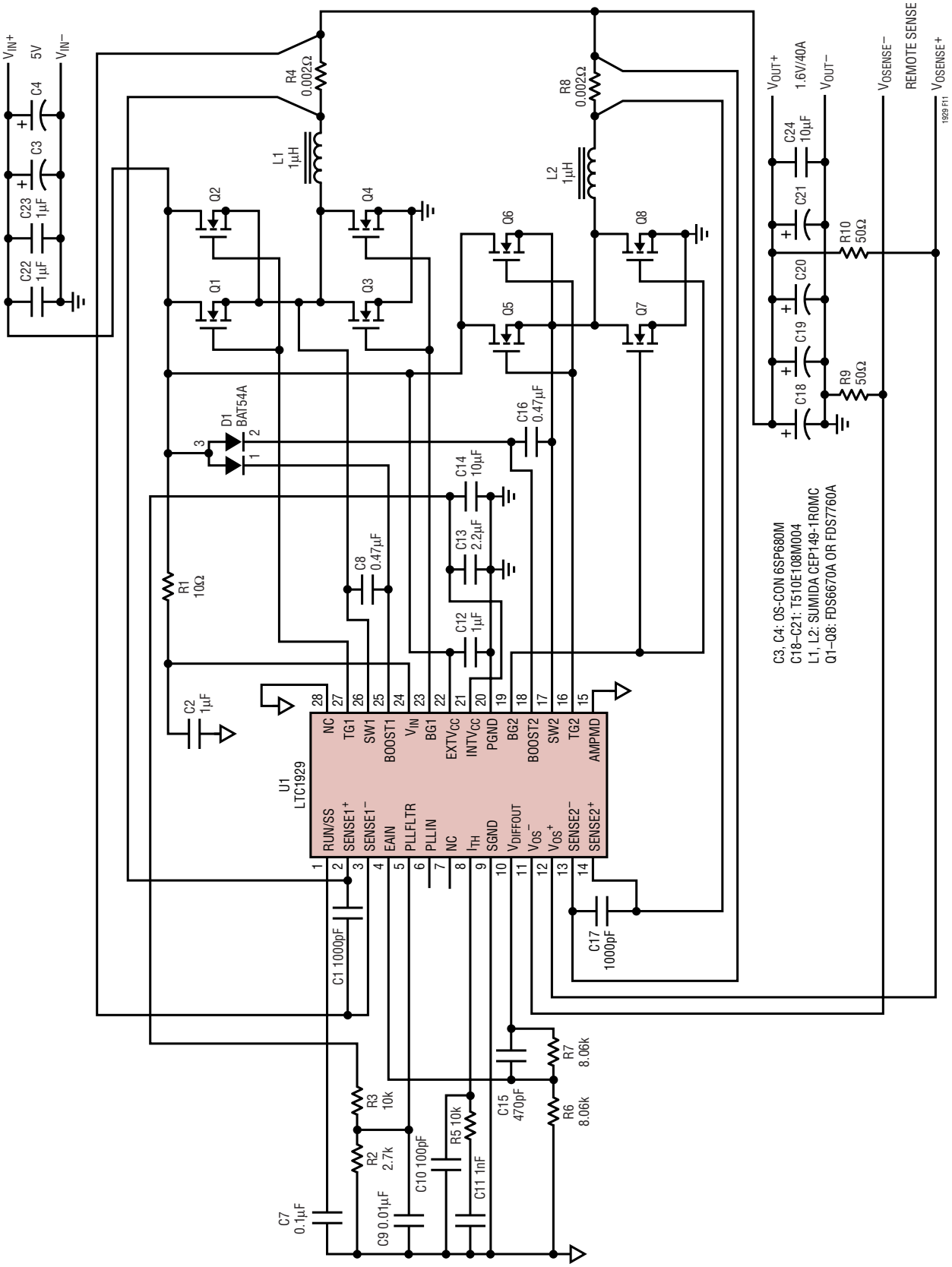


Figure 11. 5V Input, 1.6V/40A CPU Power Supply

TYPICAL APPLICATIONS

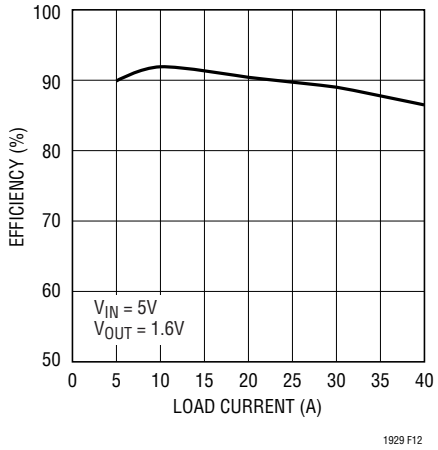
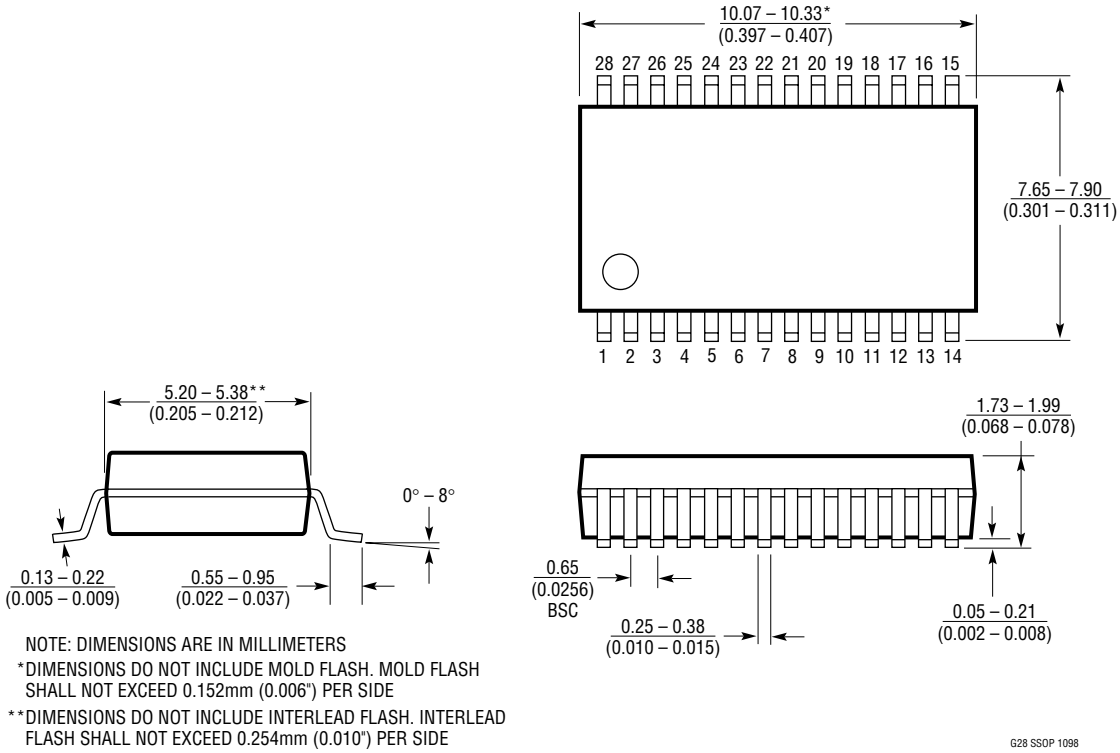


Figure 12. Efficiency Plot for Circuit of Figure 11

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



NOTE: DIMENSIONS ARE IN MILLIMETERS

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

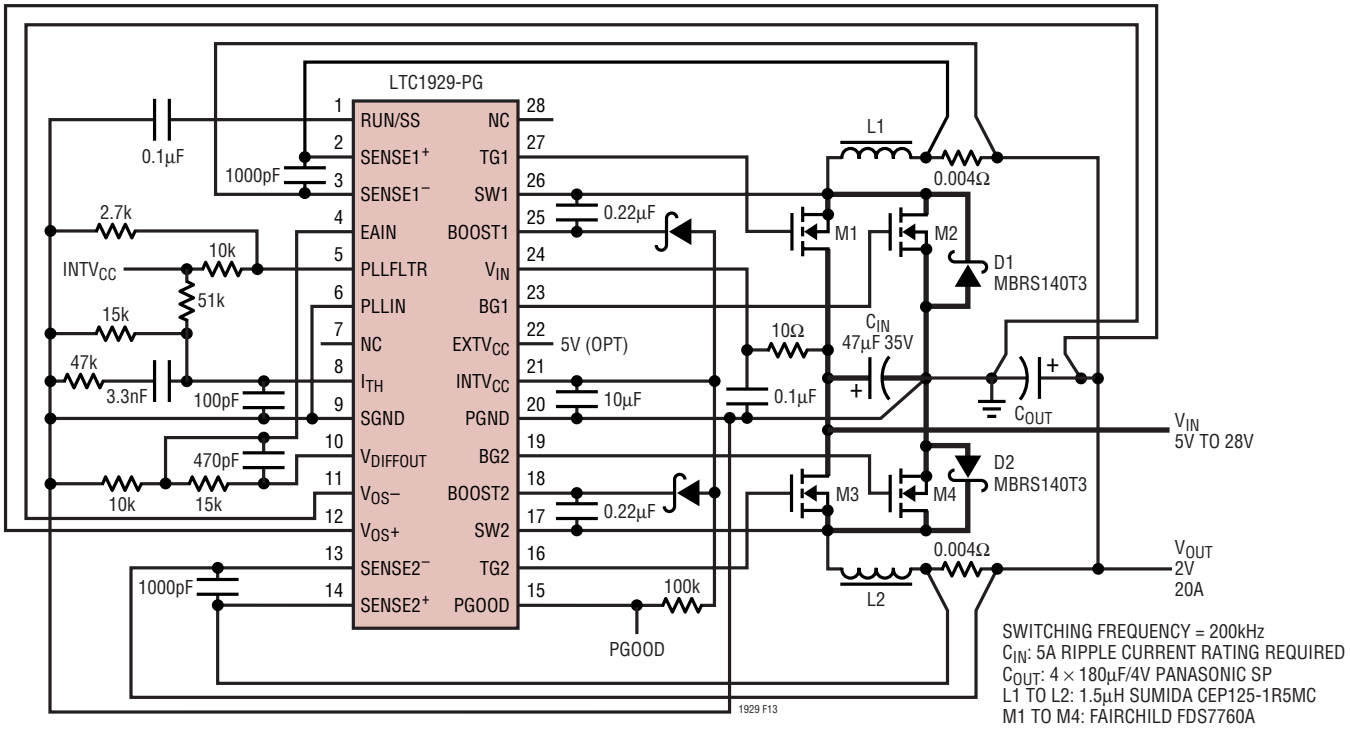


Figure 13. 2V/20A CPU Power Supply with Active Voltage Positioning

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1438/LTC1439	Dual High Efficiency Low Noise Synchronous Step-Down Switching Regulators	POR, Auxiliary Regulator
LTC1438-ADJ	Dual Synchronous Controller with Auxiliary Regulator	POR, External Feedback Divider
LTC1538-AUX	Dual High Efficiency Low Noise Synchronous Step-Down Switching Regulator	Auxiliary Regulator, 5V Standby
LTC1539	Dual High Efficiency Low Noise Synchronous Step-Down Switching Regulator	5V Standby, POR, Low-Battery, Aux Regulator
LTC1435/LTC1435A	High Efficiency Synchronous Step-Down Switching Regulator	Burst Mode™ Operation, 16-Pin Narrow SO
LTC1436A-PLL	High Efficiency Low Noise Synchronous Step-Down Switching Regulator	Adaptive Power™ Mode, 24-Pin SSOP
LTC1628/LTC1628-PG	Dual High Efficiency, 2-Phase Synchronous Step-Down Switching Regulator	Constant Frequency, Standby, 5V and 3.3V LDOs
LTC1629/LTC1629-PG	PolyPhase High Efficiency Controller	Expandable Up to 12 Phases, G-28, Up to 120A
LTC1702/LTC1703	Dual High Efficiency, 2-Phase Synchronous Step-Down Switching Regulator	500kHz, 25MHz GBW
LTC1735	High Efficiency Synchronous Step-Down Controller	Burst Mode Operation, 16-Pin Narrow SSOP, Fault Protection, $3.5V \le V_{IN} \le 36V$
LTC1736	High Efficiency Synchronous Step-Down Controller with 5-Bit VID	Output Fault Protection, Power Good, GN-24, $3.5V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 6V$

Adaptive Power and Burst Mode are trademarks of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
1929f LT/TP 0500 4K • PRINTED IN USA
© LINEAR TECHNOLOGY CORPORATION 1999

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View LTC1929IG-PG#PBF on WIN SOURCE
- Linear Technology Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management