THE DATASHEET OF

LTC1850CFW#PBF

www.win-source.net 0086-755-83957316

8-Channel, 10-Bit/12-Bit, 1.25Msps Sampling ADCs

FEATURES

- **Flexible 8-Channel Multiplexer**
- **Single-Ended or Differential Inputs**
- **Two Gain Ranges Plus Unipolar and Bipolar Operation**
- **1.25Msps Sampling Rate**
- **Single 5V Supply and 40mW Power Dissipation**
- **Scan Mode and Programmable Sequencer**
- Pin Compatible 10-Bit LTC1850 and 12-Bit LTC1851
- True Differential Inputs Reject Common Mode Noise
- Internal 2.5V Reference
- Parallel Output Includes MUX Address
- Easy Interface to 3V Logic
- Nap and Sleep Shutdown Modes

APPLICATIONS

- High Speed Data Acquisition
- Test and Measurement
- Imaging Systems
- Telecommunications
- Industrial Process Control
- Spectrum Analysis

DESCRIPTION

The 10-bit LTC®1850 and 12-bit LTC1851 are complete 8-channel data acquisition systems. They include a flexible 8-channel multiplexer, a 1.25Msps successive approximation analog-to-digital converter with sample-and-hold, an internal 2.5V reference and reference buffer amplifier, and a parallel output interface. The multiplexer can be configured for single-ended or differential inputs, two gain ranges and unipolar or bipolar operation.

The ADCs have a scan mode that will repeatedly cycle through all 8 multiplexer channels and can also be programmed with a sequence of up to 16 addresses and configurations that can be scanned in succession. The sequence memory can also be read back. The reference and buffer amplifier provide pin strappable ranges of 4.096V, 2.5V and 2.048V. The parallel output includes the 10-bit or 12-bit conversion result plus the 4-bit multiplexer address. The digital outputs are powered from a separate supply allowing for easy interface to 3V digital logic. Typical power consumption is 40mW at 1.25Msps from a single 5V supply.

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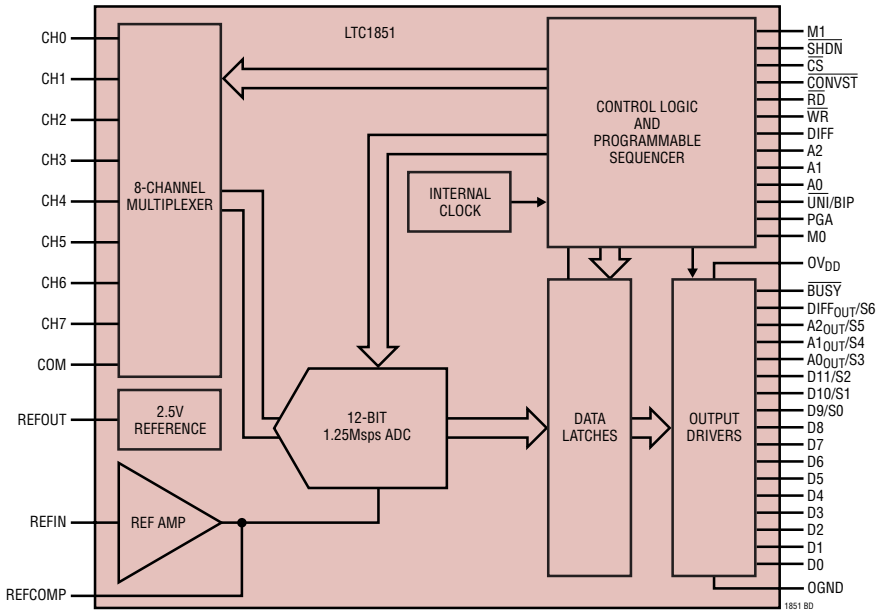
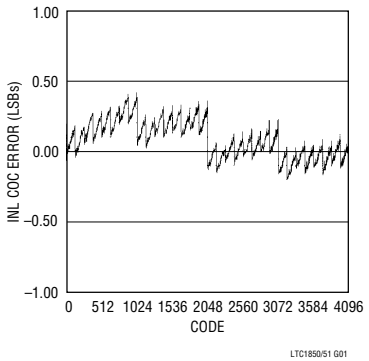
BLOCK DIAGRAM



Integral Linearity, LTC1851



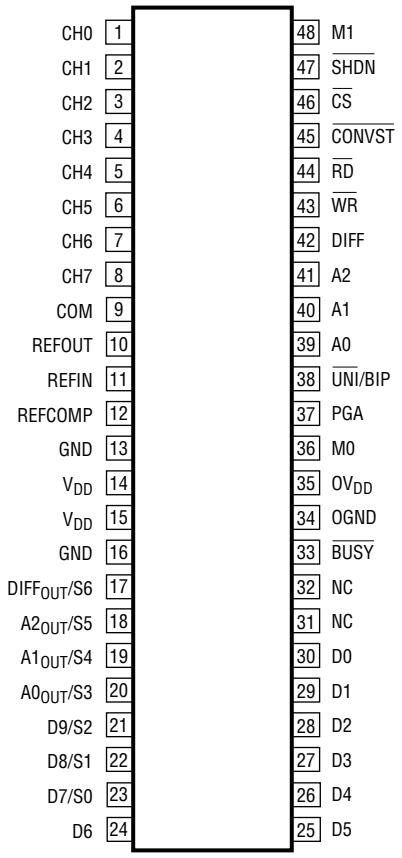
ABSOLUTE MAXIMUM RATINGS $OV_{DD} = V_{DD}$ (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Analog Input Voltage (Note 3) ..... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage (Note 4) ..... –0.3V to 10V
Digital Output Voltage ..... –0.3V to (V_{DD} + 0.3V)
Power Dissipation 500mW

Ambient Operating Temperature Range
LTC1850C/LTC1851C ..... 0°C to 70°C
LTC1850I/LTC1851I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

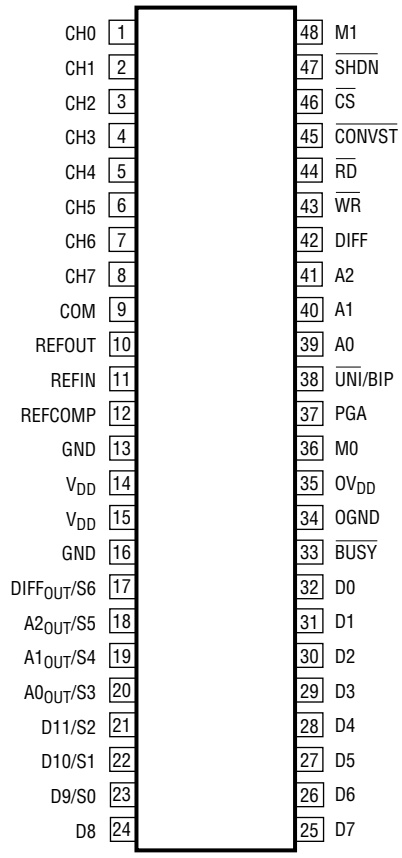


FW PACKAGE
48-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LTC1850CFW
LTC1850IFW

TOP VIEW



FW PACKAGE
48-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LTC1851CFW
LTC1851IFW

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 5, 6)

PARAMETER	CONDITIONS		LTC1850 MIN	LTC1850 TYP	LTC1850 MAX	LTC1851 MIN	LTC1851 TYP	LTC1851 MAX	UNITS
Resolution (No Missing Codes)		●	10			12			Bits
Integral Linearity Error	(Note 7)	●		±0.25	±0.5		±0.35	±1	LSB
Differential Linearity Error		●		±0.25	±0.5		±0.25	±1	LSB
Offset Error (Bipolar and Unipolar)	(Note 8)								
Gain = 1 (PGA = 1)	REFCOMP ≥ 2V				±2			±5	LSB
Gain = 1 (PGA = 1)	REFCOMP ≥ 2V	●		±0.5	±2		±1	±7	LSB
Gain = 2 (PGA = 0)		●		±1	±4		±2	±10	LSB
Offset Error Match					±0.5			±1	LSB
Unipolar Gain Error	With External 4.096V Reference								
Gain = 1 (PGA = 1)	Applied to REFCOMP (Note 12)				±2			±6	LSB
Gain = 2 (PGA = 0)					±4			±10	LSB
Unipolar Gain Error Match					±0.5			±1	LSB
Bipolar Gain Error	With External 4.096V Reference								
Gain = 1 (PGA = 1)	Applied to REFCOMP (Note 12)				±2			±6	LSB
Gain = 2 (PGA = 0)					±4			±10	LSB
Bipolar Gain Error Match					±0.5			±1	LSB
Full-Scale Error Temperature Coefficient				15			15		ppm/°C

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.75V ≤ V_{DD} ≤ 5.25V					
	Unipolar, Gain = 1 (PGA = 1)				0 – REFCOMP		V
	Unipolar, Gain = 2 (PGA = 0)				0 – REFCOMP/2		V
	Bipolar, Gain = 1 (PGA = 1)				±REFCOMP/2		V
	Bipolar, Gain = 2 (PGA = 0)				±REFCOMP/4		V
I_{IN}	Analog Input Leakage Current	V_{IN} > 0V < V_{DD}, All Channels	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Gain = 1)			15		pF
		Between Conversions (Gain = 2)			25		pF
		During Conversions			5		pF
t_{ACQ}	Sample-and-Hold Acquisition Time		●		50	150	ns
$t_{S(MUX)}$	Multiplexer Settling Time (Includes t_{ACQ})		●		50	150	ns
t_{AP}	Sample-and-Hold Aperture Delay Time				–0.5		ns
t_{jitter}	Sample-and-Hold Aperture Delay Time Jitter				2		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	0V < (A_{IN}^- = A_{IN}^+) < 5V			60		dB

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LTC1850 MIN	LTC1850 TYP	LTC1850 MAX	LTC1851 MIN	LTC1851 TYP	LTC1851 MAX	UNITS
SNR	Signal-to-Noise Ratio	47kHz Input Signal							
	Unipolar, PGA = 0			61.6			71		dB
	Unipolar, PGA = 1			61.7			72		dB
	Bipolar, PGA = 0			61.6			71		dB
	Bipolar, PGA = 1			61.7			72		dB
S/(N+D)	Signal-to-(Noise + Distortion) Ratio	47kHz Input Signal							
	Unipolar, PGA = 0			61.0			70		dB
	Unipolar, PGA = 1			61.0			71		dB
	Bipolar, PGA = 0			61.0			71		dB
	Bipolar, PGA = 1			61.2			72		dB
THD	Total Harmonic Distortion	47kHz Input Signal,							
	Unipolar, PGA = 0	First 5 Harmonics		–76			–80		dB
	Unipolar, PGA = 1			–78			–82		dB
	Bipolar, PGA = 0			–81			–87		dB
	Bipolar, PGA = 1			–80			–86		dB
SFDR	Spurious-Free Dynamic Range	47kHz Input Signal							
	Unipolar, PGA = 0			74			82		dB
	Unipolar, PGA = 1			80			86		dB
	Bipolar, PGA = 0			84			90		dB
	Bipolar, PGA = 1			82			88		dB

INTERNAL REFERENCE T_A = 25°C. (Notes 5, 6)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFOUT Output Voltage	I_{OUT} = 0	2.48	2.50	2.52	V
REFOUT Output Temperature Coefficient	I_{OUT} = 0		±15		ppm/°C
REFOUT Line Regulation			0.01		LSB/V
Reference Buffer Gain	$V_{REFCOMP}/V_{REFIN}$	1.636	1.638	1.640	V/V
REFCOMP Output Voltage	External 2.5V Reference	4.090	4.096	4.100	V
	Internal 2.5V Reference	4.060	4.096	4.132	V
REFCOMP Impedance	REFIN = V_{DD}		6.4		kΩ

DIGITAL INPUTS AND DIGITAL OUTPUTS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±5	µA
C_{IN}	Digital Input Capacitance				2		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V, I_O = –10µA			4.5		V
		V_{DD} = 4.75V, I_O = –200µA	●	4.0			V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V, I_O = 160µA			0.05		V
		V_{DD} = 4.75V, I_O = 1.6mA	●		0.10	0.4	V
I_{OZ}	Hi-Z Output Leakage D11 to D0, AD_{OUT}, $A1_{OUT}$, $A2_{OUT}$, $DIFF_{OUT}$	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	Hi-Z Capacitance D11 to D0, AD_{OUT}, $A1_{OUT}$, $A2_{OUT}$, $DIFF_{OUT}$	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–20		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			30		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Note 10)	●	4.75		5.25	V
OV_{DD}	Output Positive Supply Voltage	(Note 10)	●	2.7		5.25	V
I_{DD}	Positive Supply Current	V_{DD} = V_{DD} = OV_{DD} = 5V, f_{SAMPLE} = 1.25MHz	●		8	10	mA
P_{DISS}	Power Dissipation		●		40	50	mW
	Power Down Positive Supply Current Nap Mode Sleep Mode	 $\overline{SHDN}$ = 0V, $\overline{CS}$ = 0V $\overline{SHDN}$ = 0V, $\overline{CS}$ = 5V			 1 50		 mA µA
	Power Down Power Dissipation Nap Mode Sleep Mode	 $\overline{SHDN}$ = 0V, $\overline{CS}$ = 0V $\overline{SHDN}$ = 0V, $\overline{CS}$ = 5V			 5 0.25		 mW mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency Acquisition + Conversion		● ●	1.25		 800	MHz ns
t_{CONV}	Conversion Time		●			650	ns
t_{ACQ}	Acquisition Time		●			150	ns
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time	(Notes 9, 10)	●	0			ns
t_2	$\overline{CS}$ to $\overline{CONVST}$ Setup Time	(Notes 9, 10)	●	10			ns
t_3	$\overline{CS}$ to $\overline{SHDN}$ Setup Time	(Notes 9, 10)			200		ns
t_4	$\overline{SHDN}$ to $\overline{CONVST}$ Wake-Up Time	Nap Mode (Note 10) Sleep Mode, 10µF REFCOMP Bypass Capacitor (Note 10)			200 10		ns ms
t_5	$\overline{CONVST}$ Low Time	(Notes 10, 11)	●	50			ns
t_6	$\overline{CONVST}$ to $\overline{BUSY}$ Delay	C_L = 25pF	 ●		10	 60	ns ns
t_7	Data Ready Before $\overline{BUSY}$		 ●	20 15	35		ns ns
t_8	Delay Between Conversions	(Note 10)	●	50			ns
t_9	Wait Time $\overline{RD}$ After $\overline{BUSY}$		●	–5			ns
t_{10}	Data Access Time After $\overline{RD}$	C_L = 25pF	 ●		20	35 45	ns ns
		C_L = 100pF	 ●		25	45 60	ns ns
t_{11}	BUS Relinquish Time	 0°C to 70°C –40°C to 85°C	 ● ●		10	30 35 40	ns ns ns
t_{12}	$\overline{RD}$ Low Time		●	t_{10}			ns
t_{13}	$\overline{CONVST}$ High Time	(Note 10)	●	50			ns
t_{14}	Latch Setup Time	(Notes 9, 10)	●	10			ns
t_{15}	Latch Hold Time	(Notes 9, 10)	●	10			ns
t_{16}	$\overline{WR}$ Low Time	(Note 10)	●	50			ns

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{17}	$\overline{WR}$ High Time	(Note 10)	●	50			ns
t_{18}	M1 to M0 Setup Time	(Notes 9, 10)	●	10			ns
t_{19}	M0 to $\overline{BUSY}$ Delay	M1 High			20		ns
t_{20}	M0 to $\overline{WR}$ (or $\overline{RD}$) Setup Time	(Notes 9, 10)	●	t_{19}			ns
t_{21}	M0 High Pulse Width	(Note 10)	●	50			ns
t_{22}	$\overline{RD}$ High Time Between Readback Reads	(Note 10)	●	50			ns
t_{23}	Last $\overline{WR}$ (or $\overline{RD}$) to M0	(Note 10)	●	10			ns
t_{24}	M0 to $\overline{RD}$ Setup Time	(Notes 9, 10)	●	t_{19}			ns
t_{25}	M0 to $\overline{CONVST}$	(Note 10)	●	t_{19}			ns
t_{26}	Aperture Delay				–0.5		ns
t_{27}	Aperture Jitter				2		ps_{RMS}

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with GND, OGND and GND wired together unless otherwise noted.

Note 3: When these pin voltages are taken below ground or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of 100mA below ground or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below ground, they will be clamped by internal diodes. This product can handle input currents of 100mA below ground without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 4.75V to 5.25V, f_{SAMPLE} = 1.25MHz, $t_r = t_f$ = 2ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended input on any channel with COM grounded.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual end points of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0111 1111 1111 and 1000 0000 0000 for LTC1851 and between 01 1111 1111 and 10 0000 0000 for LTC1850.

Note 9: Guaranteed by design, not subject to test.

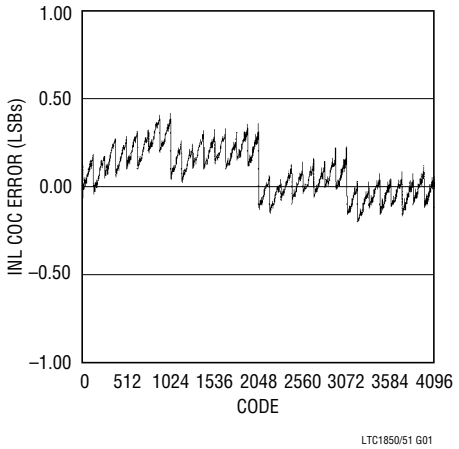
Note 10: Recommended operating conditions.

Note 11: The falling $\overline{CONVST}$ edge starts a conversion. If $\overline{CONVST}$ returns high at a critical point during the conversion it can create small errors. For the best results, ensure that $\overline{CONVST}$ returns high either within 400ns after the start of the conversion or after $\overline{BUSY}$ rises.

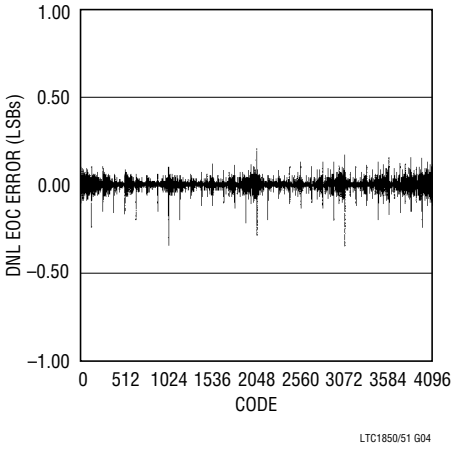
Note 12: The analog input range is determined by the voltage on REFCOMP. The gain error specification is tested with an external 4.096V but is valid for any value of REFCOMP.

TYPICAL PERFORMANCE CHARACTERISTICS

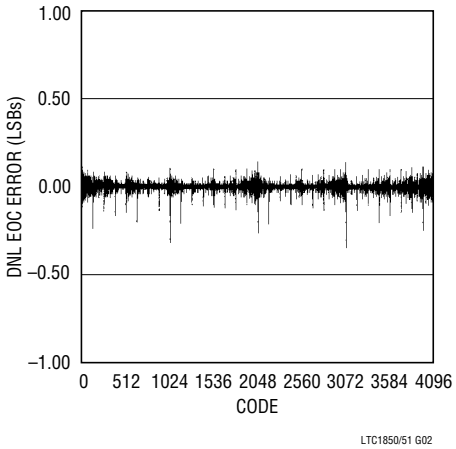
Typical INL, PGA =1, LTC1851



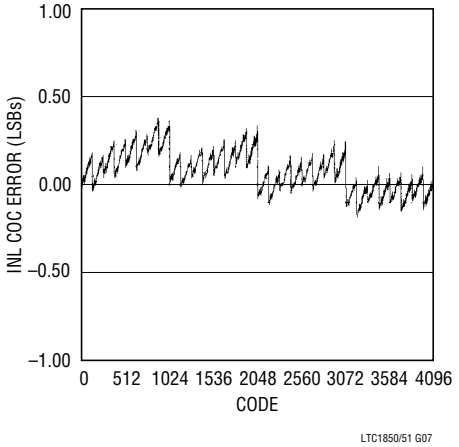
Typical DNL, PGA =1, LTC1851



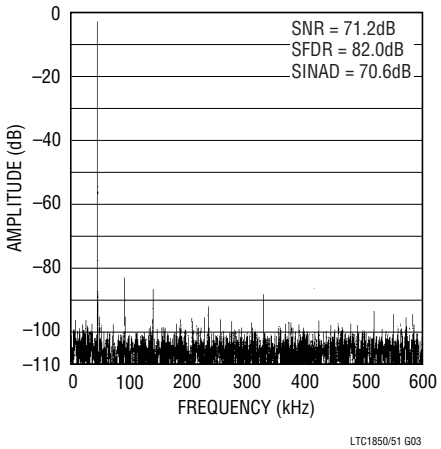
Typical DNL, PGA = 0, LTC1851



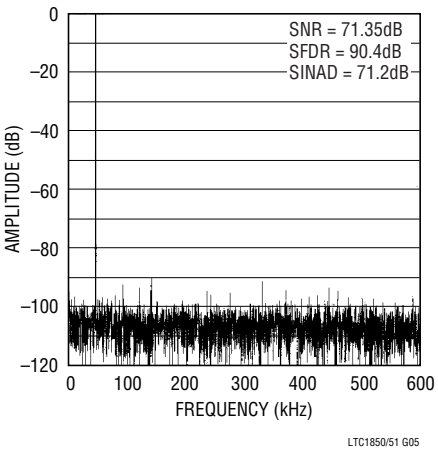
Typical INL, PGA = 0, LTC1851



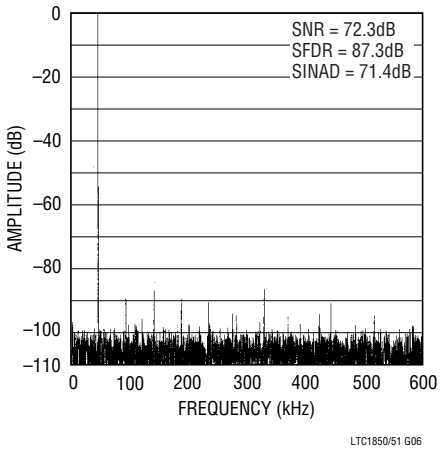
Nonaveraged 4096 Point FFT, f_{IN} = 47kHz, Unipolar Mode, PGA = 0, LTC1851



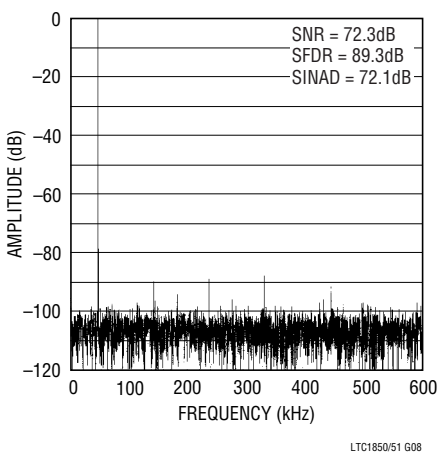
Nonaveraged 4096 Point FFT, f_{IN} = 47kHz, Bipolar Mode, PGA = 0, LTC1851



Nonaveraged 4096 Point FFT, f_{IN} = 47kHz, Unipolar Mode, PGA = 1, LTC1851

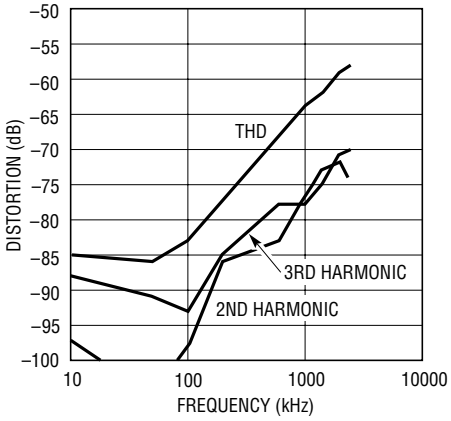


Nonaveraged 4096 Point FFT, f_{IN} = 47kHz, Bipolar Mode, PGA = 1, LTC1851



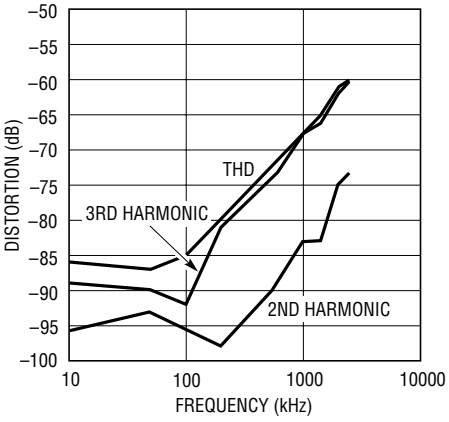
TYPICAL PERFORMANCE CHARACTERISTICS

Distortion vs Input Frequency, Bipolar Mode, PGA = 1



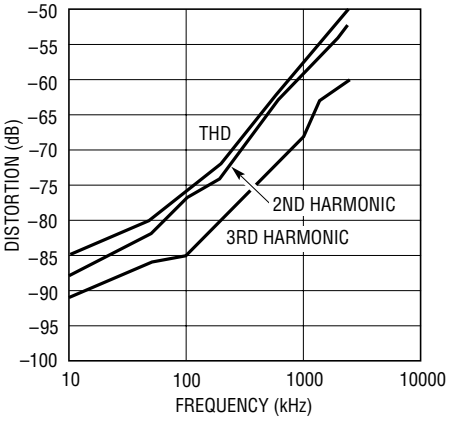
185051 G09

Distortion vs Input Frequency, Bipolar Mode, PGA = 0



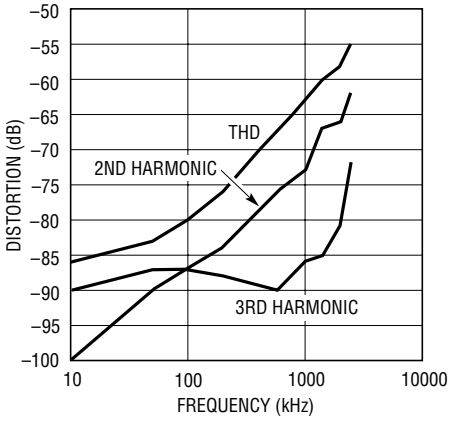
185051 G10

Distortion vs Input Frequency, Unipolar Mode, PGA = 0



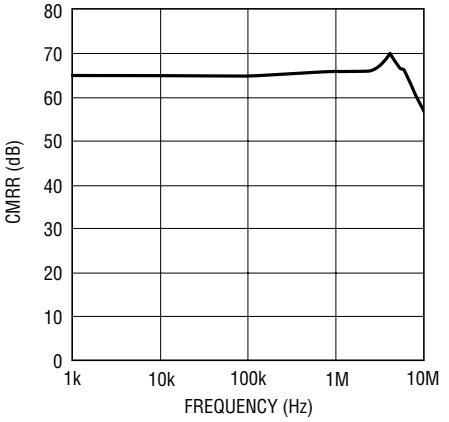
185051 G19

Distortion vs Input Frequency, Unipolar Mode, PGA = 1



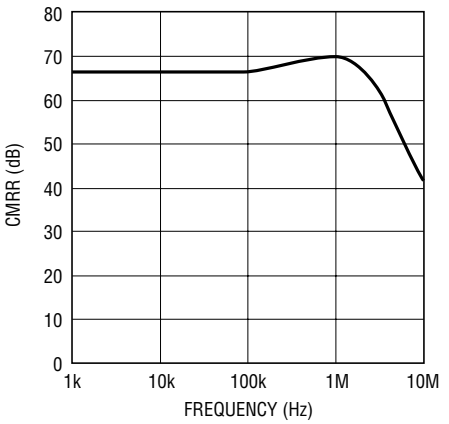
185051 G20

Input Common Mode Rejection Ratio vs Frequency, Bipolar Mode, PGA = 0



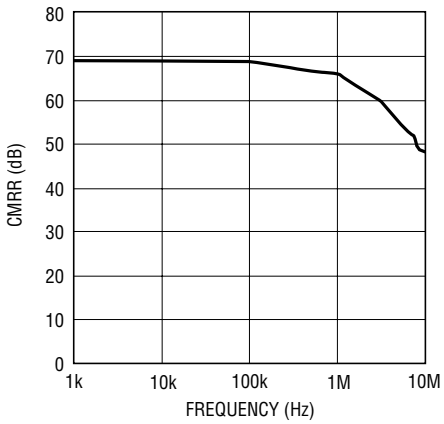
LTC1850/51 G11

Input Common Mode Rejection Ratio vs Frequency, Unipolar Mode, PGA = 0



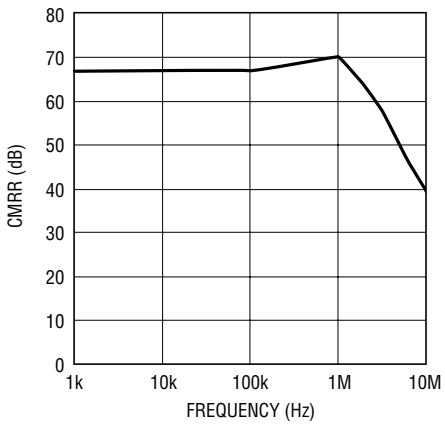
LTC1850/51 G13

Input Common Mode Rejection Ratio vs Frequency, Bipolar Mode, PGA = 1



LTC1850/51 G14

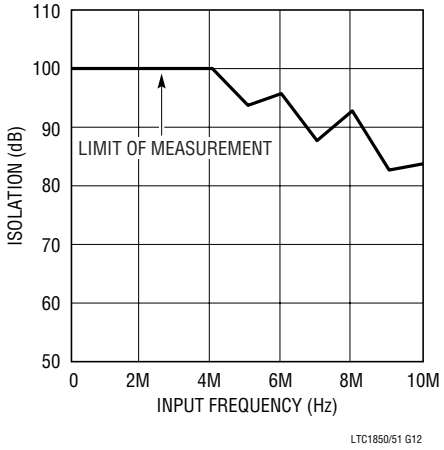
Input Common Mode Rejection Ratio vs Frequency, Unipolar Mode, PGA = 1



LTC1850/51 G16

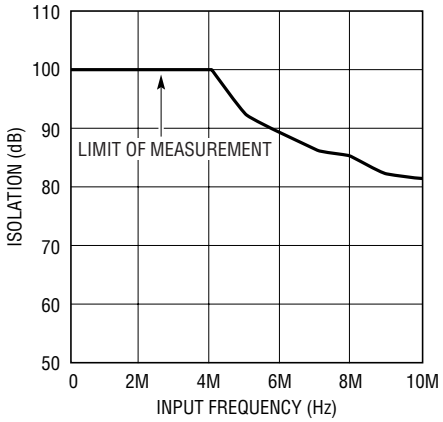
TYPICAL PERFORMANCE CHARACTERISTICS

Channel-to-Channel Isolation (Worst Pair) Bipolar Mode, PGA = 0



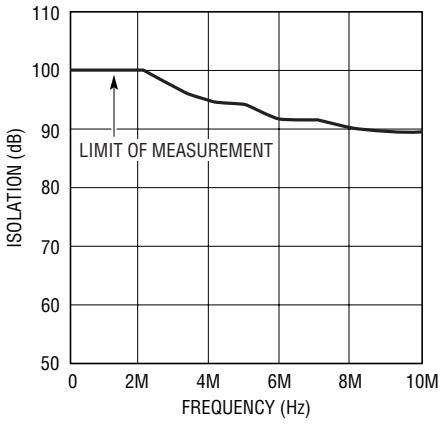
LTC1850/51 G12

Channel-to-Channel Isolation (Worst Pair), Unipolar Mode, PGA = 0



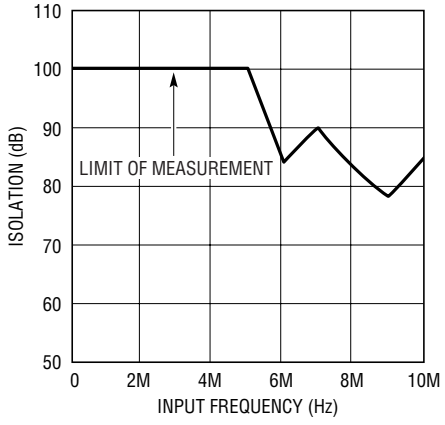
LTC1850/51 G15

Channel-to-Channel Isolation (Worst Pair), Unipolar Mode, PGA = 1



LTC1850/51 G18

Channel-to-Channel Isolation (Worst Pair), Bipolar Mode, PGA =1



LTC1850/51 G17

PIN FUNCTIONS

CH0 to CH7 (Pins 1 to 8): Analog Input Pins. Input pins can be used single ended relative to the analog input common pin (COM) or differentially in pairs (CH0 and CH1, CH2 and CH3, CH4 and CH5, CH6 and CH7).

COM (Pin 9): Analog Input Common Pin. For single-ended operation (DIFF = 0), COM is the "–" analog input. COM is disabled when DIFF is high.

REFOUT (Pin 10): Internal 2.5V Reference Output. Requires bypass to analog ground plane with 1µF.

REFIN (Pin 11): Reference Mode Select/Reference Buffer Input. REFIN selects the Reference mode and acts as the reference buffer Input. REFIN tied to ground will produce 2.048V on the REFCOMP pin. REFIN tied to the positive supply disables the reference buffer to allow REFCOMP to be driven externally. For voltages between 1V and 2.6V, the reference buffer produces an output voltage on the REFCOMP pin equal to 1.6384 times the voltage on REFIN (4.096V on REFCOMP for a 2.5V input on REFIN).

REFCOMP (Pin 12): Reference Buffer Output. REFCOMP sets the full-scale input span. The reference buffer produces an output voltage on the REFCOMP pin equal to 1.6384 times the voltage on the REFIN pin (4.096V on REFCOMP for a 2.5V input on REFIN). REFIN tied to ground will produce 2.048V on the REFCOMP pin. REFCOMP can be driven externally if REFIN is tied to the positive supply. Requires bypass to analog ground plane with 10µF tantalum in parallel with 0.1µF ceramic or 10µF ceramic.

GND (Pin 13): Ground. Tie to analog ground plane.

V_{DD} (Pin 14): 5V Supply. Short to Pin 15.

V_{DD} (Pin 15): 5V Supply. Bypass to GND with 10µF tantalum in parallel with 0.1µF ceramic or 10µF ceramic.

GND (Pin 16): Ground for Internal Logic. Tie to analog ground plane.

$DIFF_{OUT}$/S6 (Pin 17): Three-State Digital Data Output. Active when $\overline{RD}$ is low. Following a conversion, the single-ended/differential bit of the present conversion is available on this pin concurrent with the conversion result. In Readback mode, the single-ended/differential bit of the current sequencer location (S6) is available on this pin. The output swings between OV_{DD} and OGND.

$A2_{OUT}$/S5, $A1_{OUT}$/S4, $A0_{OUT}$/S3 (Pins 18 to 20): Three-State Digital MUX Address Outputs. Active when $\overline{RD}$ is low. Following a conversion, the MUX address of the present conversion is available on these pins concurrent with the conversion result. In Readback mode, the MUX address of the current sequencer location (S5-S3) is available on these pins. The outputs swing between OV_{DD} and OGND.

D9/S2 (Pin 21, LTC1850): Three-State Digital Data Output. Active when $\overline{RD}$ is low. Following a conversion, bit 9 of the present conversion is available on this pin. In Readback mode, the unipolar/bipolar bit of the current sequencer location (S2) is available on this pin. The output swings between OV_{DD} and OGND.

D11/S2 (Pin 21, LTC1851): Three-State Digital Data Output. Active when $\overline{RD}$ is low. Following a conversion, bit 11 of the present conversion is available on this pin. In Readback mode, the unipolar/bipolar bit of the current sequencer location (S2) is available on this pin. The output swings between OV_{DD} and OGND.

D8/S1 (Pin 22, LTC1850): Three-State Digital Data Outputs. Active when $\overline{RD}$ is low. Following a conversion, bit 8 of the present conversion is available on this pin. In Readback mode, the gain bit of the current sequencer location (S1) is available on this pin. The output swings between OV_{DD} and OGND.

D10/S1 (Pin 22, LTC1851): Three-State Digital Data Outputs. Active when $\overline{RD}$ is low. Following a conversion, bit 10 of the present conversion is available on this pin. In Readback mode, the gain bit of the current sequencer location (S1) is available on this pin. The output swings between OV_{DD} and OGND.

D7/S0 (Pin 23, LTC1850): Three-State Digital Data Outputs. Active when $\overline{RD}$ is low. Following a conversion, bit 7 of the present conversion is available on this pin. In Readback mode, the end of sequence bit of the current sequencer location (S0) is available on this pin. The output swings between OV_{DD} and OGND.

PIN FUNCTIONS

D9/S0 (Pin 23, LTC1851): Three-State Digital Data Outputs. Active when $\overline{RD}$ is low. Following a conversion, bit 9 of the present conversion is available on this pin. In Readback mode, the end of sequence bit of the current sequencer location (S0) is available on this pin. The output swings between OV_{DD} and OGND.

D6 to D0 (Pins 24 to 30, LTC1850): Three-State Digital Data Outputs. Active when $\overline{RD}$ is low. The outputs swing between OV_{DD} and OGND.

D8 to D0 (Pins 24 to 32, LTC1851): Three-State Digital Data Outputs. Active when $\overline{RD}$ is low. The outputs swing between OV_{DD} and OGND.

NC (Pins 31, 32, LTC1850): No Connect. There is no internal connection to these pins.

$\overline{BUSY}$ (Pin 33): Converter Busy Output. The $\overline{BUSY}$ output has two functions. At the start of a conversion, $\overline{BUSY}$ will go low and remain low until the conversion is completed. The rising edge may be used to latch the output data. $\overline{BUSY}$ will also go low while the part is in Program/Readback mode (M1 high, M0 low) and remain low until M0 is brought back high. The output swings between OV_{DD} and OGND.

OGND (Pin 34): Digital Data Output Ground. Tie to analog ground plane. May be tied to logic ground if desired.

OV_{DD} (Pin 35): Digital Data Output Supply. Normally tied to 5V, can be used to interface with 3V digital logic. Bypass to OGND with 10µF tantalum in parallel with 0.1µF ceramic or 10µF ceramic. See Table 5.

M0 (Pin 36): Mode Select Pin 0. Used in conjunction with M1 to select operating mode. See Table 5

PGA (Pin 37): Gain Select Input. A high logic level selects gain = 1, a low logic level selects gain = 2.

$\overline{UNI}$/BIP (Pin 38): Unipolar/Bipolar Select Input. Logic low selects a unipolar input span, a high logic level selects a bipolar input span.

A0 to A2 (Pins 39 to 41): MUX Address Input Pins.

DIFF (Pin 42): Single-Ended/Differential Select Input. A low logic level selects single-ended mode, a high logic level selects differential mode.

$\overline{WR}$ (Pin 43): Write Input. In Direct Address mode, $\overline{WR}$ low enables the MUX address and configuration input pins (Pins 37 to 42). $\overline{WR}$ can be tied low or the rising edge of $\overline{WR}$ can be used to latch the data. In Program mode, $\overline{WR}$ is used to program the sequencer. $\overline{WR}$ low enables the MUX address and configuration input pins (Pins 37 to 42). The rising edge of $\overline{WR}$ latches the data and increments the counter to the next sequencer location.

$\overline{RD}$ (Pin 44): Read Input. During normal operation, $\overline{RD}$ enables the output drivers when $\overline{CS}$ is low. In Readback mode (M1 high, M0 low), $\overline{RD}$ going low reads the current sequencer location, $\overline{RD}$ high advances to the next sequencer location.

$\overline{CONVST}$ (Pin 45): Conversion Start Input. This active low signal starts a conversion on its falling edge.

$\overline{CS}$ (Pin 46): Chip Select Input. The chip select input must be low for the ADC to recognize the $\overline{CONVST}$ and $\overline{RD}$ inputs. If $\overline{SHDN}$ is low, a low logic level on $\overline{CS}$ selects Nap mode; a high logic level on $\overline{CS}$ selects Sleep mode.

$\overline{SHDN}$ (Pin 47): Power Shutdown Input. A low logic level will invoke the Shutdown mode selected by the $\overline{CS}$ pin. $\overline{CS}$ low selects Nap mode, $\overline{CS}$ high selects Sleep mode. Tie high if unused.

M1 (Pin 48): Mode Select Pin 1. Used in conjunction with M0 to select operating mode.

PIN FUNCTIONS

PIN	NAME	DESCRIPTION	NOMINAL (V) MIN	NOMINAL (V) TYP	NOMINAL (V) MAX	ABSOLUTE MAXIMUM (V) MIN	ABSOLUTE MAXIMUM (V) MAX
1 to 8	CH0 to CH7	Analog Inputs	0		V_{DD}	–0.3	V_{DD} + 0.3
9	COM	Analog Input Common Pin	0		V_{DD}	–0.3	V_{DD} + 0.3
10	REFOUT	2.5V Reference Output		2.5		–0.3	V_{DD} + 0.3
11	REFIN	Reference Buffer Input	0	2.5	V_{DD}	–0.3	V_{DD} + 0.3
12	REFCOMP	Reference Buffer Output		4.096		–0.3	V_{DD} + 0.3
13	GND	Ground, Substrate Ground		0		–0.3	V_{DD} + 0.3
14	V_{DD}	Supply	4.75	5	5.25	–0.3	6
15	V_{DD}	Supply	4.75	5	5.25	–0.3	6
16	GND	Ground		0		–0.3	V_{DD} + 0.3
17	$DIFF_{OUT}$/S6	Single-Ended/Differential Output	OGND		OV_{DD}	–0.3	V_{DD} + 0.3
18	$A2_{OUT}$/S5	MUX Address Output	OGND		OV_{DD}	–0.3	V_{DD} + 0.3
19	$A1_{OUT}$/S4	MUX Address Output	OGND		OV_{DD}	–0.3	V_{DD} + 0.3
20	$A0_{OUT}$/S3	MUX Address Output	OGND		OV_{DD}	–0.3	V_{DD} + 0.3
21	D9/S2 (LTC1850)	Data Output	OGND		OV_{DD}	–0.3	V_{DD} + 0.3
21	D11/S2 (LTC1851)	Data Output	OGND		OV_{DD}	–0.3	V_{DD} + 0.3
22	D8/S1 (LTC1850)	Data Output	OGND		OV_{DD}	–0.3	V_{DD} + 0.3
22	D10/S1 (LTC1851)	Data Output	OGND		OV_{DD}	–0.3	V_{DD} + 0.3
23	D7/S0 (LTC1850)	Data Output	OGND		OV_{DD}	–0.3	V_{DD} + 0.3
23	D9/S0 (LTC1851)	Data Output	OGND		OV_{DD}	–0.3	V_{DD} + 0.3
24 to 30	D6 to D0 (LTC1850)	Data Outputs	OGND		OV_{DD}	–0.3	V_{DD} + 0.3
24 to 32	D8 to D0 (LTC1851)	Data Outputs	OGND		OV_{DD}	–0.3	V_{DD} + 0.3
31 to 32	NC (LTC1850)						
33	$\overline{BUSY}$	Converter Busy Output	OGND		OV_{DD}	–0.3	V_{DD} + 0.3
34	OGND	Output Ground		0		–0.3	V_{DD} + 0.3
35	OV_{DD}	Output Supply	2.7	5	5.25	–0.3	6
36	M0	Mode Select Pin 0	0		V_{DD}	–0.3	10
37	PGA	Gain Select Input	0		V_{DD}	–0.3	10
38	$\overline{UNI}$/BIP	Unipolar/Bipolar Input	0		V_{DD}	–0.3	10
39 to 41	A0 to A2	MUX Address Inputs	0		V_{DD}	–0.3	10
42	DIFF	Single-Ended/Differential Input	0		V_{DD}	–0.3	10
43	$\overline{WR}$	Write Input, Active Low	0		V_{DD}	–0.3	10
44	$\overline{RD}$	Read Input, Active Low	0		V_{DD}	–0.3	10
45	$\overline{CONVST}$	Conversion Start Input, Active Low	0		V_{DD}	–0.3	10
46	$\overline{CS}$	Chip Select Input, Active Low	0		V_{DD}	–0.3	10
47	$\overline{SHDN}$	Shutdown Input, Active Low	0		V_{DD}	–0.3	10
48	M1	Mode Select Pin 1	0		V_{DD}	–0.3	10

APPLICATIONS INFORMATION

The LTC1850/LTC1851 are complete and very flexible data acquisition systems. They consist of a 10-bit/12-bit, 1.25Msps capacitive successive approximation A/D converter with a wideband sample-and-hold, a configurable 8-channel analog input multiplexer, an internal reference and reference buffer amplifier, a 16-bit parallel digital output and digital control logic including a programmable sequencer.

CONVERSION DETAILS

The core analog-to-digital converter in the LTC1850/LTC1851 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 10-bit/12-bit parallel output. Conversion start is controlled by the $\overline{CS}$ and $\overline{CONVST}$ inputs. At the start of the conversion, the successive approximation register (SAR) is reset. Once a conversion cycle is begun, it cannot be restarted. During the conversion, the internal differential 10-bit/12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). The outputs of the analog input multiplexer are connected to the sample-and-hold capacitors (C_{SAMPLE}) during the acquire phase and the comparator offset is nulled by the zeroing switches. In this acquire phase, a minimum delay of 150ns will provide enough time for the sample-and-hold capacitors to acquire the analog signal. During the convert phase, the comparator zeroing switches are open, putting the comparator into compare mode. The input switches connect C_{SAMPLE} to ground, transferring the differential analog input charge onto the summing junction. This input charge is successively compared with the binary weighted charges supplied by the differential capacitive DAC. Bit decisions are made by the high speed comparator. At the end of the conversion, the differential DAC output balances the input charges. The SAR contents (a 10-bit/12-bit data word), which represents the difference of the analog input multiplexer outputs, and the 4-bit address word are loaded into the 14-bit/16-bit output latches.

DYNAMIC PERFORMANCE

Signal-to-Noise Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency. The effective number of bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$ENOB = [S/(N + D) – 1.76]/6.02$$

where ENOB is the effective number of bits and S/(N + D) is expressed in dB. At the maximum sampling rate of 1.25MHz, the LTC1850/LTC1851 maintain near ideal ENOBs up to and beyond the Nyquist input frequency of 625kHz.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20Log\frac{\sqrt{V2^2 + V3^2 + V4^2 + ...Vn^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. The LTC1850/LTC1851 have good distortion performance up to the Nyquist frequency and beyond.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

APPLICATIONS INFORMATION

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa ± fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\left(fa \pm fb\right) = 20Log\frac{\text{Amplitude at}\left(fa \pm fb\right)}{\text{Amplitude at fa}}$$

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal.

The full-linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB for the LTC1851 (11 effective bits) or 56dB for the LTC1850 (9 effective bits). The LTC1850/LTC1851 have been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

ANALOG INPUT MULTIPLEXER

The analog input multiplexer is controlled using the single-ended/differential pin (DIFF), three MUX address pins (A2, A1, A0), the unipolar/bipolar pin ($\overline{UNI}$/BIP) and the gain select pin (PGA). The single-ended/differential pin (DIFF) allows the user to configure the MUX as eight single-ended channels relative to the analog input common pin (COM) when DIFF is low or as four differential pairs (CH0 and CH1, CH2 and CH3, CH4 and CH5, CH6 and CH7) when DIFF is high. The channels (and polarity in the differential case) are selected using the MUX address inputs as shown in Table 1. Unused inputs (including the COM in the differential case) should be grounded to prevent noise coupling.

Table 1. Multiplexer Address Table

MUX ADDRESS				SINGLE-ENDED CHANNEL SELECTION								
DIFF	A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	0	+								–
0	0	0	1		+							–
0	0	1	0			+						–
0	0	1	1				+					–
0	1	0	0					+				–
0	1	0	1						+			–
0	1	1	0							+		–
0	1	1	1								+	–

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION								
DIFF	A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
1	0	0	0	+	–							*
1	0	0	1	–	+							*
1	0	1	0			+	–					*
1	0	1	1			–	+					*
1	1	0	0					+	–			*
1	1	0	1					–	+			*
1	1	1	0							+	–	*
1	1	1	1							–	+	*

*Not used in differential mode. Connect to GND.

In addition to selecting the MUX channel, the LTC1850/LTC1851 also allows the user to select between two gains and unipolar or bipolar inputs for a total of four input spans. PGA high selects a gain of 1 (the input span is equal to the voltage on REFCOMP). PGA low selects a gain of 2 where the input span is equal to half of the voltage on REFCOMP. $\overline{UNI}$/BIP low selects a unipolar input span, $\overline{UNI}$/BIP high selects a bipolar input span. Table 2 summarizes the possible input spans.

APPLICATIONS INFORMATION

Table 2. Input Span Table

		INPUT SPAN	
$\overline{UNI}$/BIP	PGA		REFCOMP = 4.096V
0	0	0 – REFCOMP/2	0 – 2.048V
0	1	0 – REFCOMP	0 – 4.096V
1	0	±REFCOMP/4	±1.024V
1	1	±REFCOMP/2	±2.048V

It should be noted that the bipolar input span of the LTC1850/LTC1851 does not allow negative inputs with respect to ground. The LTC1850/LTC1851 have a unique differential sample-and-hold circuit that allows rail-to-rail inputs. The ADC will always convert the difference of the "+" and "–" inputs independent of the common mode voltage. The common mode rejection holds up to high frequencies. The only requirement is that both inputs can not exceed the V_{DD} power supply voltage or ground. When a bipolar input span is selected the "+" input can swing ±full scale relative to the "–" input but neither input can exceed V_{DD} or go below ground.

Integral nonlinearity errors (INL) and differential nonlinearity errors (DNL) are independent of the common mode voltage, however, the bipolar zero error (BZE) will vary. The change in BZE is typically less than 0.1% of the common mode voltage.

Some AC applications may have their performance limited by distortion. The ADC and many other circuits exhibit higher distortion when signals approach the supply or ground. THD will degrade as the inputs approach either power supply rail. Distortion can be reduced by reducing the signal amplitude and keeping the common mode voltage at approximately midsupply.

Driving the Analog Inputs

The inputs of the LTC1850/LTC1851 are easy to drive. Each of the analog inputs can be used as a single-ended input relative to the input common pin (CH0-COM, CH1-COM, etc.) or in pairs (CH0 and CH1, CH2 and CH3, CH4 and CH5, CH6 and CH7) for differential inputs. Regardless of the MUX configuration, the "+" and "–" inputs are sampled at the same instant. Any unwanted signal that is common mode to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, then the LTC1850/LTC1851 inputs can be driven directly. As source impedance increases, so will acquisition time. For minimum acquisition time with high source impedance, a buffer amplifier should be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 150ns for full throughput rate).

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of +1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz should be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 20MHz to ensure adequate small-signal settling for full throughput rate. The following list is a summary of the op amps that are suitable for driving the LTC1850/LTC1851, more detailed information is available in the Linear Technology Databooks, the LinearView™ CD-ROM and on our web site at www.linear-tech.com.

LT®1360: 50MHz Voltage Feedback Amplifier. ±2.5V to ±15V supplies. 5mA supply current. Low distortion.

LT1363: 70MHz Voltage Feedback Amplifier. ±2.5V to ±15V supplies. 7.5mA supply current. Low distortion.

LT1364/LT1365: Dual and Quad 70MHz Voltage Feedback Amplifiers. ±2.5V to ±15V supplies. 7.5mA supply current per amplifier. Low distortion.

LinearView is a trademark of Linear Technology Corporation.

APPLICATIONS INFORMATION

LT1468/LT1469: Single and Dual 90MHz Voltage Feedback Amplifier. ±5V to ±15V supplies. 7mA supply current per amplifier. Lowest noise and low distortion.

LT1630/LT1631: Dual and Quad 30MHz Rail-to-Rail Voltage Feedback Amplifiers. Single 3V to ±15V supplies. 3.5mA supply current per amplifier. Low noise and low distortion.

LT1632/LT1633: Dual and Quad 45MHz Rail-to-Rail Voltage Feedback Amplifiers. Single 3V to ±15V supplies. 4.3mA supply current per amplifier. Low distortion.

LT1806/LT1807: Single and Dual 325MHz Rail-to-Rail Voltage Feedback Amplifier. Single 3V to ±5V supplies. 13mA supply current. Lowest distortion.

LT1809/LT1810: Single and Dual 180MHz Rail-to-Rail Voltage Feedback Amplifier. Single 3V to ±15V supplies. 20mA supply current. Lowest distortion.

LT1812/LT1813: 100MHz Voltage Feedback Amplifier. Single 5V to ±5V supplies. 3.6mA supply current. Low noise and low distortion.

Input Filtering

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1850/LTC1851 noise and distortion. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For instance, a 100Ω source resistor and a 1000pF capacitor to ground on the input will limit the input bandwidth to 1.6MHz. The capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling glitch sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can also generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

REFERENCE

The LTC1850/LTC1851 include an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.500V and has a very flexible 3-pin interface. REFOUT is the 2.5V bandgap output, REFIN is the input to the reference buffer and REFCOMP is the reference buffer output. REFOUT must be bypassed with a 1µF or greater capacitor to ground for stability. The input span is determined by the voltage appearing on the REFCOMP pin as shown in Table 2. The reference buffer has a gain of 1.6384 and is factory trimmed by forcing an external 2.500V on the REFIN pin and trimming REFCOMP to 4.096V. The 3-pin interface allows for three pin-strappable Reference modes as well as two additional external Reference modes. For voltages on the REFIN pin ranging from 1V to 2.6V, the output voltage on REFCOMP will equal 1.6384 times the voltage on the REFIN pin. In this mode, the REFIN pin can be tied to REFOUT to utilize the internal 2.5V reference to get 4.096V on REFCOMP or driven with an external reference or DAC. If REFIN is tied low, the internal 2.5V reference divided by 2 (1.25V) is connected internally to the input of the reference buffer resulting in 2.048V on REFCOMP. If REFIN is tied high, the reference buffer is disabled and REFCOMP can be tied to REFOUT to achieve a 2.5V span or driven with an external reference or DAC. Table 3 summarizes the Reference modes.

Table 3. Reference Mode Table

MODE	REFIN	REFCOMP
REFIN Tied Low	= GND	2.048V Output
REFIN is Buffer Input	1V to 2.6V Input	1.6384V to 4.26V Output (1.6384 • REFIN)
REFIN Tied High	= V_{DD}	Input, 6.4kΩ to Ground

Full Scale and Offset

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero during a calibration sequence. Offset error must be adjusted before full-scale error. Zero offset is achieved by adjusting

APPLICATIONS INFORMATION

the offset applied to the "–" input. For single-ended inputs, this offset should be applied to the COM pin. For differential inputs, the "–" input is dictated by the MUX address. For zero offset error, apply 0.5LSB (actual voltage will vary with input span selected) to the "+" input and adjust the offset at the "–" input until the output code flickers between 0000 0000 0000 and 0000 0000 0001 for the LTC1851 and between 00 0000 0000 and 00 0000 0001 for the LTC1850.

As mentioned earlier, the internal reference is factory trimmed to 2.500V. To make sure that the reference buffer gain is not compensating for trim errors in the reference, REFCOMP is trimmed to 4.096V with an accurate external 2.5V reference applied to REFIN. Likewise, to make sure that the full-scale gain trim is not compensating for errors in the reference buffer gain, the input full-scale gain is trimmed with an accurate 4.096V reference applied to REFCOMP (REFIN = 5V to disable the reference buffer). This allows the use of either a 2.5V reference applied to REFIN or a 4.096V reference applied to REFCOMP to achieve accurate results. Full-scale errors can be trimmed to zero by adjusting the appropriate reference voltage. For unipolar inputs, an input voltage of FS – 1.5LSBs should be applied to the "+" input and the appropriate reference adjusted until the output code flickers between 1111 1111 1110 and 1111 1111 1111 for the LTC1851 and between 11 1111 1110 and 11 1111 1111 for the LTC1850.

For bipolar inputs, an input voltage of FS – 1.5LSBs should be applied to the "+" input and the appropriate reference adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111 for the LTC1851 and between 01 1111 1110 and 01 1111 1111 for the LTC1850.

These adjustments as well as the factory trims affect all channels. The channel-to-channel offset and gain error matching are guaranteed by design to meet the specifications in the Converter Characteristics table.

OUTPUT DATA FORMAT

The LTC1850/LTC1851 have a 14-bit/16-bit parallel output. The output word normally consists of a 10-bit/12-bit conversion result data word and a 4-bit address (three address bits $A2_{OUT}$, $A1_{OUT}$, $A0_{OUT}$ and the $DIFF_{OUT}$ bit). The output drivers are enabled when $\overline{RD}$ is low provided the chip is selected ($\overline{CS}$ is low). All 14/16 data output pins and $\overline{BUSY}$ are supplied by OV_{DD} and OGND to allow easy interface to 3V or 5V digital logic.

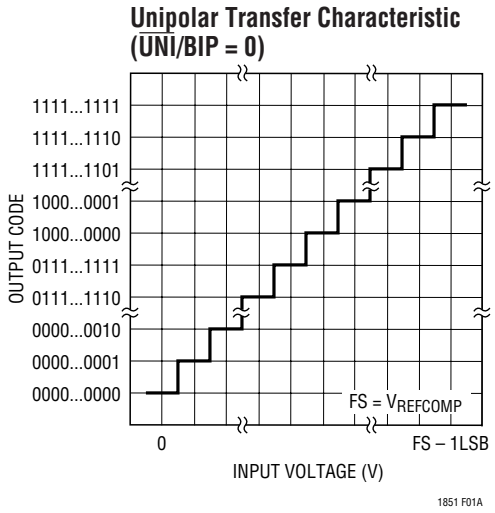
The data format of the conversion result is automatically selected and determined by the $\overline{UNI}$/BIP input pin. If the $\overline{UNI}$/BIP pin is low indicating a unipolar input span (0 – REFCOMP assuming PGA = 1), the format for the data is straight binary with 1 LSB = FS/4096 (1mV for REFCOMP = 4.096V) for the LTC1851 and 1LSB = FS/1024 (4mV for REFCOMP = 4.096V) for the LTC1850.

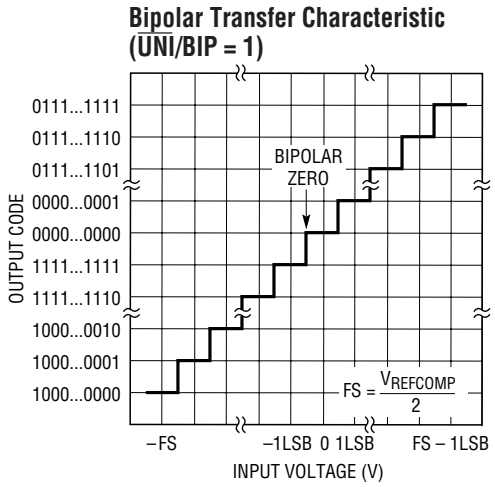
If the $\overline{UNI}$/BIP pin is high indicating a bipolar input span (±REFCOMP/2 for PGA = 1), the format for the data is two's complement binary with 1 LSB = [(+FS) – (–FS)]/4096 (1mV for REFCOMP = 4.096V) for the LTC1851 and 1LSB = [(+FS) – (–FS)]/1024 (4mV for REFCOMP = 4.096V) for the LTC1850.

In both cases, the code transitions occur midway between successive integer LSB values (i.e., –FS + 0.5LSB, –FS + 1.5LSB, ... –1.5LSB, –0.5LSB, 0.5LSB, 1.5LSB, ... FS – 1.5LSB, FS – 0.5LSB).

The three most significant bits of the data word (D11, D10, and D9 for the LTC1851; D9, D8 and D7 for the LTC1850) also function as output bits when reading the contents of the programmable sequencer. During readback, a 7-bit status word (S6-S0) containing the contents of the current sequencer location is available when $\overline{RD}$ is low. The individual bits of the status word are outlined in Figure 1. During readback, the D8 to D0 pins (LTC1851) or D6 to D0 pins (LTC1850) remain high impedance irrespective of the state of $\overline{RD}$.

APPLICATIONS INFORMATION





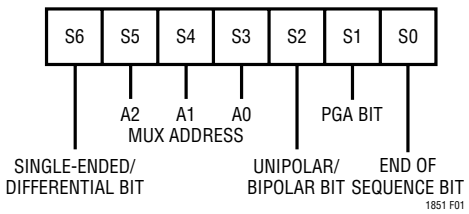


Figure 1. Readback Status Word

BOARD LAYOUT AND BYPASSING

To obtain the best performance from the LTC1850/LTC1851, a printed circuit board with ground plane is required. The ground plane under the ADC area should be as free of breaks and holes as possible, such that a low impedance path between all ADC grounds and all ADC decoupling capacitors is provided. It is critical to prevent digital noise from being coupled to the analog inputs, reference or analog power supply lines. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

An analog ground plane separate from the logic system ground should be established under and around the ADC. Pin 34 (OGND), Pin 13 (GND), Pin 16 (ADC's GND) and all other analog grounds should be connected to this single analog ground point. The bypass capacitors should also be connected to this analog ground plane. No other digital grounds should be connected to this analog ground plane. In some applications, it may be desirable to connect the OV_{DD} to the logic system supply and OGND to the logic system ground. In these cases, OV_{DD} should be bypassed to OGND instead of the analog ground plane.

Low impedance analog and digital power supply common returns are essential to the low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversions or by using three-state buffers to isolate the ADC bus. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1850/LTC1851 have differential inputs to minimize noise coupling. Common mode noise on the "+" and "–" inputs will be rejected by the input CMRR. The LTC1850/LTC1851 will hold and convert the difference between whichever input is selected as the "+" input and whichever input is selected as the "–" input. Leads to the inputs should be kept as short as possible.

APPLICATIONS INFORMATION

SUPPLY BYPASSING

High quality, low series resistance ceramic 10µF bypass capacitors should be used. Surface mount ceramic capacitors provide excellent bypassing in a small board space. Alternatively, 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors can be used. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

DIGITAL INTERFACE

Internal Clock

The A/D converter has an internal clock that eliminates the need of synchronization between the external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 550ns, and a maximum conversion time over the full operating temperature range of 650ns. No external adjustments are required. The guaranteed maximum acquisition time is 150ns. In addition, a throughput time of 800ns and a minimum sampling rate of 1.25Msps is guaranteed.

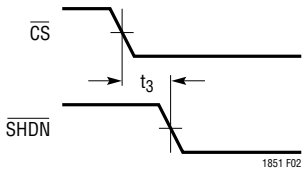


Figure 2. $\overline{CS}$ to $\overline{SHDN}$ Timing

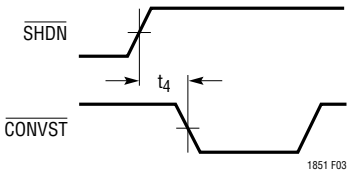


Figure 3. $\overline{SHDN}$ to $\overline{CONVST}$ Wake-Up Timing

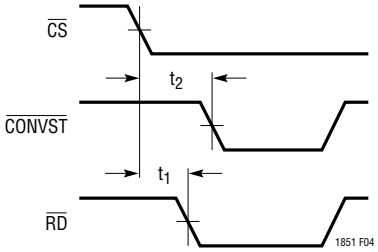


Figure 4. $\overline{CS}$ to $\overline{CONVST}$ Setup Timing

Power Shutdown

The LTC1850/LTC1851 provide two power shutdown modes, Nap and Sleep, to save power during inactive periods. The Nap mode reduces the power to 5mW and leaves only the digital logic and reference powered up. The wake-up time from Nap to active is 200ns. In Sleep mode, all bias currents are shut down and only leakage current remains—about 50µA. Wake-up time from sleep mode is much slower since the reference circuit must power-up and settle to 0.005% for full 12-bit accuracy (0.02% for full 10-bit accuracy). Sleep mode wake-up time is dependent on the value of the capacitor connected to the REFCOMP (Pin 12). The wake-up time is 10ms with the recommended 10µF capacitor.

Shutdown is controlled by Pin 47 ($\overline{SHDN}$); the ADC is in shutdown when it is low. The shutdown mode is selected with Pin 46 ($\overline{CS}$); low selects Nap.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: $\overline{CONVST}$, $\overline{CS}$ and $\overline{RD}$. A transition from 1 to 0 applied to the $\overline{CONVST}$ pin will start a conversion after the ADC has been selected (i.e., $\overline{CS}$ is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output. $\overline{BUSY}$ is low during a conversion. If $\overline{CONVST}$ returns high at a critical point during the conversion it can create small errors. For the best results, ensure that $\overline{CONVST}$ returns high either within 400ns after the start of the conversion or after $\overline{BUSY}$ rises.

APPLICATIONS INFORMATION

Figures 5 through 9 show several different modes of operation. In modes 1a and 1b (Figures 5 and 6), $\overline{CS}$ and $\overline{RD}$ are both tied low. The falling edge of $\overline{CONVST}$ starts the conversion. The data outputs are always enabled and data can be latched with the BUSY rising edge. Mode 1a shows operation with a narrow logic low $\overline{CONVST}$ pulse. Mode 1b shows a narrow logic high $\overline{CONVST}$ pulse.

In mode 2 (Figure 7), $\overline{CS}$ is tied low. The falling edge of $\overline{CONVST}$ signal again starts the conversion. Data outputs are in three-state until read by the MPU with the $\overline{RD}$ signal. Mode 2 can be used for operation with a shared MPU databus.

In slow memory and ROM modes (Figures 8 and 9), $\overline{CS}$ is tied low and $\overline{CONVST}$ and $\overline{RD}$ are tied together. The MPU starts the conversion and reads the output with the $\overline{RD}$ signal. Conversions are started by the MPU or DSP (no external sample clock).

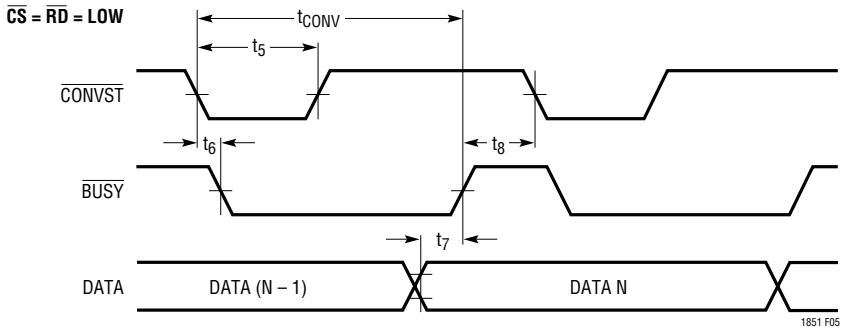


Figure 5. Mode 1a $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled

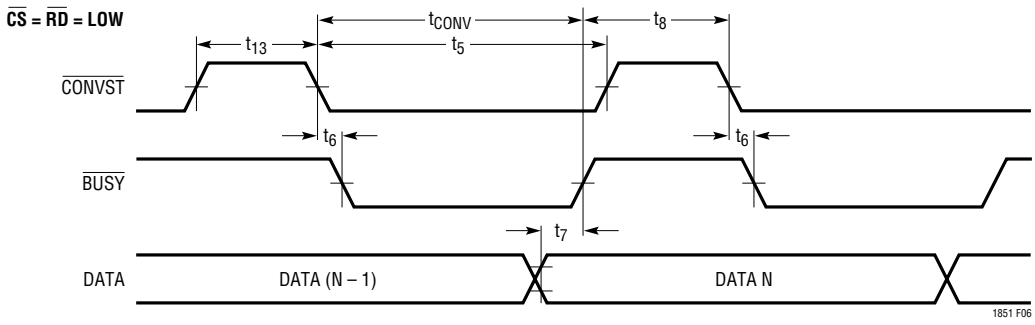


Figure 6. Mode 1b $\overline{CONVST}$ Starts a Conversion. Data is Read by $\overline{RD}$

APPLICATIONS INFORMATION

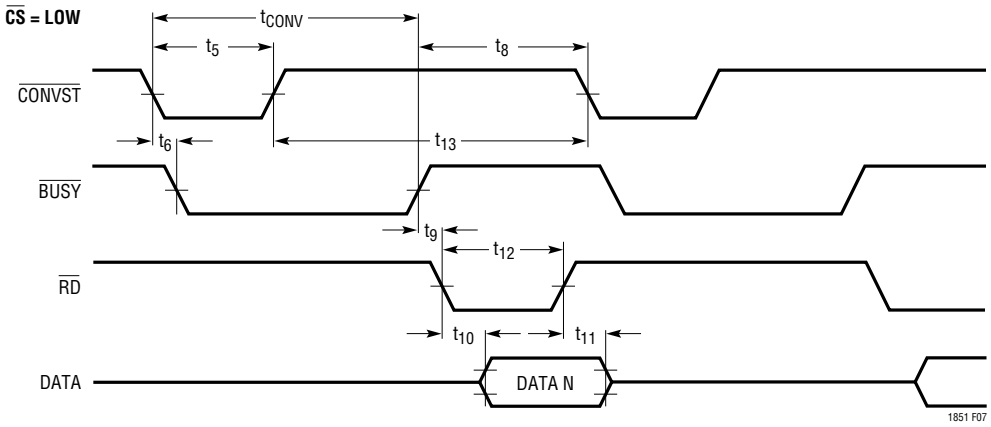


Figure 7. Mode 2 $\overline{\text{CONVST}}$ Starts a Conversion. Data is Read by $\overline{\text{RD}}$

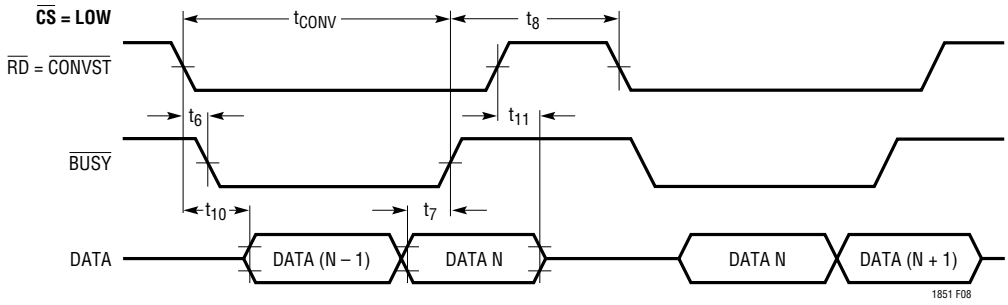


Figure 8. Slow Memory Mode Timing

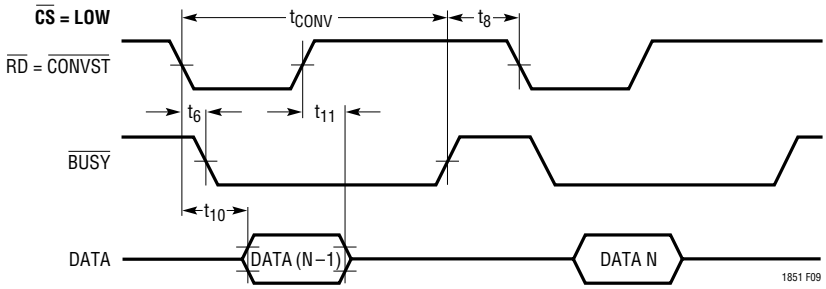


Figure 9. ROM Mode Timing

APPLICATIONS INFORMATION

In slow memory mode, the processor applies a logic low to RD (= CONVST), starting the conversion. BUSY goes low, forcing the processor into a Wait state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; BUSY goes high releasing the processor, and the processor takes RD (= CONVST) back high and reads the new conversion data.

In ROM mode, the processor takes RD (= CONVST) low, starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.

MODES OF OPERATION

Direct Address Mode

The simplest mode of operation is the Direct Address mode. This mode is selected when both the M1 and M0 pins are low. In this mode, the address input pins directly control the MUX and the configuration input pins directly control the input span. The address and configuration input pins are enabled when WR is low. WR can be tied low if the pins will be constantly driven or the rising edge of WR can be used to latch and hold the inputs for as long as WR is held high.

Scan Mode

Scan mode is selected when M1 is low and M0 is high. This mode allows the converter to scan through all of the input channels sequentially and repeatedly without the user having to provide an address. The address input pins (A2 to A0) are ignored but the DIFF, PGA and UNI/BIP pins are still enabled when WR is low. As in the direct address mode, WR can be held low or the rising edge of WR can be used to latch and hold the information on these pins for as long as WR is held high. The DIFF pin selects the scan pattern. If DIFF is held low, the scan pattern will consist of all eight channels in succession, single-ended relative to COM (CH0-COM, CH1-COM, CH2-COM, CH3-COM, CH4-COM, CH5-COM, CH6-COM, CH7-COM, repeat). At the maximum conversion rate the throughput rate for each channel would be 1.25Msps/8 or 156.25ksps. If DIFF is held high, the scan pattern will consist of four differential pairs (CH0-CH1, CH2-CH3, CH4-CH5, CH6-CH7, repeat). At the maximum conversion rate, the throughput rate for each pair would be 1.25Msps/4 or 312.5ksps. It is possible to drive the DIFF input pin while the part is in Scan mode to achieve combinations of single-ended and differential inputs. For instance, if the $A0_{OUT}$ pin is tied to the DIFF input pin, the scan pattern will consist of four single-ended inputs and two differential pairs (CH0-COM single-ended, CH1-COM single-ended, CH2-CH3 differential, CH4-COM single-ended, CH5-COM single-ended, CH6-CH7 differential, repeat).

The scan counter is reset to zero whenever the M0 pin changes state so that the first conversion after M0 rises will be MUX Address 000 (CH0-COM single-ended or CH0-CH1 differential depending on the state of the DIFF pin). A conversion is initiated by the falling edge of CONVST. After each conversion, the address counter is advanced (by one if DIFF is low, by two if DIFF is high) and the MUX address for the present conversion is available on the address output pins ($DIFF_{OUT}$, $A2_{OUT}$ to $A0_{OUT}$) along with the conversion result.

Program/Readback Mode

The LTC1850/LTC1851 include a sequencer that can be programmed to run a sequence of up to 16 locations containing a MUX address and input configuration. The MUX address and input configuration for each location are programmed using the DIFF, A2 to A0, UNI/BIP and PGA pins and are stored in memory along with an end-of-sequence (EOS) bit that is generated automatically. The six input address and configuration bits plus the EOS bit can be read back by accessing the 7-bit readback status word (S6-S0) through the data output pins. The sequencer memory is a 16×7 block of memory represented by the block diagram in Figure 10.

APPLICATIONS INFORMATION

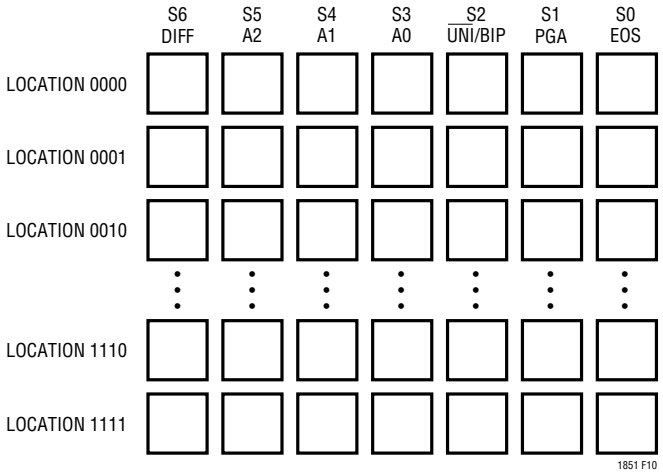


Figure 10. Sequencer Memory Block Diagram

The sequencer is accessed by taking the M1 mode pin high. With M1 high, the sequencer memory is accessed by taking the M0 mode pin low. This will cause BUSY to go low, disabling conversions during the programming and readback of the sequencer. The sequencer is reset to location 0000 whenever M1 or M0 changes state. One of these signals should be cycled prior to any read or write operation to guarantee that the sequencer will be programmed or read starting at location 0000.

The sequencer is programmed sequentially starting from location 0000. $\overline{RD}$ and $\overline{WR}$ should be held high, the appropriate signals applied to the DIFF pin, the A2 to A0 MUX address pins, the UNI/BIP pin and the PGA pin and $\overline{WR}$ taken low to write to the memory. The rising edge of $\overline{WR}$ will latch the data into memory and advance the pointer to the next sequencer location. Up to 16 locations can be programmed and the last location written before M0 is taken back high will be the last location in the sequence. After 16 writes, the pointer is reset to location 0000 and any subsequent writes will overwrite the previous contents and start a new sequence.

The sequencer memory can be read by holding $\overline{WR}$ high and driving $\overline{RD}$. Taking $\overline{RD}$ low accesses the sequencer memory and enables the data output pins. The sequencer should be reset to location 0000 (by pulsing M0 high) before beginning a read operation. The seven output bits will be available on the $DIFF_{OUT}$/S6, $A2_{OUT}$/S5, $A1_{OUT}$/S4, $A0_{OUT}$/S3, D11/S2, D10/S1 and D9/S0 pins (LTC1851) or $DIFF_{OUT}$/S6, $A2_{OUT}$/S5, $A1_{OUT}$/S4, $A0_{OUT}$/S3, D9/S2, D8/S1 and D7/S0 pins (LTC1850). The D8 to D0 (LTC1851) or D6 to D0 (LTC1850) data output pins will remain high impedance during readback. $\overline{RD}$ going high will return the data output pins to a high impedance state and advance the pointer to the next location. A logic 1 on the D9/S0 (or D7/S0) pin indicates the last location in the current sequence but all 16 locations can be read by continuing to clock $\overline{RD}$. After 16 reads, the pointer is reset to location 0000. When all programming and/or reading of the sequencer memory is complete, M0 is taken high. BUSY will come back high enabling $\overline{CONVST}$ and indicating that the part is ready to start a conversion.

APPLICATIONS INFORMATION

Sequence Run Mode

Once the sequencer is programmed, M0 is taken high. BUSY will also come back high enabling CONVST and the next falling CONVST will begin a conversion using the MUX address and input configuration stored in location 0000 of the sequencer memory. After each conversion, the sequencer pointer is advanced by one and the MUX address (the actual channel or channels being converted, not the sequencer pointer) for the present conversion is available on the address output pins along with the conversion result. When the sequencer finishes converting the last programmed location, the sequencer pointer will return to location 0000 for the next conversion. The sequencer will also reset to location 0000 anytime the M1 or M0 pin changes state.

The contents of the sequencer memory will be retained as long as power is continuously applied to the part. This allows the user to switch from Sequence Run mode to either Direct Address or Scan Mode and back without losing the programmed sequence. The part can also be disabled using $\overline{CS}$ or shutdown in Nap or Sleep mode without losing the programmed sequence. Table 5 outlines the operational modes of the LTC1850/LTC1851. Figures 11 and 12 show the timing diagrams for writing to, reading from and running a sequence with the LTC1850/LTC1851.

Table 5

OPERATION MODE	M1	M0	$\overline{WR}$	$\overline{RD}$	COMMENTS
Direct Address	0	0	0	$\overline{OE}$	Address and Configuration are Driven from External Pins
	0	0	↑	$\overline{OE}$	Address and Configuration are Latched on Rising Edge of $\overline{WR}$ or Falling Edge of $\overline{CONVST}$
Scan	0	1	0	$\overline{OE}$	Address is Provided by Internal Scan Counter, Configuration is Driven from External Pins
	0	1	↑	$\overline{OE}$	Configuration is Latched on Rising Edge of $\overline{WR}$ or Falling Edge of $\overline{CONVST}$
Program	1	0	↑	1	Write Sequencer Location, $\overline{WR}$ Low Enables Inputs, Rising Edge of $\overline{WR}$ Latches Data and Advances to Next Location
Readback	1	0	1	↓↑	Read Sequencer Location, Falling Edge of $\overline{RD}$ Enables Output, Rising Edge of $\overline{RD}$ Advances to Next Location
Sequence Run	1	1	X	$\overline{OE}$	Run Programmed Sequence, Falling Edge of $\overline{CONVST}$ Starts Conversion and Advances to Next Location

APPLICATIONS INFORMATION

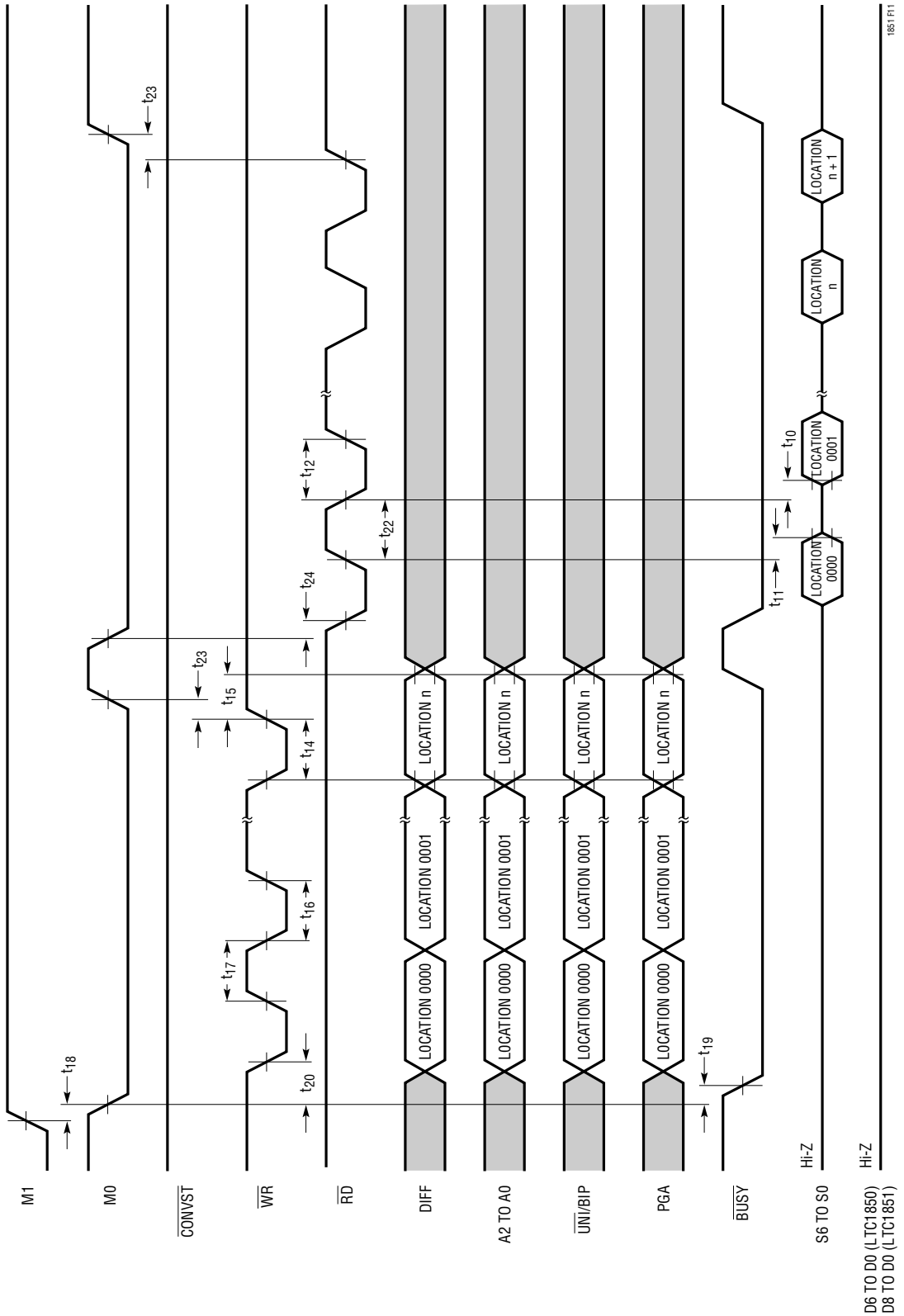


Figure 11. Sequencer I/O

APPLICATIONS INFORMATION

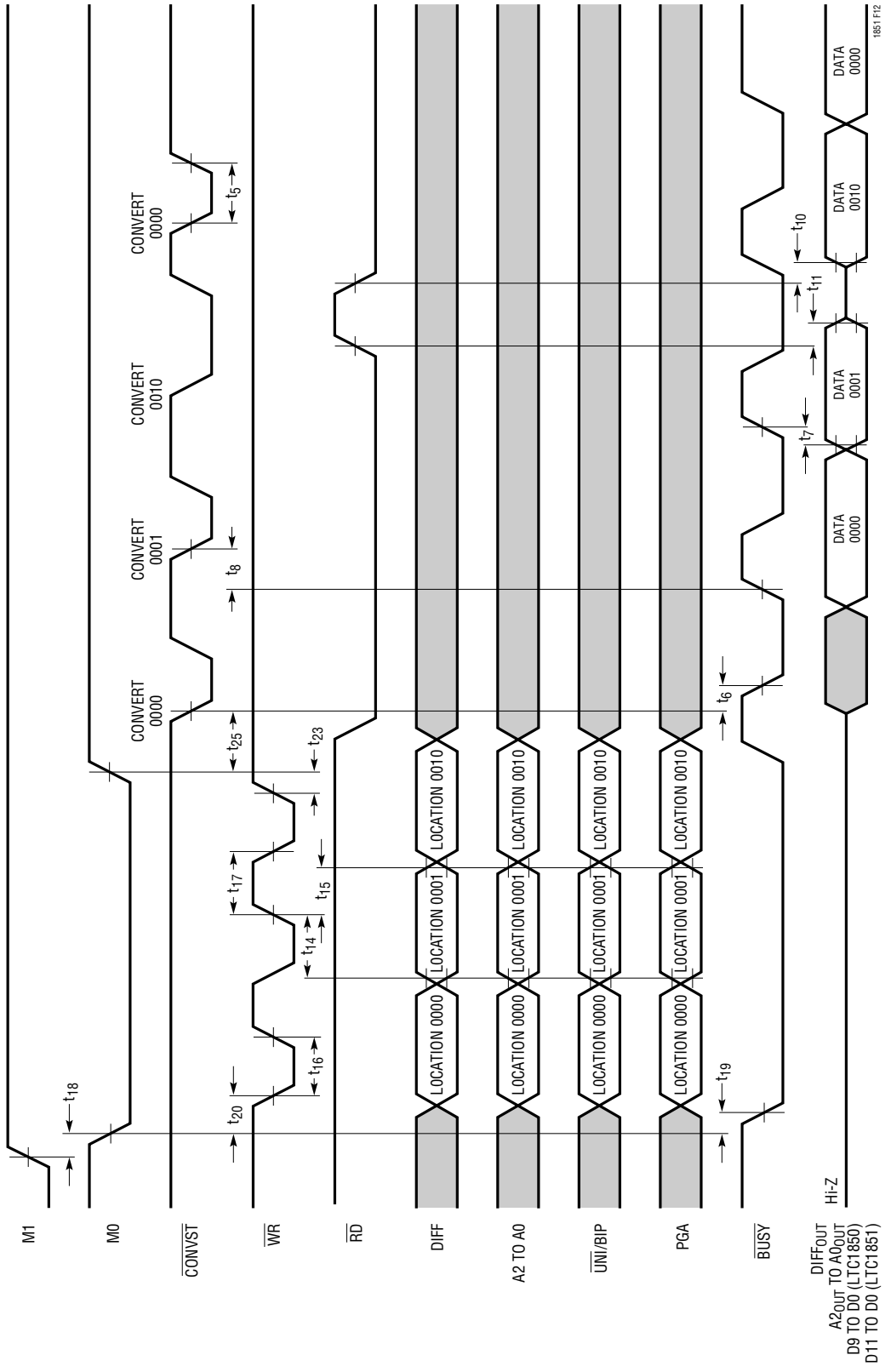
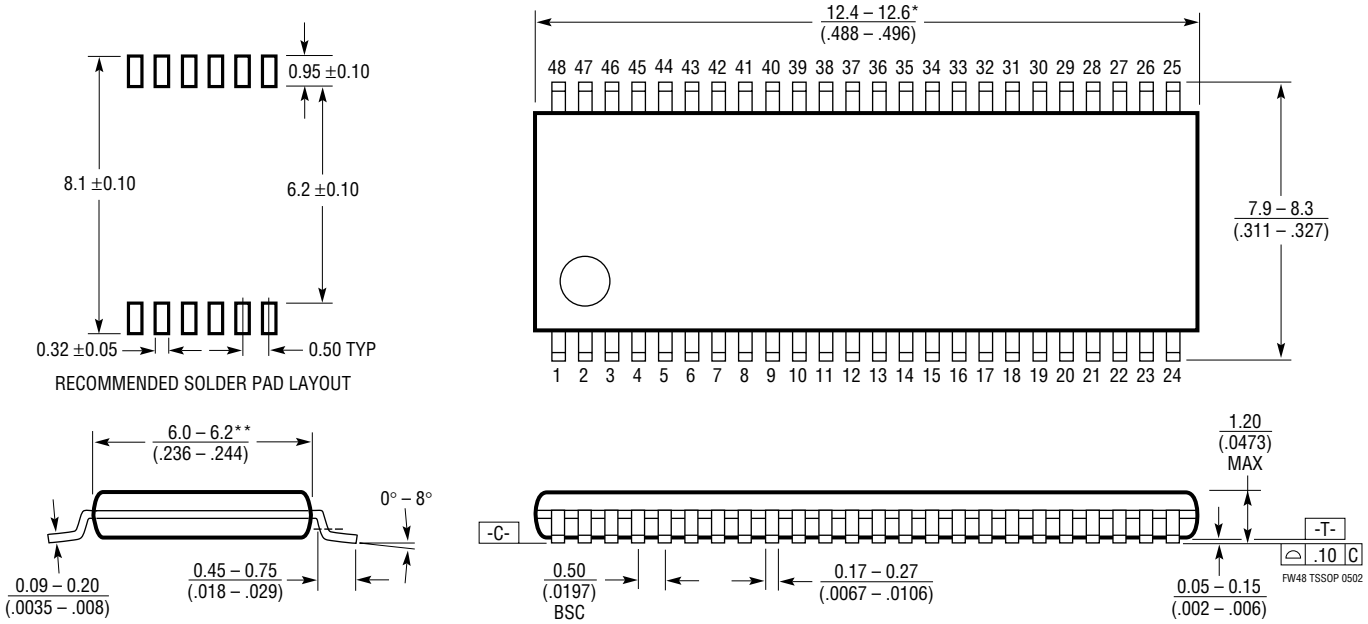


Figure 12. Programming and Running a Sequence

PACKAGE DESCRIPTION

FW Package
48-Lead Plastic TSSOP (6.1mm)
(Reference LTC DWG # 05-08-1651)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

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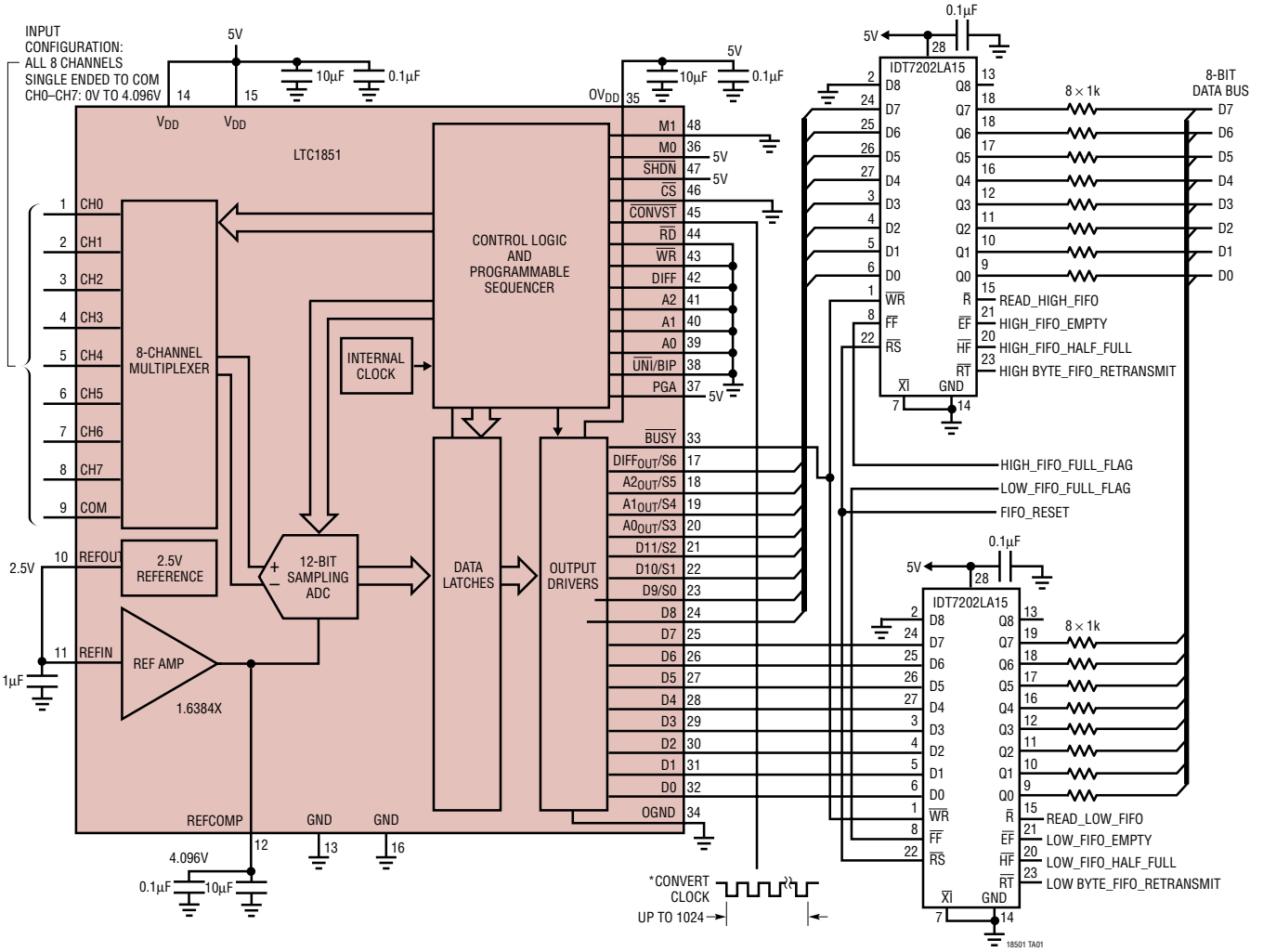
TYPICAL APPLICATION

Data buffering using two IDT7202LA15 1k x 9-bit FIFOs allows rapid collection of 1024 samples and simple interface to low power, low speed, 8-bit microcontrollers. Data and channel information are clocked in simultaneously and read out as two bytes using READ HIGH FIFO and READ LOW FIFO lines. In the event of bus contention, resistors limit peak output current. If both FIFOs are read completely or reset before a burst of conversions, the empty, half full, and full flags from only one FIFO need to be monitored. The retransmit inputs may also be tied together. Retransmit may be used to read data repeatedly, allowing a memory limited processor to perform transform and filtering functions that would otherwise be difficult.



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1410	12-Bit, 1.25Msps, ±5V ADC	71.5dB SINAD at Nyquist, 150mW Dissipation
LTC1415	12-Bit, 1.25Msps, Single 5V ADC	55mW Power Dissipation, 72dB SINAD
LTC1418	14-Bit, 200ksps, Single 5V ADC	15mW, Serial/Parallel ±10V
LTC1419	Low Power 14-Bit, 800ksps ADC	True 14-Bit Linearity, 81.5dB SINAD, 150mW Dissipation
LTC1604	16-Bit, 333ksps, ±5V ADC	90dB SINAD, 220mW Power Dissipation, Pin Compatible with LTC1608
LTC1852/LTC1853	10-Bit/12-Bit, 8-Channel, 400ksps ADCs	Pin-Compatible, Programmable Multiplexer and Sequencer

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- Alternative Solution
- Excess Inventory Management