



**THE DATASHEET OF
LTC1428CS8-50#PBF**



Micropower 8-Bit Current Sink Output D/A Converter

FEATURES

- **Precision Full-Scale DAC Output Current at 25°C: 50µA ±3%**
- Wide Output Voltage DC Compliance: 2V to 10V
- Wide Supply Range: $3V \leq V_{CC} \leq 6.5V$
- Supply Current in Shutdown: 0.2µA
- Low Supply Current: 130µA
- Available in 8-Pin SO
- Triple Mode™ Interface
 1. Standard 3-Wire Mode
 2. 1-Wire Pulse Mode Interface: Increment-Only
 3. 2-Wire Pulse Mode Interface: Increment/Decrement
- DAC Value Read Back Capability in 3-Wire Mode
- DAC Powers Up at Midrange
- **DAC Contents Are Retained in Shutdown**

APPLICATIONS

- LCD Contrast Control
- Backlight Brightness Control
- Power Supply Voltage Adjustment
- Battery Charger Voltage/Current Adjustment
- GaAs FET Bias Adjustment
- Trimmer Pot Elimination

DESCRIPTION

The LTC[®]1428-50 is a micropower 8-bit current sink output D/A converter (DAC) with an output range of 0µA to 50µA. In 3.3V or 5V systems, the DAC I_{OUT} pin can be biased from 2V to 10V. Supply current is only 130µA. Shutdown mode drops the supply current to 0.2µA.

The LTC1428-50 communicates with external circuitry by using one of three interface modes: standard 3-wire serial mode or one of two pulse modes. Upon power-up, the internal counter resets to 10000000B, the DAC output assumes midrange and the chip configures to 3-wire or pulse mode depending on the CS signal level.

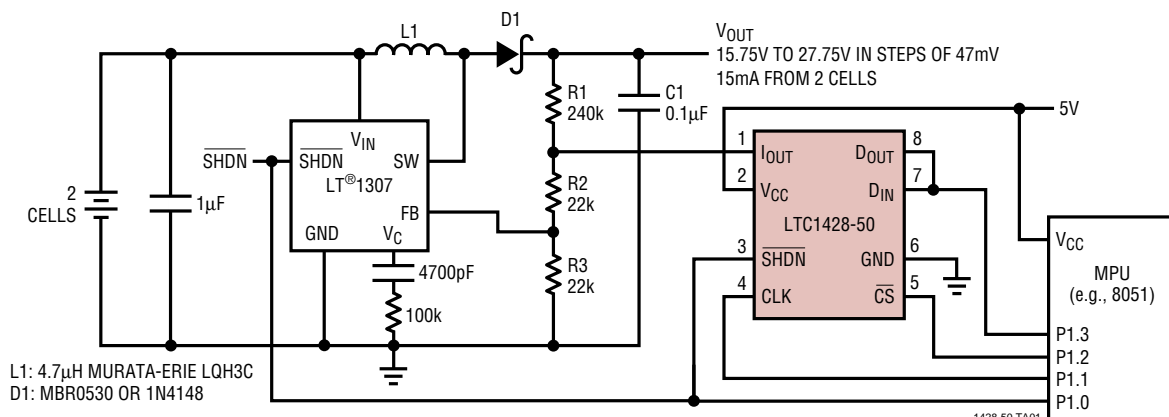
In 3-wire mode, the system MPU can serially transfer 8-bit data to and from the LTC1428-50. In pulse mode, the upper six bits of the DAC output program for increment-only (1-wire interface) or increment/decrement (2-wire interface) operation depending on the D_{IN} signal level. In increment-only mode, the counter rolls over and sets the DAC to zero if the counter increases beyond full scale. In increment/decrement mode, the counter stops incrementing at full scale, stops decrementing at zero scale and does not roll over.

LTC1428-50 is available in an 8-pin SO package.

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TYPICAL APPLICATION

Digitally Controlled LCD Bias Generator (Standard 3-Wire Mode)



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 7V
 Input Voltage (All Inputs) $-0.3V$ to $(V_{CC} + 0.3V)$
 Output Voltage
 I_{OUT} $-0.3V$ to $10V$
 D_{OUT} $-0.3V$ to $(V_{CC} + 0.3V)$
 Short-Circuit Duration (All Outputs) Indefinite
 Operating Temperature Range $0^{\circ}C$ to $70^{\circ}C$
 Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Lead Temperature (Soldering, 10 sec) $300^{\circ}C$

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LTC1428CS8-50
	S8 PART MARKING
	14285

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS $V_{CC} = 3.3V$, $T_A = 25^{\circ}C$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}			3.0		6.5	V
I_{CC}	Supply Current	$V_{SHDN} = V_{DIN} = V_{CS} = V_{CC}$, $V_{CLK} = 0V$, $D_{OUT} = NC$, $I_{OUT} = NC$ Shutdown		130 0.2	225 10	μA μA
	DAC Resolution			8		Bits
	DAC Full-Scale Current	I_{OUT} Bias Voltage = 2.5V	48.5 47.5	50 50	51.5 52.5	μA μA
	DAC Zero-Scale Current	I_{OUT} Bias Voltage = 2.5V			200	nA
	DAC Differential Nonlinearity	Monotonicity Guaranteed, No Missing Codes			± 0.9	LSB
	Supply Voltage Rejection	$V_{CC} = 3V$ to $6.5V$, Full Scale Current, I_{OUT} Bias Voltage = 2.5V		± 1	± 4	LSB
	Output Voltage Rejection	$V_{CC} = 5V$, Full Scale Current, $2V \leq V(I_{OUT}) \leq 3V$			± 1	LSB
		$V_{CC} = 5V$, Full Scale Current, $3V \leq V(I_{OUT}) \leq 10V$		± 1	± 4	LSB
	Logic Input Current	$0V \leq V_{IN} \leq V_{CC}$			± 1	μA
V_{IH}	High Level Input Voltage	$V_{CC} = 5V$	2.0			V
		$V_{CC} = 3.3V$	1.9			V
V_{IL}	Low Level Input Voltage	$V_{CC} = 5V$			0.80	V
		$V_{CC} = 3.3V$			0.45	V
V_{OH}	High Level Output Voltage	$V_{CC} = 5V$, $I_O = 400\mu A$	2.4			V
		$V_{CC} = 3.3V$, $I_O = 400\mu A$	2.1			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 5V$, $I_O = 2mA$			0.4	V
		$V_{CC} = 3.3V$, $I_O = 1mA$			0.4	V
I_{OZ}	Three-State Output Leakage	$V_{CS} = V_{CC}$			± 5	μA

RECOMMENDED OPERATING CONDITIONS $V_{CC} = 5V$, unless otherwise specified. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Interface						
f_{CLK}	Clock Frequency		●		2	MHz
t_{CKS}	Setup Time, CLK↓ Before \overline{CS} ↓		●	150		ns
t_{CSS}	Setup Time, \overline{CS} ↓ Before CLK↑		●	400		ns
t_{DV}	\overline{CS} ↓ to D_{OUT} Valid	See Test Circuits	●	150		ns
t_{DS}	D_{IN} Setup Time Before CLK↑		●	150		ns
t_{DH}	D_{IN} Hold Time After CLK↑		●	150		ns
t_{DO}	CLK↓ to D_{OUT} Valid	See Test Circuits	●	150		ns
t_{CKHI}	CLK High Time		●	200		ns
t_{CKLO}	CLK Low Time		●	250		ns
t_{CSH}	CLK↓ Before \overline{CS} ↑		●	150		ns
t_{DZ}	\overline{CS} ↑ to D_{OUT} in Hi-Z	See Test Circuits	●		400	ns
t_{CKH}	\overline{CS} ↑ Before CLK↑		●		400	ns
t_{CSLO}	\overline{CS} Low Time	$f_{CLK} = 2MHz$ (Note 4) $V_{CLK} = 0V$	●	4550 400		ns ns
t_{CSHI}	\overline{CS} High Time		●	400		ns

The ● denotes specifications which apply over the full operating temperature range.

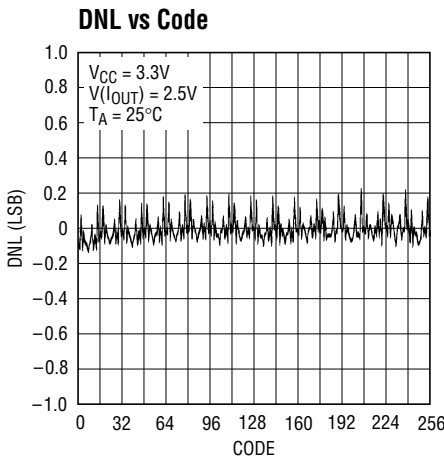
Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Timing for all input signals is measured at 0.8V for a High-to-Low transition and at 2V for a Low-to-High transition.

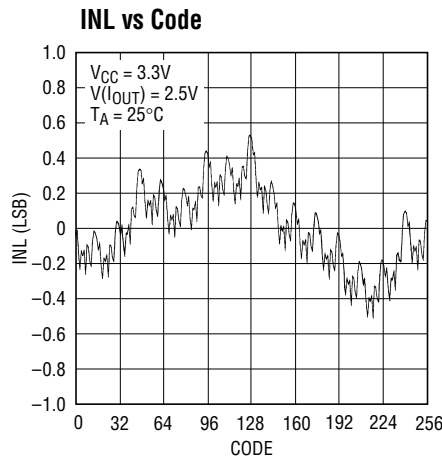
Note 3: Timing specifications are guaranteed by design but not tested.

Note 4: This is the minimum time required for valid data transfer.

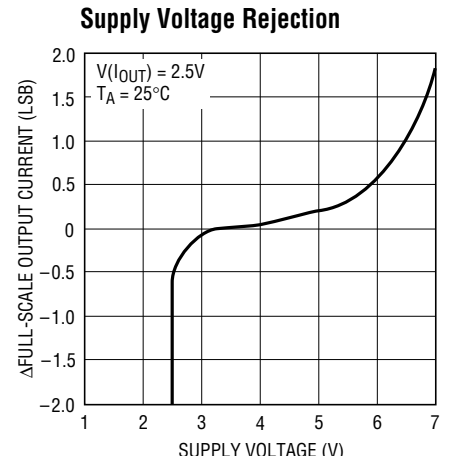
TYPICAL PERFORMANCE CHARACTERISTICS



1428-50 G01



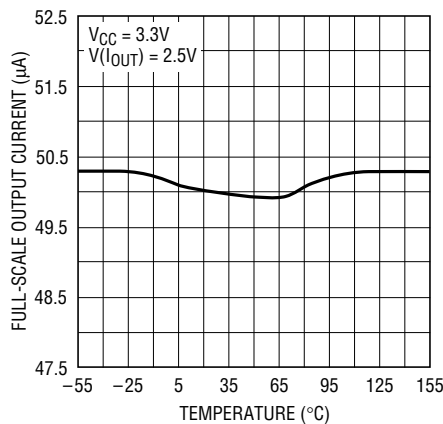
1428-50 G02



1428-50 G03

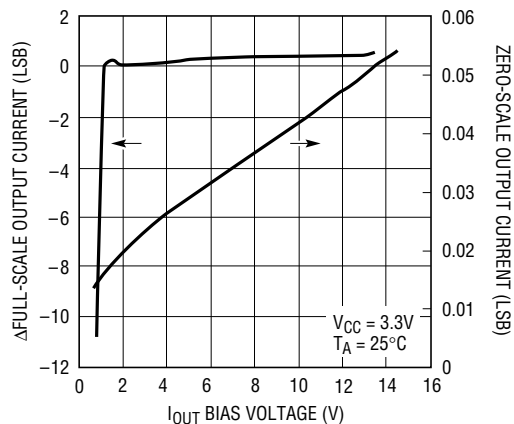
TYPICAL PERFORMANCE CHARACTERISTICS

Temperature Variation



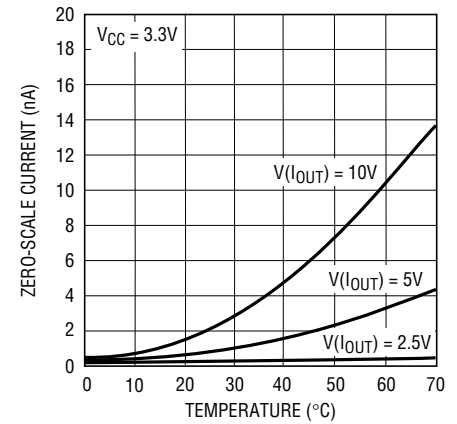
1428-50 G04

Bias Voltage Rejection



1428-50 G05

Zero-Scale I_{OUT} vs Temperature



1428-50 G06

PIN FUNCTIONS

I_{OUT} (Pin 1): DAC Current Sink Output. In 3.3V or 5V systems, the DAC I_{OUT} pin can be biased from 2V to 10V.

V_{CC} (Pin 2): Voltage Supply ($3V \leq V_{CC} \leq 6.5V$). This supply must be kept free from noise and ripple by bypassing directly to a ground plane.

\overline{SHDN} (Pin 3): Shutdown. A logic low puts the chip into shutdown mode. The digital setting for the DAC is retained.

CLK (Pin 4): Shift Clock. This clock synchronizes the serial data and has a Schmitt trigger input.

\overline{CS} (Pin 5): Chip Select Input. In 3-wire mode, a logic low enables the LTC1428-50. Upon power-up, a logic high

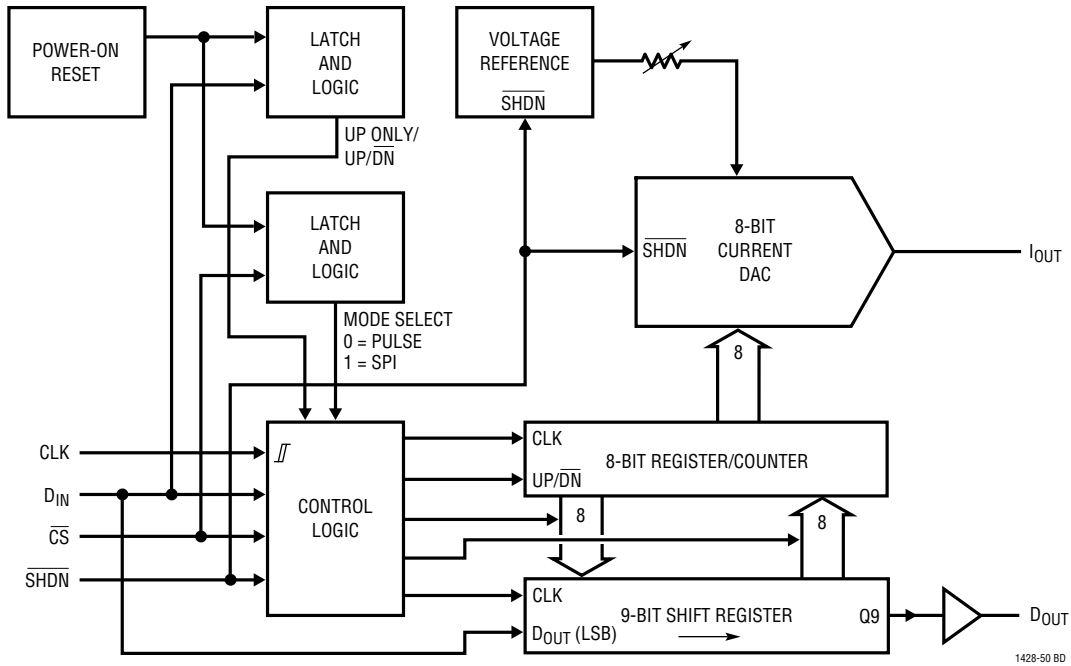
puts the chip into pulse mode. If \overline{CS} ever goes low, the chip is configured into 3-wire mode until V_{CC} is reset.

GND (Pin 6): Ground. Ground should be tied directly to a ground plane.

D_{IN} (UP/DN) (Pin 7): Data Input. In 3-wire mode, the DAC data is shifted into D_{IN} . In pulse mode, upon power-up a logic high puts the counter into increment-only mode. If D_{IN} ever goes low, the counter is configured in increment/decrement mode until V_{CC} is reset.

D_{OUT} (Pin 8): Data Output. In 3-wire mode, on every conversion D_{OUT} serially outputs the previous 8-bit DAC data. In pulse mode, D_{OUT} is three-stated.

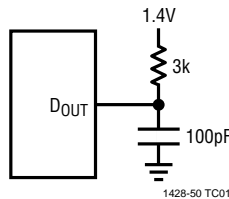
BLOCK DIAGRAM



1428-50 BD

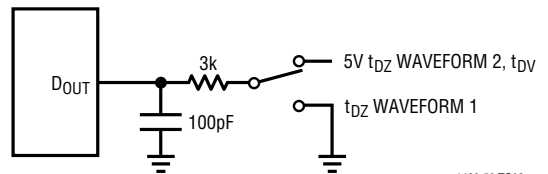
TEST CIRCUITS

Load Circuit for t_{D0}



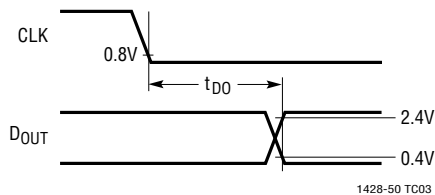
1428-50 TC01

Load Circuit for t_{DZ} , t_{DV}



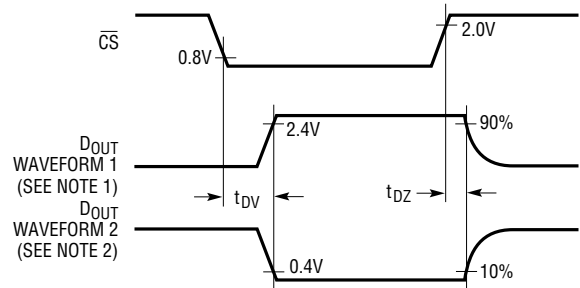
1428-50 TC02

Voltage Waveforms for t_{D0}



1428-50 TC03

Voltage Waveforms for t_{DZ} , t_{DV}



1428-50 TC04

NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY CS

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY CS

SERIAL I/O OPERATING SEQUENCE

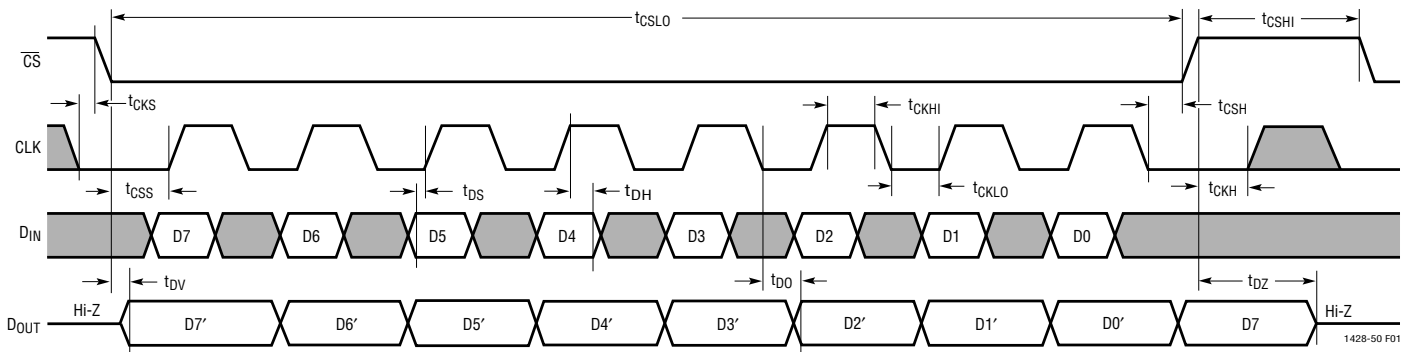


Figure 1. 3-Wire Interface Timing Specification

APPLICATIONS INFORMATION

8-BIT CURRENT OUTPUT DAC

The LTC1428-50 is an 8-bit, current sink output digital-to-analog (DAC) converter. The LTC1428-50 is guaranteed monotonic and is digitally adjustable in 256 equal steps. Upon power up, the counter resets to 1000000B and the DAC output assumes midrange. The I_{OUT} pin can be biased from 2V to 10V. The LTC1428-50 features a full-scale output current of 50µA ±3% at room temperature (±5% over temperature). This device also includes a flexible serial digital interface that allows easy interconnection to a variety of digital systems.

DIGITAL INTERFACE

Automatic Mode Selection

The LTC1428-50 includes a serial interface capable of communicating with the host system using one of three protocols; standard 3-wire mode, a 2-wire up/down pulse mode and a 1-wire increment-only pulse mode. The LTC1428-50 is designed to autoconfigure itself depending on the method

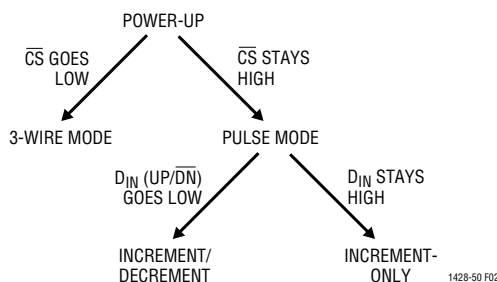


Figure 2. LTC1428-50 Operating Modes

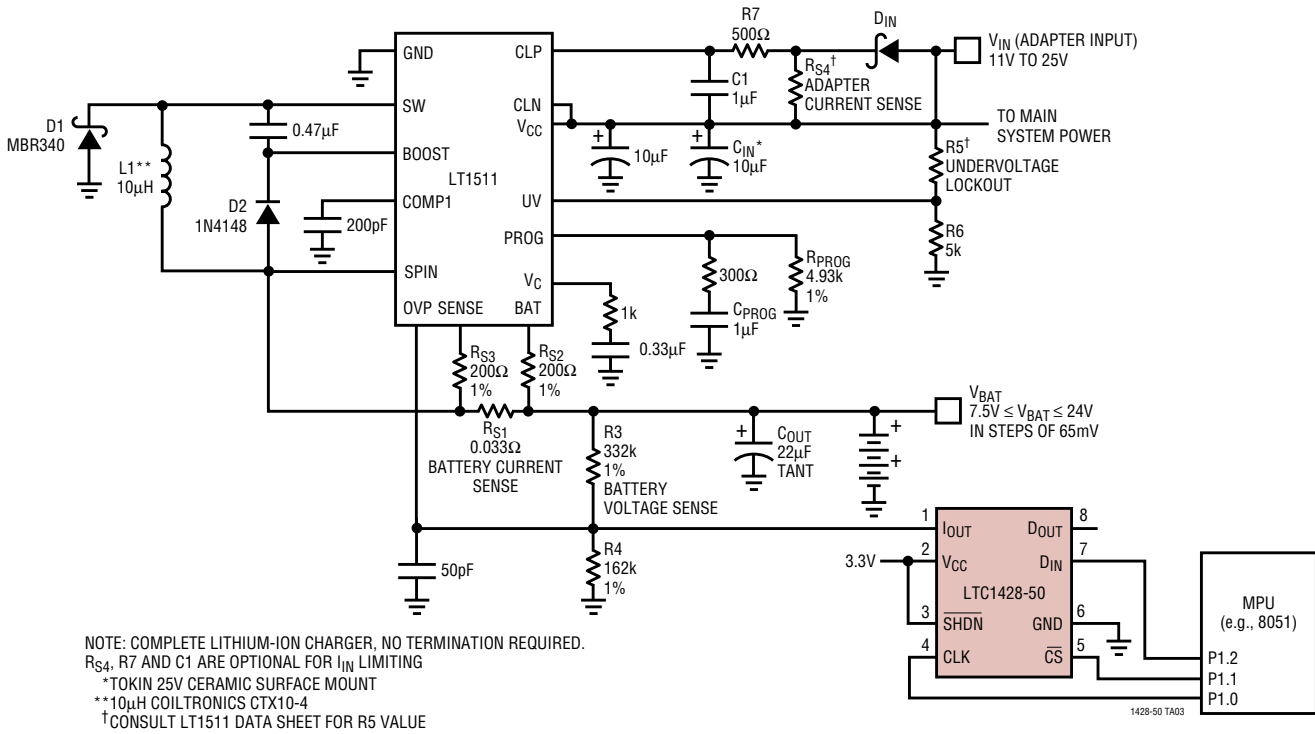
of data presentation. A diagram illustrating this autodetection behavior is shown in Figure 2. At power-up, the interface is set to 1-wire pulse mode. If the \overline{CS} line ever goes low (as it will at the beginning of a valid 3-wire serial transfer) the chip immediately reconfigures itself into 3-wire mode and remains in this mode until power is cycled. If \overline{CS} stays high, the device stays in pulse mode and monitors the UP/DN pin to determine whether to switch to 2-wire mode. If UP/DN ever goes low (as it will the first time a “down” command is given) the chip switches into 2-wire pulse mode and remains in this mode until power is cycled. In a properly configured 1-wire system, \overline{CS} and UP/DN will always remain high. 2-wire pulse mode systems must provide a single logic low pulse before the first data pulses are sent to prevent the LTC1428-50 from remaining in 1-wire mode if the first several pulses are logic high.

Standard 3-Wire Mode (Figure 3)

Refer to the Serial Interface Operating Sequence in Figure 1. When operating in 3-wire mode, the LTC1428-50 will interface directly with most standard 3- or 4-wire serial interface systems. The clock (CLK) input synchronizes the data transfer with each input bit captured at the rising edge of CLK and each output data bit shifted through D_{OUT} at the falling edge. Data is shifted into and out of the LTC1428-50 starting with the MSB bit. A falling edge at \overline{CS} initiates the data transfer and brings the D_{OUT} pin out of three-state. The serial 8-bit data representing the new DAC setting is shifted into the D_{IN} pin. Simultaneously, the previous DAC setting is shifted out of the D_{OUT} pin. After the new data is

TYPICAL APPLICATION

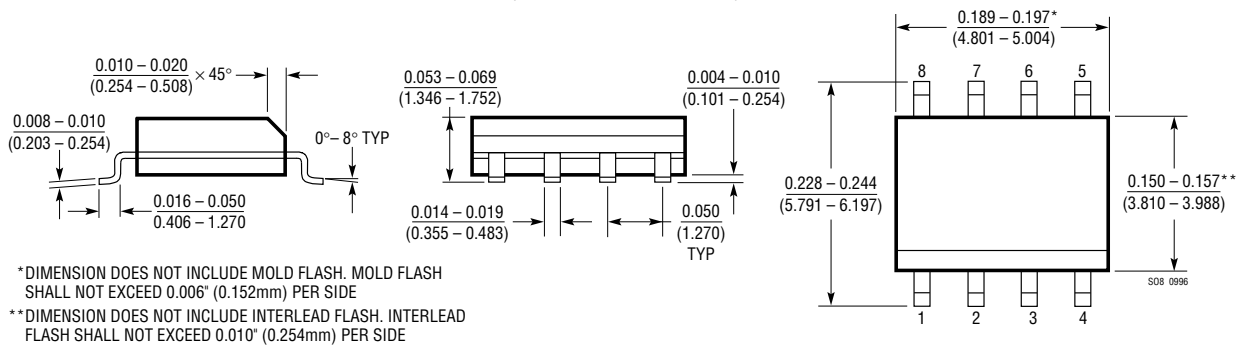
Digitally Adjustable 3A Lithium-Ion Battery Charger



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
 (LTC DWG # 05-08-1610)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1329	8-Bit Current Output D/A Converter	Current Source Output, Full-Scale Current 10µA or 50µA
LTC1451	12-Bit Micropower Serial Input V _{OUT} DAC	Higher Resolution, 8-Pin SO
LTC1452	12-Bit Multiplying Serial Input V _{OUT} DAC	Higher Resolution, 8-Pin SO
LTC8043	12-Bit Multiplying Serial Input I _{OUT} DAC	Higher Resolution, 8-Pin SO

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