THE DATASHEET OF

LTC1093CN

1-, 2-, 6- and 8-Channel, 10-Bit Serial I/O Data Acquisition Systems

FEATURES

- **Programmable Features**
  - **– Unipolar/Bipolar Conversions**
  - **– Differential/Single-Ended Multiplexer Configurations**
- Sample-and-Holds
- Single Supply 5V, 10V or ±5V Operation
- Direct 3- or 4-Wire Interface to Most MPU Serial Ports and All MPU Parallel I/O Ports
- Analog Inputs Common Mode to Supply Rails
- Resolution: 10 Bits
- Total Unadjusted Error (A Grade): ±1LSB Over Temp
- Fast Conversion Time: 20µs
- Low Supply Current
  LTC1091: 3.5mA Max, 1.5mA Typ
  LTC1092/LTC1093/LTC1094: 2.5mA Max, 1mA Typ

DESCRIPTION

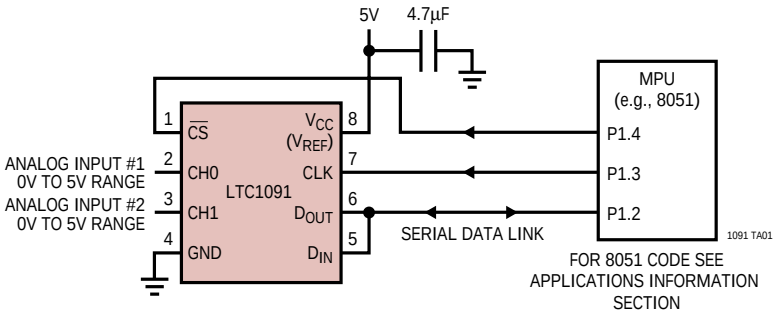
The LTC®1091/LTC1092/LTC1093/LTC1094 10-bit data acquisition systems are designed to provide complete function, excellent accuracy and ease of use when digitizing analog data from a wide variety of signal sources and transducers. Built around a 10-bit, switched capacitor, successive approximation A/D core, these devices include software configurable analog multiplexers and bipolar and unipolar conversion modes as well as on-chip sample-and-holds. On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers. These circuits can provide a complete data acquisition system in ratiometric applications or can be used with an external reference in others.

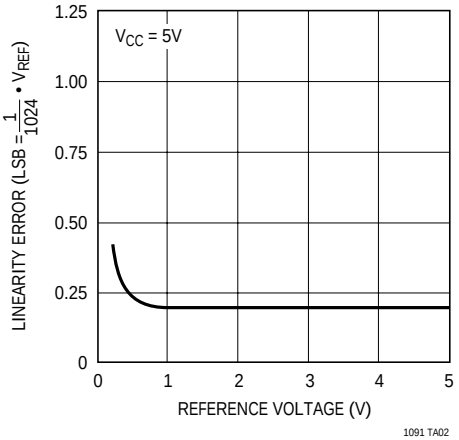
The high impedance analog inputs and the ability to operate with reduced spans (below 1V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

An efficient serial port communicates without external hardware to most MPU serial ports and all MPU parallel I/O ports allowing eight channels of data to be transmitted over as few as three wires. This, coupled with low power consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

Temperature drift of offset, linearity and full-scale error are all extremely low (1ppm/°C typically) allowing all grades to be specified with offset and linearity errors of ±0.5LSB maximum over temperature. In addition, the A grade devices are specified with full-scale error and total unadjusted error (including the effects of offset, linearity and full-scale errors) of ±1LSB maximum over temperature. The lower grade has a full-scale specification of ±2LSB for applications where full scale is adjustable or less critical.

TYPICAL APPLICATION





ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{CC}) to GND or V^- 12V
Negative Supply Voltage (V^-) ..... –6V to GND
Voltage
  Analog Reference and LTC1091/2 $\overline{CS}$
  Inputs ..... (V^-) –0.3V to (V_{CC} + 0.3V)
  Digital Inputs (except LTC1091/2 $\overline{CS}$) .. –0.3V to 12V
  Digital Outputs ..... –0.3V to (V_{CC} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
  LTC1091/2/3/4AC, LTC1091/2/3/4C ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION

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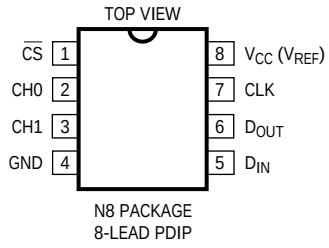
<td> 

N8 PACKAGE
8-LEAD PDIP
T_{JMAX} = 110°C, θ_{JA} = 150°C/W (N)</td>
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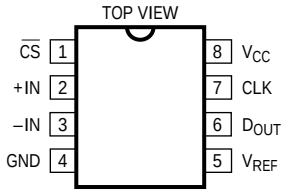
LTC1091ACN8
LTC1091CN8</td>
<td> 

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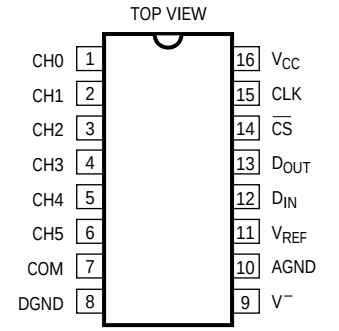
<td> 

N PACKAGE
16-LEAD PDIP
SW PACKAGE
16-LEAD PLASTIC SO WIDE
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T_{JMAX} = 110°C, θ_{JA} = 130°C/W (SW)</td>
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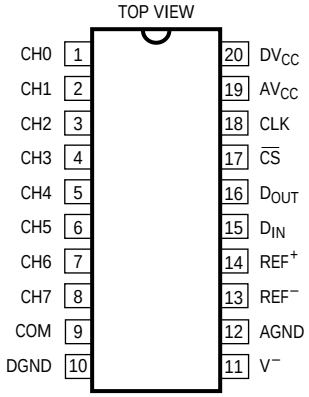
LTC1093CSW</td>
<td> 

N PACKAGE
20-LEAD PDIP
T_{JMAX} = 110°C, θ_{JA} = 150°C/W (N)</td>
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Consult factory for Industrial and Military grade parts.

PRODUCT GUIDE

PART NUMBER	#CHANNELS	CONVERSION MODES		REDUCED SPAN CAPABILITY (SEPARATE V_{REF})	±5V CAPABILITY	
		UNIPOLAR	BIPOLAR			
LTC1091	2	●				Pin-for-Pin 10-Bit Upgrade of ADC0832
LTC1092	1	●		●		Pin-for-Pin 10-Bit Upgrade of ADC0831
LTC1093	6	●	●	●	●	
LTC1094	8	●	●	●	●	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LTC1091A/LTC1092A/LTC1093A/LTC1094A LTC1091/LTC1092/LTC1093/LTC1094 MIN	MAX	UNITS
V_{CC}	Supply Voltage		4.5	10	V
V^-	Negative Supply Voltage	LTC1093/LTC1094, V_{CC} = 5V	–5.5	0	V
f_{CLK}	Clock Frequency	V_{CC} = 5V	0.01	0.5	MHz
t_{CYC}	Total Cycle Time	LTC1091	15 CLK Cycles + 2µs		
		LTC1092	12 CLK Cycles + 2µs		
		LTC1093/LTC1094	18 CLK Cycles + 2µs		
t_{hDI}	Hold Time, D_{IN} Alter SCLK↑	V_{CC} = 5V	150		ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before CLK↑	V_{CC} = 5V	1		µs
t_{suDI}	Setup Time D_{IN} Stable Before CLK↑	V_{CC} = 5V	400		ns
t_{WHCLK}	CLK High Time	V_{CC} = 5V	0.8		µs
t_{WLCLK}	CLK Low Time	V_{CC} = 5V	1		µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 5V	2		µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1091 LTC1092 LTC1093/LTC1094	15 12 18		CLK Cycles CLK Cycles CLK Cycles

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. (Note 3)

PARAMETER	CONDITIONS		LTC1091A/LTC1092A LTC1093A/LTC1094A MIN	TYP	MAX	LTC1091/LTC1092 LTC1093/LTC1094 MIN	TYP	MAX	UNITS
Offset Error	(Note 4)	●			±0.5			±0.5	LSB
Linearity Error	(Notes 4, 5)	●			±0.5			±0.5	LSB
Full-Scale Error	(Note 4)	●			±1.0			±2.0	LSB
Total Unadjusted Error	V_{REF} = 5.000V (Notes 4, 6)	●			±1.0				LSB
Reference Input Resistance	LTC1092/LTC1093/LTC1094 V_{REF} = 5V	●	5	10		5	10		kΩ
Analog and REF Input Range	(Note 7)		(V^-) –0.05V to V_{CC} + 0.05V						V
On-Channel Leakage Current (Note 8)	On-Channel = 5V Off-Channel = 0V	●			1			1	µA
	On-Channel = 0V Off-Channel = 5V	●			–1			–1	µA
Off-Channel Leakage Current (Note 8)	On-Channel = 5V Off-Channel = 0V	●			–1			–1	µA
	On-Channel = 0V Off-Channel = 5V	●			1			1	µA

AC CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1091A/LTC1092A/LTC1093A/LTC1094A LTC1091/LTC1092/LTC1093/LTC1094 MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			10		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		400	850	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		180	450	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●		160	450	ns
t_{hDO}	Time Output Data Remains Valid After SCLK↓				150		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		90	300	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		60	300	ns
C_{IN}	Input Capacitance	Analog Inputs On-Channel Analog Inputs Off-Channel Digital Inputs			65 5 5		pF pF pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1091A/LTC1092A/LTC1093A/LTC1094A LTC1091/LTC1092/LTC1093/LTC1094 MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_{OUT} = 10µA V_{CC} = 4.75V, I_{OUT} = 360µA	 ●	 2.4	4.7 4.0		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_{OUT} = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$V_{OUT} = V_{CC}$, $\overline{CS}$ High V_{OUT} = 0V, $\overline{CS}$ High	● ●			3 –3	µA µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			10		mA
I_{CC}	Positive Supply Current	LTC1091, $\overline{CS}$ High LTC1092/LTC1093/LTC1094, $\overline{CS}$ High, REF^+ Open	● ●		1.5 1.0	3.5 2.5	mA mA
I_{REF}	Reference Current	LTC1092/LTC1093/LTC1094, V_{REF} = 5V	●		0.5	1.0	mA
I^-	Negative Supply Current	LTC1093/LTC1094, $\overline{CS}$ High, V^- = –5V	●		1	50	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, AGND, GND and REF^- wired together (unless otherwise noted). REF^- is internally connected to the AGND pin on the LTC1093. DGND, AGND, REF^- and V^- are internally connected to the GND pin on the LTC1091/LTC1092.

Note 3: V_{CC} = 5V, $V_{REF}{}^+$ = 5V, $V_{REF}{}^-$ = 0V, V^- = 0V for unipolar mode and –5V for bipolar mode, CLK = 0.5MHz unless otherwise specified.

Note 4: These specs apply for both unipolar (LTC1091/LTC1092/LTC1093/LTC1094) and bipolar (LTC1093/LTC1094 only) modes. In bipolar mode, one LSB is equal to the bipolar input span ($2V_{REF}$) divided by 1024. For example, when V_{REF} = 5V, 1LSB (bipolar) = 2(5V)/1024 = 9.77mV.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve.

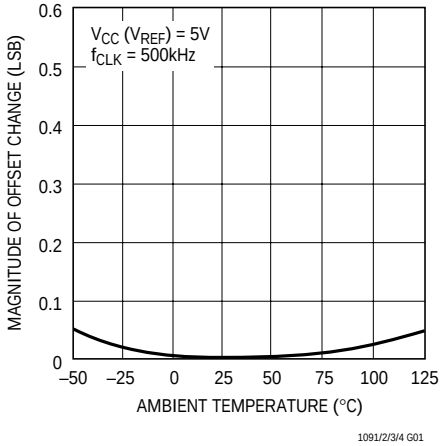
Note 6: Total unadjusted error includes offset, full scale, linearity, multiplexer and hold step errors.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below V^- or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

Note 8: Channel leakage current is measured after the channel selection.

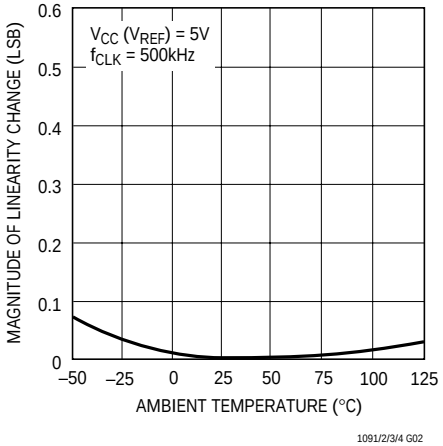
TYPICAL PERFORMANCE CHARACTERISTICS

Change in Offset Error vs Temperature



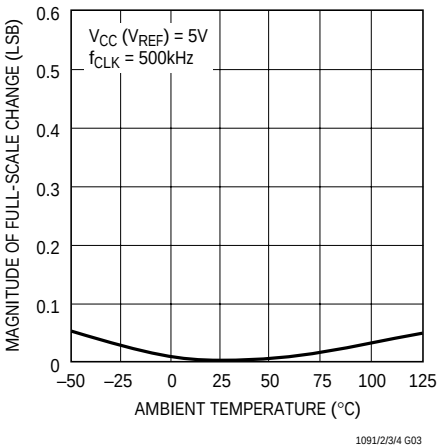
1091/2/3/4 G01

Change in Linearity Error vs Temperature



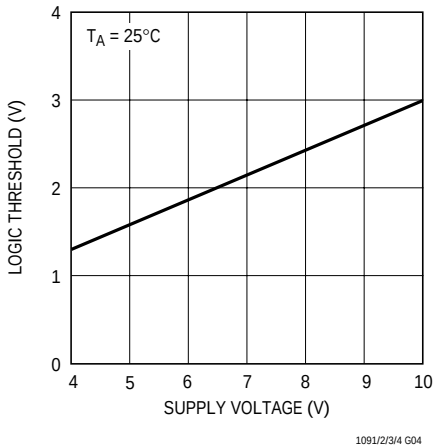
1091/2/3/4 G02

Change in Full-Scale Error vs Temperature



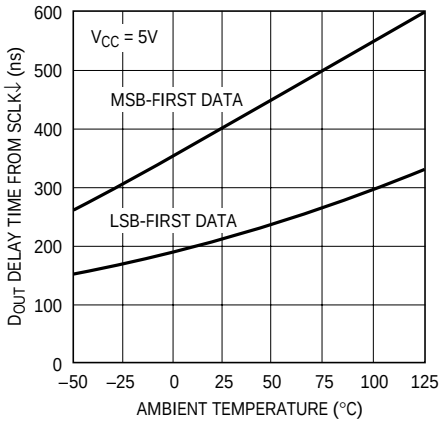
1091/2/3/4 G03

Digital Input Logic Threshold vs Supply Voltage



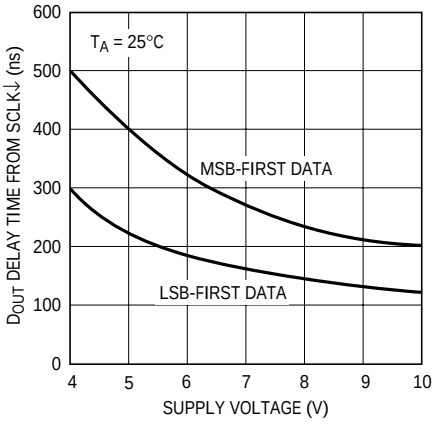
1091/2/3/4 G04

D_{OUT} Delay Time vs Temperature



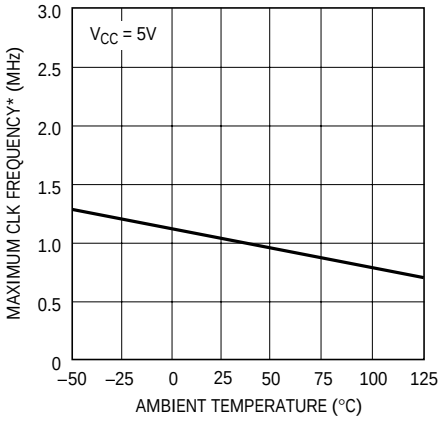
1091/2/3/4 G05

D_{OUT} Delay Time vs Supply Voltage



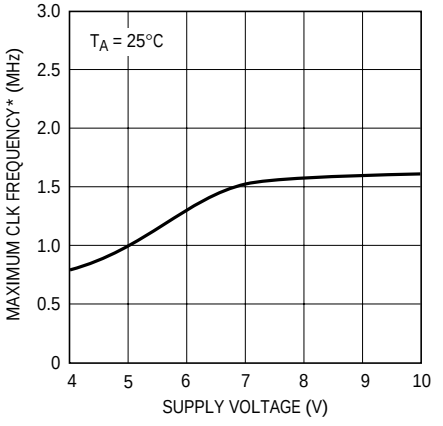
1091/2/3/4 G06

Maximum Clock Rate vs Temperature



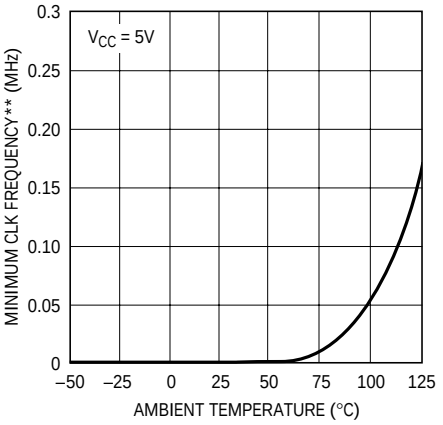
1091/2/3/4 G07

Maximum Clock Rate vs Supply Voltage



1091/2/3/4 G08

Minimum Clock Rate vs Temperature



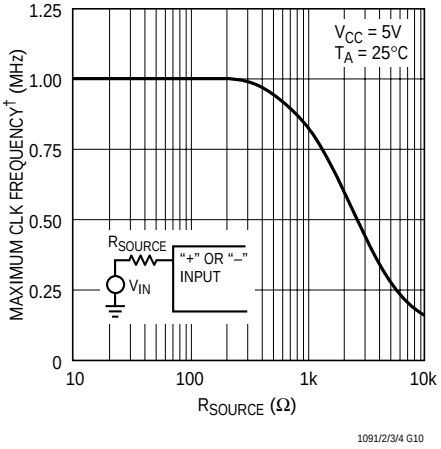
1091/2/3/4 G09

*MAXIMUM CLK FREQUENCY REPRESENTS THE HIGHEST FREQUENCY AT WHICH CLK CAN BE OPERATED (WITH 50% DUTY CYCLE) WHILE STILL PROVIDING 100ns SETUP TIME FOR THE DEVICE RECEIVING THE D_{OUT} DATA.

**AS THE CLK FREQUENCY IS DECREASED FROM 500kHz, MINIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 500kHz VALUE IS FIRST DETECTED.

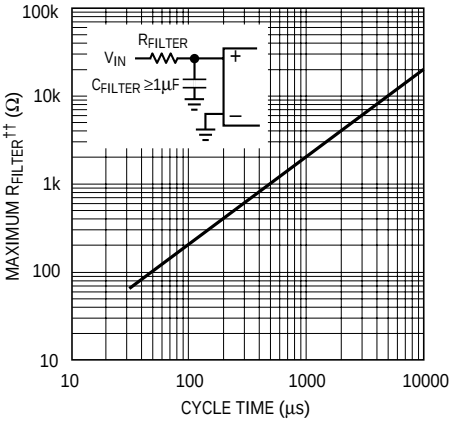
TYPICAL PERFORMANCE CHARACTERISTICS

LTC1091/LTC1092/LTC1093/LTC1094 Maximum Clock Rate vs Source Resistance



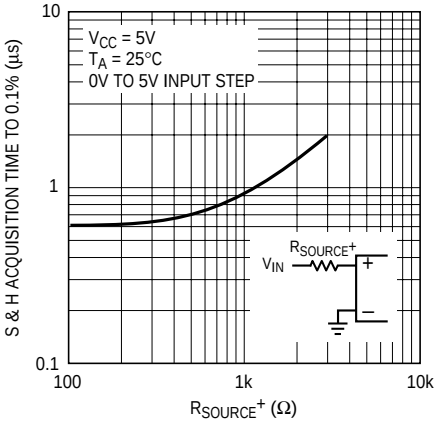
1091/2/3/4 G10

LTC1091/LTC1092/LTC1093/LTC1094 Maximum Filter Resistor vs Cycle Time



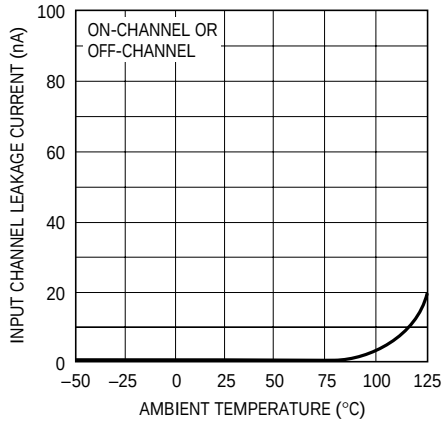
1091/2/3/4 G11

LTC1091/LTC1092/LTC1093/LTC1094 Sample-and-Hold Acquisition Time vs Source Resistance



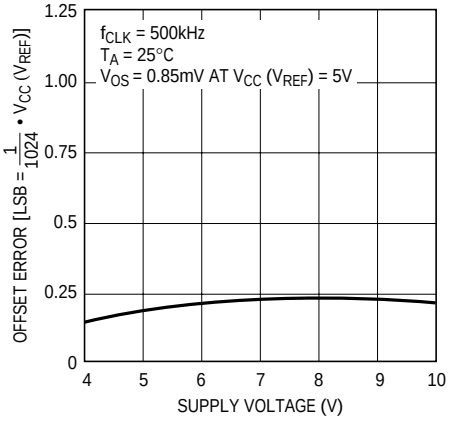
1091/2/3/4 G12

LTC1091/LTC1092 Input Channel Leakage Current vs Temperature



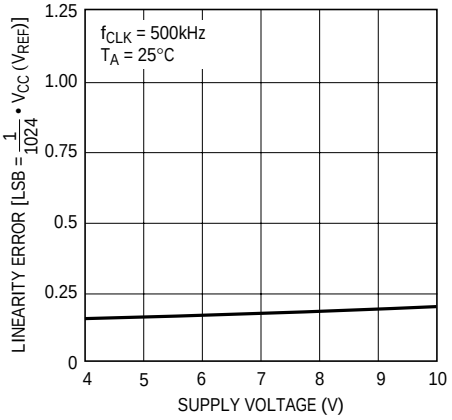
1091/2/3/4 G13

LTC1091 Offset Error vs Supply Voltage



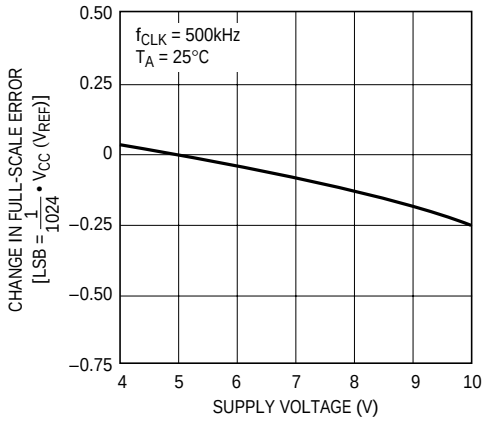
1091/2/3/4 G14

LTC1091 Linearity Error vs Supply Voltage



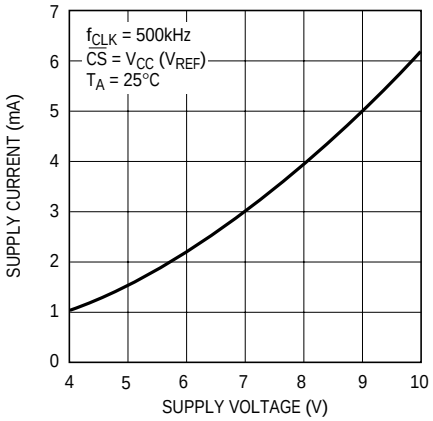
1091/2/3/4 G15

LTC1091 Change in Full-Scale Error vs Supply Voltage



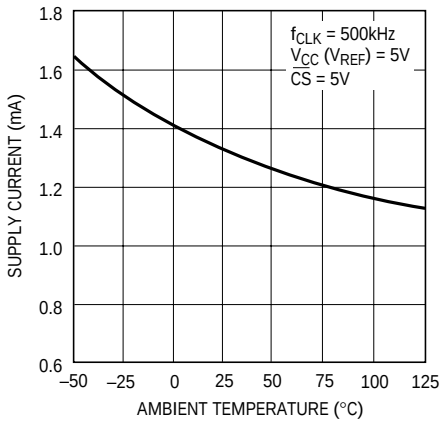
1091/2/3/4 G16

LTC1091 Supply Current vs Supply Voltage



1092/2/3/4 G17

LTC1091 Supply Current vs Temperature



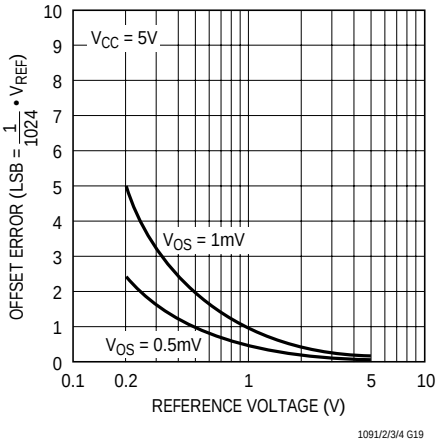
1091/2/3/4 G18

† AS THE CLK FREQUENCY AND SOURCE RESISTANCE ARE INCREASED, MAXIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 500kHz, 0Ω VALUE IS FIRST DETECTED.

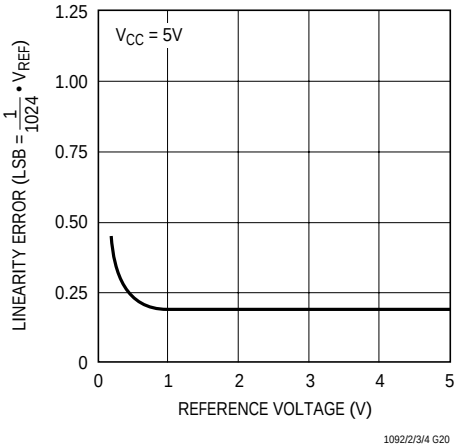
†† MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL-SCALE ERROR FROM ITS VALUE AT R_{FILTER} = 0 IS FIRST DETECTED.

TYPICAL PERFORMANCE CHARACTERISTICS

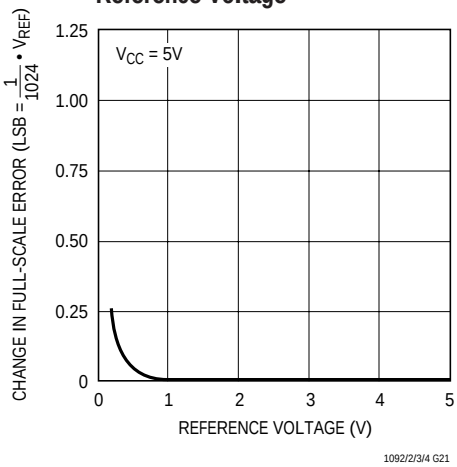
LTC1092/LTC1093/LTC1094
Unadjusted Offset Error vs Reference Voltage



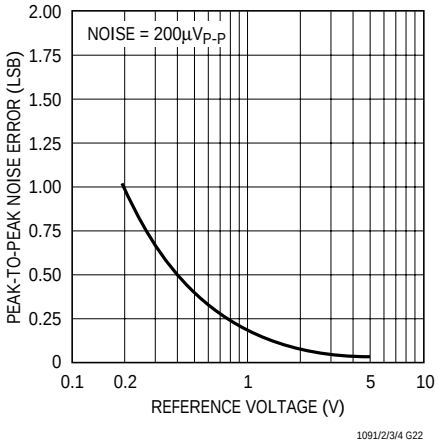
LTC1092/LTC1093/LTC1094
Linearity Error vs Reference Voltage



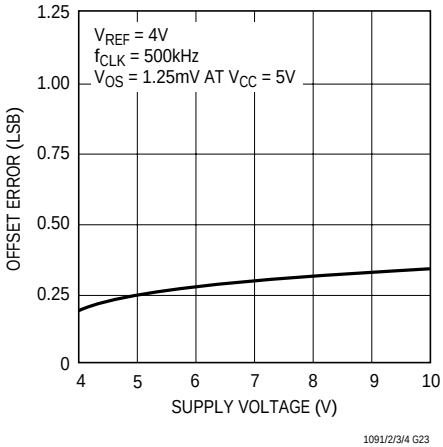
LTC1092/LTC1093/LTC1094
Change in Full-Scale Error vs Reference Voltage



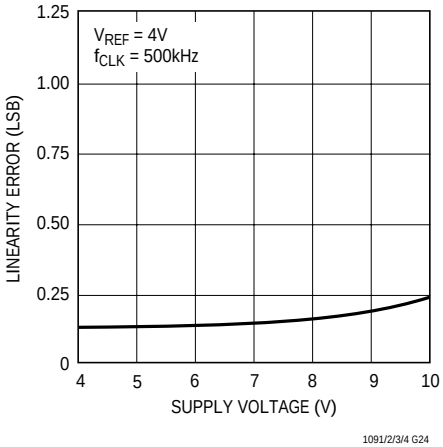
LTC1092/LTC1093/LTC1094
Noise Error vs Reference Voltage



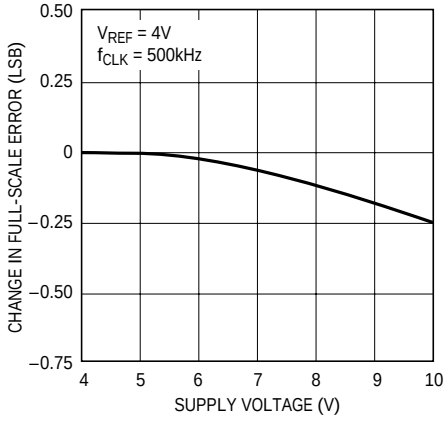
LTC1092/LTC1093/LTC1094
Offset Error vs Supply Voltage



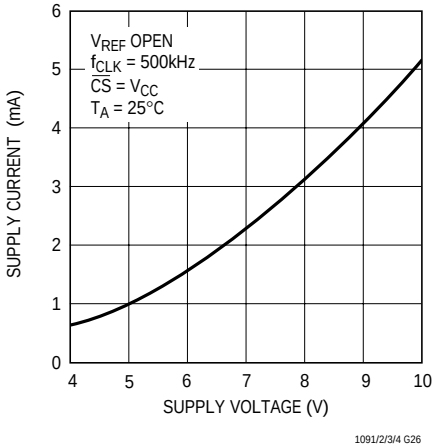
LTC1092/LTC1093/LTC1094
Linearity Error vs Supply Voltage



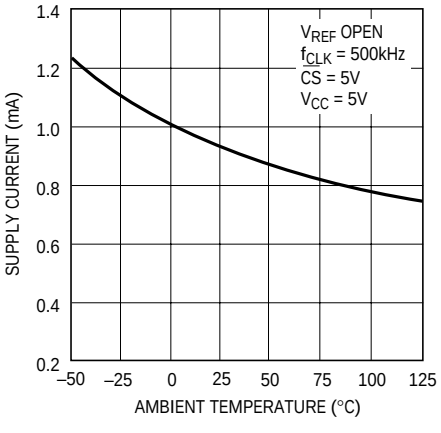
LTC1092/LTC1093/LTC1094
Change in Full-Scale Error vs Supply Voltage



LTC1092/LTC1093/LTC1094
Supply Current vs Supply Voltage

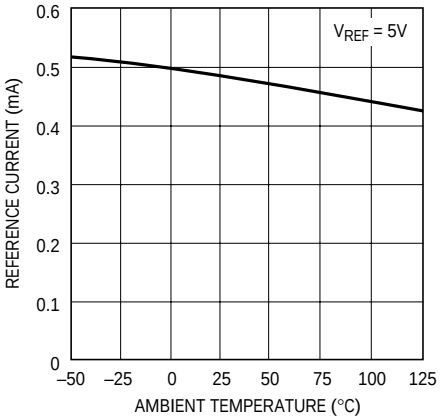


LTC1092/LTC1093/LTC1094
Supply Current vs Temperature

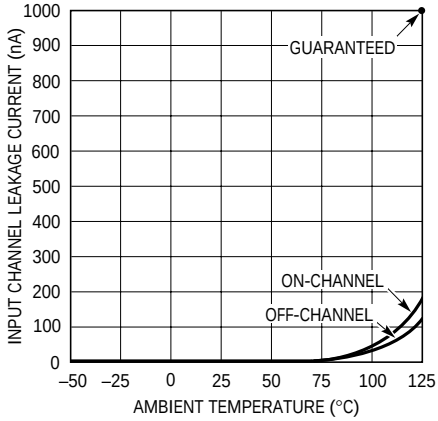


TYPICAL PERFORMANCE CHARACTERISTICS

LTC1092/LTC1093/LTC1094
Reference Current vs Temperature



LTC1093/LTC1094 Input Channel
Leakage Current vs Temperature



PIN FUNCTIONS

LTC1091/LTC1092

$\overline{CS}$ (Pin 1): Chip Select Input. A logic low on this input enables the LTC1091/LTC1092.

CH0, CH1/+IN, –IN (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

D_{IN} (Pin 5)(LTC1091): Digital Data Input. The multiplexer address is shifted into this input.

V_{REF} (Pin 5)(LTC1092): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to AGND.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

V_{CC}(V_{REF})(Pin 8)(LTC1091): Positive Supply and Reference Voltage. This pin provides power and defines the span of the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

V_{CC} (Pin 8)(LTC1092): Positive Supply Voltage. This pin provides power to the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

LTC1093/LTC1094

CH0 to CH5/CH0 to CH7 (Pins 1 to 6/Pins 1 to 8): Analog Inputs. The analog inputs must be free of noise with respect to AGND.

COM (Pin 7/Pin 9): Common. The common pin defines the zero reference point for all single-ended inputs. It must be free of noise and is usually tied to the analog ground plane.

DGND (Pin 8/Pin 10): Digital Ground. This is the ground for the internal logic. Tie to the ground plane.

V^- (Pin 9/Pin 11): Negative Supply. Tie V^- to most negative potential in the circuit. (Ground in single supply applications.)

AGND (Pin 10/Pin 12): Analog Ground. AGND should be tied directly to the analog ground plane.

PIN FUNCTIONS

V_{REF} (Pin 11)(LTC1093): Reference Input. The reference input must be kept free of noise with respect to AGND.

REF^+, REF^- (Pins 13, 14)(LTC1094): Reference Input. The reference input must be kept free of noise with respect to AGND.

D_{IN} (Pin 12/Pin 15): Data Input. The A/D configuration word is shifted into this input.

D_{OUT} (Pin 13/Pin 16): Digital Data Output. The A/D conversion result is shifted out of this output.

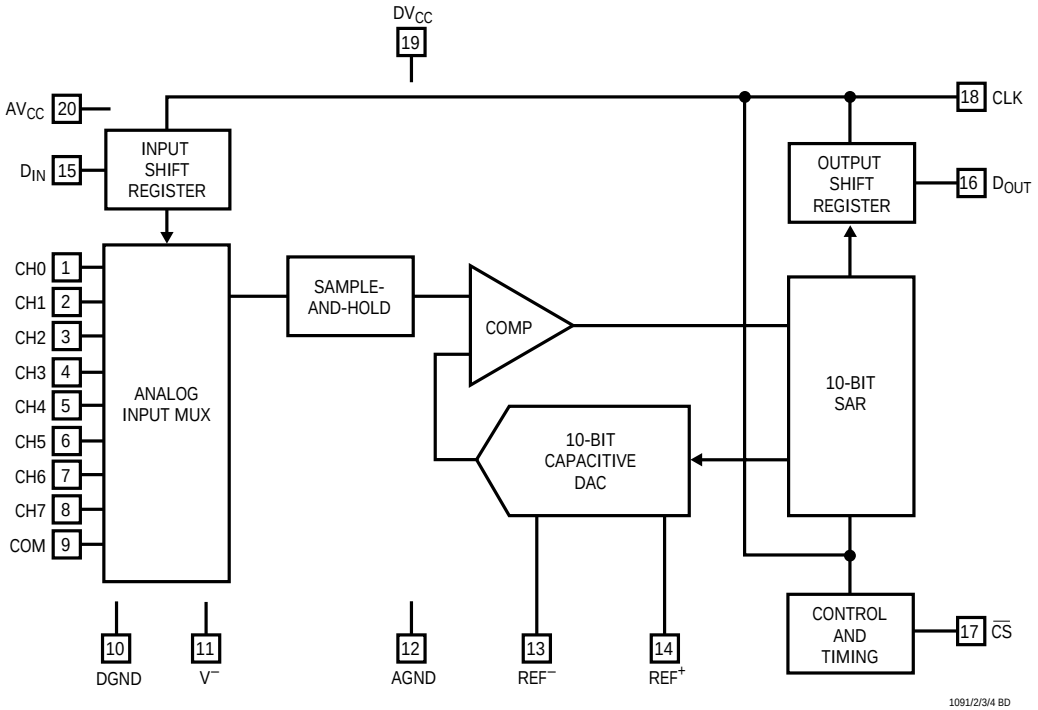
$\overline{CS}$ (Pin 14/Pin 17): Chip Select Input. A logic low on this input enables the LTC1093/LTC1094.

CLK (Pin 15/Pin 18): Shift Clock. This clock synchronizes the serial data transfer.

V_{CC} (Pin 16)(LTC1093): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

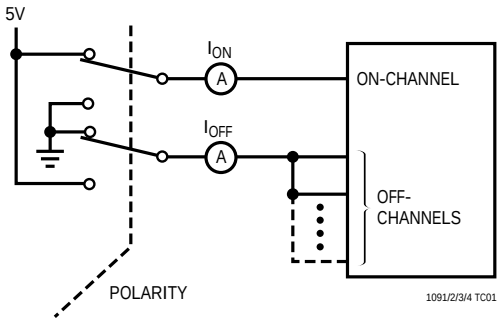
AV_{CC}, DV_{CC} (Pins 19, 20)(LTC1094): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane. AV_{CC} and DV_{CC} should be tied together on the LTC1094.

BLOCK DIAGRAM (Pin numbers refer to LTC1094)

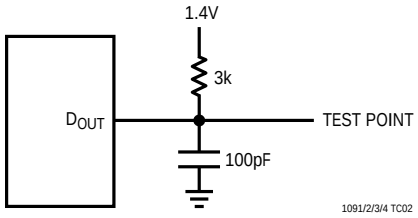


TEST CIRCUITS

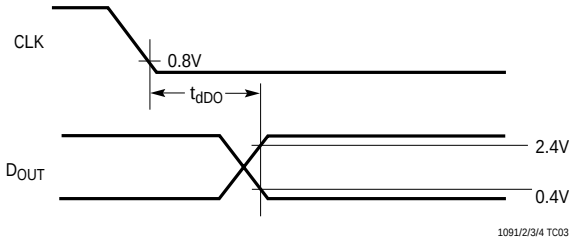
On- and Off-Channel Leakage Current



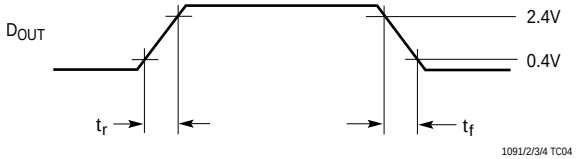
Load Circuit for t_{dDO}, t_r, t_f



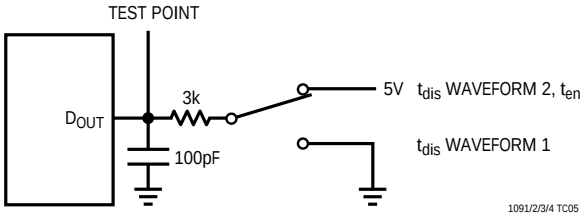
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



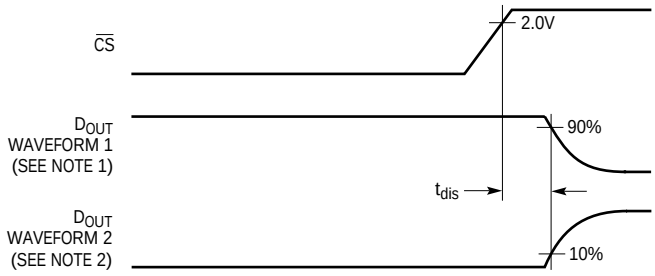
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



Load Circuit for t_{dis}, t_{en}



Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL

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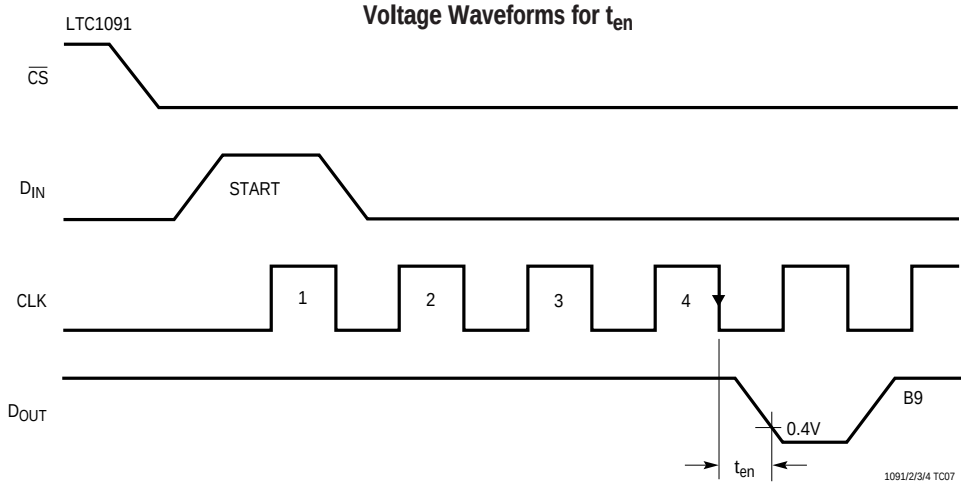
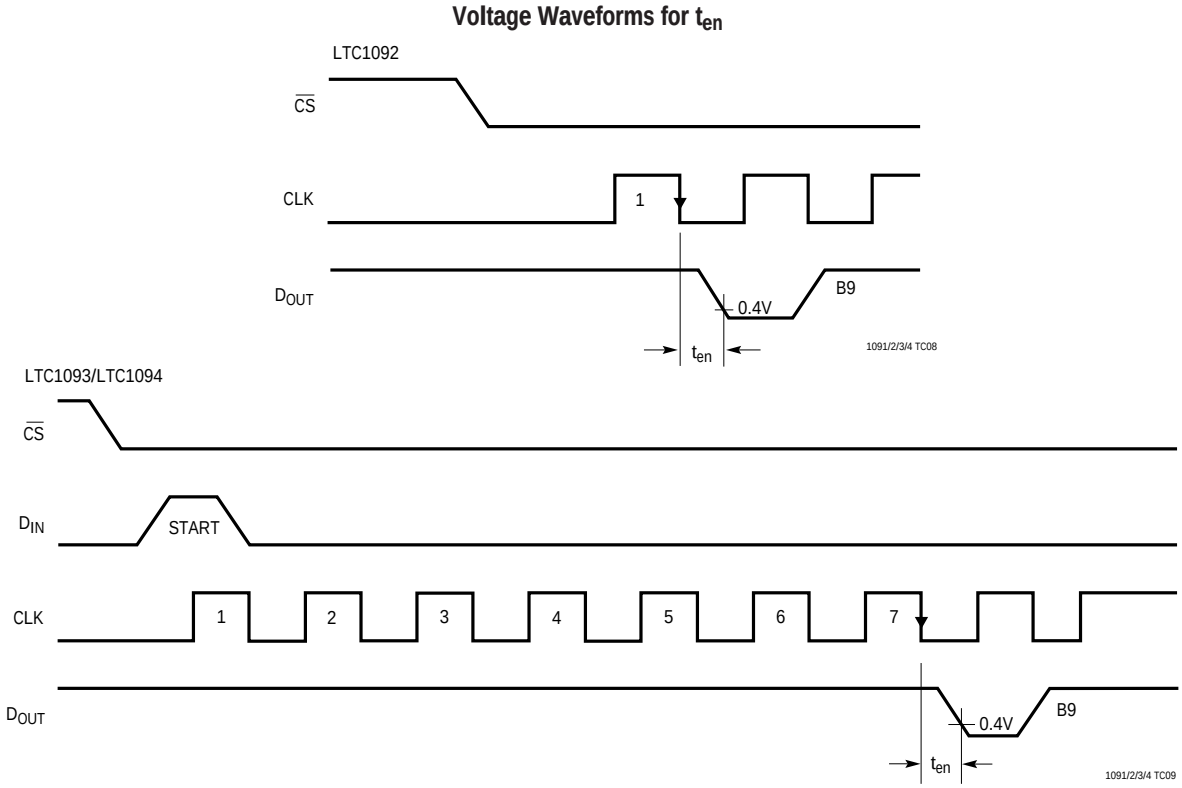
Voltage Waveforms for t_{en}



TEST CIRCUITS



APPLICATIONS INFORMATION

The LTC1091/LTC1092/LTC1093/LTC1094 are data acquisiton components that contain the following functional blocks:

1. 10-Bit Successive Approximation A/D Converter
2. Analog Multiplexer (MUX)
3. Sample-and-Hold (S/H)
4. Synchronous, Half-Duplex Serial Interface
5. Control and Timing Logic

DIGITAL CONSIDERATIONS

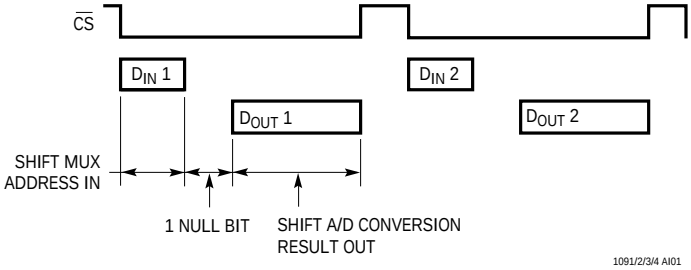
1. Serial Interface

The LTC1091/LTC1093/LTC1094 communicate with microprocessors and other external circuitry via a synchronous, half-duplex, 4-wire serial interface while the LTC1092 uses a 3-wire interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems. The LTC1091/LTC1093/LTC1094 first receive input data and then transmit back the A/D conversion result (half-duplex). Because of the half-duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just three wires: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls, the LTC1091/LTC1093/LTC1094 looks for a start bit. After the start bit is received, a 3-bit input word (6 bits for the LTC1093/LTC1094) is shifted into the D_{IN} input which configures the LTC1091/LTC1093/LTC1094 and starts the conversion. After one null bit, the result of the conversion is output on the D_{OUT} line. At the end of the data exchange, $\overline{CS}$ should be brought high. This resets the LTC1091/LTC1093/LTC1094 in preparation for the next data exchange.

The LTC1092 does not require a configuration input word and has no D_{IN} pin. A falling $\overline{CS}$ initiates data transfer as shown in the LTC1092 Operating Sequence. After $\overline{CS}$ falls,

APPLICATIONS INFORMATION



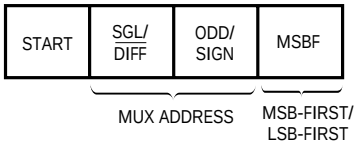
the first CLK pulse enables D_{OUT}. After one null bit, the A/D conversion result is output on the D_{OUT} line. Bringing $\overline{CS}$ high resets the LTC1092 for the next data exchange.

2. Input Data Word

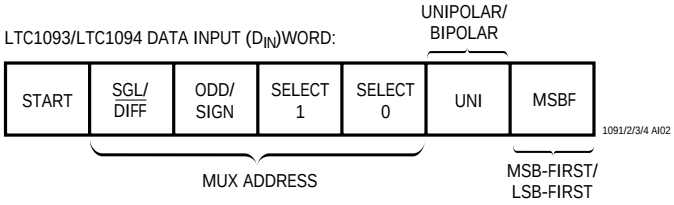
The LTC1092 requires no D_{IN} word. It is permanently configured to have a single differential input and to operate in unipolar mode. The conversion result is output on the D_{OUT} line in MSB-first sequence, followed by LSB-first sequence, providing easy interface to MSB- or LSB-first serial ports. The following disussion applies to the configuration of the LTC1091/LTC1093/LTC1094.

The LTC1091/LTC1093/LTC1094 clock data into the D_{IN} input on the rising edge of the clock. The input data words are defined as follows:

LTC1091 DATA INPUT (D_{IN}) WORD:

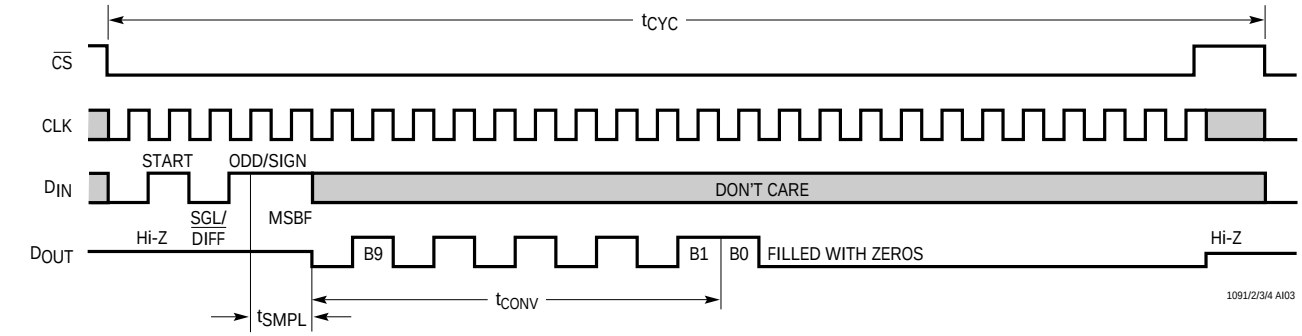


LTC1093/LTC1094 DATA INPUT (D_{IN})WORD:

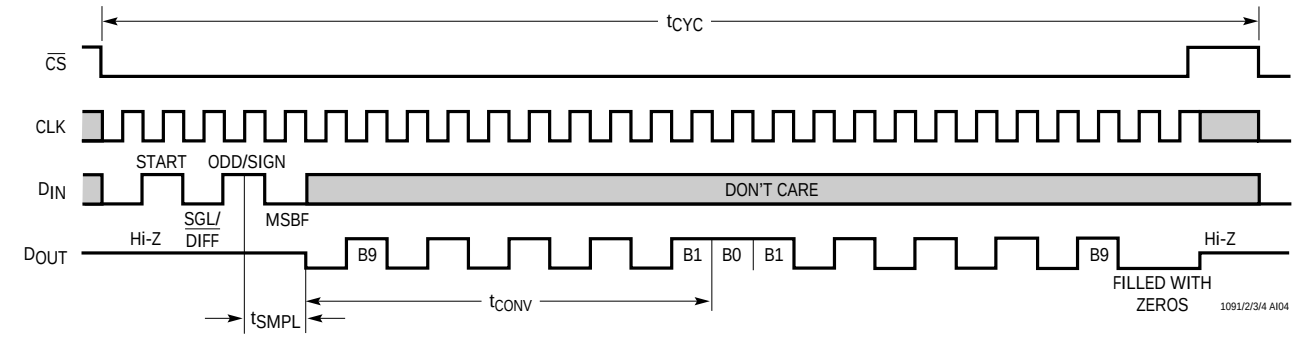


LTC1091 Operating Sequence
Example: Differential Inputs ($CH1^+$, $CH0^-$)

MSB-First Data (MSBF = 1)

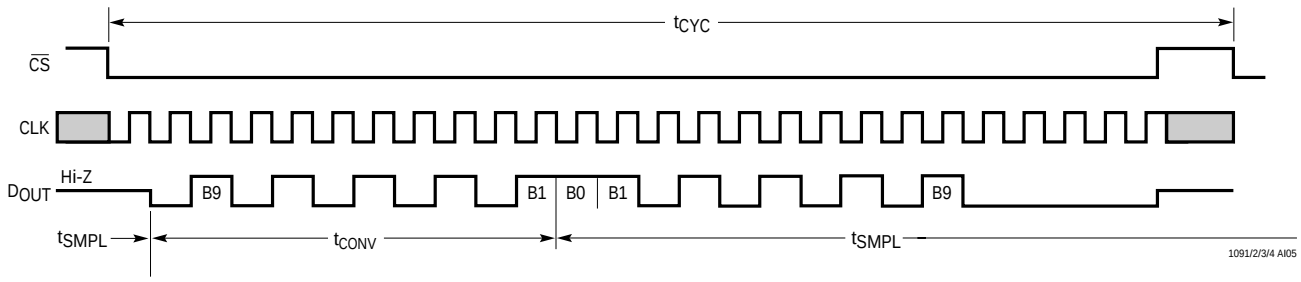


LSB-First Data (MSBF = 0)



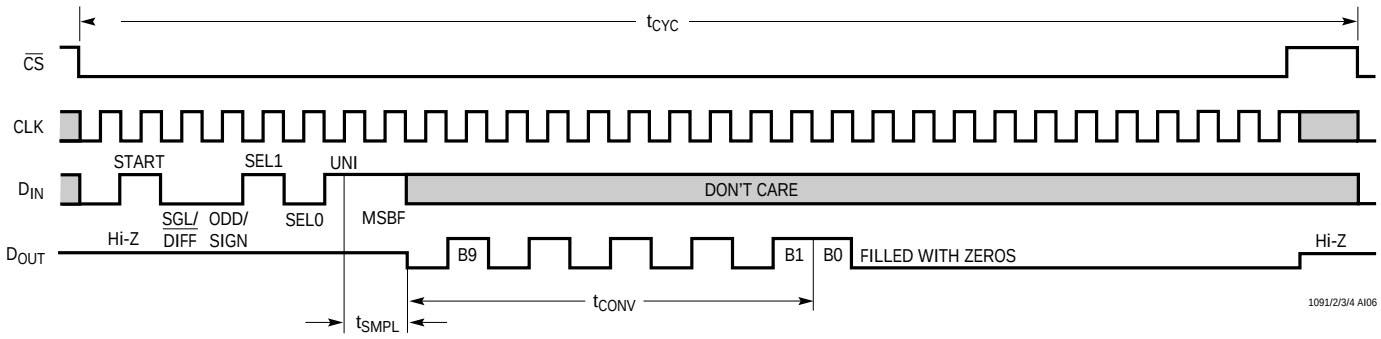
APPLICATIONS INFORMATION

LTC1092 Operating Sequence

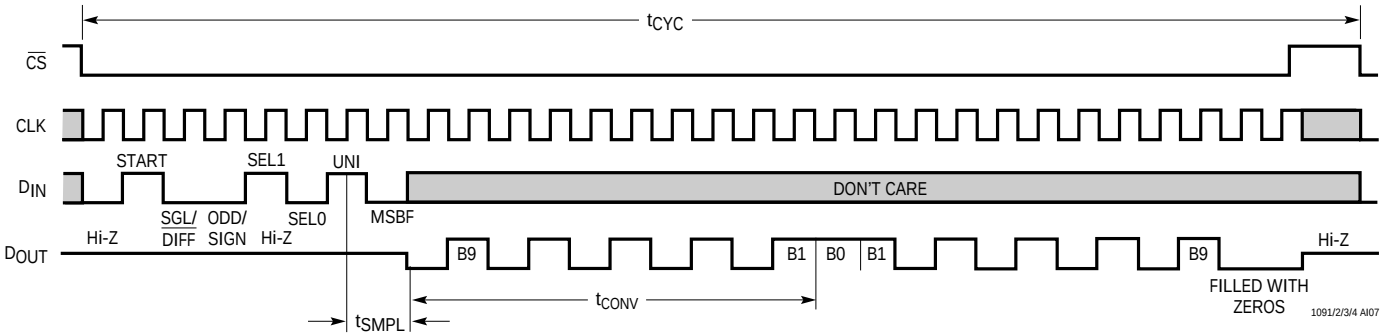


LTC1093/LTC1094 Operating Sequence
Example: Differential Inputs ($CH4^+$, $CH5^-$), Unipolar Mode

MSB-First Data (MSBF = 1)



LSB-First Data (MSBF = 0)



APPLICATIONS INFORMATION

Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer. The LTC1091/LTC1093/LTC1094 will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

Multiplexer (MUX) Address

The bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and – signs in the selected row of the following tables. In single-ended mode, all input channels are measured with respect to GND on the LTC1091 and COM on the LTC1093/LTC1094.

LTC1091 Channel Selection

	MUX ADDRESS		CHANNEL #		GND
	SGL/DIFF	ODD/SIGN	0	1	
SINGLE-ENDED MUX MODE	1	0	+		–
	1	1		+	–
DIFFERENTIAL MUX MODE	0	0	+	–	
	0	1	–	+	

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LTC1093 Channel Selection

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION					
SGL/DIFF	ODD/SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5
0	0	0	0	+	–				
0	0	0	1			+	–		
0	0	1	0					+	–
0	0	1	1	NOT USED					
0	1	0	0	–	+				
0	1	0	1			–	+		
0	1	1	0					–	+
0	1	1	1	NOT USED					

MUX ADDRESS				SINGLE-ENDED CHANNEL SELECTION						
SGL/DIFF	ODD/SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	COM
1	0	0	0	+						–
1	0	0	1			+				–
1	0	1	0					+		–
1	0	1	1	NOT USED						
1	1	0	0		+					–
1	1	0	1				+			–
1	1	1	0						+	–
1	1	1	1	NOT USED						

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LTC1094 Channel Selection

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION							
SGL/DIFF	ODD/SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7
0	0	0	0	+	–						
0	0	0	1			+	–				
0	0	1	0					+	–		
0	0	1	1							+	–
0	1	0	0	–	+						
0	1	0	1			–	+				
0	1	1	0					–	+		
0	1	1	1							–	+

MUX ADDRESS				SINGLE-ENDED CHANNEL SELECTION								
SGL/DIFF	ODD/SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7	COM
1	0	0	0	+								–
1	0	0	1			+						–
1	0	1	0					+				–
1	0	1	1							+		–
1	1	0	0		+							–
1	1	0	1				+					–
1	1	1	0						+			–
1	1	1	1								+	–

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APPLICATIONS INFORMATION

MSB-First/LSB-First (MSBF)

The output data of the LTC1091/LTC1093/LTC1094 is programmed for MSB-first or LSB-first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB-first format. Logical zeros will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When the MSBF bit is a logical zero, LSB-first data will follow the normal MSB-first data on the D_{OUT} line. (See operating sequence).

Unipolar/Bipolar (UNI)

The UNI bit of the LTC1093/LTC1094 determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below.

The LTC1091/LTC1092 are permanently configured for unipolar mode.

Unipolar Output Code (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5V)
1 1 1 1 1 1 1 1 1 1	V_{REF} – 1LSB	4.9951V
1 1 1 1 1 1 1 1 1 0	V_{REF} – 2LSB	4.9902V
•	•	•
•	•	•
•	•	•
0 0 0 0 0 0 0 0 0 1	1LSB	0.0049V
0 0 0 0 0 0 0 0 0 0	0V	0V

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Bipolar Output Code (UNI = 0) LTC1093/LTC1094 Only

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5V)
0 1 1 1 1 1 1 1 1 1	V_{REF} – 1LSB	4.9902V
0 1 1 1 1 1 1 1 1 0	V_{REF} – 2LSB	4.9805V
•	•	•
•	•	•
•	•	•
0 0 0 0 0 0 0 0 0 1	1LSB	0.0098V
0 0 0 0 0 0 0 0 0 0	0V	0V
1 1 1 1 1 1 1 1 1 1	–1LSB	–0.0098V
1 1 1 1 1 1 1 1 1 0	–2LSB	–0.0195V
•	•	•
•	•	•
•	•	•
1 0 0 0 0 0 0 0 0 1	–(V_{REF}) + 1LSB	–4.9902V
1 0 0 0 0 0 0 0 0 0	–(V_{REF})	–5.000V

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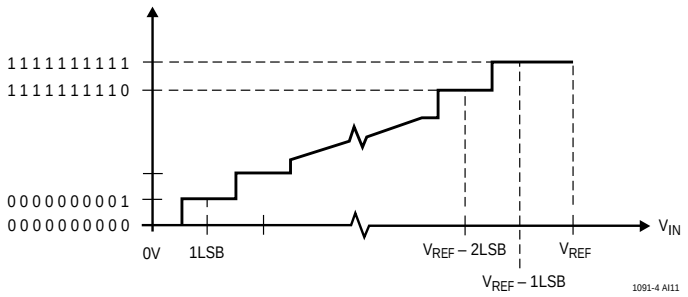
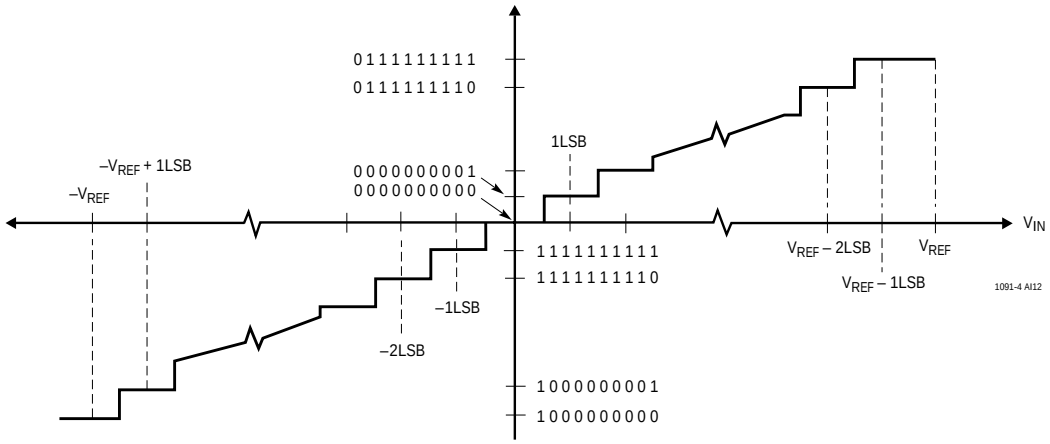
Unipolar Transfer Curve (UNI = 1)



Bipolar Transfer Curve (UNI = 0) LTC1093/LTC1094 Only



APPLICATIONS INFORMATION

3. Accommodating Microprocessors with Different Word Lengths

The LTC1091/LTC1093/LTC1094 will fill zeros indefinitely after the transmitted data until $\overline{CS}$ is brought high. At that time the D_{OUT} line is disabled. This makes interfacing easy to MPU serial ports with different transfer increments including 4 bits (e.g., COP400) and 8 bits (e.g., SPI and MICROWIRE/PLUS™). Any word length can be accommodated by the correct positioning of the start bit in the LTC1091 input word.

Figure 1 shows examples of LTC1091 input and output words for 4-bit and 8-bit processors. A complete data exchange can be implemented with two 4-bit MPU outputs and three inputs in 4-bit systems and one 8-bit output and two inputs in 8-bit systems. The resulting data winds up left justified in the MPU with zeros automatically filled in the unused low order bits by the LTC1091. In section 5 another example is given using the MC68HC05C4 which eliminates one 8-bit transfer and positions data right justified inside the MPU.

4. Operation with D_{IN} and D_{OUT} Tied Together

The LTC1091/LTC1093/LTC1094 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the MPU. Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1091, for example, will take control of the data line and drive it low on the 4th falling CLK edge after the start bit is received (see Figure 2). Therefore, the processor port line must be switched to an input before this happens, to avoid a conflict.

In the next section, an example is made of interfacing the LTC1091 with D_{IN} and D_{OUT} tied together to the Intel 8051 MPU.

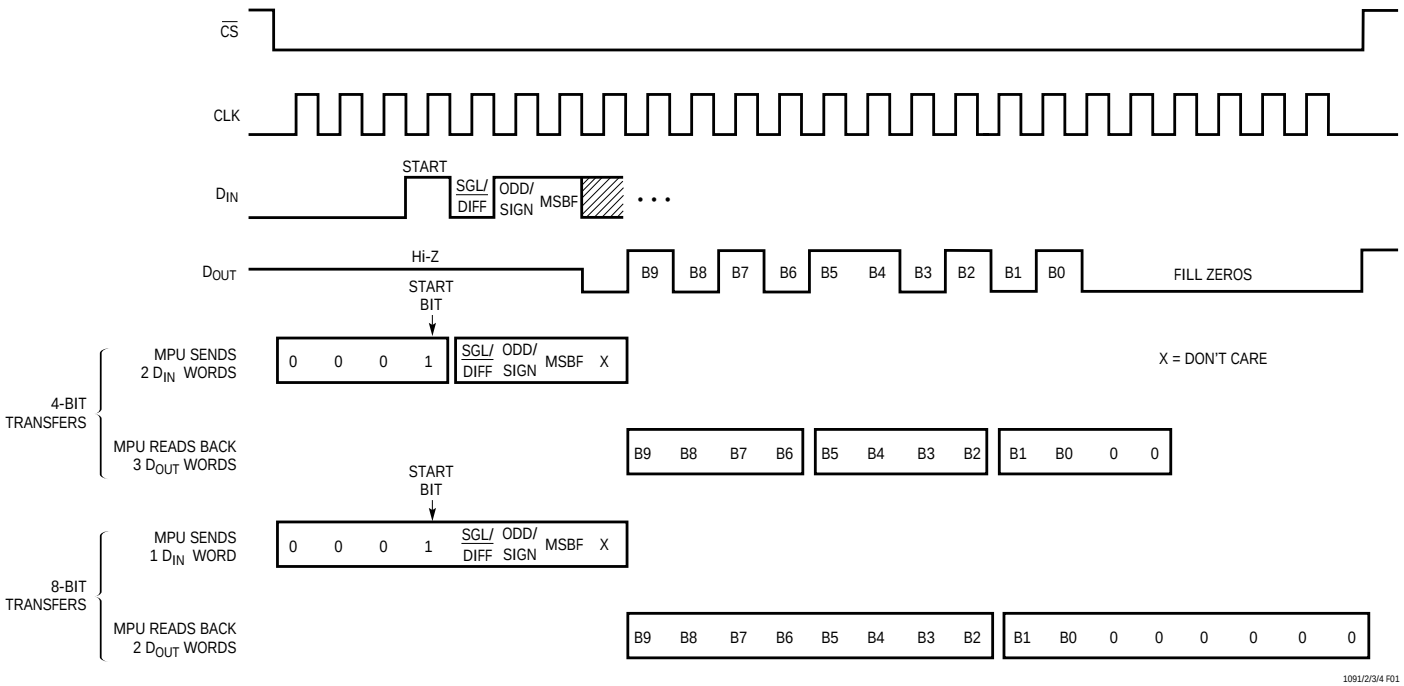


Figure 1. LTC1091 Input and Output Word Arrangements for 4-Bit and 8-Bit Serial Port Microprocessors

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APPLICATIONS INFORMATION

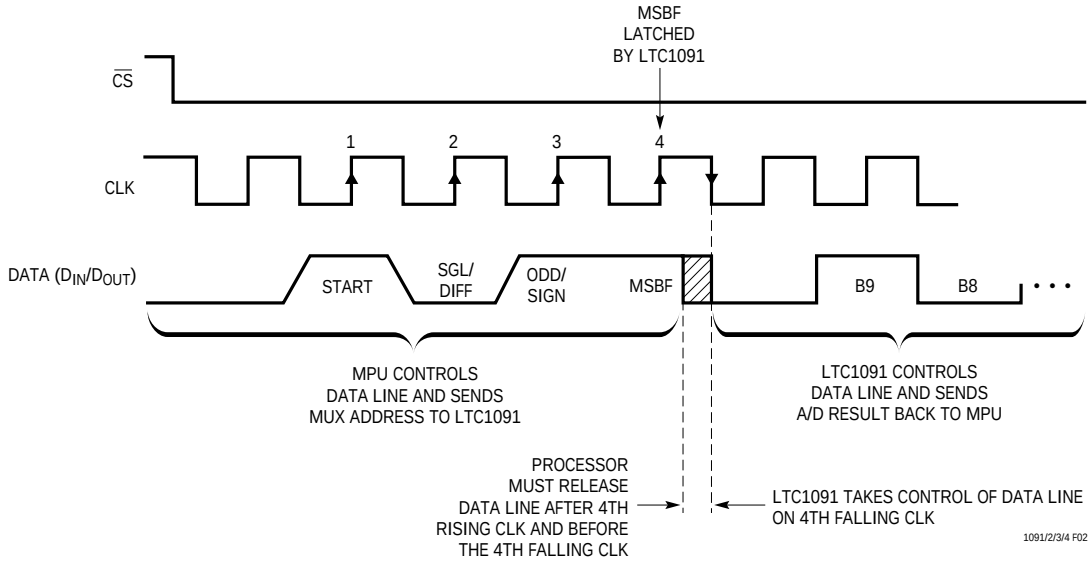

Figure 2. LTC1091 Operation with D_{IN} and D_{OUT} Tied Together

5. Microprocessor Interfaces

The LTC1091/LTC1092/LTC1093/LTC1094 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then three or four of the MPU's parallel port lines can be programmed to form the serial link to the LTC1091/LTC1092/LTC1093/LTC1094. Included here are one serial interface example and one example showing a parallel port programmed to form the serial interface.

Table 1. Microprocessors with Hardware Serial Interfaces Compatible with the LTC1091/LTC1092/LTC1093/LTC1094

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD63705	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	CSI/O
National Semiconductor	
COP400 Family	MICROWIRE™
COP800 Family	MICROWIRE/PLUS
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020	Serial Port

*Requires external hardware
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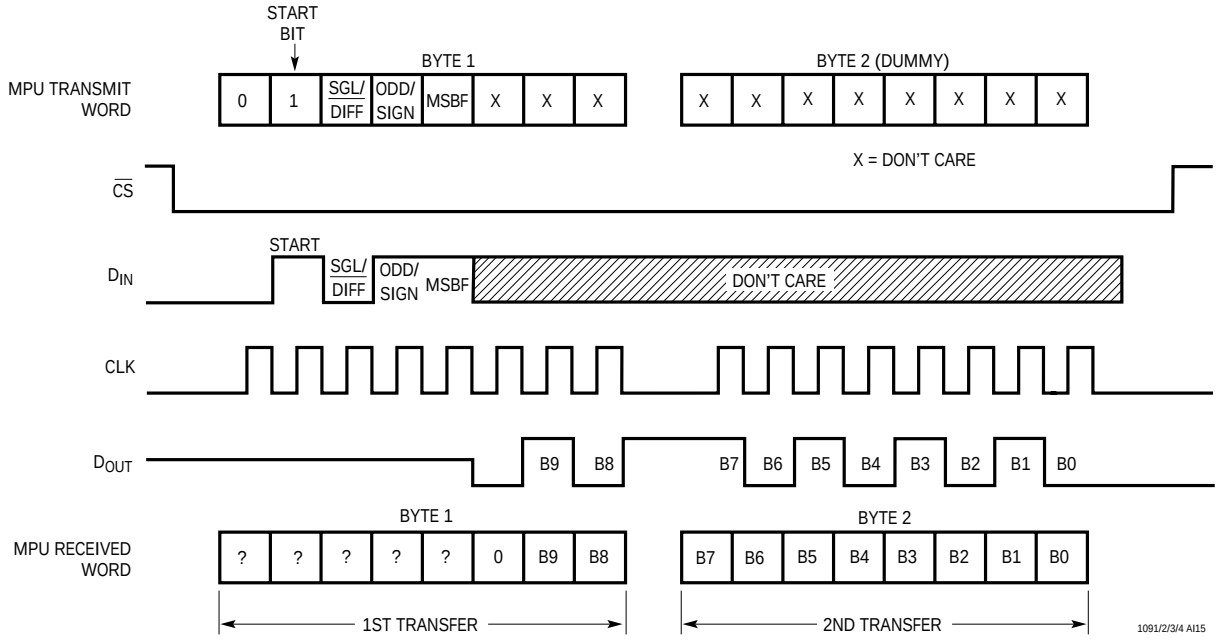
APPLICATIONS INFORMATION

Motorola SPI (MC68HC05C4, MC68HC11)

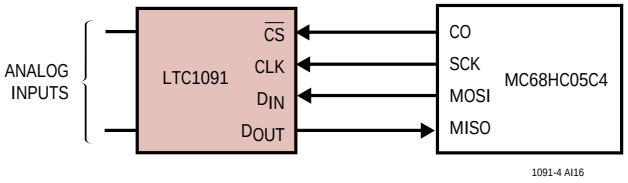
The MC68HC05C4 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB first and in 8-bit increments. With two 8-bit transfers, the A/D result is read into the MPU. The first 8-bit transfer sends the D_{IN} word to the LTC1091 and clocks B9 and B8 of the A/D conversion result into the processor. The second 8-bit transfer clocks the remaining bits, B7 through B0, into the MPU.

ANDing the first MPU received byte with 03 Hex clears the six most significant bits. Notice how the position of the start bit in the first MPU transmit word is used to position the A/D result right justified in two memory locations.

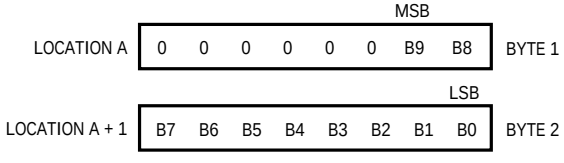
Data Exchange Between LTC1091 and MC68HC05C4



Hardware and Software Interface to Motorola MC68HC05C4 Processor



D_{OUT} from LTC1091 Stored in MC68HC05C4 RAM



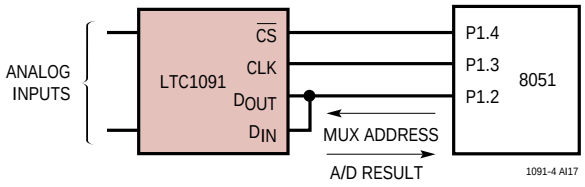
LABEL	MNEMONIC	COMMENTS
START	BCLRn	Bit 0 Port C Goes Low ($\overline{CS}$ Goes Low)
	LDA	Load LTC1090 D_{IN} Word into Acc
	STA	Load LTC1090 D_{IN} Word into SPI from Acc
		Transfer Begins
	TST	Test Status of SPIF
	BPL	Loop to Previous Instruction If Not Done with Transfer
	LDA	Load contents of SPI Data Register into Acc (D_{OUT} MSBs)
	STA	Start Next SPI Cycle
	AND	Clear 6 MSBs of First D_{OUT} Word
	STA	Store in Memory Location A (MSBs)
	TST	Test Status of SPIF
	BPL	Loop to Previous Instruction If Not Done with Transfer
	BSETn	Set B0 of Port C ($\overline{CS}$ Goes High)
	LDA	Load contents of SPI Data Register into Acc (D_{OUT} LSBs)
	STA	Store in Memory location A + 1 (LSBs)

APPLICATIONS INFORMATION

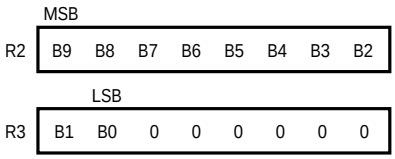
Interfacing to the Parallel Port of the Intel 8051 Family

The Intel 8051 has been chosen to demonstrate the interface between the LTC1091 and parallel port microprocessors. Normally, the $\overline{CS}$, SCLK and D_{IN} signals would be generated on three port lines and the D_{OUT} signal read on a 4th port line. This works very well. However, we will demonstrate here an interface with the D_{IN} and D_{OUT} of the LTC1091 tied together as described in section 4. This saves one wire.

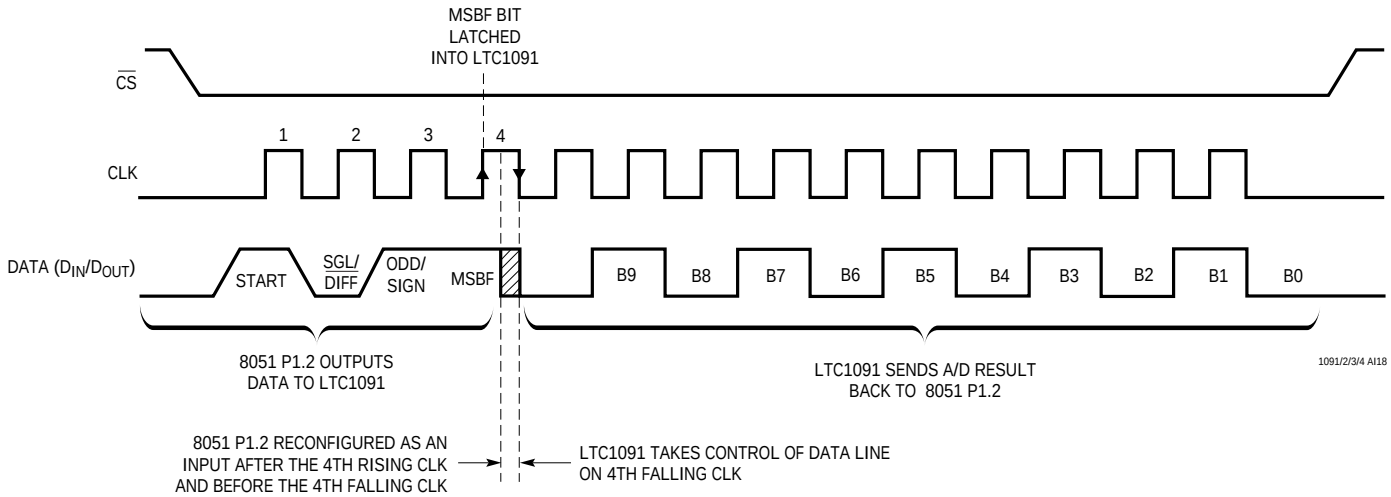
The 8051 first sends the start bit and MUX address to the LTC1091 over the data line connected to P1.2. Then P1.2 is reconfigured as an input (by writing to it a one) and the 8051 reads back the 10-bit A/D result over the same data line.



D_{OUT} from LTC1091 Stored in 8051 RAM



LABEL	MNEMONIC	OPERAND	COMMENTS
	MOV	A, #FFH	D_{IN} Word for LTC1091
	SETB	P1.4	Make Sure $\overline{CS}$ Is High
	CLR	P1.4	$\overline{CS}$ Goes Low
	MOV	R4, #04	Load Counter
LOOP 1	RLC	A	Rotate D_{IN} Bit into Carry
	CLR	P1.3	SCLK Goes Low
	MOV	P1.2, C	Output D_{IN} Bit to LTC1091
	SETB	P1.3	SCLK Goes High
	DJNZ	R4, LOOP 1	Next Bit
	MOV	P1, #04	Bit 2 Becomes an Input
	CLR	P1.3	SCLK Goes Low
	MOV	R4, #09	Load Counter
LOOP	MOV	C, P1.2	Read Data Bit into Carry
	RLC	A	Rotate Data Bit into Acc
	SETB	P1.3	SCLK Goes High
	CLR	P1.3	SCLK Goes Low
	DJNZ	R4, LOOP	Next Bit
	MOV	R2, A	Store MSBs in R2
	MOV	C, P1.2	Read Data Bit into Carry
	SETB	P1.3	SCLK Goes High
	CLR	P1.3	SCLK Goes Low
	CLR	A	Clear Acc
	RLC	A	Rotate Data Bit from Carry to Acc
	MOV	C, P1.2	Read Data Bit into Carry
	RRC	A	Rotate Right into Acc
	RRC	A	Rotate Right into Acc
	MOV	R3, A	Store LSBs in R3
	SETB	P1.4	$\overline{CS}$ Goes High



APPLICATIONS INFORMATION

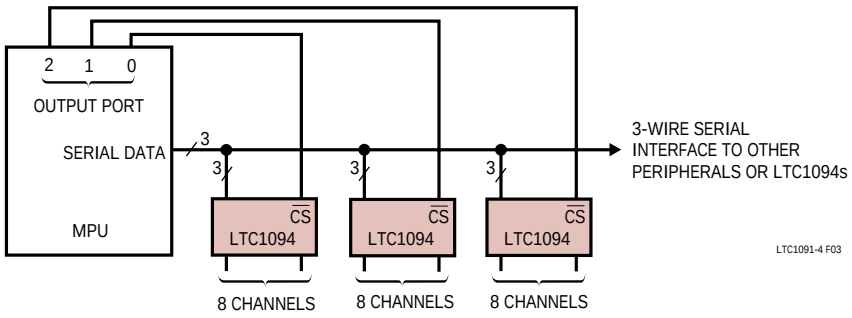


Figure 3. Several LTC1094s Sharing One 3-Wire Serial Interface

Sharing the Serial Interface

The LTC1094 can share the same 2- or 3-wire serial interface with other peripheral components or other LTC1094s (see Figure 3). In this case, the $\overline{CS}$ signals decide which LTC1094 is being addressed by the MPU.

ANALOG CONSIDERATIONS

1. Grounding

The LTC1091/LTC1092/LTC1093/LTC1094 should be used with an analog ground plane and single point grounding techniques.

The AGND pin (GND on the LTC1091/LTC1092) should be tied directly to this ground plane.

The DGND pin of the LTC1093/LTC1094 can also be tied directly to this ground plane because minimal digital noise is generated within the chip itself.

The V_{CC} pin should be bypassed to the ground plane with a 4.7µF tantalum with leads as short as possible. AV_{CC} and DV_{CC} should be tied together on the LTC1094. The V^- pin (LTC1093/LTC1094) should be bypassed with a 0.1µF ceramic disk. For single supply applications, V^- can be tied to the ground plane.

It is also recommended that the REF^- pin and the COM pin be tied directly to the ground plane. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

Figure 4 shows an example of an ideal LTC1091 ground plane design for a 2-sided board. Of course, this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

2. Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to analog ground during a conversion cycle can induce errors or noise in the output code. Because the V_{CC} (V_{REF}) pin of the LTC1091 defines the voltage span of the A/D converter, its bypassing is especially important. V_{CC} noise and ripple can be kept below 1mV by bypassing the V_{CC} pin directly to the analog ground plane with a 4.7µF tantalum with leads as short as possible. AV_{CC} and DV_{CC} should be tied together on the LTC1094. Figures 5 and 6 show the effects of good and poor V_{CC} bypassing.

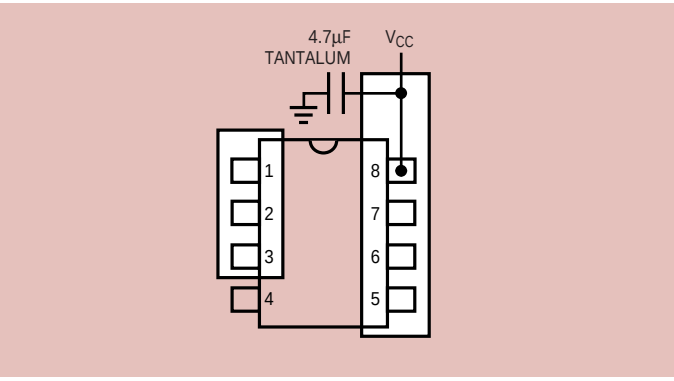


Figure 4. Example Ground Plane for the LTC1091

APPLICATIONS INFORMATION

3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1091/LTC1092/LTC1093/LTC1094 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to ensure that the transients caused by the current spikes settle completely before the conversion begins.

Source Resistance

The analog inputs of the LTC1091/LTC1092/LTC1093/LTC1094 look like a 60pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}) as shown in Figure 7. C_{IN} gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

"+" Input Settling

This input capacitor is switched onto the "+" input during the sample phase (t_{SMPL}, see Figure 8). The sample phase is the 1 1/2 CLK cycles before the conversion starts. The voltage on the "+" input must settle completely within this sample time. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 3µs, **R_{SOURCE}^+ < 2k and C1 < 20pF will provide adequate settling**.

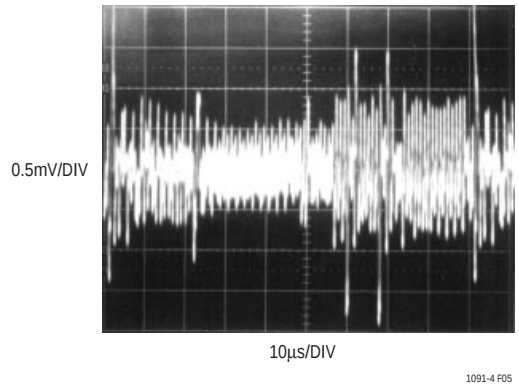


Figure 5. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors

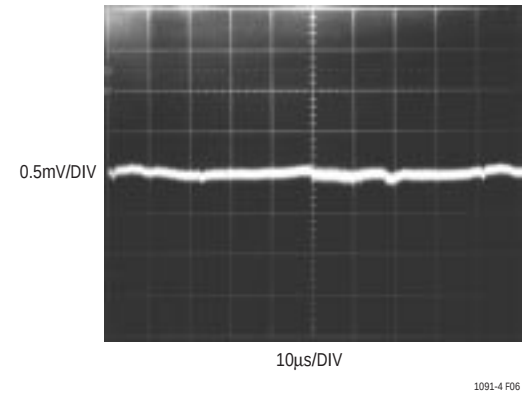


Figure 6. Good V_{CC} Bypassing Keeps Noise and Ripple on V_{CC} Below 1mV

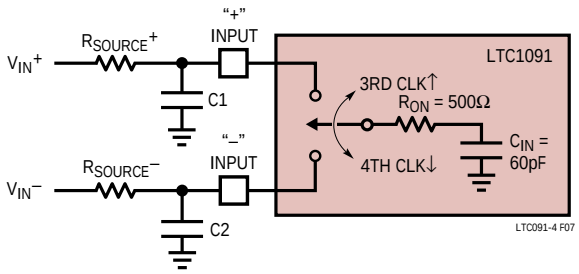


Figure 7. Analog Input Equivalent Circuit

APPLICATIONS INFORMATION

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "–" input and the conversion starts (see Figure 8). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. However, it is critical that the "–" input voltage settle completely during the first CLK cycle of the conversion time and be free of noise. Minimizing R_{SOURCE}^- and C2 will improve settling time. If large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency. At the maximum CLK rate of 500kHz, **R_{SOURCE}^- < 1kΩ and C2 < 20pF will provide adequate settling.**

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 8). Again, the "+" and "–" input sampling times can be extended as previously described to accommodate slower op amps. Most op amps, including the LT1006 and LT1013 single supply op amps, can be made to settle well even with the minimum settling windows of 3µs ("+" input) and 2µs ("–" input) which occur at the maximum clock rate of 500kHz. Figures 9 and 10 show examples of adequate and poor op amp settling.

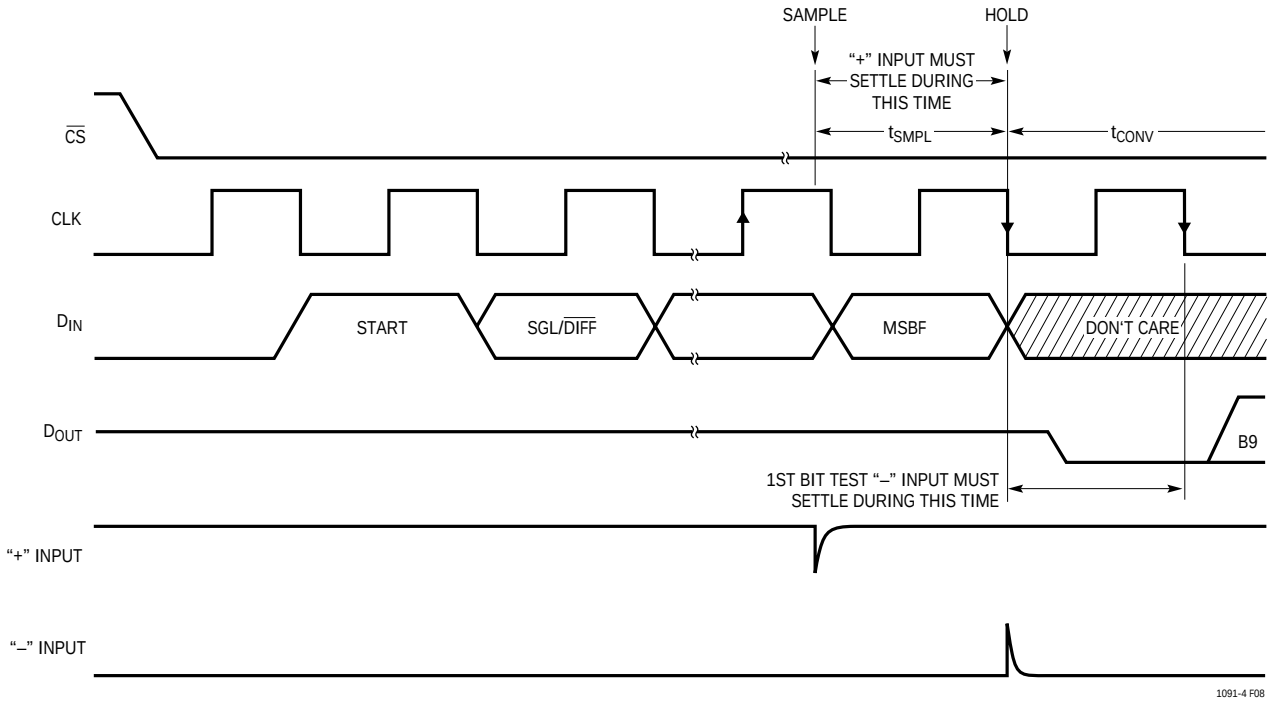


Figure 8. "+" and "–" Input Settling Windows

APPLICATIONS INFORMATION

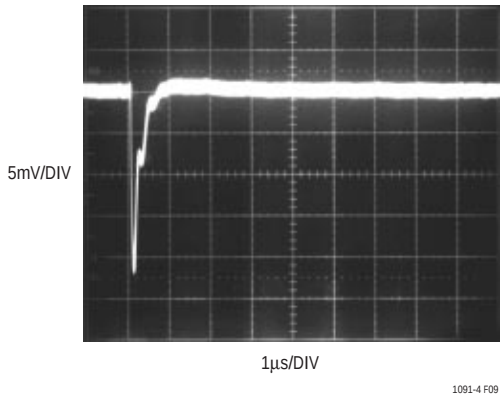


Figure 9. Adequate Settling of Op Amp Driving Analog Input

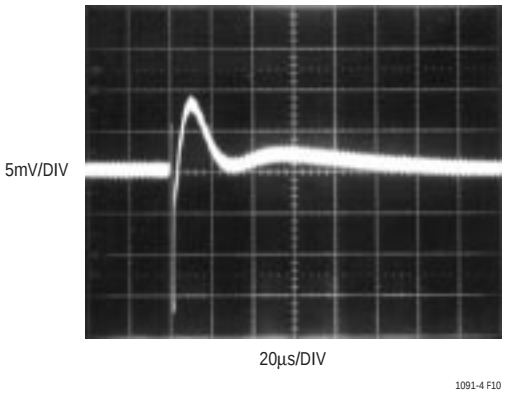


Figure 10. Poor Op Amp Settling Can Cause A/D Errors

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 11. For large values of C_F (e.g., 1µF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = (60pF)(V_{IN}/t_{CYC})$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 32µs, the input current equals 9µA at $V_{IN} = 5V$. In this case, a filter resistor of 50Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time as shown in the typical curve of Maximum Filter Resistor vs Cycle Time.

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1µA (at 125°C) flowing through a source resistance of 1kΩ will cause a voltage drop of 1mV or 0.2LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see the typical curve of Input Channel Leakage Current vs Temperature).

4. Sample-and-Hold

Single-Ended Inputs

The LTC1091/LTC1093/LTC1094 provide a built-in sample-and-hold (S&H) function for all signals acquired in the single-ended mode. This sample-and-hold allows conversion of rapidly varying signals (see typical curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 8. The sampling interval begins as the bit preceding the MSBF bit is shifted in and continues until the falling CLK edge after the MSBF bit is received. On this falling edge, the S&H goes into hold mode and the conversion begins.

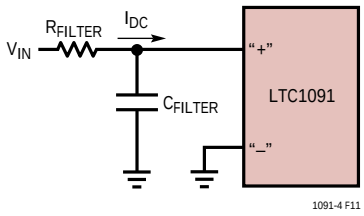


Figure 11. RC Input Filtering

APPLICATIONS INFORMATION

Differential Inputs

With differential inputs, the A/D no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 10 CLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR(MAX)} = (V_{PEAK})(2\pi) \bullet f("-")(10/f_{CLK})$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 0.25LSB error (1.25mV) with the converter running at CLK = 500kHz, its peak value would have to be 150mV.

5. Reference Inputs

The voltage between the reference inputs of the LTC1091/LTC1092/LTC1093/LTC1094 defines the voltage span of the A/D converter. The reference inputs look primarily like a 10k resistor but will have transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 12). During each bit test of the conversion (every CLK cycle), a capacitive current spike will be generated on the reference pins by the A/D. These current spikes settle quickly and do not cause a problem. However, if slow settling circuitry is used to drive the reference inputs, care must be taken to ensure that transients caused by these current spikes settle completely during each bit test of the conversion.

When driving the reference inputs, three things should be kept in mind:

1. The source resistance (R_{OUT}) driving the reference inputs should be low (less than 1Ω) to prevent DC drops caused by the 1mA maximum reference current (I_{REF}).
2. Transients on the reference inputs caused by the capacitive switching currents must settle completely during each bit test (each CLK cycle). Figures 13 and 14 show examples of both adequate and poor settling. Using a slower CLK will allow more time for the reference to settle. However, even at the maximum CLK rate of 500kHz most references and op amps can be made to settle within the 2µs bit time.
3. It is recommended that the REF^- input of the LTC1094 be tied directly to the analog ground plane. If REF^- is biased at a voltage other than ground, the voltage must not change during a conversion cycle. This voltage must also be free of noise and ripple with respect to analog ground.

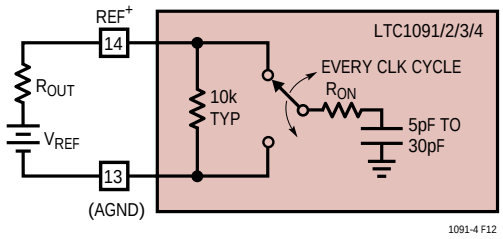


Figure 12. Reference Input Equivalent Circuit

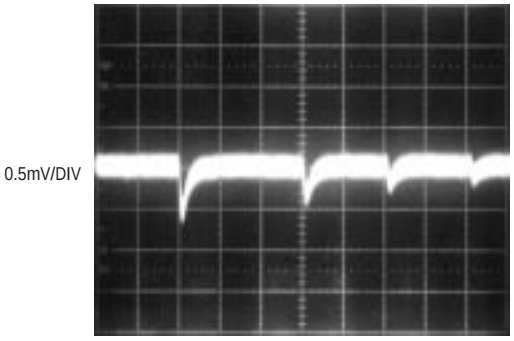


Figure 13. Adequate Reference Settling

APPLICATIONS INFORMATION

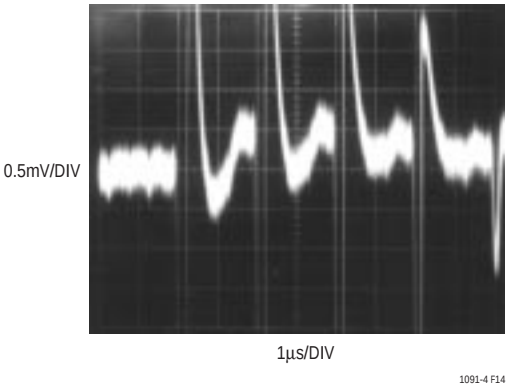


Figure 14. Poor Reference Settling Can Cause A/D Errors

6. Reduced Reference Operation

The minimum reference voltage of the LTC1091 is limited to 4.5V because the V_{CC} supply and reference are internally tied together. However, the LTC1092/LTC1093/LTC1094 can operate with reference voltages below 1V.

The effective resolution of the LTC1092/LTC1093/LTC1094 can be increased by reducing the input span of the converter. The parts exhibit good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Full-Scale Error vs Reference Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values:

1. Offset
2. Noise
3. Conversion speed (CLK frequency)

Offset with Reduced V_{REF}

The offset of the LTC1092/LTC1093/LTC1094 has a larger effect on the output code when the A/D is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 0.5mV which is 0.1LSB with a 5V reference becomes 0.5LSB with a 1V reference and 2.5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input to the LTC1092/LTC1093/LTC1094.

Noise with Reduced V_{REF}

The total input-referred noise of the LTC1092/LTC1093/LTC1094 can be reduced to approximately 200µV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200µV of noise.

For operation with a 5V reference, the 200µV noise is only 0.04LSB peak-to-peak. In this case, the LTC1092/LTC1093/LTC1094 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1V reference, this same 200µV noise is 0.2LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.2LSB. If the reference is further reduced to 200mV, the 200µV noise becomes equal to one LSB and a stable code may be difficult to achieve. In this case averaging readings may be necessary.

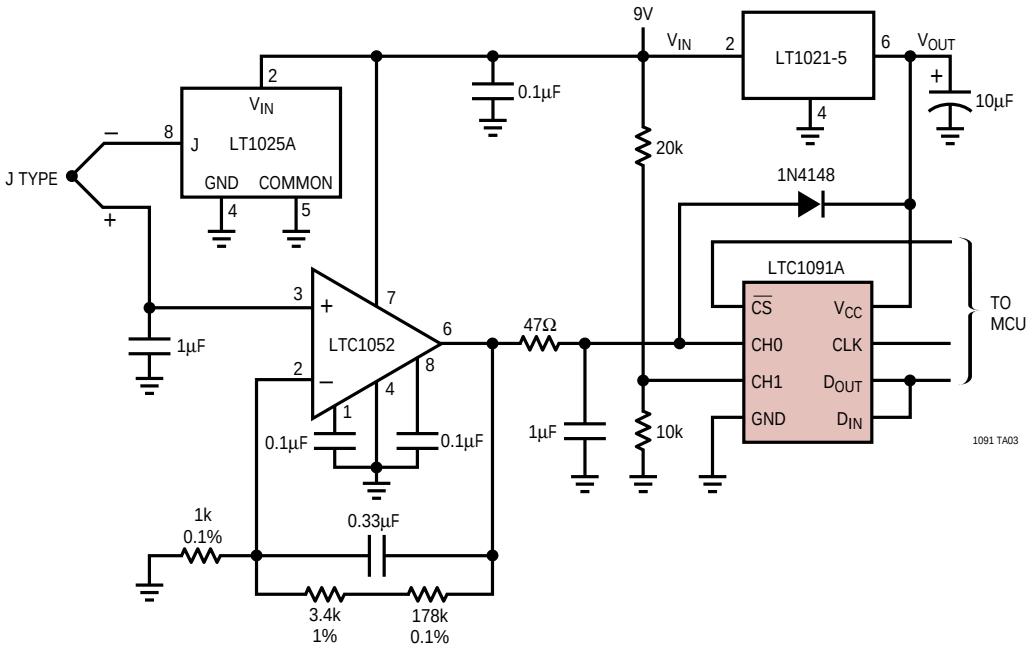
This noise data was taken in a very clean setup. Any setup-induced noise (noise or ripple on V_{CC}, V_{REF}, V_{IN} or V^-) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

Conversion Speed with Reduced V_{REF}

With reduced reference voltages, the LSB step size is reduced and the LTC1092/LTC1093/LTC1094 internal comparator overdrive is reduced. Therefore, it may be necessary to reduce the maximum CLK frequency when low values of V_{REF} are used.

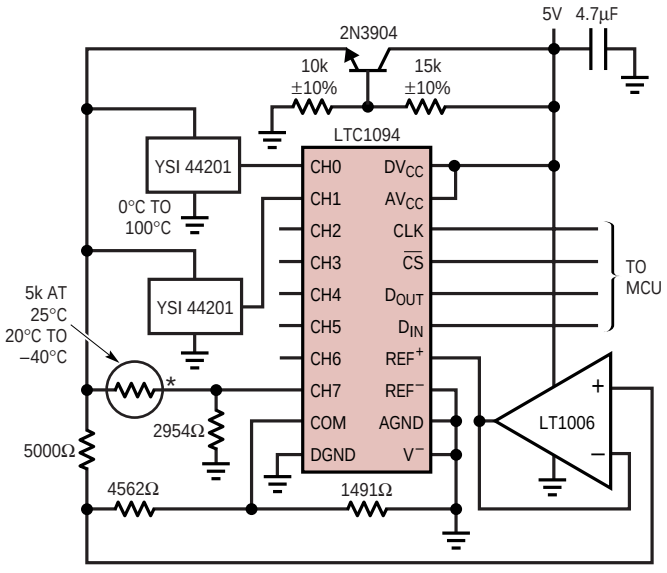
TYPICAL APPLICATIONS

0°C to 500°C Furnace Exhaust Gas Temperature Monitor with Low Supply Detection



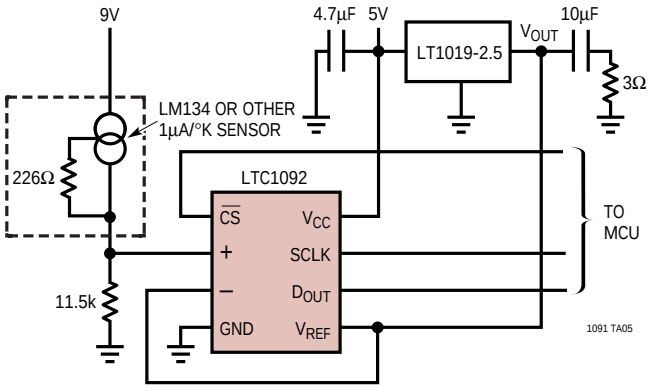
TYPICAL APPLICATIONS

0°C to 100°C 0.25°C Accurate Thermistor Based Temperature Measurement System



*YSI 44007, 44034 OR EQUIVALENT

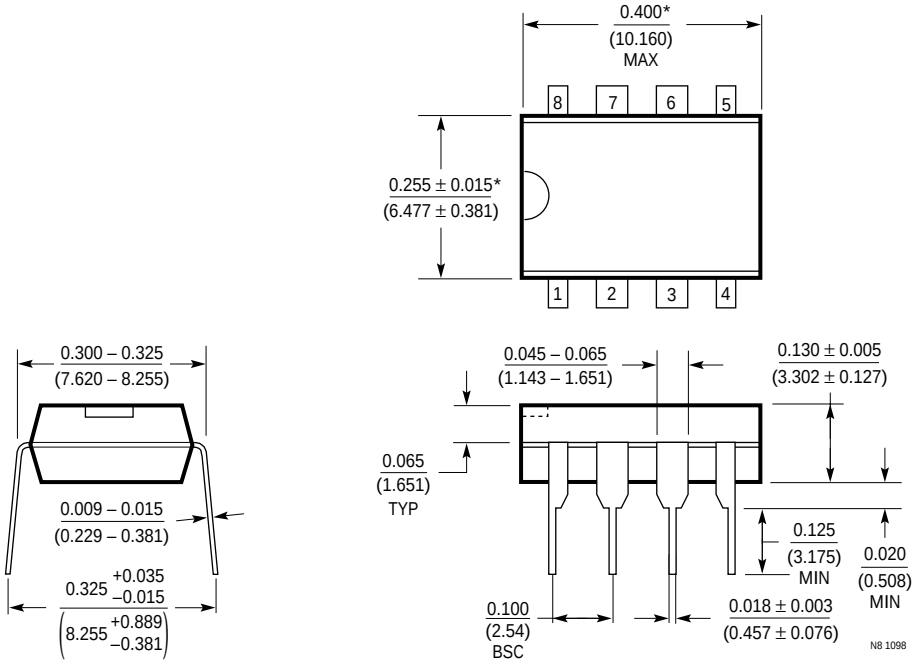
–55°C to 125°C Thermometer Using Current Output Silicon Sensors



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

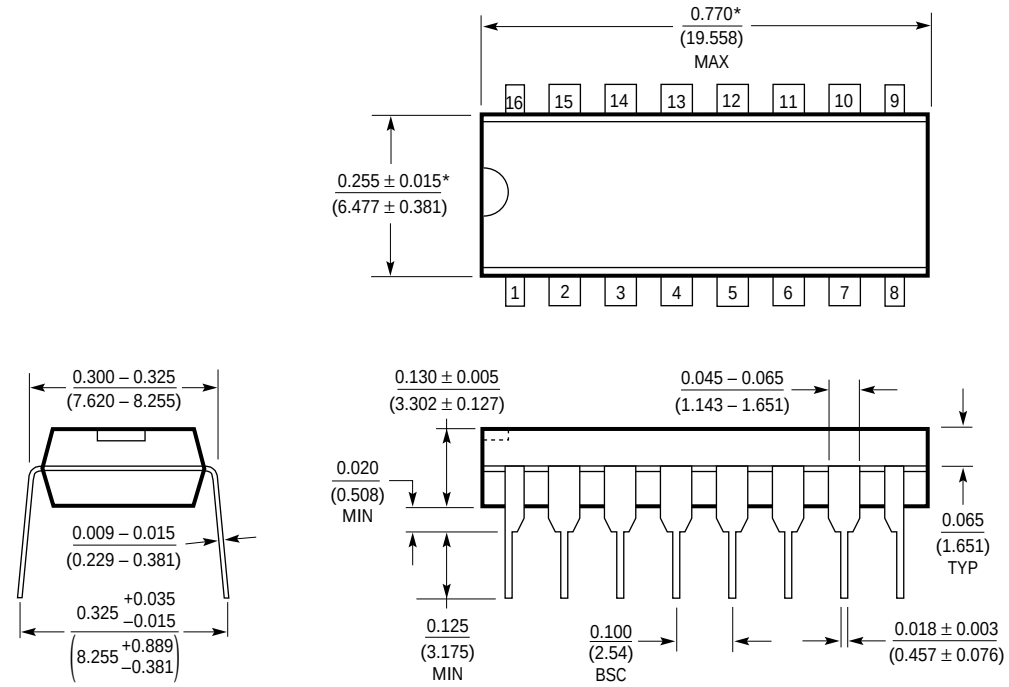


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
16-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



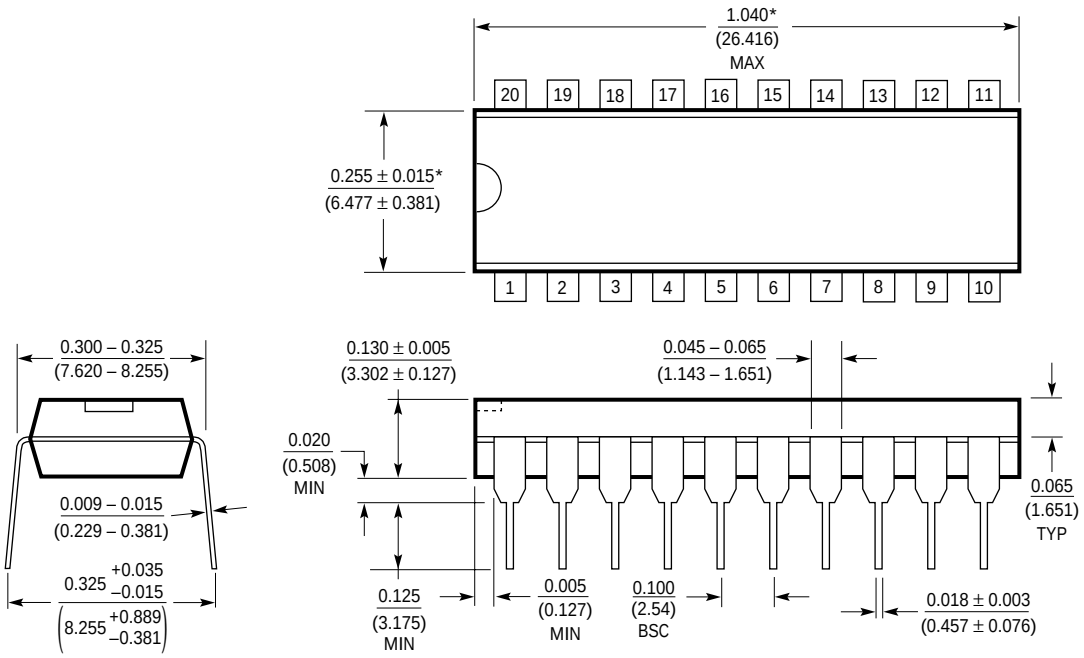
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N16 1098

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
20-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



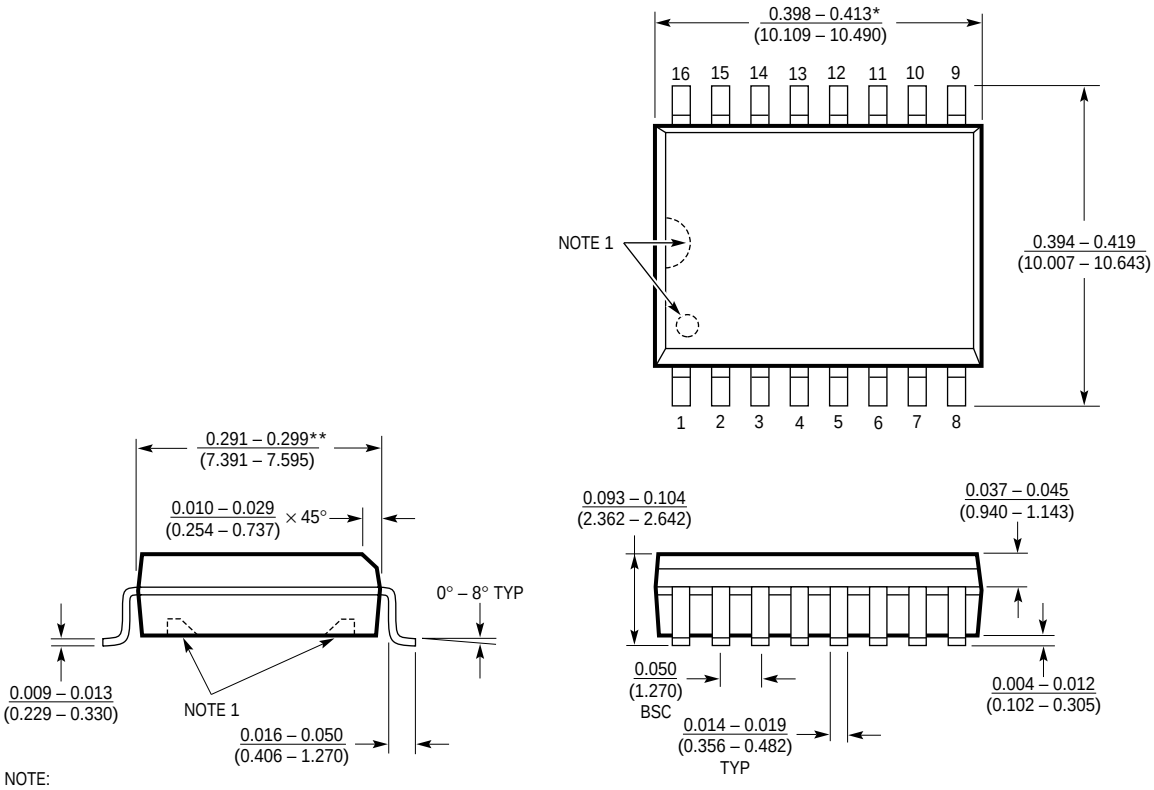
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N20 1098

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

SW Package
16-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

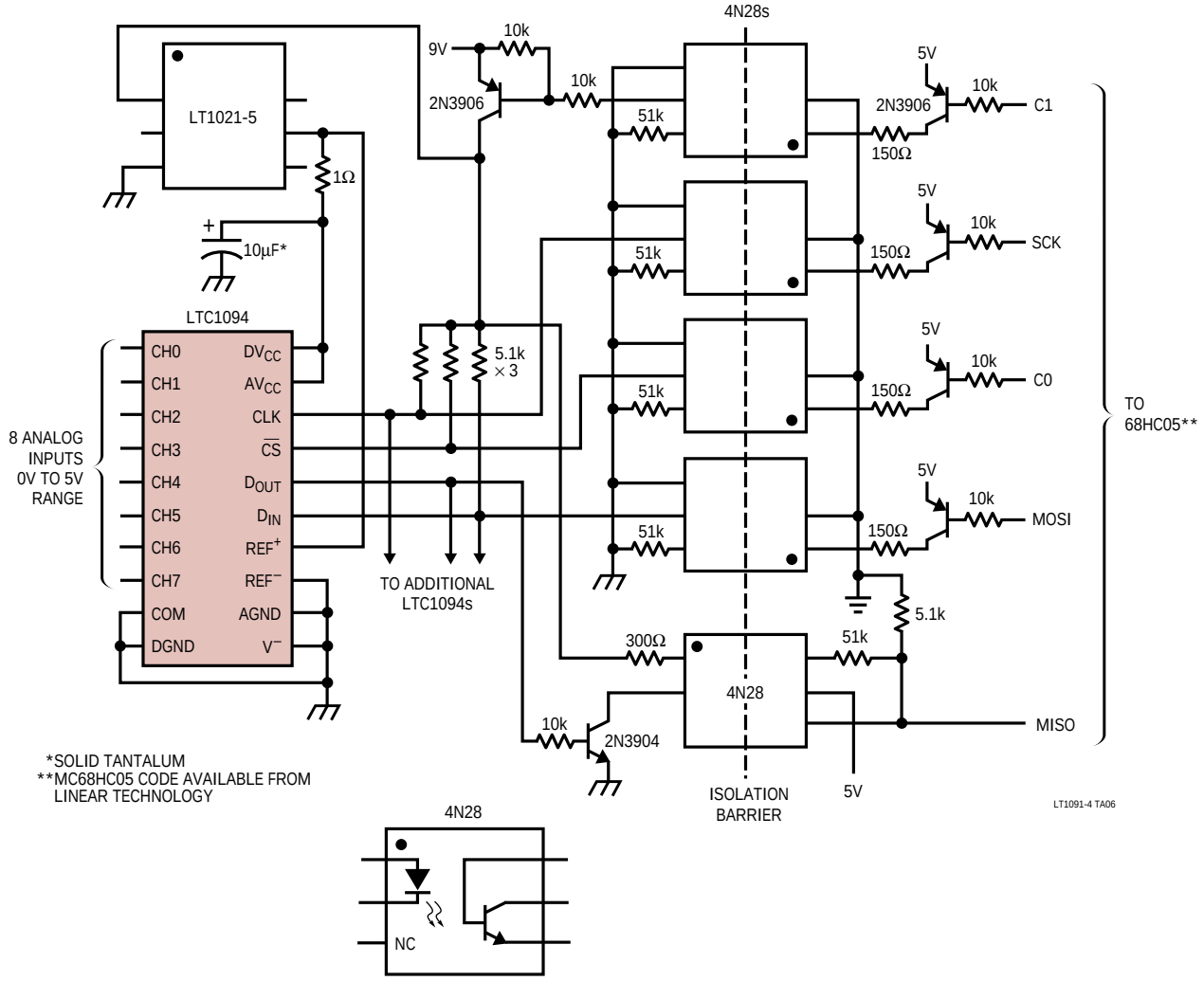
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S16 (WIDE) 1098

TYPICAL APPLICATION

Micropower, 500V Optoisolated, Multichannel, 10-Bit Data Acquisition System Is Accessed Once Every Two Seconds



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1090	10-Bit, 8-Channel ADC	Serial I/O, 1.5mA Supply Current
LTC1291/LTC1292	12-BIT, 2-Channel and Differential ADCs	Pin Compatible Upgrades to LTC1091/LTC1092
LTC1293/LTC1294	12-Bit, 6- and 8-Channel ADCs	Pin Compatible Upgrades to LTC1093/LTC1094

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
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- Alternative Solution
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