THE DATASHEET OF

LTC1040CSW#PBF

www.win-source.net 0086-755-83957316

Dual Micropower Comparator

FEATURES

- Micropower
  1.5µW (1 Sample/Second)
- Power Supply Flexibility
  Single Supply 2.8V to 16V
  Split Supply ±2.8V to ±8V
- *Guaranteed* Max Offset 0.75mV
- *Guaranteed* Max Tracking Error Between Input Pairs ± 0.1%
- Input Common Mode Range to Both Supply Rails
- TTL/CMOS Compatible with ±5V or Single 5V Supply
- Input Errors are Stable with Time and Temperature

APPLICATIONS

- Battery-Powered Systems
- Remote Sensing
- Window Comparator
- BANG-BANG Controllers

DESCRIPTION

The LTC®1040 is a monolithic CMOS dual comparator manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. Extremely low operating power levels are achieved by internally switching the comparator ON for short periods of time. The CMOS output logic holds the output information continuously while not consuming any power.

In addition to switching power ON, a switched output is provided to drive external loads during the comparator's active time. This allows not only low comparator power, but low total system power.

Sampling is controlled by an external strobe input or an internal oscillator. The oscillator frequency is set by an external RC network.

Each comparator has a unique input structure, giving two differential inputs. The output of the comparator will be high if the algebraic sum of the inputs is positive and low if the algebraic sum of the inputs is negative.

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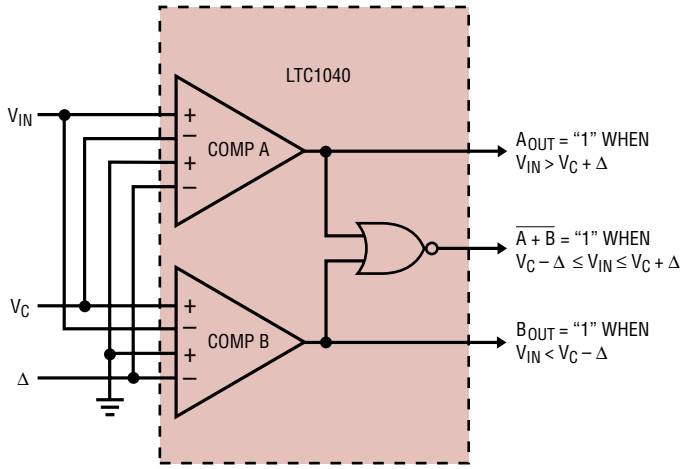
LTCMOS™ is a trademark of Linear Technology Corporation.

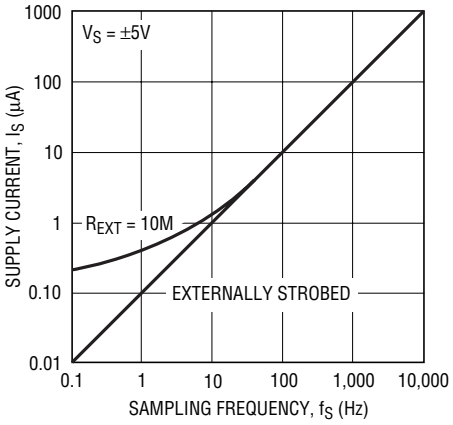
TYPICAL APPLICATION

Window Comparator with Symmetric Window Limits



LTC1040 • TA01

Typical LTC1040 Supply Current vs Sampling Frequency



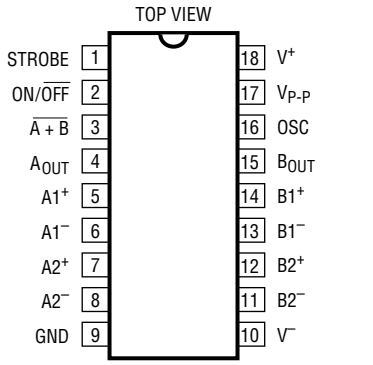
LTC1040 • TA02

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage ..... (V^+ + 0.3V) to (V^- – 0.3V)
Operating Temperature Range
LTC1040C ..... $-40°C \le T_A \le 85°C$
LTC1040M **(OBSOLETE)** ..... –55°C to 125°C
Storage Temperature Range ..... –55°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Output Short-Circuit Duration ..... Continuous

PACKAGE/ORDER INFORMATION



N PACKAGE
18-LEAD PDIP

SW PACKAGE
18-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 120°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (SW)

ORDER PART NUMBER

LTC1040CN
LTC1040CSW

J PACKAGE
18-LEAD CERDIP
T_{JMAX} = 150°C, θ_{JA} = 80°C/W

LTC1040MJ
LTC1040CJ

OBSOLETE PACKAGE
Consider the N18 Package as an Alternate Source

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions: V^+ = 5V, V^- = –5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1040M/LTC1040C MIN	TYP	MAX	UNITS
V_{OS}	Offset Voltage (Note 2)	Split Supplies ±2.8V to ±6V Single Supply (V^- = GND) 2.8V to 6V	●		±0.3	±0.75	mV
		Split Supplies ±6V to ±8V Single Supply (V^- = GND) 6V to 15V	●		±1	±4.5	mV
	Tracking Error Between Input Pairs (Notes 2 and 3)	Split Supplies ±2.8V to ±8V Single Supplies (V^- = GND) 2.8 to 16V	●		0.05	0.1	%
I_{BIAS}	Input Bias Current	OSC = GND			±0.3		nA
R_{IN}	Average Input Resistance	f_S = 1kHz (Note 4)	●	20	30		MΩ
CMR	Common Mode Range		●	V^-		V^+	V
PSR	Power Supply Range	Split Supplies	●	±2.8		±8	V
		Single Supplies (V^- = GND)	●	2.8		16	V
$I_{S(ON)}$	Power Supply ON Current (Note 5)	V^+ = 5V, V_{P-P} On	●		1.2	3	mA
$I_{S(OFF)}$	Power Supply OFF Current (Note 5)	V^+ = 5V, V_{P-P} Off LTC1040C LTC1040M	● ●		0.001 0.001	0.5 5	µA µA
t_D	Response Time (Note 6)			60	80	100	µs
	A, B, $\overline{A + B}$ and ON/$\overline{OFF}$ Outputs (Note 7)						
V_{OH}	Logic "1" Output Voltage	V^+ = 4.75V, I_{OUT} = –360µA	●	2.4	4.4		V
V_{OL}	Logic "0" Output Voltage	V^+ = 4.75V, I_{OUT} = 1.6mA	●		0.25	0.4	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range otherwise specifications are at T_A = 25°C. Test conditions: V^+ = 5V, V^- = –5V, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		LTC1040M/LTC1040C MIN	TYP	MAX	UNITS
	STROBE Input (Note 7)						
V_{IH}	Logic "1" Input Voltage	V^+ = 5.25V	●	2.0	1.6		V
V_{IL}	Logic "0" Input Voltage	V^+ = 4.75V			1.0	0.8	V
R_{EXT}	External Timing Resistor	Resistor Tied Between V^+ and OSC Pin	●	100		10,000	kΩ
f_S	Sampling Frequency	R_{EXT} = 1M, C_{EXT} = 0.1μF			5		Hz

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Applies over input voltage range limit and includes gain uncertainty.

Note 3: Tracking error = $(V_{IN1} – V_{IN2})/ V_{IN1}$.

Note 4: R_{IN} is guaranteed by design and is not tested. $R_{IN} = 1/(f_S \bullet 33pF)$.

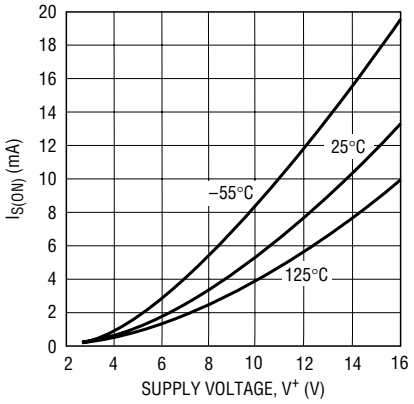
Note 5: Average supply current = $t_D \bullet I_{S(ON)} \bullet f_S + (1 – t_D \times f_S) \bullet I_{S(OFF)}$.

Note 6: Response time is set by an internal oscillator and is independent of overdrive voltage.

Note 7: Inputs and outputs also capable of meeting EIA/JEDEC B series CMOS specifications.

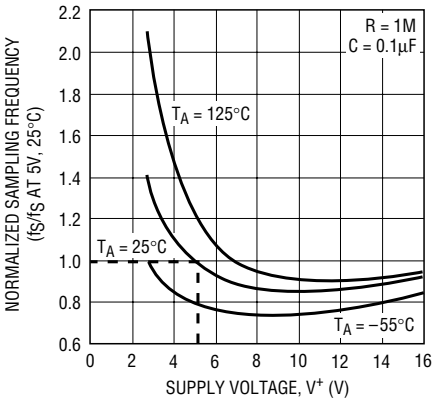
TYPICAL PERFORMANCE CHARACTERISTICS

Peak Supply Current vs Supply Voltage



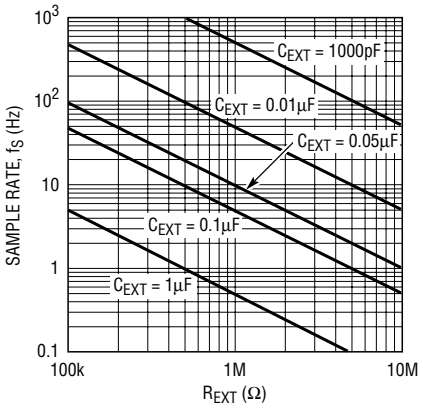
LTC1040 • TPC01

Normalized Sampling Frequency vs Supply Voltage and Temperature



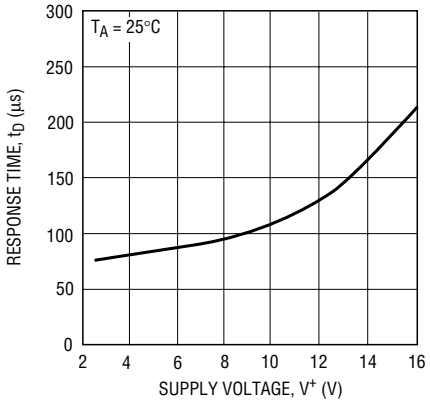
LTC1040 • TPC02

Sampling Rate vs R_{EXT}, C_{EXT}



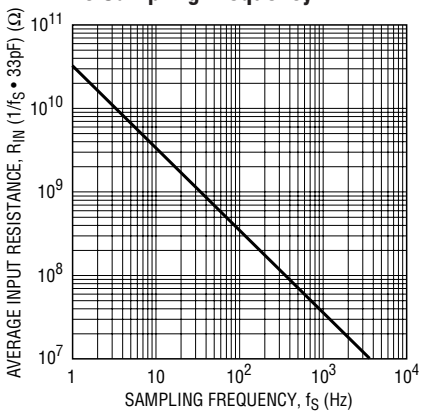
LT1040 • TPC03

Response Time vs Supply Voltage



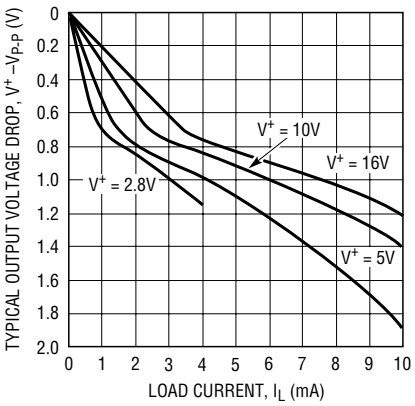
LTL1040 • TPC04

Input Resistance vs Sampling Frequency



LTC1040 • TPC05

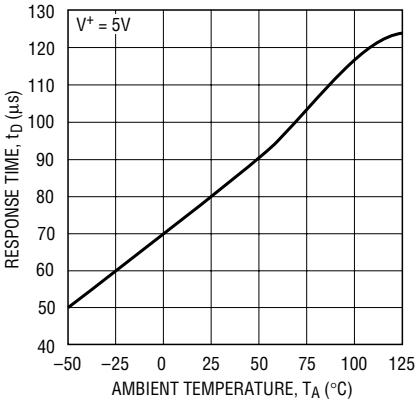
V_{P-P} Output Voltage vs Load Current



LTC1040 • TPC06

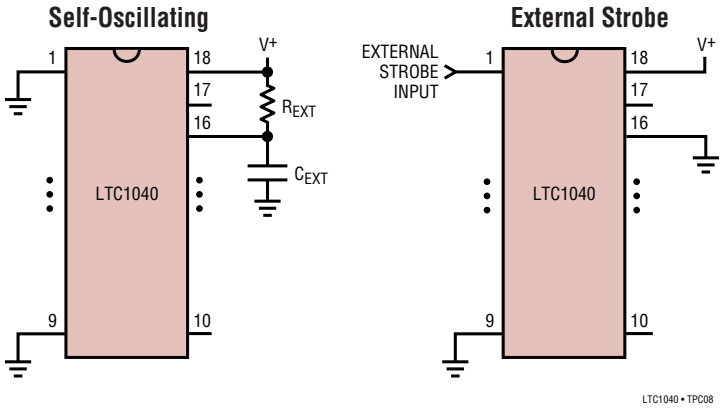
TYPICAL PERFORMANCE CHARACTERISTICS

Response Time vs Temperature



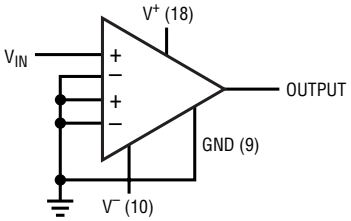
LTC1040 • TPC07

Quick Hookup Guide



LTC1040 • TPC08

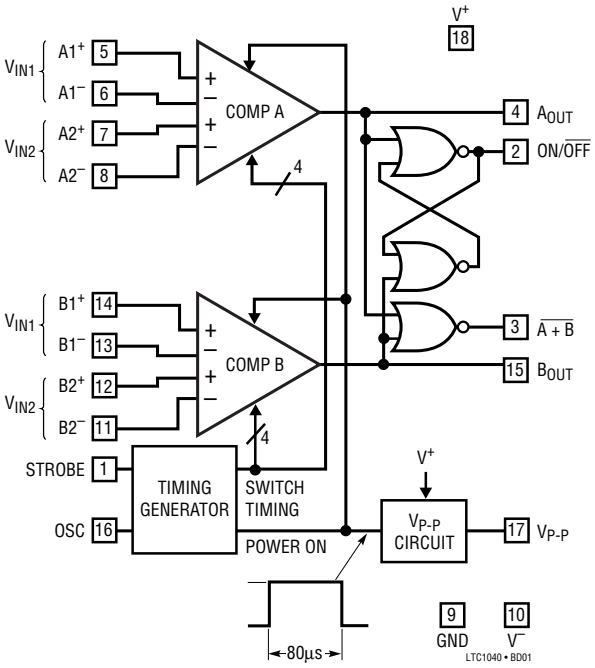
TEST CIRCUIT



ALL INPUTS ON OPPOSITE COMPARATOR AT GROUND

LTC1040 • TA01

BLOCK DIAGRAM



LTC1040 • BD01

APPLICATIONS INFORMATION

The LTC1040 uses sampled data techniques to achieve its unique characteristics. Some of the experience acquired using classic linear comparators does not apply to this circuit, so a brief description of internal operation is essential to proper application.

The most obvious difference between the LTC1040 and other comparators is the dual differential input structure. Functionally, when the sum of inputs is positive, the comparator output is high and when the sum of the inputs is negative, the output is low. This unique input structure is achieved with CMOS switches and a precision capacitor array. Because of the switching nature of the inputs, the concept of input current and input impedance needs to be examined.

The equivalent input circuit is shown in Figure 1. Here, the input is being driven by a resistive source, R_S, with a bypass capacitor, C_S. The bypass capacitor may or may not be needed, depending on the size of the source resistance and the magnitude of the input voltage, V_{IN}.

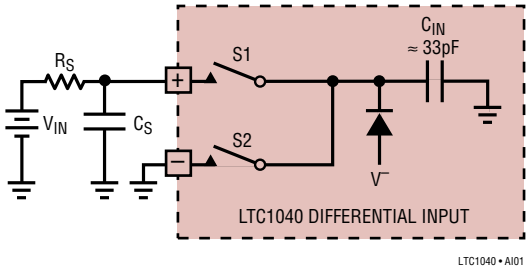


Figure 1. Equivalent Input Circuit

For R_S < 10k

Assuming C_S is zero, the input capacitor, C_{IN}, charges to V_{IN} with a time constant of $R_S\,C_{IN}$. When R_S is too large, C_{IN} does not have a chance to fully charge during the sampling interval (≈ 80µs) and errors will result. If R_S exceeds 10kΩ, a bypass capacitor is necessary to minimize errors.

For R_S > 10kΩ

For R_S greater than 10kΩ, C_{IN} cannot fully charge and a bypass capacitor, C_S, is needed. When switch S1 closes, charge is shared between C_S and C_{IN}. The change in voltage on C_S because of this charge sharing is:

$$\Delta V = V_{IN} \bullet \frac{C_{IN}}{C_{IN} + C_S}$$

This represents an error and can be made arbitrarily small by increasing C_S.

With the addition of C_S, a second error term caused by the finite input resistance of the LTC1040 must be considered. Switches S1 and S2 alternately open and close, charging and discharging C_{IN} between V_{IN} and ground. The alternate charge and discharge of C_{IN} causes a current to flow into the positive input and out of the negative input. The magnitude of this current is:

$$I_{IN} = q \bullet f_S = V_{IN}\,C_{IN}\,f_S$$

where f_S is the sampling frequency. Because the input current is directly proportional to input voltage, the LTC1040 can be said to have an average input resistance of:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{1}{f_S\,C_{IN}} = \frac{1}{f_S \bullet 33pF}$$

(see typical curve of Input Resistance vs Sampling Frequency). A voltage divider is set up between R_S and R_{IN} causing error.

The input voltage error caused by these two effects is:

$$V_{ERROR} = V_{IN}\left(\frac{C_{IN}}{C_{IN} + C_S} + \frac{R_S}{R_S + R_{IN}}\right)$$

Example: f_S = 10Hz, R_S = 1MΩ,
C_S = 1µF, V_{IN} = 1V

$$V_{ERROR} = 1V\left(\frac{33 \bullet 10^{-12}}{1 \bullet 10^{-6}} + \frac{10^6}{10^6 + 3 \bullet 10^9}\right)$$

$$= 33\mu V + 330\mu V = 363\mu V.$$

Notice that most of the error is caused by R_{IN}. If the sampling frequency is reduced to 1Hz, the voltage error is reduced to 66µV.

APPLICATIONS INFORMATION

Minimizing Comparison Errors

The two differential input voltages, V1 and V2, are converted to charge by the input capacitors C_{IN1} and C_{IN2} (see Figure 2). The charge is summed at the virtual ground point; if the net charge is positive, the comparator output is high and if negative, it is low. There is an optimum way to connect these inputs, in a specific application, to minimize error.

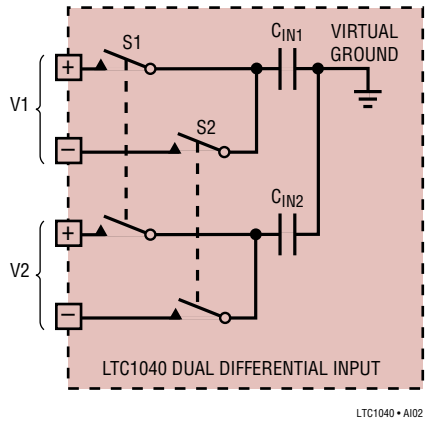


Figure 2. Dual Differential Equivalent Input Circuit

Ignoring internal offset, the LTC1040 will be at its switching point when:

$$V1 \bullet C_{IN1} + V2 \bullet C_{IN2} = 0.$$

Optimum error will be achieved when the differential voltages, V1 and V2, are individually minimized. Figure 3 shows two ways to connect the LTC1040 to compare an input voltage, V_{IN}, to a reference voltage, V_{REF}. Using the above equation, each method will be at null when:

(a) $(V_{REF} - 0V)\ C_{IN1} - (0V - V_{IN})\ C_{IN2} = 0$
or $V_{IN} = V_{REF}\ (C_{IN1}/C_{IN2})$

(b) $(V_{REF} - V_{IN})\ C_{IN1} - (0V - 0V)\ C_{IN2} = 0$
or $V_{IN} = V_{REF}$.

Notice that in method (a) the null point depends on the ratio of C_{IN1}/C_{IN2}, but method (b) is independent of this ratio. Also, because method (b) has zero differential input voltage, the errors due to finite input resistance are negligible. The LTC1040 has a high accuracy capacitor array and even the non-optimum connection will only result in ±0.1% more error, worst-case compared to the optimum connection.

Tracking Error

Tracking error is caused by the ratio error between C_{IN1} and C_{IN2} and is expressed as a percentage. For example, consider Figure 3a with V_{REF} = 1V. Then at null,

$$V_{IN} = V_{REF}\ \frac{C_{IN1}}{C_{IN2}} = 1V \pm 1mV$$

because C_{IN1} is guaranteed to equal C_{IN2} to within 0.1%.

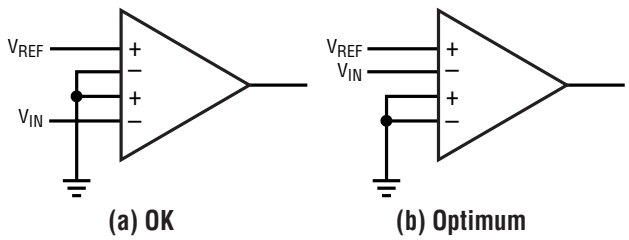


Figure 3. Two Ways to Do It

Common Mode Range

The input switches of the LTC1040 are capable of switching to either the V^+ or V^- supply. This means that the input common mode range includes both supply rails. Many applications, not feasible with conventional comparators, are possible with the LTC1040. In the load current detector shown in Figure 4, a 0.1Ω resistor is used to sense the current in the V^+ supply. This application requires the dual differential input and common mode capabilities of the LTC1040.

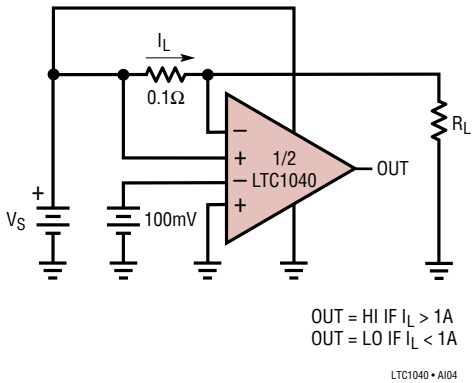


Figure 4. Load Current Detector

APPLICATIONS INFORMATION

Offset Voltage Error

The errors due to offset, common mode, power supply variation, gain and temperature are all included in the offset voltage specification. This makes it easy to compute the error when using the LTC1040.

Example: error computation for Figure 4.
Assume: $2.8V \le V_S \le 6V$.

Then total worst-case error is:

$$I_{L\,(ERROR)} = \pm(100mV \bullet \underset{\substack{\uparrow \\ \text{Tracking Error}}}{0.001} + \underset{\substack{\uparrow \\ V_{OS}}}{0.5mV}) \bullet \frac{1A}{100mV} = \pm 6mA$$

$$I_{L\,(ERROR)}\% = \frac{6mA}{1A} \bullet 100 = \pm 0.6\%.$$

Note: If source resistance exceeds 10k, bypass capacitors should be used and the associated errors must be included.

Pulsed Power (V_{P-P}) Output

It is often desirable to use comparators with resistive networks such as bridges. Because of the extremely low power consumption of the LTC1040, the power consumed by these resistive networks can far exceed that of the device itself.

At low sample rates the LTC1040 spends most of its time off. To take advantage of this, a pulsed power (V_{P-P}) output is provided. V_{P-P} is switched to V^+ when the comparator is on and to a high impedance (open circuit) when the comparator is off. The ON time is nominally 80µs. Figure 5 shows the V_{P-P} output circuit.

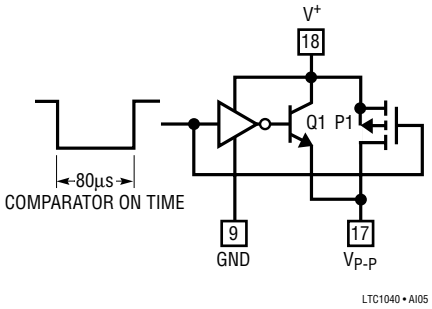


Figure 5. V_{P-P} Output Switch

The V_{P-P} output voltage is not precise (see V_{P-P} Output Voltage versus Load Current curve). There are two ways V_{P-P} can be used to power external networks without excessive errors: (1) ratiometric networks and (2) fast settling references.

In a ratiometric network, the inputs are all proportional to V_{P-P} (see Figure 6). Consequently, for small changes, the absolute value of V_{P-P} does not affect accuracy.

It is critical that the inputs to the LTC1040 completely settle within 4µs of the start of the comparison cycle and that they do not change during the 80µs ON time. When driving resistive networks with V_{P-P}, capacitive loading on

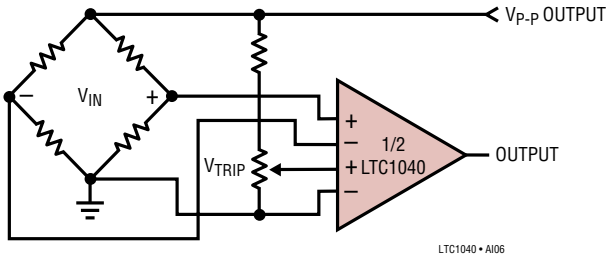


Figure 6. Ratiometric Network Driven by V_{P-P}

the network should be minimized to meet the 4µs settling time requirement. It is not recommended that V_{P-P} be used to drive networks with source impedances, as seen by the inputs, of greater than 10kΩ.

In applications where an absolute reference is required, the V_{P-P} output can be used to drive a fast settling reference. The LT1009 2.5V reference, ideal in this application, settles in approximately 2µs (see Figure 7). The current through R1 must be large enough to supply the LT1009 minimum bias current (≈1mA) and the load current, I_L.

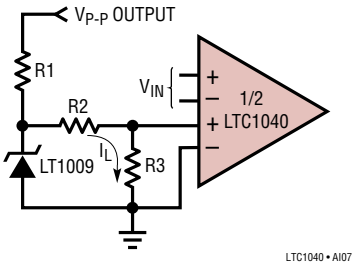


Figure 7. Driving Reference with V_{P-P} Output

APPLICATIONS INFORMATION

Output Logic

In addition to the normal outputs (A_{OUT} and B_{OUT}), two additional outputs, $\overline{A + B}$ and ON/$\overline{OFF}$, are provided (see Figure 8 and Table 1). All logic is powered from V^+ and ground, thus input and output logic levels are independent of the V^- supply. The LTC1040 is directly compatible with CMOS logic and is TTL compatible for $4.75V \leq V^+ \leq 5.25V$. No external pull-up resistors are required.

Table 1. Output Logic Truth Table

ΣA INPUTS	ΣB INPUTS	A_{OUT}	B_{OUT}	$\overline{A + B}$	ON/$\overline{OFF}$
+	+	H	H	L	L
+	–	H	L	L	L
–	+	L	H	L	H
–	–	L	L	H	I*

*I = indeterminate. When both A and B outputs are low, the ON/$\overline{OFF}$ output remains in the state it was in prior to entering $A_{OUT} = B_{OUT} = L$.

Using External Strobe

A positive pulse on the strobe input, with the OSC input tied to ground, will initiate a comparison cycle. The STROBE input is edge-sensitive and pulse widths of 50ns will typically trigger the device.

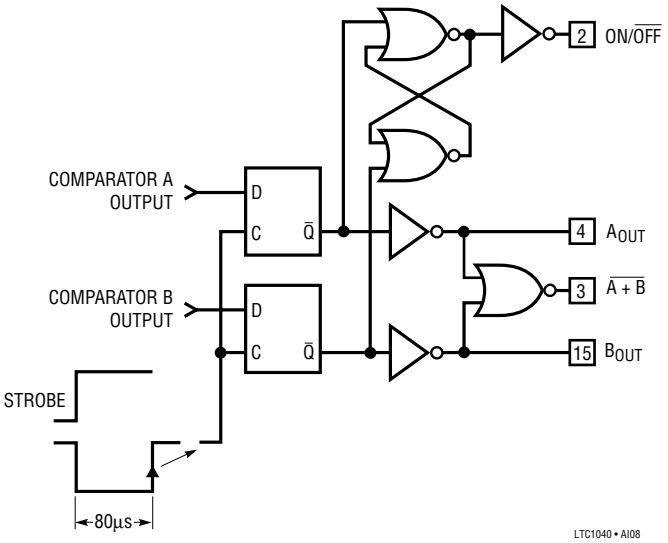


Figure 8. LTC1040 Logic Diagram

Because of the sampling nature of the LTC1040, some sensitivity exists between the offset voltage and the falling edge of the input strobe. When the falling edge of the strobe signal falls within the comparator's active time (80µs after rising edge), offset changes of as much as 2mV can occur. To eliminate this problem, make sure the strobe pulse width is greater than the response time, t_D.

Using Internal Strobe

An internal oscillator allows the LTC1040 to strobe itself. The frequency of oscillation, and hence sampling rate, is set by an external RC network (see typical curve of Sampling Rate vs R_{EXT}, C_{EXT}).

For self-oscillation, the STROBE pin must be tied to ground. The external RC network is connected as shown in Figure 9.

To assure oscillation, R_{EXT} must be between 100k and 10M. There is no limit to the size of C_{EXT}.

R_{EXT} is very important in determining the power consumption. The average voltage at the oscillator pin is approximately $V^+/2$. The power consumed by R_{EXT} is then: $P_{REXT} = (V^+/2)^2/R_{EXT}$.

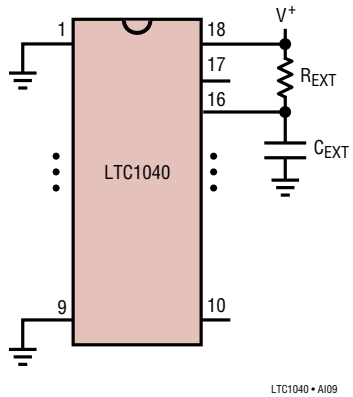


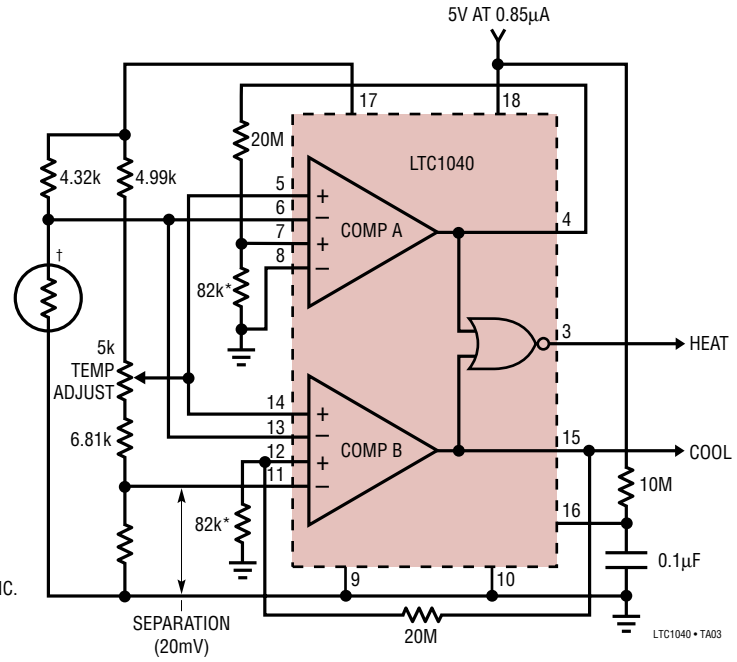
Figure 9. External RC Connection

Example: R_{EXT} = 1M, V^+ 5V, $P_{REXT} = (2.5)^2/10^6 = 6.25 \cdot 10^{-6}W$.

This is about four times the power consumed by the LTC1040 at $V^+ = 5V$ and f_S = 1 sample/second. Where power is a premium R_{EXT} should be made as large as possible. Note that the power consumed by R_{EXT} is *not* a function of f_S or C_{EXT}.

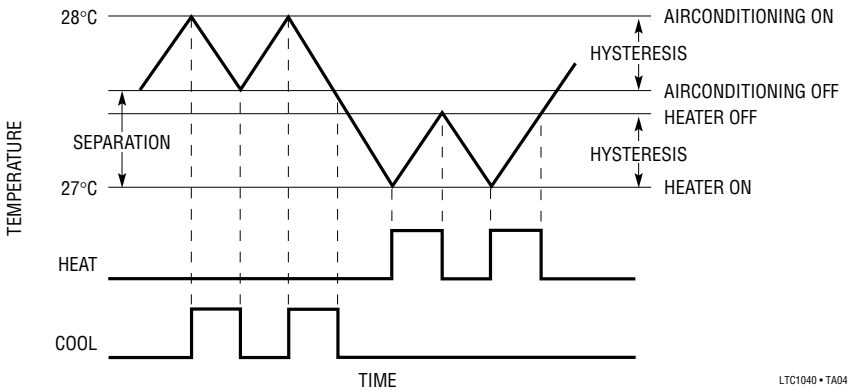
TYPICAL APPLICATIONS

Complete Heating/Cooling Automatic Thermostat

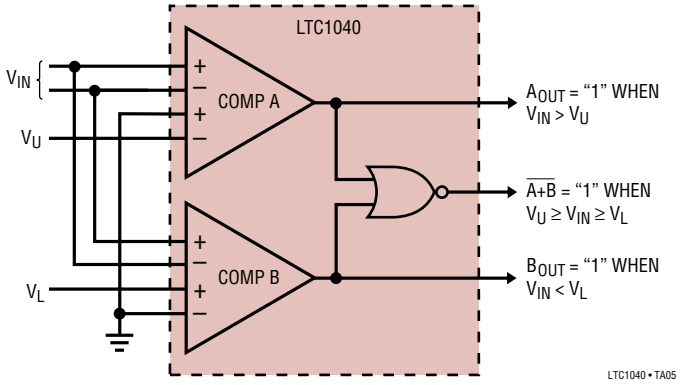


† THERMISTOR # 44007
YELLOW SPRINGS INSTRUMENT CO., INC.

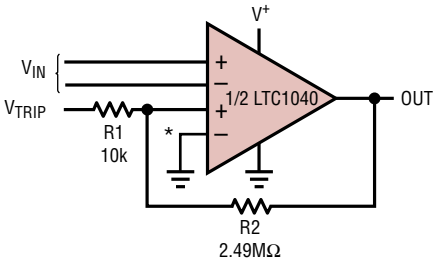
* HYSTERESIS = 5V • $\frac{82k}{20M}$ = 20mV



Window Comparator with Independent Window Limits and Fully Floating Differential Input



Hysteresis Comparator with Fully Floating Differential Input



OUT = "0" WHEN $V_{IN} > V_U = \frac{V_{TRIP}\,R2 + (5V)\,R1}{R1 + R2} = 0.996\,V_{TRIP} + 20mV$

OUT = "1" WHEN $V_{IN} < V1 = \frac{V_{TRIP}\,R2}{R1 + R2} = 0.996V_{TRIP}$

* TO CENTER HYSTERESIS ABOUT V_{TRIP}, FORCE THIS INPUT TO HYSTERESIS/2 (10mV)

LTC1040 • TA06

TYPICAL APPLICATIONS

The LTC1040 as a Linear Amplifier

With a simple RC filter, the LTC1040 can be made to function as a linear amplifier. By filtering the logic output and feeding it back to the negative input, the loop forces the output duty cycle $[t_{ON}/(t_{ON} + t_{OFF})]$ so that V_{OUT} equals V_{IN} (Figure 10).

The RC time constant is set to keep the ripple on the output small. The maximum output ripple is: $\Delta V = V^+/f_S RC$ and should be set to 0.5mV to 1mV for best results. Notice that the higher the sampling frequency, f_S, the lower RC can be. This is important because the RC filter also sets the loop response. A convenient way to keep f_S as high as possible under all conditions is to connect a 100k resistor to pin 16 (OSC) with no capacitance to ground.

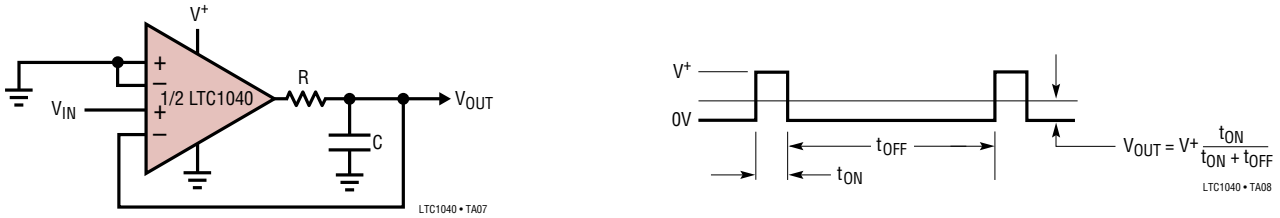
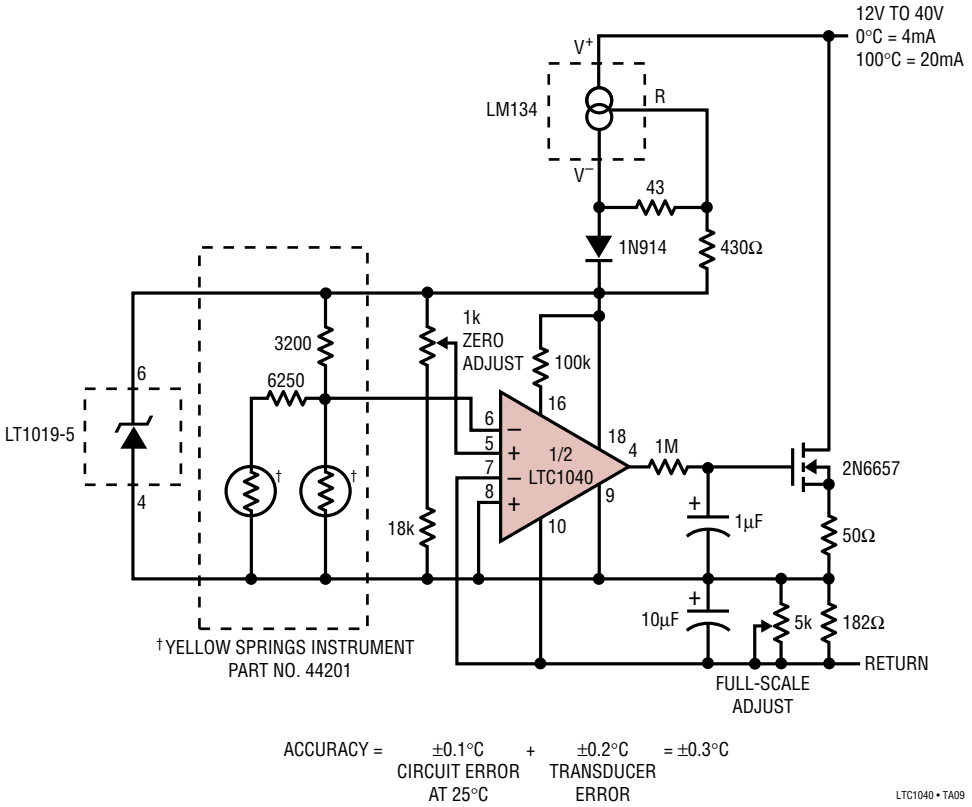


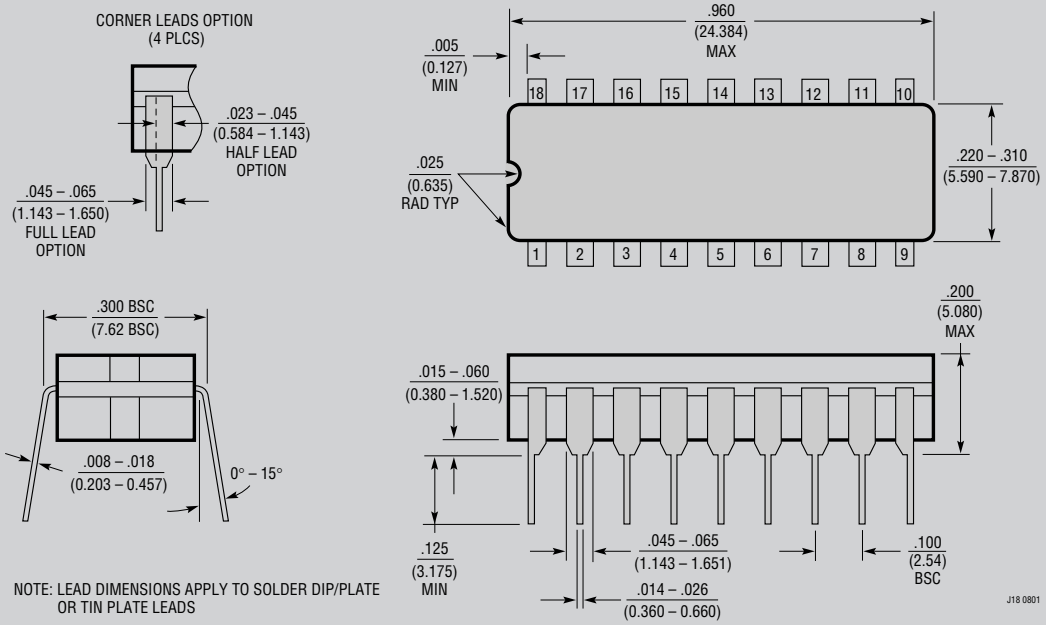
Figure 10. The LTC1040 as a Linear Amplifier

2-Wire 0°C to 100°C Temperature Transducer with 4mA to 20mA Output



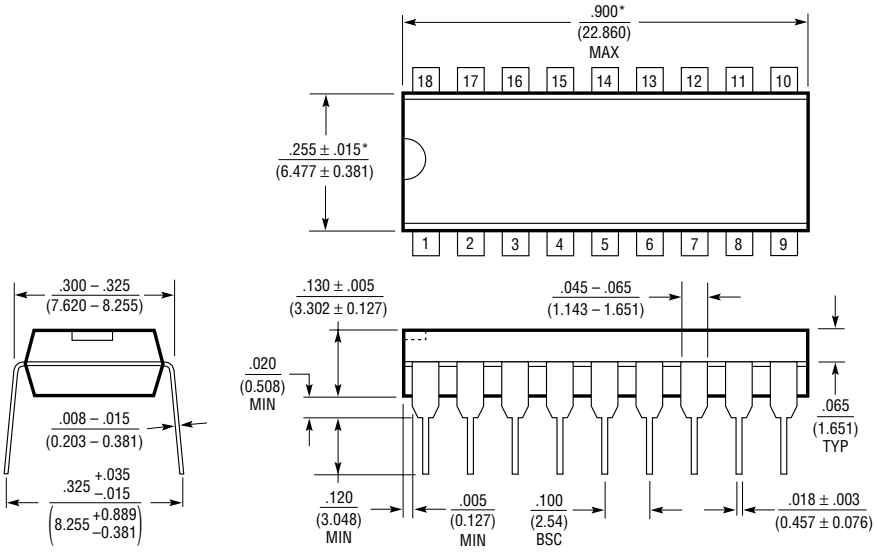
PACKAGE DESCRIPTION

J Package
18-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



OBSOLETE PACKAGE

N Package
18-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

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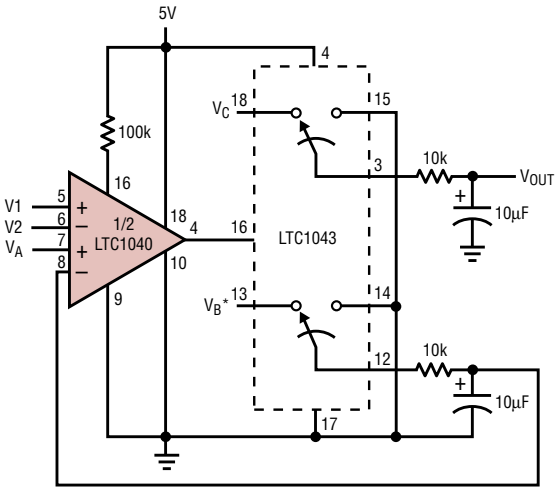
TYPICAL APPLICATIONS

Analog Multiplier/Divider

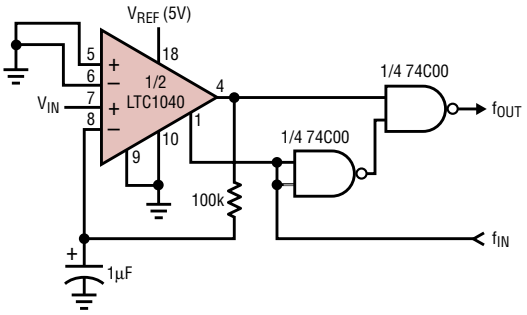


$$V_{OUT} = \frac{(V_A + V1 - V2) \bullet V_C}{V_B}$$

ACCURACY = ±10mV NO TRIM
*V_B MUST BE > V_A + (V1 – V2)

LTC1040 • TA10

Single + 5V Voltage-to-Frequency Converter

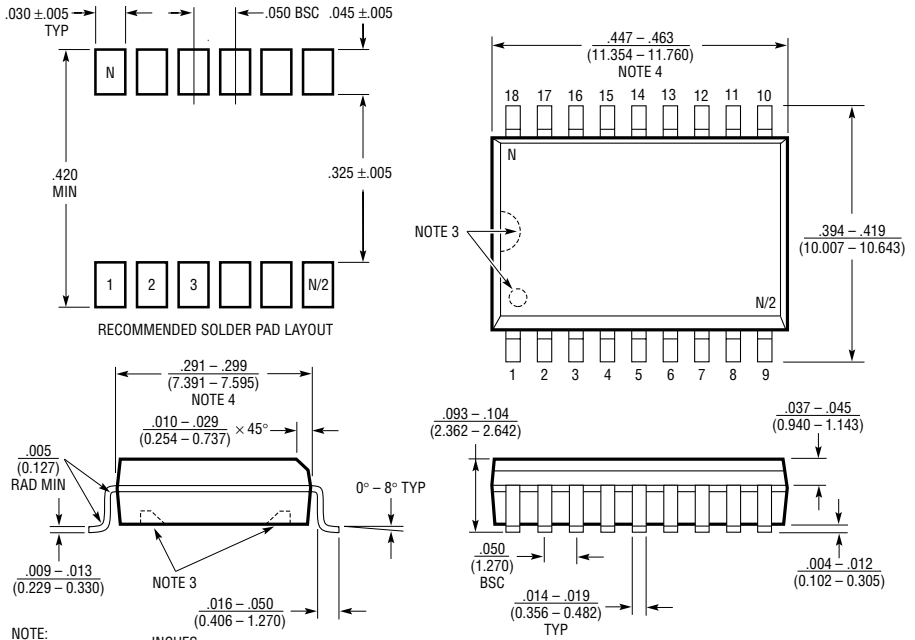


$$f_{OUT}\ (AVERAGE) = f_{IN}\ \frac{V_{IN}}{V_{REF}}\ \pm 0.1\%\ FS$$

LTC1040 • TA11

PACKAGE DESCRIPTION

SW Package
18-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

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