



**THE DATASHEET OF  
LT4254IGN#TRPBF**





## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage ( $V_{CC}$ ) .....	-0.3 to 44V
SENSE, PWRGD .....	-0.3 to 44V
GATE .....	-0.3 to 50V
FB, UV, OPEN .....	-0.3 to 44V
OV .....	-0.3 to 18V
RETRY .....	-0.3 to 15V
TIMER .....	-0.3V to 4.3V
Maximum Input Current (TIMER) .....	100 $\mu$ A
Operating Temperature	
LT4254C .....	0°C to 70°C
LT4254I .....	-40°C to 85°C
Storage Temperature Range .....	-65°C to 150°C
Lead Temperature (Soldering, 10 sec) .....	300°C

## PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LT4254CGN LT4254IGN
	GN PART MARKING
	4254 4254I
<b>Order Options</b> Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF Lead Free Part Marking: <a href="http://www.linear.com/leadfree/">http://www.linear.com/leadfree/</a>	

Consult LTC Marketing for parts specified with wider operating temperature ranges.  
**Note:** NC = No Connect

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 24\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{CC}$	Operating Voltage		● 10.8		36	V	
$I_{CC}$	Operating Current			1.9	3	mA	
$UV_{LH}$	Undervoltage Threshold	$V_{CC}$ Low-to-High Transition	● 3.96	4	4.04	V	
$V_{UVHYS}$	Hysteresis		0.25	0.4	0.55	V	
$I_{INUV}$	UV Input Current	UV = 4.5V UV = 0V		-0.1 -1.5	-1 -3	$\mu$ A $\mu$ A	
$OV_{VHL}$	Overvoltage Threshold	$V_{CC}$ Low-to-High Transition	● 3.96	4	4.04	V	
$OV_{VHYS}$	Hysteresis		0.25	0.4	0.55	V	
$I_{INO}$	OV Input Current	$0\text{V} \leq OV < 6.5\text{V}$		0.1	1	$\mu$ A	
$V_{OPEN}$	Open-Circuit Voltage Threshold ( $V_{CC} - V_{SENSE}$ )		● 2	3.5	5	mV	
$V_{OLOPEN}$	OPEN Output Low Voltage	$I_O = 2\text{mA}$ $I_O = 5\text{mA}$		0.20 0.75	0.5 1.3	V V	
$I_{INOPEN}$	Leakage Current	$V_{OPEN} = 5\text{V}$		0.1	1	$\mu$ A	
$V_{SENSETRIP}$	SENSE Pin Trip Voltage ( $V_{CC} - V_{SENSE}$ )	FB = 0V FB $\geq 2\text{V}$	● 5.5 ● 40	12 50	25 60	mV mV	
$I_{INSNS}$	SENSE Pin Input Current			40	70	$\mu$ A	
$I_{PU}$	GATE Pull-Up Current	Charge Pump On, $\Delta V_{GATE} = 7\text{V}$	● -15	-35	-63	$\mu$ A	
$I_{PD}$	GATE Pull-Down Current	Any Fault, $V_{GATE} = 3\text{V}$		40	60	80	mA
$\Delta V_{GATE}$	External N-Channel Gate Drive (Note 2)	$V_{GATE} - V_{CC}$ , $12\text{V} \leq V_{CC} \leq 20\text{V}$ $20\text{V} \leq V_{CC} \leq 36\text{V}$	● 4.5 ● 10	8.8 11	12.5 12.5	V V	
$V_{FB}$	FB Voltage Threshold	FB High-to-Low Transition FB Low-to-High Transition	● 3.96 ● 4.20	4 4.45	4.04 4.65	V V	
$V_{FBHYS}$	FB Hysteresis Voltage		0.3	0.45	0.60	V	
$V_{OLPGD}$	PWRGD Output Low Voltage	$I_O = 1.6\text{mA}$ $I_O = 5\text{mA}$		0.25 0.63	0.4 1.0	V V	

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 24\text{V}$  unless otherwise noted.

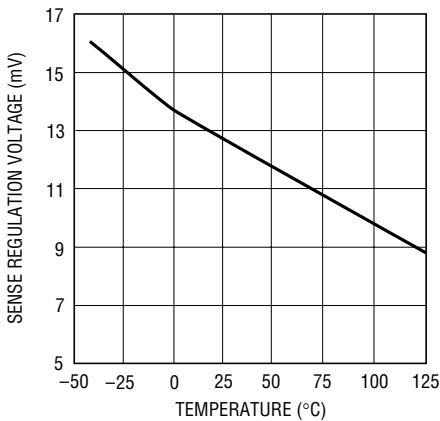
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{PWRGD}$	PWRGD Pin Leakage Current	$V_{PWRGD} = 36\text{V}$		0.1	10	$\mu\text{A}$
$I_{INFB}$	FB Input Current	$\text{FB} = 4.5\text{V}$	-1	-0.1		$\mu\text{A}$
$I_{TIMERPU}$	TIMER Pull-Up Current		● -60	-120	-180	$\mu\text{A}$
$I_{TIMERPD}$	TIMER Pull-Down Current		● 1	3	5	$\mu\text{A}$
$V_{THTIMER}$	TIMER Shut-Down Threshold Voltage	$C_{TIMER} = 10\text{nF}$	● 4.3	4.65	5	V
$D_{TIMER}$	Duty Cycle (RETRY Mode)		● 1.5	3	4.5	%
$V_{RETRY(TH)}$	RETRY Threshold		● 0.4	0.8	1.2	V
$I_{INRTR}$	RETRY Input Current	$\text{RETRY} = \text{GND}$	-120	-85	-40	$\mu\text{A}$
$t_{PHLUV}$	UV Low to GATE Low	$C_{GATE} = 100\text{pF}$		1.7		$\mu\text{s}$
$t_{PLHUV}$	UV High to GATE High	$C_{GATE} = 100\text{pF}$		6		$\mu\text{s}$
$t_{PHLFB}$	FB Low to PWRGD Low			0.8		$\mu\text{s}$
$t_{PLHFB}$	FB High to PWRGD High			3.2		$\mu\text{s}$
$t_{PHLSENSE}$	$(V_{CC} - V_{SENSE})$ High to GATE Low	$V_{CC} - V_{SENSE} = 275\text{mV}$		2.5	4	$\mu\text{s}$

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** An internal clamp limits the GATE pin to a maximum of 11V above  $V_{CC}$  (under normal operating conditions). Driving this pin to a voltage beyond the clamp voltage may damage the part.

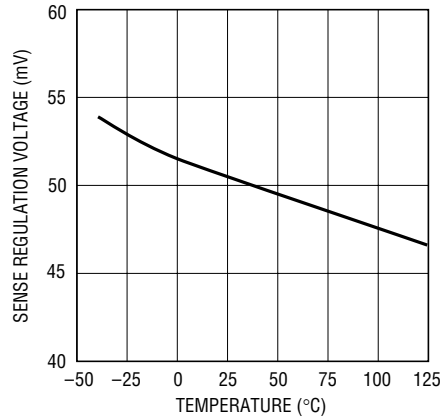
**TYPICAL PERFORMANCE CHARACTERISTICS**

**SENSE Pin Regulation Voltage vs Temperature,  $\text{FB} = 0\text{V}$**



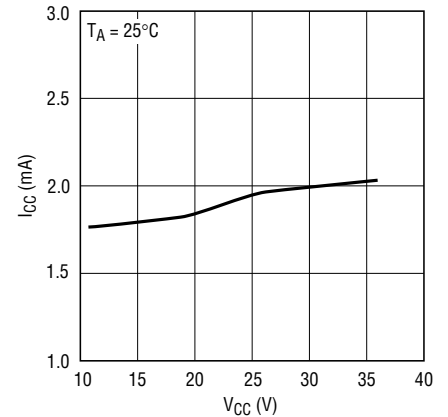
4254 G01

**SENSE Pin Regulation Voltage vs Temperature,  $\text{FB} > 2\text{V}$**



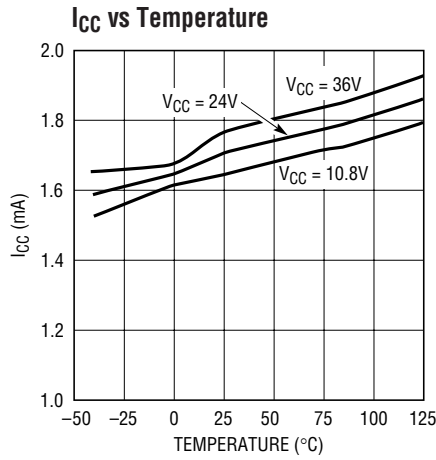
4254 G02

**$I_{CC}$  vs  $V_{CC}$**

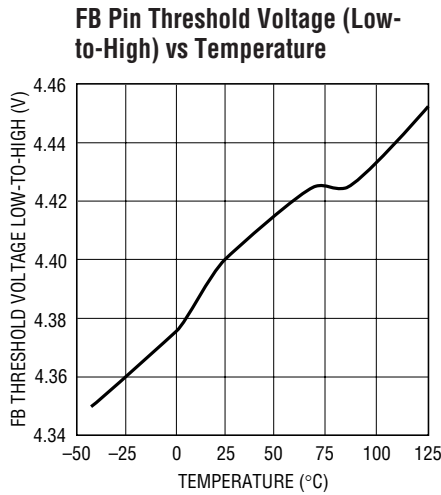


4254 G03

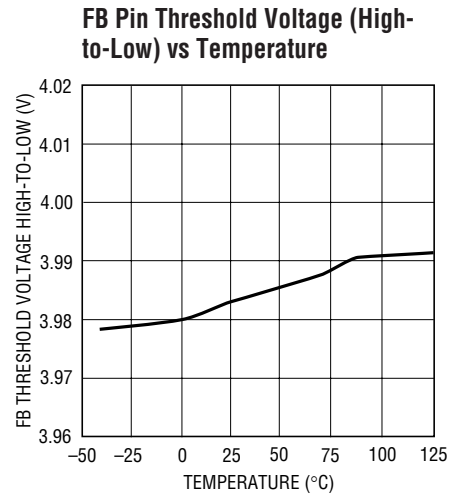
# TYPICAL PERFORMANCE CHARACTERISTICS



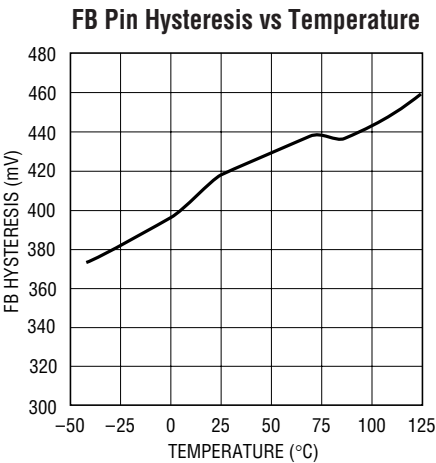
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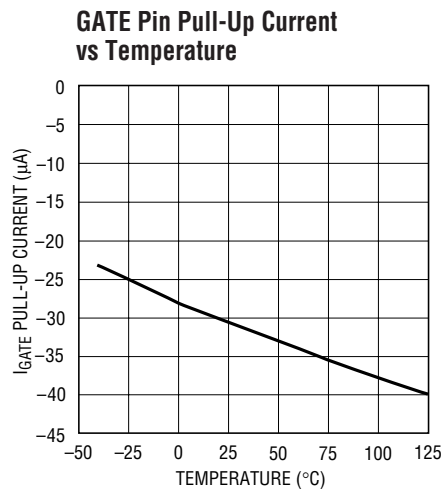
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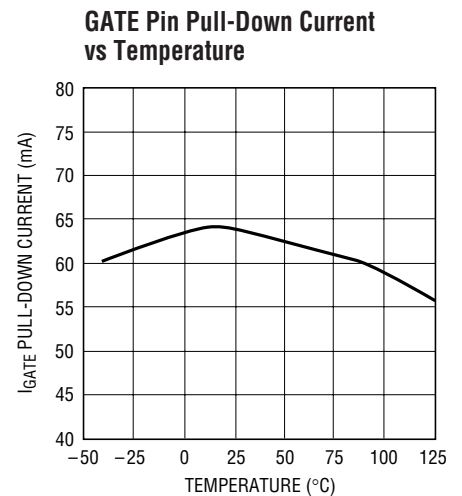
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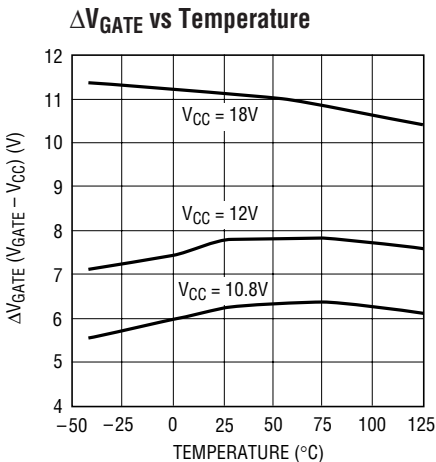
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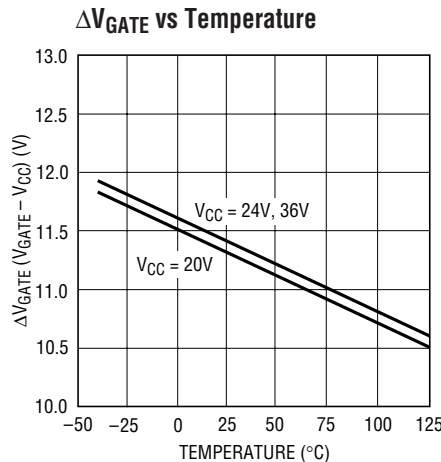
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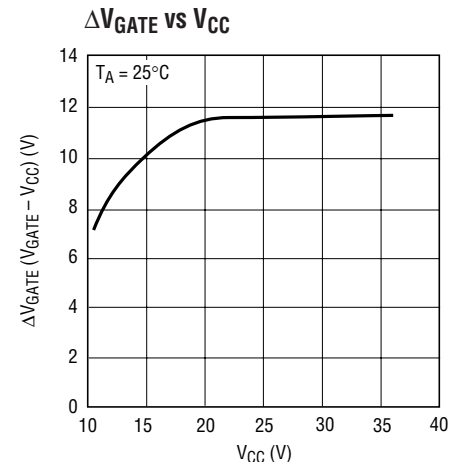
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4254 G10



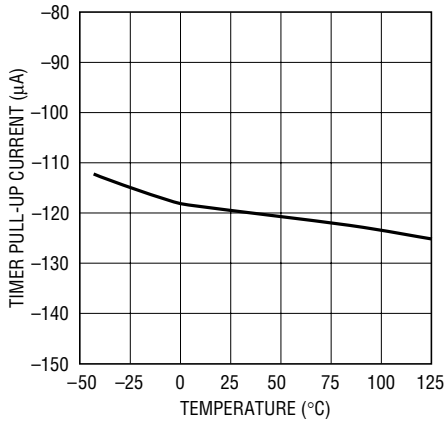
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4254 G12

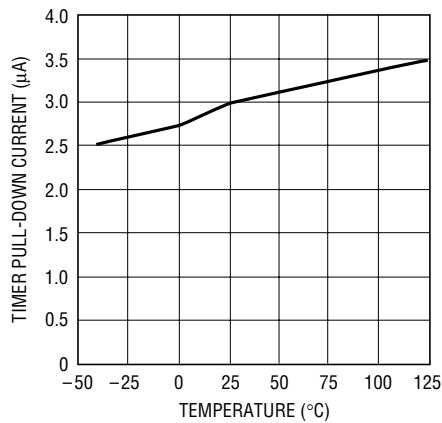
# TYPICAL PERFORMANCE CHARACTERISTICS

**TIMER Pin Pull-Up Current vs Temperature**



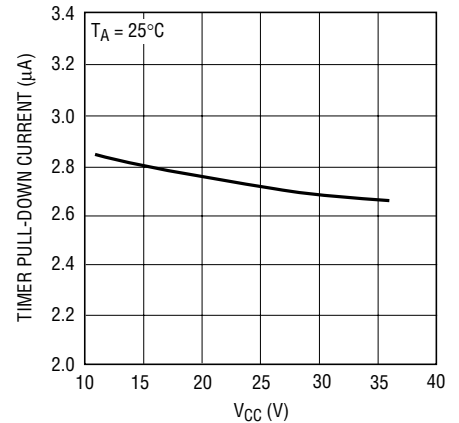
4254 G13

**TIMER Pin Pull-Down Current vs Temperature**



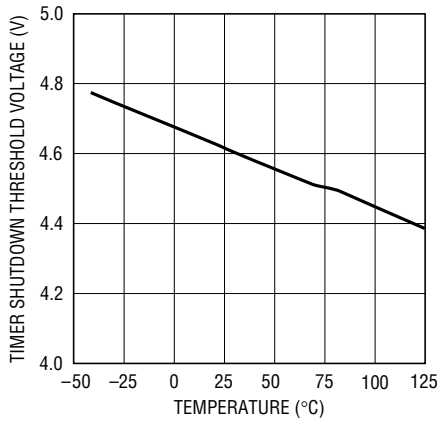
4254 G14

**TIMER Pin Pull-Down Current vs V<sub>CC</sub>**



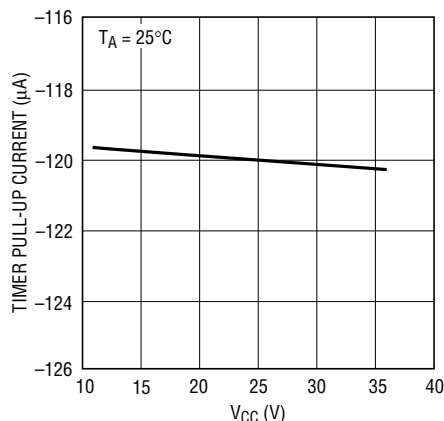
4254 G15

**TIMER Shutdown Threshold vs Temperature**



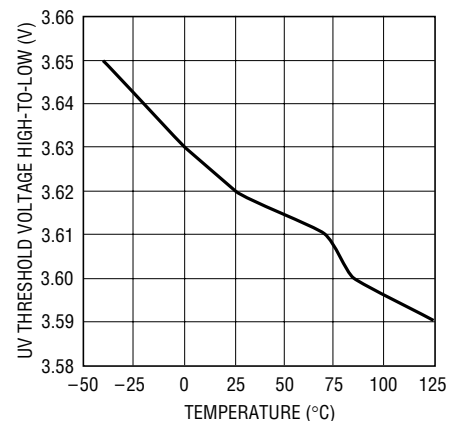
4254 G16

**TIMER Pin Pull-Up Current vs V<sub>CC</sub>**



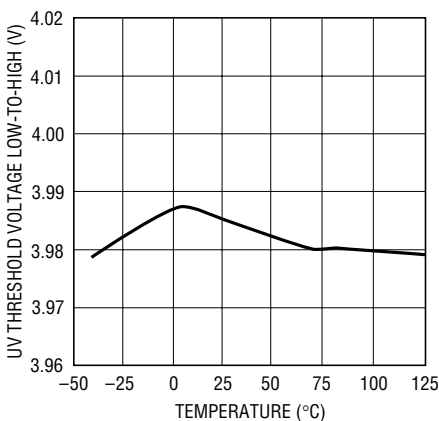
4254 G17

**UV Threshold Voltage (High-to-Low) vs Temperature**



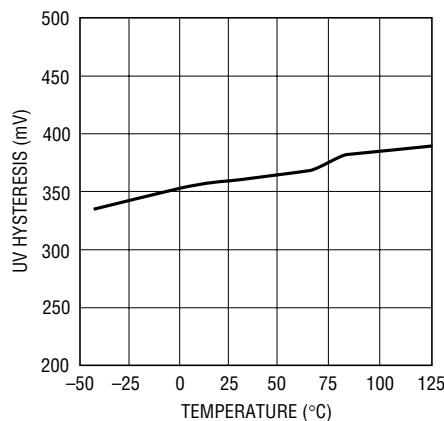
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**UV Threshold Voltage (Low-to-High) vs Temperature**



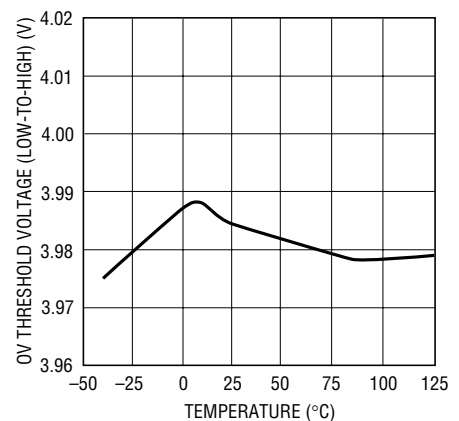
4254 G19

**UV Hysteresis vs Temperature**



4254 G20

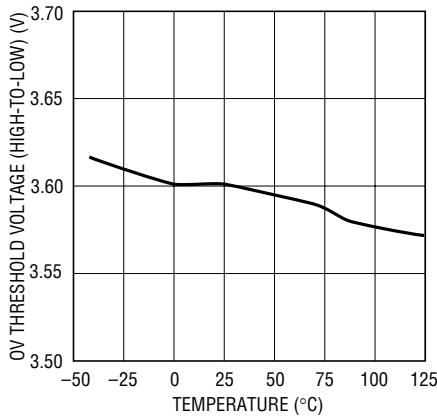
**OV Threshold Voltage (Low-to-High) vs Temperature**



4257 G21

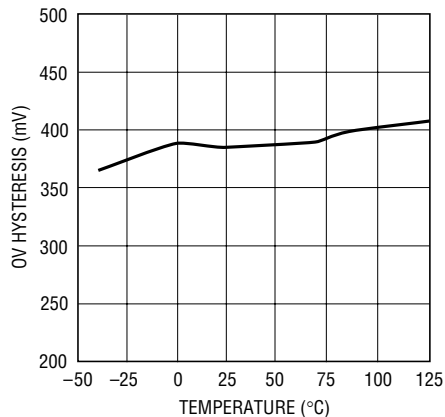
## TYPICAL PERFORMANCE CHARACTERISTICS

**OV Threshold Voltage (High-to-Low) vs Temperature**



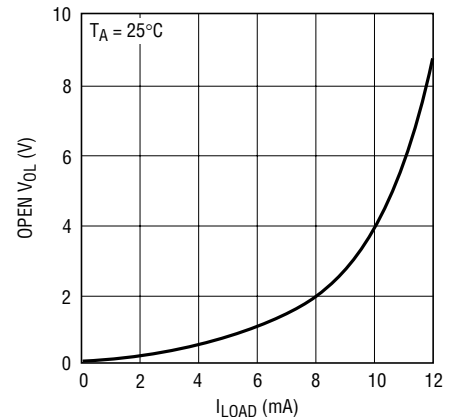
4254 G22

**OV Hysteresis vs Temperature**



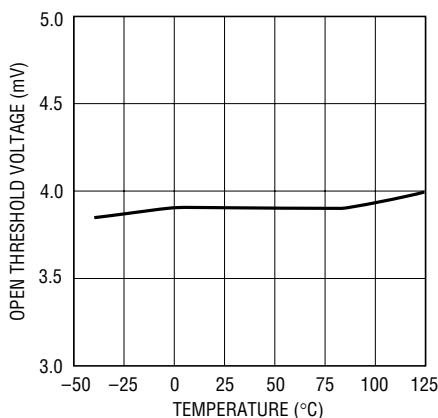
4254 G23

**OPEN Output Voltage vs I<sub>LOAD</sub>**



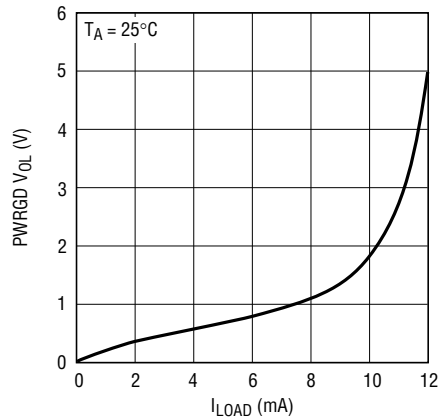
4254 G24

**OPEN Pin Threshold Voltage vs Temperature**



4254 G25

**PWRGD Output Voltage vs I<sub>LOAD</sub>**



4254 G26

## PIN FUNCTIONS

**V<sub>CC</sub>**: Input Supply Voltage. The positive supply input ranges from 10.8V to 36V for normal operation. I<sub>CC</sub> is typically 1.9mA. An internal circuit disables the LT4254 for inputs less than 9.8V (typ).

**GND**: Device Ground. This pin must be tied to a ground plane for best performance.

**FB**: Power Good Comparator Input. FB monitors the output voltage through an external resistive divider. When the voltage on the FB pin is lower than the high-to-low threshold of 4V, the PWRGD pin is pulled low and released

when the FB pin is pulled above the 4.45V low-to-high threshold.

The FB pin also affects foldback current limit (see Figure 7 and related discussion). To disable PWRGD monitoring, connect FB to the output voltage and float the PWRGD pin.

**TIMER**: Timing Input. An external timing capacitor from TIMER to GND programs the maximum time the part is allowed to remain in current limit. When the part goes into current limit, a 120μA pull-up current starts to charge the timing capacitor. When the voltage on the TIMER pin

## PIN FUNCTIONS

reaches 4.65V (typ), the GATE pin is pulled low; the TIMER pull-up current will be turned off and the capacitor is discharged by a 3 $\mu$ A pull-down current. When the TIMER pin falls below 0.65V (typ), the GATE pin turns on again if the RETRY pin is high (if the RETRY pin is low, the UV pin must be pulsed low to reset the internal fault latch before the GATE pin will turn on). If the RETRY pin is grounded and the UV pin is not cycled low, the GATE pin remains latched off and the TIMER pin will be discharged near ground. The UV pin must be cycled low after the TIMER pin has discharged below 0.65V (typ) to reset the part.

If the RETRY pin is floating or connected to a voltage above its 1.2V threshold, the LT4254 automatically restarts after a current fault. Under an output short-circuit condition, the LT4254 cycles on and off with a 3% on-time duty cycle.

**RETRY:** Current Fault Retry. RETRY commands the operational mode of the current limit. If the RETRY pin is floating, the LT4254 automatically restarts after a current fault. If it is connected to a voltage below 0.4V, the part latches off after a current fault (which requires that the UV pin be cycled low in order to start normal operation again).

**GATE:** High Side Gate Drive for the External N-Channel MOSFET. An internal charge pump guarantees at least 10V of gate drive for  $V_{CC}$  supply voltages above 20V and 4.5V gate drive for  $V_{CC}$  supply voltages between 10.8V and 20V. The rising slope of the voltage on GATE is set by an external capacitor connected from the GATE pin to GND and an internal 35 $\mu$ A pull-up current source from the charge pump output.

If the current limit is reached, the GATE pin voltage is adjusted to maintain a constant voltage across the sense resistor while the timing capacitor starts to charge. If the TIMER pin voltage ever exceeds 4.65V, the GATE pin is pulled low.

The GATE pin is also pulled to GND whenever the UV pin is pulled low, or the  $V_{CC}$  supply voltage drops below the externally programmed undervoltage threshold or above the overvoltage threshold.

The GATE pin is clamped internally to a maximum voltage of 11V (typ) above  $V_{CC}$  under normal operating conditions.

Driving this pin beyond the clamp voltage may damage the part. A zener diode is needed between the gate and source of the external MOSFET to protect its gate oxide under instantaneous short-circuit conditions. See Applications Information.

**SENSE:** Current Limit Sense. A sense resistor is placed in the supply path between  $V_{CC}$  and SENSE. The current limit circuit regulates the voltage across the sense resistor ( $V_{CC} - \text{SENSE}$ ) to 50mV while in current limit when FB is 2V or higher. If FB drops below 2V, the regulated voltage across the sense resistor decreases linearly and stops at 15mV when FB is 0V. The OPEN output also uses SENSE to detect when the output current is less than (3.5mV)/R5. To defeat current limit, connect SENSE to  $V_{CC}$ .

**PWRGD:** Open Collector Output to GND. PWRGD is pulled low whenever the voltage on FB falls below the high-to-low threshold voltage. It goes into a high impedance state when the voltage on FB exceeds the low-to-high threshold voltage. An external pull-up resistor can pull PWRGD to a voltage higher or lower than  $V_{CC}$ . To disable PWRGD, float this pin and connect FB to the output voltage.

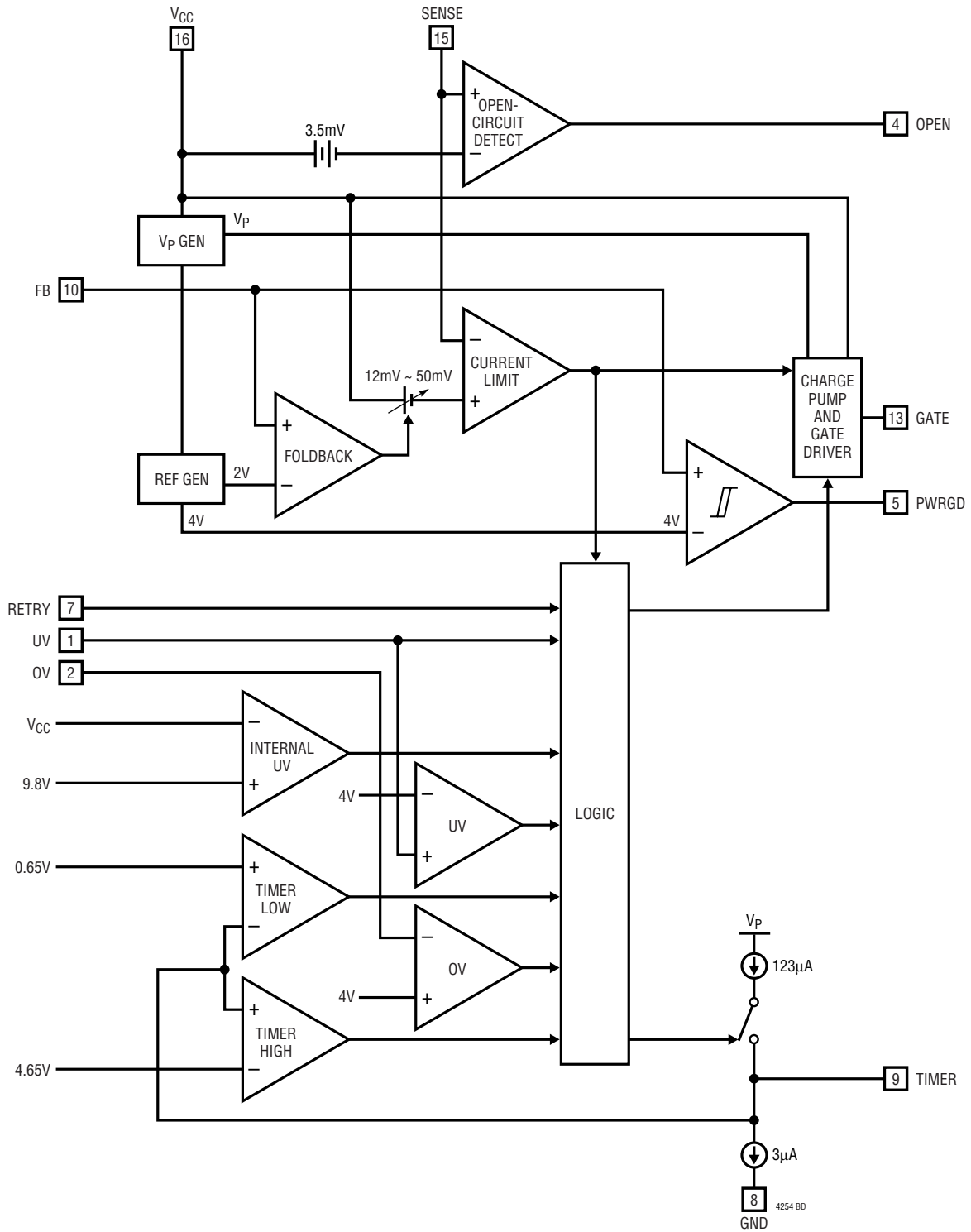
**UV:** Undervoltage Sense. UV is an input that enables the output voltage. When the UV pin is driven above 4V, the GATE pin starts charging and the output turns on. When the UV pin goes below 3.6V, the GATE pin discharges and the output shuts off.

Pulsing the UV pin to ground after a current limit fault cycle (TIMER pin discharged to below 0.65V typ) resets the fault latch (when RETRY pin is low, commanding latch off operation) and allows the part to turn back on. To disable UV sensing, connect the pin to  $V_{CC}$  through a 10k resistor.

**OV:** Overvoltage Sense. OV is an input that disables the output voltage. If OV ever goes above 4V, the GATE pin is discharged and the output shuts off. When OV goes below 3.6V, the GATE pin starts charging and the output turns back on. To disable OV sensing, connect pin to ground.

**OPEN:** Open Circuit Detect Output. This pin is an open collector output that releases and is pulled high through an external resistor if the load current is less than (3.5mV/R5). If not used, leave this pin disconnected.

**BLOCK DIAGRAM**



## TEST CIRCUIT

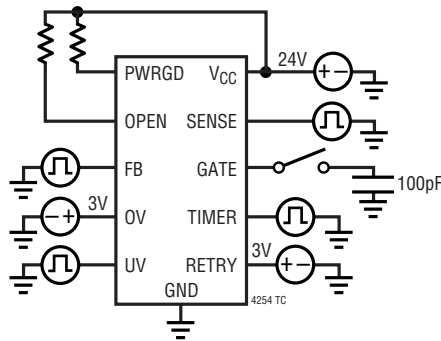


Figure 1

## TIMING DIAGRAMS

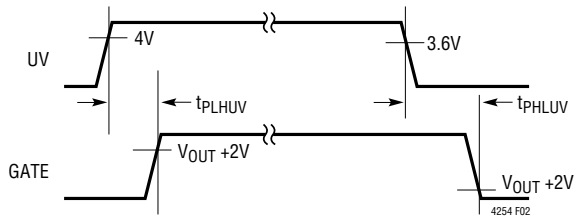


Figure 2. UV to GATE Timing

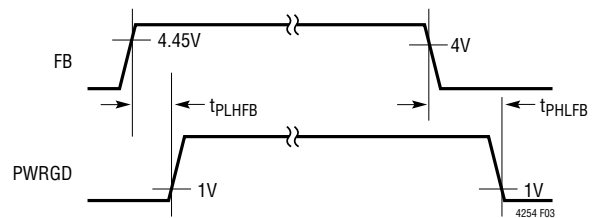


Figure 3.  $V_{OUT}$  to PWRGD Timing

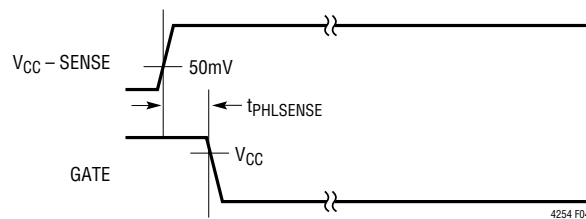


Figure 4. SENSE to GATE Timing

## APPLICATIONS INFORMATION

### Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the supply bypass capacitors on the boards draw high peak currents from the backplane power bus as they charge. The transient currents can permanently damage the connector pins and glitch the system supply, causing other boards in the system to reset.

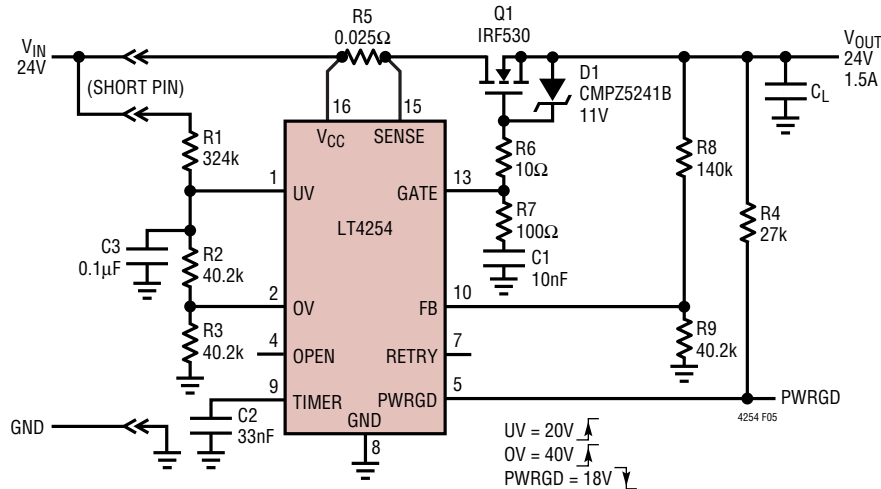
The LT4254 is designed to turn on a board's supply voltage in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. The

device also provides undervoltage and overvoltage as well as overcurrent protection while a power good output signal indicates when the output supply voltage is ready with a high output.

### Power-Up Sequence

An external N-channel MOSFET pass transistor (Q1) is placed in the power path to control the power up of the supply voltage (Figure 5). Resistor R5 provides current detection and capacitor C1 controls the GATE slew rate.

**APPLICATIONS INFORMATION**



**Figure 5. 2A, 24V Application**

Resistor R7 compensates the current control loop while R6 prevents high frequency oscillations in Q1.

When the power pins first make contact, transistor Q1 is held off. If the voltage on the V<sub>CC</sub> pin is between the externally programmed undervoltage and overvoltage thresholds, and the voltage on the TIMER pin is less than 4.65V (typ), transistor Q1 will be turned on (Figure 6). The voltage at the GATE pin rises with a slope equal to 35μA/C1 and the supply inrush current is set at:

$$I_{INRUSH} = C_L \cdot 35\mu A/C1$$

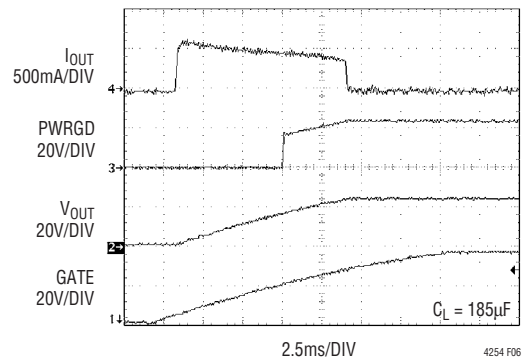
If the voltage across the current sense resistor R5 reaches V<sub>SENSETRIP</sub>, the inrush current will be limited by the internal current limit circuitry. The voltage on the GATE pin is adjusted to maintain a constant voltage across the sense resistor and the TIMER pin begins to charge.

When the FB pin voltage goes above the low-to-high V<sub>FB</sub> threshold, the PWRGD pin goes high.

**Short-Circuit Protection**

The LT4254 features a programmable foldback current limit with an electronic circuit breaker that protects against short circuits or excessive load currents. The current limit is set by placing a sense resistor (R5) between V<sub>CC</sub> and SENSE.

To limit excessive power dissipation in the pass transistor and to reduce voltage spikes on the input supply during short-circuit conditions at the output, the current folds



**Figure 6. Start-Up Waveforms**

back as a function of the output voltage, which is sensed internally on the FB pin.

When the voltage at the FB pin is 0V, the current limit circuit drives the GATE pin to force a constant 12mV drop across the sense resistor. As the output at the FB pin increases, the voltage across the sense resistor increases until the FB pin reaches 2V, at which point the voltage across the sense resistor is held constant at 50mV (see Figure 7). The current limit threshold is calculated as:

$$I_{LIMIT} = 50mV/R5$$

where R5 is the sense resistor.

For a 0.025Ω sense resistor, the current limit is set at 2000mA and folds back to 600mA when the output is shorted to ground. Thus, MOSFET dissipation under short-circuit conditions is reduced from 36W to 12W. See the

## APPLICATIONS INFORMATION

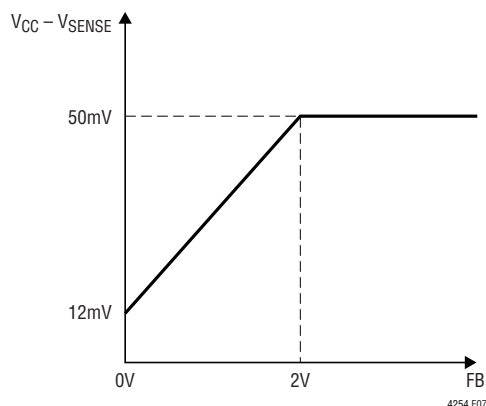


Figure 7. Current Limit Sense Voltage vs Feedback Pin Voltage

Layout Considerations section for important information about board layout to minimize current limit threshold error.

The LT4254 also features a variable overcurrent response time. The time required for the part to regulate the GATE pin voltage is a function of the voltage across the sense resistor connected between the V<sub>CC</sub> pin and the SENSE pin. This helps to eliminate sensitivity to current spikes and transients that might otherwise unnecessarily trigger a current limit response and increase MOSFET dissipation. Figure 8 shows the response time as a function of the overdrive at the SENSE pin.

### TIMER

The TIMER pin provides a method for programming the maximum time the part is allowed to operate in current limit. When the current limit circuitry is not active, the TIMER pin is pulled to GND by a 3μA current source. When the current limit circuitry becomes active, a 123μA pull-up current source is added to the TIMER pin and the voltage will rise with a slope equal to 120μA/C<sub>TIMER</sub> as long as the circuitry stays active. Once the desired maximum current limit time is known, the capacitor value is:

$$C(\text{nF}) = 25.8 \cdot t(\text{ms})$$

Whenever the TIMER pin reaches 4.65V (typ), the internal fault latch is set causing the GATE to be pulled low and the TIMER pin to be discharged to GND by the 3μA current source. The part is not allowed to turn on again until the voltage at the TIMER pin falls below 0.65V (typ).

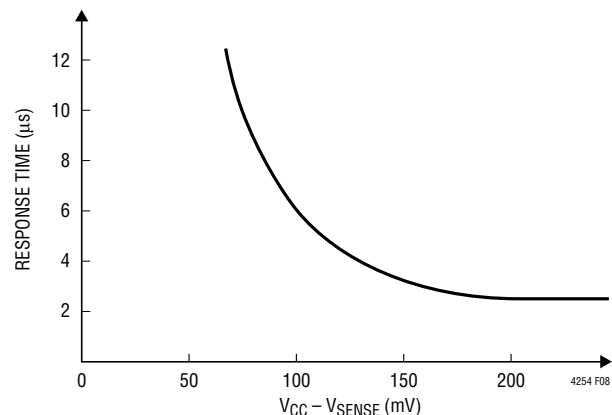


Figure 8. Response Time to Overcurrent

The TIMER pin must never be pulled high by a low impedance because whenever the TIMER pin voltage rises above the upper threshold (typically 4.65V) the pin characteristics change from a high impedance current source to a low impedance. If the pin must be pulled high by a logic signal, then a resistor must be put in series with the TIMER pin to limit the current to approximately 100 microamperes. The resistance should be chosen as follows:

$$R_{\text{SERIES}} = (V_{\text{LOGIC}} - 4.65\text{V})/100\mu\text{A}$$

Whenever the GATE pin is commanded off by any fault condition, it is discharged with a high current, turning off the external MOSFET. The waveform in Figure 9 shows how the output latches off following a short-circuit. The drop across the sense resistor is held at 12mV as the timer ramps up. Since the output did not rise bringing FB above 2V and the current is still 12mV/R<sub>5</sub>, the circuit latches off.

### Automatic Restart

If the RETRY pin is floating, then the functionality is as described in the previous section.

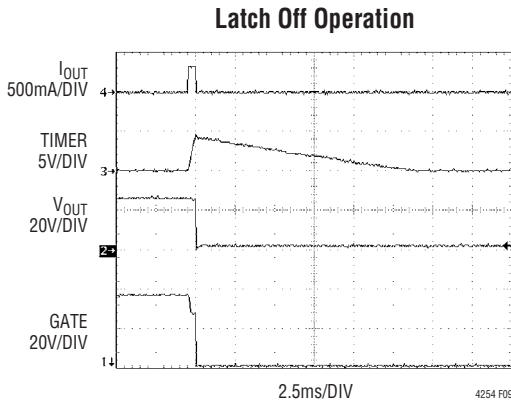
When the voltage at the TIMER pin ramps back down to 0.65V (typ), the LT4254 turns on again. If the short-circuit condition at the output still exists, the cycle will repeat itself indefinitely. The duty cycle under short-circuit conditions is 3% which prevents Q1 from overheating.

### Latch Off Operation

If the RETRY pin is grounded, the LT4254 will latch off after a current fault. After the part latches off, it may be

4254fb

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**Figure 9. Latch Off Waveforms**

commanded to start back up. This can be commanded by cycling the UV pin to ground and then back high (this command can only be accepted after the TIMER pin discharges below the 0.65V typ threshold, so as to prevent overheating transistor Q1).

Therefore, using the RETRY pin only, the LT4254 will either latch off after an overcurrent fault condition or it will go into a hiccup mode.

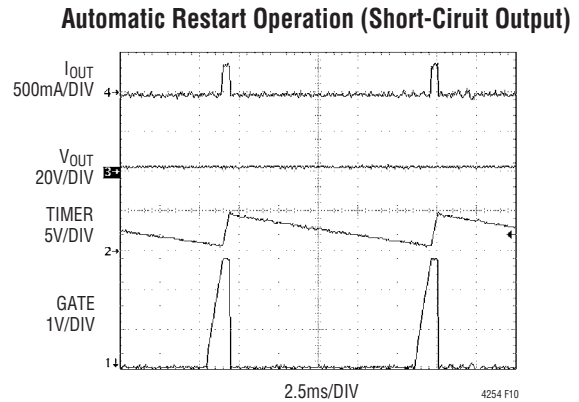
**Undervoltage and Overvoltage Detection**

The LT4254 uses the UV and OV pins to monitor the  $V_{CC}$  voltage and allow the user the greatest flexibility for setting the operational thresholds. The UV and OV pins are internally connected to an analog window comparator. Any time that the UV pin goes below 3.6V or the OV pin goes above 4V, the gate will be pulled low until the UV/OV pin voltages return to the normal operation voltage window (4V and 3.65V, respectively).

**Power Good Detection**

The LT4254 includes a comparator for monitoring the output voltage. The output voltage is sensed through the FB pin via an external resistor string. The comparator's output (PWRGD pin) is an open collector capable of operating from a pull-up as high as 36V.

The PWRGD pin can be used to directly enable/disable a power module with an active high enable input. Figure 11 shows how to use the PWRGD pin to control an active low enable input power module. Signal inversion is accomplished by transistor Q2 and R10.



**Figure 10. RETRY Waveforms**

**Open FET Detection**

The LT4254 can be used to detect the presence of an open FET. When the voltage across the sense resistor is less than 3.5mV, the open collector pull-down device is shut off allowing the OPEN pin to be externally pulled high.

An open FET condition is signalled when the OPEN pin is high and the PWRGD pin is low (after the part has completed its start-up cycle). This open FET condition can be falsely signalled during start-up if the load is not activated until after PWRGD goes high. To avoid this false indication, the OPEN and PWRGD pins should not be polled for a period of time,  $t_{STARTUP}$ , given by:

$$\frac{3 \cdot V_{CC} \cdot C1}{35\mu A} = t_{STARTUP}$$

This can be accomplished either by a microcontroller (if available) or by placing an RC filter as shown in Figure 12.

Once the OPEN voltage exceeds the monitoring logic threshold,  $V_{THRESH}$ , and PWRGD is low, an open FET condition is signalled. In order to prevent a false indication, the RC product should be set with the following equation:

$$RC > \frac{3 \cdot V_{CC} \cdot C1}{35\mu A \left( \ln \left( \frac{V_{LOGIC}}{V_{LOGIC} - V_{THRESH}} \right) \right)}$$

Another condition that can cause a false indication is if the LT4254 goes into current limit during start-up. This will cause  $t_{STARTUP}$  to be longer than calculated. Also, if the

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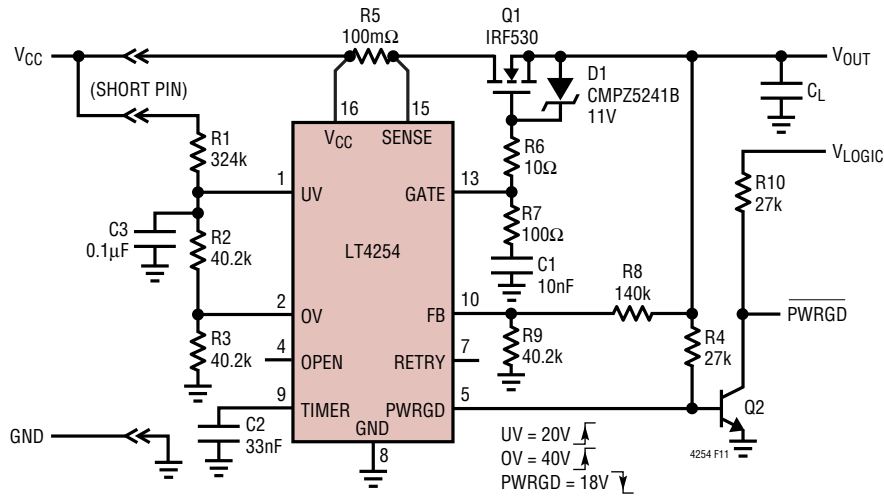


Figure 11. Active Low Enable PWRGD Application

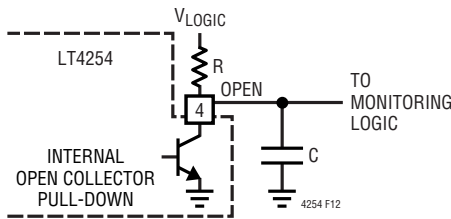


Figure 12. Delay Circuit for OPEN FET Detection

LT4254 stays in current limit long enough for the TIMER pin to fully charge up to its threshold, the LT4254 will either latch off (RETRY = 0) or go into the current limit hiccup mode (RETRY = floating). In either case, an open FET condition will be falsely signalled. If the LT4254 does go into current limit during start-up, C1 can be increased (see Power-Up Sequence).

Supply Transient Protection

The LT4254 is 100% tested and guaranteed to be safe from damage with supply voltages up to 44V. However, voltage transients above 44V may damage the part. During a short-circuit condition, the large change in currents flowing through the power supply traces can cause inductive voltage transients which could exceed 44V. To minimize the voltage transients, the power trace parasitic inductance should be minimized by using wider traces or heavier trace plating and a 0.1µF bypass capacitor should be placed between VCC and GND. A surge

suppressor (Transorb) at the input can also prevent damage from voltage transients.

GATE Pin

A curve of gate drive vs VCC is shown in Figure 13. The GATE pin is clamped to a maximum voltage of 12V above the VCC voltage. This clamp is designed to withstand the internal charge pump current. An external zener diode should be used if the possibility exists for an instantaneous low resistance short on VOUT to occur. At a minimum input supply voltage of 12V, the minimum gate drive voltage is 4.5V. When the input supply voltage is higher than 20V, the gate drive voltage is at least 10V and a

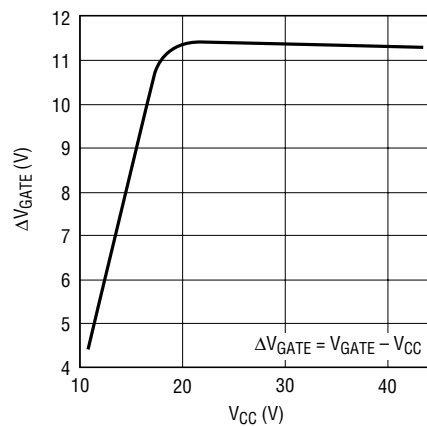


Figure 13. ΔVGATE vs VCC

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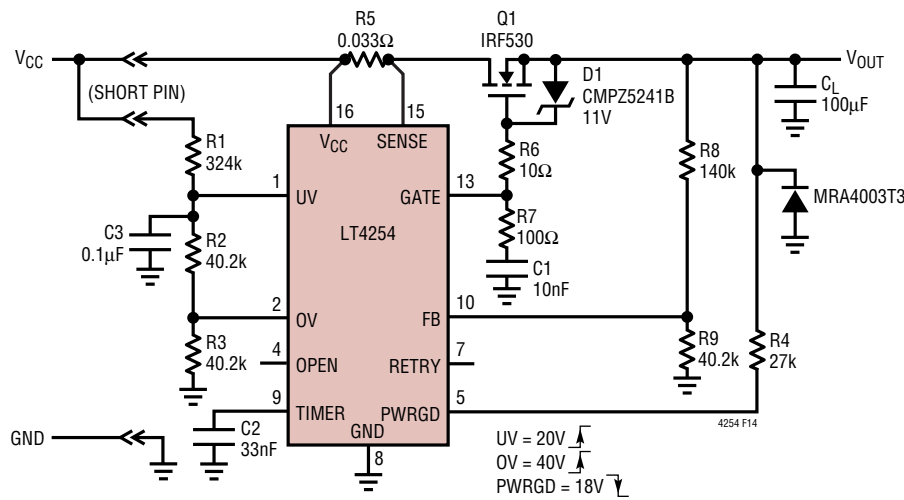


Figure 14. Negative Output Voltage Protection Diode Application

standard threshold MOSFET can be used. In applications from 12V to 15V range, a logic level MOSFET must be used.

In some applications it may be possible for the  $V_{OUT}$  pin to ring below ground (due to the parasitic trace inductance). Higher current applications, especially where the output load is physically far away from the LT4254 will be more susceptible to these transients. This is normal and the LT4254 has been designed to allow for some ringing below ground. However, if the application is such that  $V_{OUT}$  can ring more than 1V below ground, damage may occur to the LT4254 and an external diode from ground (anode) to  $V_{OUT}$  (cathode) will have to be added to the circuit as shown in Figure 14 (it is critical that the reverse breakdown voltage of the diode be higher than the highest expected  $V_{CC}$  voltage). A capacitor placed from ground to  $V_{OUT}$  directly at the LT4254 pins can help reduce the amount of ringing on  $V_{OUT}$  but it may not be enough for some applications.

During a fault condition, the LT4254 pulls down on the GATE pin with a switch capable of sinking about 55mA. Once the GATE voltage drops below the output voltage by a diode forward voltage, the external zener will forward bias and the output will also be discharged to GND. In addition to the GATE capacitance, the output capacitance will be discharged through the LT4254. In applications

that have very large output capacitors, this could cause damage to the LT4254. Therefore, the maximum output capacitance that can be used with the LT4254 is 1000μF.

In applications utilizing very large external N-channel MOSFETs, the possibility exists for the MOSFET to turn on when initially inserted into a live backplane (before the LT4254 becomes active and pulls down on GATE). This is due to the drain to gate capacitance forcing current into R7 and C1 when the drain voltage steps up from ground to  $V_{CC}$  with an extremely fast rise time. To alleviate this situation, a Schottky diode should be put across R7 with the cathode connected to C1 as shown in Figure 16.

Layout Considerations

To achieve accurate current sensing, a Kelvin connection to the current sense resistor (R5 in typical application circuit) is recommended. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530μΩ/□. Small resistances can cause large errors in high current applications. Noise immunity will be improved significantly by locating resistor dividers close to the pins with short  $V_{CC}$  and GND traces. A 0.1μF decoupling capacitor from UV to GND is also required. Figure 15 shows a layout that meets these requirements.

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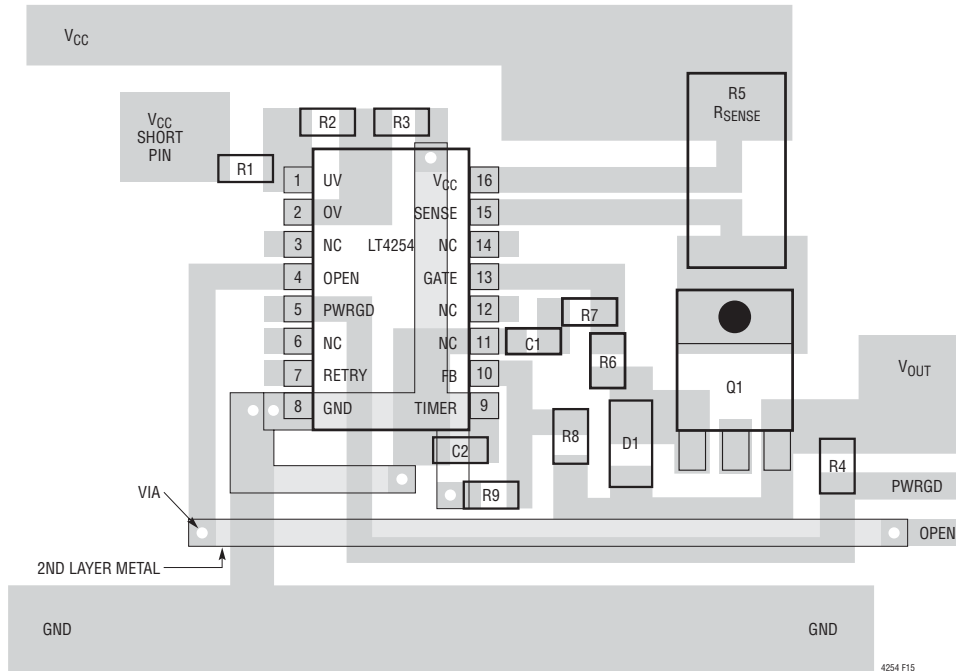
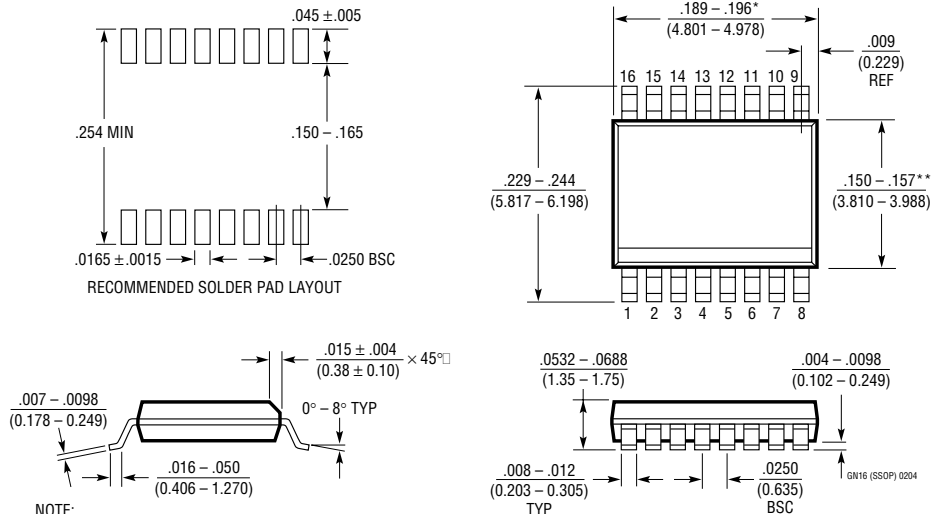


Figure 15. Recommended Component Placement

# PACKAGE DESCRIPTION

## GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



- NOTE:
1. CONTROLLING DIMENSION: INCHES
  2. DIMENSIONS ARE IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
  3. DRAWING NOT TO SCALE
- \* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
- \*\* DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE



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