THE DATASHEET OF

LPV7215MF/NOPB

LPV7215 Micropower, CMOS Input, RRIO, 1.8-V, Push-Pull Output Comparator

1 Features

- (For V^+ = 1.8 V, Typical Unless Otherwise Noted)
- Ultra-Low Power Consumption: 580 nA
- Wide Supply Voltage Range: 1.8 V to 5.5 V
- Propagation Delay: 4.5 µs
- Push-Pull Output Current Drive at 5 V 19 mA
- Temperature Range: −40°C to 125°C
- Rail-to-Rail Input
- Tiny 5-Pin SOT-23 and SC70 Packages

2 Applications

- RC Timers
- Window Detectors
- IR Receivers
- Multivibrators
- Alarm and Monitoring Circuits

3 Description

The LPV7215 device is an ultra-low-power comparator with a typical power supply current of 580 nA. It has the best-in-class power supply current versus propagation delay performance available among TI's low-power comparators. The propagation delay is as low as 4.5 µs with 100-mV overdrive at 1.8-V supply.

Designed to operate over a wide range of supply voltages, from 1.8 V to 5.5 V, with ensured operation at 1.8 V, 2.7 V, and 5 V, the LPV7215 is ideal for use in a variety of battery-powered applications. With rail-to-rail common-mode voltage range, the LPV7215 is well suited for single-supply operation.

Featuring a push-pull output stage, the LPV7215 allows for operation with absolute minimum power consumption when driving any capacitive or resistive load.

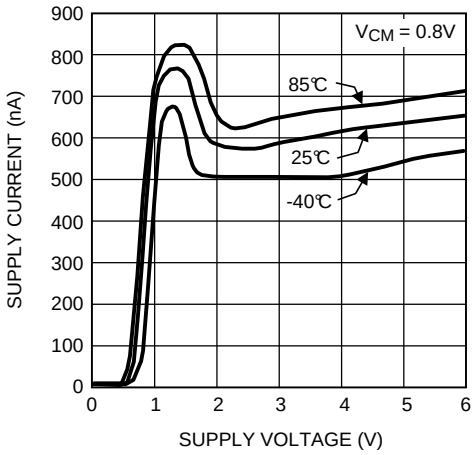
Available in a choice of space-saving packages, the LPV7215 is ideal for use in handheld electronics and mobile phone applications. The LPV7215 is manufactured with TI's advanced VIP50 process.

Device Information(1)

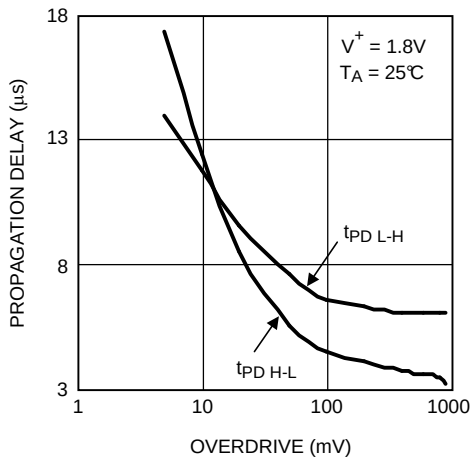
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LPV7215	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Supply Current vs Supply Voltage



Propagation Delay vs Overdrive



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (April 2013) to Revision J **Page**

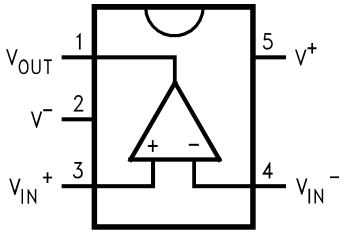
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Updated values in the *Thermal Information* table to align with JEDEC standards. ... 4

Changes from Revision H (April 2013) to Revision I **Page**

- Changed layout of National Data Sheet to TI format ... 22

5 Pin Configuration and Functions

DBV and DCK Package
5-Pin SOT-23 and SC70
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{OUT}	O	Output
2	V^-	P	Negative Supply
3	VIN+	I	Noninverting Input
4	VIN–	I	Inverting Input
5	V^+	P	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN} differential	−2.5	2.5	V
Supply voltage (V^+ - V^-)		6	V
Voltage at input and output pins	V^- − 0.3	V^+ + 0.3	V
Junction temperature, T_J (2)		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1)	±2000	V
		Machine model (MM)(2)	±200	

(1) Human-body model, applicable std. MIL-STD-883, Method 3015.7.
(2) Machine model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Temperature (1)	–40	125	°C
Supply voltage ($V^+ – V^-$)	1.8	5.5	V

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PCB.

6.4 Thermal Information

THERMAL METRIC (1)		LPV7215		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	234	456	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	153	110.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.7	59.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	38	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.2	59	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PCB.

6.5 Electrical Characteristics: 1.8 V

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 1.8V, V^- = 0 V, and $V_{CM} = V^+/2$, $V_O = V^-$. (1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
I_S	Supply current	V_{CM} = 0.3 V	T_A = 25°C		580	750	nA
			Temperature extremes			1050	
		V_{CM} = 1.5 V	T_A = 25°C		790	980	
			Temperature extremes			1300	
V_{OS}	Input offset voltage	V_{CM} = 0 V	T_A = 25°C		±0.3	±6	mV
			Temperature extremes			±8	
		V_{CM} = 1.8 V	T_A = 25°C		±0.4	±5	
			Temperature extremes			±7	
TCV_{OS}	Input offset average drift	See (4)			±1		µV/C
I_B	Input bias current (5)	V_{CM} = 1.6 V			−40		fA
I_{OS}	Input offset current				10		fA

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.

Electrical Characteristics: 1.8 V (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 1.8V, V^- = 0 V, and V_{CM} = V^+/2, V_O= V^-.(1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
CMRR	Common-mode rejection ratio	V_{CM} Stepped from 0 V to 0.7 V	T_A = 25°C	66	88		dB
			Temperature extremes	62			
		V_{CM} Stepped from 1.2 V to 1.8 V	T_A = 25°C	68	87		
			Temperature extremes	62			
		V_{CM} Stepped from 0 V to 1.8 V	T_A = 25°C	44	77		
			Temperature extremes	43			
PSRR	Power supply rejection ratio	V^+ = 1.8 V to 5.5 V, V_{CM} = 0 V	T_A = 25°C	66	82		dB
			Temperature extremes	63			
CMVR	Input common-mode voltage range	CMRR ≥ 40 dB	Temperature Extremes	–0.1		1.9	V
A_V	Voltage gain				120		dB
V_O	Output swing high	I_O = 500 µA	T_A = 25°C	1.63	1.69		V
			Temperature extremes	1.58			
		I_O = 1 mA	T_A = 25°C	1.46	1.6		
			Temperature extremes	1.37			
	Output swing low	I_O = −500 µA	T_A = 25°C		88	180	mV
			Temperature extremes			230	
		I_O = −1 mA	T_A = 25°C		180	310	
			Temperature extremes			400	
I_{OUT}	Output current	Source V_O = V^+/2	T_A = 25°C	1.75	2.26		mA
			Temperature extremes	1.3			
		Sink V_O = V^+/2	T_A = 25°C	2.35	3.1		
			Temperature extremes	1.45			
	Propagation delay (high to low)	Overdrive = 10 mV			13		µs
		Overdrive = 100 mV	T_A = 25°C		4.5	6.5	
			Temperature extremes			9	
	Propagation delay (low to high)	Overdrive = 10 mV			12.5		µs
		Overdrive = 100 mV	T_A = 25°C		6.6	9	
			Temperature extremes			12	
t_{rise}	Rise time	Overdrive = 10 mV C_L = 30 pF, R_L = 1 MΩ			80		ns
		Overdrive = 100 mV C_L = 30 pF, R_L = 1 MΩ			75		
t_{fall}	Fall time	Overdrive = 10 mV C_L = 30 pF, R_L = 1 MΩ			70		ns
		Overdrive = 100 mV C_L = 30 pF, R_L = 1 MΩ			65		

6.6 Electrical Characteristics: 2.7 V

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 2.7 V, V^- = 0 V, and V_{CM} = V^+/2, V_O= V^-.(1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
I_S	Supply current	V_{CM} = 0.3 V	T_A = 25°C		605	780	nA
			Temperature extremes			1100	
		V_{CM} = 2.4 V	T_A = 25°C		815	1010	
			Temperature extremes			1350	
V_{OS}	Input offset voltage	V_{CM} = 0 V	T_A = 25°C		±0.3	±6	mV
			Temperature extremes			±8	
		V_{CM} = 2.7 V	T_A = 25°C		±0.3	±5	
			Temperature extremes			±7	
TCV_{OS}	Input offset average drift	See (4)			±1		µV/C
I_B	Input bias current (5)	V_{CM} = 1.8 V			−40		fA
I_{OS}	Input offset current				20		fA
CMRR	Common-mode rejection ratio	V_{CM} Stepped from 0 V to 1.6 V	T_A = 25°C	72	90		dB
			Temperature extremes	66			
		V_{CM} Stepped from 2.1V to 2.7V	T_A = 25°C	71	94		
			Temperature extremes	63			
		V_{CM} Stepped from 0 V to 2.7 V	T_A = 25°C	47	80		
			Temperature extremes	46			
PSRR	Power supply rejection ratio	V^+ = 1.8 V to 5.5 V, V_{CM} = 0 V	T_A = 25°C	66	82		dB
			Temperature extremes	63			
CMVR	Input common-mode voltage range	CMRR ≥ 40 dB	Temperature extremes	−0.1		2.8	V
A_V	Voltage gain				120		dB
V_O	Output swing high	I_O = 500 µA	T_A = 25°C	2.57	2.62		V
			Temperature extremes	2.53			
		I_O = 1 mA	T_A = 25°C	2.47	2.53		
			Temperature extremes	2.4			
	Output swing low	I_O = −500 µA	T_A = 25°C		60	130	mV
			Temperature extremes			190	
		I_O = −1 mA	T_A = 25°C		120	250	
			Temperature extremes			330	

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.

Electrical Characteristics: 2.7 V (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 2.7 V, V^- = 0 V, and V_{CM} = V^+/2, V_O= V^-.(1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
I_{OUT}	Output current	Source V_O = V^+/2	T_A = 25°C	4.5	5.7		mA
			Temperature extremes	3.4			
		Sink V_O = V^+/2	T_A = 25°C	5.6	7.5		
			Temperature extremes	3.2			
	Propagation delay (high to low)	Overdrive = 10 mV			14.5		µs
		Overdrive = 100 mV	T_A = 25°C		5.8	8.5	
			Temperature extremes			10.5	
	Propagation delay (low to high)	Overdrive = 10 mV			15		
		Overdrive = 100 mV	T_A = 25°C		7.5	10	
			Temperature extremes			12.5	
t_{rise}	Rise time	Overdrive = 10 mV C_L = 30 pF, R_L = 1 MΩ			90		ns
		Overdrive = 100 mV C_L = 30 pF, R_L = 1 MΩ			85		
t_{fall}	Fall time	Overdrive = 10 mV C_L = 30 pF, R_L = 1 MΩ			85		ns
		Overdrive = 100 mV C_L = 30 pF, R_L = 1 MΩ			75		

6.7 Electrical Characteristics: 5 V

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 5 V, V^- = 0 V, and V_{CM} = V^+/2, V_O= V^-. (1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
I_S	Supply current	V_{CM} = 0.3 V	T_A = 25°C		612	790	nA
			Temperature extremes			1150	
		V_{CM} = 4.7 V	T_A = 25°C		825	1030	
			Temperature extremes			1400	
V_{OS}	Input offset voltage	V_{CM} = 0 V	T_A = 25°C		±0.3	±6	mV
			Temperature extremes			±8	
		V_{CM} = 5 V	T_A = 25°C			±5	
			Temperature extremes			±7	
TCV_{OS}	Input offset average drift	See (4)			±1		µV/C
I_B	Input bias current (5)	V_{CM} = 4.5 V			−400		fA
I_{OS}	Input offset current				20		fA

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.

Electrical Characteristics: 5 V (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 5 V, V^- = 0 V, and V_{CM} = V^+/2, V_O= V^-. (1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
CMRR	Common-mode rejection ratio	V_{CM} Stepped from 0 V to 3.9 V	T_A = 25°C	72	98		dB
			Temperature extremes	66			
		V_{CM} Stepped from 4.4 V to 5 V	T_A = 25°C	73	92		
			Temperature extremes	67			
		V_{CM} Stepped from 0 V to 5 V	T_A = 25°C	53	82		
			Temperature extremes	49			
PSRR	Power supply rejection ratio	V^+ = 1.8 V to 5.5 V, V_{CM} = 0 V	T_A = 25°C	66	82		dB
			Temperature extremes	63			
CMVR	Input common-mode voltage range	CMRR ≥ 40 dB	Temperature extremes	−0.1		5.1	V
A_V	Voltage gain				120		dB
V_O	Output swing high	I_O = 500 µA	T_A = 25°C	4.9	4.94		V
			Temperature extremes	4.86			
		I_O = 1 mA	T_A = 25°C	4.82	4.89		
			Temperature extremes	4.77			
	Output swing low	I_O = −500 µA	T_A = 25°C		43	90	mV
			Temperature extremes			130	
		I_O = −1 mA	T_A = 25°C		88	170	
			Temperature extremes			230	
I_{OUT}	Output current	Source V_O = V^+/2	T_A = 25°C	13	17		mA
			Temperature extremes	7.5			
		Sink V_O = V^+/2	T_A = 25°C	14.5	19		
			Temperature extremes	8.5			
	Propagation delay (high to low)	Overdrive = 10 mV			18		µs
		Overdrive = 100 mV	T_A = 25°C		7.7	13.5	
			Temperature extremes			16	
	Propagation delay (low to high)	Overdrive = 10 mV			30		µs
		Overdrive = 100 mV	T_A = 25°C		12	15	
			Temperature extremes			20	
t_{rise}	Rise time	Overdrive = 10 mV, C_L = 30 pF, R_L = 1 MΩ			100		ns
		Overdrive = 100 mV, C_L = 30 pF, R_L = 1 MΩ			100		
t_{fall}	Fall time	Overdrive = 10 mV, C_L = 30 pF, R_L = 1 MΩ			115		ns
		Overdrive = 100 mV, C_L = 30 pF, R_L = 1 MΩ			95		

6.8 Typical Characteristics

At T_J = 25°C unless otherwise specified.

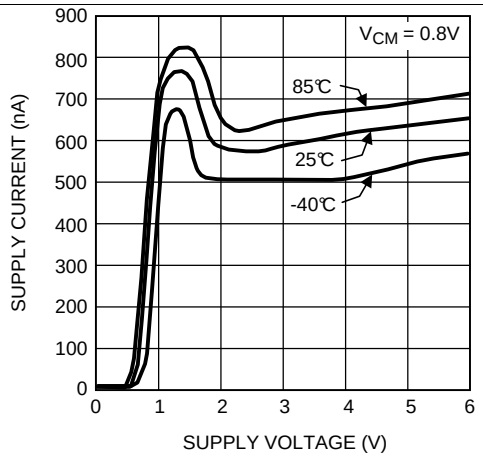


Figure 1. Supply Current vs Supply Voltage

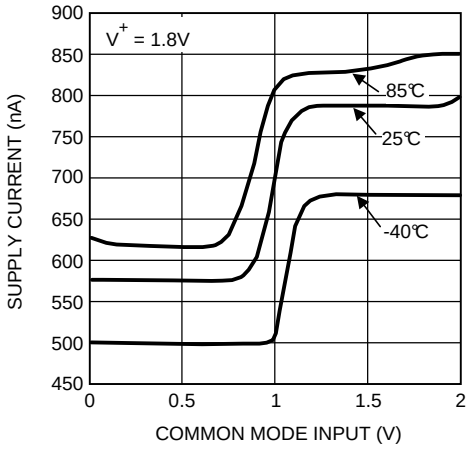


Figure 2. Supply Current vs Common-Mode Input

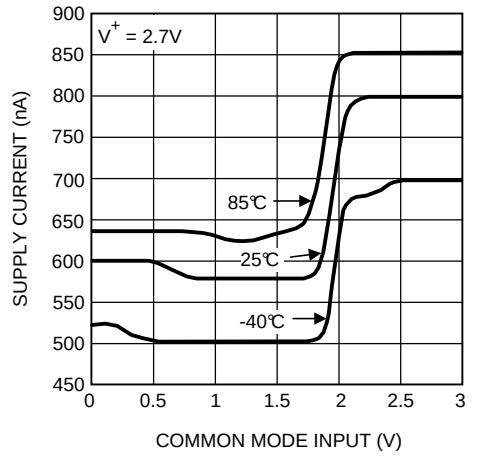


Figure 3. Supply Current vs Common-Mode Input

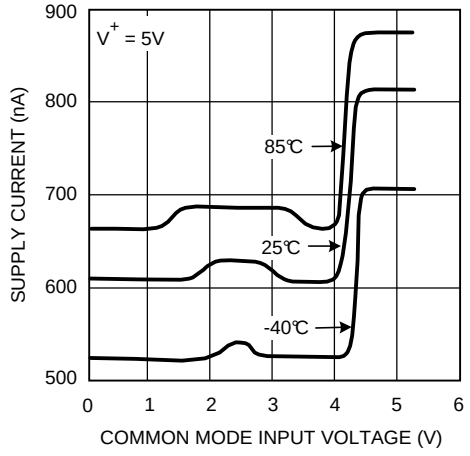


Figure 4. Supply Current vs Common-Mode Input

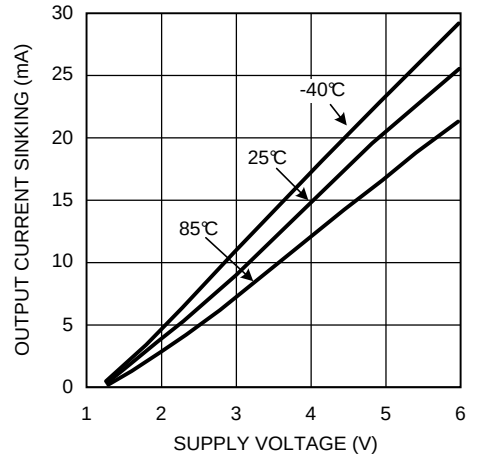


Figure 5. Short-Circuit Sinking Current vs Supply Voltage

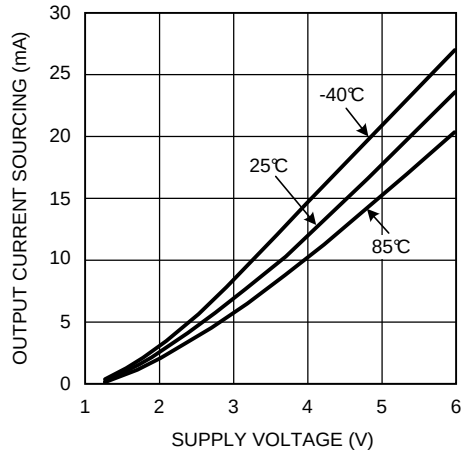


Figure 6. Short-Circuit Sourcing Current vs Supply Voltage

Typical Characteristics (continued)

At T_J = 25°C unless otherwise specified.

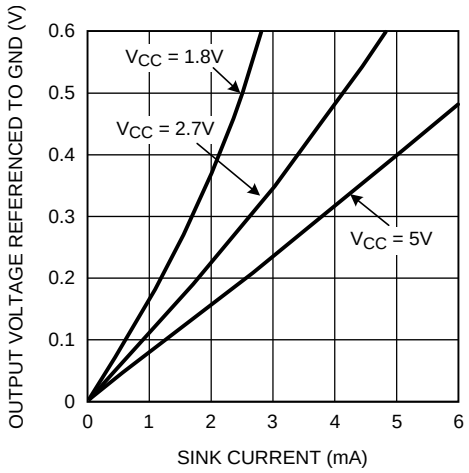


Figure 7. Output Voltage Low vs Sink Current

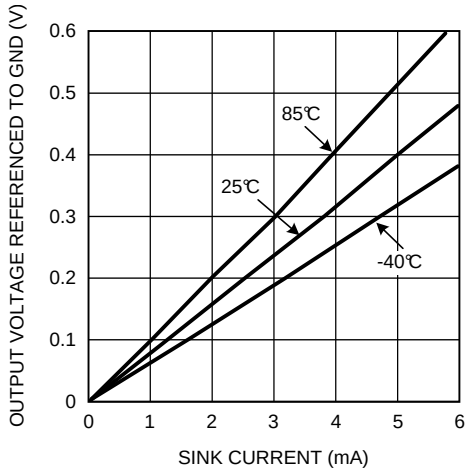


Figure 8. Output Voltage Low vs Sink Current

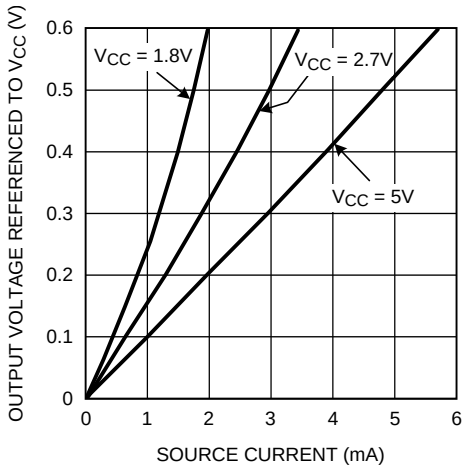


Figure 9. Output Voltage High vs Source Current

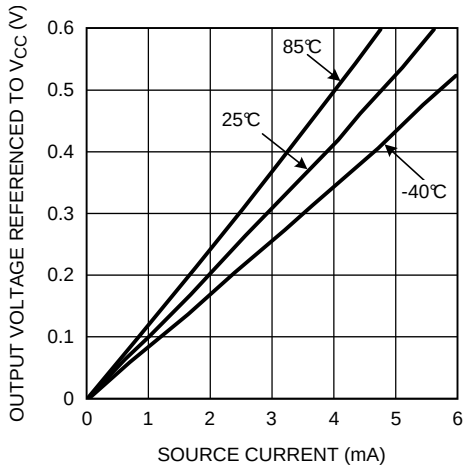


Figure 10. Output Voltage High vs Source Current

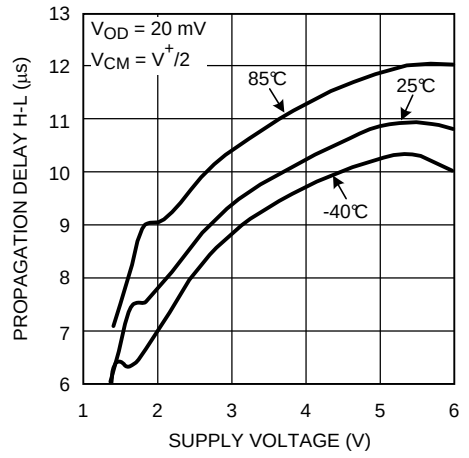


Figure 11. Propagation Delay vs Supply Voltage

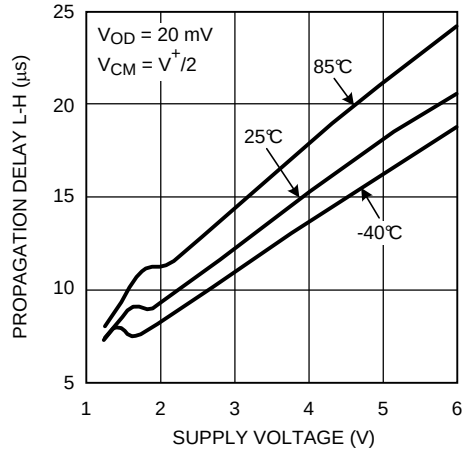


Figure 12. Propagation Delay vs Supply Voltage

Typical Characteristics (continued)

At T_J = 25°C unless otherwise specified.

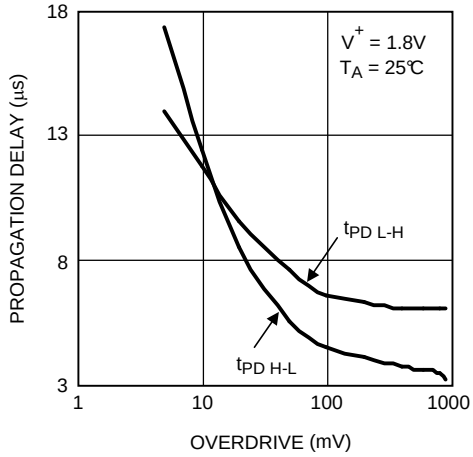


Figure 13. Propagation Delay vs Overdrive

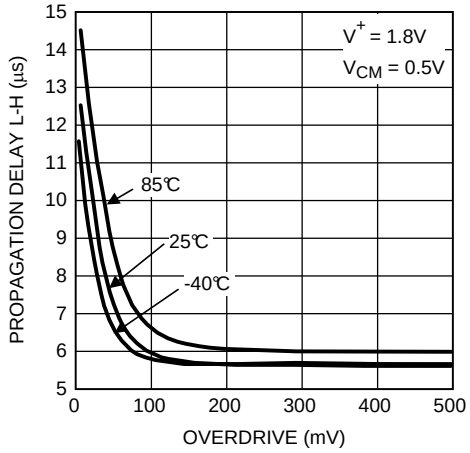


Figure 14. Propagation Delay vs Overdrive

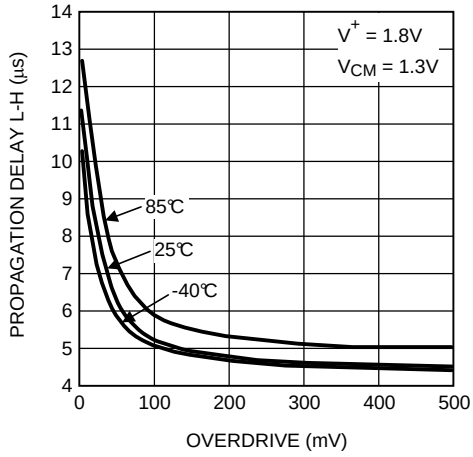


Figure 15. Propagation Delay vs Overdrive

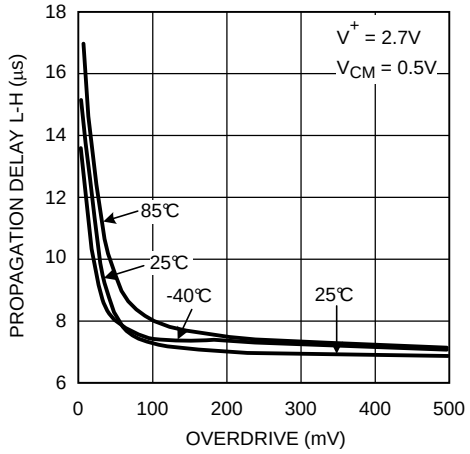


Figure 16. Propagation Delay vs Overdrive

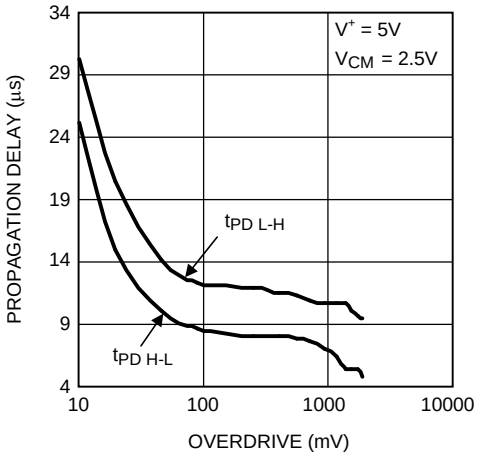


Figure 17. Propagation Delay vs Overdrive

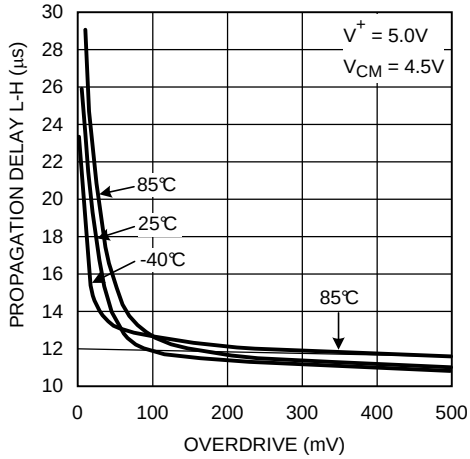


Figure 18. Propagation Delay vs Overdrive

Typical Characteristics (continued)

At T_J = 25°C unless otherwise specified.

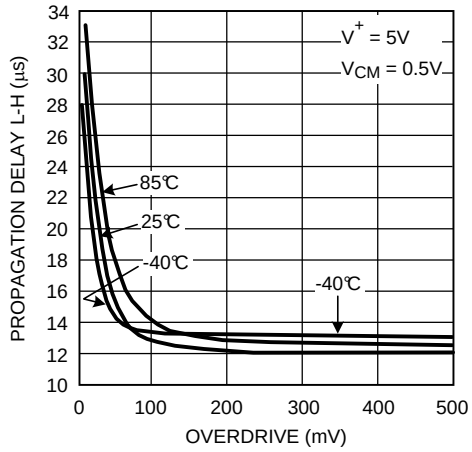


Figure 19. Propagation Delay vs Overdrive

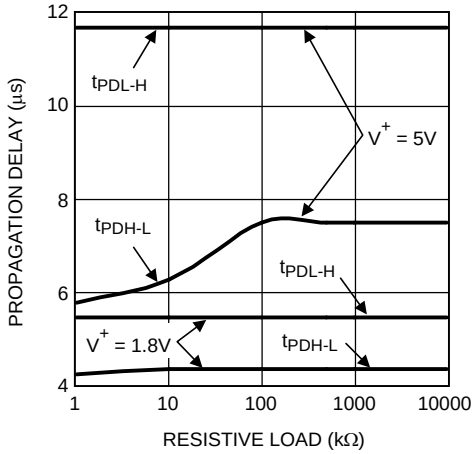


Figure 20. Propagation Delay vs Resistive Load

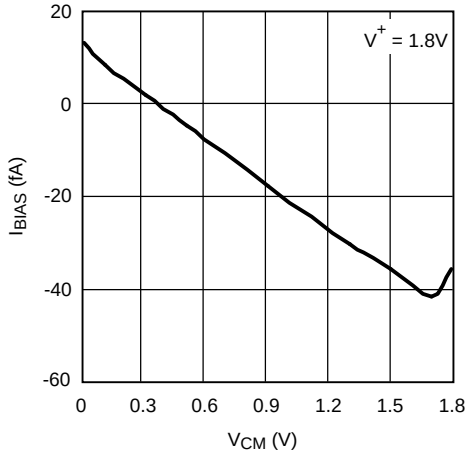


Figure 21. I_{BIAS} vs V_{CM}

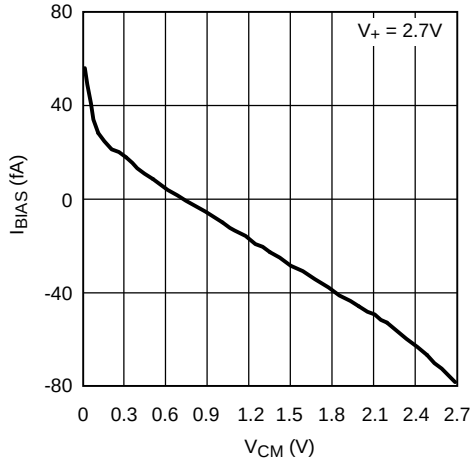


Figure 22. I_{BIAS} vs V_{CM}

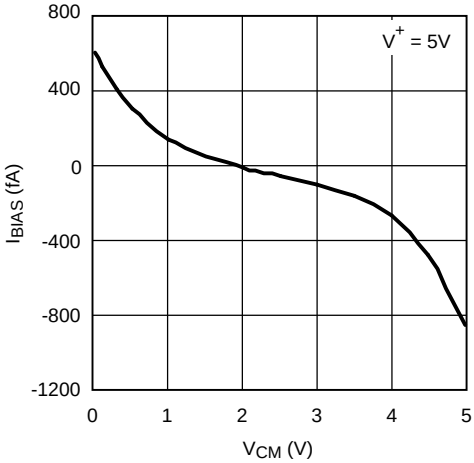


Figure 23. I_{BIAS} vs V_{CM}

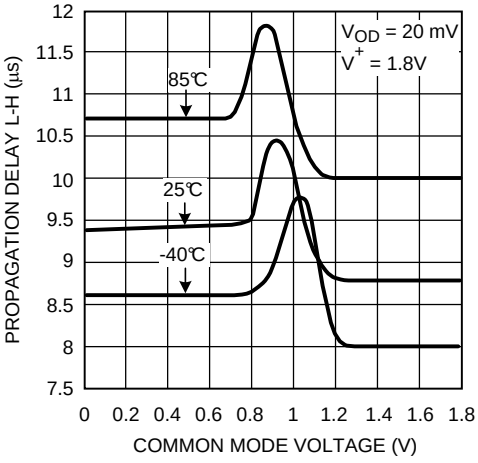


Figure 24. Propagation Delay vs Common-Mode Input

Typical Characteristics (continued)

At T_J = 25°C unless otherwise specified.

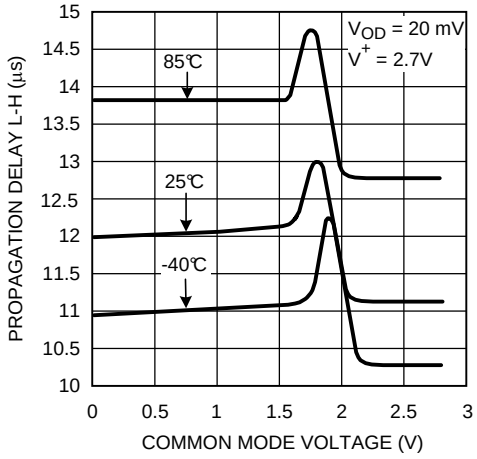


Figure 25. Propagation Delay vs Common-Mode Input

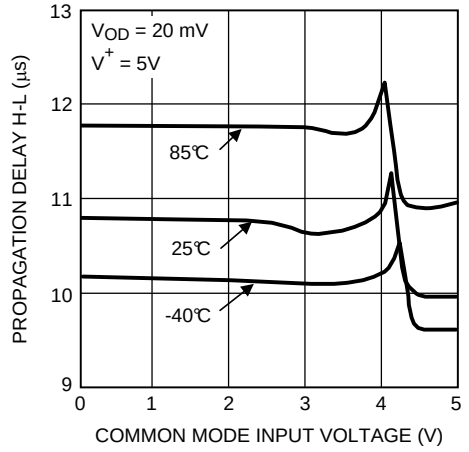


Figure 26. Propagation Delay vs Common-Mode Input

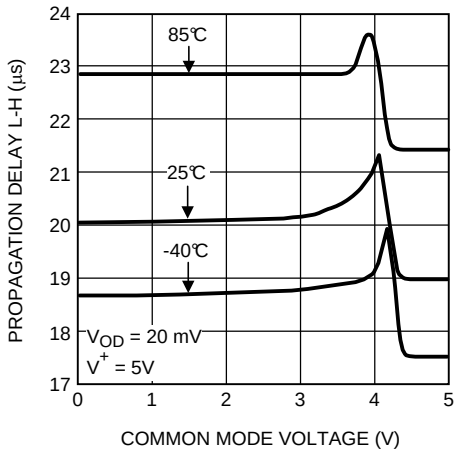


Figure 27. Propagation Delay vs Common-Mode Input

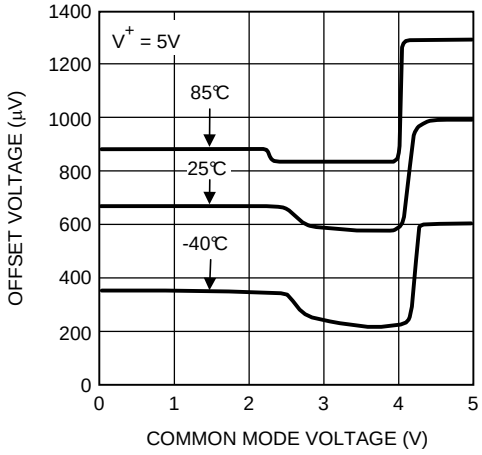


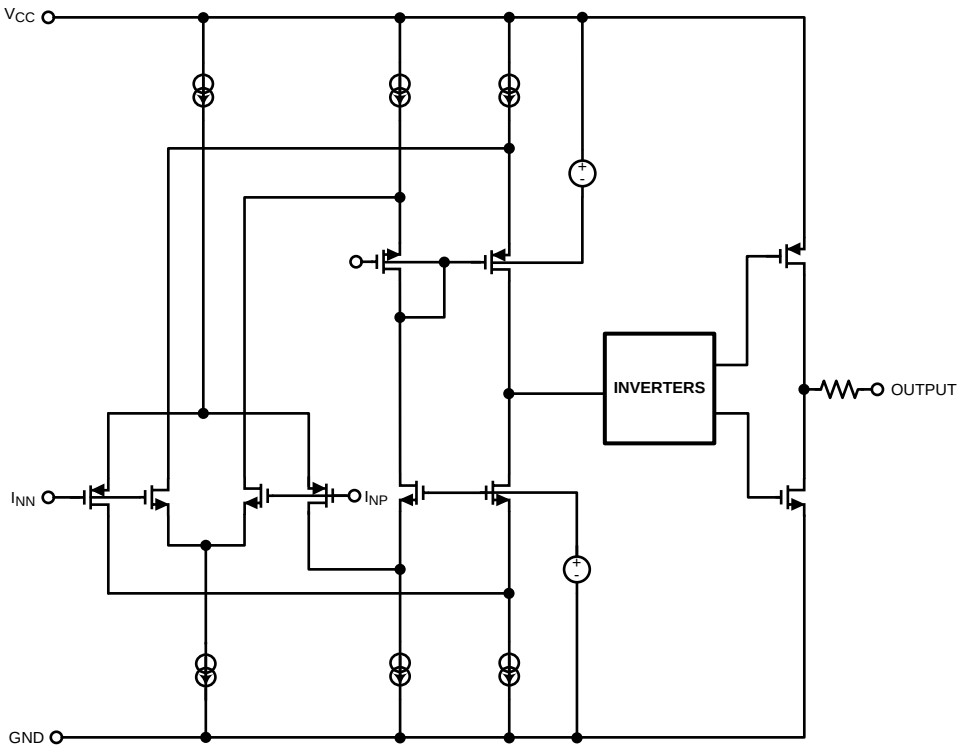
Figure 28. Offset Voltage vs Common-Mode Input

7 Detailed Description

7.1 Overview

The LPV7215 is a single-channel comparator with a push-pull output stage. This comparator is optimized for low-power consumption and single-supply operation with greater than rail-to-rail input operation. The push-pull output of the LPV7215 supports rail-to-rail output swing and interfaces with TTL/CMOS logic.

7.2 Functional Block Diagram



7.3 Feature Description

Low supply current and fast propagation delay distinguish the LPV7215 from other low-power comparators.

7.3.1 Input Stage

The LPV7215 has rail-to-rail input common-mode voltage range. It can operate at any differential input voltage within this limit as long as the differential voltage is greater than zero. A differential input of zero volts may result in oscillation.

The differential input stage of the comparator is a pair of PMOS and NMOS transistors, therefore, no current flows into the device. The input bias current measured is the leakage current in the MOS transistors and input protection diodes. This low bias current allows the comparator to interface with a variety of circuitry and devices with minimal concern about matching the input resistances.

The input to the comparator is protected from excessive voltage by internal ESD diodes connected to both supply rails. This protects the circuit from both ESD events, as well as signals that significantly exceed the supply voltages. When this occurs the ESD protection diodes becomes forward-biased and draws current into these structures, resulting in no input current to the terminals of the comparator. Until this occurs, there is essentially no input current to the diodes. As a result, placing a large resistor in series with an input that may be exposed to large voltages, limits the input current but have no other noticeable effect.

Feature Description (continued)

7.3.2 Output Stage

The LPV7215 has a MOS push-pull rail-to-rail output stage. The push-pull transistor configuration of the output keeps the total system power consumption to a minimum. The only current consumed by the LPV7215 is the less than 1-µA supply current and the current going directly into the load. No power is wasted through the pullup resistor when the output is low. The output stage is specifically designed with dead time between the time when one transistor is turned off and the other is turned on (break-before-make) to minimize shoot through currents. The internal logic controls the break-before-make timing of the output transistors. The break-before-make delay varies with temperature and power condition.

7.3.3 Output Current

Even though the LPV7215 uses less than 1-µA supply current, the outputs are able to drive very large currents. The LPV7215 can source up to 17 mA and can sink up to 19 mA, when operated at 5-V supply. This large current handling capability allows driving heavy loads directly.

7.3.4 Response Time

Depending upon the amount of overdrive, the propagation delay is typically 6 to 30 µs. The curves showing propagation delay vs overdrive in the *Typical Characteristics* section shows the delay time when the input is preset with 100 mV across the inputs and then is driven the other way by 10 mV to 500 mV.

The output signal can show a step during switching depending on the load. A fast RC time constant due to both small capacitive and resistive loads shows a significant step in the output signal. A slow RC time constant due to either a large resistive or capacitive load has a clipped corner on the output signal. The step is observed more prominently during a falling transition from high to low.

The plot in Figure 29 shows the output for single 5-V supply with a 100-kΩ resistor. The step is at 1.3 V.

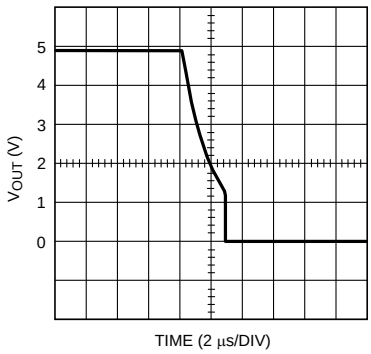


Figure 29. Output Signal Without Capacitive Load

The plot in Figure 30 shows the output signal when a 20-pF capacitor is added as a load. The step is at about 2.5 V.

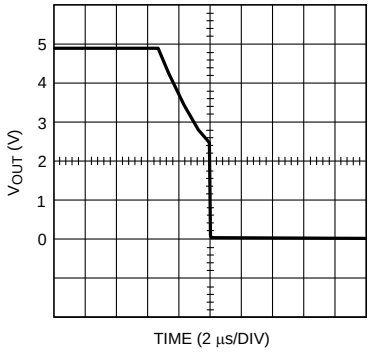


Figure 30. Output Signal With 20-pF Load

7.4 Device Functional Modes

7.4.1 Capacitive and Resistive Loads

The propagation delay is not affected by capacitive loads at the output of the LPV7215. However, resistive loads slightly affect the propagation delay on the falling edge by a reduction of almost 2 µs depending on the load resistance value.

7.4.2 Noise

Most comparators have rather low gain. This allows the output to spend time between high and low when the input signal changes slowly. The result is that the output may oscillate between high and low when the differential input is near zero. The exceptionally high gain of this comparator, 120 dB, eliminates this problem. Less than 1 µV of change on the input drives the output from one rail to the other rail. If the input signal is noisy, the output cannot ignore the noise unless some hysteresis is provided by positive feedback (see *Hysteresis*).

7.4.3 Hysteresis

To improve propagation delay when low overdrive is needed, hysteresis can be added.

7.4.4 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three resistor network that is referenced to the supply voltage V^+ of the comparator as shown in Figure 31. When V_{IN} at the inverting input is less than V_A, the voltage at the noninverting node of the comparator ($V_{IN} < V_A$), the output voltage is high (for simplicity assume V_O switches as high as V^+). The three network resistors can be represented as $R_1//R_3$ in series with R_2.

The lower input trip voltage V_{A1} is defined as Equation 1.

$$V_{A1} = V_{CC}R_2 / ((R_1//R_3) + R_2) \quad (1)$$

When V_{IN} is greater than V_A, the output voltage is low or very close to ground. In this case the three network resistors can be presented as $R_2//R_3$ in series with R_1.

The upper trip voltage V_{A2} is defined as Equation 2.

$$V_{A2} = V_{CC} (R_2//R_3) / ((R_1 + (R_2//R_3)) \quad (2)$$

The total hysteresis provided by the network is defined as $\Delta V_A = V_{A1} - V_{A2}$, as shown in Equation 3.

$$\Delta V_A = \frac{+V_{CC}R_1R_2}{R_1R_2 + R_1R_3 + R_2R_3} \quad (3)$$

Device Functional Modes (continued)

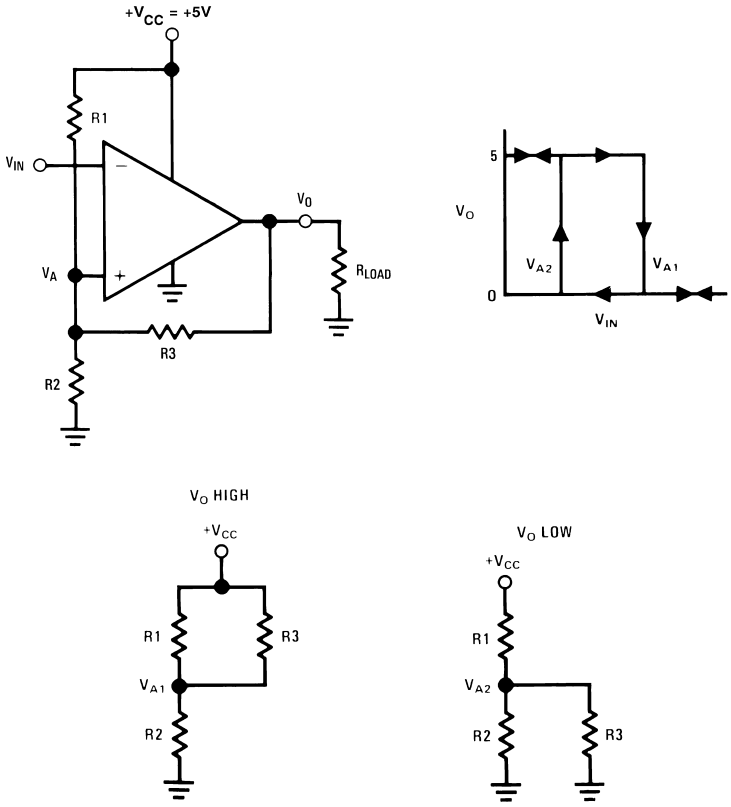


Figure 31. Inverting Comparator With Hysteresis

7.4.5 Noninverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1} where V_{IN1} is calculated by Equation 4.

$$V_{IN1} = \frac{V_{REF}(R_1 + R_2)}{R_2} \tag{4}$$

As soon as V_O switches to V_{CC}, V_A steps to a value greater than V_{REF}, which is given by Equation 5.

$$V_A = V_{IN} + \frac{(V_{CC} - V_{IN1})\,R_1}{R_1 + R_2} \tag{5}$$

To make the comparator switch back to its low state, V_{IN} must equal V_{REF} before V_A again equals V_{REF}. V_{IN2} can be calculated by Equation 6.

$$V_{IN2} = \frac{V_{REF}(R_1 + R_2) - V_{CC}\,R_1}{R_2} \tag{6}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in Equation 7.

$$\Delta V_{IN} = V_{CC}R_1/R_2 \tag{7}$$

Device Functional Modes (continued)

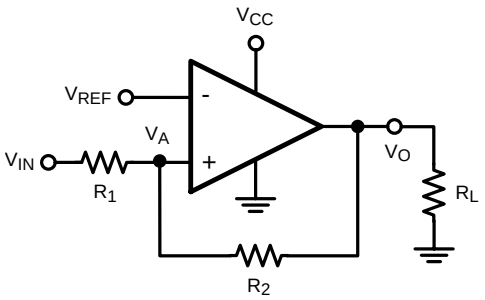


Figure 32. Noninverting Comparator With Hysteresis

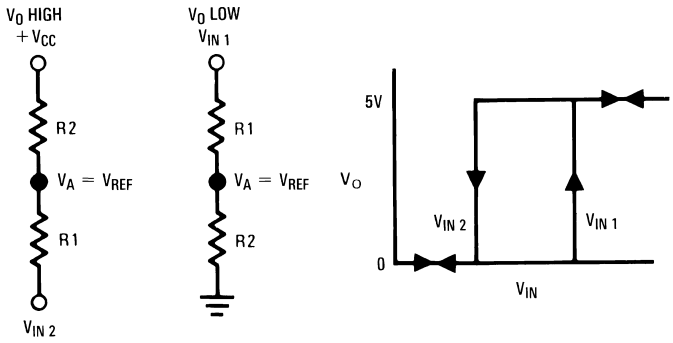


Figure 33. Noninverting Comparator With Hysteresis

7.4.6 Zero Crossing Detector

In a zero crossing detector circuit, the inverting input is connected to ground and the noninverting input is connected to a 100-mV_{PP} AC signal. As the signal at the noninverting input crosses 0 V, the comparator's output changes state.

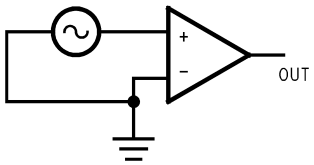


Figure 34. Zero Crossing Detector

To improve switching times and to center the input threshold to ground a small amount of positive feedback is added to the circuit. The voltage divider, R_4 and R_5, establishes a reference voltage, V_1, at the positive input. By making the series resistance, R_1 plus R_2 equal to R_5, the switching condition, $V_1 = V_2$, is satisfied when $V_{IN} = 0$. The positive feedback resistor, R_6, is made very large with respect to R_5 ($R_6 = 2000\ R_5$). The resultant hysteresis established by this network is very small ($\Delta V_1 < 10$ mV) but it is sufficient to insure rapid output voltage transitions. Diode D_1 is used to insure that the inverting input terminal of the comparator never goes below approximately −100 mV. As the input terminal goes negative, D_1 will forward bias, clamping the node between R_1 and R_2 to approximately −700 mV. This sets up a voltage divider with R_2 and R_3 preventing V_2 from going below ground. The maximum negative input overdrive is limited by the current handling ability of D_1.

Device Functional Modes (continued)

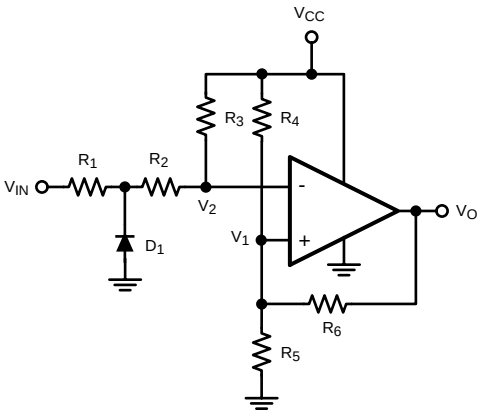


Figure 35. Zero Crossing Detector With Positive Feedback

7.4.7 Threshold Detector

Instead of tying the inverting input to 0 V, the inverting input can be tied to a reference voltage. As the input on the noninverting input passes the V_{REF} threshold, the comparator's output changes state. It is important to use a stable reference voltage to ensure a consistent switching point.

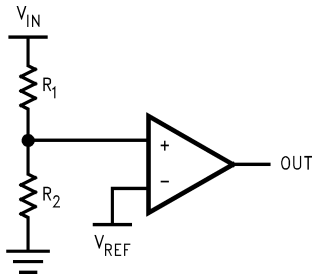


Figure 36. Threshold Detector

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LPV7215 is an ultra-low-power comparator with a typical power supply current of 580 nA. It has the best-in-class power supply current versus propagation delay performance available among TI's low-power comparators. The propagation delay is as low as 4.5 µs with 100-mV overdrive at 1.8-V supply.

8.2 Typical Applications

8.2.1 Square Wave Generator

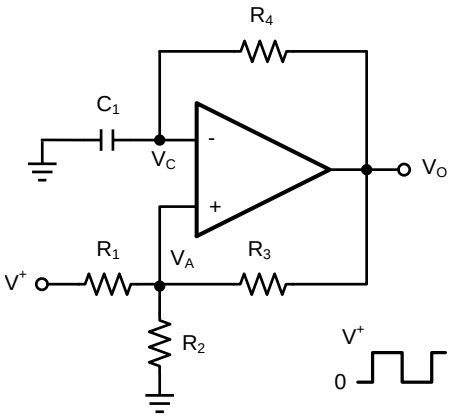


Figure 37. Square Wave Generator Schematic

8.2.1.1 Design Requirements

A typical application for a comparator is as a square wave oscillator. The circuit in Figure 38 generates a square wave whose period is set by the RC time constant of the capacitor C_1 and resistor R_4. The maximum frequency is limited by the large signal propagation delay of the comparator and by the capacitive loading at the output, which limits the output slew rate.

8.2.1.2 Detailed Design Procedure

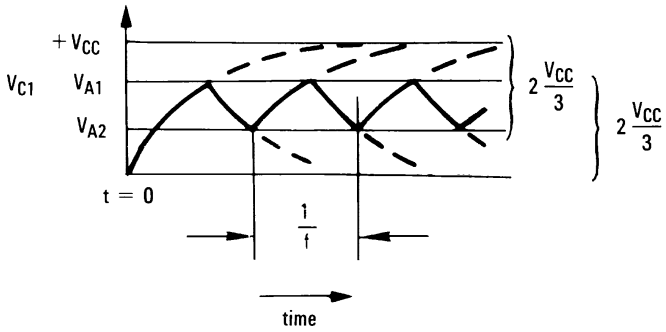


Figure 38. Square Wave Oscillator

Typical Applications (continued)

Consider the output of Figure 38 to be high to analyze the circuit. That implies that the inverted input (V_C) is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at this point is in Equation 8.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \,||\, R_3} \tag{8}$$

If $R_1 = R_2 = R_3$ then $V_{A1} = 2\ V_{CC}/3$

At this point the comparator switches pulling down the output to the negative rail. The value of V_A at this point, as shown in Equation 9:

$$V_{A2} = \frac{V_{CC}(R_2 \,||\, R_3)}{R_1 + (R_2 \,||\, R_3)} \tag{9}$$

If $R_1 = R_2 = R_3$ then $V_{A2} = V_{CC}/3$

The capacitor C_1 now discharges through R_4, and the voltage V_C decreases until it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2\ V_{CC}/3$ to $V_{CC}/3$, which is given by $R_4C_1 \times \ln 2$. Hence the formula for the frequency is given by Equation 10:

$$F = 1/(2 \times R_4 \times C_1 \times \ln 2) \tag{10}$$

8.2.1.3 Application Curves

Figure 39 shows the simulated results of an oscillator using the following values:

1. $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
2. $C_1 = 100$ pF, $C_L = 20$ pF
3. V+ = 5 V, V– = GND
4. C_{STRAY} (not shown) from V_a to GND = 10 pF

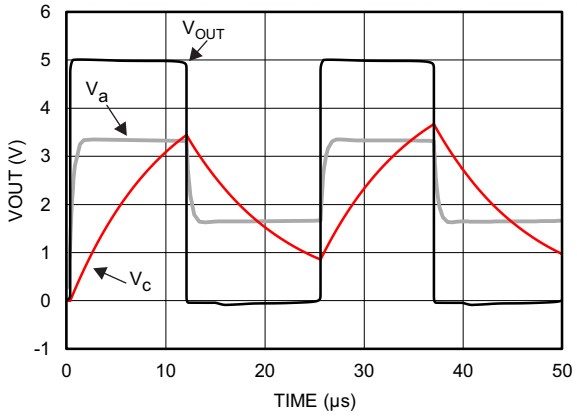


Figure 39. Square Wave Oscillator Output Waveform

Typical Applications (continued)

8.2.2 Window Detector

A window detector monitors the input signal to determine if it falls between two voltage levels.

The comparator outputs A and B are high only when $V_{REF1} < V_{IN} < V_{REF2}$ or *within the window*. These are defined as:

$$V_{REF1} = R_3 / (R_1 + R_2 + R_3) \times V^+ \quad (11)$$

$$V_{REF2} = (R_2 + R_3) / (R_1 + R_2 + R_3) \times V^+ \quad (12)$$

Others names for window detectors are: threshold detector, level detectors, and amplitude trigger or detector.

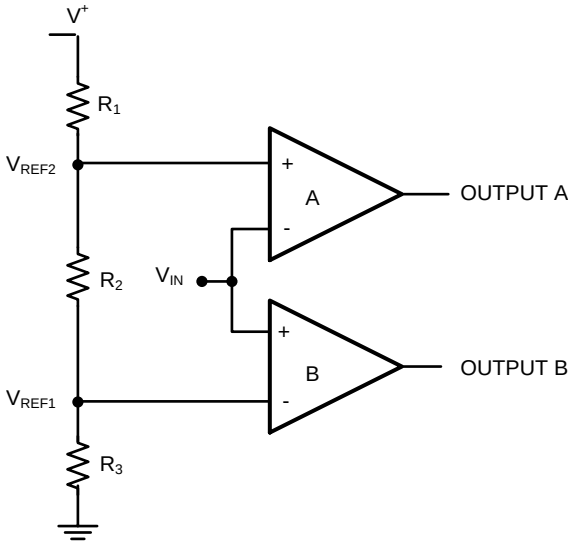


Figure 40. Window Detector

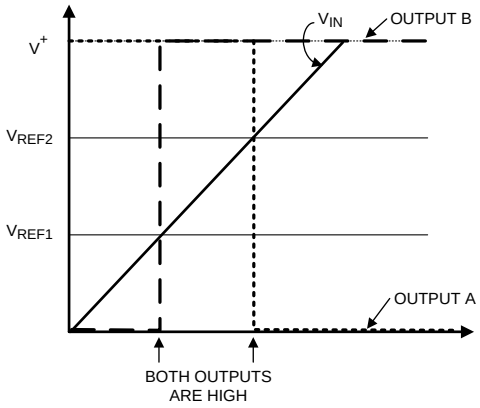


Figure 41. Window Detector Output Signal

Typical Applications (continued)

8.2.3 Crystal Oscillator

A simple crystal oscillator using the LPV7215 is shown in Figure 42. Resistors R_1 and R_2 set the bias point at the comparator's noninverting input. Resistors, R_3 and R_4 and capacitor C_1 set the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. The output duty cycle for this circuit is roughly 50%, but it is affected by resistor tolerances and to a lesser extent by the comparator offset.

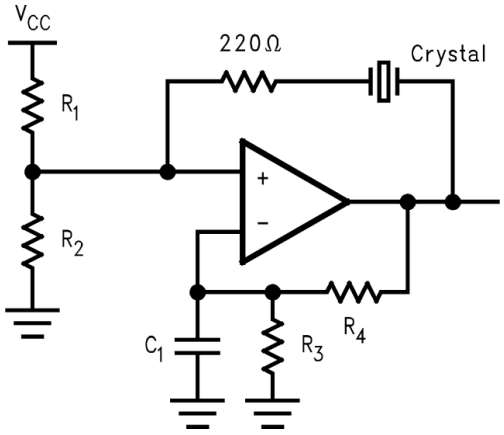


Figure 42. Crystal Oscillator

8.2.4 IR Receiver

The LPV7215 can also be used as an infrared receiver. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across R_D. When this voltage level crosses the voltage applied by the voltage divider to the inverting input, the output transitions.

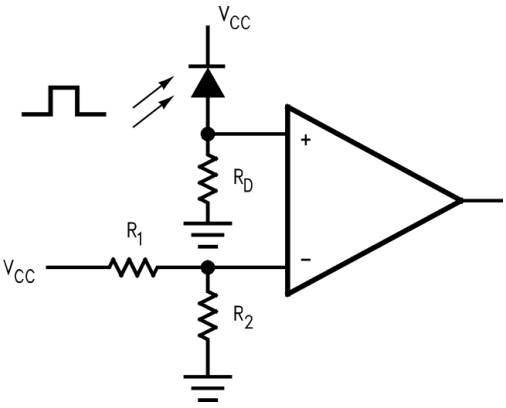


Figure 43. IR Receiver

9 Power Supply Recommendations

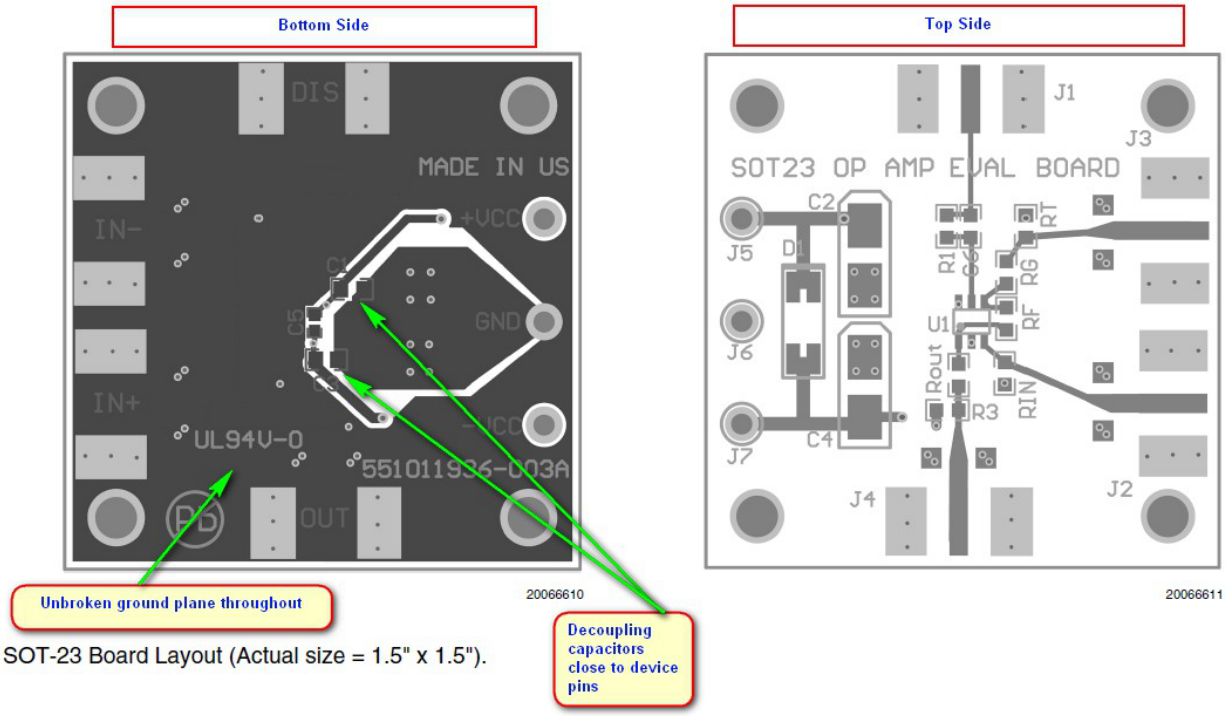
Comparators are very sensitive to input noise. To minimize supply noise, power supplies must be capacitively decoupled by a 0.01-µF ceramic capacitor in parallel with a 10-µF electrolytic capacitor.

10 Layout

10.1 Layout Guidelines

Proper grounding and the use of a ground plane help ensure the specified performance of the LPV7215. Minimizing trace lengths, reducing unwanted parasitic capacitance and using surface-mount components also helps.

10.2 Layout Example



SOT-23 Board Layout (Actual size = 1.5" x 1.5").

Figure 44. LPV7215 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

DIP Adapter Evaluation Module, http://www.ti.com/tool/dip-adapter-evm

TI Universal Operational Amplifier Evaluation Module, http://www.ti.com/tool/opampevm

11.1.2 Documentation Support

11.1.2.1 Related Documentation

For related documentation, see the following

AN-74 - A Quad of Independently Functioning Comparators (SNOA654).

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPV7215MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C30A	Samples
LPV7215MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C30A	Samples
LPV7215MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C37	Samples
LPV7215MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C37	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

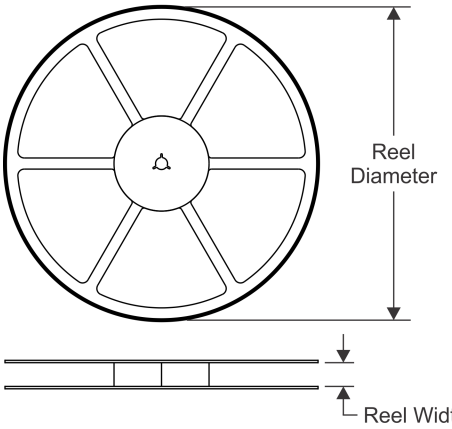
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

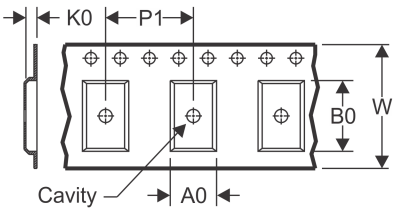
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

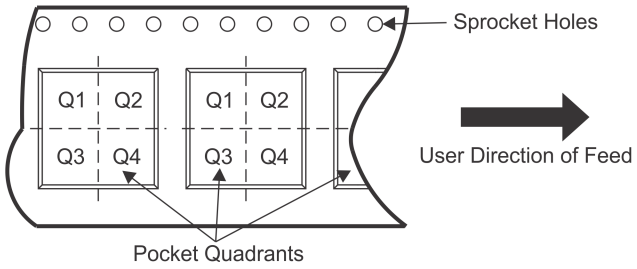


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

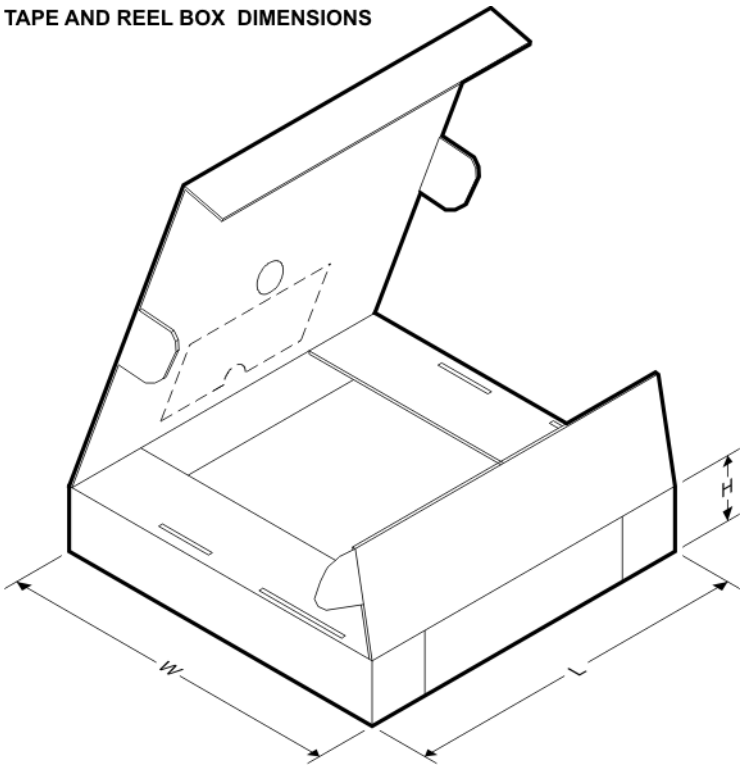
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV7215MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV7215MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV7215MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV7215MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

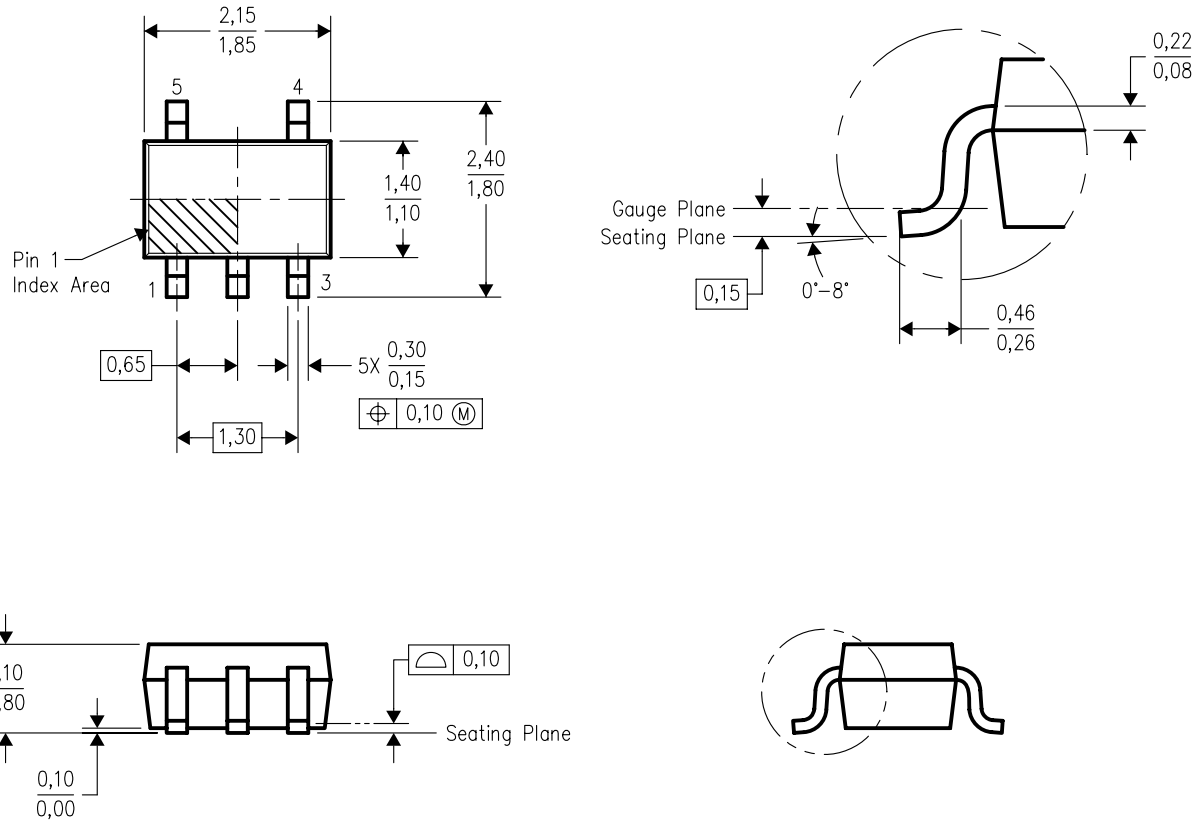
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV7215MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LPV7215MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LPV7215MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LPV7215MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0

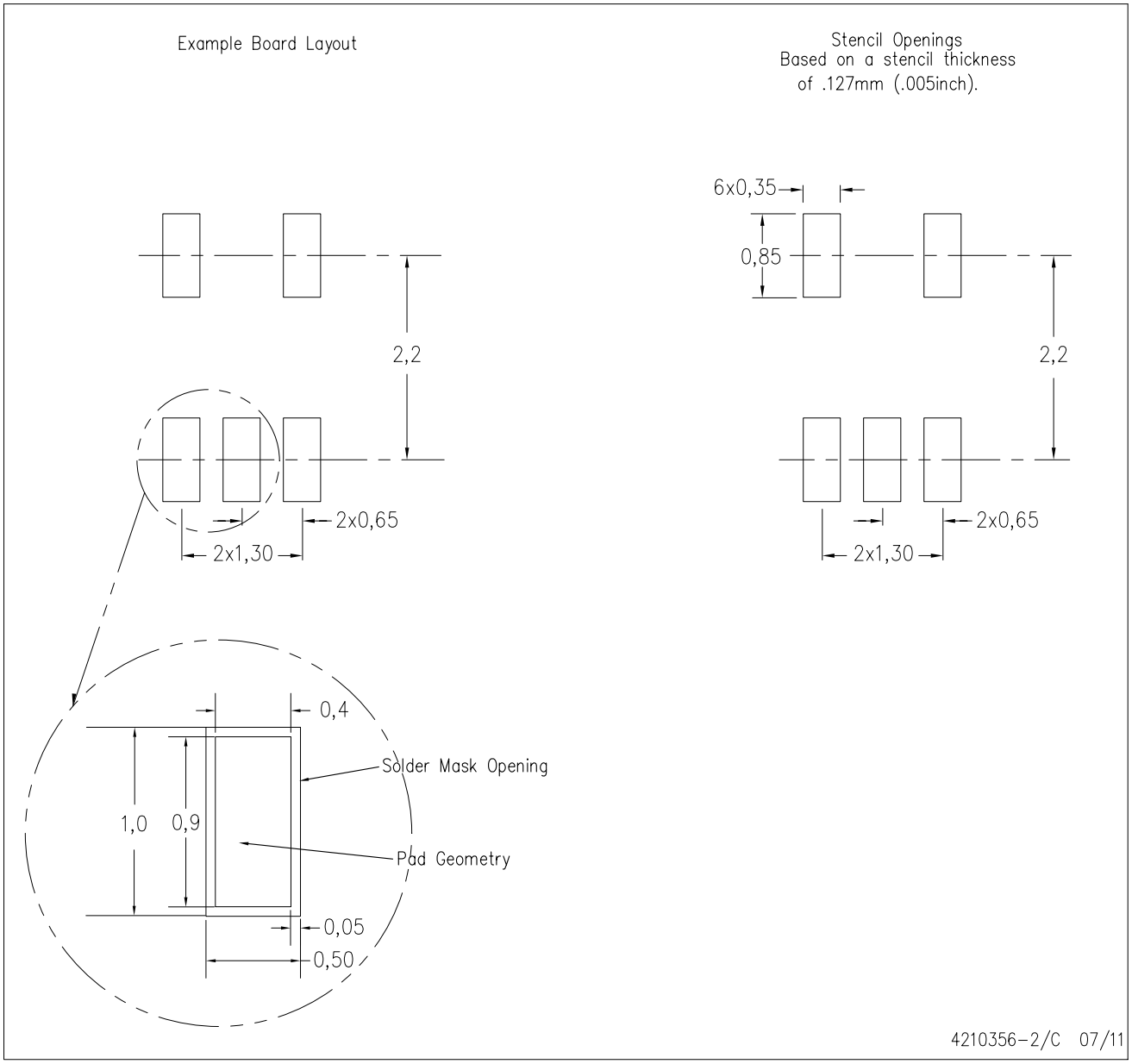
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



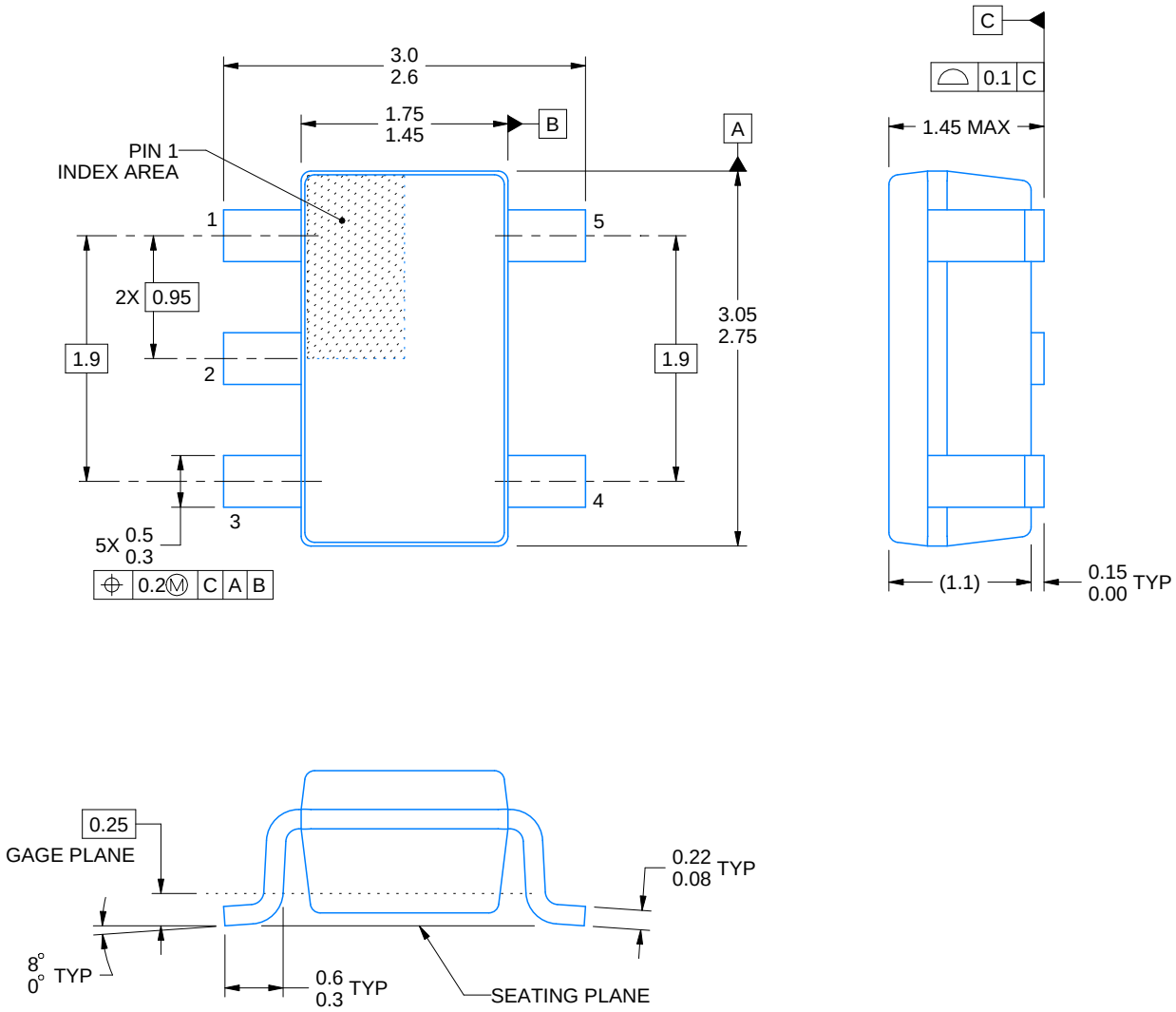
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

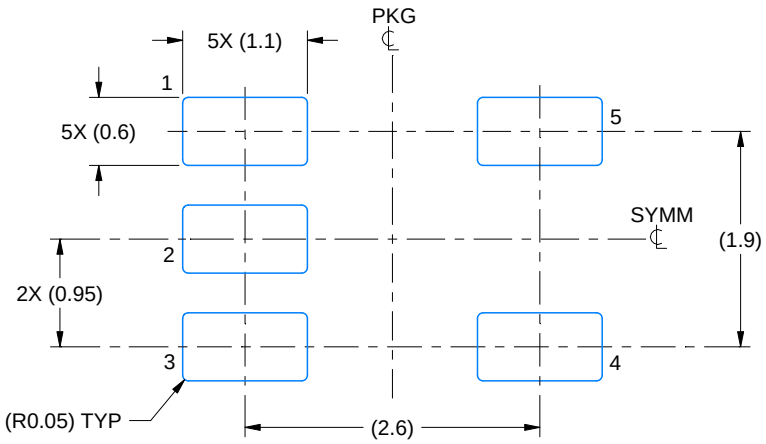
SMALL OUTLINE TRANSISTOR



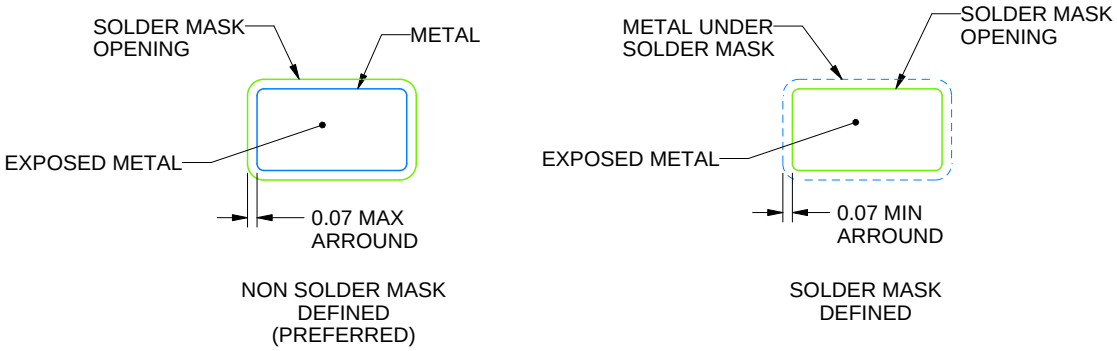
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

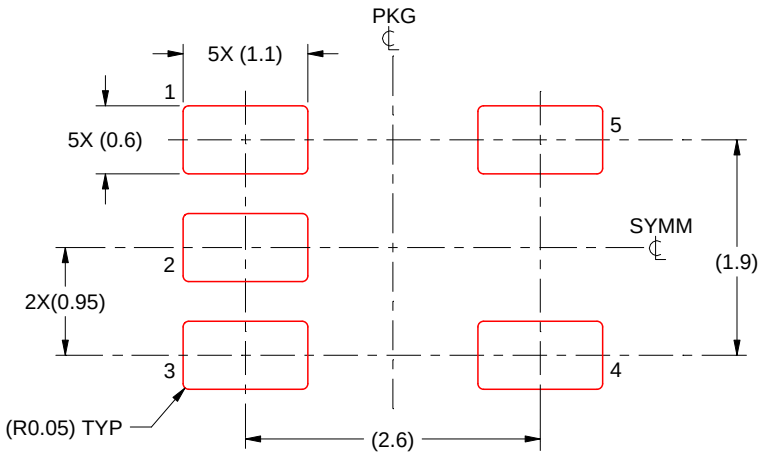


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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