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Table 4. Pin description *…continued*

Pin names with prefix m are multiplexed pins. See Table 11 for pin function selection of multiplexed pins.

TFBGA pin name	TFBGA ball	Digital I/O level [1]	Application function	Pin state after reset [2]	Cell type [3]	Description
ADC_VREFN	R16	-	AI		AIO2	ADC negative reference voltage
ADC_VREFP	T17	-	AI		AIO2	ADC positive reference voltage
ADC_VDDA18	N15	SUP2	Supply		CS1	ADC digital voltage supply
ADC_VDDA33	N14	SUP3	Supply		CS1	ADC analog voltage supply
ADC_GNDA	N16	-	Ground		CG1	ADC analog ground
Audio Stereo DAC						
DAC_VDDA33	C14	SUP3	Supply		CS1	SDAC analog supply
DAC_VREFP	F16	SUP3	AI		AIO2	SDAC positive reference voltage
DAC_VREFN	F15	-	AI		AIO2	SDAC negative reference voltage
Class AB amplifier						
HP_OUTC	D14	-	AO		AIO2	Headphone common output reference for Class AB
HP_FCL	C16	-	AI		AIO2	Headphone filter capacitor left
HP_FCR	B15	-	AI		AIO2	Headphone filter capacitor right
HP_VREF	E14	-	AI		AIO2	Analog reference supply for headphone and DAC
HP_OUTL	B17	-	AO		AIO2	Headphone left output
HP_OUTR	C15	-	AO		AIO2	Headphone right output
HP_VDDA33	A16	SUP3	Supply		CS1	Headphone analog supply Class AB
HP_GNDA	B16	-	Ground		CG1	Headphone analog ground
USB HS 2.0 OTG						
USB_VBUS	N3	SUP5	AI		AIO3	USB supply detection line
USB_ID	P3	SUP3	AI		AIO1	Indicates to the USB transceiver whether in device (USB_ID HIGH) or host (USB_ID LOW) mode (contains internal pull-up resistor)
USB_RREF	N4	SUP3	AIO		AIO1	USB connection for external reference resistor (12 kΩ +/- 1%) to analog ground supply
USB_DP	T1	SUP3	AIO		AIO1	USB D+ connection with integrated 45 Ω termination resistor
USB_DM	R1	SUP3	AIO		AIO1	USB D− connection with integrated 45 Ω termination resistor
USB_VDDA12_PLL	N2	SUP1	Supply		PS3	USB PLL supply
USB_VDDA33_DRV	T3	SUP3	Supply		PS3	USB analog supply for driver
USB_VDDA33	R3	SUP3	Supply		PS3	USB analog supply for PHY
USB_VSSA_TERM	R2	-	Ground		CG1	USB analog ground for clean reference for on chip termination resistors
USB_GNDA	T2	-	Ground		CG1	USB analog ground
USB_VSSA_REF	P2	-	Ground		CG1	USB analog ground for clean reference

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Table 4. Pin description *…continued*

Pin names with prefix m are multiplexed pins. See Table 11 for pin function selection of multiplexed pins.

TFBGA pin name	TFBGA ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
I2SRX_BCK0[4]	T9	SUP3	DIO / GPIO	I	DIO1	I^2S input bitclock
I2SRX_WS0[4]	R9	SUP3	DIO / GPIO	I	DIO1	I^2S input word select
I^2S/Digital audio output						
mI2STX_DATA0[4]	T13	SUP3	DO / GPIO	O	DIO1	I^2S output serial data out
mI2STX_BCK0[4]	T12	SUP3	DO / GPIO	O	DIO1	I^2S output bitclock
mI2STX_WS0[4]	R12	SUP3	DO / GPIO	O	DIO1	I^2S output word select
mI2STX_CLK0[4]	T11	SUP3	DO / GPIO	O	DIO1	I^2S output serial clock
General Purpose IO (IOCONFIG module)						
GPIO0[8]	R13	SUP3	GPIO	I:PD	DIO1	General Purpose IO pin 0 (mode pin 0)
GPIO1[8]	T14	SUP3	GPIO	I:PD	DIO1	General Purpose IO pin 1 (mode pin 1)
GPIO2[8]	P12	SUP3	GPIO	I	DIO1	General Purpose IO pin 2 (mode pin 2/blinking LED)
GPIO3	D12	SUP3	GPIO	I	DIO1	General Purpose IO pin 3 (connect to PSU_STOP)[5]
GPIO4	D11	SUP3	GPI	I	DIO1	General Purpose Input pin 4
mGPIO5[4]	D7	SUP3	GPIO	I	DIO4	General Purpose IO pin 5
mGPIO6[4]	B7	SUP3	GPIO	I	DIO4	General Purpose IO pin 6
mGPIO7[4]	C7	SUP3	GPIO	I	DIO4	General Purpose IO pin 7
mGPIO8[4]	D6	SUP3	GPIO	I	DIO4	General Purpose IO pin 8
mGPIO9[4]	B6	SUP3	GPIO	I	DIO4	General Purpose IO pin 9
mGPIO10[4]	C6	SUP3	GPIO	I	DIO4	General Purpose IO pin 10
External Bus Interface (NAND flash controller)						
EBI_A_0_ALE[4]	C4	SUP4	DO	O	DIO4	EBI Address Latch Enable (ALE)
EBI_A_1_CLE[4]	A2	SUP4	DO	O	DIO4	EBI Command Latch Enable (CLE)
EBI_D_0[4]	J3	SUP4	DIO	I	DIO4	EBI Data I/O 0
EBI_D_1[4]	H3	SUP4	DIO	I	DIO4	EBI Data I/O 1
EBI_D_2[4]	H4	SUP4	DIO	I	DIO4	EBI Data I/O 2
EBI_D_3[4]	G4	SUP4	DIO	I	DIO4	EBI Data I/O 3
EBI_D_4[4]	F4	SUP4	DIO	I	DIO4	EBI Data I/O 4
EBI_D_5[4]	F3	SUP4	DIO	I	DIO4	EBI Data I/O 5
EBI_D_6[4]	E4	SUP4	DIO	I	DIO4	EBI Data I/O 6
EBI_D_7[4]	E3	SUP4	DIO	I	DIO4	EBI Data I/O 7
EBI_D_8[4]	D3	SUP4	DIO	I	DIO4	EBI Data I/O 8
EBI_D_9[4]	A3	SUP4	DIO	I	DIO4	EBI Data I/O 9
EBI_D_10[4]	C2	SUP4	DIO	I	DIO4	EBI Data I/O 10
EBI_D_11[4]	D2	SUP4	DIO	I	DIO4	EBI Data I/O 11
EBI_D_12[4]	E2	SUP4	DIO	I	DIO4	EBI Data I/O 12
EBI_D_13[4]	F2	SUP4	DIO	I	DIO4	EBI Data I/O 13

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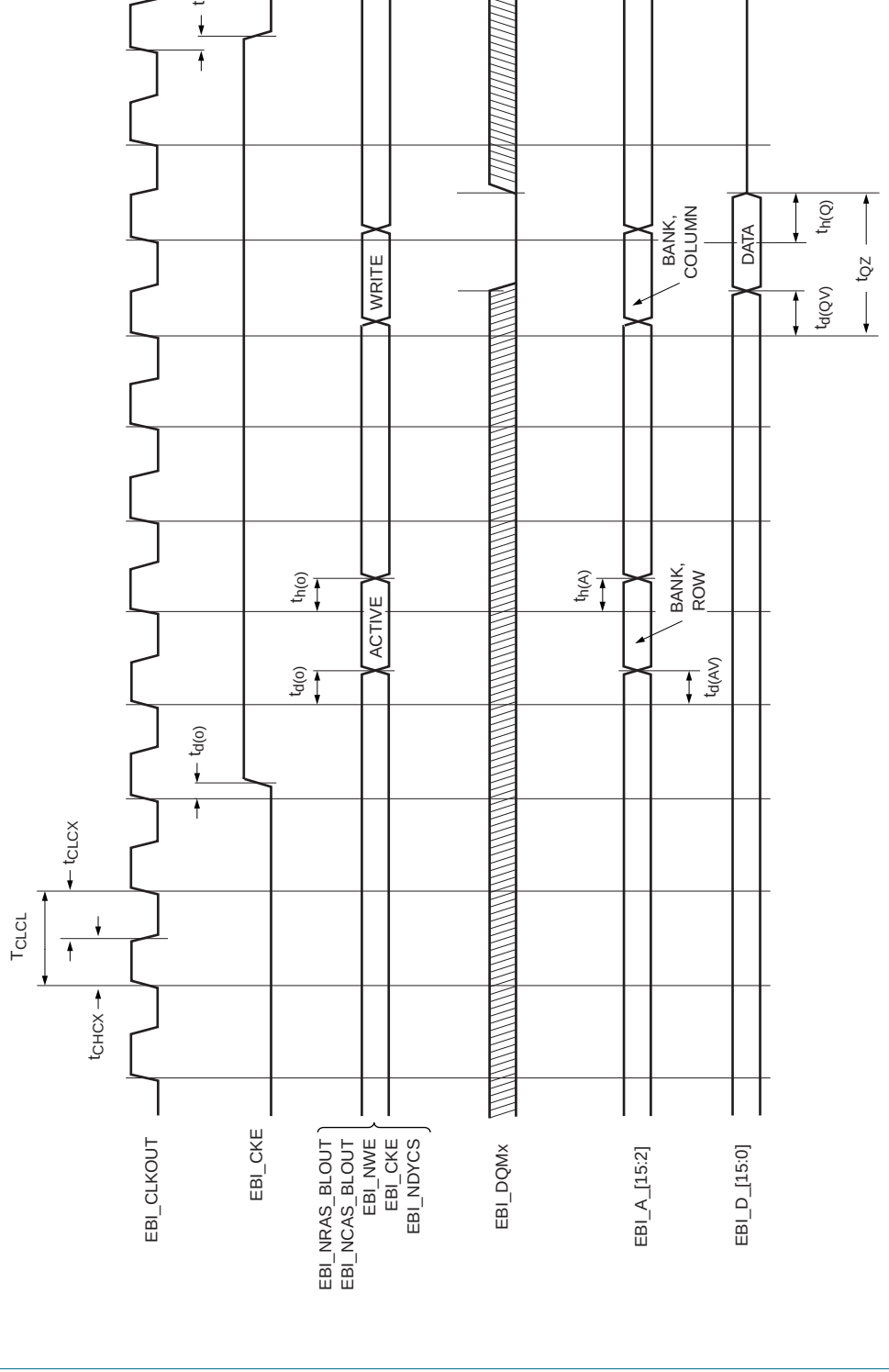

Fig 24. SDRAM bank activate and write timing

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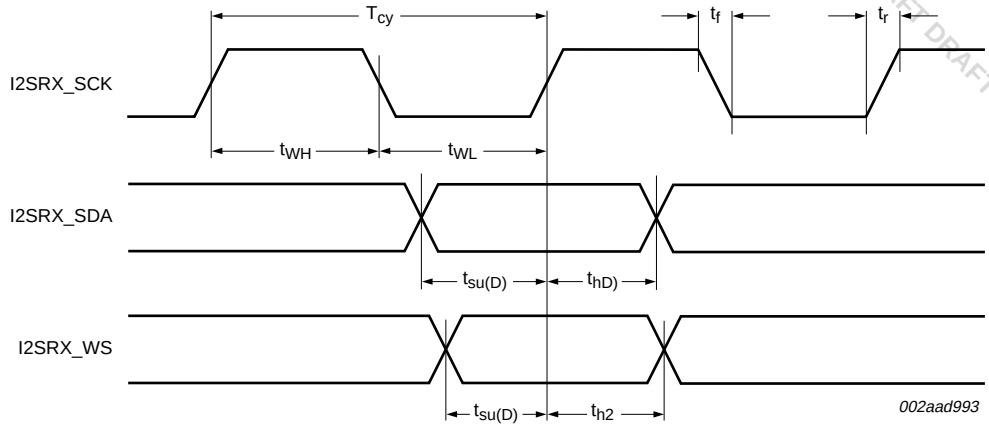

Fig 32. I²S-bus timing (input)

10.2.4 I²C-bus

Table 31. Dynamic characteristic: I²C-bus pins

T_{amb} = −40 °C to +85 °C.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{SCL}	SCL clock frequency	Standard mode	0	<tbd>	100	kHz
		Fast mode	0	<tbd>	400	kHz
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	20 + 0.1 × C_b[3]	-	-	ns
t_r	rise time	Standard mode	<tbd>	<tbd>	1000	ns
		Fast mode	20 + 0.1 × C_b[3]	<tbd>	300	ns
t_f	fall time	Standard mode	<tbd>	<tbd>	300	ns
		Fast mode	20 + 0.1 × C_b[3]	<tbd>	300	ns
t_{BUF}	bus free time between a STOP and START condition	-	<tbd>	<tbd>	<tbd>	
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7	<tbd>	<tbd>	µs
		Fast mode	1.3	<tbd>	<tbd>	µs
$t_{HD;STA}$	hold time (repeated) START condition	-	<tbd>	<tbd>	<tbd>	
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0	<tbd>	<tbd>	µs
		Fast mode	0.6	<tbd>	<tbd>	µs
$t_{SU;DAT}$	data set-up time	Standard mode	250	<tbd>	<tbd>	ns
		Fast mode	100	<tbd>	<tbd>	ns
$t_{SU;STA}$	set-up time for a repeated START condition	-	<tbd>	<tbd>	<tbd>	
$t_{SU;STO}$	set-up time for STOP condition	Standard mode	4.0	<tbd>	<tbd>	µs
		Fast mode	0.6	<tbd>	<tbd>	µs

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

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11. Application information

Table 36. LCD panel connections

TFBGA pin #	Pin name	Reset function (default)	LCD mode				
			Parallel				
			LCD panel data mapping			Control function	
			16 bit	8 bit	4 bit	6800	8080
R8	mLCD_CSB/EBI_NSTCS_0	LCD_CSB	-	-	-	LCD_CSB	LCD_CSB
P7	mLCD_E_RD/EBI_CKE	LCD_E_RD	-	-	-	LCD_E	LCD_RD
R7	mLCD_RS/EBI_NDYCS	LCD_RS	-	-	-	LCD_RS	LCD_RS
T8	mLCD_RW_WR/EBI_DQM_1	LCD_RW_WR	-	-	-	LCD_RW	LCD_WR
T7	mLCD_DB_0/EBI_CLKOUT	LCD_DB_0	LCD_DB_0	-	-	-	-
P8	mLCD_DB_1/EBI_NSTCS_1	LCD_DB_1	LCD_DB_1	-	-	-	-
T6	mLCD_DB_2/EBI_A_2	LCD_DB_2	LCD_DB_2	-	-	-	-
R6	mLCD_DB_3/EBI_A_3	LCD_DB_3	LCD_DB_3	-	-	-	-
U6	mLCD_DB_4/EBI_A_4	LCD_DB_4	LCD_DB_4	-	-	-	-
P6	mLCD_DB_5/EBI_A_5	LCD_DB_5	LCD_DB_5	-	-	-	-
R5	mLCD_DB_6/EBI_A_6	LCD_DB_6	LCD_DB_6	-	-	-	-
T5	mLCD_DB_7/EBI_A_7	LCD_DB_7	LCD_DB_7	-	-	-	-
U5	mLCD_DB_8/EBI_A_8	LCD_DB_8	LCD_DB_8	LCD_DB_0	-	-	-
P5	mLCD_DB_9/EBI_A_9	LCD_DB_9	LCD_DB_9	LCD_DB_1	-	-	-
P4	mLCD_DB_10/EBI_A_10	LCD_DB_10	LCD_DB_10	LCD_DB_2	-	-	-
U4	mLCD_DB_11/EBI_A_11	LCD_DB_11	LCD_DB_11	LCD_DB_3	-	-	-
T4	mLCD_DB_12/EBI_A_12	LCD_DB_12	LCD_DB_12	LCD_DB_4	LCD_DB_0	-	-
U3	mLCD_DB_13/EBI_A_13	LCD_DB_13	LCD_DB_13	LCD_DB_5	LCD_DB_1	-	-
U2	mLCD_DB_14/EBI_A_14	LCD_DB_14	LCD_DB_14	LCD_DB_6	LCD_DB_2	-	-
R4	mLCD_DB_15/EBI_A_15	LCD_DB_15	LCD_DB_15	LCD_DB_7	LCD_DB_3	-	-

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