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LP8765RLE

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National Semiconductor

September 7, 2011

LP8765

High Performance Power Management Unit for Handset Applications

General Description

The LP8765 is a complete Power Management Unit (PMU) designed for handset applications. The LP8765 PMU contains a 28V Over-Voltage Protection (OVP) single-input linear Li-Ion battery charger, backup battery charger, 10 low-dropout voltage regulators including 4 A-type LDOs, 4 D-type LDOs, one LILO LDO and one 28V OVP LDO, 2 high-efficiency buck regulators, 2 comparators, 3 current sinks, 12-bit ADC, real-time clock, 32 KHz OSC and one 2.5V reference output voltage. Programming is handled via a high-speed serial interface to program on/off conditions and output voltages of individual regulators, and to read status information of the PMU.

The LP8765 can safely charge and maintain a single cell Li-Ion battery operating from an AC adapter or USB power source.

The Li-Ion charger requires few external components and integrates the power FET. Charging is thermally regulated to obtain the most efficient charging rate for a given ambient temperature.

A built-in OVP circuit at the charger inputs protects the PMU from input voltages up to +28V, eliminating the need for any external protection circuitry.

Buck regulators have an automatic switch to PFM mode at low-load conditions providing very good efficiency at low-output currents.

A-type LDO regulators provide excellent PSRR and very low noise, 10 µV typ., ideally suited for supplying voltage to RF section.

The real-time clock/calendar provides time interval information as well as two programmable alarms.

The current sink provides 4-bit current resolution with 6-bit PWM dimming, up to 120 mA maximum load current.

Two general-purpose comparators can be used for detecting external accessories like ear plugs, etc.

Features

- Linear Li-Ion Battery Charger with Single Input
  - 50 mA to 1200 mA Charging Current
  - 4.05V to 4.75V Termination Voltage
  - 28V OVP on the VIN_CHG Input
  - Charging from either AC Adaptor or USB
- Two Synchronous Magnetic Buck Regulators
  - I_{OUT} 600 mA and 500 mA
  - High-efficiency PFM mode @ low I_{OUT}
  - Auto-Mode PFM/PWM Switch
  - Programmable Peak Switching Current Limit
  - Low-Inductance 2.2 µH @2 MHz Switching Frequency
  - 3% Accurate Buck Regulators up to 90% Efficiency
- LDOs
  - 4 x A-type LDOs (3 x 200 mA, 1 x 100 mA)
  - 4 x D-type LDOs (2 x 200 mA, 1 x 300 mA, 1 x 400 mA)
  - 1 x LILO LDO (1 x 300 mA)
  - 1 x 28V OVP LDO for USB Transceiver (1 x 10 mA)
  - 10 µV noise on A-type LDOs
  - 2% typ. Output Voltage Accuracy on LDOs
- 12-bit A/D Converter
- Three Controllable Current Sinks
- Two Comparators
- Interrupt Request to Reduce S/W Polling
- 32.786 KHz OSC
- Real-Time Clock with Two Programmable Alarms
- Thermal Shutdown with Early Warning Alarm
- 49-bump micro SMD package 3.7 x 3.7 mm, 0.5 mm pitch

Applications

- GSM, GPRS, EDGE, CDMA & 3G Handsets

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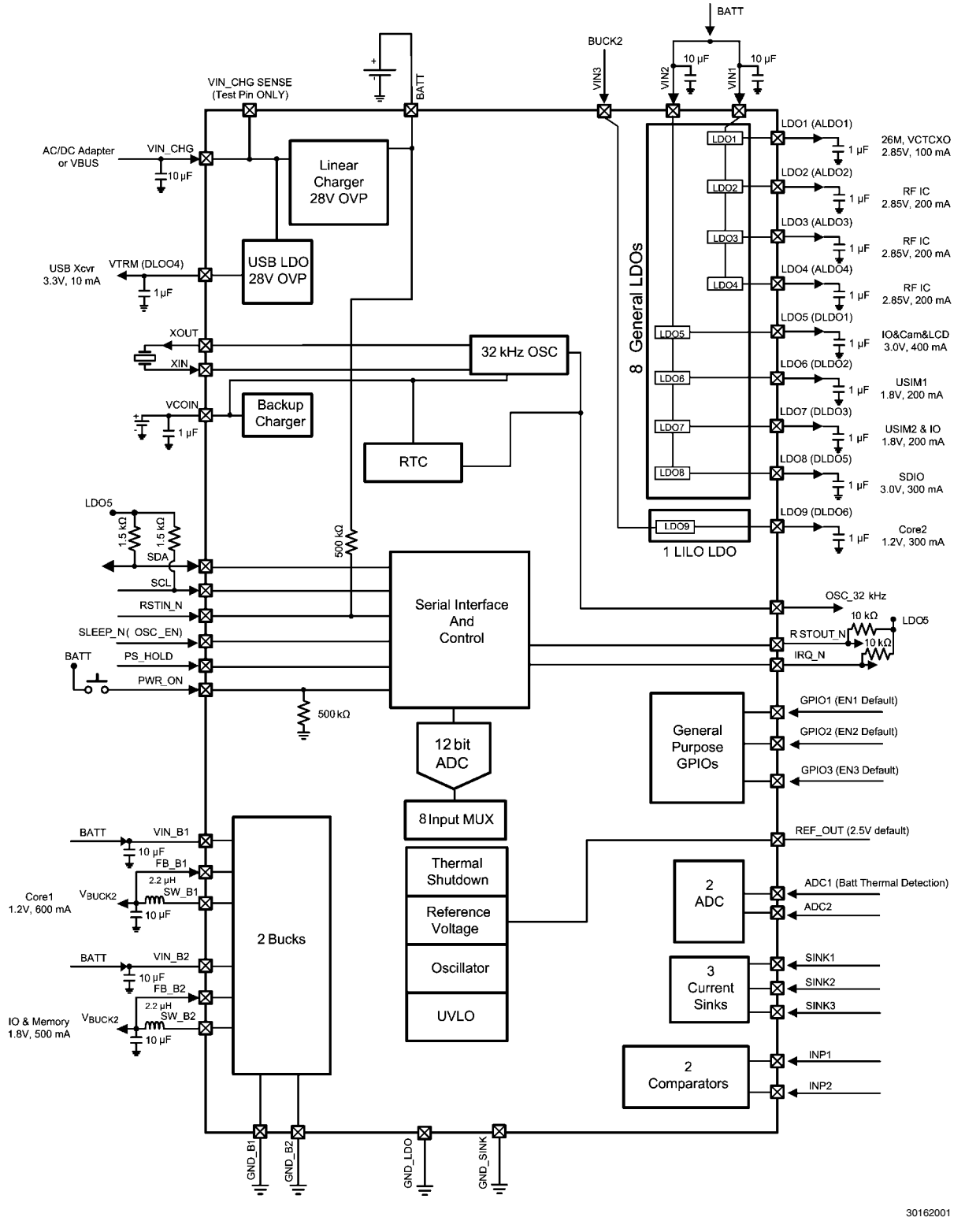
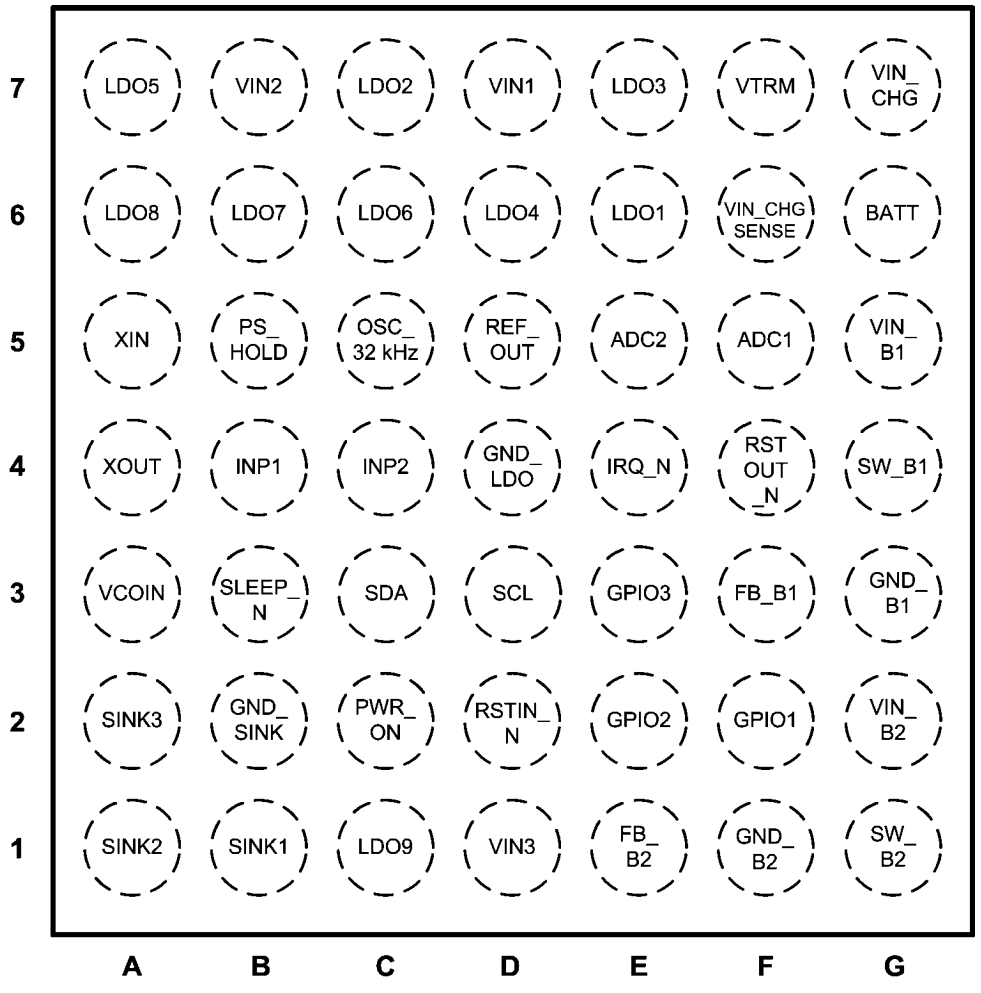
Table of Contents

General Typical Application Diagram

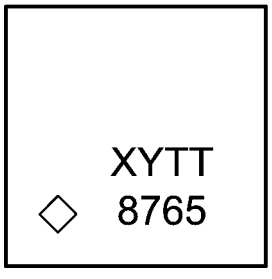


Device Pin Diagram



TOP VIEW
49-Bump (0.5 mm pitch) micro SMDxt Package

Package Marking Information



XY = 2 Digit Date Code
TT = 2 Digit Die Run Trace Code
8765 = Product Identification

◇ = Pin A1

30162003

Ordering Information

Order Number	Package Type	Product ID	Supplied As
LP8765RLE	micro SMD xT	8765	250 Units on Tape & Reel
LP8765RLX			1000 Units onTape & Reel

LP8765 Pin Descriptions

Pin #	Name	Type	Description
F5	ADC1	A	ADC input for Battery thermal NTC thermal monitor, also used for battery detection.
E5	ADC2	A	Reserved Pin for external ADC usage
G6	BATT	P	Main Battery connection
F3	FB_B1	A	Buck1 feedback
E1	FB_B2	A	Buck2 feedback
G3	GND_B1	G	Buck1 GND
F1	GND_B2	G	Buck1 GND
D4	GND_LDO	G	LDOs GND
B2	GND_SINK	G	SINKs GND
F2	GPIO1	DI	Used for Enable1
E2	GPIO2	DI	Used for Enable2
E3	GPIO3	DI	Used for Enable3
B4	INP1	DI	Comparator Input1
C4	INP2	DI	Comparator Input1
E4	IRQ_N	DO	Interrupt output, active low (Open Drain)
E6	LDO1	A	LDO1 output
C7	LDO2	A	LDO2 output
E7	LDO3	A	LDO3 output
D6	LDO4	A	LDO4 output
A7	LDO5	A	LDO5 output
C6	LDO6	A	LDO6 output
B6	LDO7	A	LDO7 output
A6	LDO8	A	LDO8 output
C1	LDO9	A	LDO9 output
C5	OSC_32KHz	A	32 KHz clock buffer output to BB
B5	PS_HOLD	DI	Control input from BB
C2	PWR_ON	DI	Power switch on input
D5	REF_OUT	A	2.5V reference output for ADC (load current should be less than 1mA)
D2	RSTIN_N	DI	Reset input, active low
F4	RSTOUT_N	DO	Reset output, active low (Open Drain)
D3	SCL	DI	Serial interface clock input, external pull up 1.5K to LDO5
C3	SDA	DI/O	Serial interface bi-directional data, external pull up 1.5K to LDO5
B1	SINK1	A	Current Sink1 Input
A1	SINK2	A	Current Sink2 Input
A2	SINK3	A	Current Sink3 Input
B3	SLEEP_N	DI	Sleep Mode input, active low
G4	SW_B1	A	Buck1 switch note
G1	SW_B2	A	Buck2 switch note
A3	VCOIN	A	Backup battery connection
G5	VIN_B1	A	Buck1 input
G2	VIN_B2	A	Buck2 input
G7	VIN_CHG	P	DC power input to charger block (AC adaptor or USB)
F6	VIN_CHG SENSE	DO	VIN_CHG pin testing point (test purpose only) and leave this pin floating.
D7	VIN1	A	LDOs Input1
B7	VIN2	A	LDOs Input2
D1	VIN3	A	LILO LDO input
F7	VTRM	A	3.3V LDO output for USB transceiver

Pin #	Name	Type	Description
A5	XIN	A	External crystal oscillator IN
A4	XOUT	A	External crystal oscillator OUT

A:	Analog Pin	D:	Digital Pin	I:	Input Pin
DI/O:	Digital Input/Output Pin	O:	Output Pin	P:	Power Pin
G:	Ground				

Device Operation Description

OPERATION MODES

POWER-ON-RESET: In POWER-ON RESET mode all internal registers are reset to the default values.

STANDBY: In STANDBY mode all PMU functions are disabled except BB charger, 32 KHz OSC & RTC.

START UP: Startup sequence is triggered by setting Power-on-Switch (PWR_ON) high for 100 ms or connecting a suitable voltage to charger input (VIN_CHG). For RTC ALARM events the startup sequence begins after 2ms delay from the RTC events. During the startup sequence, the 2.5V reference voltage will be powered by either charger block or battery first in order to detect battery existing. If there is a battery and the battery voltage is over OPVM, then the default on regulators (Buck1, Buck2 & LDO5) will be enabled according to a pre-programmed timing pattern. If the regulators are enabled, RSTOUT_N is released, allowing the processor to start up. PS_HOLD must be set high within a programmed timer* (8s max) from the start of STARTUP state; this is true for all startup events except PWR_ON. For PWR_ON startup, PMU stays in POWER ON state when PWR_ON is held high, and the PS_HOLD must be set high before the PWR_ON goes low or Power-on-Switch is released. Otherwise, PMU will go to SHUTDOWN state.

If there is no main battery detected (voltage at ADC1 pin is about 2.4V), PMU will not start the startup sequence. In other modes, the PMU will not enable the charger. If the main battery is removed when PMU is running, then Charger will be disabled immediately to force UVLO shutdown.

If two-pin battery is used then ADC1 pin should be connect to GND through a resistor or floating in order to start up the PMU normally. However, there will be no battery exiting detection.

IDLE: PMU will enter into IDLE mode (normal operating mode) after PS_HOLD signal is asserted by the host processor. IDLE mode will enable all PMU functions that can be controlled by the Serial Interface or direct control inputs. PS_HOLD going low for 10 ms, VDD voltage below UVLO, Chip temperature over TSDH, or a flag failure in a monitored regulator (LDO5) for 10 ms will initiate a SHUTDOWN Sequence.

SLEEP: When BB pulls SLEEP_N pin LOW, the PMU will not do anything except setting BUCKs and LDOs to low-power mode in order to minimize quiescent current if LDOs_LOW_PWR_IN_SLEEP and BUCKs_LOW_PWR_IN_SLEEP bits are set to 1, otherwise both BUCKs and LDOs will stay in normally mode. However, in low-power mode, the summary of total load current of BUCKs or LDOs should stay below 5mA. Buck1 has two preset voltages (BUCK1 NORMAL & BUCK1 SLEEP); BUCK1 output equals BUCK1 SLEEP when SLEEP_N pin is low, and goes back to BUCK1 NORMAL when SLEEP_N is high. By default, BUCK1 SLEEP & NORMAL are same 1.2V. In this mode, only LDO1, LDO2, LDO3, LDO4 and LDO9 can be enabled/disabled through GPIO pins (EN1,2&3). If I^2C communication is disabled during sleep, then for other power regulators, BB need to turn them off through I^2C before SLEEP_N goes to 0. Otherwise, these power regulators will stay on during BB sleep. The condition of going to SHUTDOWN state is the same as in IDLE state. Please see Register Maps for detail.

SHUTDOWN: In this state, RSTOUT_N is pulled low, and all regulators are disabled according to pre-programmed timing pattern (opposite of STARTUP sequence). After this, all registers are reset to default values except address xxxx, then PMU will go to STANDBY state.

SYSTEM RESET: PMU goes to SYSTEM RESET mode if RSTIN_N input has been pulled low for xxms**. There are two different reset methods:

1. Cold reset (EN_RSTIN_SHUTDOWN = high); PMU will go to SHUTDOWN state first and then initiate STARTUP event automatically. PS_HOLD must be high within programmed PS_HOLD timer, otherwise PMU will go to SHUTDOWN state.

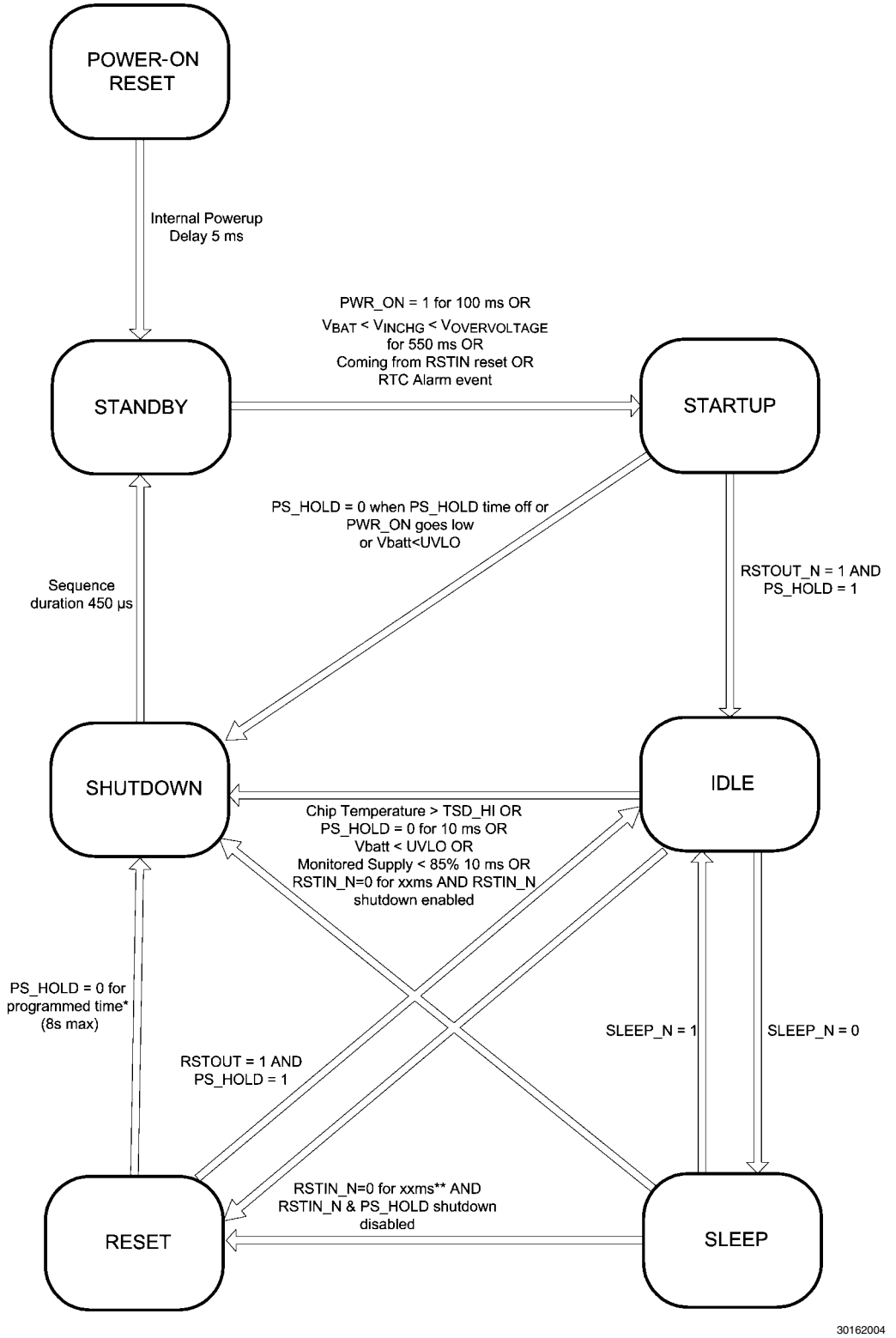
   a. Enable shutdown and enter EPROM READ + PREPARE mode, active the pulldown (Total time = 33 ms);

   b. Disable the pulldown and enter STARTUP mode;

   c. Wait 100 ms; and

   d. Enter Normal working mode.

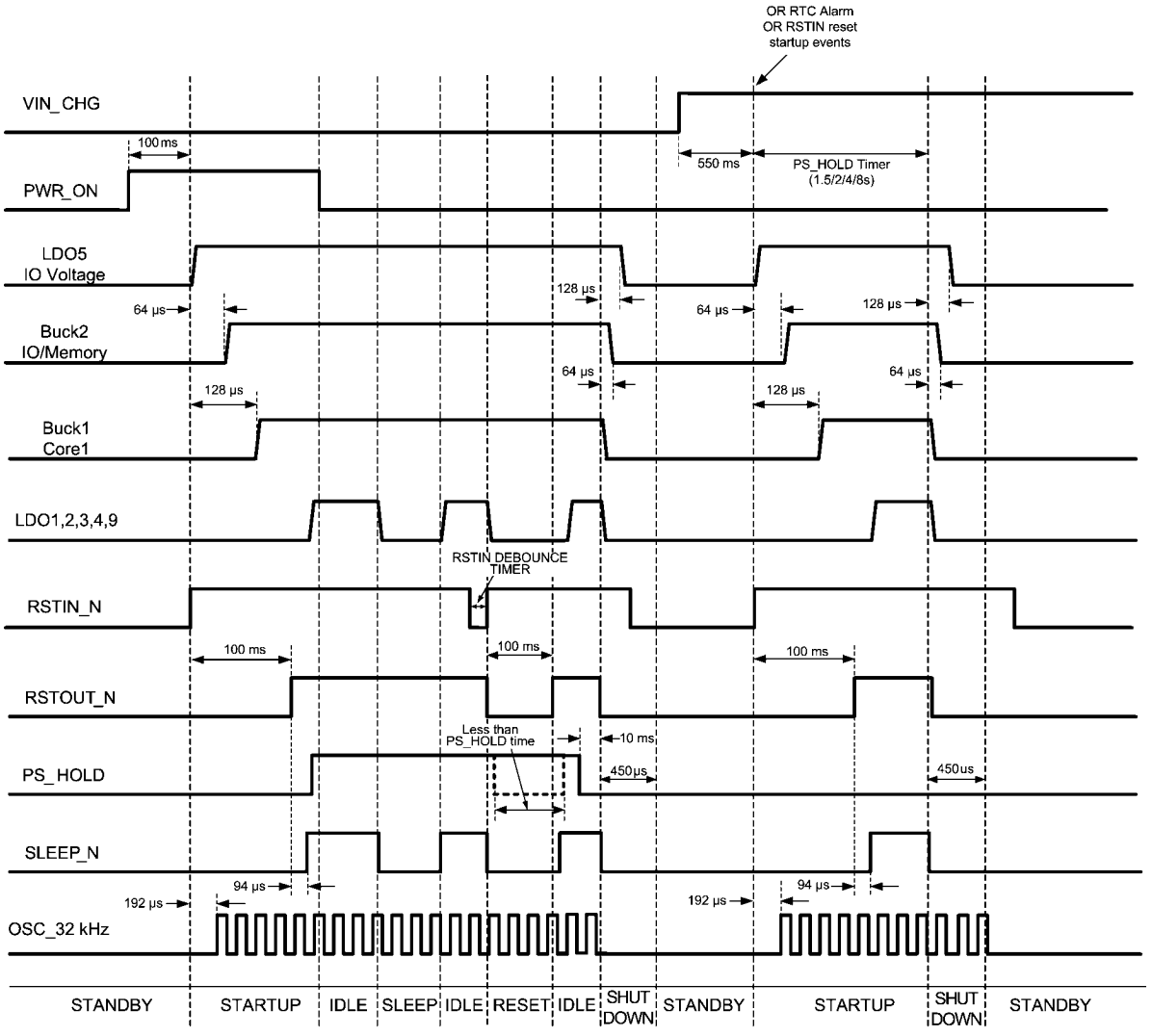
2. Hot reset (EN_RSTIN_SHUTDOWN = low); PMU will pull low RSTOUT_N and disable all the power regulators except BUCK1, BUCK2, LDO5(DLDO1), REF_OUT. A STARTUP event then initiates automatically, and PS_HOLD must be high within programmed PS_HOLD timer, otherwise PMU will go to SHUTDOWN state.



* Note 1: PS_HOLD timer is programmable 1.5s, 2s, 4s, and 8s.

** Note 2: RSTIN_N timer is programmable 0.5 ms, 1.0 ms, 2.0 ms 33 ms.

POWER-ON AND POWER-OFF SEQUENCES



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Default on power rail startup sequence: 2.5V reference voltage→LDO5 → Buck2 → Buck1.

Power-Off sequence is in reverse order of startup sequences.

LP8765 POWER REGULATOR SPEC TABLE

Outputs	Loads	Voltage Range (V)	Default Voltage (V)	Current Rating [mA]	Default ON (Y/N)	Turn-on Sequence	Voltage Steps (mV)	ON/OFF Control
BUCK1	Core1	0.8 - 1.45	1.2	600	Y	T0+128µs	50	S/I(always on)
BUCK2	IO&Memory	0.8 - 2.1	1.8	500	Y	T0+64µs	50	S/I(always on)
LDO1 (ALDO1)	26M, VCTCXO	1.5 - 3.0	2.85	100	N	-	50	S/I AND GPIO1 (EN1)
LDO2 (ALDO2)	RF IC	1.5 - 3.0	2.85	200	N	-	50	S/I AND GPIO1 (EN1)
LDO3 (ALDO3)	RF IC	1.5 - 3.0	2.85	200	N	-	50	S/I OR GPIO1 (EN1)
LDO4 (ALDO4)	RF IC	1.85 - 3.4	2.85	200	N	-	50	S/I AND GPIO2 (EN2)
LDO5 (DLDO1)	IO&Cam&LCD	1.5 - 3.3	3	400	Y	T0	100	S/I(always on)
LDO6 (DLDO2)	USIM1	1.8 or 3.0	1.8	200	N	-	-	S/I
LDO7 (DLDO3)	USIM2&IO	1.5 - 3.3	1.8	200	N	-	100	S/I
VTRM (DLDO4)	USB Xcvr	3.3 fixed	3.3	10	Y	Always as long as the USB/Adaptor plugged	-	S/I
LDO8 (DLDO5)	SDIO	1.5 - 3.3	3	300	N	-	100	S/I
LDO9 (DLDO6)	Core2	0.8 - 1.5	1.2	300	-	-	50	S/I AND GPIO3 (EN3)
REF_OUT	ADC Ref_Voltage	2.5	2.5	1	Y	Always	-	S/I(always on)

Support Functions

REFERENCE

LP8765 has an internal reference block creating all necessary references and biasing for all blocks.

OSCILLATOR

There is an internal oscillator giving clock to the bucks and to logic control (2MHz typ.).

REFERENCE VOLTAGE (2.5V)

Parameter	Typ.	Min.	Max.	Load (typ.)
REF_OUT	2.5V	**2.425 V**	**2.575V**	100 µA

OPERATING VOLTAGE MONITOR

There is Operating Voltage Monitor (OPVM) that checks VDD-pin voltage before starting Power-On sequence. OPVM is also checked during Power-On sequence. If the VDD voltage is less than OPVM threshold LP8765 will not power on. After LP8765 successfully passed Power-On sequence OPVM is not monitored.

Parameter	Typ.	Min.	Max.	Unit
OPVM threshold	3.1	3.0	3.25	V

THERMAL SHUTDOWN

The Thermal Shutdown (TSD) function monitors the chip temperature to protect the chip from temperature damage caused, e.g. by excessive power dissipation. The temperature monitoring function has two threshold values that result in protective actions. When a lower threshold of +125°C is exceeded, the TSDL bit in the Register 0x08 will be set and an “early warning” interrupt, unless masked, is generated to the processor. A read operation on the TSDL bit will reset it if the temperature has decreased to lower than 10°C below the threshold. If the temperature exceeds a higher threshold value of +160°C, the TSDH bit in the Register 0x08 is set, and the chip will automatically go to the Power-Off sequence. A read operation on the TSDH bit will reset it. Power On can be activated only if the junction temperature is less than the early warning lower threshold +115°C.

Parameter	Typ.	Unit
Higher Threshold*)	160	°C
Early Warning*)	125	
Early Warning Hysteresis*)	10	

*) Guaranteed by design.

Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN_CHG, VIN_CHG SENSE	−0.3V to +28V
V_{BATT}, VIN1, VIN2, VIN_B1, VIN_B2	−0.3V to +6V
VIN3	-0.3 to +4.5V
VCOIN	−0.3V to +4V
SINK1&2	−0.3V to V_{BATT}+0.5V and < 6V
SINK3	−0.3V to 10V
All other input-only pins	−0.3V to V_{BATT}+0.3V, max 6V
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature	−40 to 150°C
Maximum Continuous Power Dissipation P_{D-MAX}	(Note 3)
ESD (Note 4)	
VIN_CHG, BATT, GND, ADC1&2, PWR_ON, RSTIN_N	8 kV HBM
All other	2 kV HBM

Operating Ratings (Note 1, Note 2)

VIN_CHG (Note 10)	4.5V to 6.8V
BATT	3.0V to 5.5V
VCOIN	2.0V to 3.6V
VIN1, VIN2, ViN_B1, VIN_B2	2.5V to V_{BATT}
VIN3	0.7V to 4.5V
All input-output pins	0V to V_{BATT}
Junction Temperature (T_J) Range	−40°C to +125°C
Ambient Temperature (T_A)	−40°C to +85°C
Maximum Power Dissipation (Note 5)	1.4W

Thermal Properties

(Note 9)	
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Jedec Standard Thermal PCB)	38.6°C/W

General Electrical Characteristics

CURRENT CONSUMPTION

Unless otherwise noted, V_{BATT} (=V_{VIN1}=V_{VIN2}=V_{VIN3}=V_{VIN_B1}=V_{VIN_B2}) =3.7V, GND (=GND_B1=GND_B2=GND_LDO=GND_SINK) =0V, C_{VIN_CHG}=C_{VIN_B}1=C_{VIN_B2}=C_{BUCK}1=C_{BUCK2}= C_{VIN1}=C_{VIN2}=10 µF, C_{LDOx}=C_{VTRM}=C_{COIN}=1µF. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in boldface type apply over the entire junction temperature range for operation, T_J= −40°C to +125°C . (Note 6)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
$I_{Q(STANDBY)}$	Battery Standby Current	COIN on, no load	35			µA
		COIN off, no load	4			
$I_{Q(SLEEP)}$	Battery Current in SLEEP Mode @ 0 load	SLEEP_EN=LOW (Buck1, Buck2, LDO5, COIN & REF_OUT on)	165			

LOGIC AND CONTROL

Unless otherwise noted, V_{BATT} (=V_{VIN1}=V_{VIN2}=V_{VIN3}=V_{VIN_B1}=V_{VIN_B2}) =3.7V, GND (=GND_B1=GND_B2=GND_LDO=GND_SINK) =0V, C_{VIN_CHG}=C_{VIN_B}1=C_{VIN_B2}=C_{BUCK}1=C_{BUCK2}= C_{VIN1}=C_{VIN2}=10 µF, C_{LDOx}=C_{VTRM}=C_{COIN}=1µF. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= −40°C to +125°C. (Note 7)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
Logic and Control Inputs						
V_{IL}	Input Low Level	PWR_ON			**0.9**	V
V_{IH}	Input High Level			**1.5**		
V_{IL}	Input Low Level	GPIO1-3			**0.4**	V
V_{IH}	Input High Level			**1.3**		
V_{IL}	Input Low Level	SDA,SCL			**0.35**	V
V_{IH}	Input High Level			**1.3**		

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
V_{IL}	Input Low Level	SLEEP_N, PS_HOLD, RSTIN_N			**0.2* VLDO5**	V
V_{IH}	Input High Level			**0.7* VLDO5**		V
I_{LEAK}	Input Current	SDA, SCL, SLEEP_N, PS_HOLD, GPIO1-3 $0V<V_{IN}<V_{BATT}$		**–5**	**+5**	µA
R_{IN}	Input Resistance	RSTIN_N, PWR_ON	**500**			kΩ
Logic and Control Outputs						
V_{OL}	Output Low Level	SDA, IRQ_N, RESTOUT_N, I_{OL} = 2mA (*Note 7*)			**0.15* VLDO5**	V
V_{OH}	Output High Level	SDA I_{OH} = 2mA (*Note 7*)		**0.75* VLDO5**		V
I_{OH}	Open Drain Leakage	IRQ_N, RSTOUT_N, $V_{OH}=V_{LDO5}$ = 3V			1	µA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. .

Note 4: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Note 5: Care must be exercised where high power dissipation is likely. The maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction to ambient thermal resistance of the package in the application (θ_{JA}). This relationship is given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Note 6: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 7: Guaranteed by design.

Note 8: Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the 2.5V minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.

Note 9: Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design

Note 10: Full charging current is guaranteed for CHG_IN = 4.5 to 6.8V, but particularly at higher input voltages. Increased power dissipation may cause the thermal regulation to limit the current to a safe level, resulting in longer charging time.

Note 11: Buck output voltage accuracy depends on the accuracy of the external feedback resistors. Resistor values should be chosen for the divider network to ensure that at the desired output voltage the FB pin is at the specified value of VOUT. See Buck Converter Application Information.

Linear Li-Ion Battery Charger with Single Input

LP8765 has a built-in Li-Ion/Li-Poly battery management system. Its main features are:

- Single input - AC adapter or USB
- CC/CV linear charging
- Selectable battery regulation voltage
- Flexible charging cycle control
- Wide array of charging current
- Safety timer

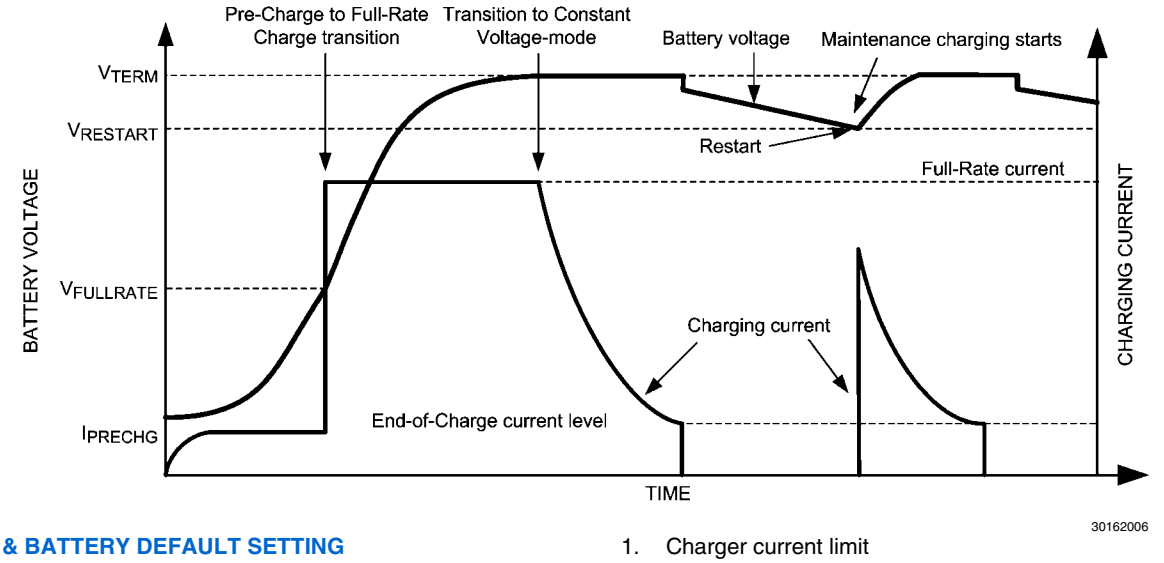
CHARGER FUNCTION

After detecting stable voltage on input (Put 10 µF 35V rated capacitor at input), charger enters pre-charge mode. In this mode battery is charged with pre-charge current until battery voltage reaches full-rate threshold. Now full charging current is applied to the battery, until termination voltage is reached. After that, charger enters constant voltage mode, where constant battery voltage is maintained.

END-OF-CHARGE (EOC) FUNCTION

This function ends the charging cycle if charger has reached constant voltage mode. It has automatic and manual control possibilities. Automatic EOC is enabled if AUTOMATIC START/STOP bit is set to 1, otherwise manual control is used.

Automatic EOC measures charging current and compares it to selected EOC current level. If charging current drops below EOC current threshold, then charging cycle is ended. It is also possible to set EOC time delay. This is the duration for which charging current must be below EOC level before charging ends. For manual EOC write '1' to STOP CHARGING in register 0x39 to stop charging, and write '1' to START CHARGING in register 0x39 to start charging again. These two bits are WRITE ONLY, and only one bit can be set to '1' at a time.



EOC & BATTERY DEFAULT SETTING

By default the EOC and Battery Detection Function will be disabled/masked off (2 EOC bits = 00) in order to support factory testing or software downloading without the main battery. in a normal customer usage, the BB processor should enable the EOC and Battery detection through the I²C after the system startup.

HIGH-CURRENT MODE

The high-current mode should be used only during factory test, and there are few limitations since it is an add-on feature after the LP8765 was defined.

Once the high-current mode is enabled by programming the 2 MSB of ICHARGE to 11, three charger functions will be disabled:

1. Charger current limit
2. Battery voltage OVP (4.9V)
3. Charger Thermal regulation (115°C)

This high-current mode is not guaranteed to operate normally if the load is too high or with fast dynamic changes due to the following limitations:

1. There is only one bump assigned for VBATT, so the maximum DC load is 1.5A.
2. The charger output will vary when load step is applied since there is no main battery connected.

CHARGER ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{BATT} (=V_{VIN1}=V_{VIN2}=V_{VIN3}=V_{VIN_B1}=V_{VIN_B2}) =3.7V, GND (=GND_B1=GND_B2=GND_LDO=GND_SINK) =0V, C_{VIN_CHG}=C_{VIN_B}1=C_{VIN_B2}=C_{BUCK}1=C_{BUCK2}= C_{VIN1}=C_{VIN2}=10 µF, C_{LDOx}=C_{VTRM}=C_{COIN}=1µF. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= −40°C to +125°C. (*Note 6*, *Note 9*)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
V_{CHG_IN}	AC wall adapter input voltage operating range			**4.5**	**6.7**	V
V_{OK_CHG}	CHG_IN OK Trip Point	V_{CHG_IN}	150			mV
		V_{CHG_IN}	40			
V_{TERM}	Battery charging termination Voltage	V_{TERM} = 4.2V, I_{CHG} = 50 mA		−0.35	+0.35	%
		V_{TERM} is measured at 10% of the programmed I_{CHG} current		**−1**	**+1**	
I_{CHG}	CHG_IN programmable full-rate charging current	6.8V ≥ V_{CHG} ≥ 4.5V V_{BATT} < V_{CHG-IN} - V_{OK_CHG} $V_{FULLRATE}$ < V_{BATT} < V_{TERM} (*Note 10*)		**50**	**1200**	mA
	Full-rate charging current tolerance	I_{CHG} = 400 mA		**−10**	**+10**	%
$I_{PREEQUAL}$	Pre-charging current	2.2V < V_{BATT} < V_{FULL_RATE}	50	**20**	**80**	mA
V_{FULL_RATE}	Full-rate qualification threshold	V_{BATT} rising, transition from pre-charging to full-rate charging	2.8	**2.7**	**2.9**	V
I_{EOC}	End-of-charge current, % of full-rate current	0.1C option selected	10			%
$V_{RESTART}$	Restart threshold voltage	From V_{TERM} voltage (4.2V - 100 mV option selected)	−100	**−70**	**−130**	mV
C_{BATT}	Capacitance on BATT	(*Note 7*)		**30**	**1000**	µF
T_{REG}	Regulated junction temperature	(*Note 7*)	115			°C

Buck Converters

The LP8765 contains two high-efficiency step-down DC-DC switching buck converters, capable of delivering a constant voltage from a single Li-Ion battery. Using a voltage mode architecture with synchronous rectification, the LP8765 has the ability to deliver up to 600 mA (Buck1) and 500 mA (Buck2) depending on the input voltage, the output voltage, the ambient temperature, and the inductor chosen.

There are two modes of operation depending on the current required: PWM and PFM. PWM mode handles current loads of approximately 70 mA or higher, delivering voltage precision of ±3% with up to 90% efficiency or better. Lighter output current loads cause the device to automatically switch into PFM for reduced current consumption (I_Q = 16 µA typ.) and a longer battery life. User can force the buck converters to PWM mode by setting FORCE PWM BUCKx bit in Control Register.

Besides PFM power-saving feature, the buck regulators inside the LP8765 also have low-power operation mode, which has lower current consumption compare to PFM. The low-power mode can be enabled when SLEEP_N pin goes low if control bit BUCKS LOW PWR IN SLEEP = 1. However, the total load capability of bucks will be limited to 5mA when they operate at low-power mode. The buck regulators inside the LP8765 can operate up to a 100% duty cycle (PFET switch always on) for low-dropout control of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage.

CIRCUIT OPERATION

During the first portion of each switching cycle, the control block in the buck regulator turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of (V_{IN} – V_{OUT})/L by storing energy in a magnetic field. During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of – V_{OUT}/L. The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

Modulating the PFET switch-on time to control the average current sent to the load regulates the output voltage. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM OPERATION

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve good load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage, is introduced.

While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. In this case the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

PFM OPERATION

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency. The part will automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

1. The inductor current becomes discontinuous; or
2. The peak PFET switch current drops below the I_{MODE} level.

Typically,

$$I_{MODE} < 30\ mA + \frac{V_{IN}}{42\Omega}$$

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between ~0.6% and ~1.7% above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PFET switch is turned on. It remains on until the output voltage exceeds the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode.

The typical peak current in PFM mode is:

$$I_{PFM} = 112\ mA + \frac{V_{IN}}{27\Omega}$$

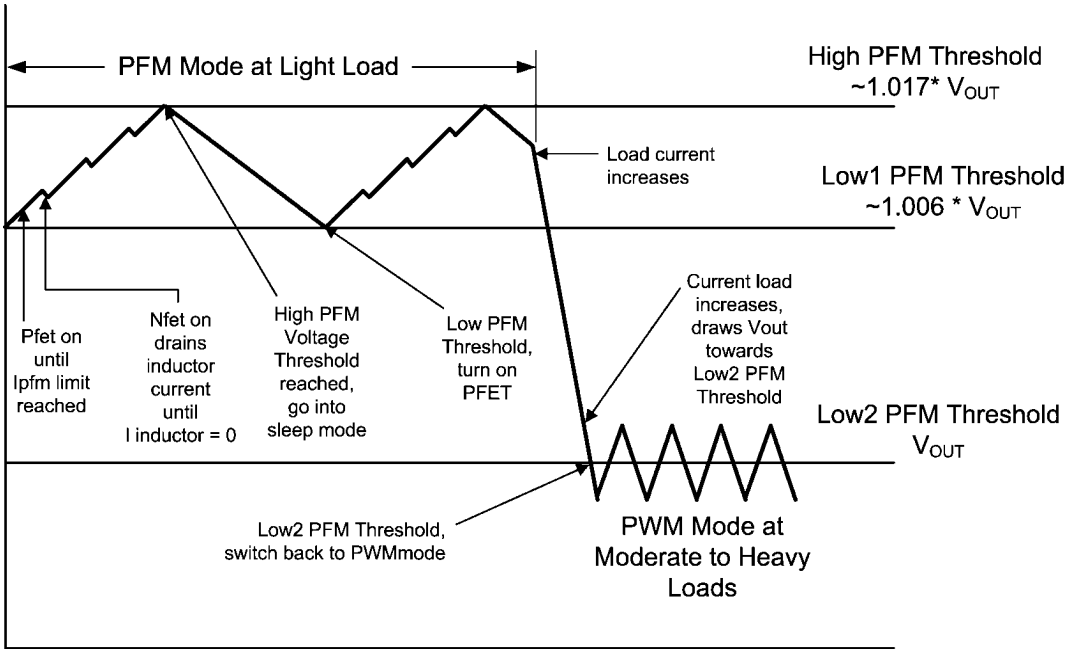
Once the PFET switch is turned off, the NFET switch is turned on until the inductor current ramps to zero. When the NFET zero-current condition is detected, the NFET switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see figure below), the PFET switch is again turned on, and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NFET switch is turned on briefly to ramp the inductor current to zero; then both output switches are turned off, and the part enters an extremely low-power mode which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the 'low' PFM threshold, the cycle repeats to restore the output voltage (average voltage in PFM mode) to ~1.15% above the nominal PWM output voltage.

If the load current should increase during PFM mode (see below figure) causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode.

V_{IN}	PWM to PFM (Typ.)	PFM to PWM (Typ.)
3.6V	50 mA	100 mA
4.5	65 mA	115 mA

FORCE PWM BUCK1 and FORCE PWM BUCK2 bits in Serial Interface control registers determine whether the buck converter chooses PFM/PWM operating mode automatically or operates constantly in PWM mode.

Forced PWM BUCKx	PFM/ PWM Mode
0	Auto mode PFM/PWM
1	Forced PWM mode



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INTERNAL SYNCHRONOUS RECTIFICATION

While in PWM mode, the converter uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

CURRENT LIMITING

A current limit feature allows the circuit to protect itself and external components during overload conditions PWM mode implements cycle-by-cycle current limiting using an internal comparator that trips at 1000 mA (typ.) for Buck1 and Buck2. If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold. This ensures the inductor current has more time to decay, thereby preventing runaway.

SOFT-START

The LP8765 buck regulators have a soft start circuit which limits in-rush current during startup.

LOW-DROPOUT OPERATION

The buck converter can operate at 100% duty cycle (no switching, PFET switch completely on) for low-dropout support of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage. The minimum input voltage needed to support the output voltage is:

- $V_{IN,MIN}$: $=I_{LOAD} * (R_{DSON(P)} + R_{INDUCTOR}) + V_{OUT}$
- I_{LOAD}: I_{LOAD} current
- $R_{DSON(P)}$: PFET drain-source resistance in the triode region
- $R_{INDUCTOR}$: Inductor resistance

BUCK ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{BATT} (=V_{VIN1}=V_{VIN2}=V_{VIN3}=V_{VIN_B1}=V_{VIN_B2}) =3.7V, GND (=GND_B1=GND_B2=GND_LDO=GND_SINK) =0V, C_{VIN_CHG}=C_{VIN_B}1=C_{VIN_B2}=C_{BUCK}1=C_{BUCK2}= C_{VIN1}=C_{VIN2}=10 µF, C_{LDOx}=C_{VTRM}=C_{COIN}=1µF. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= −40°C to +125°C. (*Note 6*, *Note 11*)

Symbol	Parameter	Conditions	Typ.	Limit		Units
				Min	Max	
$V_{FB\ 1}$	Feedback Voltage (Buck1)	V_{OUT} = 1.2V	1.2	**1.164**	**1.236**	V
$V_{FB\ 2}$	Feedback Voltage (Buck1)	V_{OUT} = 1.8V	1.8	**1.746**	**1.854**	
$V_{OUT,PFM}$	Output voltage regulation in PFM mode relative to regulation in PWM mode	(*Note 7*)	1.5			%
V_{OUT}	Line regulation (*Note 7*)	3.0V ≤ V_{IN} ≤ 5.5V I_{OUT} = 10 mA	0.14			%/V
V_{OUT}	Load regulation (*Note 7*)	100 mA ≤ I_{OUT} ≤ 300 mA	0.09			%/mA
I_{LIM_PWM}	Switch peak current limit	PWM mode @ 600 mA 3.0V ≤ V_{IN} ≤ 4.2V (Buck1)	1025	**710**	**1500**	mA
		PWM mode @ 500 mA 3.0V ≤ V_{IN} ≤ 4.2V (Buck2)	925	**630**	**1400**	
$R_{DSON\ (P)}$	P channel FET on resistance	V_{IN} = 3.6V, I_{OUT} = 100 mA	300			mΩ
$R_{DSON\ (N)}$	N channel FET on resistance		150			
f_{OSC}	Internal Oscillator Frequency	PWM mode	2	1.9	2.1	MHz
η	Efficiency	I_{OUT} = 5 mA, PFM mode V_{OUT} = 1.35V (*Note 7*)	88			%
		I_{OUT} = 300 mA, PWM mode V_{OUT} = 1.35V (*Note 7*)	90			
T_{STUP}	Startup time	I_{OUT} = 0 V_{OUT_BUCK1} = 1.2V V_{OUT_BUCK2} = 1.8V (*Note 7*)	120 140			µs

Output Voltage Programming

BUCK#	Function	I (mA)	Output Voltage (V)	Startup Default	Enable Control
Buck1	CORE1	600	0.8-1.45 (50 mV step)	**ON**	S/I
Buck2	IO&Memory	500	0.8-1.45 (50 mV step)	**ON**	S/I

BUCK1 has two pre-programmed voltages BUCK1 NORMAL & BUCK1 SLEEP at 0x1C.

DVS FUNCTION FOR BUCK1

SLEEP_N	
High	Buck1 V_{OUT} = BUCK1 NORMAL
Low	Buck1 V_{OUT} = BUCK1 SLEEP

NOTE: If user does not want this DVS function, just program BUCK1 SLEEP = BUCK1 NORMAL = 1.2V.

LDO's

There are all together 10 LDO's in LP8765 grouped as:

- A-type LDO's (LDO's 1-4)
- D-type LDO's (LDO's 5-8)
- LILO LDO (LDO 9)
- USB LDO (LDO 10)

The A-type LDO's are optimized for supplying of analog loads and have ultra-low noise (10 µVRMS) and excellent PSRR (75 dB) performance.

The D-type LDO's are optimized for good dynamic performance to supply different fast changing (digital) loads with still reasonable noise (30 µVRMS) and PSRR (60 dB) performance.

The LILO LDO (LDO9) is powered by the output of BUCK2 in order to get better efficiency.

The USB LDO (VTRM) is a high-voltage LDO that uses VIN_CHG as supply; it has 28V OVP capability.

All LDO's can be programmed through serial interface for different output voltage values.

A-TYPE LDO ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{BATT} (=V_{VIN1}=V_{VIN2}=V_{VIN3}=V_{VIN_B1}=V_{VIN_B2}) =3.7V, GND (=GND_B1=GND_B2=GND_LDO=GND_SINK) =0V, C_{VIN_CHG}=C_{VIN_B}1=C_{VIN_B2}=C_{BUCK}1=C_{BUCK2}= C_{VIN1}=C_{VIN2}=10 µF, C_{LDOx}=C_{VTRM}=C_{COIN}=1µF. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= −40°C to +125°C. (*Note 6*)

Symbol	Parameter	Condition	LDO#	Typ.	Limits		Units
					Min	Max	
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 1mA, V_{OUT} = default	1-4		**−2**	**+2**	%
					−3	**+3**	
I_{SLEEP}	Max output current in sleep mode (TXCO_EN = 0)	V_{OUT} +0.5V ≤ V_{IN} ≤ 5.5V (*Note 7*)	2			**1**	mA
I_{SC}	Output current limit	V_{OUT} = 0V	1	230	**100**		mA
			2,3,4	395	**200**		
V_{DO}	Dropout Voltage	V_{OUT} = 2.85V, I_{OUT} = I_{MAX} (*Note 8*)	1-4	90		**150**	mV
ΔV_{OUT}	Line Regulation	V_{OUT} +0.5V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 1mA		25			mV
	Load Regulation	1 mA ≤ I_{OUT} ≤ 450 mA		0.3			
e_N	Output noise voltage	10 Hz ≤ f ≤ 100 kHz C_{OUT} = 1µF (*Note 7*)	1-4	10			μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	f=10 kHz, C_{OUT} = 1µF I_{OUT} = 20 mA (*Note 7*)	1-4	75			dB
$t_{STARTUP}$	Startup Time from Shutdown	C_{OUT} = 1µF, I_{OUT} = I_{MAX}, GPIO to 0.95*V_{OUT} (*Note 7*)	1-4	35			µs
$V_{TRANSIENT}$	Startup Transient Overshoot	C_{OUT} = 1µF, I_{OUT} = I_{MAX}	1-4			**30**	mV
C_{OUT}	External output capacitance for stability		1-4	1.0	**0.5**	**20**	µF

D-TYPE LDO ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{BATT} (=V_{VIN1}=V_{VIN2}=V_{VIN3}=V_{VIN_B1}=V_{VIN_B2}) =3.7V, GND (=GND_B1=GND_B2=GND_LDO=GND_SINK) =0V, C_{VIN_CHG}=C_{VIN_B}1=C_{VIN_B2}=C_{BUCK}1=C_{BUCK2}= C_{VIN1}=C_{VIN2}=10 µF, C_{LDOx}=C_{VTRM}=C_{COIN}=1µF. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= −40°C to +125°C. (*Note 6*)

Symbol	Parameter	Condition	LDO#	Typ.	Limits		Units
					Min	Max	
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 1mA, V_{OUT} = default	5-8		**−2**	**+2**	%
					−3	**+3**	
I_{SLEEP}	Max output current in sleep mode (TXCO_EN = 0)	V_{OUT} +0.5V ≤ V_{IN} ≤ 5.5V	5-6			**1**	mA
I_{SC}	Output current limit	V_{OUT} = 0V	5	680	**400**		mA
			6,7	380	**200**		
			8	540	**300**		

Symbol	Parameter	Condition	LDO#	Typ.	Limits		Units
					Min	Max	
V_{DO}	Dropout Voltage	V_{OUT} = 3V, I_{OUT} = I_{MAX} (*Note 8*)	5	175		**280**	mV
			6,7	90		**150**	
			8	135		**225**	
ΔV_{OUT}	Line Regulation	V_{OUT} +0.5V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 1 mA	5-8	30			mV
	Load Regulation	1 mA ≤ I_{OUT} ≤ 450 mA		2			
e_N	Output noise voltage	10 Hz ≤ f ≤ 100 kHz C_{OUT} = 1µF (*Note 7*)	5-8	35			μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	f=10 kHz, C_{OUT} = 1µF I_{OUT} = 20 mA (*Note 7*)	1-4	65			dB
$t_{STARTUP}$	Startup Time from Shutdown	C_{OUT} = 1µF, I_{OUT} = I_{MAX}, GPIO2 to 0.95*V_{OUT} (*Note 7*)	5-8	35			µs
$V_{TRANSIENT}$	Startup Transient Overshoot	C_{OUT} = 1µF, I_{OUT} = I_{MAX} (*Note 7*)	5-8			**30**	mV
C_{OUT}	External output capacitance for stability		5-8	1.0	**0.5**	**20**	µF

LDO9 (LILO) ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_A = 25°C. Limits in **boldface** type apply over the operating ambient temperature range −40°C ≤ T_A ≤ + 125°C). Unless otherwise noted, specifications apply to the closed loop typical application circuit with V_{IN3} =3.7V, I_{OUT} = 1mA, C_{OUT} = 1µF, V_{EN} = V_{BATT} (*Note 6*).

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
V_{OUT}	Output Voltage Tolerance	V_{OUT} = 1.2V at V_{IN3} = 1.8V		**−2**	**2**	%
$\Delta V_{OUT}/V_{IN}$	Line Regulation Error	V_{IN3} = $V_{OUT(NOM)}$ + 0.3V to 1.8V, I_{OUT} = 300 mA	0.1		**1.5**	mV
$\Delta V_{OUT}/\Delta mA$	Load Regulation Error	V_{IN3} = 1.8V, I_{OUT} = 1mA to 300 mA	2		**20**	mV
I_{SC}	Output Current (short circuit)	V_{OUT} = 0V, V_{IN3} = 1.8V, I_{OUT} = 1 mA	595	**300**		mA
V_{DO}	Output Voltage Dropout	V_{OUT} = 1.2V, I_{OUT} = 300 mA (*Note 8*)	55		**110**	mV
		I_{OUT}=150 mA (*Note 8*)	27.5		**60**	mV
EN	Output Noise	10 Hz to 100 Hz (*Note 7*)	100			mVRMS
PSRR	Power Supply Rejection Ration	Sine modulated V_{BATT} (*Note 7*) f = 10 Hz f = 100 Hz f = 1kHz	 70 65 45			dB
		Sine modulated V_{BATT} (*Note 7*) f = 10 Hz f = 100 Hz f = 1kHz f = 10kHz f = 100 kHz	 80 90 95 85 64			dB
I_Q	Quiescent Current into V_{IN3} (Normal mode)	I_{LOAD} = 0 (*Note 7*)	11			µA
$I_{Q(SHUTDOWN)}$	V_{IN3} Shutdown Current	Output disabled (*Note 7*)	0.1			µA
ΔV_{OUT}	Line Transient Response (*Note 7*)	V_{IN3} = $V_{OUT(NOM)}$ + 0.3V to $V_{OUT(NOM)}$ + 0.9V; tr, tf = 10 µs	±1			mV
	Load Transient Response (*Note 7*)	Pulsed load 0↔300 mA, di/dt = 300 mA/1µs	±15			mV
$T_{STARTUP}$	Startup Time	GPIO3 to 0.95*V_{OUT} (*Note 7*)	70		**150**	µs

USB LDO (VTRM) ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40 to +125°C. Unless otherwise specified, the following applies for V_{VIN_CHG} = 5V. (*Note 6*)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 1mA,	3.3	**3.15**	**3.5**	V
I_{SC}	Output Current Limit	V_{OUT} = 0V	135	10		mA
ΔV_{OUT}	Line Regulation	4.5V ≤ V_{IN_CHG} ≤ 6.5V I_{OUT} = 10 mA	10			mV
ΔV_{OUT}	Load Regulation	1mA ≤ I_{OUT} ≤ 10mA	60			
PSRR	Power Supply Ripple Rejection Ratio	f = 10 kHz, C_{OUT} = 1mF I_{OUT} = 20 mA (*Note 7*)	45			dB
$t_{START-UP}$	Startup Time from Shutdown	C_{OUT} = 1mF, I_{OUT} = 10 mA (*Note 7*)	15			µs
$V_{TRANSIENT}$	Startup Transient Overshoot	C_{OUT} = 1mF, I_{OUT} = 10 mA (*Note 7*)	250			mV
C_{OUT}	External output capacitance for stability		1	**0.6**	**20**	µF

A/D Converter

LP8765 is equipped with a 12-bit successive approximation analog-to-digital converter to enable the conversion of analog inputs:

- Battery voltage
- Charge voltage or current
- IC temperature
- Battery Temperature (external input)

The battery voltage input and the charge current are scaled linearly to adapt the voltage/current range of the source to the input voltage range of the A/D core. The ADC is clocked by the internal 1MHz system clock. The conversion result is available in the registers 0x11 & 0x12 80 µs after the setting of the CONV_START bit in the ADC Control Register. The ADC will automatically enter power save mode if conversions are not performed.

A/D CONVERTER DATA AND CONTROL REGISTERS

The Read/Write Control register ADC_CTRL allows starting the conversion, source selection and output format selection. Setting the CONV_START bit in the control register starts a new A/D conversion. Setting ADC_FORMAT register to '1' allows throwing out the MSB and shifting the result 1 bit left. This can be used if result's MSB is known, to get more data with one register read. User should wait at least 80 µs between two readings, or check the register bit CONVERSION_DONE=1 at 0x13 bit0 before read ADC data out.

ADC INPUT SELECTION (REGISTER 0x10)

ADC INPUT SEL			ADC Input	Max_Value in Formula	Accuracy
bit3	bit2	bit1			
0	0	0	V_{BATT}	5.5V	±2% in operating range
0	0	1	V_{IN_CHG}	6.0V	±3% in operating range
0	1	0	I_{IN_CHG}	2.5A	TBD
0	1	1	T_J	125°C	**See *Figure 1***
1	0	0	V_{BATT}	6.0V	±3% in operating range
1	0	1	V_{BATT}	5.0V	±2% in operating range
1	1	0	V_{ADC1}	2.5V	±(2%+30 mV) in operating range
1	1	1	V_{ADC2}	2.5V	±(2%+30 mV) in operating range

MEASUREMENT RESULT CALCULATION

The transfer functions for conversions can be given as: VALUE = MAX_VALUE*(i+0.5)/4095 where i = 0…4095.

If only 8 most significant bits are read, then: VALUE = MAX_VALUE*(i+0.5)/255 where i = 0…255.

If ADC_FORMAT is set to 1 and 8 bits are read, then: VALUE = MAX_VALUE*(i+0.5)/511 where i = 0…255.

If MSB is assumed 1, then MAX_VALUE/2 must be added to this Value.

WORKING RANGE AND ACCURACY

ADC reading is accurate for VBATT voltages over 2.7V. ADC uses internal bandgap reference. Total absolute accuracy for voltage measurement is better than 3% over all working conditions.

For current measurement the absolute accuracy is better than 5% or 10 mA whatever is bigger.

S&H

Sample in time is 1µs. As result ADC may sample in possible spikes that may occur during phone operation. To filter spikes out ADC code readings averaging can be used.

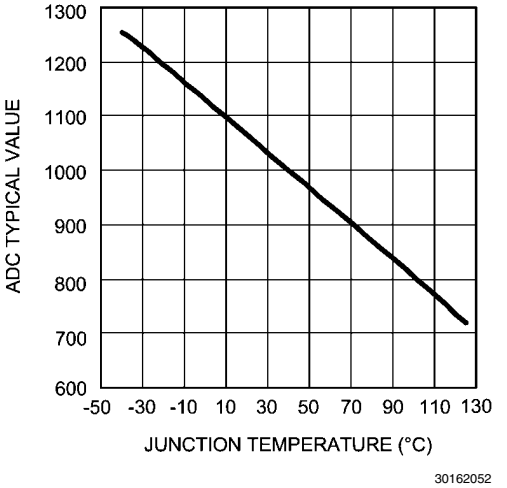


FIGURE 1. ADC Typical Value vs. Junction Temperature

ADC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{BATT} (=V_{VIN1}=V_{VIN2}=V_{VIN3}=V_{VIN_B1}=V_{VIN_B2}) =3.7V, GND (=GND_B1=GND_B2=GND_LDO=GND_SINK) =0V, C_{VIN_CHG}=C_{VIN_B}1=C_{VIN_B2}=C_{BUCK}1=C_{BUCK2}= C_{VIN1}=C_{VIN2}=10 µF, C_{LDOx}=C_{VTRM}=C_{COIN}=1µF. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. (*Note 6*)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
	Resolution		12			bits
INL	Integral Nonlinearity	(*Note 7*)		**−4**	**4**	LSB
DNL	Differential Nonlinearity	No missing code (*Note 7*)		**−2**	**2**	
	Conversion Time	(*Note 7*)			**80**	µs

Real-Time Clock

Real-time clock (RTC) block is used for time tracking in any chip condition. It uses 32 kHz crystal oscillator for accurate time predictions and is supplied either from system supply in normal condition or from coin battery when the chip is in shutdown mode.

This RTC has the following features:

- Accurate time counting, with fine-grained correction for inaccuracies caused by environment;
- Calendar for years 2000 - 2099 with leap-year compensation and automatic day-of-week calculation; and
- Two highly customizable alarms.

All RTC data is presented in binary format, with following details:

- Seconds, minutes: codes from 000000 to 111011 represent numbers from 0 to 59;
- Hours: codes from 00000 to 10111 represent numbers from 0 to 23; only 24-hour mode available;
- Days of week: codes from 000 to 110 represent days from Monday to Sunday;
- Days of month: codes from 00000 to 11110 represent days from 1st to 31st; and
- Years: codes from 0000000 to 1100011 represent years from 2000 to 2099.

RTC time and alarm registers are user-writable, except for day-of-week registers, which are calculated automatically and are read-only.

Alarms allow creating periodical or one-time events. The result of an alarm event depends on the PMU state. If PMU is in standby, then alarm causes PMU to start up. If PMU is in working mode, then alarm creates an interrupt.

Alarm event happens if the alarm is activated (ALARM ACTIVATED bit is '1') and current RTC time matches the time in alarm configuration time stored in the register. The smallest alarm selection time unit is 1 minute, and the event always happens on the first second of the minute. To exclude a time unit value from matching check, all alarm configuration bits for this value must be written to '1'. For example, to ignore month number on alarm creation, the ALARM MONTH code must be 1111. Alarm weekday bits must also be configured - alarm event can only happen on selected weekdays. If weekday is not important or not known, then all weekday bits should be set to '1'.

If the user writes some data into RTC alarm registers, then this data is stored inside RTC. This data will stay there as long as RTC has power. Turning off the phone will not remove RTC supply, so the alarms will still work and can trigger a phone power-up.

RTC UNLOCK FUNCTION

If the Battery voltage is lower than 3.4V/3.5V, the RTC level shifts will be disabled when AC adapter or USB cable is plugged in. In order to unlock the RTC date, two control bits in address 0x39, “RTC UNLOCK” & “RTC DATA LATCH” are used by following sequence:

1. Write 04h to address 0x39h
2. Write 08h to address 0x39h

RTC TIME SELECTION TABLE 1
Registers 0x4C...0x51

RTC TIME SECONDS	Current RTC time: seconds (0x00...0x3B)
RTC TIME MINUTES	Current RTC time: minutes (0x00...0x3B)
RTC RESET SECONDS	Write '1' to reset seconds value to 0
RTC TIME HOURS	Current RTC time: hours (0x00...0x17)
RTC TIME DAY OF MONTH	Current RTC time: day of month (0x00...0x1E; 0x00 is the first day of the month)
RTC TIME WEEKDAY	Current RTC time: weekday (0x0...0x6; 0x0 - Monday, 0x1 - Tuesday, 0x2 - Wednesday, 0x3 - Thursday, 0x4 - Friday, 0x5 - Saturday, 0x6 - Sunday)
RTC TIME MONTH	Current RTC time: month (0x0...0xB; 0x0 - January, 0x1 - February, 0x2 - March, 0x3 - April, 0x4 - May, 0x5 - June, 0x6 - July, 0x7 - August, 0x8 - September, 0x9 - October, 0xA - November, 0xB - December)
RTC TIME YEAR	Current RTC time: year (0x00...0x63 - years 2000...2099)

RTC TIME SELECTION TABLE 2
Registers 0x54…0x62

ALARMX MINUTES	Minute setting for alarm; 0x3F to ignore minutes
ALARMX HOURS	Hour setting for alarm; 0x1F to ignore hours
ALARMX DAY OF MONTH	Day of month setting for alarm; 0x1F to ignore day of month
ALARMX MONTH	Month setting for alarm; 0xF to ignore month
ALARMX YEAR	Year setting for alarm; 0x7F to ignore year
ALARMX MONDAY/ TUESDAY/ WEDNESDAY/ THURSDAY/ FRIDAY/ SATURDAY/SUNDAY	Weekday selection for alarm; write '1' to allow alarm on that day
ALARMX ACTIVATED	0 - Alarm not activated 1 - Alarm activated

Backup Battery Charger

Backup battery charger (BBC) is intended for charging an external coin cell battery. Its output is connected to the VCOIN pin. It consists of Voltage Limited Current Source with 1kΩ output resistor. By default it is always on.

It is possible to turn backup battery charger off via registers. VCOIN – voltage limit and ICOIN – current source values are also programmable via registers (the possible values are stated in *Backup Battery Charger*). BBC has a reverse current protection. VCOIN pin voltage can be measured by an internal ADC.

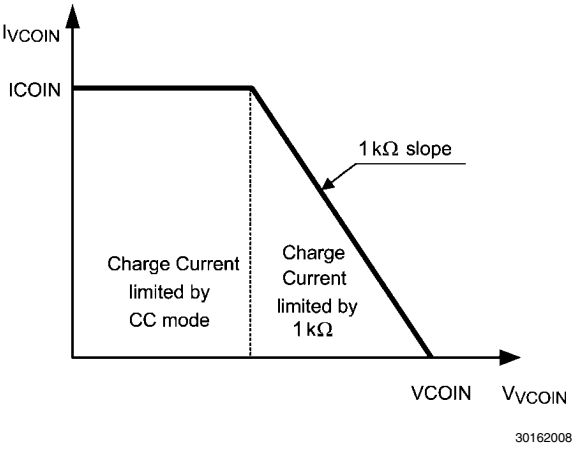


FIGURE 2. BBC IU Characteristic

BACKUP BATTERY CHARGER ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = –40 to +125°C. Unless otherwise specified, the following applies for V_{VIN_CHG} = 5V. (*Note 6*)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
VCOIN	Voltage limit	I_{LOAD} = 1µA VCOIN programmed to 3V	3V	–7%	+7%	V
ICOIN	Charging current	VCOIN pin shorted to GND ICOIN programmed to 200 µA	200	–20%	+20%	µA
R_{VCOIN}	Internal series resistor		1.0	0.5	1.6	kΩ
I_{LEAK}	Reverse leakage current	VRTC pin current = 0			10	µA
I_{RTC}	COIN input current	V_{COIN} = 3V	1.7		5	µA

32.768 kHz Crystal Oscillator

There are two options for implementing the 32.768 kHz oscillator:

1. An external crystal that is connected between XIN and XOUT. The external crystal ESR must not exceed 100 kΩ; if this value is exceeded the circuit may never start oscillating.
2. An external oscillator module could be used by connecting the module output directly into XIN. When using an external oscillator module, the XOUT pin should be unconnected.

Pins XIN and XOUT are not able to drive external load. Oscillator output is buffered to pin OSC_32KHZx.

Comparators

LP8765 contains two general purpose comparators which can be used for detecting external accessories like ear plugs, etc.

COMPARATOR ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{BATT} (=V_{VIN1}=V_{VIN2}=V_{VIN3}=V_{VIN_B1}=V_{VIN_B2}) =3.7V, GND (=GND_B1=GND_B2=GND_LDO=GND_SINK) =0V, C_{VIN_CHG}=C_{VIN_B}1=C_{VIN_B2}=C_{BUCK}1=C_{BUCK2}= C_{VIN1}=C_{VIN2}=10 µF, C_{LDOx}=C_{VTRM}=C_{COIN}=1µF. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= −40°C to +125°C. (*Note 6*)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
V_{TH}	Input threshold voltage	Default setting	250			mV
		Programmable threshold voltages	25			
			50			
			100			
			150			
			250			
			500			
			750			
			1000			
I_{IL}	Input leakage current	INP1, INP2 0V ≤ V_{INPUT} ≤ V_{BATT}		−1	+1	

3 Current Sinks

SINK1: Powered up to VBATT+0.5V, 100 mA/120 mA Max Current.
SINK2: Powered up to VBATT+0.5V, 100 mA/120 mA Max Current.
SINK3: Powered up to 10V, 100 mA/120 mA Max Current.

Recommendation: use either SINK1 or SINK2 to drive DC motor.

CURRENT SINK ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{BATT} (=V_{VIN1}=V_{VIN2}=V_{VIN3}=V_{VIN_B1}=V_{VIN_B2}) =3.7V, GND (=GND_B1=GND_B2=GND_LDO=GND_SINK) =0V, C_{VIN_CHG}=C_{VIN_B}1=C_{VIN_B2}=C_{BUCK}1=C_{BUCK2}= C_{VIN1}=C_{VIN2}=10 µF, C_{LDOx}=C_{VTRM}=C_{COIN}=1µF. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= −40°C to +125°C. (*Note 6*)

Symbol	Parameter	Typ	Limit		Units
			Min	Max	
V_{SINK_MAX}	Voltage tolerance at SINK1+2 pins			V_{BATT}+0.5	V
	Voltage tolerance at SINK3 pins			10	
I_{OUT} (100 mA)	Sink current range		6.25	100	mA
I_{OUT} (120 mA)	Sink current range		7.5	120	mA
I_{OUT} Resolution	Current control resolution	4			bits
I_{OUT} Accuracy	Current accuracy at default current		−5	5	%
PWM Resolution	PWM control resolution	6			bits
V_{SAT} (100 mA)	Saturation voltage at 90 mA*	310			mV
V_{SAT} (120 mA)	Saturation voltage at 108 mA*	385			mV
f_{PWM}	PWM frequency	20.4			kHz

* Headroom voltage at SINK pin when current drop to 90% of its nominal value.

SINK DRIVERS

Each driver may be configured for 100 mA or 120 mA current range.

Sink Scale = 0

SINK IOUT[3:0]	I_{OUT} (mA)
1111	100.00
1110	93.75
1101	87.50
1100	81.25
1011	75.00
1010	68.75
1001	62.50
1000	56.25
0111	50.00
0110	43.75
0101	37.50
0100	31.25
0011	25.00
0010	18.75
0001	12.50
0000	6.25

Sink Scale = 0

SINK IOUT[3:0]	I_{OUT} (mA)
1111	120.00
1110	112.50
1101	105.00
1100	97.50
1011	90.00
1010	82.50
1001	75.00
1000	67.50
0111	60.00
0110	52.50
0101	45.00
0100	37.50
0011	30.00
0010	22.50
0001	15.00
0000	7.50

I²C-Compatible Serial Bus Interface

INTERFACE BUS OVERVIEW

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device.

This protocol uses a two-wire interface for bi-directional communications between the ICs connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pull-up resistor of 1.5 kΩ and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the SCL.

DATA TRANSACTIONS

One data bit is transferred during each clock pulse. Data is sampled during the high state of the SCL. Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

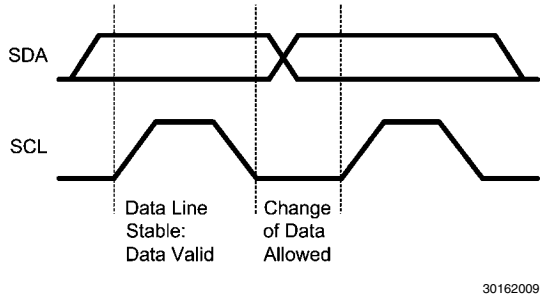


FIGURE 3. Bit Transfer

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

START AND STOP

The Master device on the bus always generates the Start-and-Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy, and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

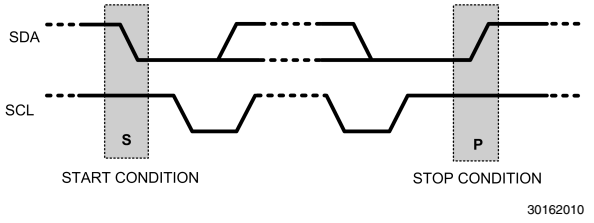


FIGURE 4. Start-and-Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

ACKNOWLEDGE CYCLE

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device. The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

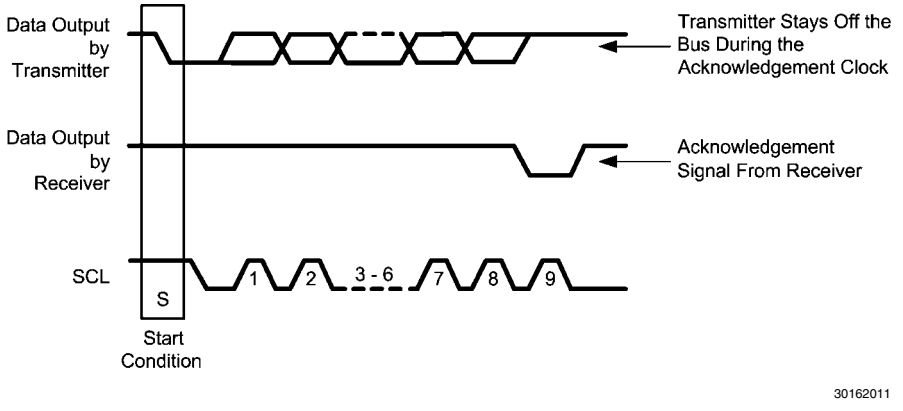
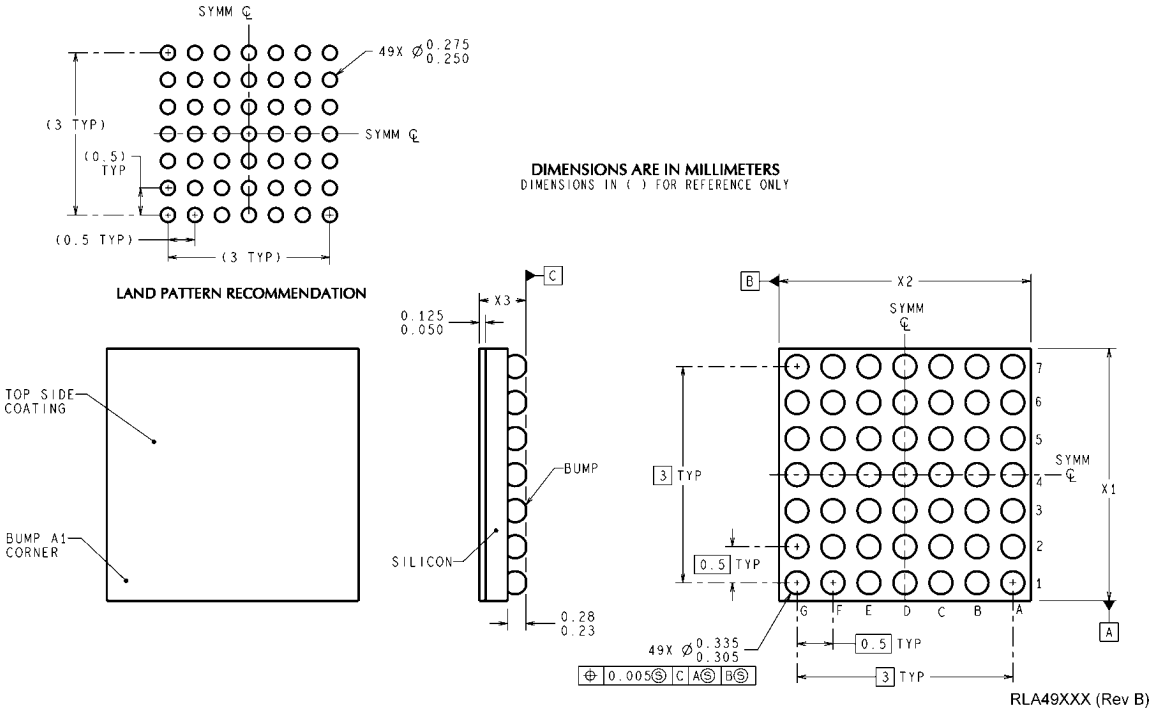


FIGURE 5. Bus Acknowledge Cycle

Physical Dimensions inches (millimeters) unless otherwise noted



25-bump Thin micro SMD Package
NS Package Number RLA49JJA
X1 = 3.669 mm ±0.030 mm
X2 = 3.669 mm ±0.030 mm
X3 = 0.650 mm ±0.075 mm

Notes

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