



# THE DATASHEET OF LOG101AID





# Precision LOGARITHMIC AND LOG RATIO AMPLIFIER

## FEATURES

- EASY-TO-USE COMPLETE CORE FUNCTION
- HIGH ACCURACY: 0.01% FSO Over 5 Decades
- WIDE INPUT DYNAMIC RANGE:  
7.5 Decades, 100pA to 3.5mA
- LOW QUIESCENT CURRENT: 1mA
- WIDE SUPPLY RANGE:  $\pm 4.5V$  to  $\pm 18V$

## APPLICATIONS

- LOG, LOG RATIO COMPUTATION:  
Communication, Analytical, Medical, Industrial,  
Test, and General Instrumentation
- PHOTODIODE SIGNAL COMPRESSION AMPS
- ANALOG SIGNAL COMPRESSION IN FRONT  
OF ANALOG-TO-DIGITAL (A/D) CONVERTERS

## DESCRIPTION

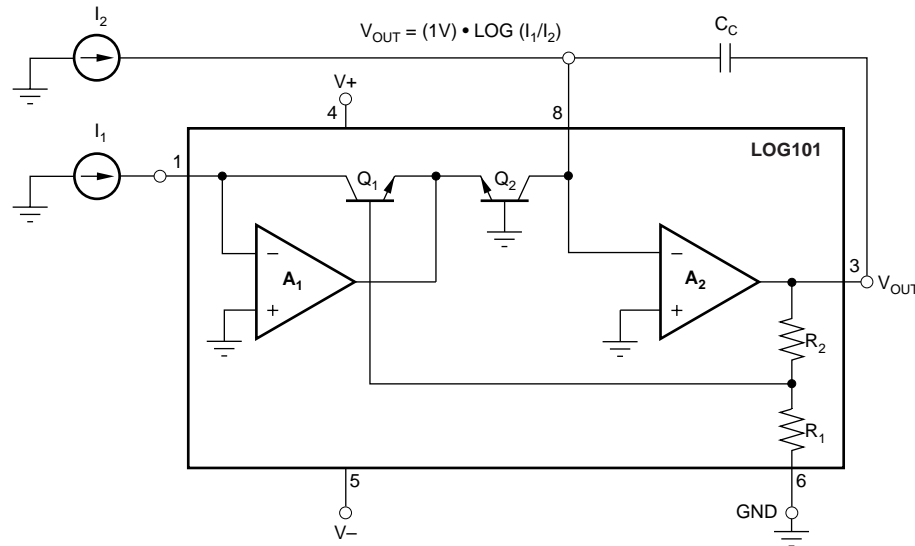
The LOG101 is a versatile integrated circuit that computes the logarithm or log ratio of an input current relative to a reference current.

The LOG101 is tested over a wide dynamic range of input signals. In log ratio applications, a signal current can come from a photodiode, and a reference current from a resistor in series with a precision external reference.

The output signal at  $V_{OUT}$  is trimmed to 1V per decade of input current allowing seven decades of input current dynamic range.

Low DC offset voltage and temperature drift allow accurate measurement of low-level signals over a wide environmental temperature range. The LOG101 is specified over the temperature range  $-5^{\circ}C$  to  $+75^{\circ}C$ , with operation over  $-40^{\circ}C$  to  $+85^{\circ}C$ .

Note: Protected under US Patent #6,667,650; other patents pending.



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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage, V+ to V-.....	36V
Input Voltage .....	(V-) - 0.5 to (V+) + 0.5V
Input Current .....	±10mA
Output Short-Circuit <sup>(2)</sup> .....	Continuous
Operating Temperature .....	-40°C to +85°C
Storage Temperature .....	-55°C to +125°C
Junction Temperature.....	+150°C
Lead Temperature (soldering, 10s).....	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Short-circuit to ground.

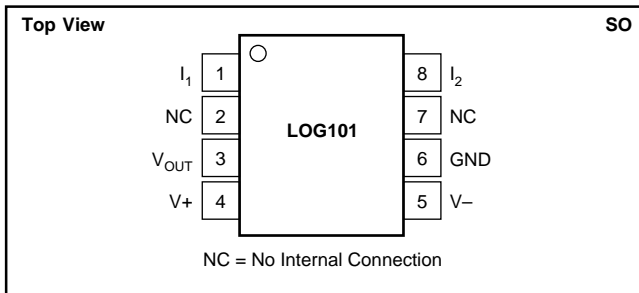


## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN DESCRIPTION



## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
LOG101AID	SO-8	D	-5°C to +75°C	LOG101	LOG101AID	Rails, 100
"	"	"	"	"	LOG101AIDR	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

## ELECTRICAL CHARACTERISTICS

**Boldface** limits apply over the specified temperature range,  $T_A = -5^\circ\text{C}$  to  $+75^\circ\text{C}$ .

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$ , and  $R_{OUT} = 10\text{k}\Omega$ , unless otherwise noted.

PARAMETER	CONDITION	LOG101AID			UNITS
		MIN	TYP	MAX	
<b>CORE LOG FUNCTION</b> $I_{IN}/V_{OUT}$ Equation		$V_O = (1V) \cdot \log(I_1/I_2)$			V
<b>LOG CONFORMITY ERROR<sup>(1)</sup></b> Initial	1nA to 100 $\mu$ A (5 decades) 100pA to 3.5mA (7.5 decades)		0.01 0.06	0.2	% %
<b>over Temperature</b>	<b>1nA to 100<math>\mu</math>A (5 decades)</b> 100pA to 3.5mA (7.5 decades) <sup>(2)</sup>		0.0001 0.0005		<b>%/°C</b> <b>%/°C</b>
<b>GAIN<sup>(3)</sup></b> Initial Value	1nA to 100 $\mu$ A		1		V/decade
Gain Error	1nA to 100 $\mu$ A		0.15	±1	%
<b>vs Temperature</b>	<b><math>T_{MIN}</math> to <math>T_{MAX}</math></b>		<b>0.003</b>	<b>0.01</b>	<b>%/°C</b>
<b>INPUT, A1 and A2</b> Offset Voltage	$T_{MIN}$ to $T_{MAX}$ $V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$		±0.3	±1.5	mV
<b>vs Temperature</b>			±2		$\mu\text{V}/^\circ\text{C}$
vs Power Supply (PSRR)			5	50	$\mu\text{V}/\text{V}$
Input Bias Current			±5		pA
<b>vs Temperature</b>	<b><math>T_{MIN}</math> to <math>T_{MAX}</math></b>		<b>Doubles Every 10°C</b>		
Voltage Noise	$f = 10\text{Hz}$ to $10\text{kHz}$		3		$\mu\text{Vrms}$
Current Noise	$f = 1\text{kHz}$		30		$\text{nV}/\sqrt{\text{Hz}}$
Common-Mode Voltage Range (Positive)		(V+) - 2	(V+) - 1.5		V
(Negative)		(V-) + 2	(V-) + 1.2		V
Common-Mode Rejection Ratio (CMRR)			105		dB
<b>OUTPUT, A2 (<math>V_{OUT}</math>)</b> Output Offset, $V_{OSO}$ , Initial	$T_{MIN}$ to $T_{MAX}$ $V_S = \pm 5\text{V}$		±3	±15	mV
<b>vs Temperature</b>			±2		$\mu\text{V}/^\circ\text{C}$
Full-Scale Output (FSO)		(V-) + 1.2		(V+) - 1.5	V
Short-Circuit Current			±18		mA

# ELECTRICAL CHARACTERISTICS (Cont.)

**Boldface** limits apply over the specified temperature range,  $T_A = -5^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$ .

At  $T_A = +25^{\circ}\text{C}$ ,  $V_S = \pm 5\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

PARAMETER	CONDITION	LOG101AID			UNITS	
		MIN	TYP	MAX		
<b>TOTAL ERROR</b> <sup>(4)(5)</sup> Initial	$I_1$ or $I_2$ remains fixed while other varies. Min to Max					
	$I_1$ or $I_2 = 3.5\text{mA}$			$\pm 75$	mV	
	$I_1$ or $I_2 = 1\text{mA}$			$\pm 20$	mV	
	$I_1$ or $I_2 = 100\mu\text{A}$			$\pm 20$	mV	
	$I_1$ or $I_2 = 10\mu\text{A}$			$\pm 20$	mV	
	$I_1$ or $I_2 = 1\mu\text{A}$			$\pm 20$	mV	
	$I_1$ or $I_2 = 100\text{nA}$			$\pm 20$	mV	
	$I_1$ or $I_2 = 10\text{nA}$			$\pm 20$	mV	
	$I_1$ or $I_2 = 1\text{nA}$			$\pm 20$	mV	
	$I_1$ or $I_2 = 350\text{pA}$			$\pm 20$	mV	
	$I_1$ or $I_2 = 100\text{pA}$			$\pm 20$	mV	
	<b>vs Temperature</b>	<b><math>I_1</math> or <math>I_2 = 3.5\text{mA}</math></b>		$\pm 1.2$		<b>mV/°C</b>
		<b><math>I_1</math> or <math>I_2 = 1\text{mA}</math></b>		$\pm 0.4$		<b>mV/°C</b>
		<b><math>I_1</math> or <math>I_2 = 100\mu\text{A}</math></b>		$\pm 0.1$		<b>mV/°C</b>
		<b><math>I_1</math> or <math>I_2 = 10\mu\text{A}</math></b>		$\pm 0.05$		<b>mV/°C</b>
		<b><math>I_1</math> or <math>I_2 = 1\mu\text{A}</math></b>		$\pm 0.05$		<b>mV/°C</b>
		<b><math>I_1</math> or <math>I_2 = 100\text{nA}</math></b>		$\pm 0.09$		<b>mV/°C</b>
		<b><math>I_1</math> or <math>I_2 = 10\text{nA}</math></b>		$\pm 0.2$		<b>mV/°C</b>
		<b><math>I_1</math> or <math>I_2 = 1\text{nA}</math></b>		$\pm 0.3$		<b>mV/°C</b>
		<b><math>I_1</math> or <math>I_2 = 350\text{pA}</math></b>		$\pm 0.1$		<b>mV/°C</b>
<b><math>I_1</math> or <math>I_2 = 100\text{pA}</math></b>			$\pm 0.3$		<b>mV/°C</b>	
<b>vs Supply</b>	$I_1$ or $I_2 = 3.5\text{mA}$		$\pm 3.0$		mV/V	
	$I_1$ or $I_2 = 1\text{mA}$		$\pm 0.1$		mV/V	
	$I_1$ or $I_2 = 100\mu\text{A}$		$\pm 0.1$		mV/V	
	$I_1$ or $I_2 = 10\mu\text{A}$		$\pm 0.1$		mV/V	
	$I_1$ or $I_2 = 1\mu\text{A}$		$\pm 0.1$		mV/V	
	$I_1$ or $I_2 = 100\text{nA}$		$\pm 0.1$		mV/V	
	$I_1$ or $I_2 = 10\text{nA}$		$\pm 0.1$		mV/V	
	$I_1$ or $I_2 = 1\text{nA}$		$\pm 0.25$		mV/V	
	$I_1$ or $I_2 = 350\text{pA}$		$\pm 0.1$		mV/V	
	$I_1$ or $I_2 = 100\text{pA}$		$\pm 0.1$		mV/V	
<b>FREQUENCY RESPONSE, CORE LOG</b> <sup>(6)</sup> BW, 3dB	$I_2 = 10\text{nA}$	$C_C = 4500\text{pF}$	0.1		kHz	
	$I_2 = 1\mu\text{A}$	$C_C = 150\text{pF}$	38		kHz	
	$I_2 = 10\mu\text{A}$	$C_C = 150\text{pF}$	40		kHz	
	$I_2 = 1\text{mA}$	$C_C = 50\text{pF}$	45		kHz	
	Step Response Increasing	$I_2 = 1\mu\text{A}$ to $1\text{mA}$	$C_C = 150\text{pF}$	11		$\mu\text{s}$
		$I_2 = 100\text{nA}$ to $1\mu\text{A}$	$C_C = 150\text{pF}$	7		$\mu\text{s}$
	Decreasing	$I_2 = 10\text{nA}$ to $100\text{nA}$	$C_C = 150\text{pF}$	110		$\mu\text{s}$
		$I_2 = 1\text{mA}$ to $1\mu\text{A}$	$C_C = 150\text{pF}$	45		$\mu\text{s}$
	Operating Range	$I_2 = 1\mu\text{A}$ to $100\text{nA}$	$C_C = 150\text{pF}$	20		$\mu\text{s}$
		$I_2 = 100\text{nA}$ to $10\text{nA}$	$C_C = 150\text{pF}$	550		$\mu\text{s}$
<b>POWER SUPPLY</b> Operating Range	$V_S$		$\pm 4.5$		V	
	Quiescent Current $I_O = 0$		$\pm 1$		mA	
<b>TEMPERATURE RANGE</b> Specified Range, $T_{\text{MIN}}$ to $T_{\text{MAX}}$ Operating Range Storage Range Thermal Resistance, $\theta_{\text{JA}}$ SO-8			-5	75	°C	
			-40	85	°C	
			-55	125	°C	
				150	°C/W	

NOTES: (1) Log Conformity Error is peak deviation from the best-fit straight line of  $V_{\text{OUT}}$  versus  $\log(I_1/I_2)$  curve expressed as a percent of peak-to-peak full-scale.

(2) May require higher supply for full dynamic range.

(3) Output core log function is trimmed to 1V output per decade change of input current.

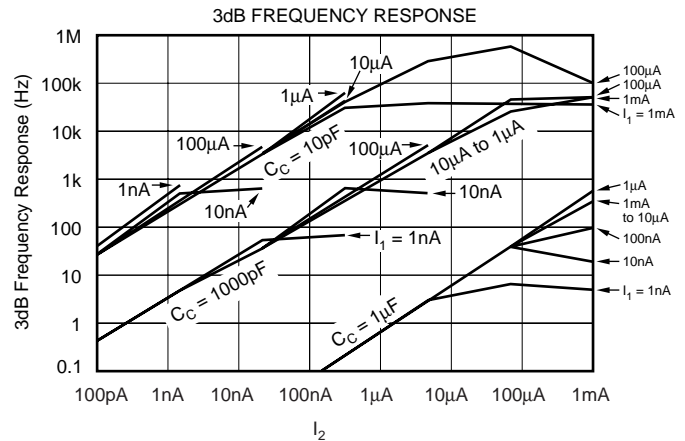
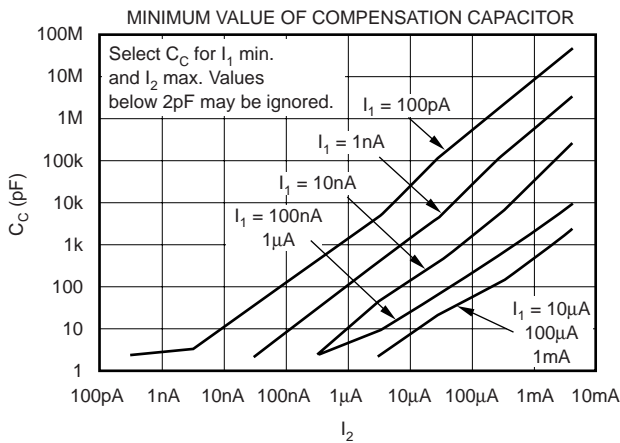
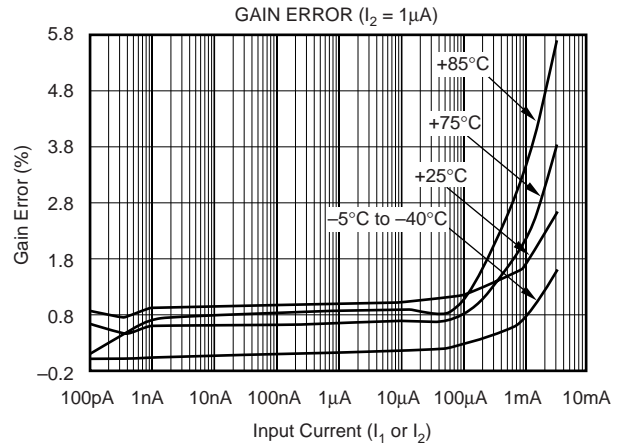
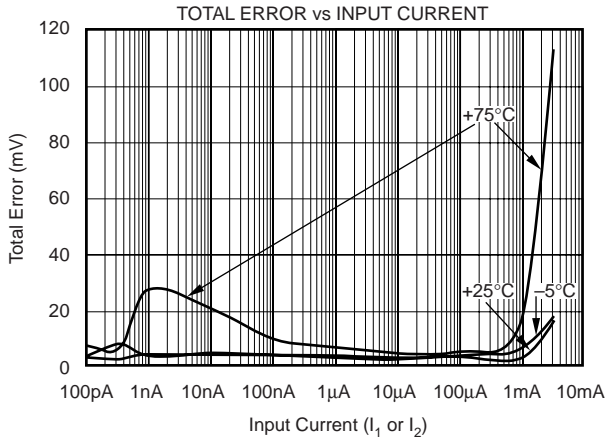
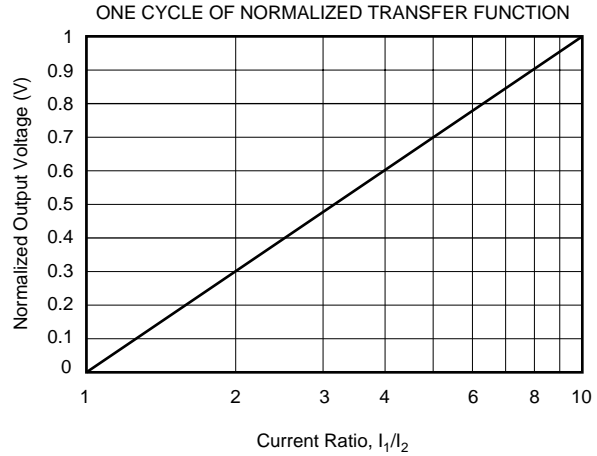
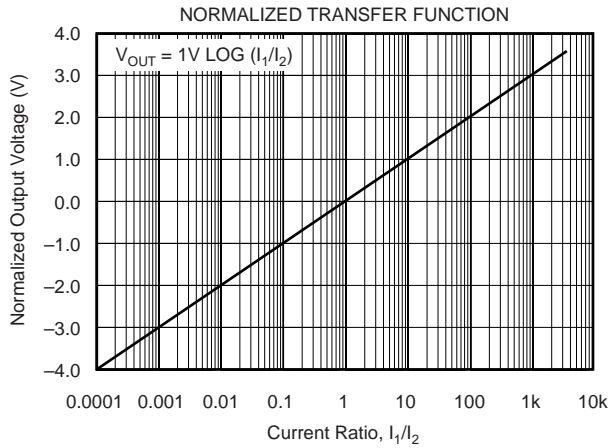
(4) Worst-case Total Error for any ratio of  $I_1/I_2$  is the largest of the two errors, when  $I_1$  and  $I_2$  are considered separately.

(5) Total  $I_1 + I_2$  should be kept below 4.5mA on  $\pm 5\text{V}$  supply.

(6) Bandwidth (3dB) and transient response are a function of both the compensation capacitor and the level of input current.

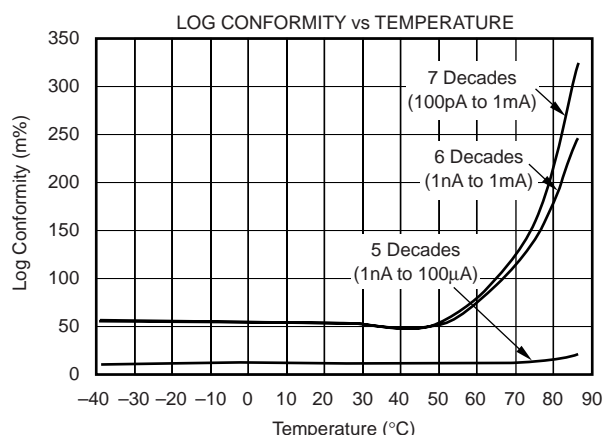
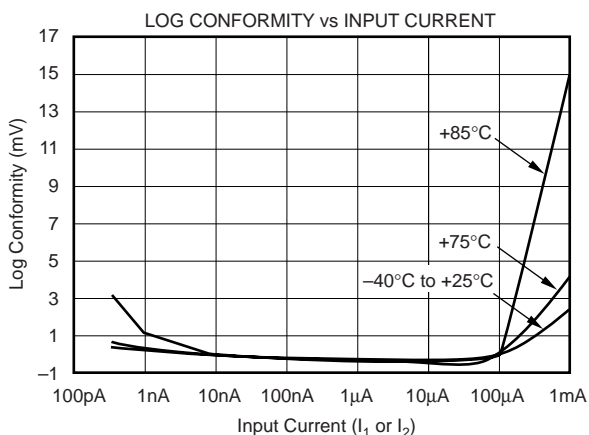
# TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



## APPLICATION INFORMATION

The LOG101 is a true logarithmic amplifier that uses the base-emitter voltage relationship of bipolar transistors to compute the logarithm, or logarithmic ratio of a current ratio.

Figure 1 shows the basic connections required for operation of the LOG101. In order to reduce the influence of lead inductance of power-supply lines, it is recommended that each supply be bypassed with a  $10\mu\text{F}$  tantalum capacitor in parallel with a  $1000\text{pF}$  ceramic capacitor, as shown in Figure 1. Connecting the capacitors as close to the LOG101 as possible will contribute to noise reduction as well.

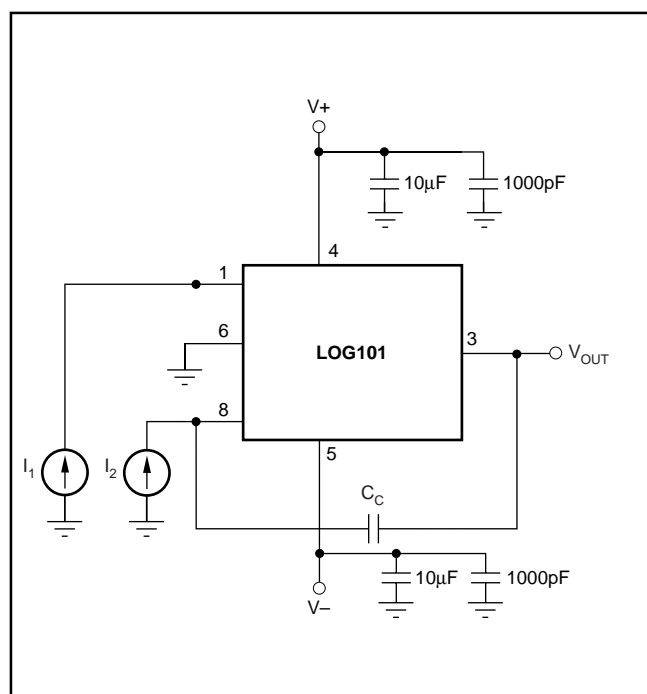


FIGURE 1. Basic Connections of the LOG101.

## INPUT CURRENT RANGE

To maintain specified accuracy, the input current range of the LOG101 should be limited from 100pA to 3.5mA. Input currents outside of this range may compromise LOG101 performance. Input currents larger than 3.5mA result in increased nonlinearity. An absolute maximum input current rating of 10mA is included to prevent excessive power dissipation that may damage the logging transistor.

On  $\pm 5\text{V}$  supplies, the total input current ( $I_1 + I_2$ ) is limited to 4.5mA. Due to compliance issues internal to the LOG101, to accommodate larger total input currents, supplies should be increased.

Currents smaller than 100pA will result in increased errors due to the input bias currents of op amps  $A_1$  and  $A_2$  (typically 5pA). The input bias currents may be compensated for, as shown in Figure 2. The input stages of the amplifiers have FET inputs, with input bias current doubling every  $10^\circ\text{C}$ , which makes the nulling technique shown practical only where the temperature is fairly stable.

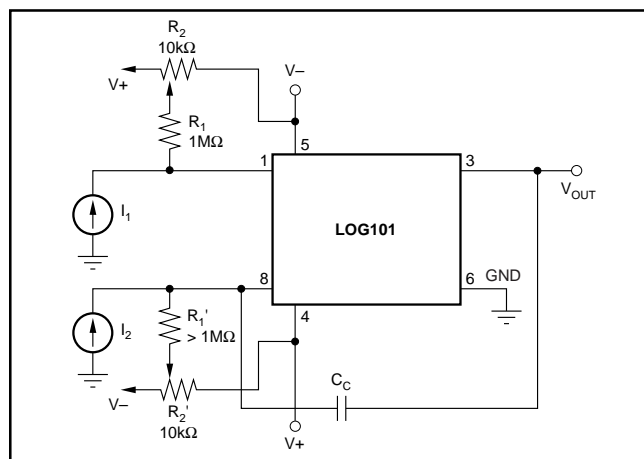


FIGURE 2. Bias Current Nulling.



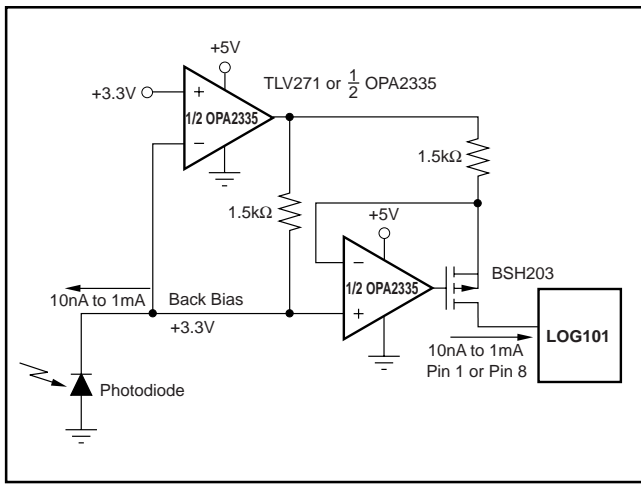


FIGURE 7. Precision Current Inverter/Current Source.

### VOLTAGE INPUTS

The LOG101 gives the best performance with current inputs. Voltage inputs may be handled directly with series resistors, but the dynamic input range is limited to approximately three decades of input voltage by voltage noise and offsets. The transfer function of Equation (13) applies to this configuration.

## APPLICATION CIRCUITS

### LOG RATIO

One of the more common uses of log ratio amplifiers is to measure absorbance. A typical application is shown in Figure 9.

$$\text{Absorbance of the sample is } A = \log \lambda_1' / \lambda_1 \quad (3)$$

$$\text{If } D_1 \text{ and } D_2 \text{ are matched } A \propto (1V) \log I_1 / I_2 \quad (4)$$

### DATA COMPRESSION

In many applications the compressive effects of the logarithmic transfer function are useful. For example, a LOG101 preceding a 12-bit Analog-to-Digital (A/D) converter can produce the dynamic range equivalent to a 20-bit converter.

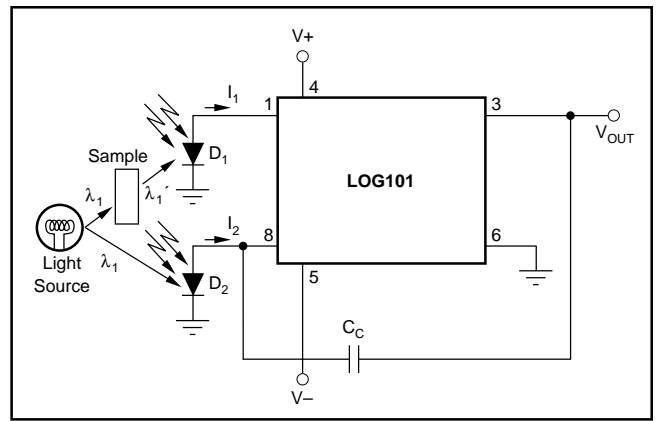


FIGURE 9. Absorbance Measurement.

### OPERATION ON SINGLE SUPPLY

Many applications do not have the dual supplies required to operate the LOG101. Figure 10 shows the LOG101 configured for operation with a single +5V supply.

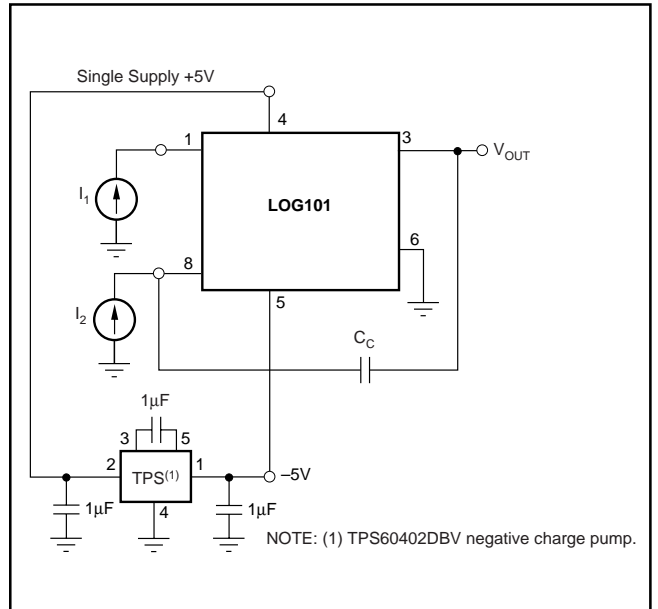


FIGURE 10. Single +5V Power-Supply Operation.

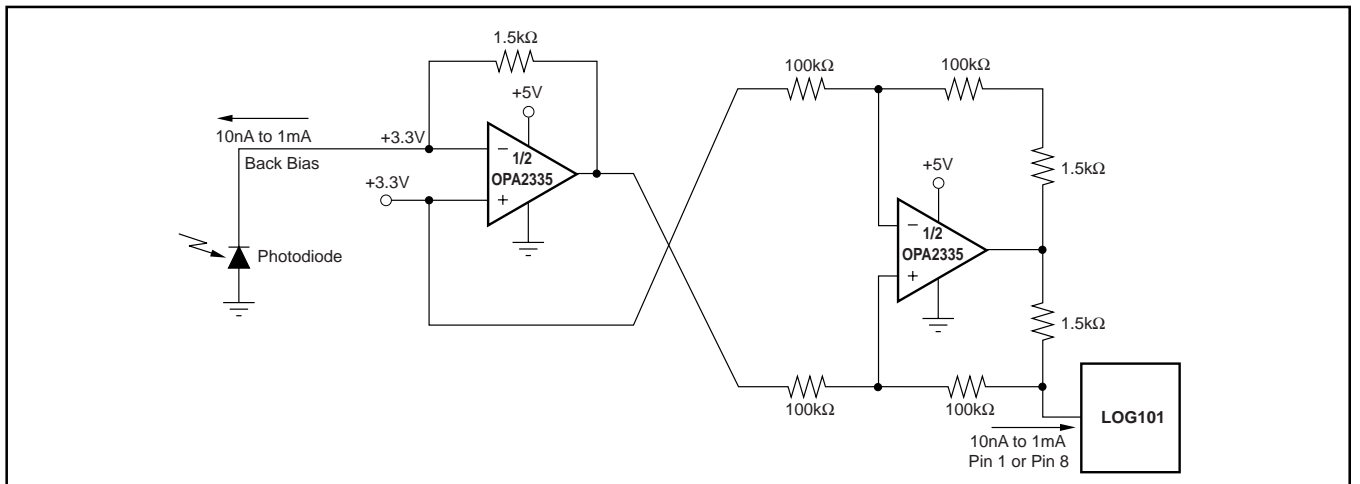


FIGURE 8. Precision Current Inverter/Current Source.

# INSIDE THE LOG101

Using the base-emitter voltage relationship of matched bipolar transistors, the LOG101 establishes a logarithmic function of input current ratios. Beginning with the base-emitter voltage defined as:

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \quad \text{where: } V_T = \frac{kT}{q} \quad (1)$$

$k$  = Boltzman's constant =  $1.381 \cdot 10^{-23}$

$T$  = Absolute temperature in degrees Kelvin

$q$  = Electron charge =  $1.602 \cdot 10^{-19}$  Coulombs

$I_C$  = Collector current

$I_S$  = Reverse saturation current

From the circuit in Figure 11, we see that:

$$V_L = V_{BE1} - V_{BE2} \quad (2)$$

Substituting (1) into (2) yields:

$$V_L = V_{T1} \ln \frac{I_1}{I_{S1}} - V_{T2} \ln \frac{I_2}{I_{S2}} \quad (3)$$

If the transistors are matched and isothermal and  $V_{T1} = V_{T2}$ , then (3) becomes:

$$V_L = V_{T1} \left[ \ln \frac{I_1}{I_S} - \ln \frac{I_2}{I_S} \right] \quad (4)$$

$$V_L = V_T \ln \frac{I_1}{I_2} \quad \text{and since} \quad (5)$$

$$\ln x = 2.3 \log_{10} x \quad (6)$$

$$V_L = n V_T \log \frac{I_1}{I_2} \quad (7)$$

$$\text{where } n = 2.3 \quad (8)$$

also

$$V_{OUT} = V_L \frac{R_1 + R_2}{R_1} \quad (9)$$

$$V_{OUT} = \frac{R_1 + R_2}{R_1} n V_T \log \frac{I_1}{I_2} \quad (10)$$

or

$$V_{OUT} = (1V) \cdot \log \frac{I_1}{I_2} \quad (11)$$

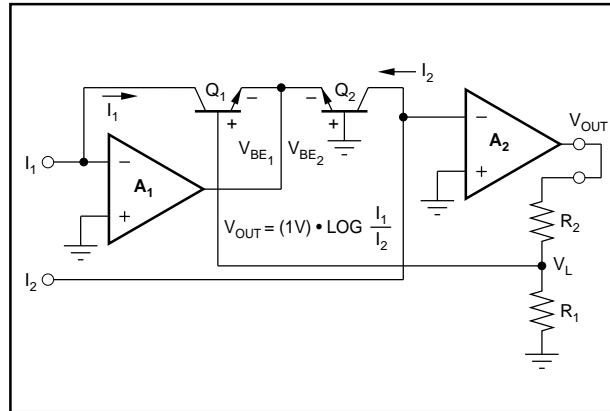


FIGURE 11. Simplified Model of a Log Amplifier.

It should be noted that the temperature dependence associated with  $V_T = kT/q$  is internally compensated on the LOG101 by making  $R_1$  a temperature sensitive resistor with the required positive temperature coefficient.

## DEFINITION OF TERMS

### TRANSFER FUNCTION

The ideal transfer function is:

$$V_{OUT} = 1V \cdot \log (I_1/I_2) \quad (5)$$

Figure 12 shows the graphical representation of the transfer over valid operating range for the LOG101.

### ACCURACY

Accuracy considerations for a log ratio amplifier are somewhat more complicated than for other amplifiers. This is because the transfer function is nonlinear and has two inputs, each of which can vary over a wide dynamic range. The accuracy for any combination of inputs is determined from the total error specification.

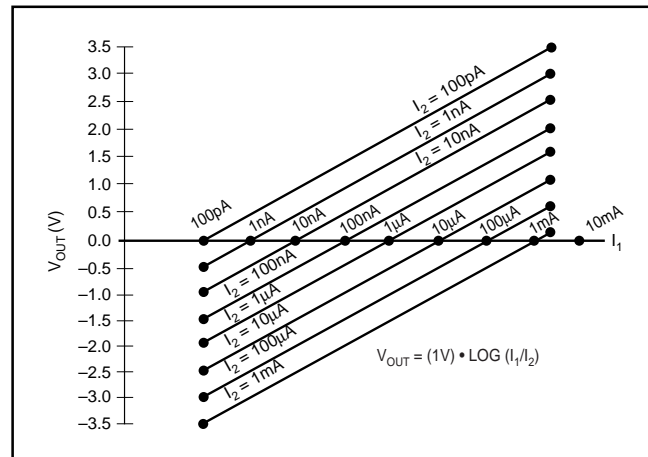


FIGURE 12. Transfer Function with Varying  $I_2$  and  $I_1$ .

## TOTAL ERROR

The total error is the deviation (expressed in mV) of the actual output from the ideal output of  $V_{OUT} = 1V \cdot \log(I_1/I_2)$ .

Thus,

$$V_{OUT(ACTUAL)} = V_{OUT(IDEAL)} \pm \text{Total Error.} \quad (6)$$

It represents the sum of all the individual components of error normally associated with the log amp when operated in the current input mode. The worst-case error for any given ratio of  $I_1/I_2$  is the largest of the two errors when  $I_1$  and  $I_2$  are considered separately. Temperature can affect total error.

## ERRORS RTO AND RTI

As with any transfer function, errors generated by the function itself may be Referred-to-Output (RTO) or Referred-to-Input (RTI). In this respect, log amps have a unique property:

Given some error voltage at the log amp's output, that error corresponds to a constant percent of the input regardless of the actual input level.

## USING A LARGER REFERENCE VOLTAGE REDUCES OFFSET ERRORS

Using a larger reference voltage to create the reference current minimizes errors due to the LOG101's input offset voltage. Maintaining an increasing output voltage as a function of increasing photodiode current is also important in many optical sensing applications. All zeros from the A/D converter output represent zero or low-scale photodiode current. Inputting the reference current into  $I_1$ , and designing  $I_{REF}$  such that it is as large or larger than the expected maximum photodiode current is accomplished using this requirement. The LOG101 configured with the reference current connecting  $I_1$  and the photodiode current connecting

to  $I_2$  is shown in Figure 13. The OPA703 is configured as a level shifter with inverting gain and is used to scale the photodiode current directly into the A/D converter input voltage range.

The wide dynamic range of the LOG101 is also useful for measuring avalanche photodiode current (APD) (see Figure 14).

## LOG CONFORMITY

For the LOG101, log conformity is calculated the same as linearity and is plotted  $I_1/I_2$  on a semi-log scale. In many applications, log conformity is the most important specification. This is because bias current errors are negligible (5pA compared to input currents of 100pA and above) and the scale factor and offset errors may be trimmed to zero or removed by system calibration. This leaves log conformity as the major source of error.

Log conformity is defined as the peak deviation from the best fit straight line of the  $V_{OUT}$  versus  $\log(I_1/I_2)$  curve. This is expressed as a percent of ideal full-scale output. Thus, the nonlinearity error expressed in volts over m decades is: (7)

$$V_{OUT(NONLIN)} = 1V/\text{dec} \cdot 2NmV$$

where N is the log conformity error, in percent.

## INDIVIDUAL ERROR COMPONENTS

The ideal transfer function with current input is:

$$V_{OUT} = (1V) \cdot \log \frac{I_1}{I_2} \quad (8)$$

The actual transfer function with the major components of error is:

$$V_{OUT} = (1V) (1 \pm \Delta K) \log \frac{I_1 - I_{B1}}{I_2 - I_{B2}} \pm 2Nm \pm V_{OS0} \quad (9)$$

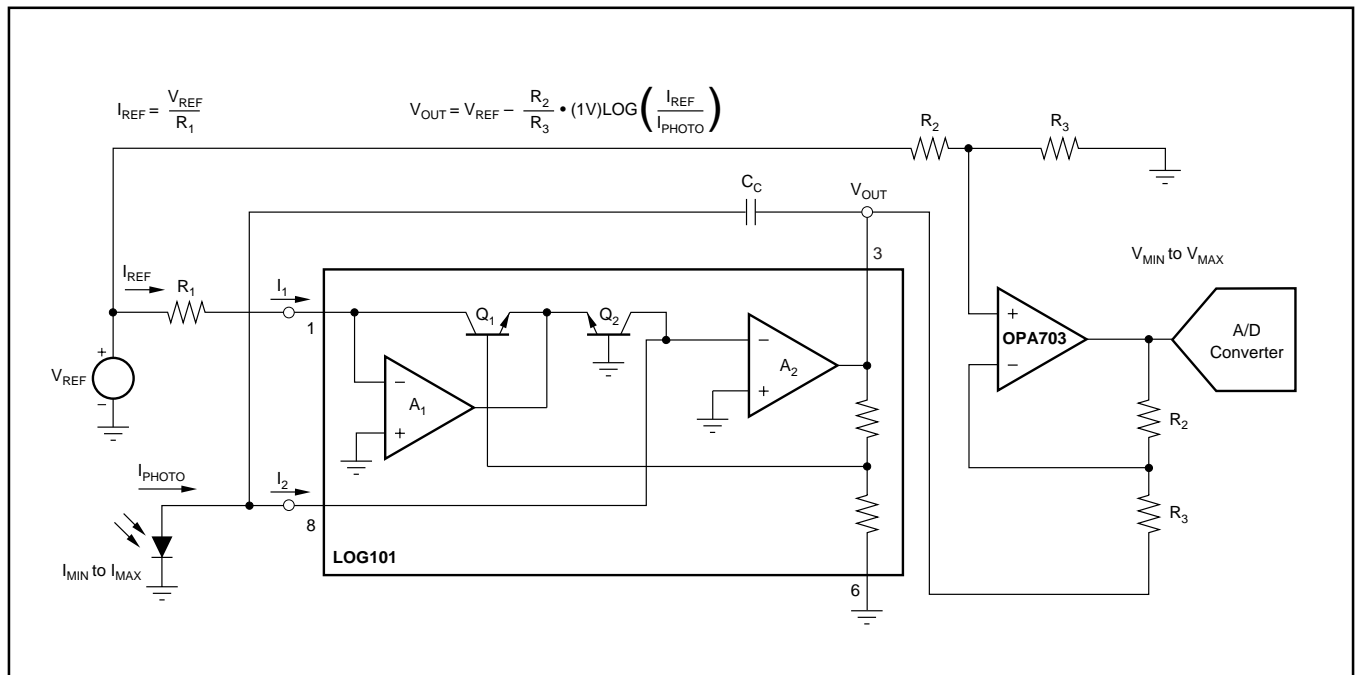


FIGURE 13. Technique for Using Full-Scale Reference Current Such that  $V_{OUT}$  Increases with Increasing Photodiode Current.

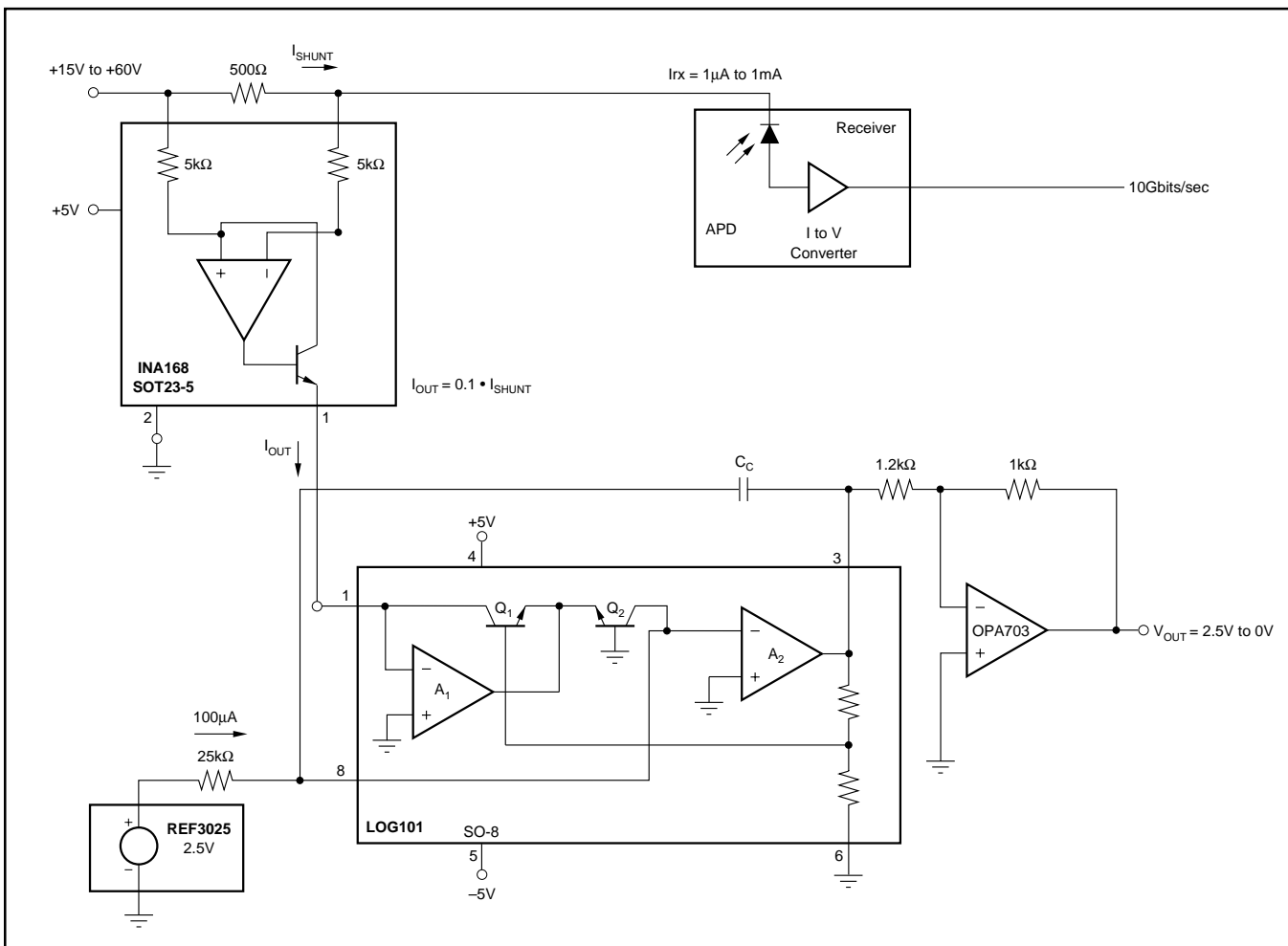


FIGURE 14. High Side Shunt for Avalanche Photodiode (APD) Measures 3-Decades of APD Current.

The individual component of error is:

$\Delta K$  = gain accuracy (0.15%, typ), as specified in the specification table.

$I_{B1}$  = bias current of  $A_1$  (5pA, typ)

$I_{B2}$  = bias current of  $A_2$  (5pA, typ)

$N$  = log conformity error (0.01%, 0.06%, typ)

0.01% for  $n = 5$ , 0.06% for  $n = 7$

$V_{OSO}$  = output offset voltage (3mV, typ)

$n$  = number of decades over which  $N$  is specified:

Example: what is the error when

$$I_1 = 1\mu\text{A} \text{ and } I_2 = 100\text{nA} \quad (10)$$

$$V_{OUT} = (1 \pm 0.0015) \log \frac{10^{-6} - 5 \cdot 10^{-12}}{10^{-7} - 5 \cdot 10^{-12}} \pm (2)(0.0001)5 \pm 3.0\text{mV} \\ = 1.005055\text{V} \quad (11)$$

Since the ideal output is 1.000V, the error as a percent of reading is

$$\% \text{ error} = \frac{0.005055}{1} \cdot 100\% = 0.5\% \quad (12)$$

For the case of voltage inputs, the actual transfer function is

$$V_{OUT} = (1V)(1 \pm \Delta K) \log \frac{\frac{V_1}{R_1} - I_{B1} \pm \frac{E_{OS1}}{R_1}}{\frac{V_2}{R_2} - I_{B2} \pm \frac{E_{OS2}}{R_2}} \pm 2Nn \pm V_{OSO} \quad (13)$$

Where  $\frac{E_{OS1}}{R_1}$  and  $\frac{E_{OS2}}{R_2}$  are considered to be zero for large values of resistance from external input current sources.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LOG101AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	LOG 101A	<a href="#">Samples</a>
LOG101AIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	LOG 101A	<a href="#">Samples</a>
LOG101AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	LOG 101A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LOG101AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LOG101AIDR	SOIC	D	8	2500	367.0	367.0	35.0

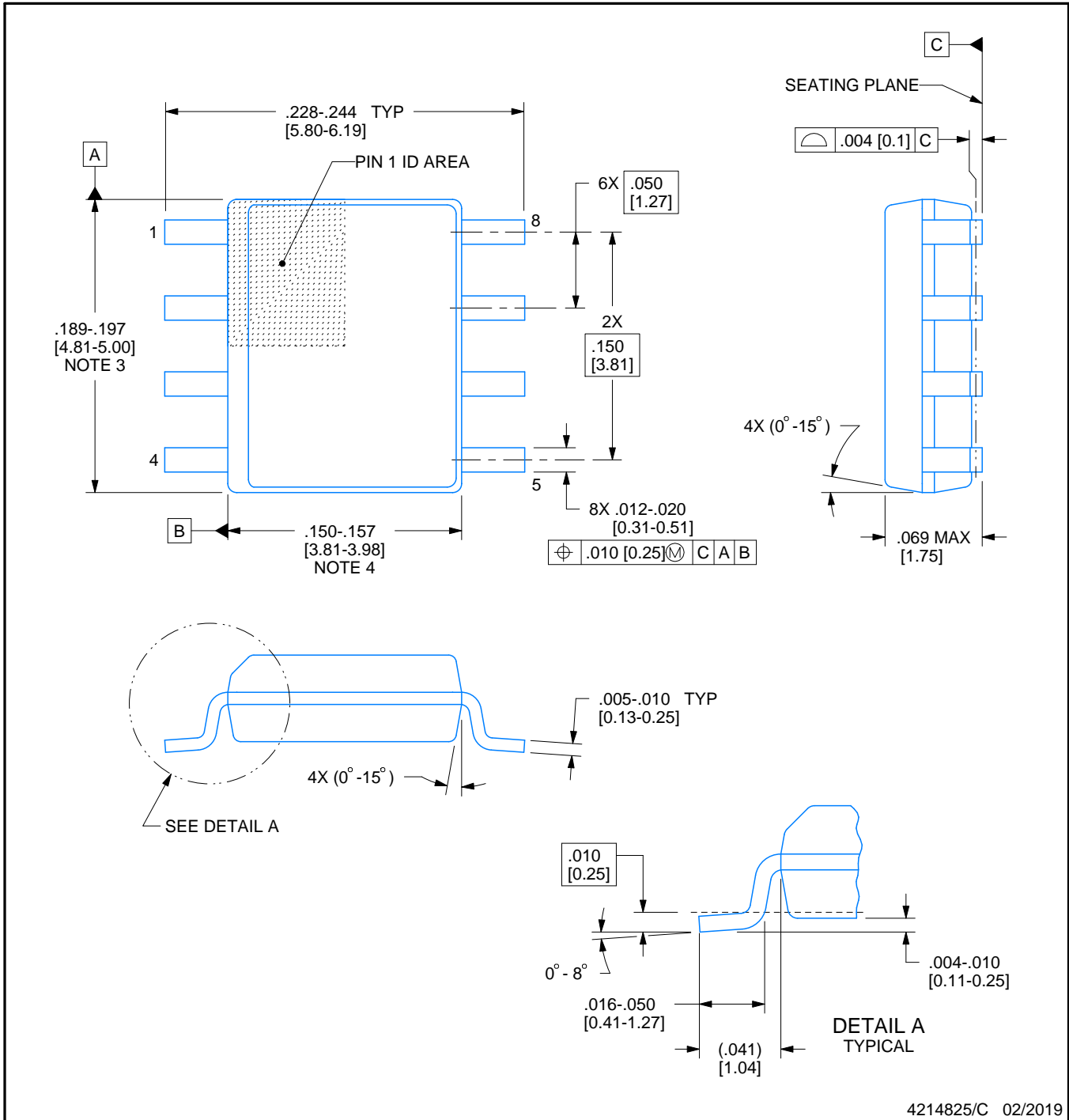


D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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