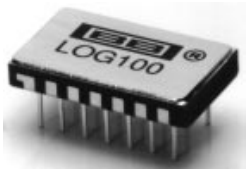
THE DATASHEET OF

LOG100JP

BURR - BROWN®



LOG100

Precision LOGARITHMIC AND LOG RATIO AMPLIFIER

FEATURES

- **ACCURACY**
  0.37% FSO max Total Error
  Over 5 Decades
- **LINEARITY**
  0.1% max Log Conformity
  Over 5 Decades
- **EASY TO USE**
  Pin-selectable Gains
  Internal Laser-trimmed Resistors
- **WIDE INPUT DYNAMIC RANGE**
  6 Decades, 1nA to 1mA
- **HERMETIC CERAMIC DIP**

APPLICATIONS

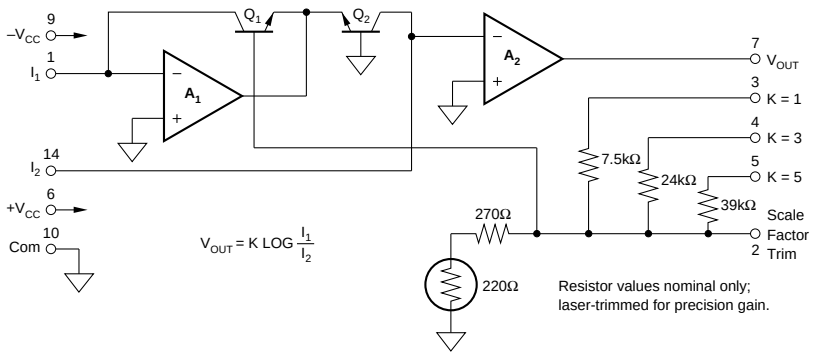
- **LOG, LOG RATIO AND ANTILOG COMPUTATIONS**
- **ABSORBANCE MEASUREMENTS**
- **DATA COMPRESSION**
- **OPTICAL DENSITY MEASUREMENTS**
- **DATA LINEARIZATION**
- **CURRENT AND VOLTAGE INPUTS**

DESCRIPTION

The LOG100 uses advanced integrated circuit technologies to achieve high accuracy, ease of use, low cost, and small size. It is the logical choice for your logarithmic-type computations. The amplifier has guaranteed maximum error specifications over the full six-decade input range (1nA to 1mA) and for all possible combinations of I_1 and I_2. Total error is guaranteed so that involved error computations are not necessary.

The circuit uses a specially designed compatible thin-film monolithic integrated circuit which contains amplifiers, logging transistors, and low drift thin-film resistors. The resistors are laser-trimmed for maximum precision. FET input transistors are used for the amplifiers whose low bias currents (1pA typical) permit signal currents as low as 1nA while maintaining guaranteed total errors of 0.37% FSO maximum.

Because scaling resistors are self-contained, scale factors of 1V, 3V or 5V per decade are obtained simply by pin selections. No other resistors are required for log ratio applications. The LOG100 will meet its guaranteed accuracy with no user trimming. Provisions are made for simple adjustments of scale factor, offset voltage, and bias current if enhanced performance is desired.



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SPECIFICATIONS

ELECTRICAL

T_A = +25°C and $\pm V_{CC}$ = ±15V, after 15 minute warm-up, unless otherwise specified.

PARAMETER	CONDITIONS	LOG100JP MIN	LOG100JP TYP	LOG100JP MAX	UNITS
TRANSFER FUNCTION			V_{OUT} = K Log (I_1/I_2)		
Log Conformity Error[1]	Either I_1 or I_2				
Initial	1nA to 100µA (5 decades)		0.04	0.1	%
	1nA to 1mA (6 decades)		0.15	0.25	%
Over Temperature	1nA to 100µA (5 decades)		0.002		%/°C
	1nA to 1mA (6 decades)		0.001		%/°C
K Range[2]			1, 3, 5		V/decade
Accuracy			0.3		%
Temperature Coefficient			0.03		%/°C
ACCURACY					
Total Error[3]	K = 1,[4] Current Input Operation				
Initial	I_1, I_2 = 1mA			±55	mV
	I_1, I_2 = 100µA			±30	mV
	I_1, I_2 = 10µA			±25	mV
	I_1, I_2 = 1µA			±20	mV
	I_1, I_2 = 100nA			±25	mV
	I_1, I_2 = 10nA			±30	mV
	I_1, I_2 = 1nA			±37	mV
vs Temperature	I_1, I_2 = 1mA		±0.20		mV/°C
	I_1, I_2 = 100µA		±0.37		mV/°C
	I_1, I_2 = 10µA		±0.28		mV/°C
	I_1, I_2 = 1µA		±0.033		mV/°C
	I_1, I_2 = 100nA		±0.28		mV/°C
	I_1, I_2 = 10nA		±0.51		mV/°C
	I_1, I_2 = 1nA		±1.26		mV/°C
vs Supply	I_1, I_2 = 1mA		±4.3		mV/V
	I_1, I_2 = 100µA		±1.5		mV/V
	I_1, I_2 = 10µA		±0.37		mV/V
	I_1, I_2 = 1µA		±0.11		mV/V
	I_1, I_2 = 100nA		±0.61		mV/V
	I_1, I_2 = 10nA		±0.91		mV/V
	I_1, I_2 = 1nA		±2.6		mV/V
INPUT CHARACTERISTICS (of Amplifiers A_1 and A_2)					
Offset Voltage					
Initial			±0.7	±5	mV
vs Temperature			±80		µV/°C
Bias Current					
Initial			1	5[5]	pA
vs Temperature			Doubles Every 10°C		
Voltage Noise	10Hz to 10kHz, RTI		3		µVrms
Current Noise	10Hz to 10kHz, RTI		0.5		pArms
AC PERFORMANCE					
3dB Response[6], I_2 = 10µA					
1nA	C_C = 4500pF		0.11		kHz
1µA	C_C = 150pF		38		kHz
10µA	C_C = 150pF		27		kHz
1mA	C_C = 50pF		45		kHz
Step Response[6]					
Increasing	C_C = 150pF				
1µA to 1mA			11		µs
100nA to 1µA			7		µs
10nA to 100nA			110		µs
Decreasing	C_C = 150pF				
1mA to 1µA			45		µs
1µA to 100nA			20		µs
100nA to 10nA			550		µs
OUTPUT CHARACTERISTICS					
Full Scale Output (FSO)		±10			V
Rated Output					
Voltage	I_{OUT} = ±5mA	±10			V
Current	V_{OUT} = ±10V	±5			mA
Current Limit					
Positive			12.5		mA
Negative			15		mA
Impedance			0.05		Ω

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = +25°C and $\pm V_{CC}$ = ±15V, after 15 minute warm-up, unless otherwise specified.

PARAMETER	CONDITIONS	LOG100JP MIN	LOG100JP TYP	LOG100JP MAX	UNITS
POWER SUPPLY REQUIREMENTS					
Rated Voltage			±15		VDC
Operating Range	Derated Performance	±12		±18	VDC
Quiescent Current			±7	±9	mA
AMBIENT TEMPERATURE RANGE					
Specification		0		+70	°C
Operating Range	Derated Performance	–25		+85	°C
Storage		–40		+85	°C

NOTES: (1) Log Conformity Error is the peak deviation from the best-fit straight line of the V_{OUT} vs Log I_{IN} curve expressed as a percent of peak-to-peak full scale output. (2) May be trimmed to other values. See Applications section. (3) The worst-case Total Error for any ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately. (4) Total Error at other values of K is K times Total Error for K = 1. (5) Guaranteed by design. Not directly measurable due to amplifier's committed configuration. (6) 3dB and transient response are a function of both the compensation capacitor and the level of input current. See Typical Performance Curves.

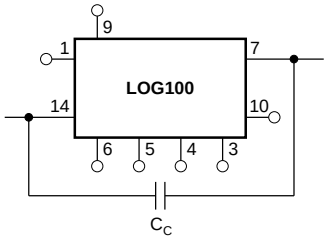
ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Internal Power Dissipation	600mV
Input Current	10mA
Input Voltage Range	±18V
Storage Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	175°C

SCALE FACTOR PIN CONNECTIONS

K, V/DECADE	CONNECTIONS
5	5 to 7
3	4 to 7
1.9	4 and 5 to 7
1	3 to 7
0.85	3 and 5 to 7
0.77	3 and 4 to 7
0.68	3 and 4 and 5 to 7

FREQUENCY COMPENSATION

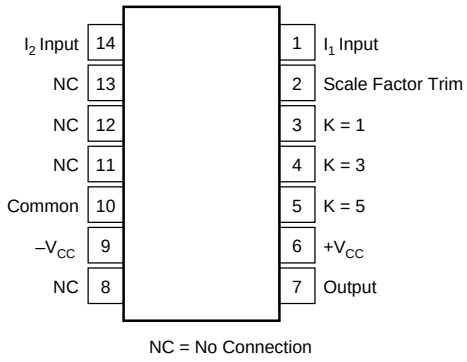


ORDERING INFORMATION

MODEL	PACKAGE	SPECIFIED TEMPERATURE RANGE
LOG100JP	14-Pin Hermetic Ceramic DIP	0°C to +70°C

PIN CONFIGURATION

Bottom View



NC = No Connection

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION

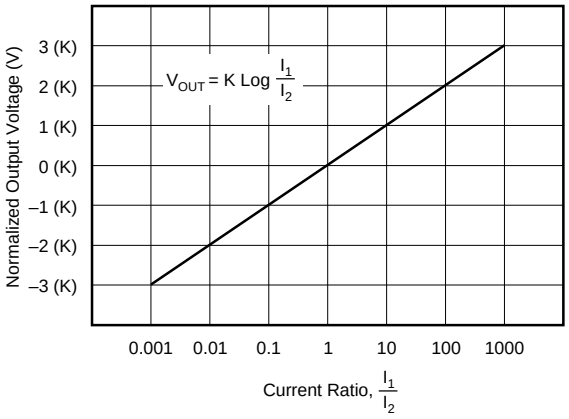
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
LOG100JP	14-Pin Hermetic Ceramic DIP	148(2)

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book. (2) During 1994, the package was changed from plastic to hermetic ceramic. Pinout, model number, and specifications remained unchanged. The metal lid of the new package is internally connected to common, pin 10.

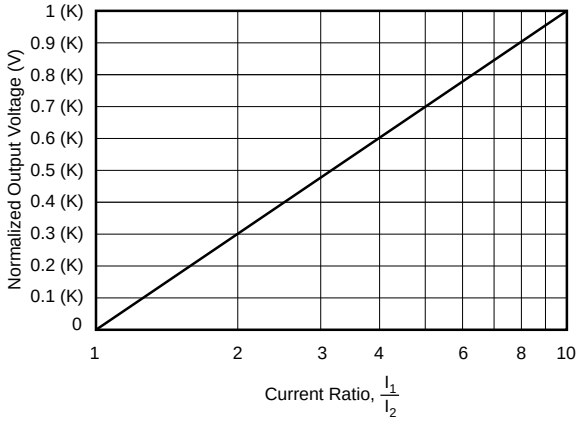
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC, unless otherwise noted.

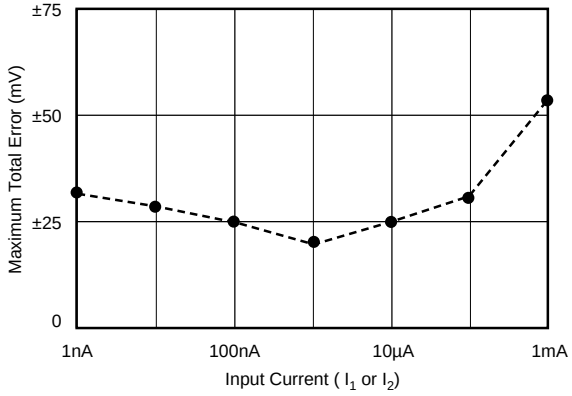
NORMALIZED TRANSFER FUNCTION



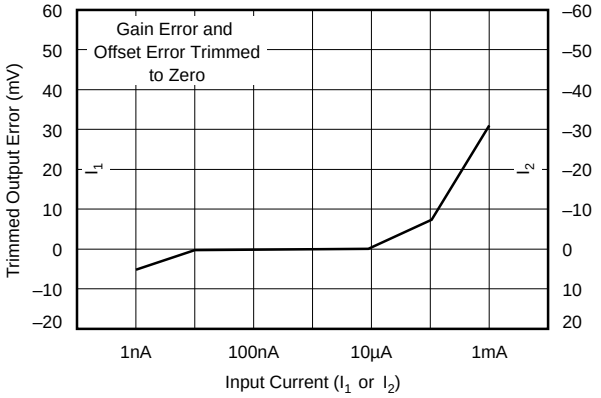
ONE CYCLE OF NORMALIZED TRANSFER FUNCTION



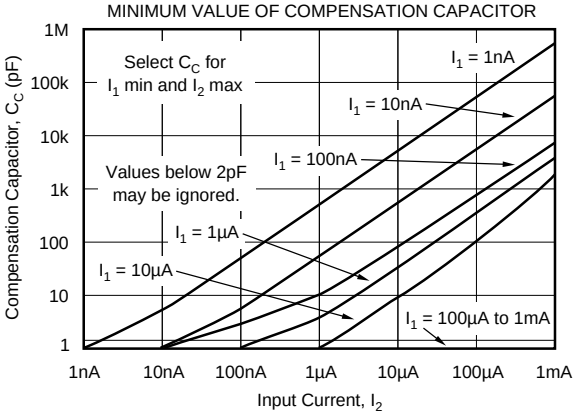
TOTAL ERROR vs INPUT CURRENT



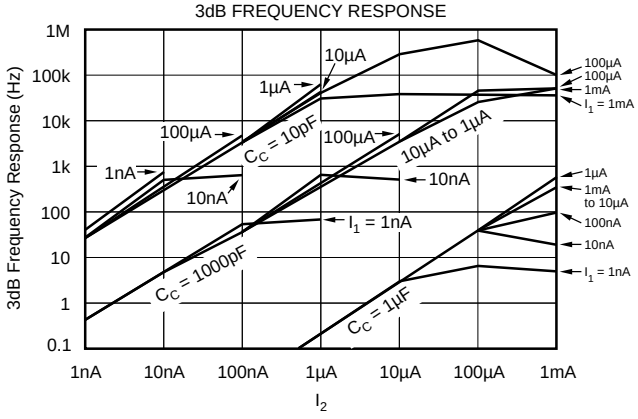
TRIMMED OUTPUT ERROR vs INPUT CURRENT



MINIMUM VALUE OF COMPENSATION CAPACITOR



3dB FREQUENCY RESPONSE



THEORY OF OPERATION

The base-emitter voltage of a bipolar transistor is

$$V_{BE} = V_T \ell n \frac{I_C}{I_S} \quad \text{where: } V_T = \frac{KT}{q} \tag{1}$$

K = Boltzman's constant = 1.381 x 10^{-23}

T = Absolute temperature in degrees Kelvin

q = Electron charge = 1.602 x 10^{-19} Coulombs

I_C = Collector current

I_S = Reverse saturation current

From the circuit in Figure 1, we see that

$$V_{OUT}' = V_{BE_1} - V_{BE_2} \tag{2}$$

Substituting (1) into (2) yields

$$V_{OUT}' = V_{T_1} \ell n \frac{I_1}{I_{S_1}} - V_{T_2} \ell n \frac{I_1}{I_{S_2}} \tag{3}$$

If the transistors are matched and isothermal and $V_{T1} = V_{T2}$, then (3) becomes:

$$V_{OUT}' = V_T \left[\ell n \frac{I_1}{I_S} - \ell n \frac{I_2}{I_S}\right] \tag{4}$$

$$V_{OUT}' = V_T \ell n \frac{I_1}{I_2} \text{ and since} \tag{5}$$

$$\ell n\, x = 2.3 \log_{10} x \tag{6}$$

$$V_{OUT}' = n\, V_T \log \frac{I_1}{I_2} \tag{7}$$

where n = 2.3 (8)

also

$$V_{OUT} = V_{OUT}' \frac{R_1 + R_2}{R_1} \tag{9}$$

$$= \frac{R_1 + R_2}{R_1} n\, V_T \log \frac{I_1}{I_2} \tag{10}$$

or

$$V_{OUT} = K \log \frac{I_1}{I_2} \tag{11}$$

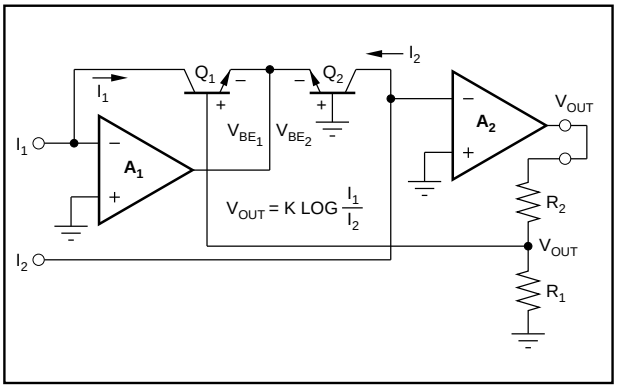


FIGURE 1. Simplified Model of Log Amplifier.

It should be noted that the temperature dependance associated with V_T = KT/q is compensated by making R_1 a temperature sensitive resistor with the required positive temperature coefficient.

DEFINITION OF TERMS

TRANSFER FUNCTION

The ideal transfer function is $V_{OUT} = K \log \frac{I_1}{I_2}$

where:

K = the scale factor with units of volts/decade

I_1 = numerator input current

I_2 = denominator input current.

ACCURACY

Accuracy considerations for a log ratio amplifier are somewhat more complicated than for other amplifiers. The reason is that the transfer function is nonlinear and has two inputs, each of which can vary over a wide dynamic range. The accuracy for any combination of inputs is determined from the total error specification.

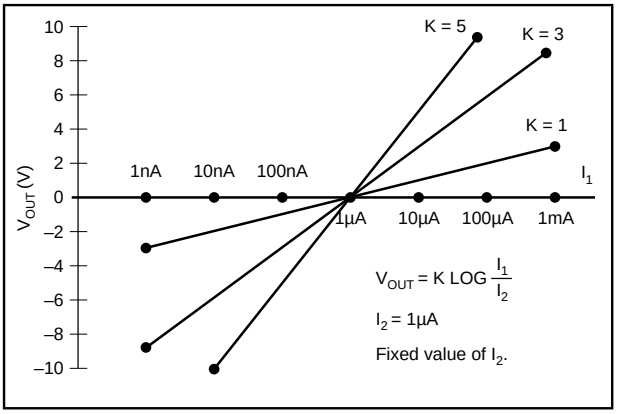


FIGURE 2. Transfer Function with Varying K and I_1.

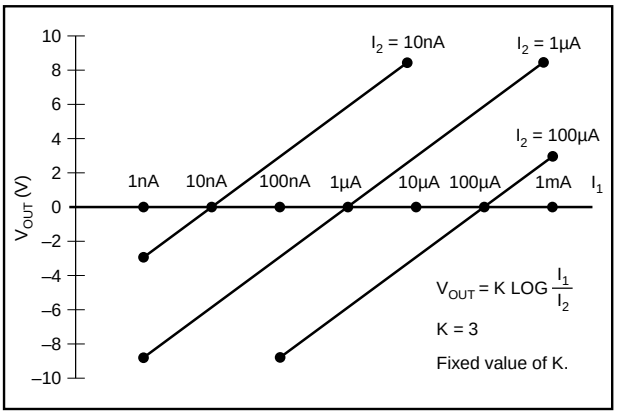


FIGURE 3. Transfer Function with Varying I_2 and I_1.

TOTAL ERROR

The total error is the deviation (expressed in mV) of the actual output from the ideal output of $V_{OUT} = K \log (I_1/I_2)$. Thus,

$$V_{OUT\ (ACTUAL)} = V_{OUT\ (IDEAL)} \pm \text{Total Error.}$$

It represents the sum of all the individual components of error normally associated with the log amp when operated in the current input mode. The worst-case error for any given ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately.

Example:

I_1 varies over a range of 10nA to 1µA and I_2 varies from 100nA to 10µA. What is the maximum error?

Table I shows the maximum errors for each decade combination of I_1 and I_2.

I_2 (maximum error)[1] \ I_1 (maximum error)[1]	10nA (30mV)	100nA (25mV)	1µA (20mV)
100nA (25mV)	0.1 (30mV)	1 (25mV)	10 (25mV)
1µA (20mV)	0.01 (30mV)	0.1 (25mV)	1 (20mV)
10µA (25mV)	0.001 (30mV)	0.01 (25mV)	0.1 (25mV)

NOTE: (1) Maximum errors are in parenthesis.

TABLE I. I_1/I_2 and Maximum Errors.

Since the largest value of I_1/I_2 is 10 and the smallest is 0.001, K is set at 3V per decade so the output will range from +3V to –9V. The maximum total error occurs when I_1 = 10nA and is equal to K x 30mV. This represents a 0.75% of peak-to-peak FSO error 3 x 0.030/12 x 100% = 0.75% where the full scale output is 12V (from +3V to –9V).

ERRORS RTO AND RTI

As with any transfer function, errors generated by the function itself may be Referred-to-Output (RTO) or Referred-to-Input (RTI). In this respect, log amps have a unique property:

> Given some error voltage at the log amp's output, that error corresponds to a constant percent of the input regardless of the actual input level.

Refer to: Yu Jen Wong and William E. Ott, "Function Circuits: Design & Applications", McGraw-Hill Book, 1976.

LOG CONFORMITY

Log conformity corresponds to linearity when V_{OUT} is plotted versus I_1/I_2 on a semilog scale. In many applications, log conformity is the most important specification. This is true because bias current errors are negligible (1pA compared to input currents of 1nA and above) and the scale factor and offset errors may be trimmed to zero or removed by system calibration. This leaves log conformity as the major source of error.

Log conformity is defined as the peak deviation from the best-fit straight line of the V_{OUT} versus log (I_1/I_2) curve. This is expressed as a percent of peak-to-peak full scale output. Thus, the nonlinearity error expressed in volts over m decades is

$$V_{OUT\ (NONLIN)} = K\ 2Nm\ V \tag{12}$$

where N is the log conformity error, in percent.

INDIVIDUAL ERROR COMPONENTS

The ideal transfer function with current input is

$$V_{OUT} = K \text{ Log } \frac{I_1}{I_2} \tag{13}$$

The actual transfer function with the major components of error is

$$V_{OUT} = K\ (1 \pm \Delta K) \log \frac{I_1 - I_{B1}}{I_2 - I_{B2}} \pm K\ 2Nm \pm V_{OS\ OUT} \tag{14}$$

The individual component of error is

ΔK = scale factor error (0.3%, typ)
I_{B1} = bias current of A_1 (1pA, typ)
I_{B2} = bias current of A_2 (1pA, typ)
N = log conformity error (0.05%, 0.1%, typ)
$V_{OS\ OUT}$ = output offset voltage (1mV, typ)
m = number of decades over which N is specified:
0.05% for m = 5, 0.1% for m = 6

Example: what is the error with K = 3 when

I_1 = 1µA and I_2 = 100nA

$$V_{OUT} = 3(1 \pm 0.003) \log \frac{10^{-6} - 10^{-12}}{10^{-7} - 10^{-12}} \pm 3(2)(0.0005)5 \pm 1\text{mV} \tag{15}$$

$$\approx 3.009 \log \frac{10^{-6}}{10^{-7}} + 0.015 + 0.001 \tag{16}$$

$$= 3.009\ (1) + 0.015 + 0.001 \tag{17}$$

$$= 3.025\text{V} \tag{18}$$

Since the ideal output is 3.000V, the error as a percent of reading is

$$\%\ \text{error} = \frac{0.025}{3} \text{ x } 100\% = 0.83\% \tag{19}$$

For the case of voltage inputs, the actual transfer function is

$$V_{OUT} = K(1 \pm \Delta K) \log \frac{\frac{V_1}{R_1} - I_{B_1} \pm \frac{E_{OS_1}}{R_1}}{\frac{V_2}{R_2} - I_{B_2} \pm \frac{E_{OS_2}}{R_2}} \pm K\ 2Nm \pm V_{OS\ OUT} \tag{20}$$

FREQUENCY RESPONSE

The 3dB frequency response of the LOG100 is a function of the magnitude of the input current levels and of the value of the frequency compensation capacitor. See Typical Performance Curves for details.

The frequency response curves are shown for constant DC I_1 and I_2 with a small signal AC current on one of them.

The transient response of the LOG100 is different for increasing and decreasing signals. This is due to the fact that a log amp is a nonlinear gain element and has different gains at different levels of input signals. Frequency response decreases as the gain increases.

GENERAL INFORMATION

INPUT CURRENT RANGE

The stated input range of 1nA to 1mA is the range for specified accuracy. Smaller or larger input currents may be applied with decreased accuracy. Currents larger than 1mA result in increased nonlinearity. The 10mA absolute maximum is a conservative value to limit the power dissipation in the output stage of A_1 and the logging transistor. Currents below 1nA will result in increased errors due to the input bias currents of A_1 and A_2 (1pA typical). These errors may be nulled. See Optional Adjustments section.

FREQUENCY COMPENSATION

Frequency compensation for the LOG100 is obtained by connecting a capacitor between pins 7 and 14. The size of the capacitor is a function of the input currents as shown in the Typical Performance Curves. For any given application, the smallest value of the capacitor which may be used is determined by the maximum value at I_2 and the minimum value of I_1. Larger values of C_C will make the LOG100 more stable, but will reduce the frequency response.

SETTING THE REFERENCE CURRENT

When the LOG100 is used as a straight log amplifier I_2 is constant and becomes the reference current in the expression

$$V_{OUT} = K \log \frac{I_1}{I_{REF}} \qquad (21)$$

I_{REF} can be derived from an external current source (such as shown in Figure 4), or it may be derived from a voltage source with one or more resistors.

When a single resistor is used, the value may be quite large when I_{REF} is small. If I_{REF} is 10nA and +15V is used

$$R_{REF} = \frac{15V}{10nA} = 1500M\Omega.$$

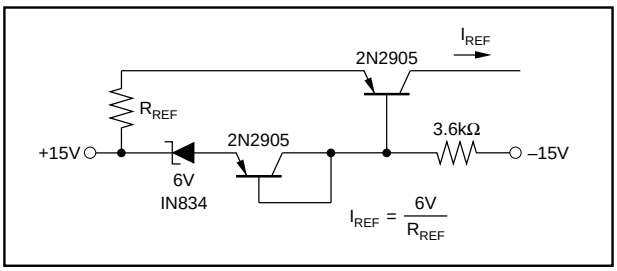


FIGURE 4. Temperature-Compensated Current Reference.

A voltage divider may be used to reduce the value of the resistor. When this is done, one must be aware of possible errors caused by the amplifier's input offset voltage. This is shown in Figure 5.

In this case the voltage at pin 14 is not exactly zero, but is equal to the value of the input offset voltage of A_1, which ranges from zero to ±5mV. V_T must be kept much larger than 5mV in order to make this effect negligible. This concept also applies to pin 1.

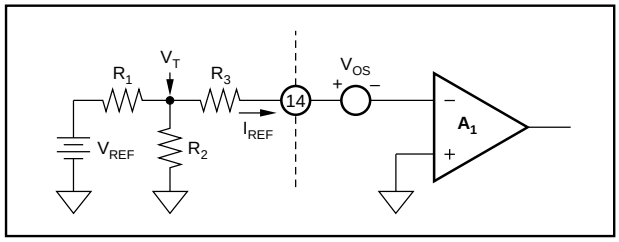


FIGURE 5. "T" Network for Reference Current.

OPTIONAL ADJUSTMENTS

The LOG100 will meet its specified accuracy with no user adjustments. If improved performance is desired, the following optional adjustments may be made.

INPUT BIAS CURRENT

The circuit in Figure 6 may be used to compensate for the input bias currents of A_1 and A_2. Since the amplifiers have FET inputs with the characteristic bias current doubling every 10°C, this nulling technique is practical only where the temperature is fairly stable.

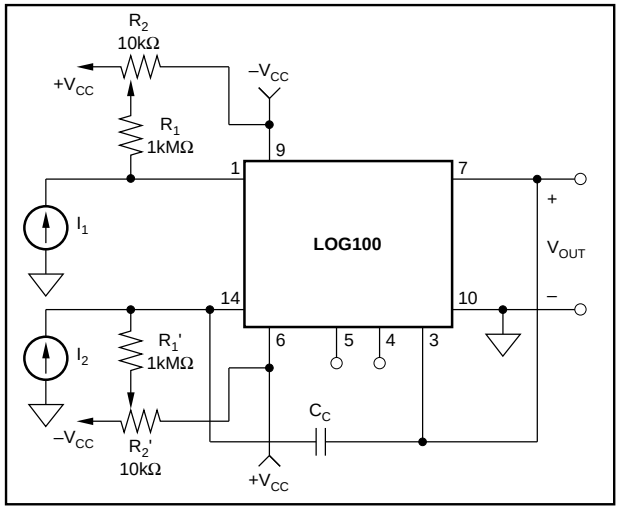


FIGURE 6. Bias Current Nulling.

OUTPUT OFFSET

The output offset may be nulled with the circuit in Figure 7. I_1 and I_2 are set equal at some convenient value in the range of 100nA to 100µA. R_1 is then adjusted for zero output voltage.

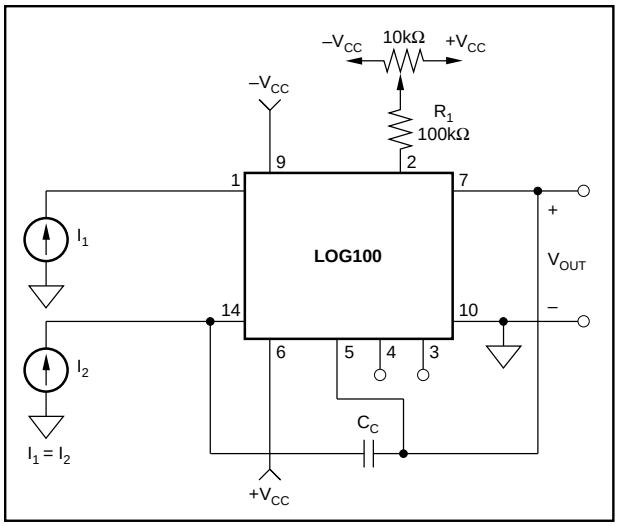


FIGURE 7. Output Offset Nulling.

ADJUSTMENTS OF SCALE FACTOR K

The value of K may be changed by increasing or decreasing the voltage divider resistor normally connected to the output, pin 7. To increase K put resistance in series between pin 7 and the appropriate scaling resistor pin (3, 4 or 5). To decrease K place a parallel resistor between pin 2 and either pin 3, 4 or 5.

APPLICATION INFORMATION

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10µF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins to the power supply common. The connection of these capacitors should be as close to the LOG100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads of up to 100pF, typically. Higher capacitive loads can be driven if a 22Ω carbon resistor is connected in series with the LOG100's output. This resistor will, of course, form a voltage divider with other resistive loads.

CIRCUIT PROTECTION

The LOG100 can be protected against accidental power supply reversal by putting a diode (1N4001 type) in series with each power supply line as shown in Figure 8. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off. If this protection circuit is used, the accuracy of the LOG100 will be degraded slightly by the voltage drops across the diodes as determined by the power supply sensitivity specification.

The LOG100 uses small geometry FET transistors to achieve the low input bias currents. Normal FET handling techniques should be used to avoid damage caused by low energy electrostatic discharge (ESD).

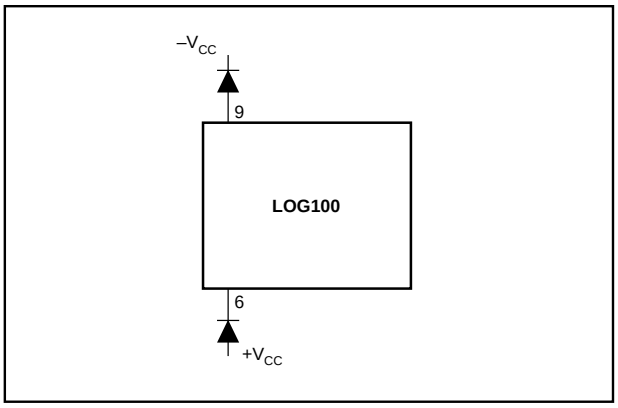


FIGURE 8. Reverse Polarity Protection.

LOG RATIO

One of the more common uses of log ratio amplifiers is to measure absorbance. A typical application is shown in Figure 9.

$$\text{Absorbance of the sample is } A = \log \frac{\lambda_1'}{\lambda_1} \qquad (22)$$

$$\text{If } \lambda_2 = \lambda_1 \text{ and } D_1 \text{ and } D_2 \text{ are matched } A \propto K \log \frac{I_1}{I_2}. \qquad (23)$$

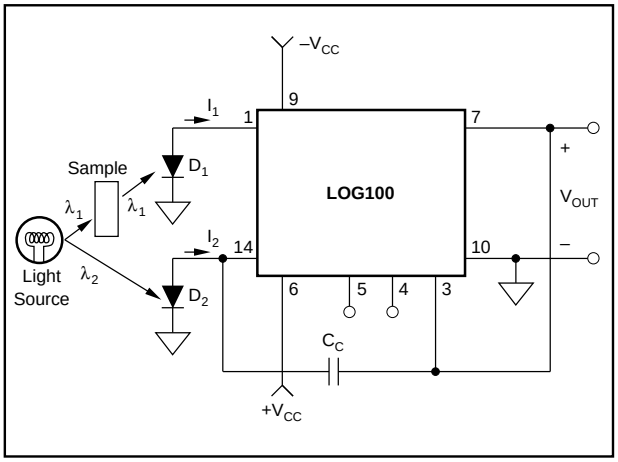


FIGURE 9. Absorbance Measurement.

DATA COMPRESSION

In many applications the compressive effects of the logarithmic transfer function is useful. For example, a LOG100 preceding an 8-bit analog-to-digital converter can produce equivalent 20-bit converter operation.

SELECTING OPTIMUM VALUES OF I_2 AND K

In straight log applications (as opposed to log ratio), both K and I_2 are selected by the designer. In order to minimize errors due to output offset and noise, it is normally best to

scale the log amp to use as much of the ±10V output range as possible. Thus, with the range of I_1 from $I_{1\ MIN}$ to $I_{1\ MAX}$;

$$\text{For } I_{1\ MAX} \qquad +10V = K \log I_{1\ MAX}/I_2 \tag{24}$$

$$\text{For } I_{1\ MIN} \qquad -10V = K \log I_{1\ MIN}/I_2 \tag{25}$$

Addition of these two equations and solving for I_2 shows that its optimum value, $I_{2\ OPT}$, is the geometric mean of $I_{1\ MAX}$ and $I_{1\ MIN}$.

$$I_{2\ OPT} = \sqrt{I_{1\ MAX} \times I_{1\ MIN}} \tag{26}$$

$$K_{OPT} = \frac{10}{\log \dfrac{I_{1\ MAX}}{I_{2\ OPT}}} \tag{27}$$

Since K is selectable in discrete steps, use the largest value of K available which does not exceed K_{OPT}.

NEGATIVE INPUT CURRENTS

The LOG100 will function only with positive input currents (conventional current flow into pins 1 and 14). Some current sources (such as photomultiplier tubes) provide negative input currents. In such situations, the circuit in Figure 10 may be used.(1)

VOLTAGE INPUTS

The LOG100 gives the best performance with current inputs. Voltage inputs may be handled directly with series resistors, but the dynamic input range is limited to approximately three decades of input voltage by voltage noise and offsets. The transfer function of equation (20) applies to this configuration.

NOTE: (1) More detailed information may be found in "Properly Designed Log Amplifiers Process Bipolar Input Signals" by Larry McDonald, EDN, 5 Oct. 80, pp 99–102.

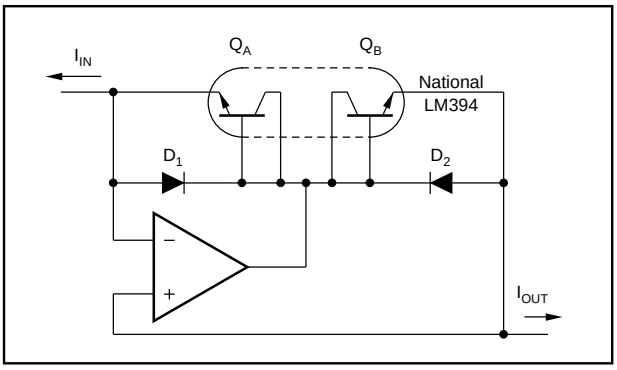


FIGURE 10. Current Inverter.

ANTILOG CONFIGURATION (an implicit technique)

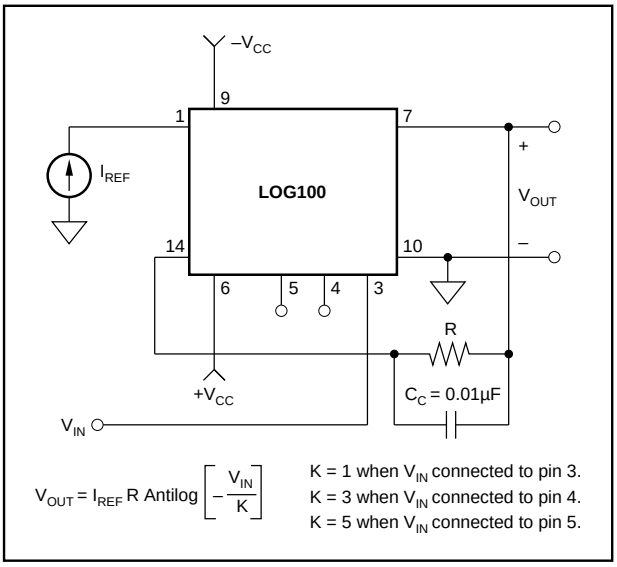


FIGURE 11. Connections for Antilog Function.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
LOG100JP	NRND	CDIP BB	JDE	14		TBD	Call TI	Call TI
LOG100JP-2	NRND	CDIP BB	JDE	14		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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