WINSOURCE
ELECTRONICS

THE DATASHEET OF

LMX2354TM/NOPB

PLLatinum™ Fractional N RF/ Integer N IF Dual Low Power Frequency Synthesizer LMX2354 2.5 GHz/550 MHz

Check for Samples: LMX2354

FEATURES

- **Pin Compatible/Functional Equivalent to the LMX2350**
- **Enhanced Low Noise Fractional Engine**
- **2.7V to 5.5V Operation**
- **Low Current Consumption**
  - **LMX2354: I_{CC} = 7 mA Typical at 3V**
- **Programmable or Logical Power Down Mode:**
  - **I_{CC} = 5 µA Typical at 3V**
- **Modulo 15 or 16 Fractional RF N Divider Supports Ratios of 1, 2, 3, 4, 5, 8, 15, or 16**
- **Programmable Charge Pump Current Levels**
  - **RF 100 µA to 1.6 mA in 100 µA Steps**
  - **IF 100 µA or 800 µA**
- **Digital Filtered Lock Detect**
- **Available in 24-Pin TSSOP and 24-Pin LGA**

APPLICATIONS

- **Portable Wireless Communications (PCS/PCN, Cordless)**
- **Dual Mode Cellular Telephone Systems**
- **Zero Blind Slot TDMA Systems**
- **Spread Spectrum Communication Systems (CDMA)**
- **Cable TV Tuners (CATV)**

DESCRIPTION

The LMX2354 is part of a family of monolithic integrated fractional N/Integer N frequency synthesizers designed to be used in a local oscillator subsystem for a radio transceiver. It is fabricated using TI's 0.5 µ ABiC V silicon BiCMOS process. The LMX2354 contains quadruple modulus prescalers along with modulo 15 or 16 fractional compensation circuitry in the RF divider. The LMX2354 provides a continuous divide ratio of 80 to 32767 in 16/17/20/21 (1.2 GHz–2.5 GHz) fractional mode and 40 to 16383 in 8/9/12/13 (550 MHz–1.2 GHz) fractional mode. The IF circuitry for the LMX2354 contains an 8/9 prescaler, and is fully programmable. Using a fractional N phase locked loop technique, the LMX2354 can generate very stable low noise control signals for UHF and VHF voltage controlled oscillators (VCOs).

For the RF PLL, a highly flexible 16 level programmable charge pump supplies output current magnitudes from 100 µA to 1.6 mA. Two uncommitted CMOS outputs can be used to provide external control signals, or configured to FastLock mode. Serial data is transferred into the LMX2354 via a three wire interface (Data, LE, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX2354 family features very low current consumption; typically LMX2354 (2.5 GHz) — 7.0 mA. The LMX2354 are available in a 24-pin TSSOP surface mount plastic package and 24-pin LGA.

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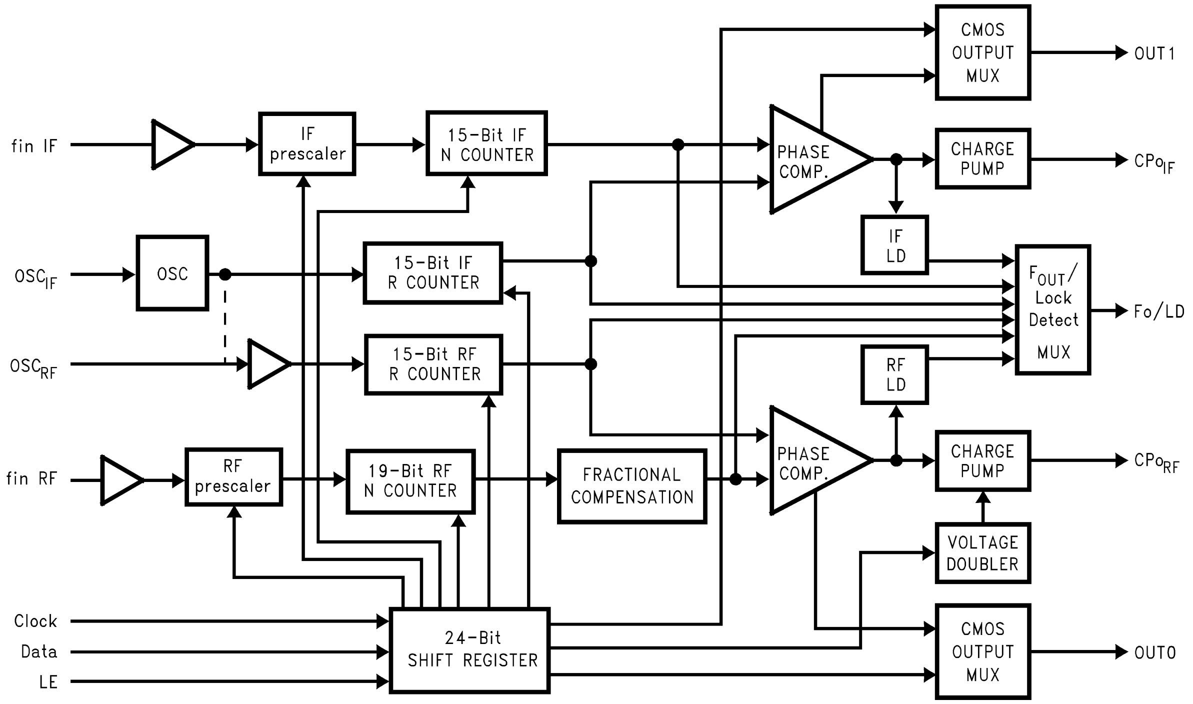
Functional Block Diagram



Connection Diagram

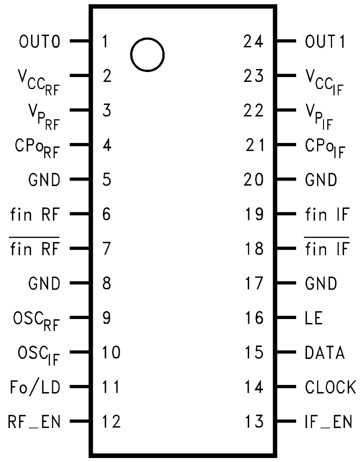


Figure 1. LMX2336U Pin Out
See Package Number PW0024A

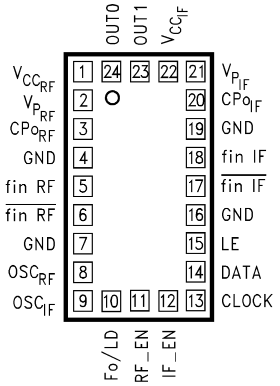


Figure 2. LMX2336U Pin Out
See Package Number NPH

PIN DESCRIPTIONS

Pin No. for TSSOP Package	Pin No. for LGA Package	Pin Name	I/O	Description
1	24	OUT0	O	Programmable CMOS output. Level of the output is controlled by IF_N [17] bit.
2	1	V_{CCRF}	—	RF PLL power supply voltage input. Must be equal to Vcc_{IF}. May range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
3	2	V_{PRF}	—	Power supply for RF charge pump. Must be ≥ V_{CCRF} and V_{CCIF}.
4	3	CP_{oRF}	O	RF charge pump output. Connected to a loop filter for driving the control input of an external VCO.
5	4	GND	—	Ground for RF PLL digital circuitry.
6	5	fin RF	I	RF prescaler input. Small signal input from the VCO.
7	6	$\overline{\text{fin RF}}$	I	RF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
8	7	GND	—	Ground for RF PLL analog circuitry.
9	8	OSC_{RF}	I	Dual mode oscillator output or RF R counter input. Has a $V_{CC}/2$ input threshold when configured as an input and can be driven from an external CMOS or TTL logic gate.
10	9	OSC_{IF}	I	Oscillator input which can be configured to drive both the IF and RF R counter inputs or only the IF R counter depending on the state of the OSC programming bit. (See REFERENCE OSCILLATOR INPUTS and Register Location Truth Table)
11	10	Fo/LD	O	Multiplexed output of N or R divider and RF/IF lock detect. CMOS output. (See Register Location Truth Table)
12	11	RF_EN	I	RF PLL Enable. Powers down RF N and R counters, prescaler, and TRI-STATE charge pump output when LOW. Bringing RF_EN high powers up RF PLL depending on the state of RF_CTL_WORD. (See POWER CONTROL)
13	12	IF_EN	I	IF PLL Enable. Powers down IF N and R counters, prescaler, and TRI-STATE charge pump output when LOW. Bringing IF_EN high powers up IF PLL depending on the state of IF_CTL_WORD. (See POWER CONTROL)
14	13	CLOCK	I	High impedance CMOS Clock input. Data for the various counters is clocked into the 24-bit shift register on the rising edge.
15	14	DATA	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
16	15	LE	I	Load Enable high impedance CMOS input. Data stored in the shift registers is loaded into one of the 4 internal latches when LE goes HIGH. (See MICROWIRE SERIAL INTERFACE)
17	16	GND	—	Ground for IF analog circuitry.
18	17	$\overline{\text{fin IF}}$	I	IF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
19	18	fin IF	I	IF prescaler input. Small signal input from the VCO.

PIN DESCRIPTIONS (continued)

Pin No. for TSSOP Package	Pin No. for LGA Package	Pin Name	I/O	Description
20	19	GND	—	Ground for IF digital circuitry.
21	20	CPo_{IF}	O	IF charge pump output. For connection to a loop filter for driving the input of an external VCO.
22	21	V_{PIF}	—	Power supply for IF charge pump. Must be ≥ V_{CCRF} and V_{CCIF}.
23	22	V_{CCIF}	—	IF power supply voltage input. Must be equal to V_{CCRF}. Input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
24	23	OUT1	O	Programmable CMOS output. Level of the output is controlled by IF_N [18] bit.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Parameter	Symbol		Value		Units
		Min	Typ	Max	
Power Supply Voltage	V_{CCRF}	−0.3		6.5	V
	V_{CCIF}	−0.3		6.5	V
	Vp_{RF}	−0.3		6.5	V
	Vp_{IF}	−0.3		6.5	V
Voltage on any pin with GND = 0V	Vi	−0.3		V_{CC} + 0.3	V
Storage Temperature Range	Ts	−65		+150	C°
Lead Temperature (Solder 4 sec.)	T_L			+260	C°

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.

(2) This Device is a high performance RF integrated circuit with an ESD rating < 2kV and is ESD sensitive. Handling and assembly of this device should only be done at ESD-free workstations.

Recommended Operating Conditions

Parameter	Symbol		Value		Units
		Min	Typ	Max	
Power Supply Voltage	V_{CCRF}	2.7		5.5	V
	V_{CCIF}	V_{CCRF}		V_{CCRF}	V
	V_{pRF}	V_{CC}		5.5	V
	V_{pIF}	V_{CC}		5.5	V
Operating Temperature	T_A	−40		+85	°C

Electrical Characteristics

(V_{CCRF}= V_{CCIF}= V_{PRF}= V_{PIF}= 3.0V; −40°C < T_A< +85°C except as specified)
All min/max specifications are specified by design, or test, or statistical methods.

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
GENERAL						
I_{CC}	Power Supply Current	RF and IF		6.0	8.5	mA
		IF Only		1.1	2.0	mA
$I_{CC\text{-}PWDN}$	Power Down Current	RF_EN = IF_EN = LOW		20	50	µA
f_{in} RF	RF Operating Frequency		0.5		2.5	GHz
f_{in} IF	IF Operating Frequency		10		550	MHz
f_{OSC}	Oscillator Frequency	No load on OSC_{RF}	2		50	MHz
fφ	Phase Detector Frequency	RF and IF			10	MHz
$Pf_{in\ RF}$	RF Input Sensitivity	V_{CC} = 3.0V	−15		0	dBm
		V_{CC} = 5.0V	−10		0	dBm
$Pf_{in\ IF}$	IF Input Sensitivity	2.7V ≤ V_{CC} ≤ 5.5V	−10		0	dBm
V_{OSC}	Oscillator Sensitivity	OSC_{IF}, OSC_{RF}	0.5		V_{CC}	V_{PP}
CHARGE PUMP						
$ICPo\text{-}_{source\ RF}$	RF Charge Pump Output Current (see Programming Description)	VCPo Vp/2, RF_CP_WORD = 0000		−100		µA
$ICPo\text{-}_{sink\ RF}$		VCPo = Vp/2, RF_CP_WORD = 0000		100		µA
$ICPo\text{-}_{source\ RF}$		VCPo = Vp/2, RF_CP_WORD = 1111		−1.6		mA
$ICPo\text{-}_{sink\ RF}$		VCPo = Vp/2, RF_CP_WORD = 1111		1.6		mA
$ICPo\text{-}_{source\ IF}$	IF Charge Pump Output Current (see Programming Description)	VCPo = Vp/2, CP_GAIN_8 = 0		−100		µA
$ICPo\text{-}_{sink\ IF}$		VCPo = Vp/2, CP_GAIN_8 = 0		100		µA
$ICPo\text{-}_{source\ IF}$		VCPo = Vp/2, CP_GAIN_8 = 1		−800		µA
$ICPo\text{-}_{sink\ IF}$		VCPo = Vp/2, CP_GAIN_8 = 1		800		µA
$ICPo\text{-}_{Tri}$	Charge Pump TRI-STATE Current	0.5 ≤ VCPo ≤ Vp −0.5 −40°C < T_A < +85°C	−2.5		2.5	nA
RF $ICPo\text{-}_{sink}$ vs. $ICPo\text{-}_{source}$	RF CP Sink vs. Source Mismatch	VCPo = Vp/2 T_A = 25°C RF ICPo=900µA − 1.6mA		3.5	10	%
ICPo vs. VCPo	CP Current vs. Voltage Variation	0.5 ≤ VCPo ≤ Vp −0.5 T_A = 25°C RF ICPo		5	10	%
ICPo vs. T	CP Current vs Temperature	VCPo = Vp/2 −40°C < T_A < +85°C RF ICPo		8		%
V_{CP}	Charge Pump Output Voltage (RF only)	2.7V ≤ V_{CC} ≤ 3.3V, Doubler Enabled		2* V_{CC} −0.5		V
DIGITAL INTERFACE (DATA, CLK, LE, EN, FoLD)						
V_{IH}	High-level Input Voltage	(1)	0.8 V_{CC}			V
V_{IL}	Low-level Input Voltage	(1)			0.2 V_{CC}	V
I_{IL}	Low-level Input Current	V_{IL}= 0, V_{CC}= 5.5V, (1)	−1.0		1.0	µA
I_{IH}	High-level Input Current	V_{IH}= V_{CC}= 5.5V, (1)	−1.0		1.0	µA
I_{IH}	Oscillator Input Current	V_{IH}= V_{CC}= 5.5V			100	µA
I_{IL}	Oscillator Input Current	V_{IL}= 0, V_{CC}= 5.5V	−100			µA
V_{OH}	High-level Output Voltage	I_{OH}= −500 µA	V_{CC} −0.4			V
V_{OL}	High-level Output Voltage	I_{OL}= 500 µA			0.4	V
MICROWIRE TIMING						
t_{CS}	Data to Clock Setup Time	See SERIAL DATA INPUT TIMING	50			ns
t_{CH}	Data to Clock Hold Time	See SERIAL DATA INPUT TIMING	10			ns
t_{CWH}	Clock Pulse Width High	See SERIAL DATA INPUT TIMING	50			ns
t_{CWL}	Clock Pulse Width Low	See SERIAL DATA INPUT TIMING	50			ns

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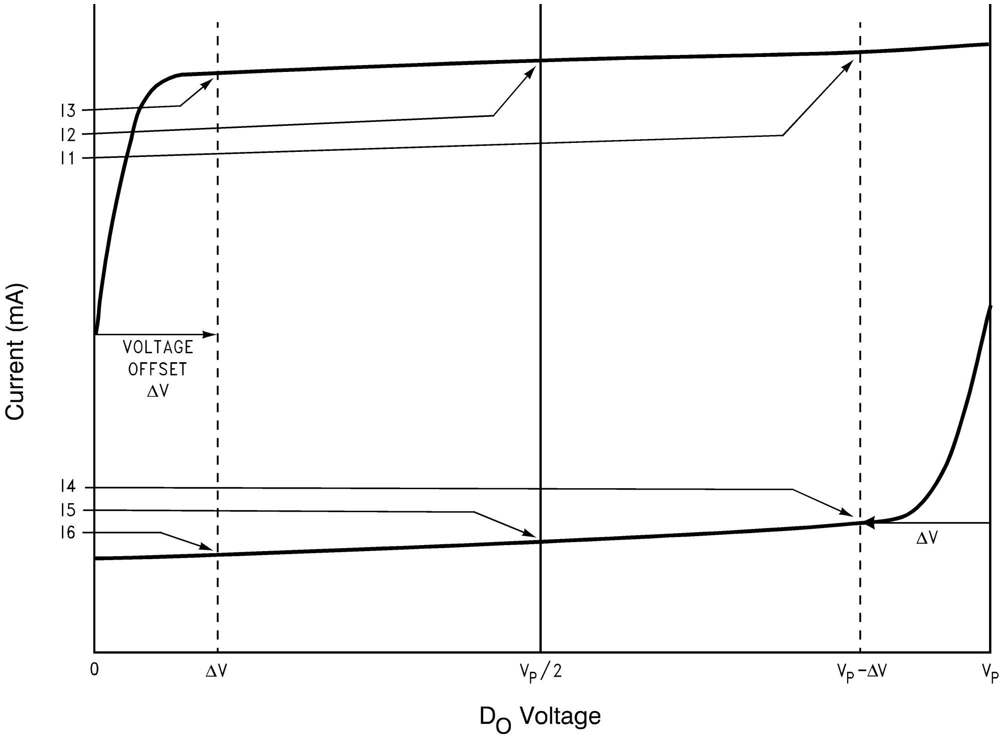
(1) except f_{IN}, OSC_{IF} and OSC_{RF}

Electrical Characteristics (continued)

(V_{CCRF}= V_{CCIF}= V_{PRF}= V_{PIF}= 3.0V; −40°C < T_A< +85°C except as specified)
All min/max specifications are specified by design, or test, or statistical methods.

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
t_{ES}	Clock to Load Enable Set Up Time	See SERIAL DATA INPUT TIMING	50			ns
t_{EW}	Load Enable Pulse Width	See SERIAL DATA INPUT TIMING	50			ns

Charge Pump Current Specification Definitions



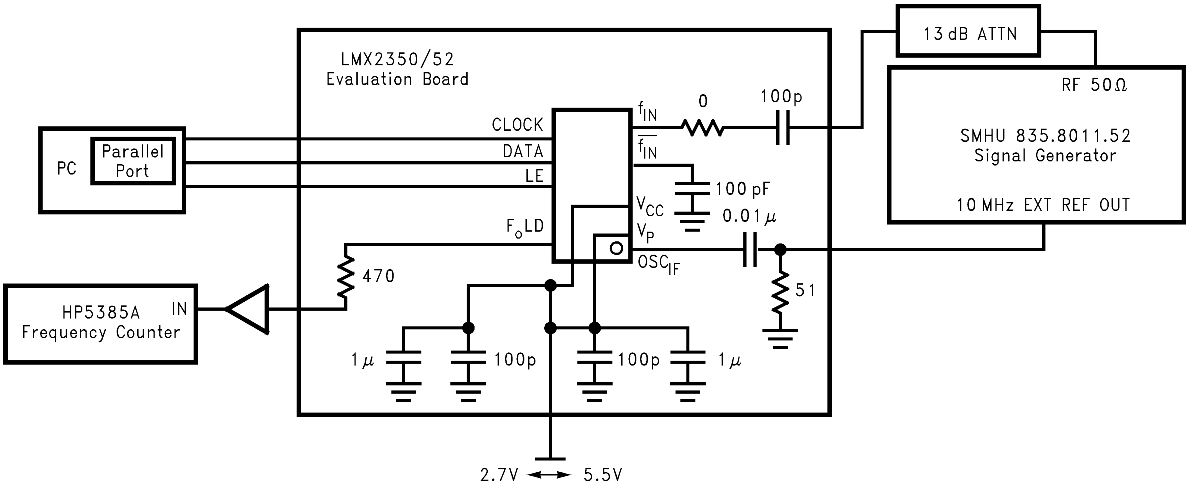
I1 = CP sink current at V_{Do} = Vp − ΔV
I2 = CP sink current at V_{Do} = Vp/2
I3 = CP sink current at V_{Do} = ΔV
I4 = CP source current at V_{Do} = Vp − ΔV
I5 = CP source current at V_{Do} = Vp/2
I6 = CP source current at V_{Do} = ΔV
ΔV = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to V_{CC} and ground. Typical values are between 0.5V and 1.0V.

I_{Do} vs V_{Do} = Charge Pump Output Current magnitude variation vs Voltage = [½ * {|I1| − |I3|}]/[½ * {|I1| + |I3|}] * 100% and [½ * {|I4| − |I6|}]/[½ * {|I4| + |I6|}] * 100%

$I_{Do\text{-}sink}$ vs $I_{Do\text{-}source}$ = Charge Pump Output Current Sink vs Source Mismatch = [|I2| − |I5|]/[½ * {|I2| + |I5|}] * 100%

I_{Do} vs T_A = Charge Pump Output Current magnitude variation vs Temperature = [|I2 @ temp| − |I2 @ 25°C|]/|I2 @ 25°C| * 100% and [|I5 @ temp| − |I5 @ 25°C|]/|I5 @ 25°C| * 100%

RF Sensitivity Test Block Diagram



Note: N = 10,000 R = 50 P = 16

Note: Sensitivity limit is reached when the error of the divided RF output, F_oLD, is ≥ 1 Hz.

Typical Performance Characteristics

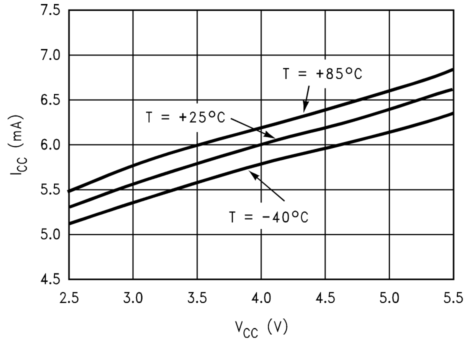

I_{CC} vs V_{CC} LMX2354

Figure 3.

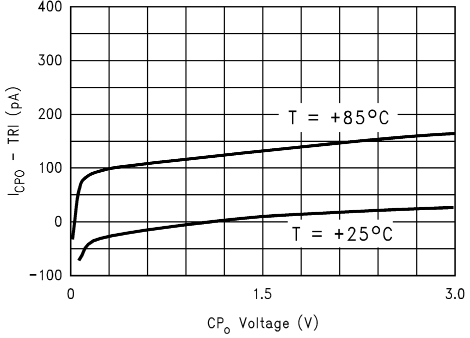

I_{CPO} TRI-STATE vs CP_O Voltage

Figure 4.

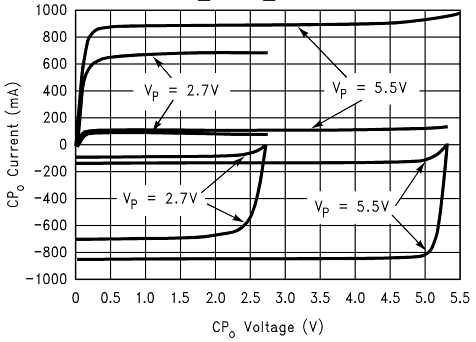

Charge Pump Current vs CP_O Voltage RF_CP_WORD = 0000 and 0111 IF CP_GAIN_8 = 0 and 1

Figure 5.

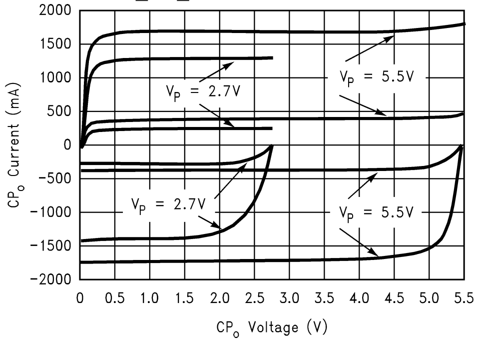

Charge Pump Current vs CP_O Voltage RF_CP_WORD = 0011 and 1111

Figure 6.

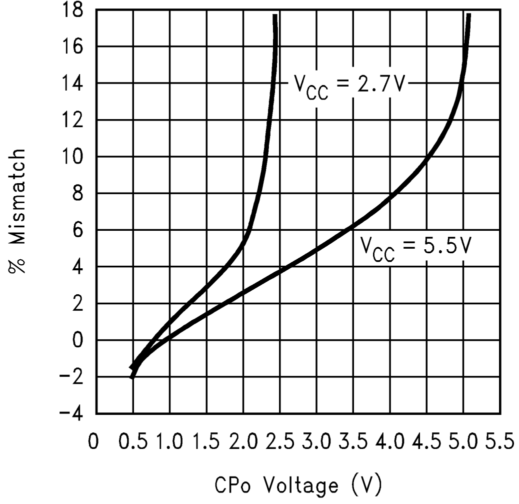
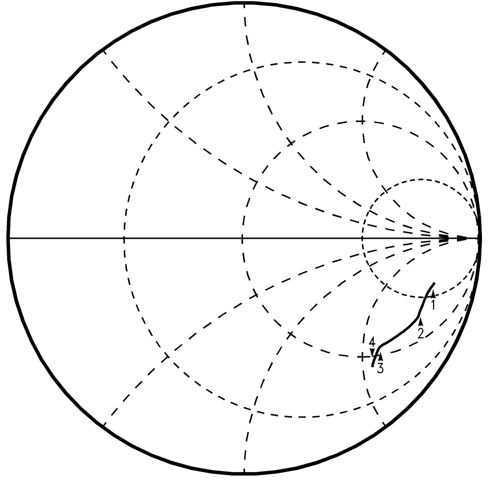

Sink vs Source Mismatch (See under Charge Pump Current Specification Definitions)

Figure 7.

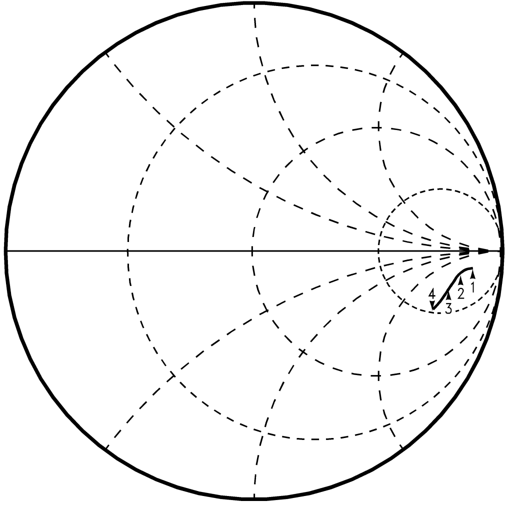

RF Input Impedance V_{CC} = 2.7V to 5.5V, f_{IN} = 550 MHz to 2.5 GHz ($\overline{f_{IN}}$ Capacitor = 100 pF)

Marker 1 = 550 MHz, Real = 212.39, Imaginary = −230.53
Marker 2 = 1 GHz, Real = 104.52, Imaginary = −178.9
Marker 3 = 1.8 GHz, Real = 58.703, Imaginary = −114.05
Marker 4 = 2.5 GHz, Real = 43.059, Imaginary = −107.78

Figure 8.

Typical Performance Characteristics (continued)

IF Input Impedance
V_{CC} = 2.7V to 5.5V, f_{IN} = 50 MHz to 550 MHz ($\overline{f_{IN}}$ Capacitor = 100 pF)



Marker 1 = 50 MHz, Real = 575.91, Imaginary = −330.06
Marker 2 = 200 MHz, Real = 388.39, Imaginary = −237.7
Marker 3 = 550 MHz, Real = 276.67, Imaginary = −219.84
Marker 4 = 550 MHz, Real = 154.95, Imaginary = −173.8

Figure 9.

LMX2354 RF Sensitivity vs Frequency

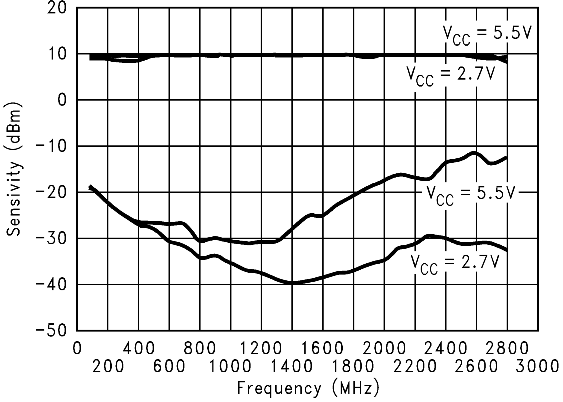


Figure 10.

IF Input Sensitivity vs Frequency

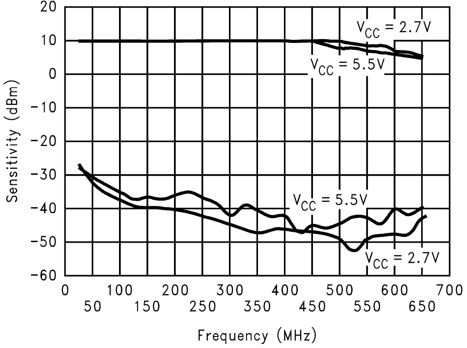


Figure 11.

Oscillator Input Sensitivity vs Frequency

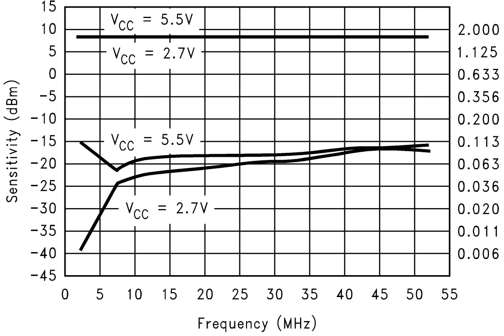


Figure 12.

FUNCTIONAL DESCRIPTION

GENERAL

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the Texas Instruments LMX2354, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, as well as programmable reference [R] and feedback [N] frequency dividers. The VCO frequency is established by dividing the crystal reference signal down via the R counter to obtain a frequency that sets the comparison frequency. This reference signal, f_r, is then presented to the input of a phase/frequency detector and compared with another signal, f_p, the feedback signal, which was obtained by dividing the VCO frequency down by way of the N counter and fractional circuitry. The phase/frequency detector's current source outputs pump charge into the loop filter, which then converts the charge into the VCO's control voltage. The phase/frequency comparator's function is to adjust the voltage presented to the VCO until the feedback signal's frequency (and phase) match that of the reference signal. When this ‘phase-locked' condition exists, the RF VCO's frequency will be N+F times that of the comparison frequency, where N is the integer divide ratio and F is the fractional component. The fractional synthesis allows the phase detector frequency to be increased while maintaining the same frequency step size for channel selection. The division value N is thereby reduced giving a lower phase noise referred to the phase detector input, and the comparison frequency is increased allowing faster switching times.

REFERENCE OSCILLATOR INPUTS

The reference oscillator frequency for the RF and IF PLLs is provided by an external reference through the OSC_{IF} pin and OSC_{RF} pin. OSC_{IF}/OSC_{RF} block can operate 50 MHz with an input sensitivity of 0.5 Vpp. The OSC bit (see OSC (IF_R[23])), selects whether the oscillator input pins OSC_{IF} and OSC_{RF} drive the IF and RF R counters separately or by a common input signal path. When an external TCXO is connected only at the OSC_{IF} input pin and not at the OSC_{RF} pin, the TCXO drives both IF R counter and RF R counter. When configured as separate inputs, the OSC_{IF} pin drives the IF R counter while the OSC_{RF} drives the RF R counter. The inputs have a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.

REFERENCE DIVIDERS (R COUNTERS)

The RF and IF R Counters are clocked through the oscillator block either separately or in common. The maximum frequency is 50 MHz. Both R Counters are 15-bit CMOS counters with a divide range from 3 to 32,767. (See 15-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (RCOUNTER) (IF_R[2]-IF_R[16])

PROGRAMMABLE DIVIDERS (N COUNTERS)

The RF and IF N Counters are clocked by the small signal fin RF and fin IF input pins respectively. The RF N Counter can be configured as a fractional or fully integer counter. The LMX2354 RF N counter is 19 bits with 15 bits integer divide and 4 bits fractional. The integer part is configured as a 2-bit A Counter, a 2-bit B Counter and a 11-bit C Counter. The LMX2354 is capable of operating from 500 MHz to 1.2 GHz with the 8/9/12/13 prescaler offering a continuous integer divide range from 40 to 16,383 in fractional mode and 24 to 262143 in full integer mode. The LMX2354 is capable of operating from 1.2 GHz to 2.5 GHz with the 16/17/20/21 prescaler offering a continuous integer divide range from 80 to 32,767 in fractional mode and 48 to 52,4287 in full integer mode. The RF counters for the LMX2354 also contain fractional compensation, programmable in either 1/15 or 1/16 modes. The LMX2354 IF N counter is 15-bit integer divider configured with a 3-bit A Counter and a 12-bit B Counter offering a continuous integer divide range from 56 to 32,767 over the frequency range of 10 MHz to 550 MHz. The IF N counter does not include fractional compensation. The tables below show the differences between the LMX2354 in integer mode and in quadruple modulus prescaler with P = 16/17/20/21. Also, the tables show that the bit used for the lower modulus prescaler values is different between the LMX2350 and the LMX2354. For the LMX2350 bit N<9>=0 (MSB of the A Word) is used for the 16/17 modulus and for the LMX2354 bit N<8>=0 is used for the 8/9/12/13 modulus. So if the LMX2354 is replacing a LMX2350 then bits N<8> and N<9> need to be swapped.

Table 1. LMX2354 RF N Counter Register in Fractional Mode with P = 16/17/20/21:

	C Word											B Word		A Word		Fractional Word			
N	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1–47	Divide ratios less than 48 are impossible since it is required that C ≥3															These bits are used for the fractional word when the part is operated in fractional mode			
48–79	Some of these values are legal divide ratios, some are not																		
80*	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0				
81	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1				
...																			
1056	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0				
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.				
32,767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				

Table 2. LMX2354 RF N Counter Register in Fractional Mode with P = 8/9/12/13

	C Word											B Word		A Word		Fractional Word			
N	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1–23	Divide ratios less than 24 are impossible since it is required that C ≥3															These bits are used for the fractional word when the part is operated in fractional mode			
24–39	Some of these values are legal divide ratios, some are not																		
40*	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0				
41	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1				
...																			
272	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0				
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.				
16,383	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1				

Prescaler

The RF and IF inputs to the prescaler consist of fin and /fin; which are complimentary inputs to differential pair amplifiers. The complimentary inputs are internally coupled to ground with a 10 pF capacitor. These inputs are typically AC coupled to ground through external capacitors as well. The input buffer drives the A counter's ECL D-type flip flops in a dual modulus configuration. An 8/9/12/13 or 16/17/20/21 prescale ratio can be selected for the LMX2354. The IF circuitry for both the LMX2354 contains an 8/9 prescaler. The prescaler clocks the subsequent CMOS flip-flop chain comprising the fully programmable A and B counters.

Fractional Compensation

The fractional compensation circuitry of the LMX2354 RF dividers allows the user to adjust the VCO's tuning resolution in 1/16 or 1/15 increments of the phase detector comparison frequency. A 4-bit register is programmed with the fractions desired numerator, while another bit selects between fractional 15 and 16 modulo base denominator (see FRACTIONAL MODULUS ACCUMULATOR (FRAC_CNTR) (RF_N[2]–RF_N[5])). An integer average is accomplished by using a 4-bit accumulator. A variable phase delay stage compensates for the accumulated integer phase error, minimizing the charge pump duty cycle, and reducing spurious levels. This technique eliminates the need for compensation current injection in to the loop filter. Overflow signals generated by the accumulator are equivalent to 1 full VCO cycle, and result in a pulse swallow.

PHASE/FREQUENCY DETECTOR

The RF and IF phase/frequency detectors are driven from their respective N and R counter outputs. The phase detector outputs control the charge pumps. The polarity of the pump-up or pump-down control is programmed using RF_PD_POL or IF_PD_POL depending on whether RF/IF VCO characteristics are positive or negative (see IF_CP_WORD (IF_R[17]–IF_R[18]) and RF_CP_WORD (RF_R[17]–RF_R[21])). The phase detector also receives a feedback signal from the charge pump, in order to eliminate dead zone.

CHARGE PUMP

The phase detector's current source outputs pump charge into an external loop filter, which then converts the charge into the VCO's control voltage. The charge pumps steer the charge pump output, CPo, to Vcc (pump-up) or ground (pump-down). When locked, CPo is primarily in a TRI-STATE mode with small corrections. The RF charge pump output current magnitude is programmable from 100 µA to 1.6 mA in 100 µA steps as shown in table RF_CP_WORD (RF_R[17]–RF_R[21]). The IF charge pump is set to either 100 µA or 800 µA levels using bit IF_R [19] (see IF_CP_WORD (IF_R[17]–IF_R[18])).

VOLTAGE DOUBLER

The V_{pRF} pin is normally driven from an external power supply over a range of V_{CC} to 5.5V to provide current for the RF charge pump circuit. An internal voltage doubler circuit connected between the V_{CC} and V_{pRF} supply pins alternately allows V_{CC} = 3V (±10%) users to run the RF charge pump circuit at close to twice the V_{CC} power supply voltage. The voltage doubler mode is enabled by setting the V2_EN bit (RF_R [22]) to a HIGH level. The voltage doubler's charge pump driver originates from the RF oscillator input (OSC_{RF}). The average delivery current of the doubler is less than the instantaneous current demand of the RF charge pump when active and is thus not capable of sustaining a continuous out of lock condition. A large external capacitor connected to V_{pRF} (≈0.1 µF) is therefore needed to control power supply droop when changing frequencies.

MICROWIRE SERIAL INTERFACE

The programmable functions are accessed through the MICROWIRE serial interface. The interface is made of 3 functions: clock, data and latch enable (LE). Serial data for the various counters is clocked in from data on the rising edge of clock, into the 24-bit shift register. Data is entered MSB first. The last two bits decode the internal register address. On the rising edge of LE, data stored in the shift register is loaded into one of the 4 appropriate latches (selected by address bits). A complete programming description is included in the following sections.

Fo/LD MULTIFUNCTION OUTPUT

The Fo/LD output pin can deliver several internal functions including analog/digital lock detects, and counter outputs. See FOLD Programming Truth Table (IF_R[19]-IF_R[21] for more details.

Lock Detect

A digital filtered lock detect function is included with each phase detector through an internal digital filter to produce a logic level output available on the Fo/LD output pin if selected. The lock detect output is high when the error between the phase detector inputs is less than 15 ns for 5 consecutive comparison cycles. The lock detect output is low when the error between the phase detector outputs is more than 30 ns for one comparison cycle. An analog lock detect signal is also selectable. The lock detect output is always low when the PLL is in power down mode. See FOLD Programming Truth Table (IF_R[19]-IF_R[21], LOCK DETECT DIGITAL FILTER – TYPICAL LOCK DETECT TIMING for more details.

POWER CONTROL

Each PLL is individually power controlled by device enable pins or MICROWIRE power down bits. The enable pins override the power down bits ***except for the V2_EN bit***. The RF_EN pin controls the RF PLL; IF_EN pin controls the IF PLL. When both pins are high, the power down bits determine the state of power control (see Programming Description). Activation of any PLL power down mode results in the disabling of the respective N counter and de-biasing of its respective fin input (to a high impedance state). The R counter functionality also becomes disabled when the power down bit is activated. The reference oscillator block powers down and the OSC_{IF} pin reverts to a high impedance state when both RF and IF enable pins or power down bit's are asserted, *unless the V2_EN bit (RF_R[22]) is high*. Power down forces the respective charge pump and phase comparator logic to a TRI-STATE condition. A power down counter reset function resets both N and R counters. Upon powering up the N counter resumes counting in “close” alignment with the R counter (The maximum error is one prescaler cycle). The MICROWIRE control register remains active and capable of loading and latching in data during all of the power down modes.

Major Differences between the LMX2354 and the LMX2350/52

	LMX2350/52	**LMX2354**
OSC_{IF}	Supports resonator mode.	Does not support resonator mode.
Low modulus prescale [1]	5-bit A counter, so if 16/17 prescale, bit-5 is the unused place holder.	4-bit A/B counters, so if 8/9/12/13, bit-4 is the unused place holder.
RF Prescaler	LMX2350—32/33 or 16/17 LMX2352—16/17 or 8/9	LMX2354—16/17/20/21 or 8/9/12/13
Fractional Engine	Standard. Fractional Compensation cannot be turned off.	Similar structure to the LMX2350/52, but with some modifications for improved phase noise and spurs. Fractional Compensation can be turned off.

(1) If the LMX2354 is replacing a LMX2350/52 in a design, and you are using the lower modulus prescale value (16/17 on the LMX2350 changes to 8/9/12/13 on the LMX2354), the unused prescaler bit of the LMX2350/52 needs to shift down one bit from N<9> to N<8>.

Programming Description

INPUT DATA REGISTER

The descriptions below describe the 24-bit data register loaded through the MICROWIRE Interface. The data register is used to program the 15-bit IF_R counter register, and the 15-bit RF_R counter register, the 15-bit IF_N counter register, and the 19-bit RF_N counter register. The data format of the 24-bit data register is shown below. The control bits CTL [1:0] decode the internal register address. On the rising edge of LE, data stored in the shift register is loaded into one of 4 appropriate latches (selected by address bits). Data is shifted in MSB first

MSB		LSB	
DATA [21:0]		CTL [1:0]	
23	2	1	0

Register Location Truth Table

CTL [1:0]		**DATA Location**
1	**0**	
0	0	IF_R register
0	1	IF_N register
1	0	RF_R register
1	1	RF_N register

Register Content Truth Table

	First Bit			REGISTER BIT LOCATION																	Last Bit		
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 c1	0 c2
IF_R	OSC	FRAC_16	FoLD			IF_CP_WORD		IF_R_CNTR															0	0
IF_N	IF_CTL_WORD			CMOS OUTPUTS/ FRAC TEST				IF_NB_CNTR												IF_NA_CNTR			0	1
RF_R	DLL_MODE	V2_EN	RF_CP_WORD					RF_R_CNTR															1	0
RF_N	RF_CTL_WORD			C_WORD											B_WORD		A_WORD		FRAC_CNTR				1	1

PROGRAMMABLE REFERENCE DIVIDERS

IF_R REGISTER

If the Control Bits (CTL [1:0]) are 0 0, when data is transferred from the 24-bit shift register into a latch when LE is transitioned high. This register determines the IF R counter value, IF Charge pump current, FoLD pin output, fractonal modulus, and oscillator mode.

MSB						LSB
OSC	FRAC_16	FoLD [2:0]	IF_CP_WORD [1:0]	IF_R_CNTR [14:0]	0	0
23	22	21 19	18 17	16 2	1	0

OSC (IF_R[23])

The **OSC** bit, IF_R [23], selects whether the oscillator inputs OSC_{IF} and OSC_{RF} drive the IF and RF R counters separately or by a common input signal path. When OSC = 0 , the OSC_{IF} pin drives the IF R counter while the OSC_{RF} pin drives the RF R counter. When the OSC = 1, the OSC_{IF} pin drives both R counters.

FRAC_16(IF_R[22])

The **FRAC_16** bit, IF_R [22], is used to set the fractional compensation at either 1/16 and 1/15 resolution. When FRAC-16 is set to one, the fractional modulus is set to 1/16 resolution, and FRAC_16 = 0 corresponds to 1/15 (See FRACTIONAL MODULUS ACCUMULATOR (FRAC_CNTR) (RF_N[2]–RF_N[5])).

15-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER) (IF_R[2]–IF_R[16])(1)

	IF_R_CNTR/RF_R_CNTR														
Divide Ratio	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32,767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(1) **Notes**: Divide ratio: 3 to 32,767 (Divide ratios less than 3 are prohibited).
RF_R_CNTR/IF_R_CNTR These bits select the divide ratio of the programmable reference dividers.

IF_CP_WORD (IF_R[17]–IF_R[18])

CP_GAIN_8	IF_PD_POL

BIT	LOCATION	FUNCTION	0	1
CP_GAIN_8	IF_R [18]	IF Charge Pump Current Gain	1X	8X
IF_PD_POL	IF_R [17]	IF Phase Detector Polarity	Negative	Positive

CP_GAIN_8 is used to toggle the IF charge pump current magnitude between 1X mode (100 µA typical) and 8X mode (800 µA typical).

IF_PD_POL is set to one when IF VCO characteristics are positive. When IF VCO frequency decreases with increasing control voltage IF_PD_POL should set to 0.

FoLD Programming Truth Table (IF_R[19]–IF_R[21])(1)

FoLD	Fo/LD OUTPUT STATE
0 0 0	IF and RF Analog Lock Detect
1 0 0	IF Digital Lock Detect

(1) FoLD - Fout/Lock Detect PROGRAMMING BITS

FoLD	Fo/LD OUTPUT STATE
0 1 0	RF Digital Lock Detect
1 1 0	IF and RF Digital Lock Detect
0 0 1	IF R counter
1 0 1	IF N counter
0 1 1	RF R counter
1 1 1	RF N counter

RF_R Register

If the Control Bits (CTL [1:0]) are 1 0, data is transferred from the 24-bit shift register into the RF_R register latch which sets the RF PLL's 15-bit R counter divide ratio. The divide ratio is programmed using the RF_R_CNTR word as shown in 15-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER) (IF_R[2]_IF_R[16]). The divide ratio must be ≥ 3. The bits used to control the voltage doubler (V2_EN) and RF Charge Pump (RF_CP_WORD) are detailed in RF_CP_WORD (RF_R[17]–RF_R[21]).

MSB							LSB
DLL_MODE	V2_EN	RF_CP_WORD [4:0]		RF_R_CNTR [14:0]		1	0
23	22	21	17	16	2	1	0

(RF_R[22]–RF_R[23])(1)

DLL_MODE	V2_EN

(1) **Note 1.** V2_EN bit when set high enables the voltage doubler for the RF Charge Pump supply.
Note 2. DLL_MODE bit should be set to one for normal usage.

BIT	LOCATION	FUNCTION	0	1
DLL_MODE	RF_R [23]	Delay Line Loop Calibration Mode	Slow	Fast
V2_EN	RF_R [22]	RF_Voltage Doubler Enable	Disabled	Enabled

RF_CP_WORD (RF_R[17]–RF_R[21])

CP_8X	CP_4X	CP_2X	CP_1X	RF_PD_POL

RF_PD_POL (RF_R[17]) should be set to one when RF VCO characteristics are positive. When RF VCO frequency decreases with increasing control voltage RF_PD_POL should be set to zero.

CP_1X, CP_2X, CP_4X, and CP_8X are used to step the RF Charge Pump output current magnitude from 100 µA to 1.6 mA in 100 µA steps as shown in the table below.

Table 3. RF Charge Pump Output Truth Table

ICPo µA (typ)	CP8X RF_R[21]	CP4X RF_R[20]	CP2X RF_R[19]	CP1X RF_R[18]
100	0	0	0	0
200	0	0	0	1
300	0	0	1	0
400	0	0	1	1
•	•	•	•	•
900	1	0	0	0
•	•	•	•	•
1600	1	1	1	1

Programmable Dividers (N Counters)

IF_N REGISTER

If the Control Bits (CTL [1:0]) are 0 1, data is transferred from the 24-bit shift register into the IF_N register latch which sets the PLL's 15-bit programmable N counter value and various control functions. The IF_N counter consists of the 3-bit swallow counter (A counter), and the 12-bit programmable counter (B counter). Serial data format is shown below in Programmable CMOS Output Truth Table and3-BIT IF SWALLOW COUNTER DIVIDE RATIO (IF A COUNTER) (IF_N[2]–IF_N[4]). The divide ratio (IF_NB_CNTR) must be ≥ 3. The divide ratio is programmed using the bits IF_N_CNTR as shown in CMOS (Programmable CMOS outputs) (IF_N[17]–IF_N[20]) and Programmable CMOS Output Truth Table. The minimum continuous divide ratio is 56. The CMOS [3:0] bits program the 2 CMOS outputs detailed in CMOS (Programmable CMOS outputs) (IF_N[17]–IF_N[20]), and also contain the fractional test bit.

MSB				LSB
IF_CTL_WORD [2:0]	CMOS [3:0]	IF_NB_CNTR [11:0]	IF_NA_CNTR [2:0]	0 1
23 21	20 17	16 5	4 2	1 0

IF_CTL_WORD (IF_N[21]–IF_N[23])

MSB		LSB
IF_CNT_RST	PWDN_IF	PWDN_MODE

NOTE

See RF/IF Control Word Truth Table for IF control word truth table.

CMOS (Programmable CMOS outputs) (IF_N[17]–IF_N[20])

MSB			LSB
FastLock	TEST	OUT_1	OUT_0

NOTE

Test bit is reserved and should be set to zero for normal usage.

Programmable CMOS Output Truth Table

Bit	Location	Function	0	1
OUT_0	IF_N[17]	OUT0 CMOS Output Pin Level Set	LOW	HIGH
OUT_1	IF_N[18]	OUT1 CMOS Output Pin Level Set	LOW	HIGH
Test	IF_N[19]	Fractional Test Bit	Normal Operation	No Fractional Compensation
Fastlock	IF_N[20]	Fastlock Mode Select	CMOS Output	Fastlock Mode

Test Bit IF_N[19] controls the fractional spur compensation and should be set to 0 for normal operation. If the test bit is set to 1, then the fractional spurs become much worse, but the phase noise improves about 5 dB.

When the **Fastlock** bit is set to 1, **OUT_0** and **OUT_1** are don't care bits. Fastlock mode utilizes the OUT0 and OUT1 output pins to synchronously switch between active low and TRI-STATE. The OUT0 = LOW state occurs whenever the RF loop's CP_8X is selected HIGH while the Fastlock bit is set HIGH (see RF_CP_WORD (RF_R[17]–RF_R[21])). The OUT0 pin reverts to TRI-STATE when the CP_8X bit is LOW. Similarly for the IF loop, the synchronous activation of OUT1 = LOW or TRI-STATE, is dependent on whether the CP_GAIN_8 is high or low respectively (see IF_CP_WORD (IF_R[17]–IF_R[18])).

3-BIT IF SWALLOW COUNTER DIVIDE RATIO (IF A COUNTER) (IF_N[2]–IF_N[4])

Swallow Count	**IF_NA_CNTR**		
(A)	**2**	**1**	**0**
0	0	0	0
1	0	0	1
•	•	•	•
7	1	1	1

NOTE

Swallow Counter Value: 0 to 7

IF_NB_CNTR ≥ IF_NA_CNTR

Minimum continuous count = 56 (A=0, B=7)

12-BIT IF PROGRAMMABLE COUNTER DIVIDE RATIO (IF B COUNTER) (IF_N[5]–IF_N[16])

	IF_NB_CNTR											
Divide Ratio	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
3	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1

NOTE

Divide ratio: 3 to 4095 (Divide ratios less than 3 are prohibited)

IF_NB_CNTR ≥ IF_NA_CNTR

N divider continuous integer divide ratio 56 to 32,767.

RF_N Register

If the control bits (CTL[2:0]) are 1 1, data is transferred from the 24-bit shift register into the RF_N register latch which sets the RF PLL's programmable N counter register and various control functions. The RF N counter consists of a 2-bit A counter, 2-bit B counter, 11-bit C counter, and a 4-bit fractional counter. For proper operation, C_WORD≧MAX{A_WORD, B_WORD}+2. Serial data format is shown below.

MSB						LSB
RF_CTL_WORD [2:0]	C_WORD [10:0]	B_WORD [1:0]	A_WORD [1:0]	FRAC_CONT [3:0]	1	1
23 21	20 10	9 8	7 6	5 2	1	0

RF_CTL_WORD (RF_N[21]–RF_N[23])

MSB		LSB
RF_CNT_RST	PWDN_RF	PRESC_SEL

RF/IF Control Word Truth Table

BIT	**FUNCTION**	**0**	**1**
IF_CNT_RST/RF_CNT_RST	IF/RF counter reset	Normal Operation	Reset
PWDN_IF/PWDN_RF	IF/RF power down	Powered up	Powered down
PWDN_MODE	Power down mode select	Asynchronous power down	Synchronous power down

BIT		FUNCTION	0	1
PRESC_SEL	LMX2354	Prescaler Modulus Select	8/9/12/13 0.5 GHz–1.2 GHz	16/17/20/21 1.2 GHZ–2.5 GHZ

The **Counter Reset** enable bit when activated allows the reset of both N and R counters. Upon powering up, the N counter resumes counting in “close” alignment with the R counter (the maximum error is one prescaler cycle).

Activation of the PLL **power down** bits result in the disabling of the respective N counter divider and de-biasing of its respective fin inputs (to a high impedance state). The respective R counter functionality also becomes disabled when the power down bit is activated. The OSC_{IF} pin reverts to a high impedance state when both RF and IF power down bits are asserted. Power down forces the respective charge pump and phase comparator logic to a TRI-STATE condition. The MICROWIRE control register remains active and capable of loading and latching in data during all of the power down modes.

Both synchronous and asynchronous power down modes are available with the LMX235x family in order to adapt to different types of applications. The power down mode bit IF_N[21] is used to select between synchronous and asynchronous power down. The MICROWIRE control register remains active and capable of loading and latching in data during all of the power down modes.

Synchronous Power Down Mode

One of the PLL loops can be *synchronously* powered down by first setting the power down mode bit HIGH (IF_N[21] = 1) and then asserting its power down bit (IF_N[22] or RF_N[22] = 1). The power down function is gated by the charge pump. Once the power down bit is loaded, the part will go into power down mode upon the completion of a charge pump pulse event.

Asynchronous Power Down Mode

One of the PLL loops can be *asynchronously* powered down by first setting the power down mode bit LOW (IF_N[21] = 0) and then asserting its power down bit (IF_N[22] or RF_N[22] = 1). The power down function is NOT gated by the charge pump. Once the power down bit is loaded, the part will go into power down mode immediately.

Prescaler select is used to set the RF prescaler. The LMX2354 contains quadruple modulus prescalers. It uses the 16/17/20/21 prescaler mode to operate at 1.2 GHz–2.5 GHz. In addition, it can use the 8/9/12/13 prescaler to operate at 550 MHz–1.2 GHz.

N REGISTER—(8/9/12/13) PRESCALER OPERATING IN FRACTIONAL MODE (RF_N[6]–RF_N[20])

	RF_N_CNTR [14:0]														
Divide Ratio	**C Word**											**B Word**		**A Word**	
1–23	Divide Ratios Less than 24 are impossible since it is required that C>=3														
24–39	Some of these N values are Legal Divide Ratios, some are not														
40	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0
41	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1
...	.	.	.	.	.	.	.	.	.	.	.	0	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1

N REGISTER—(16/17/20/21) PRESCALER OPERATING IN FRACTIONAL MODE (RF_N[6]–RF_N[20])

	RF_N_CNTR [14:0]														
Divide Ratio	**C Word**											**B Word**		**A Word**	
1–47	Divide Ratios Less than 48 are impossible since it is required that C>=3														
48–79	Some of these N values are Legal Divide Ratios, some are not														
80	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0
81	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1
...	.	.	.	.	.	.	.	.	.	.	.	0	.	.	.
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

FRACTIONAL MODULUS ACCUMULATOR (FRAC_CNTR) (RF_N[2]–RF_N[5])

Fractional Ratio (F)		**FRAC_CNTR**			
Modulus 15	**Modulus 16**	**RF_N[5]**	**RF_N[4]**	**RF_N[3]**	**RF_N[2]**
0	0	0	0	0	0
1/15	1/16	0	0	0	1
2/15	2/16	0	0	1	0
•	•	•	•	•	•
14/15	14/16	1	1	1	0
N/A	15/16	1	1	1	1

QUADRATURE MODULUS PRESCALER

The LMX2354 contains a quadrature modulus prescaler, consisting of a prescaler, A counter, B counter and C counter. Once the N value is known, the A, B, and C values can be calculated by:

C = N div P

B = (N–C•P) div 4

A = N mod 4

For the divide ratio to be legal, it is also required:

C>=max {A, B} + 2

fvco = [N + F] x [fosc / R]

N = P • C + 4•B + A

F: Fractional ratio (contents of FRAC_CNTR divided by the fractional modulus)

f_{vco}: Output frequency of external voltage controlled oscillator (VCO)

C: Preset value of the C counter

B: Preset value of the B counter

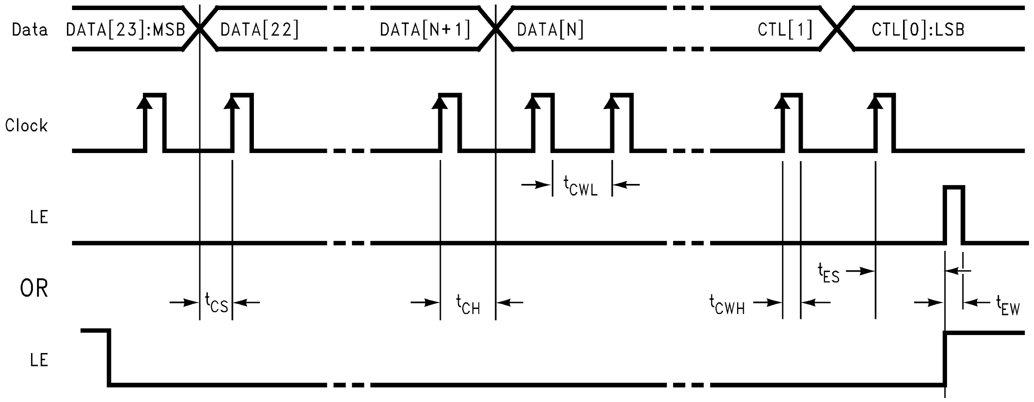
A: Preset value of the A counter

f_{osc}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 15-bit programmable reference counter (3 to 32,767)

P: Preset modulus of quadrature modulus prescaler
8/9/12/13 550 MHz–1.2 GHz
16/17/20/21 1.2 GHz–2.5 GHz

SERIAL DATA INPUT TIMING



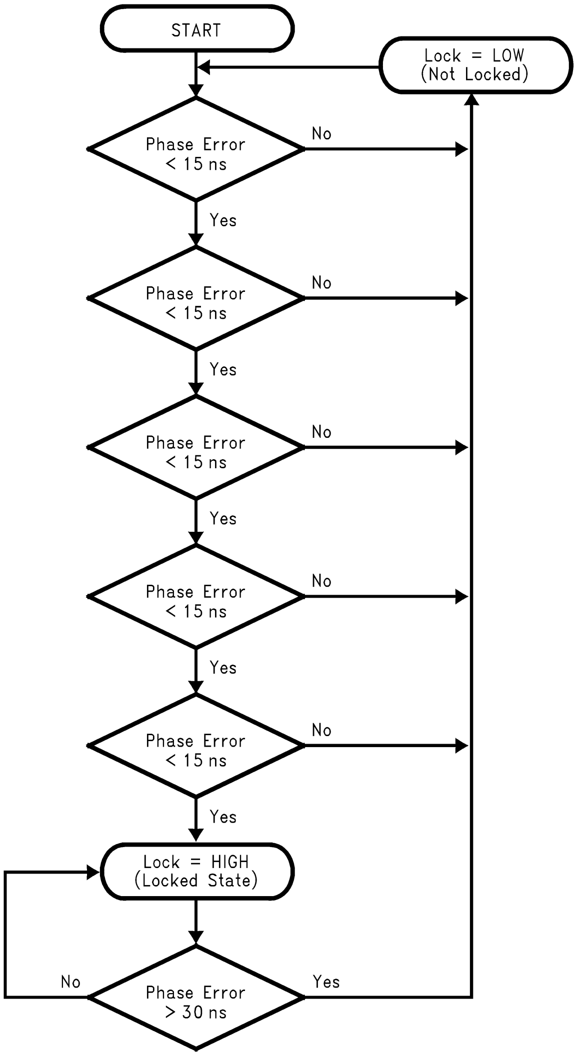
NOTE

Data shifted into register on clock rising edge. Data is shifted in MSB first.

TEST CONDITIONS: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6 V/ns with amplitudes of 2.2V @ V_{CC}=2.7V and 2.6V @ V_{CC} = 5.5V.

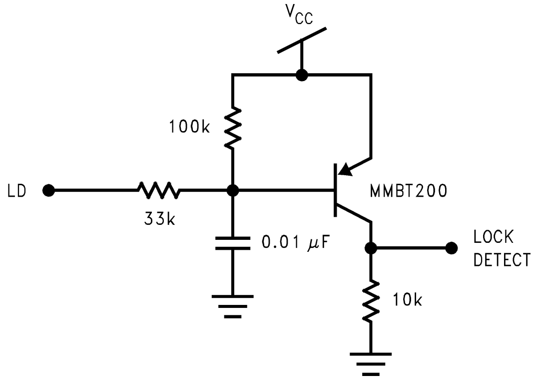
LOCK DETECT DIGITAL FILTER

The Lock Detect Digital Filter compares the difference between the phase of the inputs of the phase detector to a RC generated delay of approximately 15 ns. To enter the locked state (Lock = HIGH) the phase error must be less than the 15 ns RC delay for 5 consecutive reference cycles. Once in lock (Lock = HIGH), the RC delay is changed to approximately 30 ns. To exit the locked state (Lock = LOW), the phase error must become greater than the 30 ns RC delay. When the PLL is in the power down mode, Lock is forced LOW. A flow chart of the digital filter is shown at right.

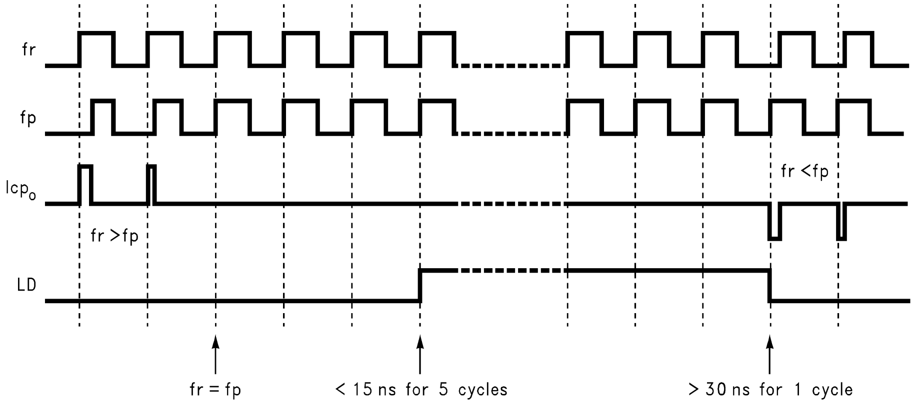


ANALOG LOCK DETECT FILTER

When the Fo/LD output is configured in analog lock detect mode an external lock detect circuit is needed in order to provide a steady LOW signal when the PLL is in the locked state. A typical circuit is shown below.



TYPICAL LOCK DETECT TIMING



REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	**Page**
• Changed layout of National Data Sheet to TI format	21

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