THE DATASHEET OF

LMV1088RL/NOPB

LMV1088 Dual Input, Far Field Noise Suppression Microphone Amplifier with Automatic Calibration Ability

Check for Samples: LMV1088

FEATURES

- **Low Power Consumption**
- **No Added Processing Delay**
- **Automatic Calibration**
- **Space-Saving 36 Bump DSBGA Package**
- **Up to 20dB SNRI**

APPLICATIONS

- **Mobile Handsets**
- **Mobile and Handheld Two-Way Radios**
- **Bluetooth and Other Powered Headsets**
- **Hand-Held Voice Microphones**
- **Portable Public Address Systems**

KEY SPECIFICATIONS

- **(3.3V Supply, Unless Otherwise Specified)**
- **Supply Voltage 2.7V to 5.5 V**
- **Supply Current 1mA (typ)**
- **Signal to Noise Ratio (A-Weighted) 60 dB (typ)**
- **Total Harmonic Distortion 0.1% (typ)**
- **Noise Cancellation 20 dB (typ)**
- **PSRR 85 dB (typ)**

DESCRIPTION

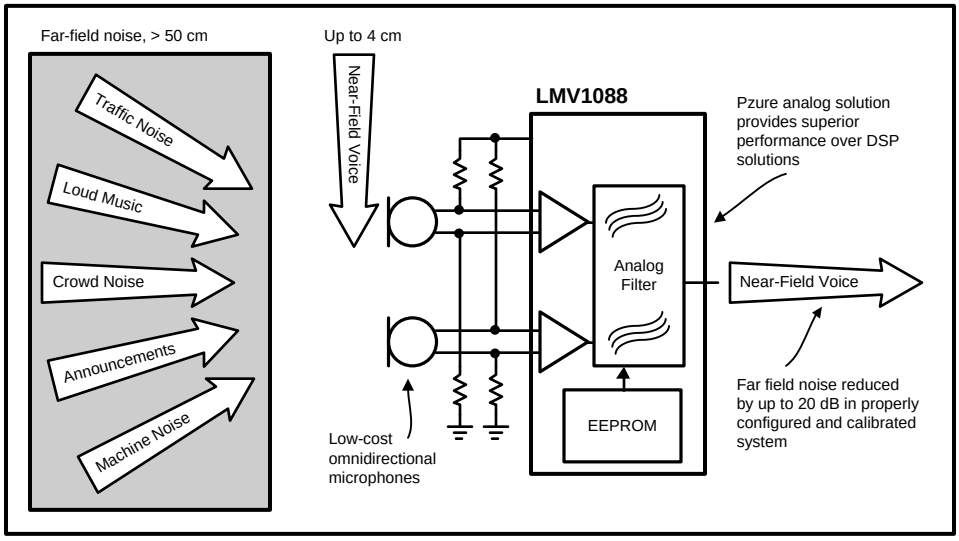
The LMV1088 amplifies near-field voice signals within 4cm of the microphones while rejecting far-field acoustic noise greater than 0.5m from the microphones. Up to 20dB of far-field rejection is possible in a properly configured and calibrated system.

Part of the Powerwise® family of energy efficient solutions, the LMV1088 consumes 1mA of supply current while providing superior performance to DSP solutions consuming over 10 times the power.

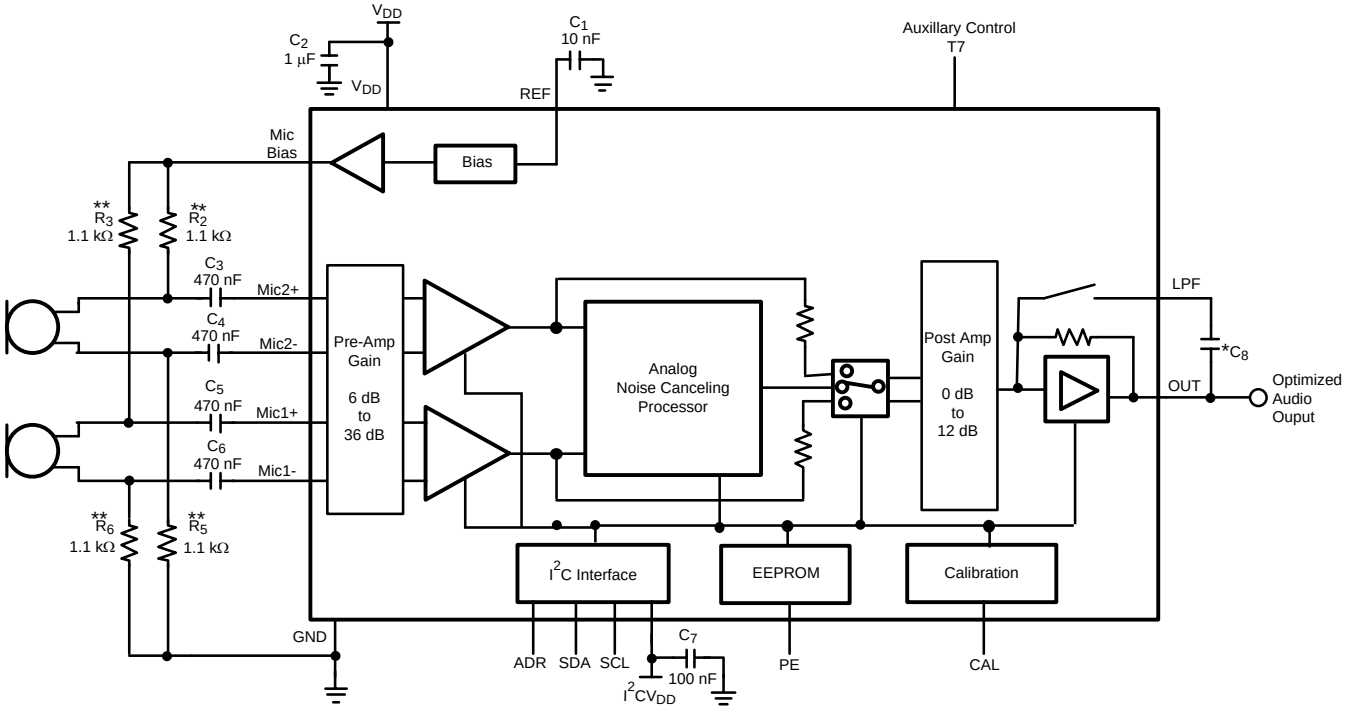
A fast calibration during the manufacturing test process allows the LMV1088 to compensate the entire microphone system. This calibration includes mismatch in microphone gain and frequency response, as well as acoustical path variances. The LMV1088 stores the calibration coefficients in on-board EEPROM. The calibration is initiated by I2C command or by pin control.

The dual microphone inputs are differential to provide excellent noise immunity. The microphones are biased with an internal low-noise bias supply.

Application of the LMV1088



Typical Application



* The value of the low pass filter capacitor is application dependent, see the application section for additional information.
** The value of the microphone resistors is a standard value often used for electric microphones.

Figure 1. Typical Dual Microphone Far Field noise Cancelling Application

Connection Diagram

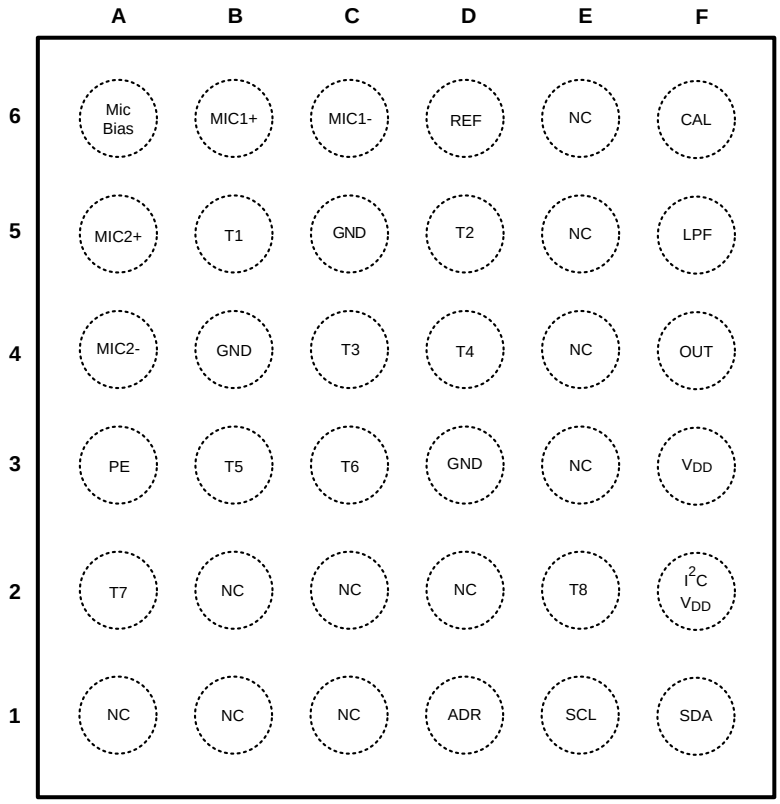


Figure 2. 36 Bump DSBGA package (Top View)
See Package Number YPG0036TTA

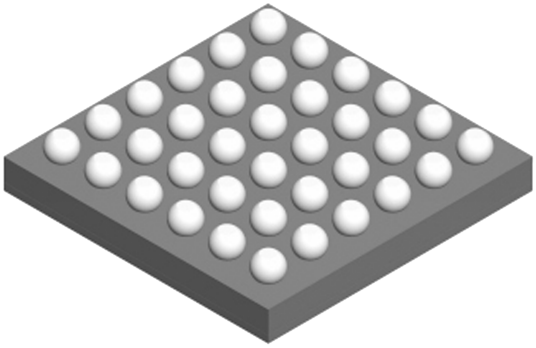


Figure 3. DSBGA Package View (Bottom View)

Pin Descriptions

Bump Number	Pin Name	Pin Type	Pin Function
A1	NC	No Connect	No Connect (1)
A2	T7	Digital Input	Auxiliary_Control pin (2)
A3	PE	Digital Input	Program Enable EEPROM
A4	MIC2–	Analog Input	microphone 2 input –
A5	MIC2+	Analog Input	microphone 2 input +
A6	Mic Bias	Analog Output	Bias for Microphones
B1	NC	No Connect	No Connect (1)
B2	NC	No Connect	No Connect (1)
B3	T5		Float (3)
B4	GND	Ground	Amplifier ground
B5	T1		Float (3)
B6	MIC1+	Analog Input	Microphone 1 input +
C1	NC	No Connect	No Connect (1)
C2	NC	No Connect	No Connect (1)
C3	T6		Float (3)
C4	T3		Float (3)
C5	GND	Ground	Amplifier ground
C6	MIC1–	Analog Input	Microphone 1 input –
D1	ADR	Digital Input	I^2C Address select
D2	NC	No Connect	No Connect (1)
D3	GND	Ground	Amplifier ground
D4	T4		Float (3)
D5	T2		Float (3)
D6	REF	Analog Reference	Reference Voltage De-coupling
E1	SCL	Digital Input	I^2C Clock
E2	T8	Ground	Connect to GND
E3	NC	No Connect	No Connect (1)
E4	NC	No Connect	No Connect (1)
E5	NC	No Connect	No Connect (1)
E6	NC	No Connect	No Connect (1)
F1	SDA	Digital Input/Output	I^2C Data
F2	I^2CV_{DD}	Supply	I^2C power supply
F3	V_{DD}	Supply	Power Supply
F4	OUT	Analog Output	Optimized Audio Out
F5	LPF	Analog Input	Lowpasss Filter Capacitor
F6	CAL	Digital Input	Calibration Start

(1) Connect NC pins to GND for optimum noise performance.
(2) Force V_{DD} setup for manual calibrations. Force GND setup for calibration circuitry.
(3) Do not ground pins.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage	6.0V
Storage Temperature	-85°C to +150°C
ESD Rating (3)	2000V
ESD Rating (4)	200V
Junction Temperature (T_{JMAX}) (5)	150°C
Mounting Temperature Infrared or Convection (20 sec.)	235°C
Thermal Resistance θ_{JA} (DSBGA)	70°C/W
Soldering Information See AN-1112 (SNVA009) "DSBGA Wafers Level Chip Scale Package."	

(1) "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum* Ratings or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human body model, applicable std. JESD22-A114C.
(4) Machine model, applicable std. JESD22-A115-A.
(5) The maximum power dissipation must be de-rated at elevated temperatures and is dictated by T_{JMAX}, θ_{JC}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/ \theta_{JA}$ or the number given in the *Absolute Maximum Ratings*, whichever is lower. For the LMV1088, T_{JMAX} = 150°C and the typical θ_{JA} for this DSBGA package is 70°C/W and for the LLP package θ_{JA} is 64°C/W Refer to the Thermal Considerations section for more information.

Operating Ratings (1)

Supply Voltage	2.7V to 5.5V
I^2CV_{DD} (2)	1.8V to 5.5V
Temperature Range	−40°C to 85°C

(1) *The Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(2) The voltage at I^2CV_{DD} must not exceed the voltage on V_{DD}.

Electrical Characteristics 3.3V and 5.0V(1)

Unless otherwise specified, all limits specified for T_J = 25°C, V_{DD} = 3.3V and 5.0V, V_{IN} = 18mV$_{P-P}$, pass through mode (2), preamplifier gain = 20dB, postamplifier gain = -2.5dB, R_L = 100kΩ, and C_L = 4.7pF.

Symbol	Parameter	Conditions	LMV1088		Units (Limits)
			Typical (3)	Limits (4)	
SNR	Signal-to-Noise Ratio	f = 1kHz, V_{IN} = 18mV$_{PP}$, A-Weighted	60		dB
V_{IN}	Max Input Signal	f = 1kHz and THD+N < 1%	97		mV$_{P-P}$
V_{OUT}	AC Output Voltage	f = 1kHz, preamp gain = 36dB V_{IN} = 30mV$_{P-P}$	500		mV$_{RMS}$
	DC Output Voltage		800		mV
THD+N	Total Harmonic Distortion + Noise	f = 1kHz, V_{IN} = 18mV$_{P-P}$	0.1		%
Z_{IN}	Input Impedance		100		kΩ
Z_{OUT}	Output Impedance		150		Ω
Z_{LOAD}		R_{LOAD} C_{LOAD}		10 10	kΩ (min) pF (max)
A_M	Microphone Pre Amplifier Gain Range	f = 1kHz	6 – 36		dB
A_{MR}	Microphone Pre Amplifier Gain Adjustment Resolution	f = 1kHz	2		dB
A_P	Post Amplifier Gain Range	f = 1kHz Pass Through Mode and Summing Mode	-2.5 – 9.5		dB
		f = 1kHz Noise Canceling Mode (5)	0 – 12		dB
A_{PR}	Post Amplifier Gain Adjustment Resolution	f = 1kHz	3		dB
A_{CR}	Gain Compensation Range	f = 300Hz – f = 3400Hz		±3	dB (max)
A_{MD}	Gain Matching Difference After Calibration	f = 300Hz f = 1kHz f = 3kHz		0.5 0.5 0.5	dB (max) dB (max) dB (max)
T_{CAL}	Calibration Duration			770	ms (max)
PSRR	Power Supply Rejection Ratio	Input Referred, Input AC grounded			
		f = 217Hz (100mV$_{P-P}$)	85		dB
		f = 1kHz (100mV$_{P-P}$)	80		dB
CMRR	Common Mode Rejection Ratio	f = 1kHz,	60		dB
V_{BM}	Microphone Bias Supply Voltage	I_{BIAS} = 1mA	2.0		V
ε_{VBM}	Microphone Bias Supply Noise	A-Weighted	10		μV$_{RMS}$
I_{BM}	Total available Microphone Bias Current			1.2	mA (min)
I_{DDQ}	Supply Quiescent Current	V_{IN} = 0V	1	1.5	mA (max)
I_{DDCP}	Supply Current during Calibration and Programming	Calibrating or Programming EEPROM	28	50	mA (max)
I_{DD}	Supply Current	V_{IN} = 25mV$_{P-P}$ both inputs, Noise canceling mode	1	1.5	mA (max)

(1) "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum* Ratings or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) In Pass Through mode, only one microphone input is active. See also I^{2}C Compatible Interface for more information how to configure the LMV1088.

(3) Typical values represent most likely parametric norms at T_A = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not specified.

(4) Datasheet min/max specification limits are specified by test, or statistical analysis.

(5) In Noise Canceling Mode there is 2.5dB additional gain before calibration when compared to the other operating modes to compensate for the gain reduction that is caused by the noise canceling effect.

Digital Interface Characteristics (1) (2)

Unless otherwise specified, all limits specified for T_J = 25°C, I^2CV_{DD} within the Operating Rating (2)

Symbol	Parameter	Conditions	LMV1088		Units (Limits)
			Typical (3)	Limits (4)	
V_{IH}	Logic High Input Level	SCL, SDA, ADR, CAL, PE pins		0.6xI^2CV_{DD}	V (min)
V_{IL}	Logic Low Input Level	SCL, SDA, ADR, CAL, PE pins		0.4xI^2CV_{DD}	V (max)
ts_{CAL}	CAL Setup Time		2		ms
th_{CAL}	CAL Hold time until calibration is finished			770	ms (min)
ts_{PEC}	PE Setup Time		2		ms
th_{PEC}	PE Hold until calibration is finished			770	ms (min)

(1) "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum* Ratings or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) The voltage at I^2CV_{DD} must not exceed the voltage on V_{DD}.
(3) Typical values represent most likely parametric norms at T_A = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not specified.
(4) Datasheet min/max specification limits are specified by test, or statistical analysis.

Typical Performance Characteristics

Unless otherwise specified, T_J = 25°C, V_{DD} = 3.3V, V_{IN} = 18mV$_{P-P}$, pass through mode (1), preamplifier gain = 20dB, postamplifier gain = –2.5dB, R_L = 100kΩ, and C_L = 4.7pF.

Supply Current vs. Supply Voltage

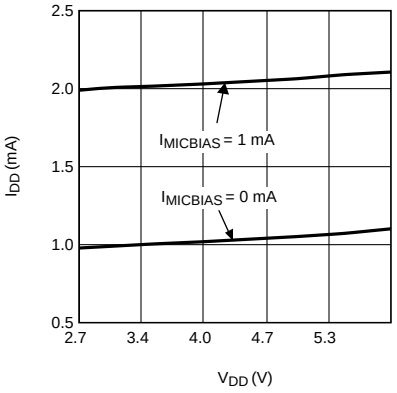


Figure 4.

THD+N vs Frequency, pass through mode Mic1, V_{IN} = 36mV$_{P-P}$

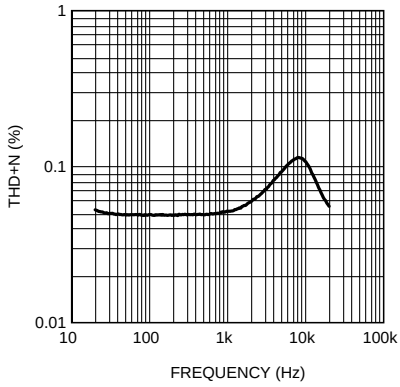


Figure 5.

THD+N vs Frequency, pass through mode Mic2, V_{IN} = 36mV$_{P-P}$

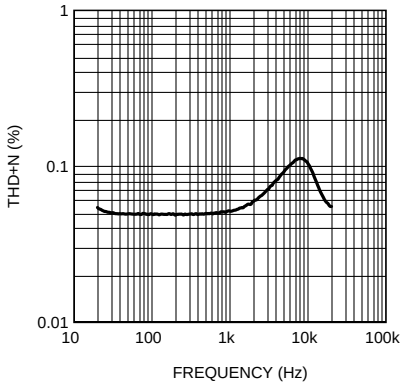


Figure 6.

THD+N vs Frequency, Noise canceling mode signal at Mic1, Mic2 AC shorted, V_{IN} = 36mV$_{P-P}$

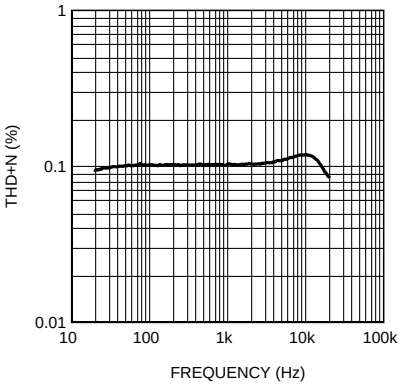


Figure 7.

THD+N vs Frequency, Noise canceling mode Mic1 AC shorted, signal at Mic2, V_{IN} = 36mV$_{P-P}$

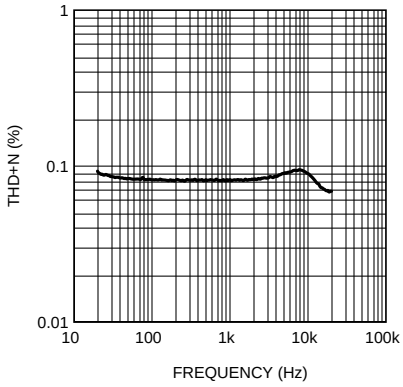


Figure 8.

THD+N vs V_{IN}, pass through mode Mic1

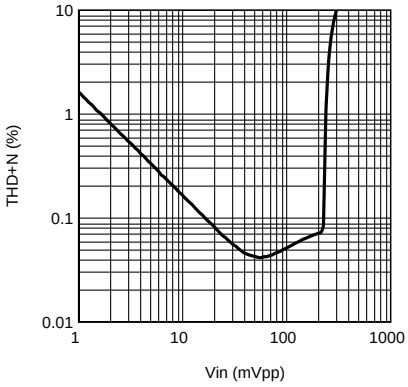


Figure 9.

(1) In Pass Through mode, only one microphone input is active. See also I²C Compatible Interface for more information how to configure the LMV1088.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_J = 25°C, V_{DD} = 3.3V, V_{IN} = 18mV$_{P-P}$, pass through mode (1), preamplifier gain = 20dB, postamplifier gain = –2.5dB, R_L = 100kΩ, and C_L = 4.7pF.

THD+N vs V_{IN}, pass through mode Mic2

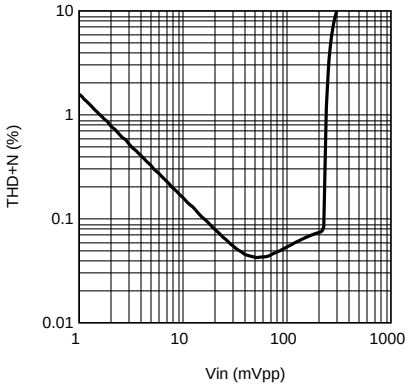


Figure 10.

THD+N vs V_{IN}, Noise canceling mode, signal at Mic1, Mic2 AC shorted

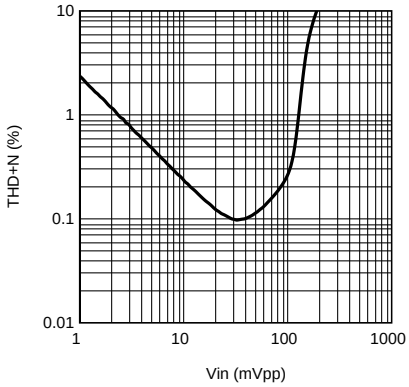


Figure 11.

THD+N vs V_{IN}, Noise canceling mode, Mic1 AC shorted, signal at Mic2

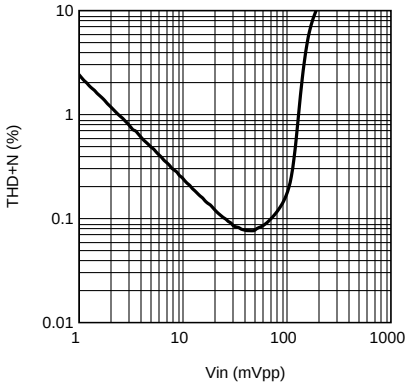


Figure 12.

PSRR vs Frequency, pass through mode Mic1, Mic1+ Mic2 AC shorted

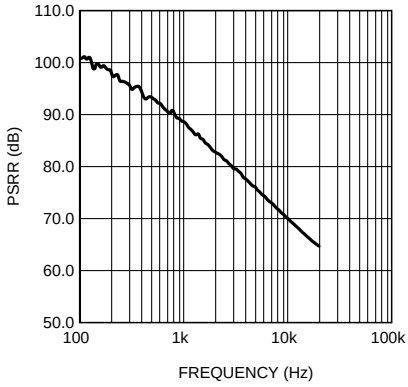


Figure 13.

PSRR vs Frequency, pass through mode Mic2, Mic1+ Mic2 AC shorted

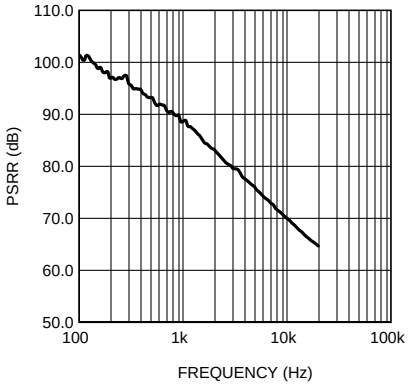


Figure 14.

PSRR vs Frequency, Noise canceling mode, Mic1+ Mic2 AC shorted

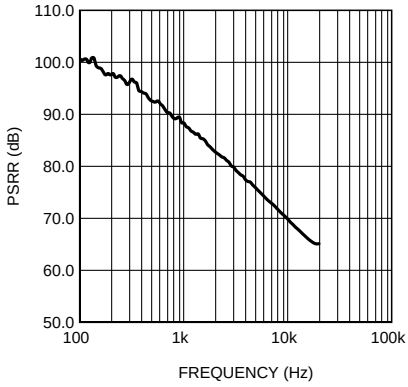


Figure 15.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_J = 25°C, V_{DD} = 3.3V, V_{IN} = 18mV_{P-P}, pass through mode (1), preamplifier gain = 20dB, postamplifier gain = –2.5dB, R_L = 100kΩ, and C_L = 4.7pF.

PSRR
vs
Frequency, Microphone Bias, Mic1+ Mic2 AC shorted

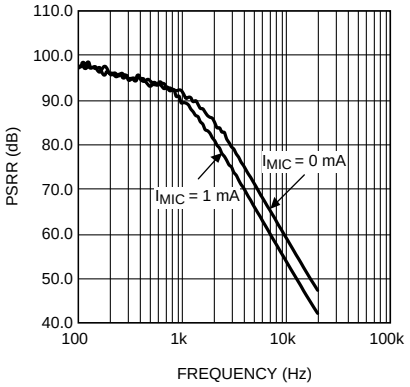


Figure 16.

APPLICATION DATA

Gain Balance and Gain Budget

In systems where input signals have a high dynamic range, critical noise levels and where the dynamic range of the output voltage is also limited, careful gain balancing can be essential for the best performance. Having not enough gain in the Pre Amplifier can result in higher noise levels while to much gain in the Pre Amplifier will result in clipping and saturation in the noise cancelling processor and output stages.

The gain ranges and maximum signal levels for the different functional blocks is shown in Figure 17. Two examples are given as a guideline how to select proper gain settings.

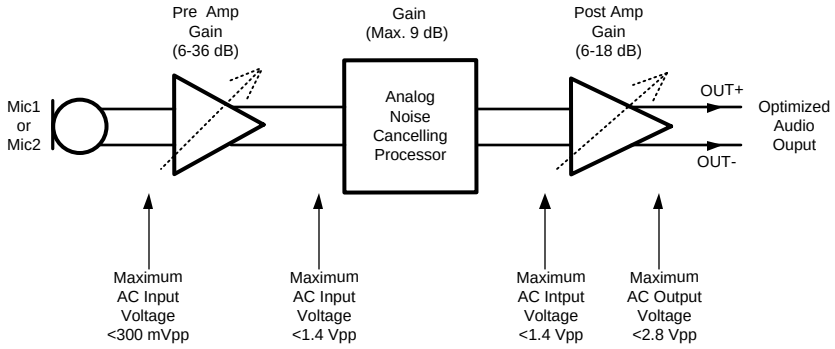


Figure 17. Maximum Signal Levels

EXAMPLE1

An application using microphones with $50mV_{pp}$ maximum output voltage, and a baseband chip after the LMV1088 with $1.5V_{pp}$ maximum input voltage.

For optimum noise performance we would like to have the maximum gain at the input stage.

So using Pre Amp gain =14dB and Post Amp gain = 6dB is the optimum for this application.

1. $50mV_{pp}$ + 36 dB = $3.1V_{pp}$.
2. This is higher than the maximum $1.4V_{pp}$ allowed for the Noice cancelling Processor (NCP). This means a gain lower then 28.9dB should be selected.
3. Select the nearest lower gain from the gain setting table to be 28dB. This will prevent the NCP from being overloaded by the microphone. With this setting, the resulting output level of the Pre Amplifier will be $1.26V_{pp}$.
4. The NCP can have a maximum processing gain of 9dB (depending on the calibration result) which will result in $3.5V_{pp}$ at the output of the LMV1088. This level is higher then maximum level hat is allowed at the input of the Post Amp of the LMV1088. Therefore the Pre Amp gain has to be reduced, to $1.4V_{pp}$ minus 9dB = $0.5V_{pp}$. This limits the Pre Amp gain to a maximum of 20dB.
5. The baseband chip limits the maximum output voltage to $1.5V_{pp}$ with the minimum of 6dB Post Amp gain, this results in having a lower level at the input of the Post Amp of $0.75V_{pp}$. Now calculating this for a maximum NCP gain of 9dB the output of the Pre Amp must be $<266mV_{pp}$.
6. Calculating the new gain for the Pre Amp will result in <1.4 dB gain.
7. The nearest lower gain will be 14dB.

So using Pre Amp gain =14dB and Post Amp gain = 6dB is the optimum for this application.

EXAMPLE 2

An application using microphones with $10mV_{pp}$ maximum output voltage, and a baseband chip after the LMV1088 with $3.3V_{pp}$ maximum input voltage.

For optimum noise performance we would like to have the maximum gain at the input stage.

1. $10mV_{pp}$ + 36dB = $631mV_{pp}$.

2. This is lower than the maximum $1.4V_{pp}$ so this is OK.
3. The NCP can have a maximum processing gain of 9dB (depending on the calibration result) which will result in $3.5V_{pp}$ at the output of the LMV1088. This level is higher then maximum level hat is allowed at the input of the Post Amp of the LMV1088. Therefore the Pre Amp gain has to be reduced, to $1.4V_{pp}$ minus 9dB = $0.5V_{pp}$. This limits the Pre Amp gain to a maximum of 34dB.
4. With a Post Amp gain setting of 6dB the output of the Post Amp will be $2.8V_{pp}$ which is OK for the baseband.
5. The nearest lower Post Amp gain will be 6dB.

So using Pre Amp gain =14dB and Post Amp gain = 6dB is the optimum for this application.

I²C Compatible Interface

I²C SIGNALS

The LMV1088 pin Serial Clock (SCL) is used for the I²C clock SCL and the pin Serial Data (SDA) is used for the I²C data signal SDA. Both of these signals need a pull-up resistor according to I²C specification. The LMV1088 can be controlled through two slave addresses. The two I²C slave address for LMV1088 are given inTable 1 .

Table 1. Chip Address

	D7	D6	D5	D4	D3	D2	D1	D0
1st Chip Address I²C Adress='0'	1	1	0	0	1	1	0	$\overline{W}$/R
2nd Chip Address I²C Adress='1'	1	1	0	0	1	1	1	$\overline{W}$/R

I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW.

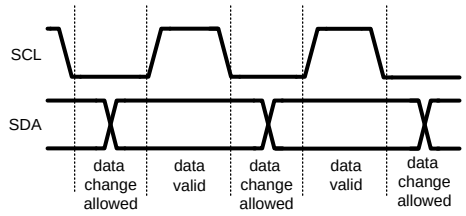
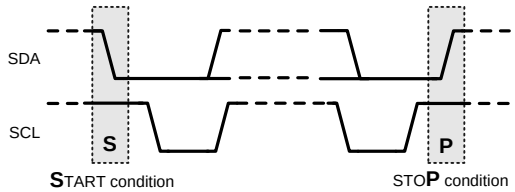


Figure 18. I²C Signals: Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C data transmission session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



The master should issue STOP after no acknowledgement.

Figure 19. I²C Start Stop Conditions

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I^2C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LMV1088 address is **11001100_2**or **11001110_2**. For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

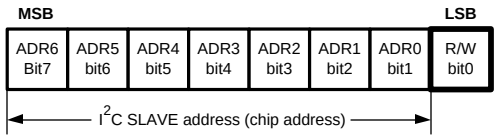
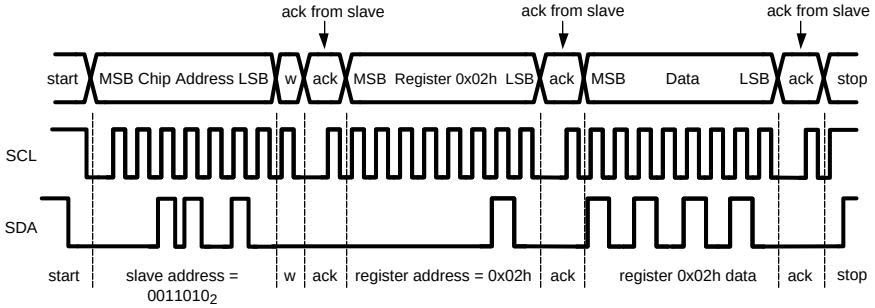


Figure 20. I^2C Chip Address

Register changes take effect at the SCL rising edge during the last acknowledge (ACK) from slave.

In Figure 21 there is a write example shown, for a device at a randomly chosen address**'00110100_2'**.



w = write (SDA = "0")
r = read (SDA = "1")
ack = acknowledge (SDA pulled down by slave)
rs = repeated start

Figure 21. Example I^2C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function.

Figure 22, shows a read example for a device at a random chosen address **'00110101_2'**.

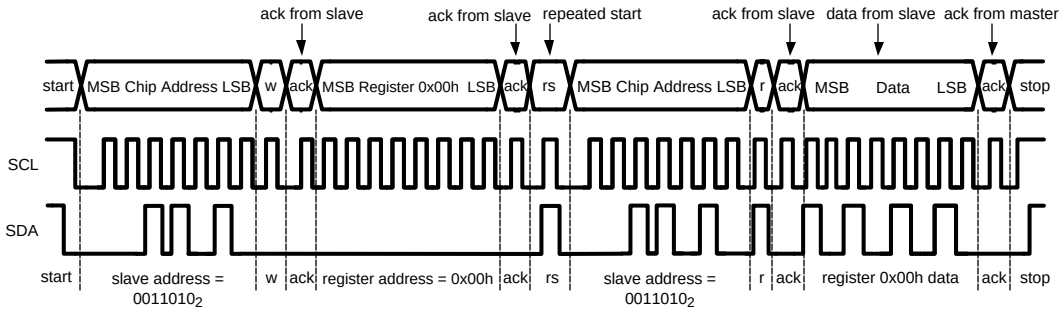


Figure 22. Example I^2C Read Cycle

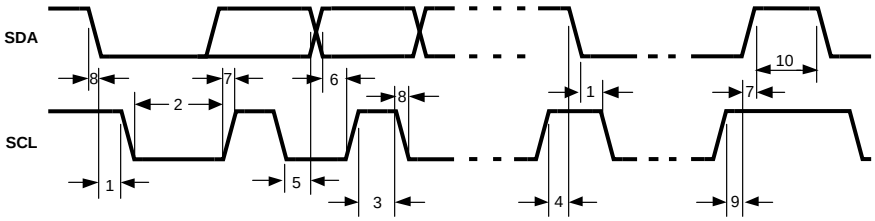


Figure 23. I²C Timing Diagram

Table 2. I²C Timing Paramters(1)

Symbol	Parameter	Limit		Units
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time (Output direction, delay generated by LMV1088)	300	900	ns
5	Data Hold Time (Input direction, delay generated by the Master)	0	900	ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	20	300	ns
8	Fall Time of SDA and SCL	15	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load for Each Bus Line	10	200	pF

(1) Data specified by design

Table 3. I²C Register Description

Address	Reg.	Bits	Description				Default
0x01h	A	[3:0]	Microphone preamplifier gain from 6dB up to 36dB in 2dB steps.				
			0000	6dB			
			0001	8dB			
			0010	10dB			
			0011	12dB			
			0100	14dB			
			0101	16dB			
			0110	18dB			
			0111	20dB			0111
			1000	22dB			
			1001	24dB			
			1010	26dB			
			1011	28dB			
			1100	30dB			
			1101	32dB			
			1110	34dB			
			1111	36dB			
		[5:4]	A4 = Mute mic1 and A5 = mute mic2. (0 = microphone on; 1 = microphone mute)				
		[7:6]	Mic enable bits, A6 = enable Mic 1, A7 = enable Mic 2 (1 = enable Mic; 0 = disable Mic)				
0x02h	B	[2:0]	Gain setting for the post amplifier from (3dB steps) (1).				
				Pass Through mode	Noise Canceling mode		
			000	-2.5dB	0db		
			001	0.5dB	3dB		
			010	3.5dB	6dB		0+00
			011	6.5dB	9dB		
			100	9.5dB	12dB		
			101	9.5dB	12dB		
			110	9.5dB	12dB		
			111	9.5dB	12dB		
		[4:3]	Mic select bits				
			00		Noise canceling mode		00
			01		Only Mic 1 on		
			10		Only Mic 2 on		
			11		Mic 1 + Mic 2		
		[7:5]	Not Used				000
0x0Ch	L	[7:0]	reads the output of the EEPROM				read only
0x0Dh	M	[7:0]	reads the output of the EEPROM				read only
0x0Eh	N	[6:0]	reads the output of the EEPROM				read only
		[7]	Reads the “ready” signal. This give the status of the program cycle. 1 = ready ; 0 = program cycle in progress				read only

(1) In Noise Canceling Mode there is 2.5dB additional gain before calibration when compared to the other operating modes to compensate for the gain reduction that is caused by the noise canceling effect.

Table 3. I²C Register Description (continued)

Address	Reg.	Bits	Description			Default
0x0Fh	O	[7:4]	Control the gain compensation between the two mics at 300Hz (2)			
			0000 (0)	0.0dB		0000
			0001 (1)	0.5dB		
			0010 (2)	1.0dB		
			0011 (3)	1.5dB		
			0100 (4)	2.0dB		
			0101 (5)	2.5dB		
			0110 (6)	3.0dB		
			0111 (7)	Not used		
			1000 (8)	Not used		
			1001 (9)	–0.5dB		
			1010 (A)	–1.0dB		
			1011 (B)	–1.5dB		
			1100 (C)	–2.0dB		
			1110 (D)	–2.5dB		
			1110 (E)	–3.0dB		
			1111 (F)	Not Used		
		[3:0]	Control the gain compensation between the two mics at 3kHz (2)			
			0000 (0)	0.0dB		0000
			0001 (1)	0.5dB		
			0010 (2)	0.0dB		
			0011 (3)	1.5dB		
			0100 (4)	2.0dB		
			0101 (5)	2.5dB		
			0110 (6)	3.0dB		
			0111 (7)	Not used		
			1000 (8)	Not used		
			1001 (9)	–0.5dB		
			1010 (A)	–1.0dB		
			1011 (B)	–1.5dB		
			1100 (C)	–2.0dB		
			1101 (D)	–2.5dB		
			1110 (E)	–3.0dB		
			1111 (F)	Not used		

(2) Connect NC pins to GND for optimum noise performance.

Table 3. I²C Register Description (continued)

Address	Reg.	Bits	Description			Default
0x10h	P	[7:4]	Control compensation gain for Mic2 channel at ALL frequencies(3)			
			0000 (0)	–3.0dB		0000
			0001 (1)	–3.0dB		
			0010 (2)	–2.5dB		
			0011 (3)	–2.0dB		
			0100 (4)	–1.5dB		
			0101 (5)	–1.0dB		
			0110 (6)	–0.5dB		
			0111 (7)	0.0dB		
			1000 (8)	0.0dB		
			1001 (9)	0.5dB		
			1010 (A)	1.0dB		
			1011 (B)	1.5dB		
			1100 (C)	2.0dB		
			1101 (D)	2.5dB		
			1110 (E)	3.0dB		
			1111 (F)	3.0dB		
		[3:0]	Control compensation gain for Mic1 channel at ALL frequencies (3)			
			0000 (0)	–3.0dB		0000
			0001 (1)	–3.0dB		
			0010 (2)	–2.5dB		
			0011 (3)	–2.0dB		
			0100 (4)	–1.5dB		
			0101 (5)	–1.0dB		
			0110 (6)	–0.5dB		
			0111 (7)	0.0dB		
			1000 (8)	0.0dB		
			1001 (9)	0.5dB		
			1010 (A)	1.0dB		
			1011 (B)	1.5dB		
			1100 (C)	2.0dB		
			1101 (D)	2.5dB		
			1110 (E)	3.0dB		
			1111 (F)	3.0dB		
0x11h	Q	[6:0]	Values are clocked into EEPROM registers once “newdata” pulse is generated			
		[7]	StoreBar signal storeBar = 0 enables EEPROM programming storeBar = 1 data clock into EEPROM registers			1
0x12h	R	[0]	Start Calibration via I2C ‘0’ to ‘1’ = start calibration (keep ‘1’ during calibration)			0
		[7]	Internal test			0000000

(3) Connect NC pins to GND for optimum noise performance.

( ) represents binary value in hexadecimal format

Automatic Calibration

The full automatic calibration should only be required once, when the product containing the LMV1088 has completed manufacture, and prior to application packaging. The product containing the LMV1088 will be calibrated to the microphones, the microphone spacings, and the acoustical properties of the final manufactured product containing the LMV1088.

The compensation or calibration technology is achieved via memory stored coefficients when the FFNS circuitry activates the calibration sequence. The purpose of the calibration sequence is to choose the optimized coefficients for the FFNS circuitry for the given microphones, spacing, and acoustical environment of the product containing the LMV1088.

A basic calibration can be performed with a single 1kHz tone, however to take full advantage of this calibration feature a three tone calibration (See the section PERFORMING A THREE TONE CALIBRATION) is preferred .

The automatic calibration process can be initiated from either a digital interface CALIBRATE pin (CAL) or via the I^2C interface.

The logic level at the PROGRAM ENABLE (PE) pin determines if the result of the calibration is volatile or permanent. To make the result of the calibration permanent (stored in the EEPROM) the PROGRAM ENABLE (PE) pin must be high during the automatic calibration process.

AUTOMATIC CALIBRATION VIA CAL PIN

To initiate the automatic calibration via the CAL pin, the following procedure is required:

- From the initial condition where both PE and CAL are at 'low' level
- bring PE to a 'high' level (enable EEprom write)
- bring CAL to a 'high' level to start Calibration
- Apply Audio stimulus (single tone 1kHz or three tone sequence as described in PERFORMING A THREE TONE CALIBRATION)
- Hold CAL 'high' for at least 770ms
- Remove Audio stimulus
- bring CAL to a 'low' level to stop Calibration
- bring PE to a 'low' level (disable EEprom write)

A tone may be applied prior to the rising of CAL and PE. Signals applied to the microphone inputs before rising of CAL and PE are ignored by the calibration system.

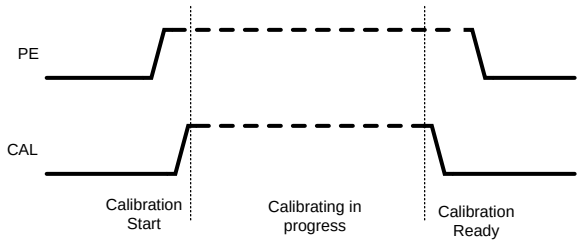


Figure 24. Automatic Calibration via CAL pin

NOTE

When the I^2C is operated, make sure that register 'R' (address 0x12) bit 0 is '0' before operating the CAL pin (default value for this bit). When this bit is set '1' the calibration engine of the LMV1088 is started and will remain active with a higher supply current than normal operation. The state of the calibration remains active until this bit is reset, '0". With the bit set the 'low' to' high' transfer of the CAL pin will be ignored.

AUTOMATIC CALIBRATION VIA I^2C COMMAND

To initiate the automatic calibration via the I^2 interface, the following procedure is required:

- From the initial condition where PE is 'low' level

- Bring PE to a 'high' level (enable EEprom write)
- Write '1' into I^2C register 'R' (address 0x12) bit 0 to start calibration
- Apply Audio stimulus (single tone 1kHz or three tone sequence as described in PERFORMING A THREE TONE CALIBRATION)
- Wait at least 770ms
- Remove Audio stimulus
- Write '0' into I^2C to finish calibration
- Bring PE to a 'low' level (disable EEprom write)

A tone may be applied prior to the rising of CAL and PE. Signals applied to the microphone inputs before rising of CAL and PE are ignored by the calibration system.

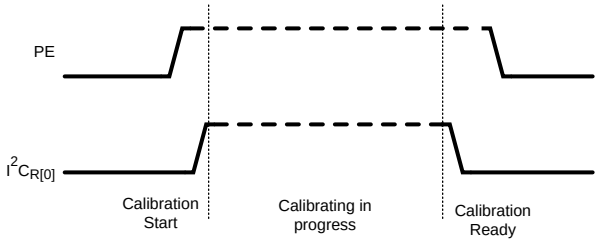


Figure 25. Automatic Calibration via I^2C COMMAND

PERFORMING A THREE TONE CALIBRATION

In a system with two microphones in an enclosure there will always be a difference in the transfer function in both gain and frequency response. The LMV1088 has the capability to perform an automatic calibration function to minimize these differences. To perform this calibration, a test sequence of three tones is required right after the PE and CAL inputs are brought to a logic high level. At the end of this sequence the calibration data is automatically stored in the internal EEPROM.

The three tones have to be applied as follows:

- A first tone with a frequency of 1kHz
- A second tone with a frequency of 300Hz
- A third tone with a frequency of 3kHz

A tone may be applied prior to the rising of CAL and PE. Signals applied to the microphone inputs before rising of CAL and PE are ignored by the calibration system. .

Between each tone pair there is a small time, indicated by a cross, to change the frequency. During that time the input tone is ignored by the calibration system.

The total calibration sequence requires less then 770ms.

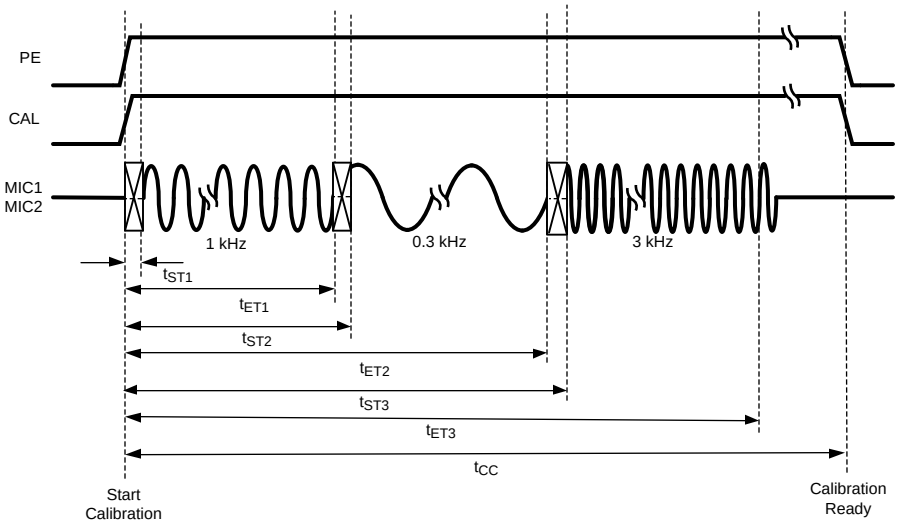


Figure 26. Three Tone Calibration Timing

Table 4. Automatic Calibration Timing Parameters(1)

Symbol	Parameter	Limits		Unitis
		Min	Max	
t_{ST1}	Calibration Start Tone 1		10	ms
t_{ET1}	Calibration End Tone 1	200		ms
t_{ST2}	Calibration Start Tone 2		215	ms
t_{ET2}	Calibration End Tone 2	400		ms
t_{ST3}	Calibration Start Tone 3		415	ms
t_{ET3}	Calibration End Tone 3	600		ms
t_{CC}	Calibration Complete	770		ms

(1) Data specified by design

THREE TONE CALIBRATION SETUP

A calibration test setup consist of a test room (acoustical box) with a loudspreaker (acoustical source) driven with the test tone sequence from Figure 26. The test setup is shown in Figure 27. The distance between the source and microphone 1 and microphone 2 must be equal and the sound must travel without any obstacle from source to both microphones.

The sound will travel with the limited speed of 300m/s from the loudspeaker source to the microphones. When creating the calibration signals this time should not be ignored, 30cm distance will cause 1ms delay.

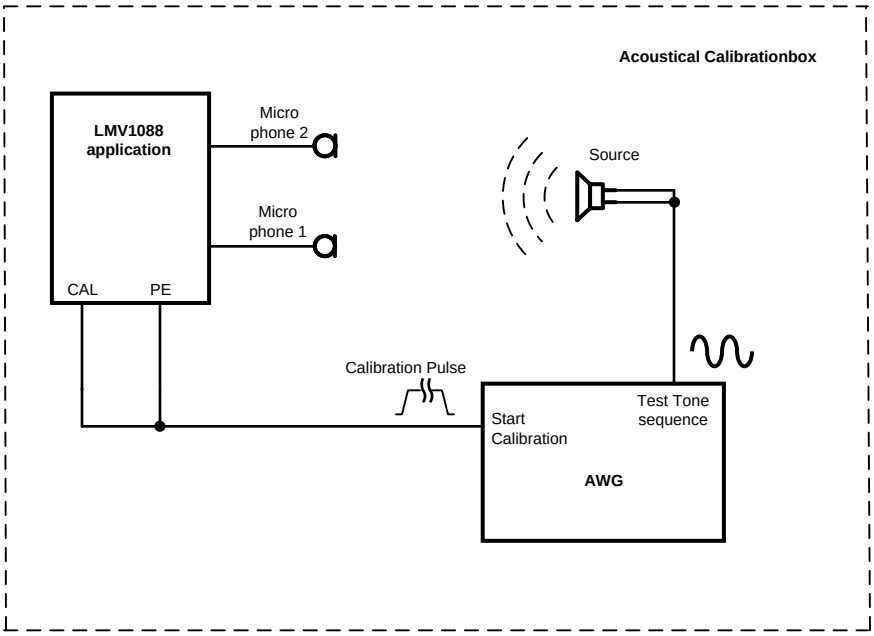
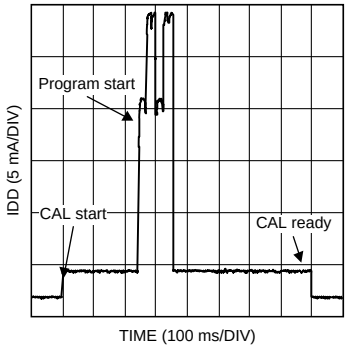


Figure 27.

SUPPLY CURRENT DURING CALIBRATION

The Calibration function performs two main tasks in a sequence. First the AC characteristics of the microphones are matched. Then in the second stage, if the PE pin is high, the on-chip EEPROM is programmed.

During the first stage of this sequence the supply current on the LMV1088 will increase to about 2.5 mA. During the writing of the EEPROM the supply current will rise for about 215ms to about 30 mA. This increased current is used for the on chip charge pump which generates the high voltages that are required for programming the EEPROM.



Manual Calibration

You can manually program the gain of the two mic inputs on the LMV1088 using the I^2C interface. Table 4 shows the control bits for I^2C Register O and P with the corresponding gains. This can be easily done by doing the following:

1) READ contents of the I^2C register N immediately after powering up.

2) Set PE pin and T7 pin to Vdd.

3) WRITE to I2C register O and P to choose the calibration settings.

Bits O<7:4> control the two mics at 300 Hz and bits O<3:0> control the two mics at 3kHz.

Bits P<7:4> control the Mic2 gain and bits P<3:0> control the Mic1 gain

4) WRITE a '0' to I2C register Q<7> bit (storeBar) and the bits from I2C register N<6:0> to I2C register Q<6:0>

5) When I2C register N<7> (ready) goes high, then the EEPROM programming is complete. Now PE pin and T7 pin should be set to GND and I2C register Q<7> (storeBar) should be returned to '1'.

Low-Pass Filter At The Output

At the output of the LMV1088 there is a provision to create a 1st order low-pass filter (only enabled in 'Noise Cancelling' mode). This low-pass filter can be used to compensate for the change in frequency response that results from the noise cancellation process.. The change in frequency response resembles a first-order high-pass filter, and for many of the applications it can be approximately compensated by a first-order low-pass filter with cutoff frequency between 1.5kHz and 2.5kHz.

The transfer function of the low pass filter is derived as:

H(s) = Post Amplifier / SRfCf + 1 (1)

This low-pass filter is created by connecting a capacitor between the LPF pin and the OUT pin of the LMV1088. The value of this capacitor also depends on the selected output gain. For different gains the feedback resistance in the Low-pass Filter network changes as shown in Table 5.

Table 5. Low-pass Filter internal impedance

Post Amplifier Gain Setting (dB) (1)	Feedback resistance R_{if} (kΩ)
0	20
3	29
6	40
9	57
12	80

(1) Noise Cancelling Mode

This will result in the following values for a cutoff frequency of 2000 Hz:

Table 6. Low—pass Filter Capacitor for 2kHz

Post Amplifier Gain Setting (dB) (1)	R_{if} (kΩ)	C_f (nF)
0	20	3.9
3	29	2.7
6	40	2.0
9	57	1.3
12	80	1.0

(1) Noise Cancelling Mode

Measurement Setup

Because of the nature of the calibration system it is not possible to predict the absolute gain in the two microphone channels of the Far Field Noise Cancelling System. This is because, after the calibration function has been operated, the noise cancelling circuit will compensate for the difference in gain between the microphones. In Noise Cancelling mode, this can result in a final gain offset of max 3dB between the gain set in the registers (RA[3:0] and RB[2:0]) and the actual measured gain between input and output of the LMV1088. After performing a calibration the frequency characteristic of the microphone channels will be matched for the two microphones. As a result of this matching there can be a slight slope in the frequency characteristic in one or both amplifiers.

A-WEIGHTED FILTER

The human ear is sensitive for acoustic signals within a frequency range from about 20Hz to 20kHz. Within this range the sensitivity of the human ear is not equal for each frequency. To approach the hearing response, weighting filters are introduced. One of those filters is the A-weighted filter.

The A-weighted filter is used in signal to noise measurements and THD+N measurements, where the wanted audio signal is compared to device noise and distortion.

The use of this filter improves the correlation of the measured values to the way these ratios are perceived by the human ear.

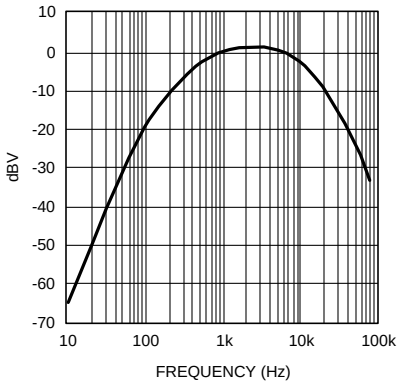


Figure 28. A-Weighted Filter

MEASURING NOISE AND SNR

The overall noise of the LMV1088 is measured within the frequency band from 10Hz to 22kHz using an A-weighted filter. The Mic+ and Mic- inputs of the LMV1088 are shorted for AC signals via a short between the input capacitors , see Figure 29.

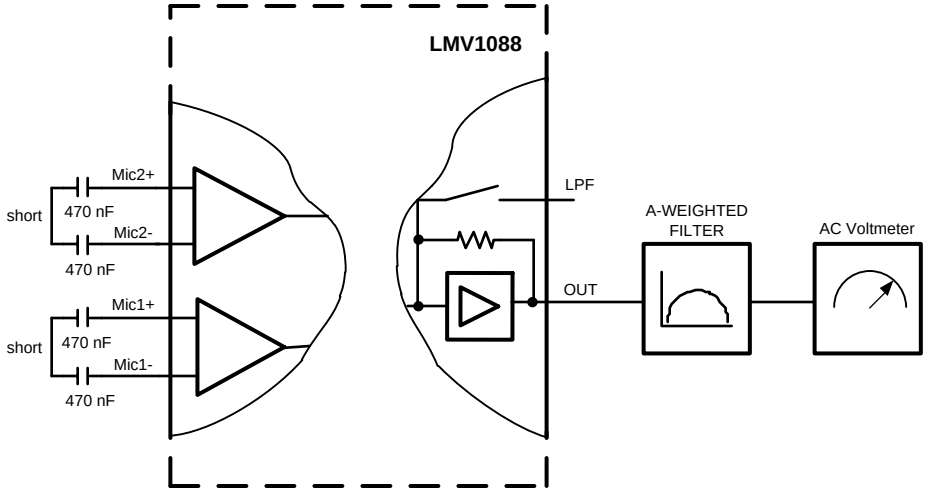


Figure 29. Noise Measurement Setup

For the signal to noise ratio (SNR) the signal level at the output is measured with a 1kHz input signal of $18mV_{PP}$ using an A-weighted filter. This voltage represents the output voltage of a typical electret condenser microphone at sound pressure level of 94dB SPL, which is the standard level for these measurements. The LMV1088 is programmed for 17.5dB of total gain (20dB pre-amplifier and -2.5dB post-amplifier) with only Mic1 or Mic2 on. (See also I^2C Compatible Interface)

The input signal is applied differential between the corresponding Mic+ and Mic- . Because the part is in Pass Through mode the Low-pass Filter at the output of the LMV1088 is disabled.

REVISION HISTORY

Rev	Date	Description
1.0	09/26/07	Initial release.
1.01	12/10/07	Few text edits (changed TL to RL).
1.02	03/07/08	Text edits.
1.03	03/10/08	Replaced Typical Appl. ckt diagrams and some text edits.
1.04	03/12/08	Deleted 5.0V EC table.
1.05	03/14/08	Replaced Tables 4 and 5. Also edited the Application diagram on page 1.
1.06	03/25/08	Text edits and replaced the Typical Application circuit diagram.
1.07	03/28/08	Text edits.
1.08	04/04/08	Text edits.
1.09	04/17/08	Text edits.
1.10	05/27/08	Text edits.
1.11	06/05/08	Edited the Application drawing on page 1.
1.12	09/19/08	Text edits.
1.13	02/11/09	Text edits.
1.14	02/19/09	Deleted the "Clarisound™" symbol from the D/S.
1.15	02/26/09	Deleted the "Clarisound™" label from the Typical Application circuit diagram.

Changes from Revision I (April 2013) to Revision J **Page**

- Changed layout of National Data Sheet to TI format 23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV1088RL/NOPB	NRND	DSBGA	YPG	36	250	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	I (-40 to 85)	ZA1	
LMV1088RLX/NOPB	NRND	DSBGA	YPG	36	1000	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	I (-40 to 85)	ZA1	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

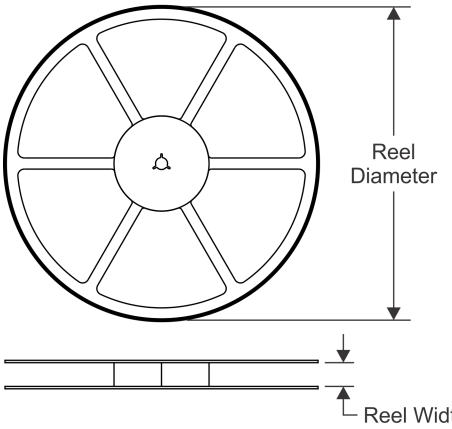
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

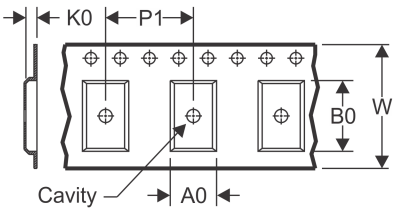
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

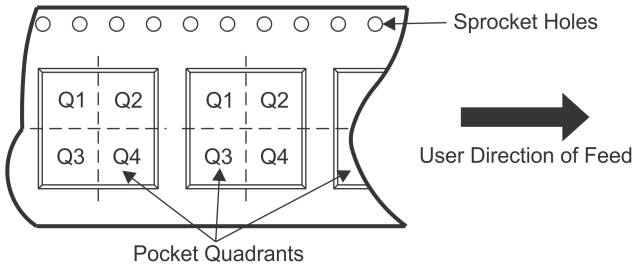


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

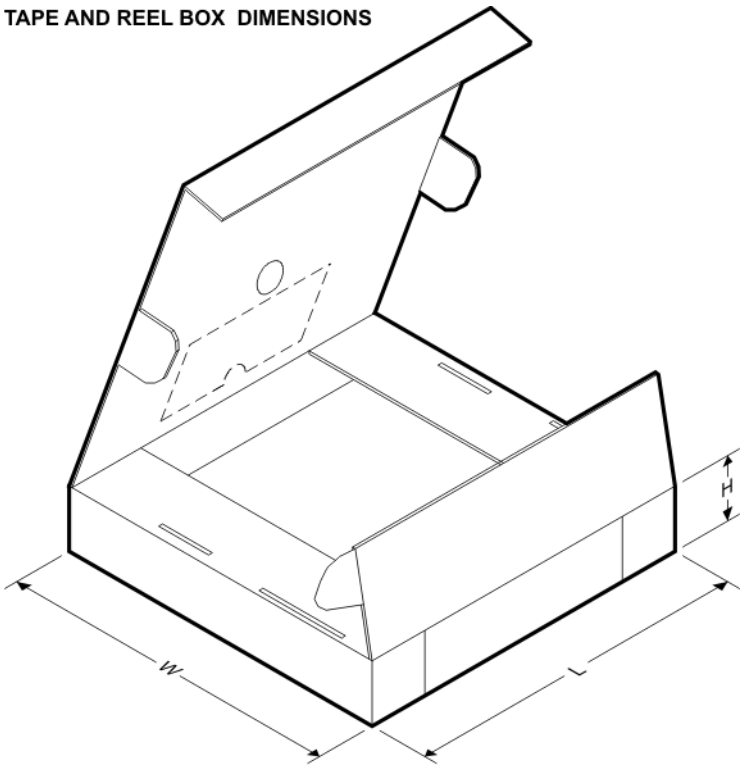
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV1088RL/NOPB	DSBGA	YPG	36	250	178.0	12.4	3.63	3.63	0.76	8.0	12.0	Q1
LMV1088RLX/NOPB	DSBGA	YPG	36	1000	178.0	12.4	3.63	3.63	0.76	8.0	12.0	Q1

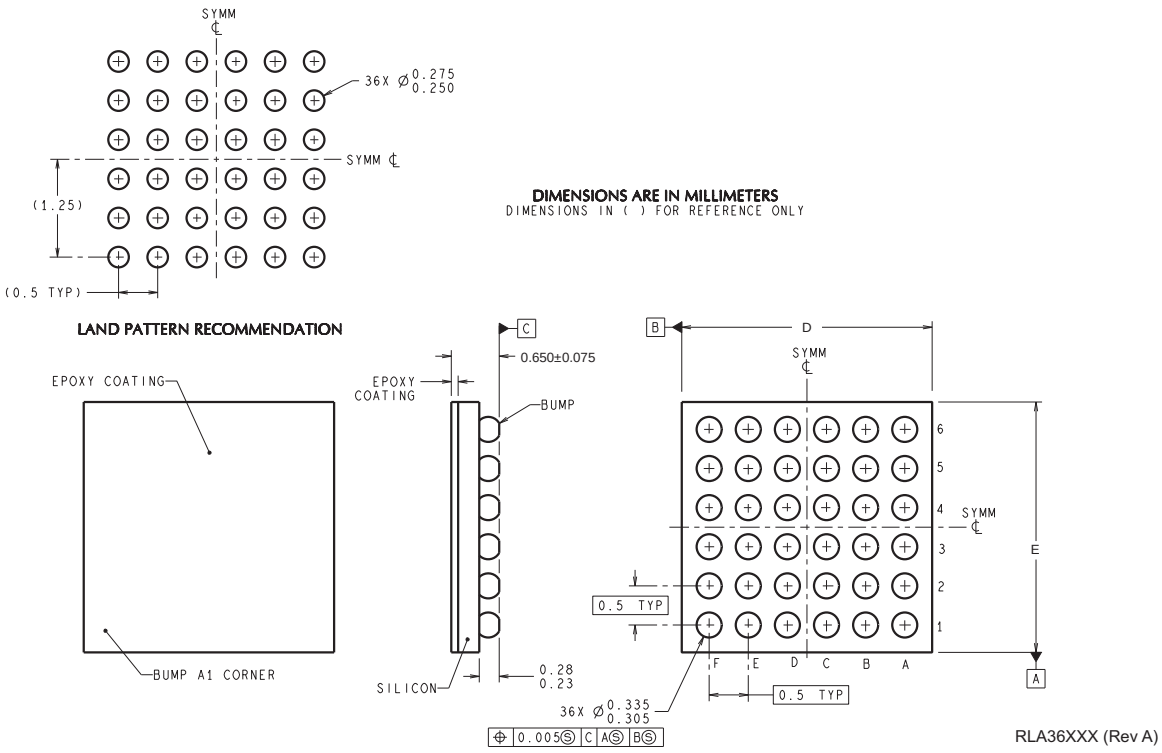
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV1088RL/NOPB	DSBGA	YPG	36	250	210.0	185.0	35.0
LMV1088RLX/NOPB	DSBGA	YPG	36	1000	210.0	185.0	35.0

YPG0036



D: Max = 3.494 mm, Min =3.434 mm

E: Max = 3.494 mm, Min =3.434 mm

4214895/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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