THE DATASHEET OF

LMP7701MF/NOPB

LMP770x Precision, CMOS Input, RRIO, Wide Supply Range Amplifiers

1 Features

- Unless Otherwise Noted, Typical Values at V_S = 5 V
- Input Offset Voltage (LMP7701): ±200-µV (Maximum)
- Input Offset Voltage (LMP7702/LMP7704): ±220-µV (Maximum)
- Input Bias Current: ±200 fA
- Input Bias Current: ±200 fA
- Input Voltage Noise: 9 nV/√Hz
- CMRR: 130 dB
- Open-Loop Gain: 130 dB
- Temperature Range: −40°C to 125°C
- Unity-Gain Bandwidth: 2.5 MHz
- Supply Current (LMP7701): 715 µA
- Supply Current (LMP7702): 1.5 mA
- Supply Current (LMP7704): 2.9 mA
- Supply Voltage Range: 2.7 V to 12 V
- Rail-to-Rail Input and Output

2 Applications

- High Impedance Sensor Interface
- Battery-Powered Instrumentation
- High Gain Amplifiers
- DAC Buffer
- Instrumentation Amplifier
- Active Filters

3 Description

The LMP770x are single, dual, and quad low-offset voltage, rail-to-rail input and output precision amplifiers, each with a CMOS input stage and a wide supply voltage range. The LMP770x are part of the LMP™ precision amplifier family and are ideal for sensor interface and other instrumentation applications.

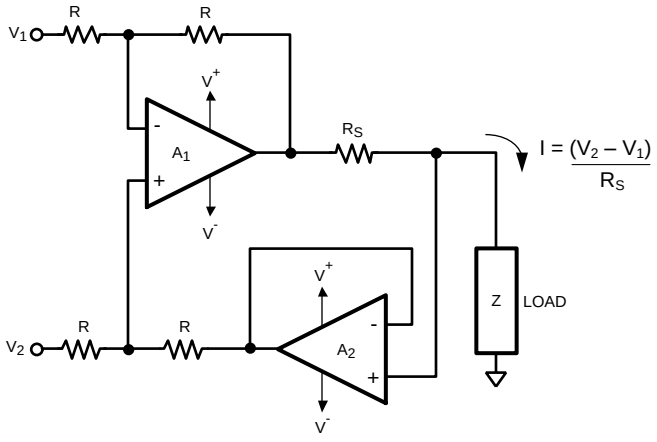
The specified low-offset voltage of less than ±200 µV, along with the specified low input bias current of less than ±1 pA, make the LMP7701 ideal for precision applications. The LMP770x are built using VIP50 technology, which allows the combination of a CMOS input stage and a 12-V common-mode and supply voltage range. This makes the LMP770x ideal for applications where conventional CMOS parts cannot operate under the desired voltage conditions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMP7701	SOT-23 (5)	1.60 mm × 2.90 mm
	SOIC (8)	3.91 mm × 4.90 mm
LMP7702	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	3.91 mm × 4.90 mm
LMP7704	TSSOP (14)	4.40 mm × 5.00 mm
	SOIC (14)	3.91 mm × 8.65 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (March 2013) to Revision I — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision G (March 2013) to Revision H — **Page**

- Changed layout of National Data Sheet to TI format ... 27

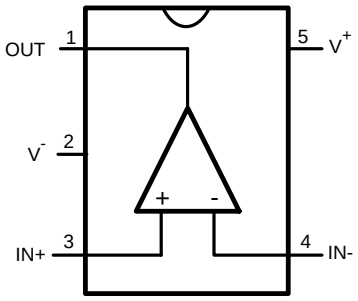
5 Description (continued)

The LMP770x each have a rail-to-rail input stage that significantly reduces the CMRR glitch commonly associated with rail-to-rail input amplifiers. This is achieved by trimming both sides of the complimentary input stage, thereby reducing the difference between the NMOS and PMOS offsets. The output of the LMP770x swings within 40 mV of either rail to maximize the signal dynamic range in applications requiring low supply voltage.

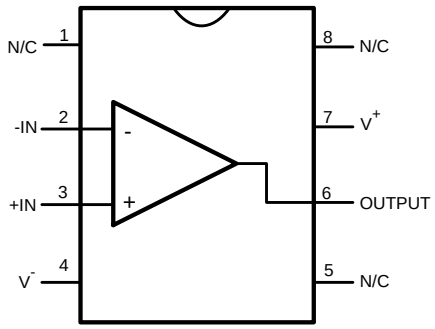
The LMP7701 is offered in the space-saving 5-Pin SOT-23 and 8-Pin SOIC package. The LMP7702 is offered in the 8-Pin SOIC and 8-Pin VSSOP package. The quad LMP7704 is offered in the 14-Pin SOIC and 14-Pin TSSOP package. These small packages are ideal solutions for area constrained PC boards and portable electronics.

6 Pin Configuration and Functions

LMP7701 DBV Package
5-Pin SOT-23
Top View



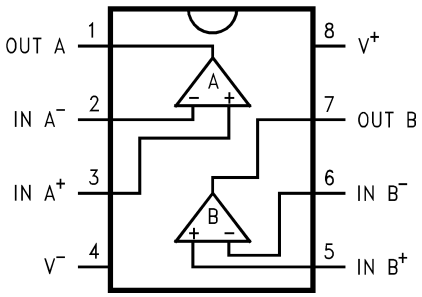
LMP7701 D Package
8-Pin SOIC
Top View



Pin Functions - LMP7701

PIN			I/O	DESCRIPTION
NAME	SOT-23	SOIC		
IN+	3	3	I	Noninverting Input
IN–	4	2	I	Inverting Input
IN A $^{+}$	—	—	I	Noninverting Input for Amplifier A
IN A^{-}	—	—	I	Inverting Input for Amplifier A
IN B^{+}	—	—	I	Noninverting Input for Amplifier B
IN B^{-}	—	—	I	Inverting Input for Amplifier B
IN C^{+}	—	—	I	Noninverting Input for Amplifier C
IN C^{-}	—	—	I	Inverting Input for Amplifier C
IN D^{+}	—	—	I	Noninverting Input for Amplifier D
IN D^{-}	—	—	I	Inverting Input for Amplifier D
NC	—	1, 5, 8	—	No connection
OUT	1	6	O	Output
OUT A	—	—	O	Output for Amplifier A
OUT B	—	—	O	Output for Amplifier B
OUT C	—	—	O	Output for Amplifier C
OUT D	—	—	O	Output for Amplifier D
V^{+}	5	7	P	Positive Supply
V^{-}	2	4	P	Negative Supply

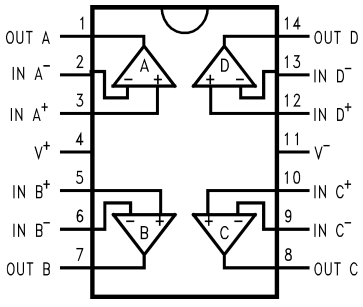
LMP7702 D or DGK Package
8-Pin SOIC or VSSOP
Top View



Pin Functions - LMP7702

PIN		I/O	DESCRIPTION
NAME	SOIC, VSSOP		
IN+	—	I	Noninverting Input
IN–	—	I	Inverting Input
IN A $^{+}$	3	I	Noninverting Input for Amplifier A
IN A^{-}	2	I	Inverting Input for Amplifier A
IN B^{+}	5	I	Noninverting Input for Amplifier B
IN B^{-}	6	I	Inverting Input for Amplifier B
IN C^{+}	—	I	Noninverting Input for Amplifier C
IN C^{-}	—	I	Inverting Input for Amplifier C
IN D^{+}	—	I	Noninverting Input for Amplifier D
IN D^{-}	—	I	Inverting Input for Amplifier D
NC	—	—	No connection
OUT	—	O	Output
OUT A	1	O	Output for Amplifier A
OUT B	7	O	Output for Amplifier B
OUT C	—	O	Output for Amplifier C
OUT D	—	O	Output for Amplifier D
V^{+}	8	P	Positive Supply
V^{-}	4	P	Negative Supply

LMP7704 D or PW Package
14-Pin SOIC or TSSOP
Top View



Pin Functions - LMP7704

PIN		I/O	DESCRIPTION
NAME	SOIC, TSSOP		
IN+	—	I	Noninverting Input
IN–	—	I	Inverting Input
IN A $^{+}$	3	I	Noninverting Input for Amplifier A
IN A^{-}	2	I	Inverting Input for Amplifier A
IN B^{+}	5	I	Noninverting Input for Amplifier B
IN B^{-}	6	I	Inverting Input for Amplifier B
IN C^{+}	10	I	Noninverting Input for Amplifier C
IN C^{-}	9	I	Inverting Input for Amplifier C
IN D^{+}	12	I	Noninverting Input for Amplifier D
IN D^{-}	13	I	Inverting Input for Amplifier D
NC	—	—	No connection
OUT	—	O	Output
OUT A	1	O	Output for Amplifier A
OUT B	7	O	Output for Amplifier B
OUT C	8	O	Output for Amplifier C
OUT D	14	O	Output for Amplifier D
V^{+}	4	P	Positive Supply
V^{-}	11	P	Negative Supply

7 Specifications

7.1 Absolute Maximum Ratings

See (1)(2)

		MIN	MAX	UNIT
V_{IN} differential			±300	mV
Supply voltage ($V_S = V^+ – V^-$)			13.2	V
Voltage at input/output pins			V^++ 0.3, V^- − 0.3	V
Input current			10	mA
Junction temperature (3)			+150	°C
Soldering information	Infrared or convection (20 sec)		235	°C
	Wave soldering lead temp. (10 sec)		260	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)	±1000	
		Machine Model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Temperature range (1)	−40		125	°C
Supply voltage ($V_S = V^+ – V^–$)	2.7		12	V

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

7.4 Thermal Information

THERMAL METRIC(1)		LMP7701	LMP7701, LMP7702	LMP7702	LMP7704		UNIT
		DBV (SOT-23)	D (SOIC)	DGK (VSSOP)	D (SOIC)	PW (TSSOP)	
		5 PINS	8 PINS	8 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	122.9	114.3	167.5	79.9	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.3	59.5	58.7	36.9	33.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.3	54.8	87.5	34.7	50.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.4	12.1	6.6	5.5	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.8	54.2	86.1	34.4	49.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

7.5 Electrical Characteristics 3-V

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 3 V, $V^–$ = 0 V, $V_{CM} = V^+/2$, and R_L > 10 kΩ to $V^+/2$.(1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
V_{OS}	Input Offset Voltage	LMP7701			±37	±200	µV
			at the temperature extremes			±500	
		LMP7702/LMP7704			±56	±220	
			at the temperature extremes			±520	
TCV_{OS}	Input Offset Voltage Temperature Drift	See (4)			±1		µV/°C
			at the temperature extremes			±5	
I_B	Input Bias Current	See (4) (5) −40°C ≤ T_A ≤ 85°C			±0.2	±1	pA
			at the temperature extremes			±50	
		See (4) (5) −40°C ≤ T_A ≤ 125°C			±0.2	±1	
			at the temperature extremes			±400	
I_{OS}	Input Offset Current				40		fA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) This parameter is specified by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.

Electrical Characteristics 3-V (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 3 V, V^- = 0 V, V_{CM} = V^+/2, and R_L > 10 kΩ to V^+/2.(1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
CMRR	Common-Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 3 V LMP7701		86	130		dB
			at the temperature extremes	80			
		0 V ≤ V_{CM} ≤ 3 V LMP7702/LMP7704		84	130		
			at the temperature extremes	78			
PSRR	Power Supply Rejection Ratio	2.7 V ≤ V^+ ≤ 12 V, Vo = V^+/2		86	98		dB
			at the temperature extremes	82			
CMVR	Common-Mode Voltage Range	CMRR ≥ 80 dB		–0.2		3.2	V
		CMRR ≥ 77 dB	at the temperature extremes	–0.2		3.2	
A_{VOL}	Open-Loop Voltage Gain	R_L = 2 kΩ (LMP7701) V_O = 0.3 V to 2.7 V		100	114		dB
			at the temperature extremes	96			
		R_L = 2 kΩ (LMP7702/LMP7704) V_O = 0.3 V to 2.7 V		100	114		
			at the temperature extremes	94			
		R_L = 10 kΩ V_O = 0.2 V to 2.8 V		100	124		
			at the temperature extremes	96			
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to V^+/2 LMP7701			40	80	mV from V^+
			at the temperature extremes			120	
		R_L = 2 kΩ to V^+/2 LMP7702/LMP7704			40	80	
			at the temperature extremes			150	
		R_L = 10 kΩ to V^+/2 LMP7701			30	40	
			at the temperature extremes			60	
		R_L = 10 kΩ to V^+/2 LMP7702/LMP7704			35	50	
			at the temperature extremes			100	
	Output Voltage Swing Low	R_L = 2 kΩ to V^+/2 LMP7701			40	60	mV
			at the temperature extremes			80	
		R_L = 2 kΩ to V^+/2 LMP7702/LMP7704			45	100	
			at the temperature extremes			170	
		R_L = 10 kΩ to V^+/2 LMP7701			20	40	
			at the temperature extremes			50	
		R_L = 10 kΩ to V^+/2 LMP7702/LMP7704			20	50	
			at the temperature extremes			90	

Electrical Characteristics 3-V (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 3 V, V^- = 0 V, V_{CM} = V^+/2, and R_L > 10 kΩ to V^+/2.(1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
I_{OUT}	Output Current (6) (7)	Sourcing V_O = V^+/2 V_{IN} = 100 mV		25	42		mA
			at the temperature extremes	15			
		Sinking V_O = V^+/2 V_{IN} = −100 mV (LMP7701)		25	42		
			at the temperature extremes	20			
		Sinking V_O = V^+/2 V_{IN} = −100 mV (LMP7702/LMP7704)		25	42		
			at the temperature extremes	15			
I_S	Supply Current	LMP7701			0.670	1	mA
			at the temperature extremes			1.2	
		LMP7702			1.4	1.8	
			at the temperature extremes			2.1	
		LMP7704			2.9	3.5	
			at the temperature extremes			4.5	
SR	Slew Rate (8)	A_V = +1, V_O = 2 V_{PP} 10% to 90%			0.9		V/µs
GBW	Gain Bandwidth				2.5		MHz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, $R._L$ = 10 kΩ			0.02%		
e_n	Input Referred Voltage Noise Density	f = 1 kHz			9		nV/√Hz
i_n	Input Referred Current Noise Density	f = 100 kHz			1		fA/√Hz

(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.
(7) The short circuit test is a momentary test.
(8) The number specified is the slower of positive and negative slew rates.

7.6 Electrical Characteristics 5-V

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2, and R_L > 10 kΩ to V^+/2.(1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
V_{OS}	Input Offset Voltage	LMP7701			±37	±200	µV
			at the temperature extremes			±500	
		LMP7702/LMP7704			±32	±220	
			at the temperature extremes			±520	
TCV_{OS}	Input Offset Voltage Temperature Drift	See (4)			±1	±5	µV/°C
			at the temperature extremes				
I_B	Input Bias Current	See (4) (5) −40°C ≤ T_A ≤ 85°C			±0.2	±1	pA
			at the temperature extremes			±50	
		See (4) (5) −40°C ≤ T_A ≤ 125°C			±0.2	±1	
			at the temperature extremes			±400	
I_{OS}	Input Offset Current				40		fA
CMRR	Common-Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 5 V LMP7701		88	130		dB
			at the temperature extremes	83			
		0 V ≤ V_{CM} ≤ 5 V LMP7702/LMP7704		86	130		
			at the temperature extremes	81			
PSRR	Power Supply Rejection Ratio	2.7 V ≤ V^+ ≤ 12 V, V_O = V^+/2		86	100		dB
			at the temperature extremes	82			
CMVR	Common-Mode Voltage Range	CMRR ≥ 80 dB		–0.2		5.2	V
		CMRR ≥ 78 dB	at the temperature extremes	–0.2		5.2	
A_{VOL}	Open-Loop Voltage Gain	R_L = 2 kΩ (LMP7701) V_O = 0.3 V to 4.7 V		100	119		dB
			at the temperature extremes	96			
		R_L = 2 kΩ (LMP7702/LMP7704) V_O = 0.3 V to 4.7 V		100	119		
			at the temperature extremes	94			
		R_L = 10 kΩ V_O = 0.2 V to 4.8 V		100	130		
			at the temperature extremes	96			

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) This parameter is specified by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.

Electrical Characteristics 5-V (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2, and R_L > 10 kΩ to V^+/2.(1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to V^+/2 LMP7701			60	110	mV from V^+
			at the temperature extremes			130	
		R_L = 2 kΩ to V^+/2 LMP7702/LMP7704			60	120	
			at the temperature extremes			200	
		R_L = 10 kΩ to V^+/2 LMP7701			40	50	
			at the temperature extremes			70	
		R_L = 10 kΩ to V^+/2 LMP7702/LMP7704			40	60	
			at the temperature extremes			120	
	Output Voltage Swing Low	R_L = 2 kΩ to V^+/2 LMP7701			50	80	mV
			at the temperature extremes			90	
		R_L = 2 kΩ to V^+/2 LMP7702/LMP7704			50	120	
			at the temperature extremes			190	
		R_L = 10 kΩ to V^+/2 LMP7701			30	40	
			at the temperature extremes			50	
		R_L = 10 kΩ to V^+/2 LMP7702/LMP7704			30	50	
			at the temperature extremes			100	
I_{OUT}	Output Current (6) (7)	Sourcing V_O = V^+/2 V_{IN} = 100 mV (LMP7701)		40	66		mA
			at the temperature extremes	28			
		Sourcing V_O = V^+/2 V_{IN} = 100 mV (LMP7702/LMP7704)		38	66		
			at the temperature extremes	25			
		Sinking V_O = V^+/2 V_{IN} = −100 mV (LMP7701)		40	76		
			at the temperature extremes	28			
		Sinking V_O = V^+/2 V_{IN} = −100 mV (LMP7702/LMP7704)		40	76		
			at the temperature extremes	23			
I_S	Supply Current	LMP7701			0.715	1	mA
			at the temperature extremes			1.2	
		LMP7702			1.5	1.9	
			at the temperature extremes			2.2	
		LMP7704			2.9	3.7	
			at the temperature extremes			4.6	
SR	Slew Rate (8)	A_V = +1, V_O = 4 V_{PP} 10% to 90%			1		V/µs
GBW	Gain Bandwidth				2.5		MHz

(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.
(7) The short circuit test is a momentary test.
(8) The number specified is the slower of positive and negative slew rates.

Electrical Characteristics 5-V (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2, and R_L > 10 kΩ to V^+/2.(1)

PARAMETER		TEST CONDITIONS	MIN (2)	TYP (3)	MAX (2)	UNIT
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 10 kΩ		0.02%		
e_n	Input Referred Voltage Noise Density	f = 1 kHz		9		nV/√Hz
i_n	Input Referred Current Noise Density	f = 100 kHz		1		fA/√Hz

7.7 Electrical Characteristics ±5-V

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5 V, V^- = −5 V, V_{CM} = 0 V, and R_L > 10 kΩ to 0 V.(1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
V_{OS}	Input Offset Voltage	LMP7701			±37	±200	µV
			at the temperature extremes			±500	
		LMP7702/LMP7704			±37	±220	
			at the temperature extremes			±520	
TCV_{OS}	Input Offset Voltage Temperature Drift	See (4)			±1		µV/°C
			at the temperature extremes			±5	
I_B	Input Bias Current	See (4) (5) −40°C ≤ T_A ≤ 85°C			±0.2	1	pA
			at the temperature extremes			±50	
		See (4) (5) −40°C ≤ T_A ≤ 125°C			±0.2	1	
			at the temperature extremes			±400	
I_{OS}	Input Offset Current				40		fA
CMRR	Common-Mode Rejection Ratio	−5 V ≤ V_{CM} ≤ 5 V LMP7701		92	138		dB
			at the temperature extremes	88			
		−5 V ≤ V_{CM} ≤ 5 V LMP7702/LMP7704		90	138		
			at the temperature extremes	86			
PSRR	Power Supply Rejection Ratio	2.7 V ≤ V^+ ≤ 12 V, V_O = 0 V		86	98		dB
			at the temperature extremes	82			
CMVR	Common-Mode Voltage Range	CMRR ≥ 80 dB		−5.2		5.2	V
		CMRR ≥ 78 dB	at the temperature extremes	−5.2		5.2	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) This parameter is specified by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.

Electrical Characteristics ±5-V (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5 V, V^- = −5 V, V_{CM} = 0 V, and R_L > 10 kΩ to 0 V.(1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
A_{VOL}	Open Loop Voltage Gain	R_L = 2 kΩ (LMP7701) V_O = −4.7 V to 4.7 V		100	121		dB
			at the temperature extremes	98			
		R_L = 2 kΩ (LMP7702/LMP7704) V_O = −4.7 V to 4.7 V		100	121		
			at the temperature extremes	94			
		R_L = 10 kΩ (LMP7701) V_O = −4.8 V to 4.8 V		100	134		
			at the temperature extremes	98			
		R_L = 10 kΩ (LMP7702/LMP7704) V_O = −4.8 V to 4.8 V		100	134		
			at the temperature extremes	97			
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to 0 V LMP7701			90	150	mV from V^+
			at the temperature extremes			170	
		R_L = 2 kΩ to 0 V LMP7702/LMP7704			90	180	
			at the temperature extremes			290	
		R_L = 10 kΩ to 0 V LMP7701			40	80	
			at the temperature extremes			100	
		R_L = 10 kΩ to 0 V LMP7702/LMP7704			40	80	
			at the temperature extremes			150	
	Output Voltage Swing Low	R_L = 2 kΩ to 0 V LMP7701			90	130	mV from V^-
			at the temperature extremes			150	
		R_L = 2 kΩ to 0 V LMP7702/LMP7704			90	180	
			at the temperature extremes			260	
		R_L = 10 kΩ to 0 V LMP7701			40	50	
			at the temperature extremes			60	
		R_L = 10 kΩ to 0 V LMP7702/LMP7704			40	60	
			at the temperature extremes			110	
I_{OUT}	Output Current (6) (7)	Sourcing V_O = 0 V V_{IN} = 100 mV (LMP7701)		50	86		mA
			at the temperature extremes	35			
		Sourcing V_O = 0 V V_{IN} = 100 mV (LMP7702/LMP7704)		48	86		
			at the temperature extremes	33			
		Sinking V_O = 0 V V_{IN} = −100 mV		50	84		
			at the temperature extremes	35			

(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.
(7) The short circuit test is a momentary test.

Electrical Characteristics ±5-V (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5 V, V^- = −5 V, V_{CM} = 0 V, and R_L > 10 kΩ to 0 V.(1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
I_S	Supply Current	LMP7701			0.790	1.1	mA
			at the temperature extremes			1.3	
		LMP7702			1.7	2.1	
			at the temperature extremes			2.5	
		LMP7704			3.2	4.2	
			at the temperature extremes			5	
SR	Slew Rate (8)	A_V = +1, V_O = 9 V_{PP} 10% to 90%			1.1		V/µs
GBW	Gain Bandwidth				2.5		MHz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 10 kΩ			0.02%		
e_n	Input Referred Voltage Noise Density	f = 1 kHz			9		nV/√Hz
i_n	Input Referred Current Noise Density	f = 100 kHz			1		fA/√Hz

(8) The number specified is the slower of positive and negative slew rates.

7.8 Typical Characteristics

T_A = 25°C, V_{CM} = V_S/2, R_L > 10 kΩ (unless otherwise noted)

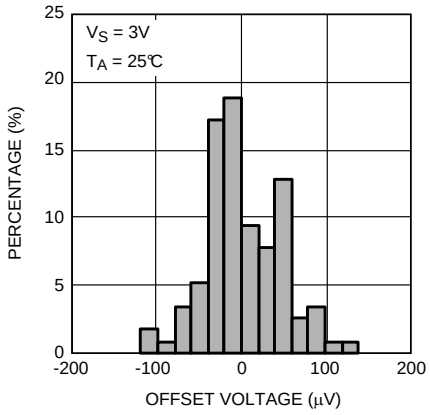


Figure 1. Figure 1. Offset Voltage Distribution

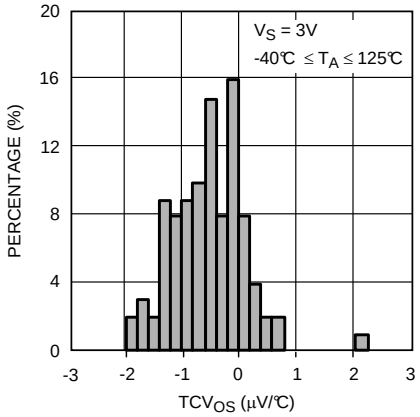


Figure 2. TCV_{OS} Distribution

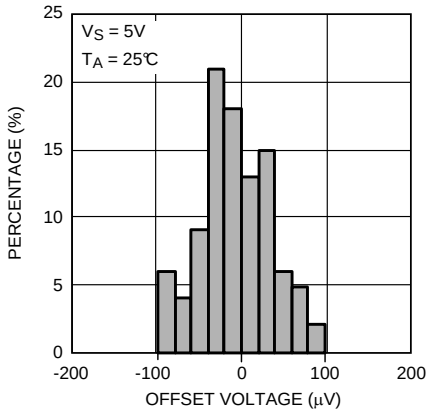


Figure 3. Offset Voltage Distribution

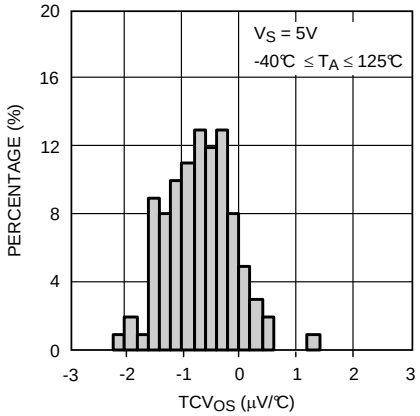


Figure 4. TCV_{OS} Distribution

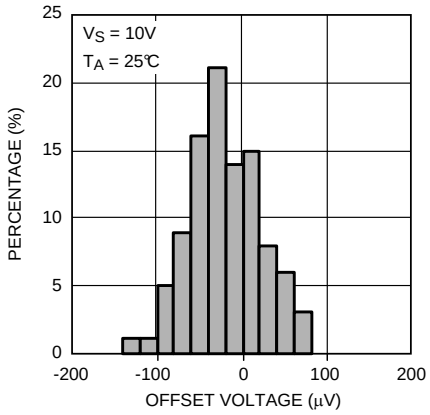


Figure 5. Offset Voltage Distribution

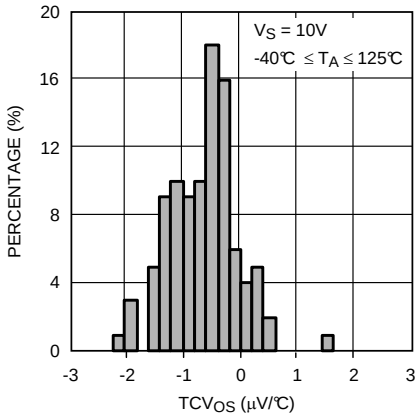


Figure 6. TCV_{OS} Distribution

Typical Characteristics (continued)

T_A = 25°C, V_{CM} = V_S/2, R_L > 10 kΩ (unless otherwise noted)

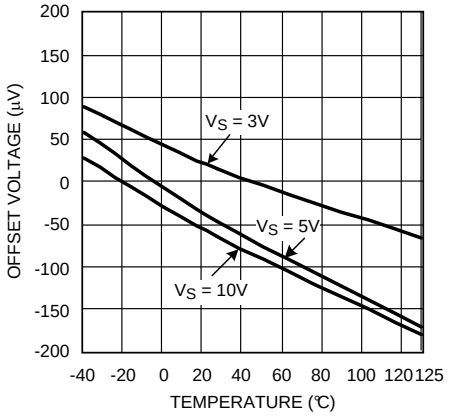


Figure 7. Offset Voltage vs Temperature

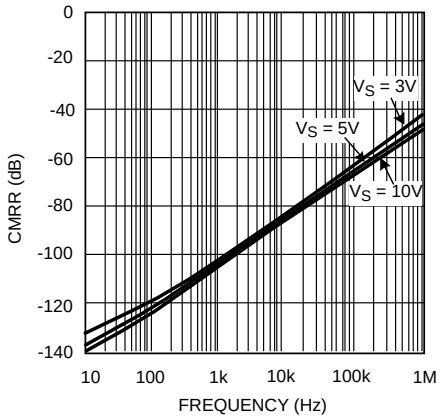


Figure 8. CMRR vs Frequency

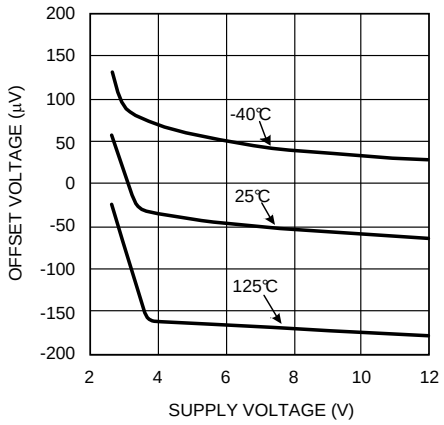


Figure 9. Offset Voltage vs Supply Voltage

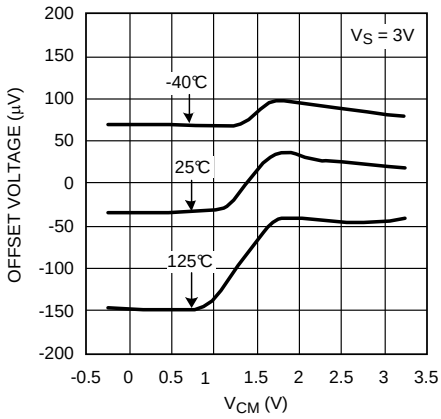


Figure 10. Offset Voltage vs V_{CM}

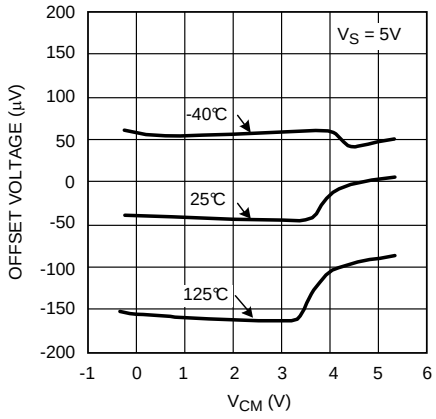


Figure 11. Offset Voltage vs V_{CM}

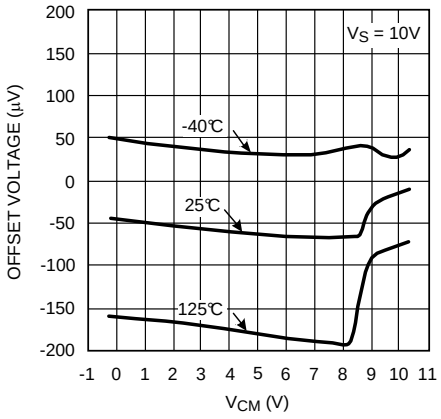


Figure 12. Offset Voltage vs V_{CM}

Typical Characteristics (continued)

T_A = 25°C, V_{CM} = V_S/2, R_L > 10 kΩ (unless otherwise noted)

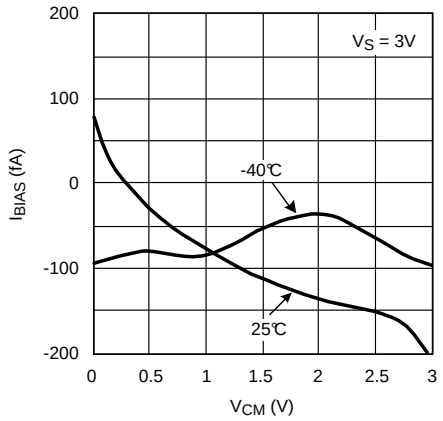


Figure 13. Input Bias Current vs V_{CM}

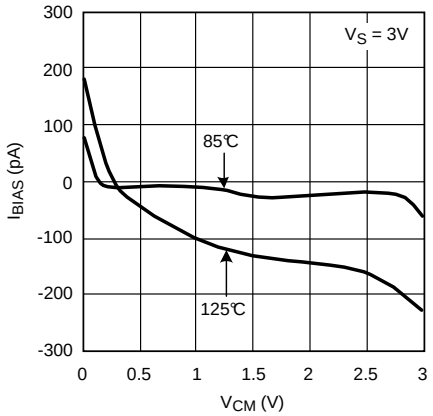


Figure 14. Input Bias Current vs V_{CM}

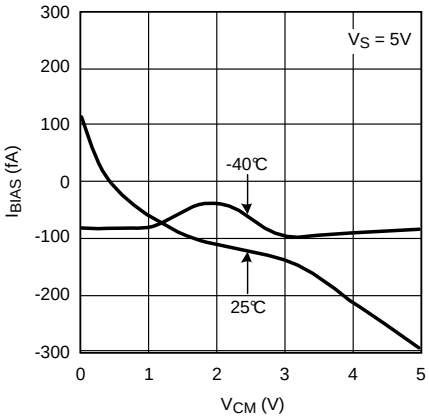


Figure 15. Input Bias Current vs V_{CM}

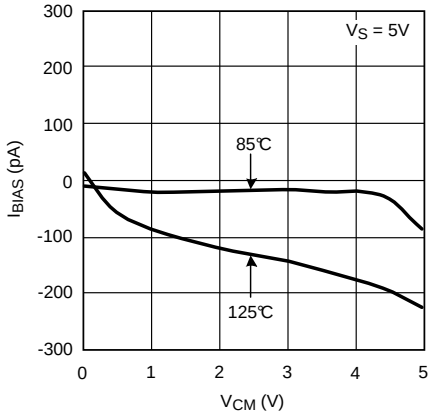


Figure 16. Input Bias Current vs V_{CM}

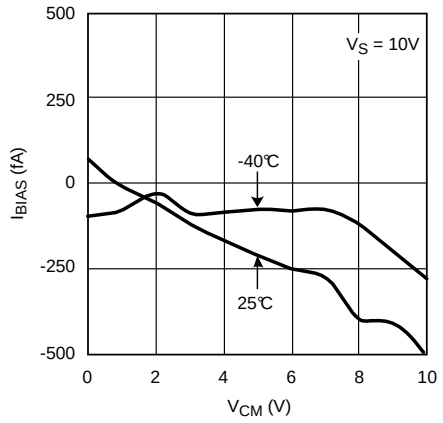


Figure 17. Input Bias Current vs V_{CM}

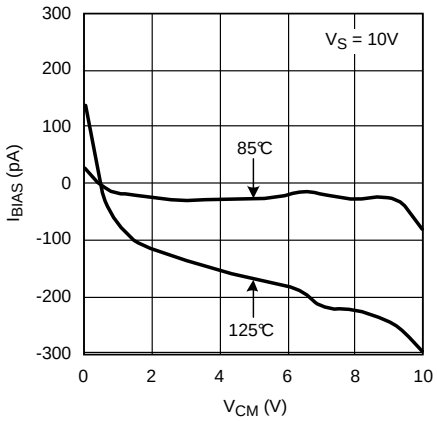


Figure 18. Input Bias Current vs V_{CM}

Typical Characteristics (continued)

T_A = 25°C, V_{CM} = V_S/2, R_L > 10 kΩ (unless otherwise noted)

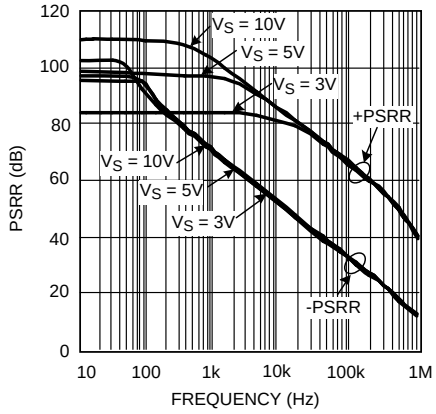


Figure 19. PSRR vs Frequency

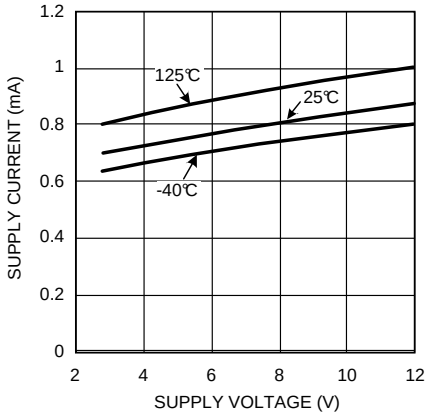


Figure 20. Supply Current vs Supply Voltage (Per Channel)

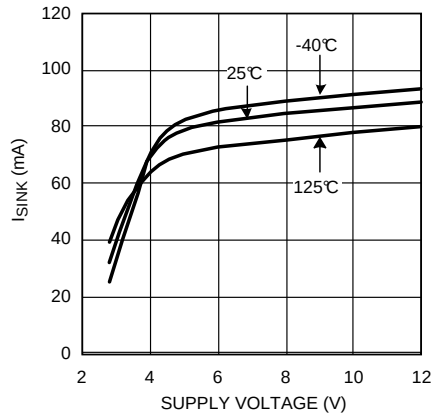


Figure 21. Sinking Current vs Supply Voltage

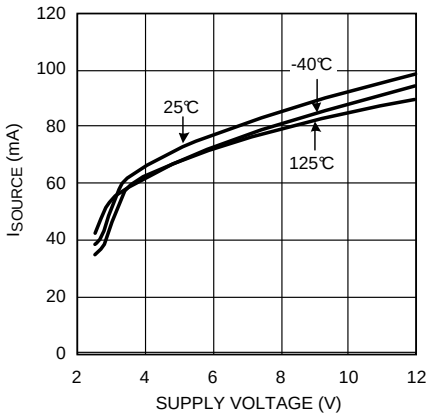


Figure 22. Sourcing Current vs Supply Voltage

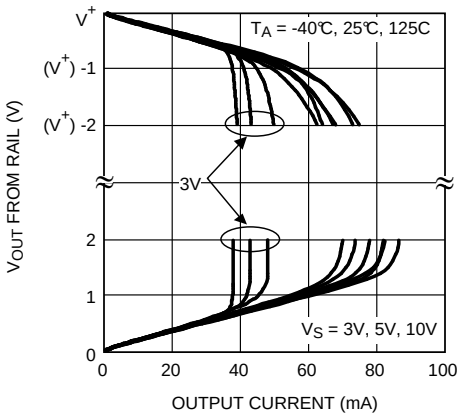


Figure 23. Output Voltage vs Output Current

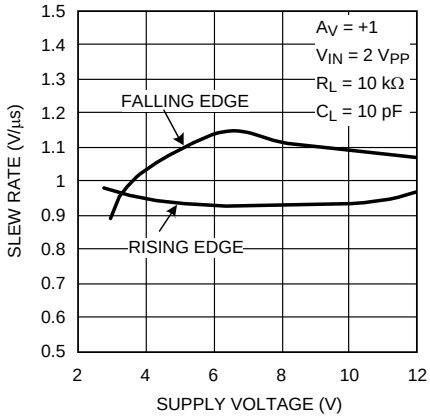


Figure 24. Slew Rate vs Supply Voltage

Typical Characteristics (continued)

T_A = 25°C, V_{CM} = V_S/2, R_L > 10 kΩ (unless otherwise noted)

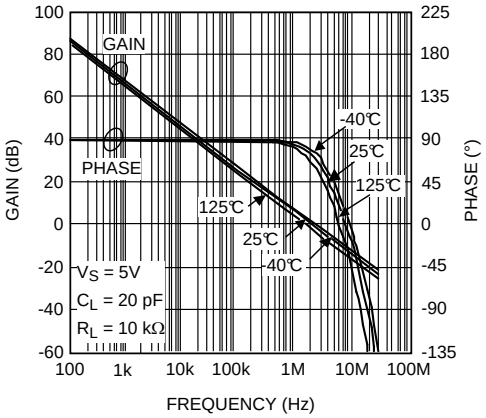


Figure 25. Open-Loop Frequency Response

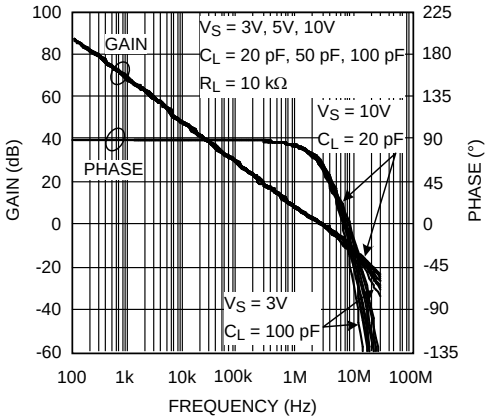


Figure 26. Open-Loop Frequency Response

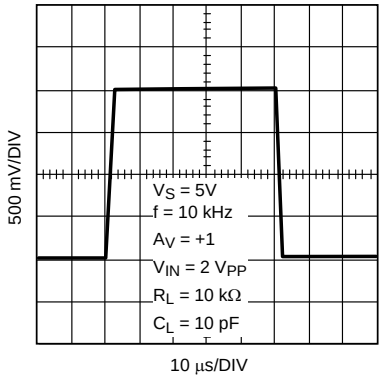


Figure 27. Large Signal Step Response

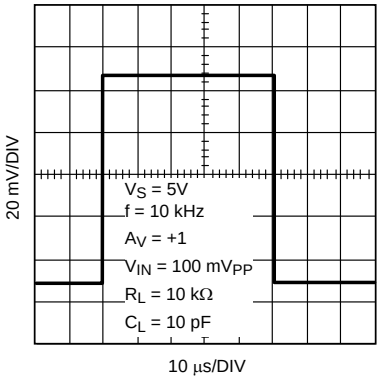


Figure 28. Small Signal Step Response

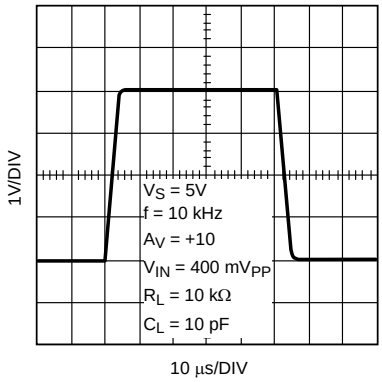


Figure 29. Large Signal Step Response

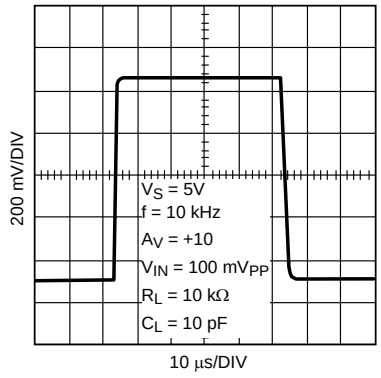


Figure 30. Small Signal Step Response

Typical Characteristics (continued)

T_A = 25°C, V_{CM} = V_S/2, R_L > 10 kΩ (unless otherwise noted)

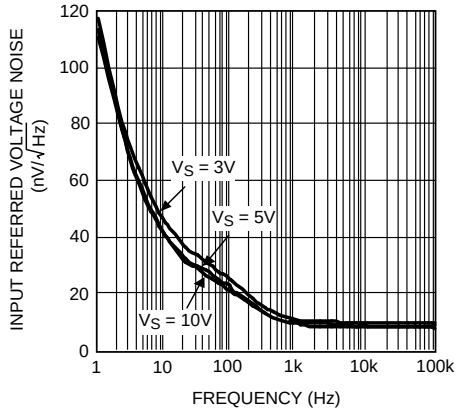


Figure 31. Input Voltage Noise vs Frequency

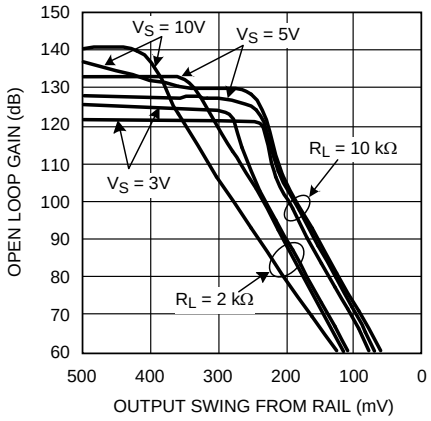


Figure 32. Open Loop Gain vs Output Voltage Swing

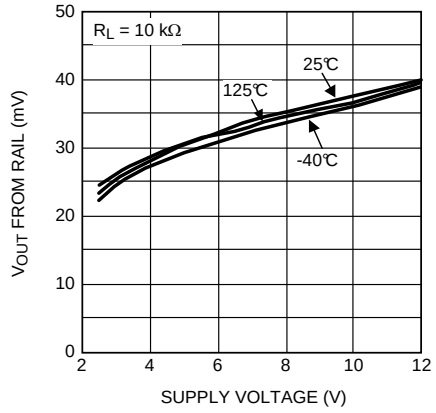


Figure 33. Output Swing High vs Supply Voltage

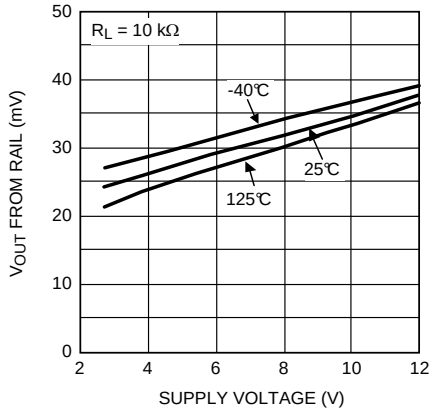


Figure 34. Output Swing Low vs Supply Voltage

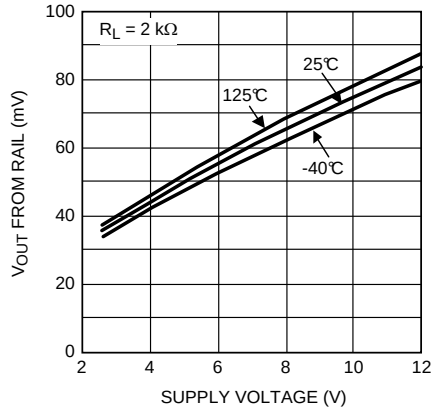


Figure 35. Output Swing High vs Supply Voltage

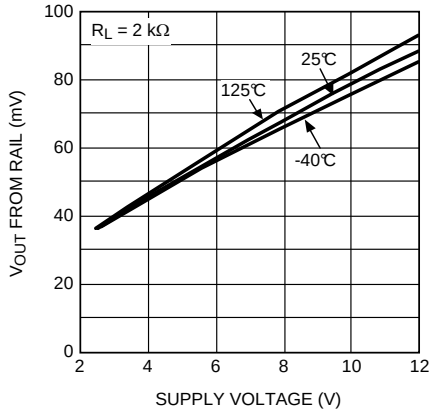


Figure 36. Output Swing Low vs Supply Voltage

Typical Characteristics (continued)

T_A = 25°C, V_{CM} = V_S/2, R_L > 10 kΩ (unless otherwise noted)

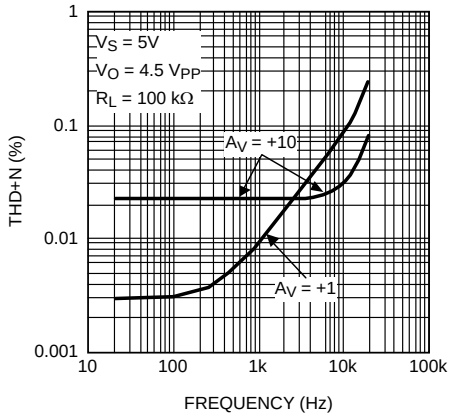


Figure 37. THD+N vs Frequency

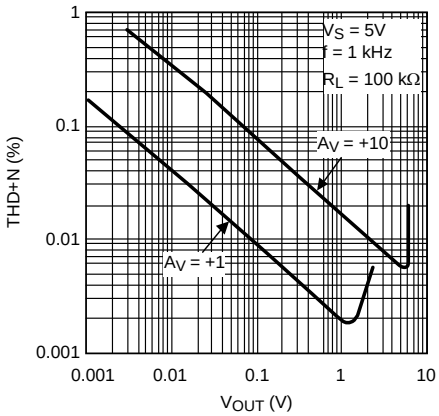


Figure 38. THD+N vs Output Voltage

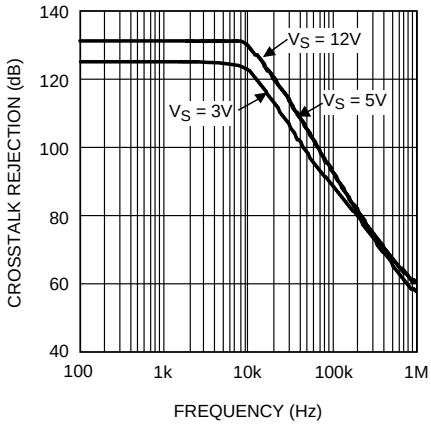


Figure 39. Crosstalk Rejection Ratio vs Frequency (LMP7702/LMP7704)

8 Detailed Description

8.1 Overview

The LMP770x are single, dual, and quad low offset voltage, rail-to-rail input and output precision amplifiers each with a CMOS input stage and wide supply voltage range of 2.7V to 12V. The LMP770x have a very low input bias current of only ±200 fA at room temperature.

The wide supply voltage range of 2.7V to 12V over the extensive temperature range of −40°C to 125°C makes the LMP770x excellent choices for low voltage precision applications with extensive temperature requirements.

The LMP770x have only ±37 µV of typical input referred offset voltage and this offset is specified to be less than ±500 µV for the single and ±520 µV for the dual and quad, over temperature. This minimal offset voltage allows more accurate signal detection and amplification in precision applications.

The low input bias current of only ±200 fA along with the low input referred voltage noise of 9 nV/$\sqrt{\text{Hz}}$ gives the LMP770x superiority for use in sensor applications. Lower levels of noise from the LMP770x mean of better signal fidelity and a higher signal-to-noise ratio.

Texas Instruments is heavily committed to precision amplifiers and the market segment they serve. Technical support and extensive characterization data is available for sensitive applications or applications with a constrained error budget.

The LMP7701 is offered in the space saving 5-Pin SOT-23 and 8-Pin SOIC package. The LMP7702 comes in the 8-Pin SOIC and 8-Pin VSSOP package. The LMP7704 is offered in the 14-Pin SOIC and 14-Pin TSSOP package. These small packages are ideal solutions for area constrained PC boards and portable electronics.

8.2 Functional Block Diagram

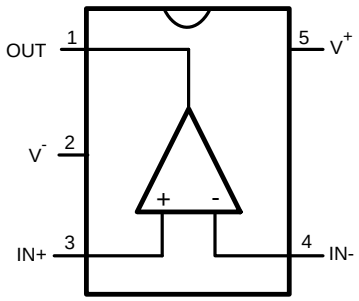


Figure 40. Functional Block Diagram (LMP7701)

8.3 Feature Description

8.3.1 Capacitive Load

The LMP770x can each be connected as a non-inverting unity gain follower. This configuration is the most sensitive to capacitive loading.

The combination of a capacitive load placed on the output of an amplifier along with the amplifier's output impedance creates a phase lag which in turn reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be either underdamped or it will oscillate.

To drive heavier capacitive loads, an isolation resistor, R_{ISO}, in Figure 41 should be used. By using this isolation resistor, the capacitive load is isolated from the amplifier's output, and hence, the pole caused by C_L is no longer in the feedback loop. The larger the value of R_{ISO}, the more stable the output voltage will be. If values of R_{ISO} are sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

Feature Description (continued)

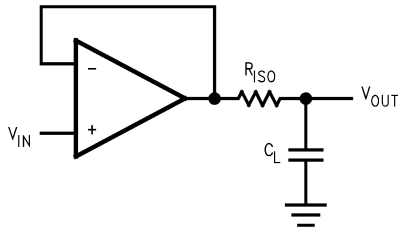
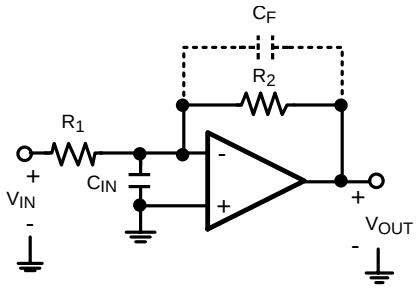


Figure 41. Isolating Capacitive Load

8.3.2 Input Capacitance

CMOS input stages inherently have low input bias current and higher input referred voltage noise. The LMP770x enhance this performance by having the low input bias current of only ±200 fA, as well as, a very low input referred voltage noise of 9 nV/√Hz. To achieve this a larger input stage has been used. This larger input stage increases the input capacitance of the LMP770x. The typical value of this input capacitance, C_{IN}, for the LMP770x is 25 pF. The input capacitance will interact with other impedances such as gain and feedback resistors, which are seen on the inputs of the amplifier, to form a pole. This pole will have little or no effect on the output of the amplifier at low frequencies and DC conditions, but will play a bigger role as the frequency increases. At higher frequencies, the presence of this pole will decrease phase margin and will also cause gain peaking. To compensate for the input capacitance, care must be taken in choosing the feedback resistors. In addition to being selective in picking values for the feedback resistor, a capacitor can be added to the feedback path to increase stability.

The DC gain of the circuit shown in Figure 42 is simply $-R_2/R_1$.



$$A_V = - \frac{V_{OUT}}{V_{IN}} = - \frac{R_2}{R_1}$$

Figure 42. Compensating for Input Capacitance

For the time being, ignore C_F. The AC gain of the circuit in Figure 42 can be calculated as follows:

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{\left[1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN} R_2}\right)}\right]} \quad (1)$$

This equation is rearranged to find the location of the two poles:

$$P_{1,2} = \frac{-1}{2C_{IN}} \left[\frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4 A_0 C_{IN}}{R_2}}\right] \quad (2)$$

Feature Description (continued)

As shown in Equation 2, as values of R_1 and R_2 are increased, the magnitude of the poles is reduced, which in turn decreases the bandwidth of the amplifier. Whenever possible, it is best to choose smaller feedback resistors. Figure 43 shows the effect of the feedback resistor on the bandwidth of the LMP770x.

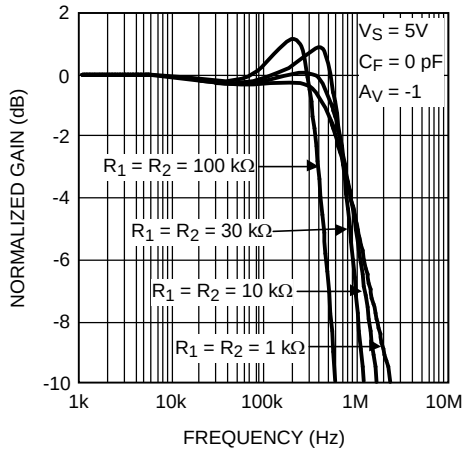


Figure 43. Closed-Loop Gain vs Frequency

Equation 2 has two poles. In most cases, it is the presence of pairs of poles that causes gain peaking. To eliminate this effect, the poles should be placed in Butterworth position, because poles in Butterworth position do not cause gain peaking. To achieve a Butterworth pair, the quantity under the square root in Equation 2 should be set to equal −1. Using this fact and the relation between R_1 and R_2, $R_2 = -A_V R_1$, the optimum value for R_1 can be found. This is shown in Equation 3. If R_1 is chosen to be larger than this optimum value, gain peaking will occur.

$$R_1 < \frac{(1 - A_V)^2}{2A_0A_VC_{IN}} \tag{3}$$

In Figure 42, C_F is added to compensate for input capacitance and to increase stability. Additionally, C_F reduces or eliminates the gain peaking that can be caused by having a larger feedback resistor. Figure 44 shows how C_F reduces gain peaking.

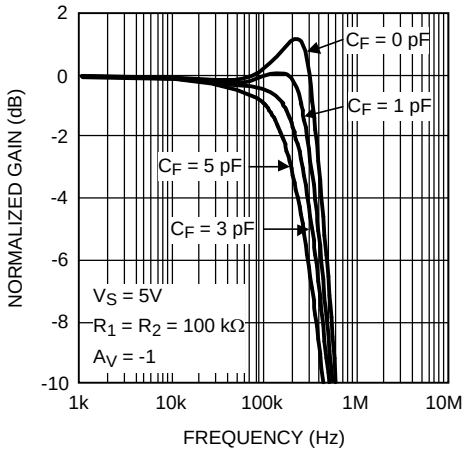


Figure 44. Closed-Loop Gain vs Frequency With Compensation

Feature Description (continued)

8.3.3 Diodes Between the Inputs

The LMP770x have a set of anti-parallel diodes between the input pins, as shown in Figure 45. These diodes are present to protect the input stage of the amplifier. At the same time, they limit the amount of differential input voltage that is allowed on the input pins. A differential signal larger than one diode voltage drop might damage the diodes. The differential signal between the inputs needs to be limited to ±300 mV or the input current needs to be limited to ±10 mA.

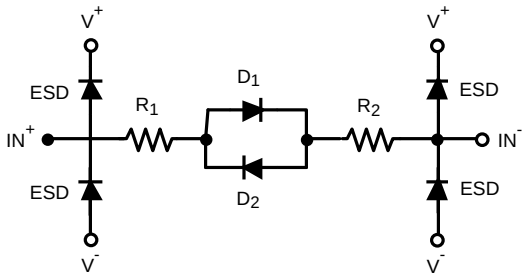


Figure 45. Input of LMP7701

8.4 Device Functional Modes

8.4.1 Precision Current Source

The LMP770x can each be used as a precision current source in many different applications. Figure 46 shows a typical precision current source. This circuit implements a precision voltage controlled current source. Amplifier A1 is a differential amplifier that uses the voltage drop across R_S as the feedback signal. Amplifier A2 is a buffer that eliminates the error current from the load side of the R_S resistor that would flow in the feedback resistor if it were connected to the load side of the R_S resistor. In general, the circuit is stable as long as the closed loop bandwidth of amplifier A2 is greater then the closed loop bandwidth of amplifier A1. If A1 and A2 are the same type of amplifiers, then the feedback around A1 will reduce its bandwidth compared to A2.

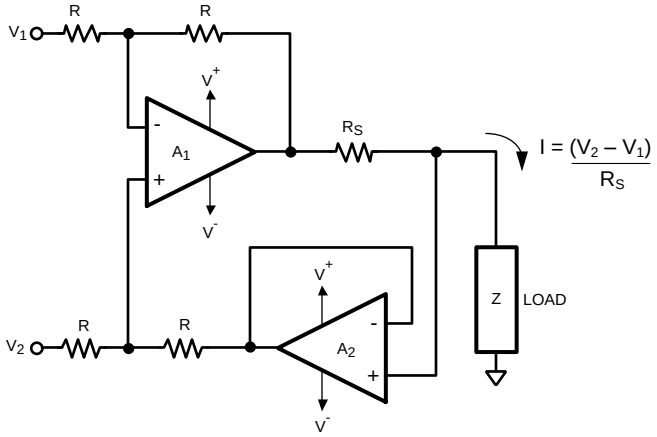


Figure 46. Precision Current Source

The equation for output current can be derived as shown in Equation 4.

$$\frac{V_2R}{R+R} + \frac{(V_0 - IR_S)R}{R+R} = \frac{V_1R}{R+R} + \frac{V_0R}{R+R} \tag{4}$$

Solving for the current I results in the Equation 5.

$$I = \frac{V_2 - V_1}{R_S} \tag{5}$$

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Low Input Voltage Noise

The LMP770x have the very low input voltage noise of 9 nV/$\sqrt{Hz}$. This input voltage noise can be further reduced by placing N amplifiers in parallel as shown in Figure 47. The total voltage noise on the output of this circuit is divided by the square root of the number of amplifiers used in this parallel combination. This is because each individual amplifier acts as an independent noise source, and the average noise of independent sources is the quadrature sum of the independent sources divided by the number of sources. For N identical amplifiers, this means:

Application Information (continued)

$$\text{REDUCED INPUT VOLTAGE NOISE} = \frac{1}{N}\sqrt{e_{n1}^2+e_{n2}^2+\cdots\cdots+e_{nN}^2}$$

$$= \frac{1}{N}\sqrt{Ne_n^2} = \frac{\sqrt{N}}{N}\ e_n$$

$$= \frac{1}{\sqrt{N}}\ e_n \tag{6}$$

Figure 47 shows a schematic of this input voltage noise reduction circuit. Typical resistor values are:

R_G = 10Ω, R_F = 1 kΩ, and R_O = 1 kΩ.

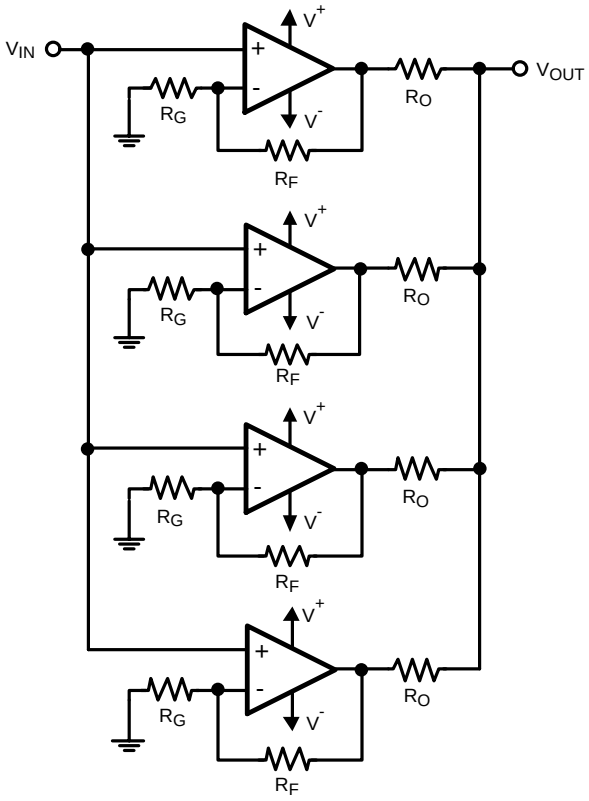


Figure 47. Noise Reduction Circuit

9.1.2 Total Noise Contribution

The LMP770x have very low input bias current, very low input current noise, and very low input voltage noise. As a result, these amplifiers are ideal choices for circuits with high impedance sensor applications.

Figure 48 shows the typical input noise of the LMP770x as a function of source resistance where:

e_n denotes the input referred voltage noise

e_i is the voltage drop across source resistance due to input referred current noise or $e_i = R_S * i_n$

e_t shows the thermal noise of the source resistance

e_{ni} shows the total noise on the input.

Where:

$$e_{ni} = \sqrt{e_n^2 + e_i^2 + e_t^2}$$

Application Information (continued)

The input current noise of the LMP770x is so low that it will not become the dominant factor in the total noise unless source resistance exceeds 300 MΩ, which is an unrealistically high value.

As is evident in Figure 48, at lower R_S values, total noise is dominated by the amplifier's input voltage noise. Once R_S is larger than a few kilo-Ohms, then the dominant noise factor becomes the thermal noise of R_S. As mentioned before, the current noise will not be the dominant noise factor for any practical application.

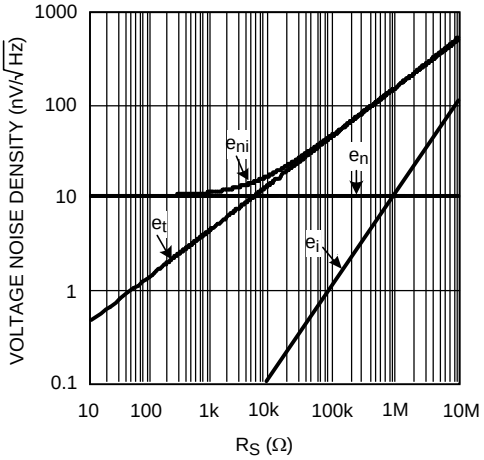


Figure 48. Total Input Noise

9.2 Typical Application

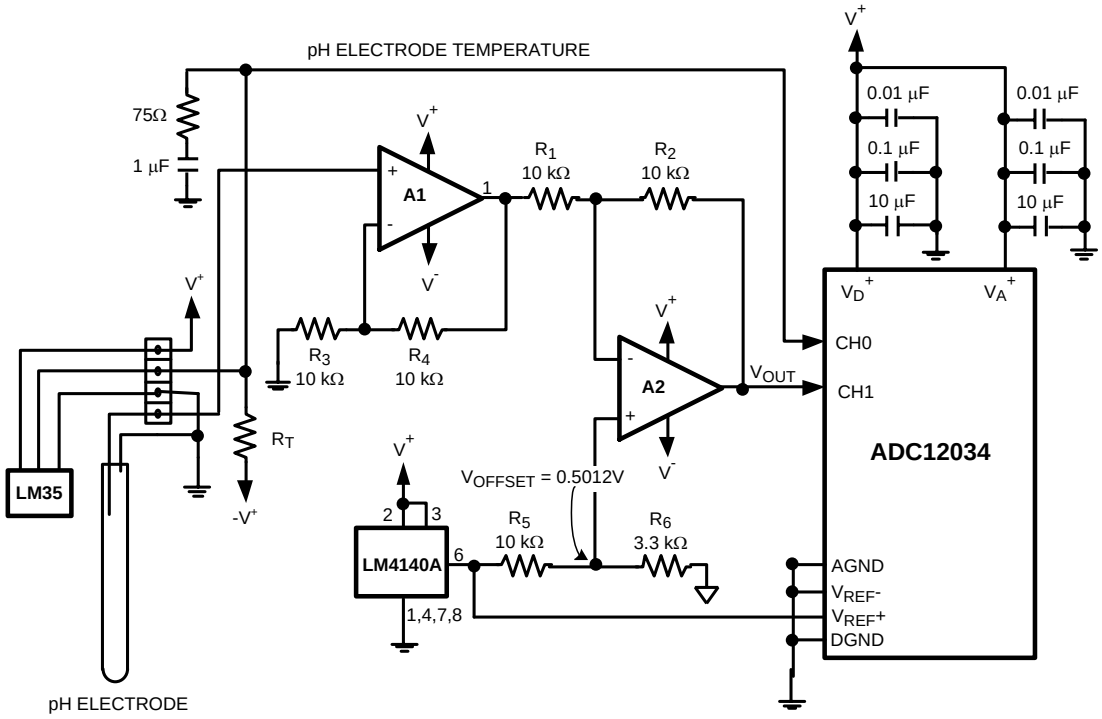


Figure 49. pH Measurement Circuit

Typical Application (continued)

9.2.1 Design Requirements

pH electrodes are very high impedance sensors. As their name indicates, they are used to measure the pH of a solution. They usually do this by generating an output voltage which is proportional to the pH of the solution. pH electrodes are calibrated so that they have zero output for a neutral solution, pH = 7, and positive and negative voltages for acidic or alkaline solutions. This means that the output of a pH electrode is bipolar and must be level shifted to be used in a single supply system. The rate of change of this voltage is usually shown in mV/pH and is different for different pH sensors. Temperature is also an important factor in a pH electrode reading. The output voltage of the senor will change with temperature.

9.2.2 Detailed Design Procedure

Many sensors have high source impedances that may range up to 10 MΩ. The output signal of sensors often needs to be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor's output and cause a voltage drop across the source resistance as shown in Figure 50, where $V_{IN}^+ = V_S - I_{BIAS}*R_S$

The last term, $I_{BIAS}*R_S$, shows the voltage drop across R_S. To prevent errors introduced to the system due to this voltage, an op amp with very low input bias current must be used with high impedance sensors. This is to keep the error contribution by $I_{BIAS}*R_S$ less than the input voltage noise of the amplifier, so that it will not become the dominant noise factor.

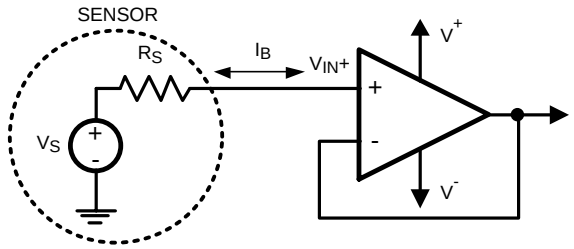


Figure 50. Noise Due to I_{BIAS}

Figure 51 shows a typical output voltage spectrum of a pH electrode. The exact values of output voltage will be different for different sensors. In this example, the pH electrode has an output voltage of 59.15 mV/pH at 25°C.

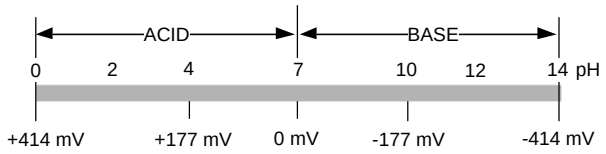


Figure 51. Output Voltage of a pH Electrode

The temperature dependence of a typical pH electrode is shown in Figure 52. As is evident, the output voltage changes with changes in temperature.

The schematic shown in Figure 49 is a typical circuit which can be used for pH measurement. The LM35 is a precision integrated circuit temperature sensor. This sensor is differentiated from similar products because it has an output voltage linearly proportional to Celcius measurement, without converting the temperature to Kelvin. The LM35 is used to measure the temperature of the solution and feeds this reading to the Analog to Digital Converter, ADC. This information is used by the ADC to calculate the temperature effects on the pH readings. The LM35 needs to have a resistor, R_T in Figure 49, to $-V^+$ to be able to read temperatures less than 0°C. R_T is not needed if temperatures are not expected to be less than zero.

Typical Application (continued)

The output of pH electrodes is usually large enough that it does not require much amplification; however, due to the very high impedance, the output of a pH electrode needs to be buffered before it can go to an ADC. Because most ADCs are operated on single supply, the output of the pH electrode also needs to be level shifted. Amplifier A1 buffers the output of the pH electrode with a moderate gain of +2, while A2 provides the level shifting. V_{OUT} at the output of A2 is given by: $V_{OUT} = -2V_{pH} + 1.024V$.

The LM4140A is a precision, low noise, voltage reference used to provide the level shift needed. The ADC used in this application is the ADC12032 which is a 12-bit, 2 channel converter with multiplexers on the inputs and a serial output. The 12-bit ADC enables users to measure pH with an accuracy of 0.003 of a pH unit. Adequate power supply bypassing and grounding is extremely important for ADCs. Recommended bypass capacitors are shown in Figure 49. It is common to share power supplies between different components in a circuit. To minimize the effects of power supply ripples caused by other components, the op amps must have bypass capacitors on the supply pins. Using the same value capacitors as those used with the ADC are ideal. The combination of these three values of capacitors ensures that AC noise present on the power supply line is grounded and does not interfere with the amplifiers' signal.

9.2.3 Application Curves

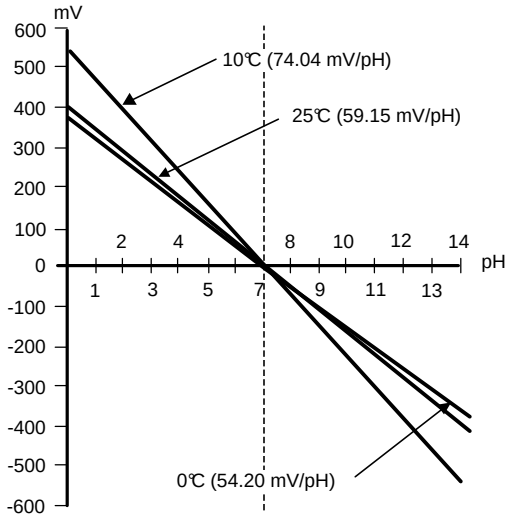


Figure 52. Temperature Dependence of a pH Electrode

10 Power Supply Recommendations

For proper operation, the power supplies must be decoupled. For supply decoupling, TI recommends placing 10-nF to 1-µF capacitors as close as possible to the operational-amplifier power supply pins. For single supply configurations, place a capacitor between the V^+ and V^- supply pins. For dual supply configurations, place one capacitor between V^+ and ground, and place a second capacitor between V^- and ground. Bypass capacitors must have a low ESR of less than 0.1 Ω.

11 Layout

11.1 Layout Guidelines

Take care to minimize the loop area formed by the bypass capacitor connection between supply pins and ground. A ground plane underneath the device is recommended; any bypass components to ground should have a nearby via to the ground plane. The optimum bypass capacitor placement is closest to the corresponding supply pin. Use of thicker traces from the bypass capacitors to the corresponding supply pins will lower the power supply inductance and provide a more stable power supply.

The feedback components should be placed as close to the device as possible to minimize stray parasitics.

11.2 Layout Example

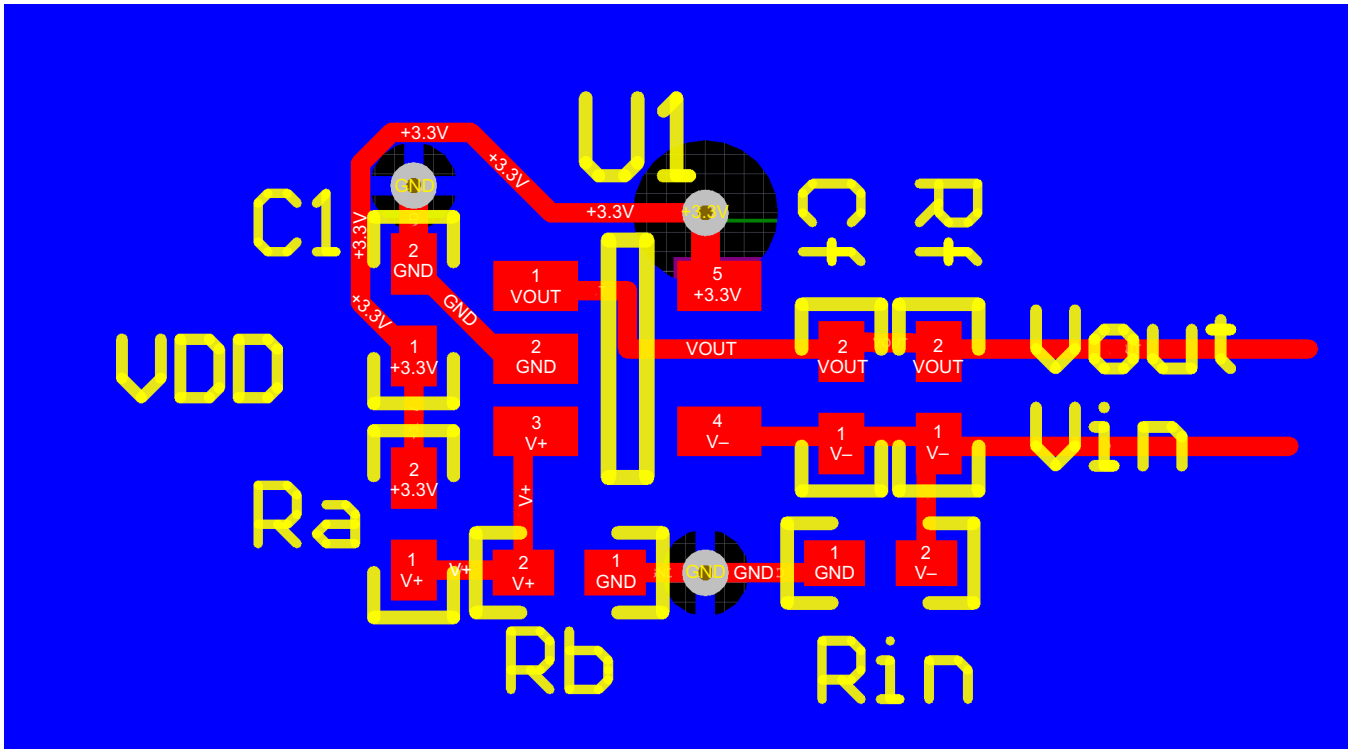


Figure 53. LMP7701 Example Layout

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE AND BUY	TECHNICAL DOCUMENTS	TOOLS AND SOFTWARE	SUPPORT AND COMMUNITY
LMP7701	Click here	Click here	Click here	Click here	Click here
LMP7702	Click here	Click here	Click here	Click here	Click here
LMP7704	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

LMP, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP7701MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMP77 01MA	Samples
LMP7701MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMP77 01MA	Samples
LMP7701MF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	AC2A	
LMP7701MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AC2A	Samples
LMP7701MFX	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	AC2A	
LMP7701MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AC2A	Samples
LMP7702MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMP77 02MA	Samples
LMP7702MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMP77 02MA	Samples
LMP7702MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	AA3A	
LMP7702MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AA3A	Samples
LMP7702MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AA3A	Samples
LMP7704MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMP7704 MA	Samples
LMP7704MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMP7704 MA	Samples
LMP7704MT	NRND	TSSOP	PW	14	94	TBD	Call TI	Call TI	-40 to 125	LMP77 04MT	
LMP7704MT/NOPB	ACTIVE	TSSOP	PW	14	94	Pb-Free (RoHS)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP77 04MT	Samples
LMP7704MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Pb-Free (RoHS)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP77 04MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

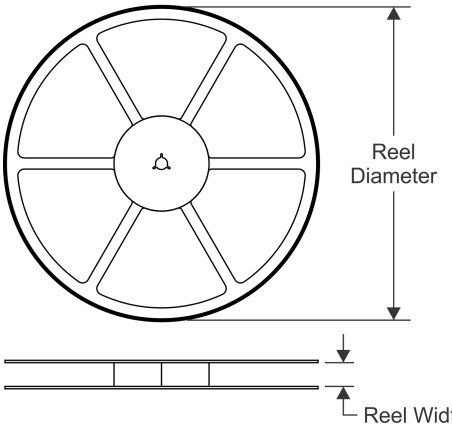
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

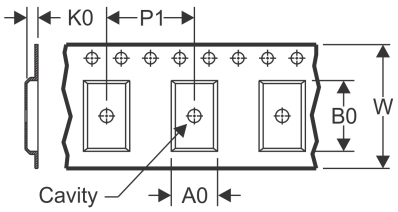
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

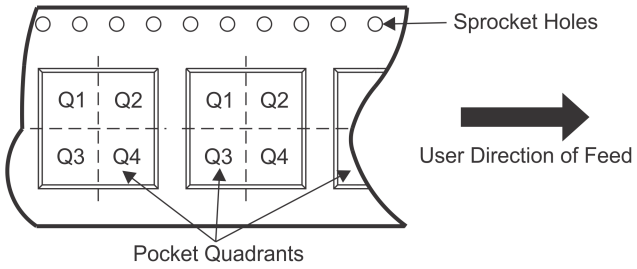


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

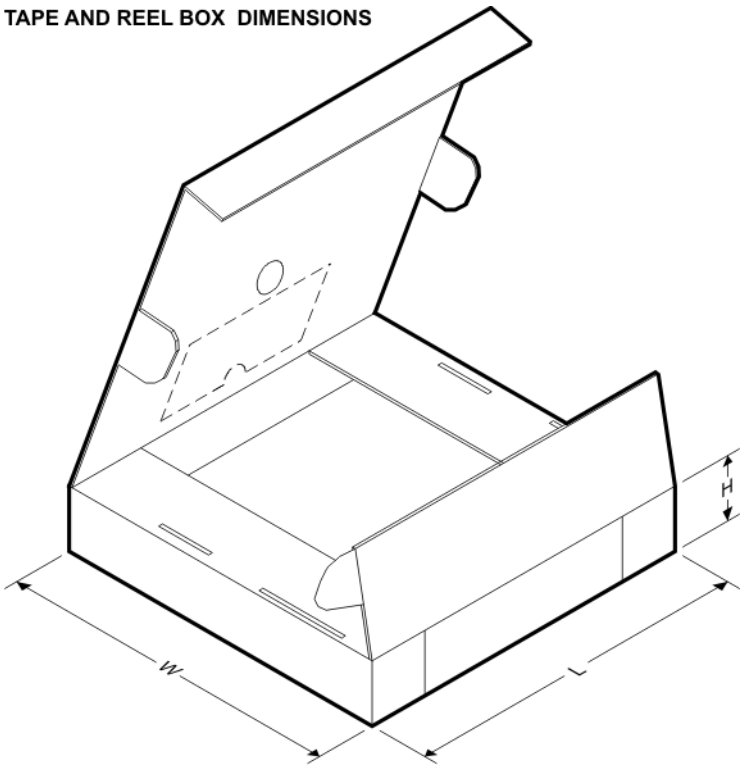
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP7701MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP7701MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7701MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7701MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7701MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7702MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP7702MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7702MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7702MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7704MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMP7704MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

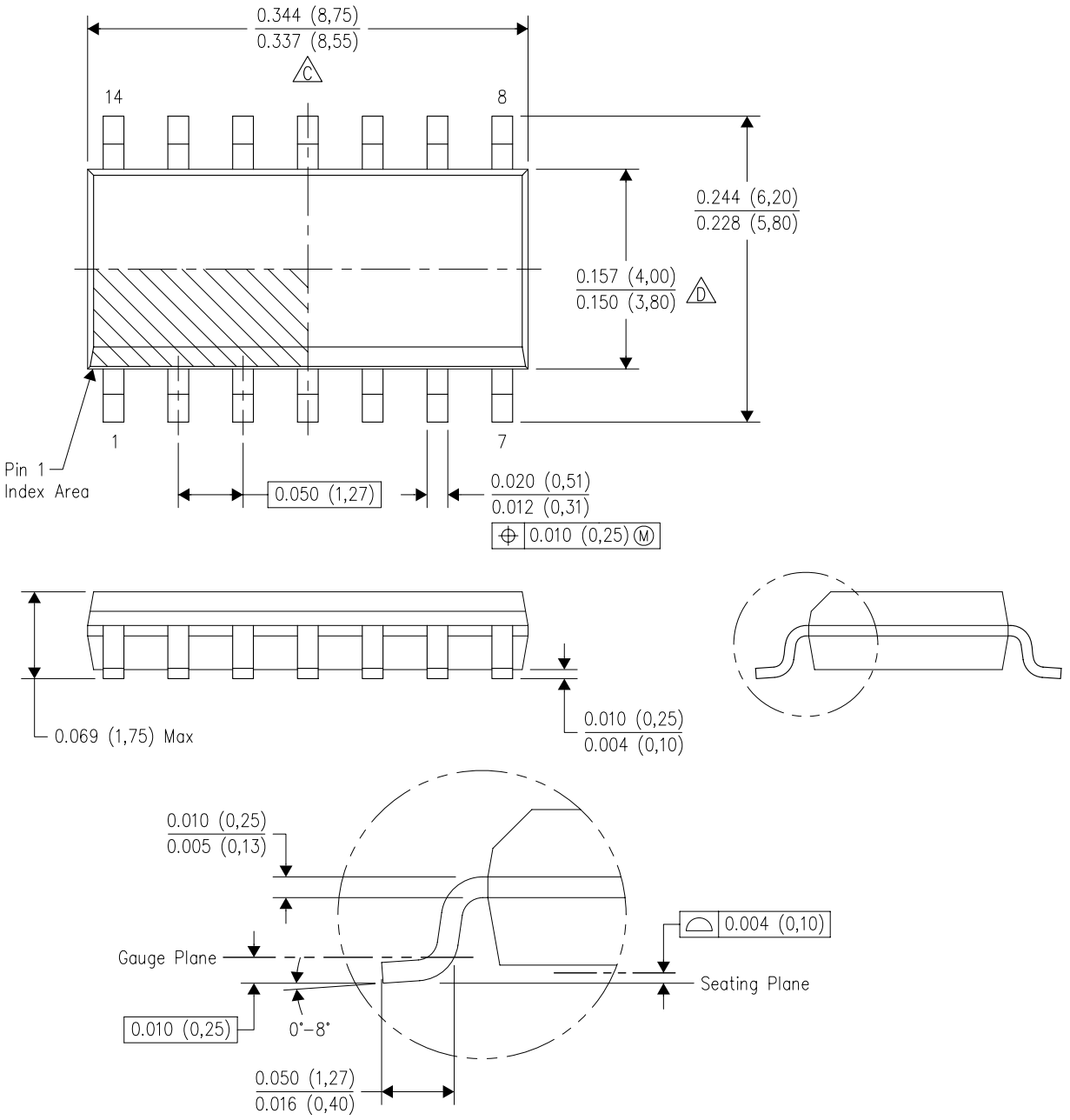
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP7701MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP7701MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMP7701MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMP7701MFX	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMP7701MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMP7702MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP7702MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP7702MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP7702MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMP7704MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMP7704MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

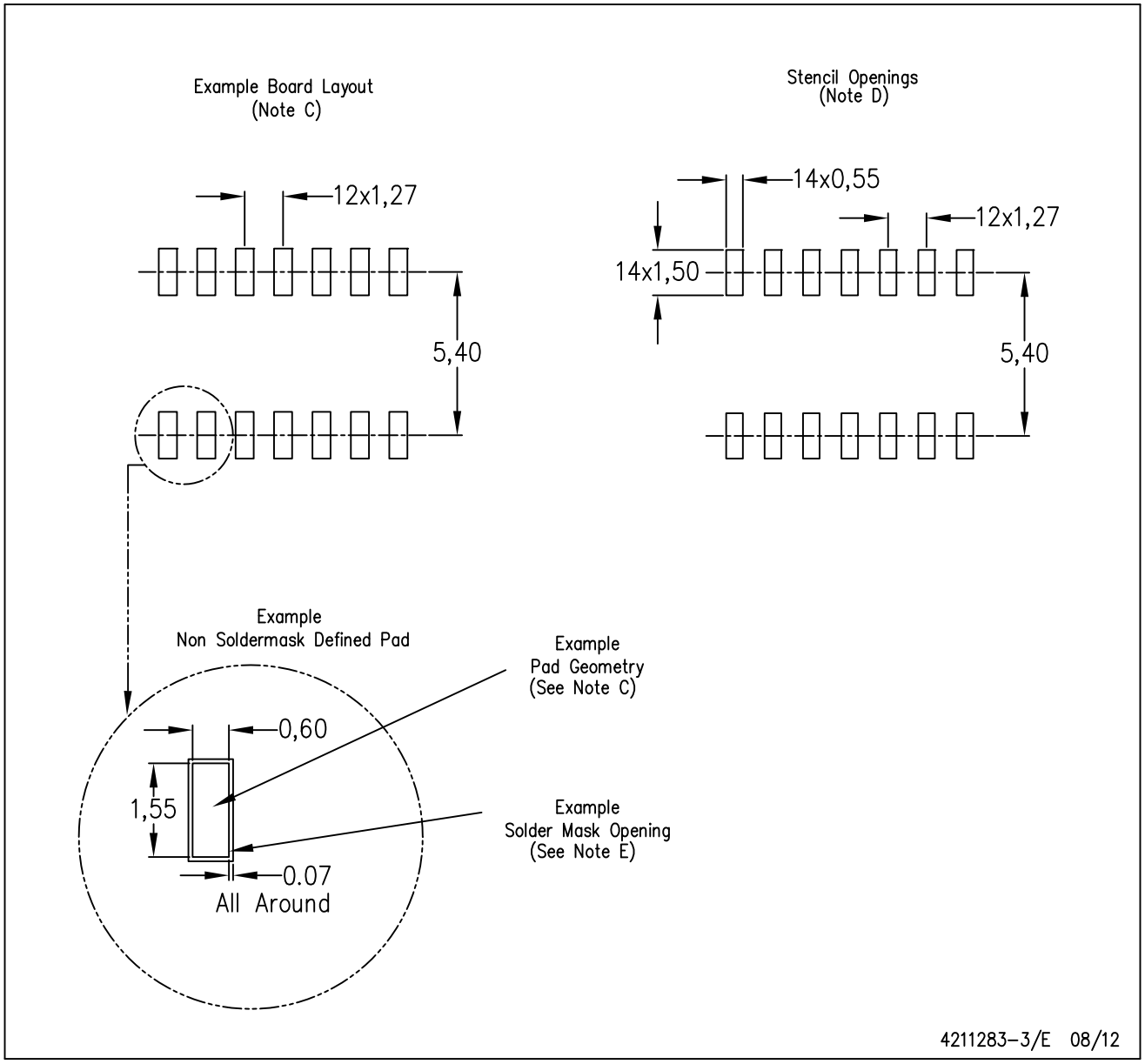
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

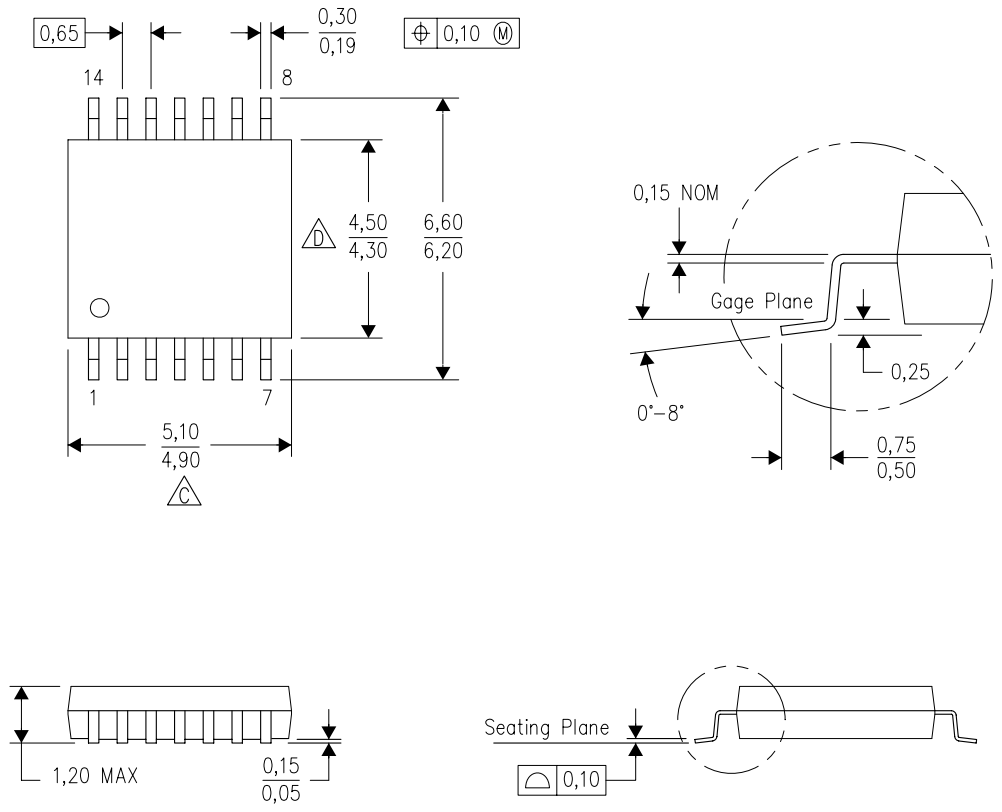
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

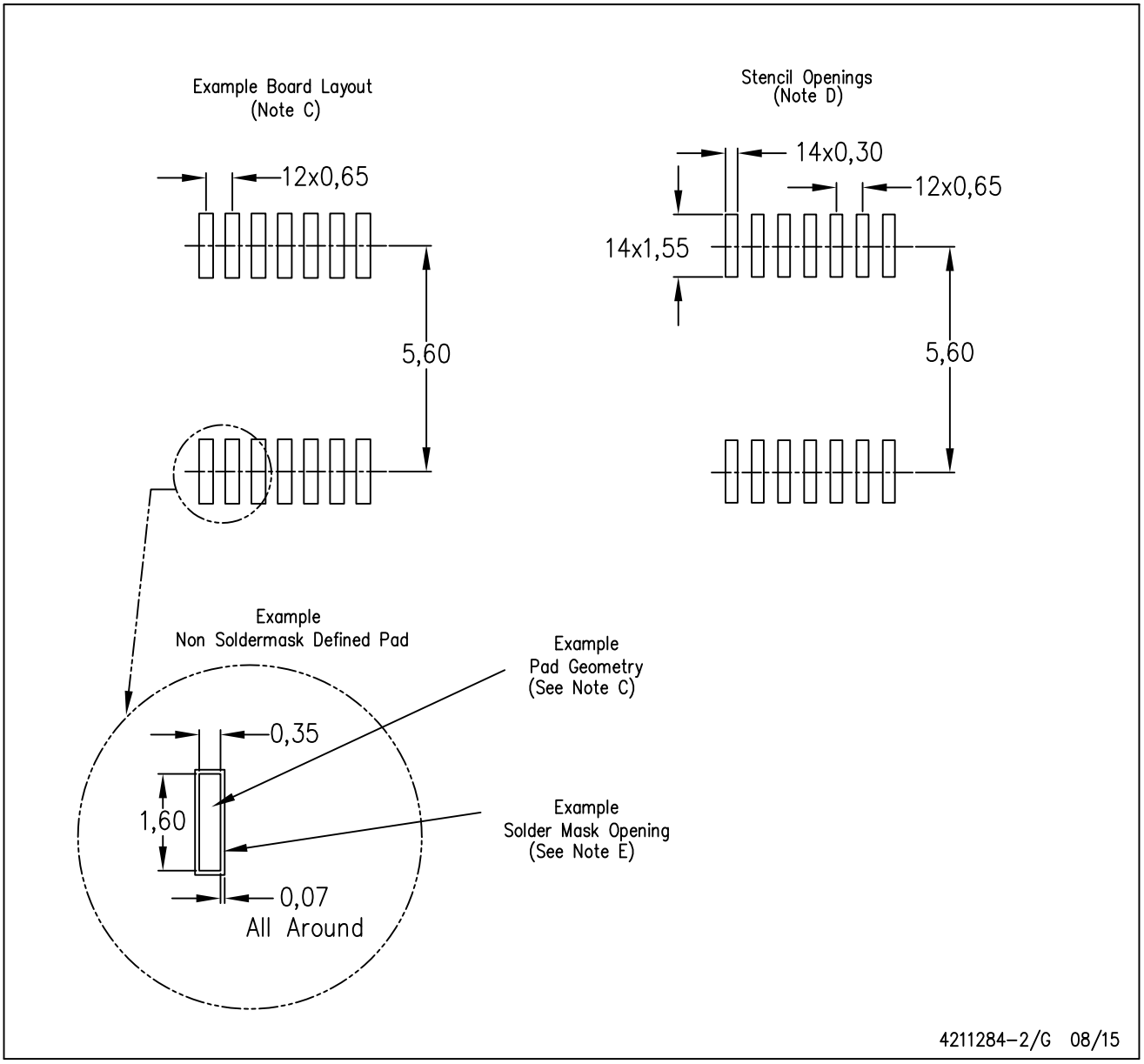
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



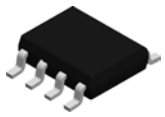
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

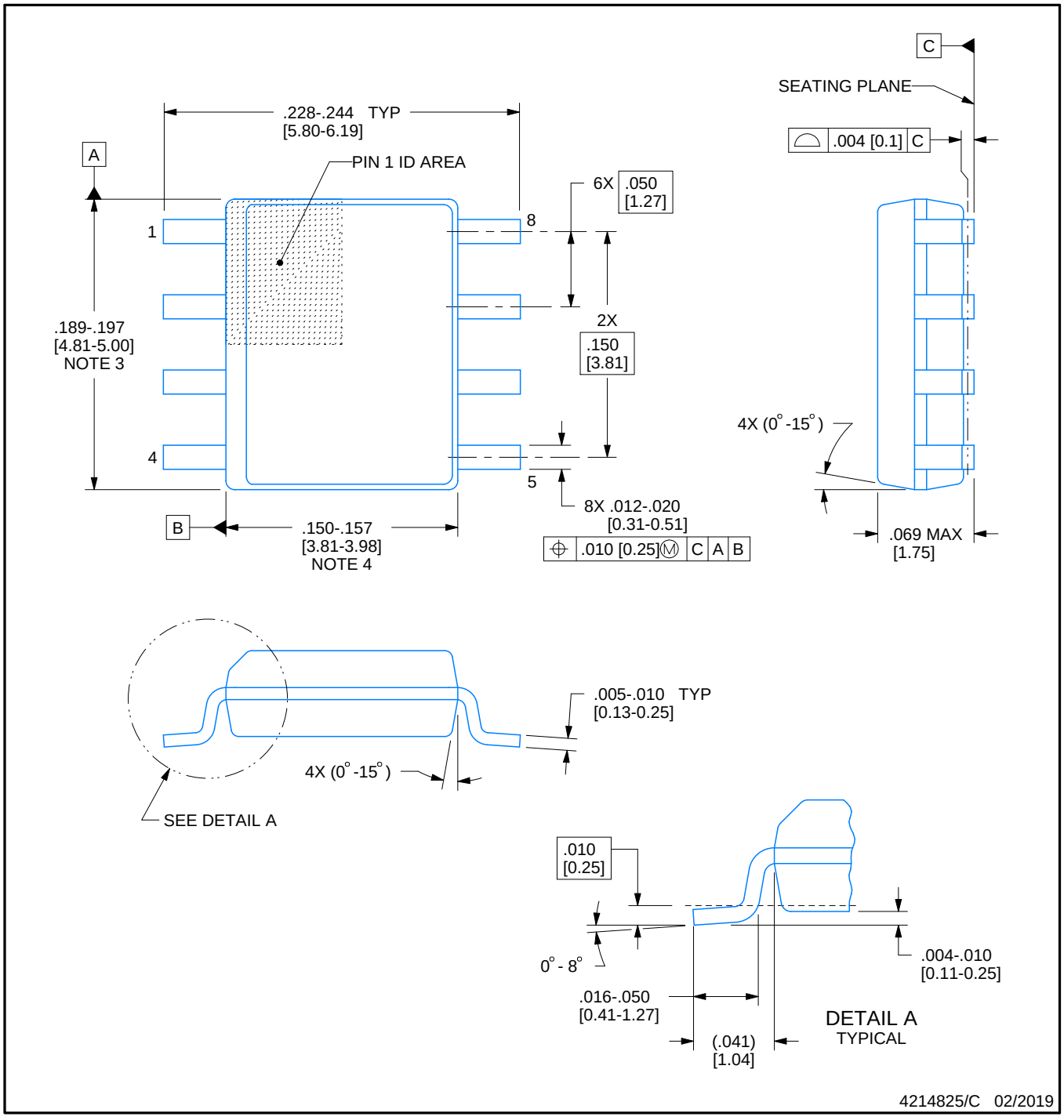


PACKAGE OUTLINE

D0008A

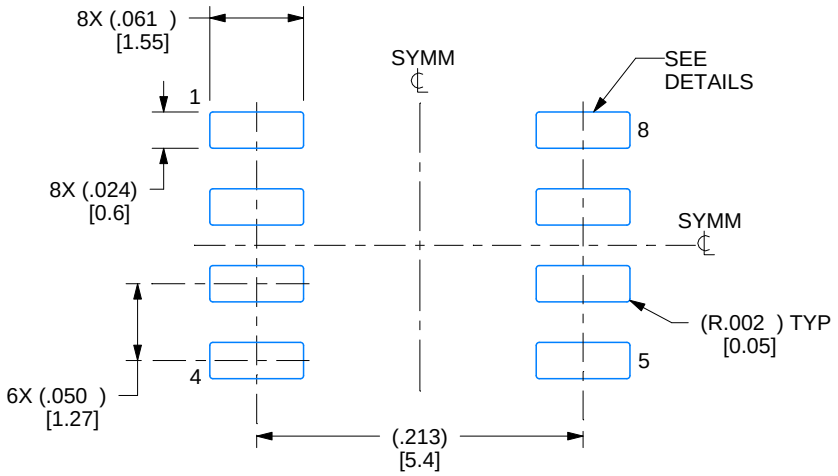
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

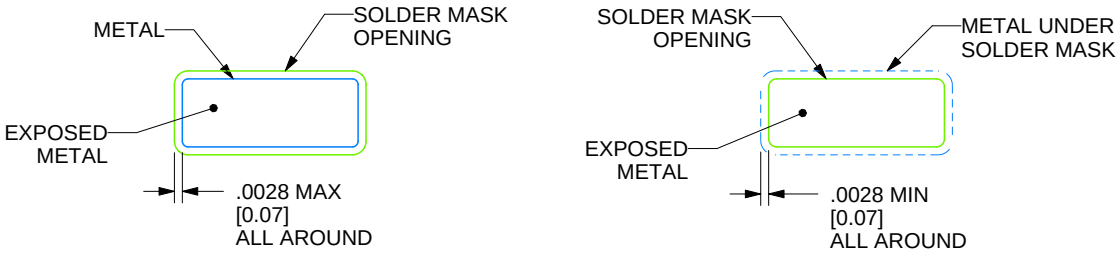


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

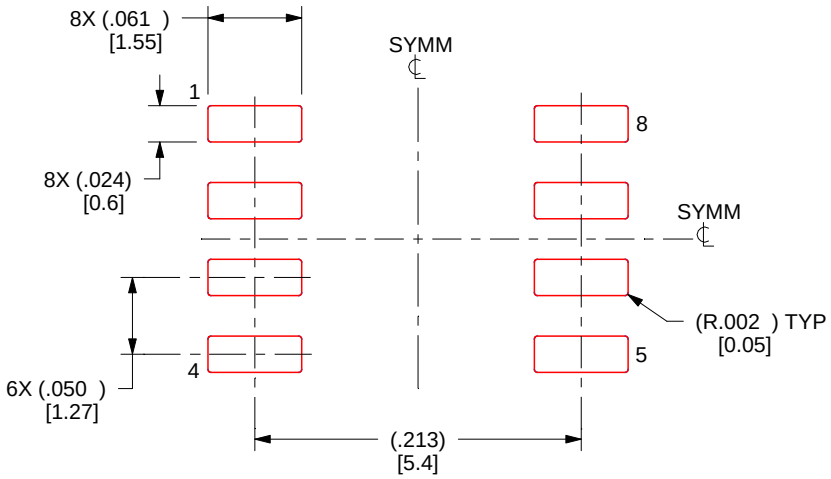
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

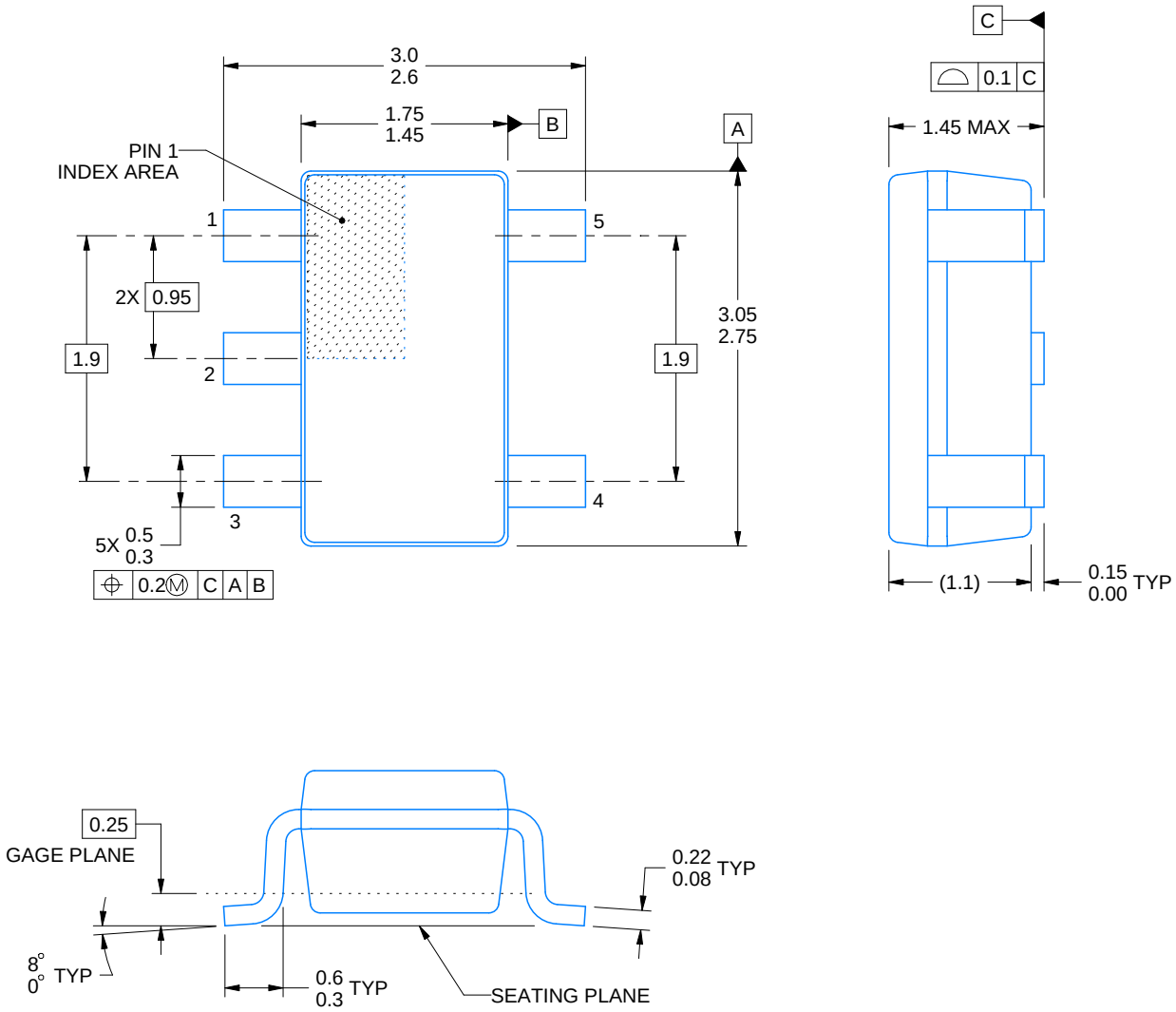
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

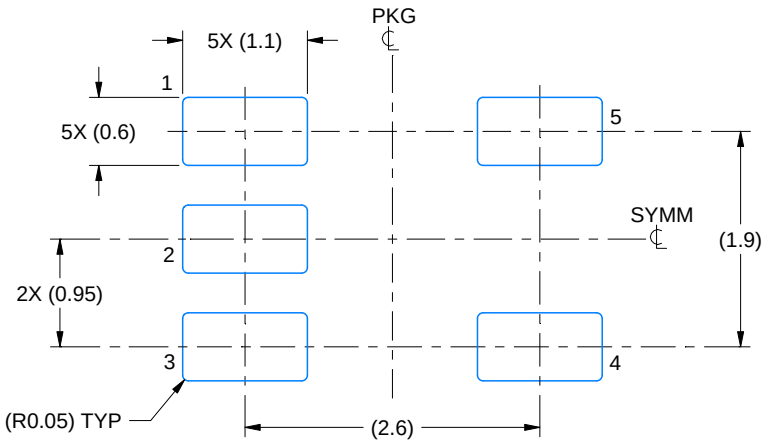
SMALL OUTLINE TRANSISTOR



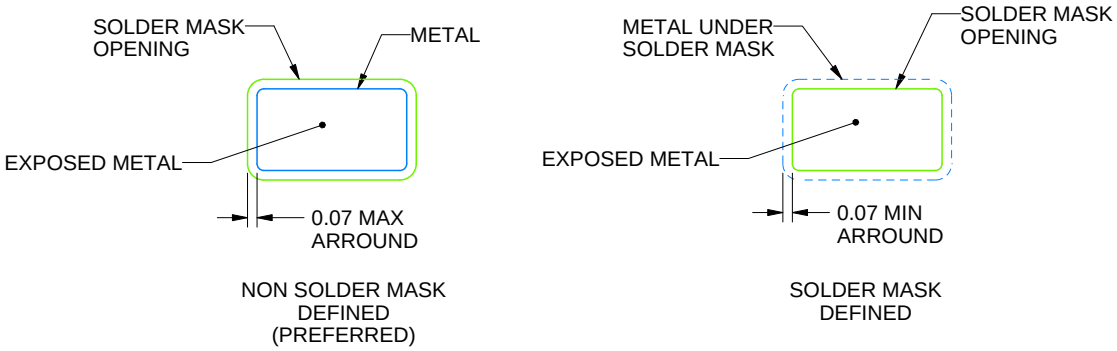
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

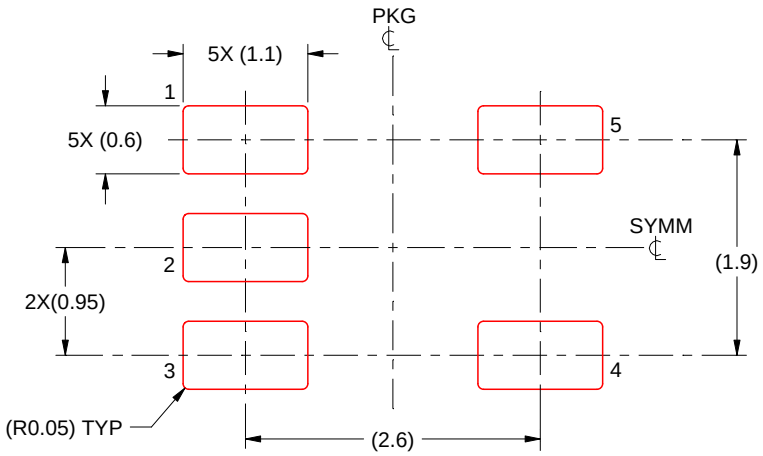


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



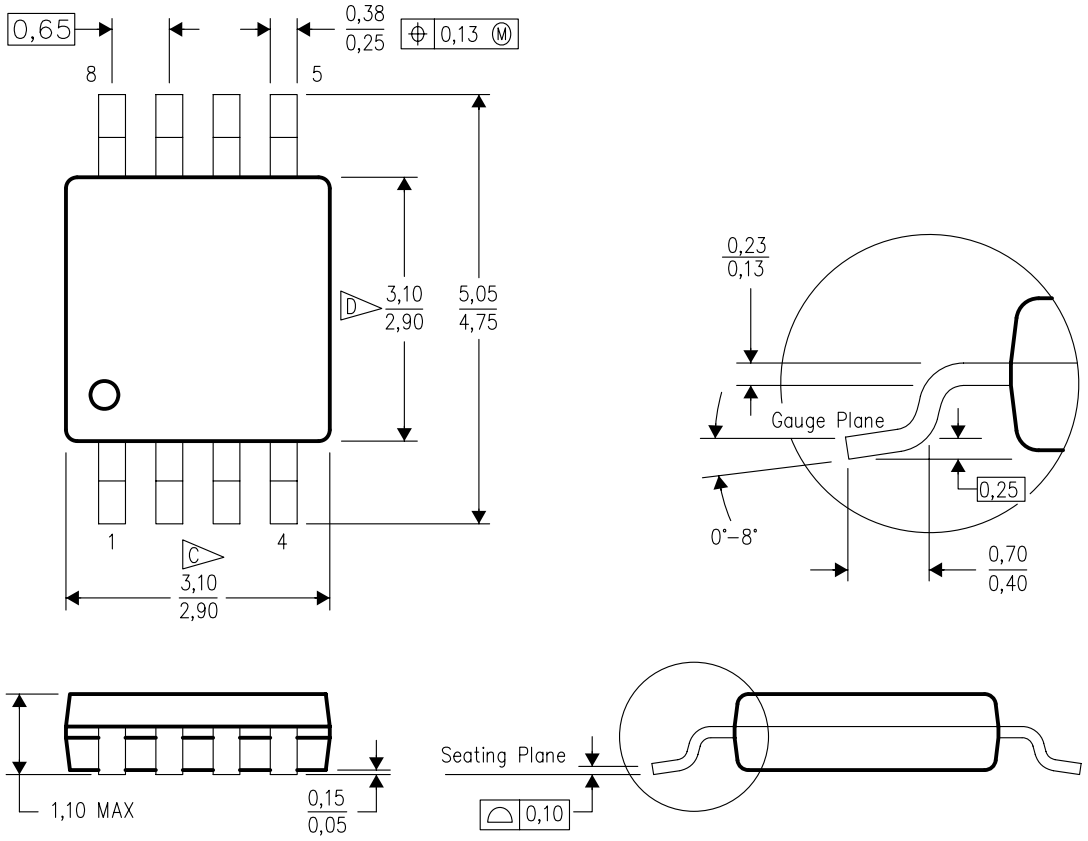
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

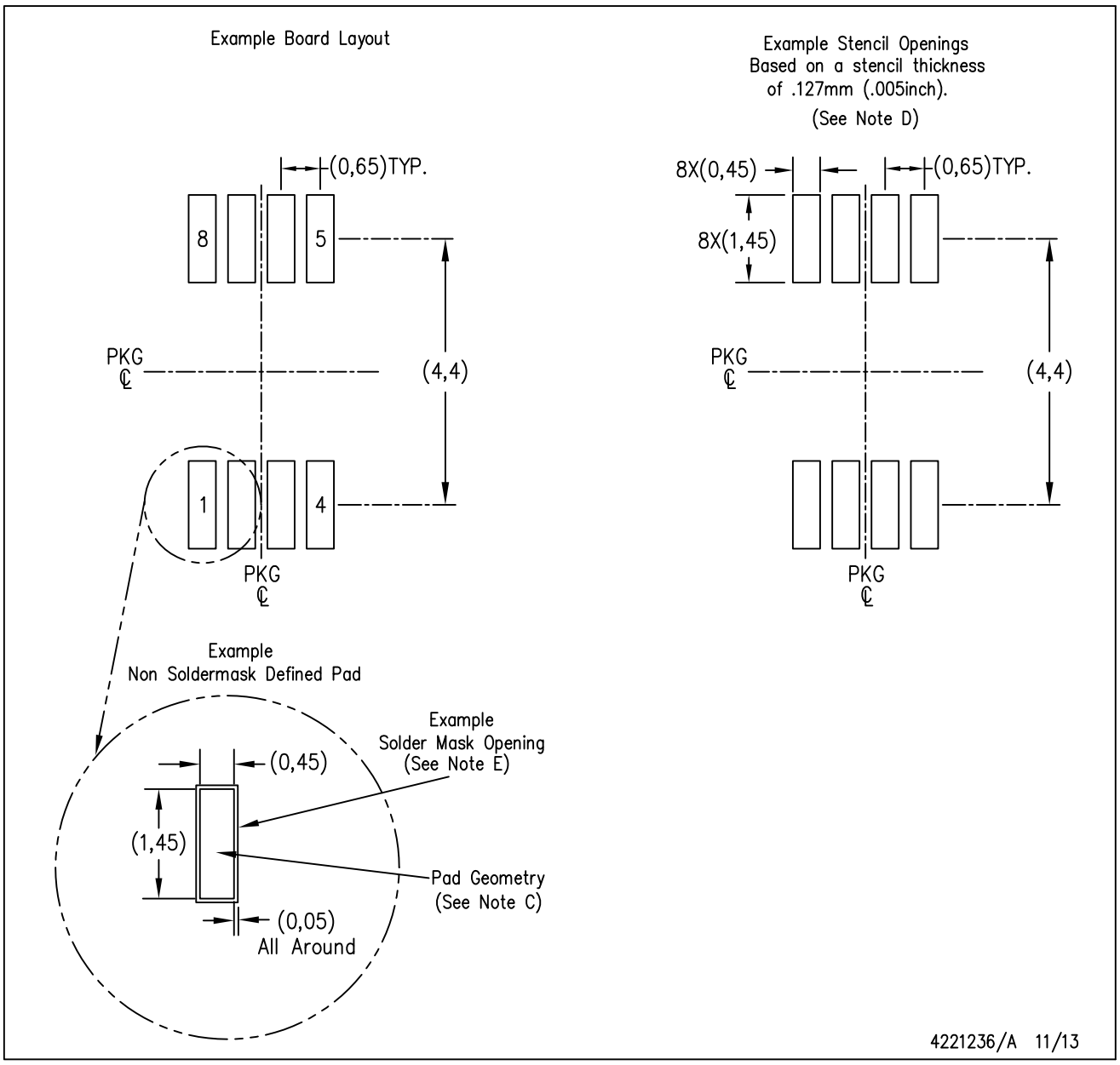
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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