



## LMH6504 Wideband, Low Power, Variable Gain Amplifier

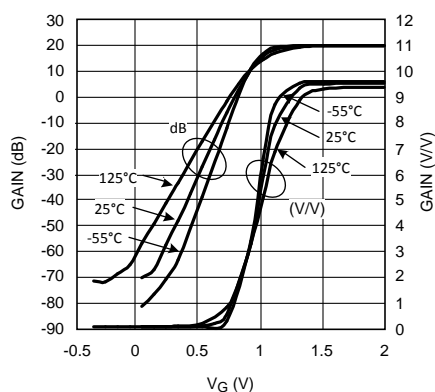
Check for Samples: [LMH6504](#)

### FEATURES

- $V_S = \pm 5V$ ,  $T_A = 25^\circ C$ ,  $R_F = 1\text{ K}\Omega$ ,  $R_G = 100\Omega$ ,  $R_L = 100\Omega$ ,  $A_V = A_{VMAX} = 9.7V/V$ , Typical values unless specified.
- -3 dB BW 150 MHz
- Gain control BW 150 MHz
- Adjustment range (<10 MHz) 80 dB
- Output offset voltage  $\pm 55\text{ mV}$
- Gain matching (limit)  $\pm 0.42\text{ dB}$
- Supply voltage range 7V to 12V
- Slew rate (inverting) 1500 V/ $\mu s$
- Supply Current (no load) 11 mA
- Linear Output Current  $\pm 60\text{ mA}$
- Output Voltage Swing  $\pm 2.2V$
- Input Noise Voltage 4.4 nV/ $\sqrt{Hz}$
- Input Noise Current 2.6 pA/ $\sqrt{Hz}$
- THD (20 MHz,  $R_L = 100\Omega$ ,  $V_O = 2\text{ V}_{PP}$ ) -45 dBc
- Replacement for CLC5523

### APPLICATIONS

- Variable attenuator
- AGC
- Voltage controlled filter
- Video imaging processing


**Figure 1. Gain vs.  $V_G$** 

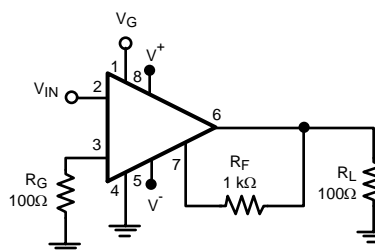
### DESCRIPTION

The LMH<sup>TM</sup>6504 is a wideband DC coupled voltage controlled gain stage followed by a high-speed current feedback Op Amp which can directly drive a low impedance load. Gain adjustment range is 80 dB for up to 10 MHz by varying the gain control input voltage,  $V_G$ .

Maximum gain is set by external components, and the gain can be reduced all the way to cut-off. Power consumption is 110 mW with a speed of 150 MHz and a gain control bandwidth (BW) of 150 MHz. Output referred DC offset voltage is less than 55 mV over the entire gain control voltage range. Device-to-device gain matching is within  $\pm 0.42\text{ dB}$  at maximum gain. Furthermore, gain is tested over a wide range. The output current feedback Op Amp allows high frequency large signals (Slew Rate > 1500 V/ $\mu s$ ) and can also drive a heavy load current (60 mA). Near ideal input characteristics (i.e. low input bias current, low offset, low pin 3 resistance) enable the device to be easily configured as an inverting amplifier as well (see Application Information section for details).

To provide ease of use when working with a single supply,  $V_G$  range is set to be from 0V to +2V relative to the ground pin potential (pin 4).  $V_G$  input impedance is high in order to ease drive requirement. In single supply operation, the ground pin is tied to a "virtual" half supply.

### Typical Application


**Figure 2.  $A_{VMAX} = 9.7\text{ V/V}$** 


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## DESCRIPTION CONTINUED

LMH6504 gain control is linear in dB for a large portion of the total gain control range. This makes the device suitable for AGC applications. For linear gain control applications, see the LMH6503 data sheet.

The combination of minimal external components and small outline packages (SOIC and VSSOP) allows the LMH6504 to be used in space-constrained applications.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings <sup>(1)</sup>

ESD Tolerance <sup>(2)</sup> :	
Human Body Model	1000V
Machine Model	100V
Input Current	±10 mA
Output Current	120 mA <sup>(3)</sup>
Supply Voltages (V <sup>+</sup> - V <sup>-</sup> )	12.6V
Voltage at Input/ Output pins	V <sup>+</sup> +0.8V, V <sup>-</sup> -0.8V
Storage Temperature Range	-65°C to 150°C
Junction Temperature	150°C
Soldering Information:	
Infrared or Convection (20 sec)	235°C
Wave Soldering (10 sec)	260°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications, see the Electrical Characteristics.
- (2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
- (3) The maximum output current (I<sub>OUT</sub>) is determined by device power dissipation limitations or value specified, whichever is lower.

### Operating Ratings

Supply Voltages (V <sup>+</sup> - V <sup>-</sup> )	7V to 12V	
Temperature Range <sup>(1)</sup>	-40°C to +85°C	
Thermal Resistance:	(θ <sub>JC</sub> )	(θ <sub>JA</sub> )
8-Pin SOIC	60	165
8-Pin VSSOP	65	235

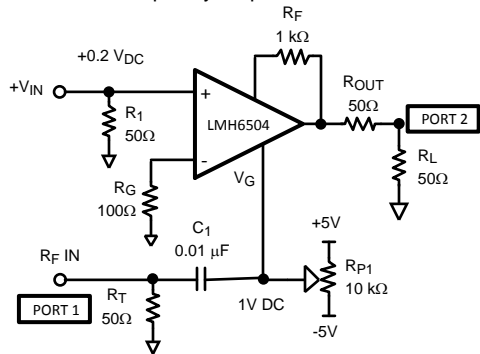
- (1) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PC Board.

**Electrical Characteristics<sup>(1)</sup>**

Unless otherwise specified, all limits are specified for  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$ ,  $A_{V\text{MAX}} = 9.7 \text{ V/V}$ ,  $R_F = 1 \text{ k}\Omega$ ,  $R_G = 100\Omega$ ,  $V_{\text{IN}} = \pm 0.1\text{V}$ ,  $R_L = 100\Omega$ ,  $V_G = +2\text{V}$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min <sup>(2)</sup>	Typ <sup>(2)</sup>	Max <sup>(2)</sup>	Units
<b>Frequency Domain Response</b>						
BW	-3dB Bandwidth	$V_{\text{OUT}} < 1 V_{\text{PP}}$		150		MHz
		$V_{\text{OUT}} < 4 V_{\text{PP}}$ , $A_{V\text{MAX}} = 100$		58		
GF	Gain Flatness	$V_{\text{OUT}} < 1 V_{\text{PP}}$ $0.9\text{V} \leq V_G \leq 2\text{V}$ , $\pm 0.2 \text{ dB}$		40		MHz
Att Range	Flat Band (Relative to Max Gain) Attenuation Range <sup>(3)</sup>	$\pm 0.2 \text{ dB Flatness}$ , $f < 30 \text{ MHz}$		26		dB
		$\pm 0.1 \text{ dB Flatness}$ , $f < 30 \text{ MHz}$		9.5		
BW Control	Gain control Bandwidth	$V_G = 1\text{V}$ <sup>(4)</sup>		150		MHz
CT (dB)	Feed-through	$V_G = 0\text{V}$ , 30 MHz (Output/Input)		-53		dB
GR	Gain Adjustment Range	$f < 10 \text{ MHz}$		80		dB
		$f < 30 \text{ MHz}$		73		
<b>Time Domain Response</b>						
$t_r$ , $t_f$	Rise and Fall Time	0.5V Step		2.1		ns
OS %	Overshoot				20	
SR	Slew Rate <sup>(5)</sup>	4V Step, Non Inverting		800		V/ $\mu\text{s}$
		4V Step, Inverting		1500		
<b>Distortion &amp; Noise Performance</b>						
HD2	2 <sup>nd</sup> Harmonic Distortion	2V <sub>PP</sub> , 20 MHz		-47		dBc
HD3	3 <sup>rd</sup> Harmonic Distortion			-55		
THD	Total Harmonic Distortion			-45		
En tot	Total Equivalent Input Noise	$f > 1 \text{ MHz}$ , $R_{\text{SOURCE}} = 50\Omega$		4.4		nV/ $\sqrt{\text{Hz}}$
I <sub>N</sub>	Input Noise Current	$f > 1 \text{ MHz}$		2.6		pA/ $\sqrt{\text{Hz}}$
DG	Differential Gain	$f = 4.43 \text{ MHz}$ , $R_L = 100\Omega$		0.45		%
DP	Differential Phase			0.13		deg

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ .
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested on shipped production material.
- (3) Flat Band Attenuation (Relative To Max Gain) Range Definition: Specified as the attenuation range from maximum which allows gain flatness specified (either  $\pm 0.2\text{dB}$  or  $\pm 0.1\text{dB}$ ), relative to  $A_{V\text{MAX}}$  gain. For example, for  $f < 30 \text{ MHz}$ , here are the Flat Band Attenuation ranges:  $\pm 0.2 \text{ dB}$ : 19.7 dB down to -6.3 dB = 26 dB range  $\pm 0.1 \text{ dB}$ : 19.7 dB down to 10.2 dB = 9.5 dB range
- (4) Gain control frequency response schematic:



- (5) Slew rate is the average of the rising and falling slew rates.

## Electrical Characteristics<sup>(1)</sup> (continued)

Unless otherwise specified, all limits are specified for  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$ ,  $A_{V\text{MAX}} = 9.7 \text{ V/V}$ ,  $R_F = 1 \text{ k}\Omega$ ,  $R_G = 100\Omega$ ,  $V_{\text{IN}} = \pm 0.1\text{V}$ ,  $R_L = 100\Omega$ ,  $V_G = +2\text{V}$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min <sup>(2)</sup>	Typ <sup>(2)</sup>	Max <sup>(2)</sup>	Units
<b>DC &amp; Miscellaneous Performance</b>						
GACCU	Gain Accuracy (See Application Note)	$V_G = 2.0\text{V}$		0	$\pm 0.45$	dB
		$0.8\text{V} < V_G < 2\text{V}$		$\pm 0.33$	$\pm 3.9$	
G Match	Gain Matching (See Application Note)	$V_G = 2.0\text{V}$		—	$\pm 0.42$	dB
		$0.8\text{V} < V_G < 2\text{V}$		—	$+2.8/-4.2$	
K	Gain Multiplier (See Application Notes)		0.920 <b>0.916</b>	0.965	1.01 <b>1.02</b>	V/V
$V_{\text{IN NL}}$	Input Voltage Range	$R_G$ Open		$\pm 3.2$		V
$V_{\text{IN L}}$		$R_G = 100\Omega$	$\pm 0.48$ <b><math>\pm 0.40</math></b>	$\pm 0.68$		
$I_{\text{RG\_MAX}}$	$R_G$ Current	Pin 3	$\pm 4.8$ <b><math>\pm 4.0</math></b>	$\pm 6.8$		mA
$I_{\text{BIAS}}$	Bias Current	Pin 2 <sup>(6)</sup>		-1.4	-3.5 <b>-3.7</b>	$\mu\text{A}$
TC $I_{\text{BIAS}}$	Bias Current Drift	Pin 2 <sup>(7) (8)</sup>		$\pm 200$		$\text{pA}/^\circ\text{C}$
$R_{\text{IN}}$	Input Resistance	Pin 2		7		M $\Omega$
$C_{\text{IN}}$	Input Capacitance	Pin 2		2.8		pF
$I_{\text{VG}}$	$V_G$ Bias Current	Pin 1, $V_G = 2\text{V}$ <sup>(6)</sup>		0.9		$\mu\text{A}$
TC $I_{\text{VG}}$	$V_G$ Bias Drift	Pin 1 <sup>(7)</sup>		10		$\text{pA}/^\circ\text{C}$
$R_{\text{VG}}$	$V_G$ Input Resistance	Pin 1		25		M $\Omega$
$C_{\text{VG}}$	$V_G$ Input Capacitance	Pin 1		2.8		pF
$V_{\text{OUT L}}$	Output Voltage Range	$R_L = 100\Omega$	$\pm 2.0$ <b><math>\pm 1.7</math></b>	$\pm 2.2$		V
$V_{\text{OUT NL}}$		$R_L = \text{Open}$		$\pm 3.1$		
$R_{\text{OUT}}$	Output Impedance	DC		0.12		$\Omega$
$I_{\text{OUT}}$	Output Current	$V_{\text{OUT}} = \pm 4\text{V}$ from Rails	$\pm 60$ <b><math>\pm 40</math></b>	$\pm 80$		mA
$V_{\text{O\_OFFSET}}$	Output Offset Voltage	$0\text{V} < V_G < 2\text{V}$		$\pm 10$	$\pm 55$ <b><math>\pm 70</math></b>	mV
+PSRR	+Power Supply Rejection Ratio <sup>(9)</sup>	Input Referred, 1V change, $V_G = 2.2\text{V}$	-65	-76		dB
-PSRR	-Power Supply Rejection Ratio <sup>(9)</sup>	Input Referred, 1V change, $V_G = 2.2\text{V}$	-65	-88		dB
$I_S$	Supply Current	No Load	8.5 <b>6.5</b>	11	15 <b>16</b>	mA

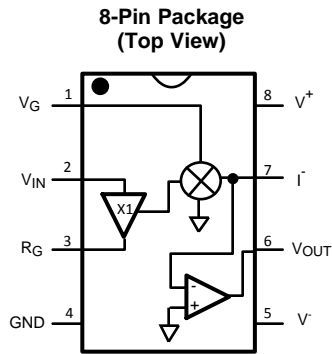
(6) Positive current corresponds to current flowing into the device.

(7) Drift determined by dividing the change in parameter distribution at temperature extremes by the total temperature change.

(8) Input bias current drift with temperature can be either positive or negative for a given sample.

(9) +PSRR definition:  $[|\Delta V_{\text{OUT}}/\Delta V^+| / A_V]$ , -PSRR definition:  $[|\Delta V_{\text{OUT}}/\Delta V^-| / A_V]$  with 0.1V input voltage.  $\Delta V_{\text{OUT}}$  is the change in output voltage with offset shift subtracted out.

**CONNECTION DIAGRAM**



**See Package Number D0008A (SOIC)  
and DGK008A (VSSOP)**

### Typical Performance Characteristics

Unless otherwise specified:  $V_S = \pm 5V$ ,  $T_A = 25^\circ C$ ,  $V_G = V_{GMAX}$ ,  $R_F = 1\text{ k}\Omega$ ,  $R_G = 100\Omega$ ,  $V_{IN} = 0.1V$ , input terminated in  $50\Omega$ .  $R_L = 100\Omega$ , Typical values.

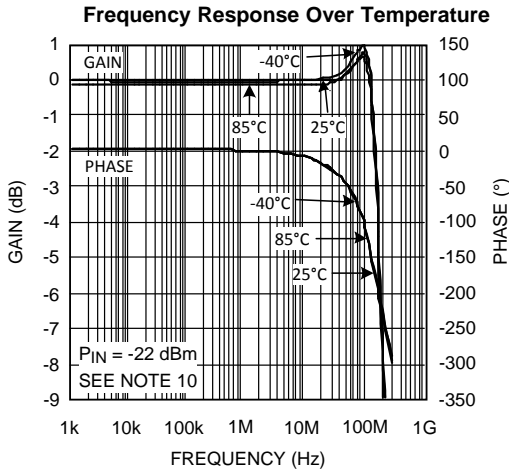


Figure 3.

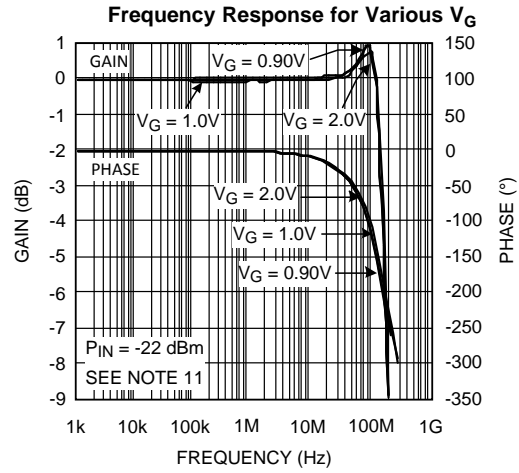


Figure 4.

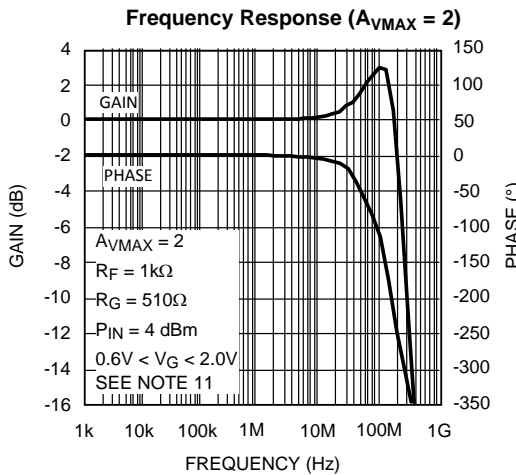


Figure 5.

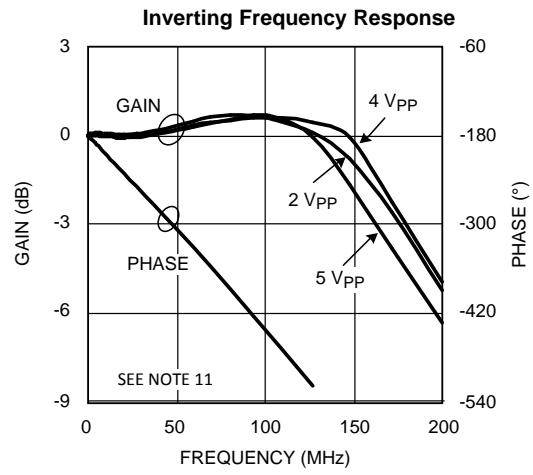


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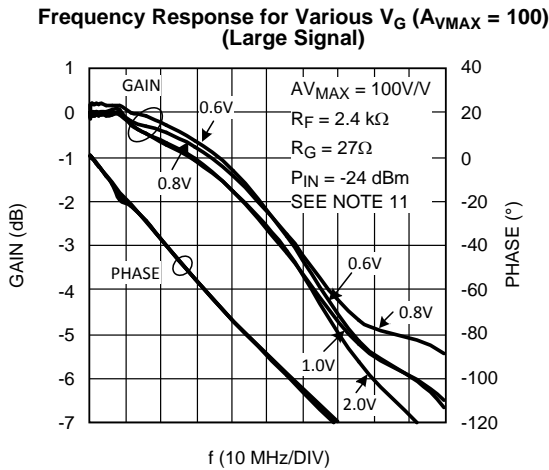


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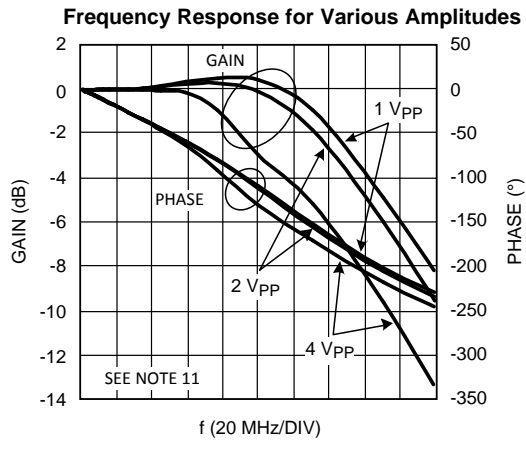


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified:  $V_S = \pm 5V$ ,  $T_A = 25^\circ C$ ,  $V_G = V_{GMAX}$ ,  $R_F = 1\text{ k}\Omega$ ,  $R_G = 100\Omega$ ,  $V_{IN} = 0.1V$ , input terminated in  $50\Omega$ .  $R_L = 100\Omega$ , Typical values.

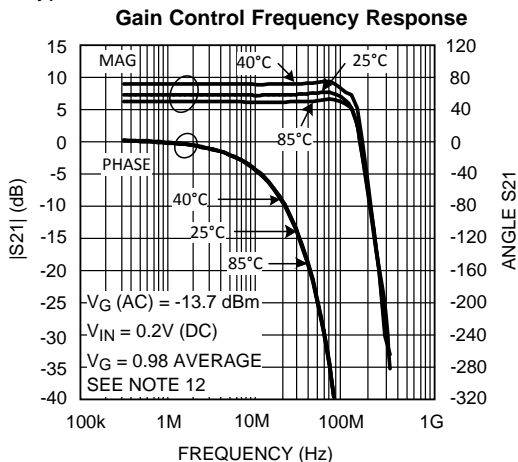


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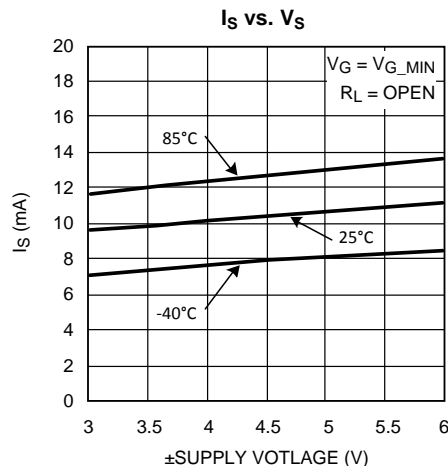


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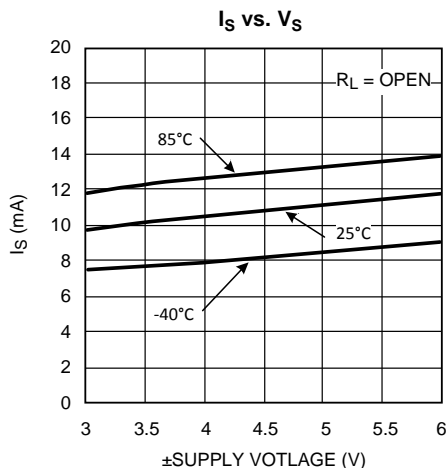


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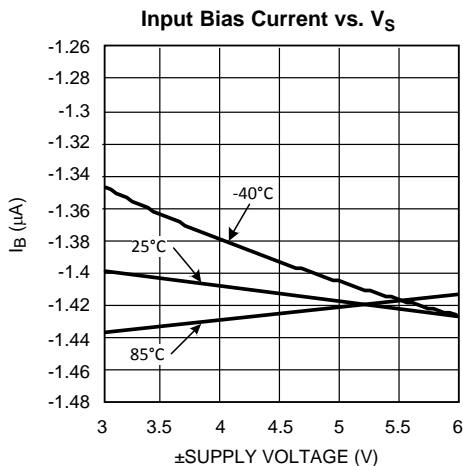


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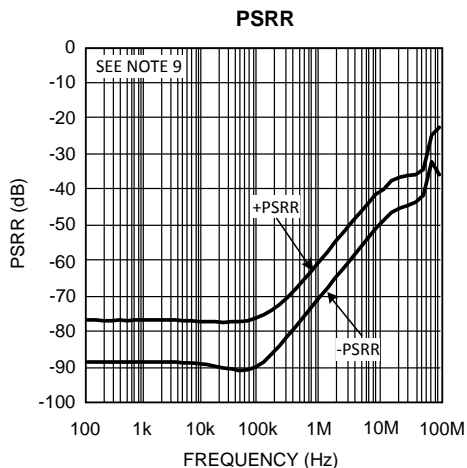


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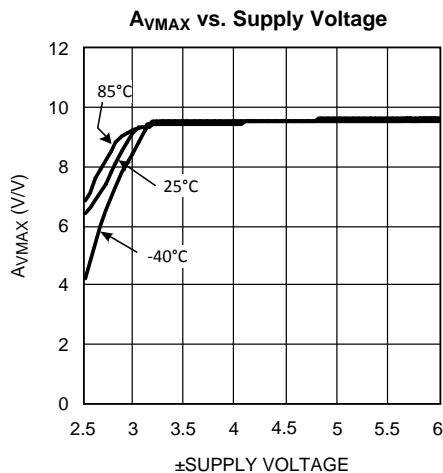


Figure 14.

**Typical Performance Characteristics (continued)**

Unless otherwise specified:  $V_S = \pm 5V$ ,  $T_A = 25^\circ C$ ,  $V_G = V_{GMAX}$ ,  $R_F = 1\text{ k}\Omega$ ,  $R_G = 100\Omega$ ,  $V_{IN} = 0.1V$ , input terminated in  $50\Omega$ .  $R_L = 100\Omega$ , Typical values.

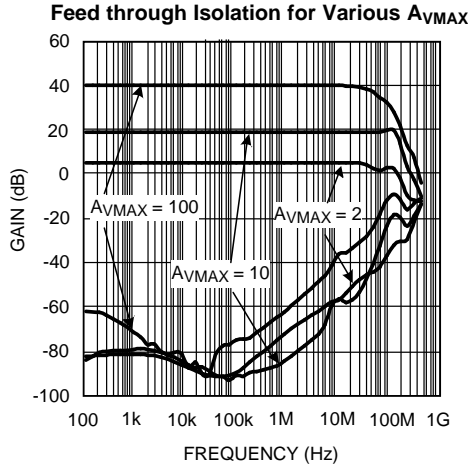


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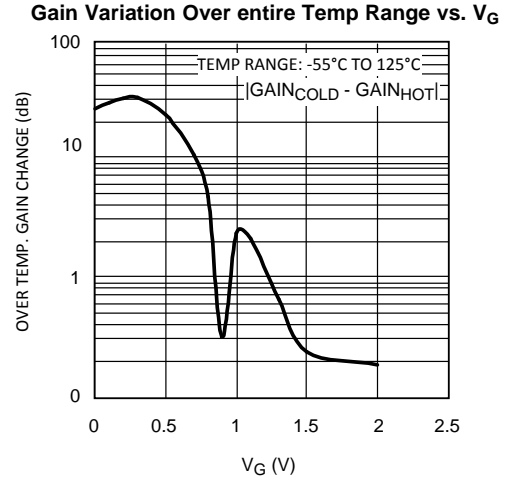


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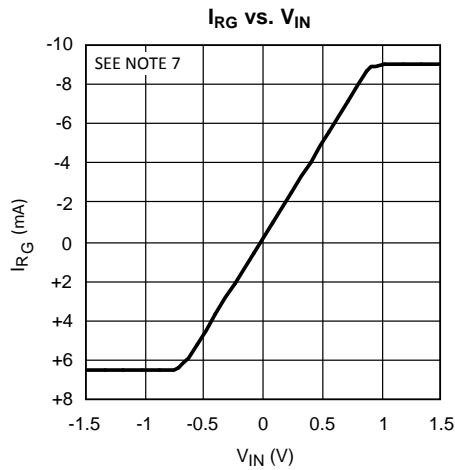


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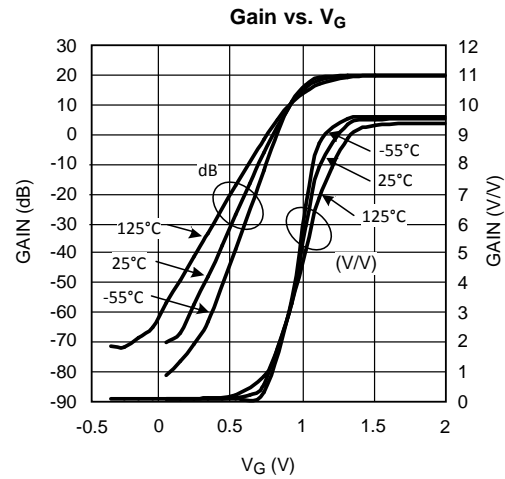


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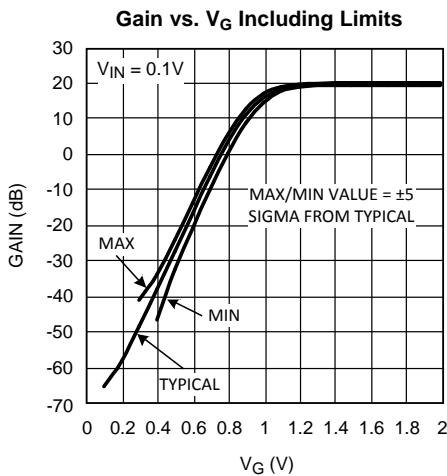


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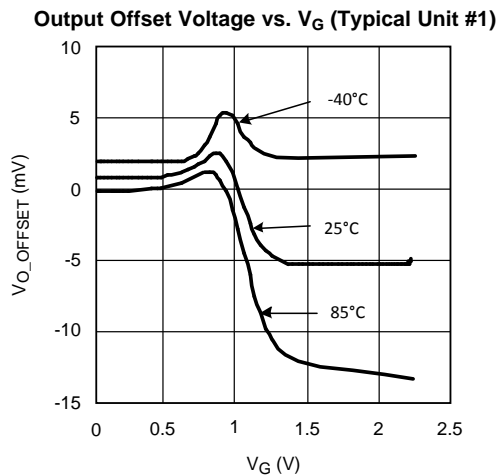


Figure 20.

**Typical Performance Characteristics (continued)**

Unless otherwise specified:  $V_S = \pm 5V$ ,  $T_A = 25^\circ C$ ,  $V_G = V_{GMAX}$ ,  $R_F = 1\text{ k}\Omega$ ,  $R_G = 100\Omega$ ,  $V_{IN} = 0.1V$ , input terminated in  $50\Omega$ .  $R_L = 100\Omega$ , Typical values.

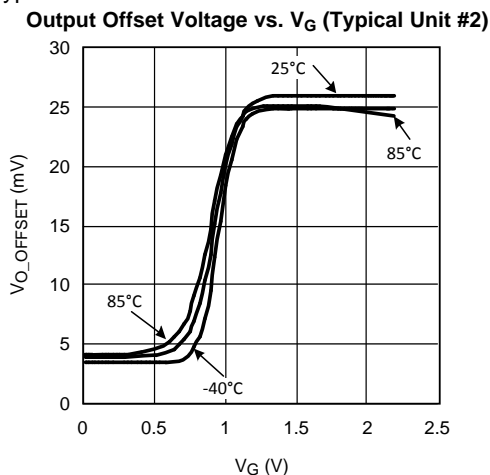


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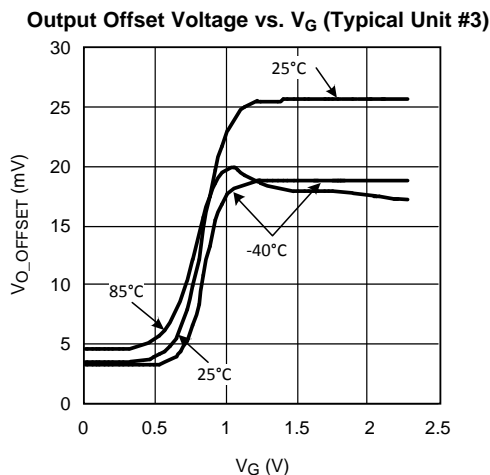


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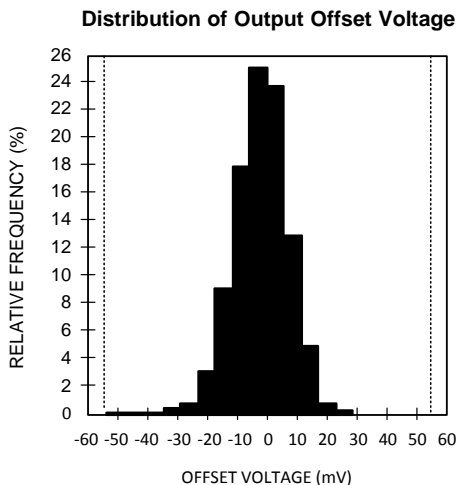


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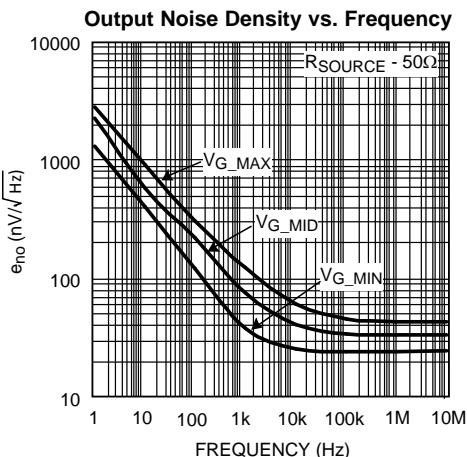


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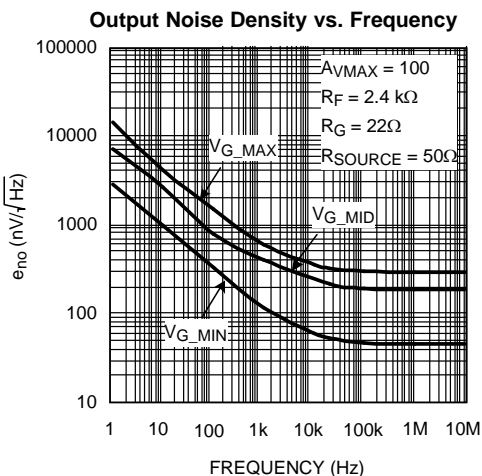


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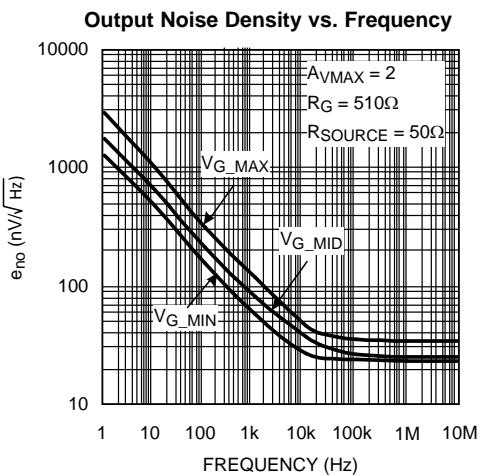


Figure 26.

**Typical Performance Characteristics (continued)**

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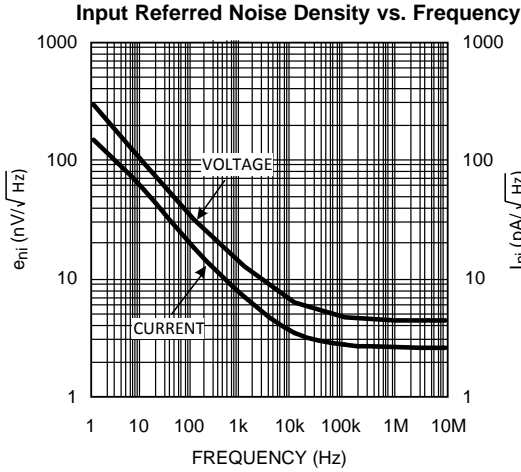


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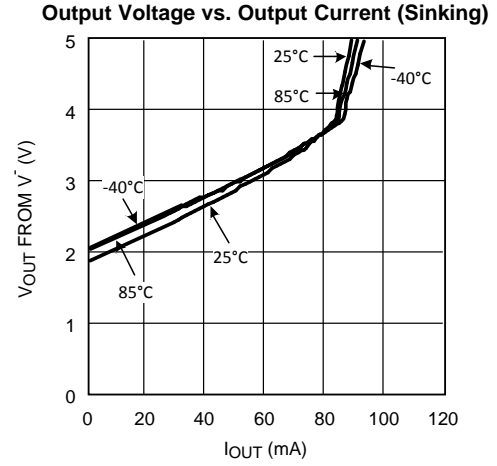


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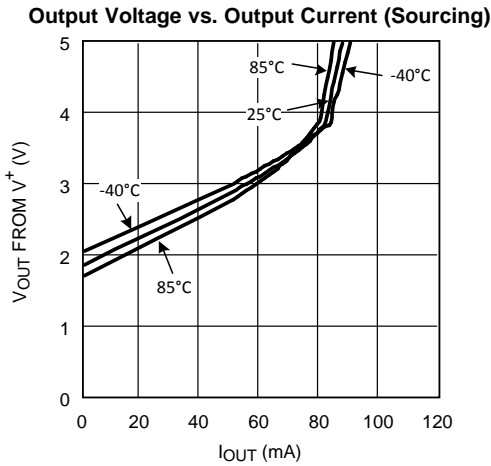


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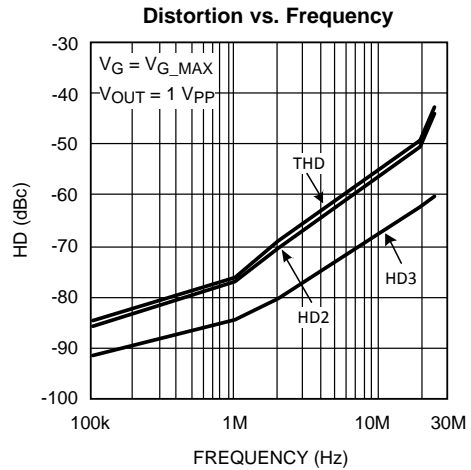


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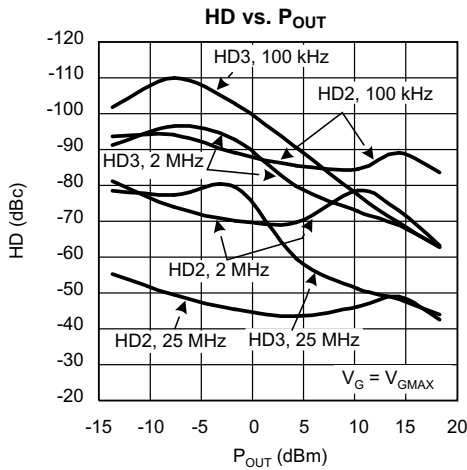


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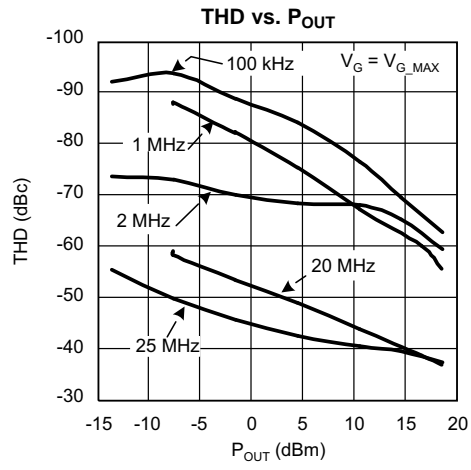


Figure 32.

**Typical Performance Characteristics (continued)**

Unless otherwise specified:  $V_S = \pm 5V$ ,  $T_A = 25^\circ C$ ,  $V_G = V_{GMAX}$ ,  $R_F = 1\text{ k}\Omega$ ,  $R_G = 100\Omega$ ,  $V_{IN} = 0.1V$ , input terminated in  $50\Omega$ .  $R_L = 100\Omega$ , Typical values.

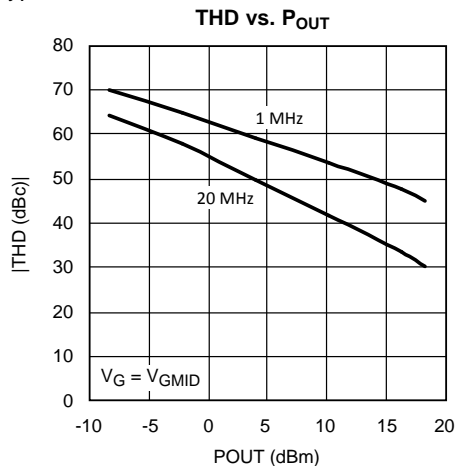


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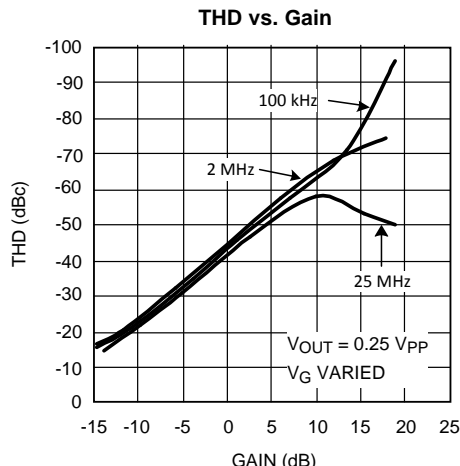


Figure 34.

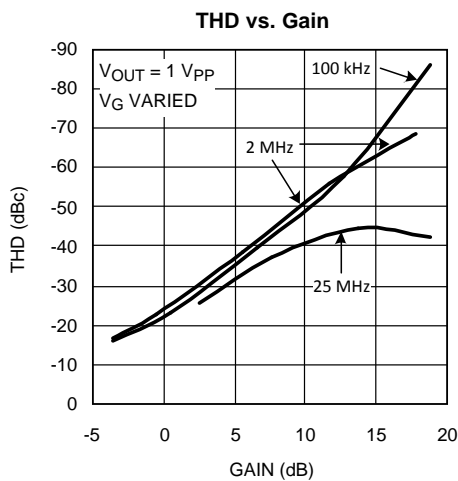


Figure 35.

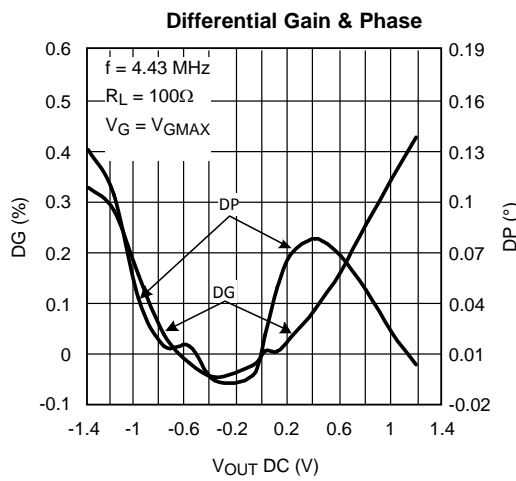


Figure 36.

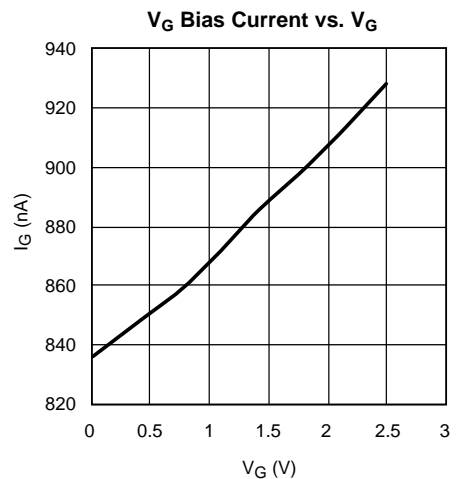


Figure 37.

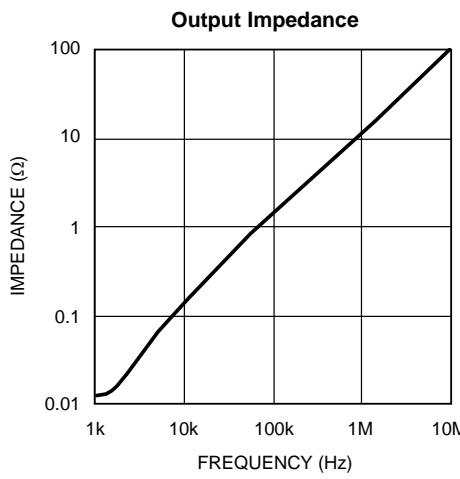


Figure 38.

**Typical Performance Characteristics (continued)**

Unless otherwise specified:  $V_S = \pm 5V$ ,  $T_A = 25^\circ C$ ,  $V_G = V_{GMAX}$ ,  $R_F = 1\text{ k}\Omega$ ,  $R_G = 100\Omega$ ,  $V_{IN} = 0.1V$ , input terminated in  $50\Omega$ .  $R_L = 100\Omega$ , Typical values.

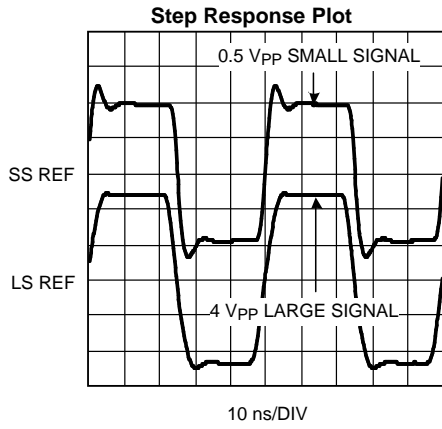


Figure 39.

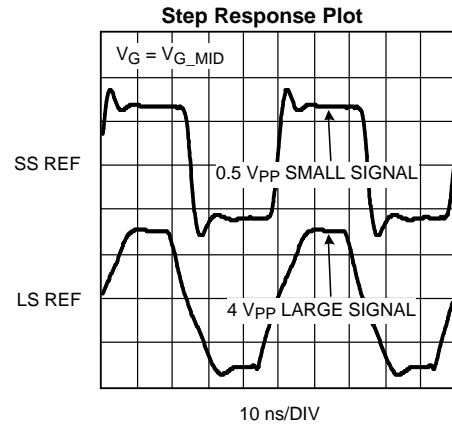


Figure 40.

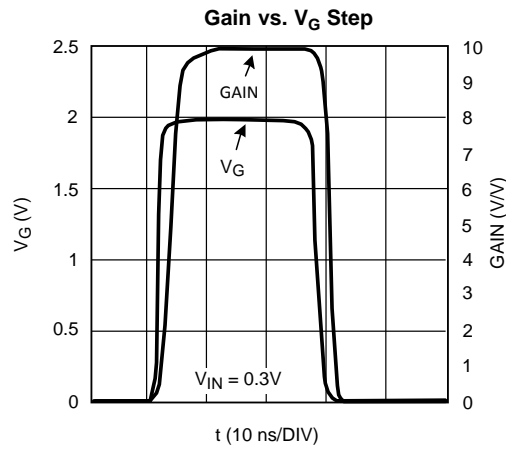


Figure 41.

## APPLICATION INFORMATION

### GENERAL DESCRIPTION

The key features of the LMH6504 are:

- Low power
- Broad voltage controlled gain and attenuation range (From  $A_{VMAX}$  down to complete cutoff)
- Bandwidth independent, resistor programmable gain range ( $R_G$ )
- Broad signal and gain control bandwidths
- Frequency response may be adjusted with  $R_F$
- High impedance signal and gain control inputs

Refer to [Figure 42](#) below. The LMH6504 combines a closed loop input buffer (“X1” Block), a voltage controlled variable gain cell (“MULT” Block) and an output amplifier (“CFA” Block). The input buffer is a transconductance stage whose gain is set by the gain setting resistor,  $R_G$ . The output amplifier is a current feedback op amp and is configured as a transimpedance stage whose gain is set by, and is equal to, the feedback resistor,  $R_F$ . The maximum gain,  $A_{VMAX}$ , of the LMH6504 is defined by the ratio:  $K \cdot R_F / R_G$  where “K” is the gain multiplier with a nominal value of 0.965. As the gain control input ( $V_G$ ) changes over its 0 to 2V range, the gain is adjusted over a range of about 80 dB relative to the maximum set gain.

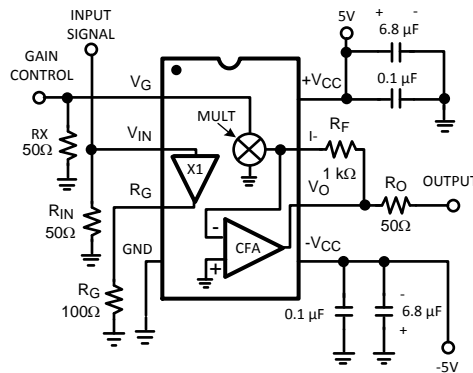


Figure 42. LMH6504 Typical Application and Block Diagram

### SETTING THE LMH6504 MAXIMUM GAIN

$$A_{VMAX} = \frac{R_F}{R_G} \cdot K \quad (1)$$

Although the LMH6504 is specified at  $A_{VMAX} = 9.7V/V$ , the recommended  $A_{VMAX}$  varies between 2 and 100. Higher gains are possible but usually impractical due to output offsets, noise and distortion. When varying  $A_{VMAX}$  several tradeoffs are made:

$R_G$ : determines the input voltage range

$R_F$ : determines overall bandwidth

The amount of current which the input buffer can source/sink into  $R_G$  is limited and is specified in the  $I_{RG\_MAX}$  spec. This sets the maximum input voltage:

$$V_{IN} (MAX) = I_{RG\_MAX} \cdot R_G \quad (2)$$

As the  $I_{RG\_MAX}$  limit is approached (with increasing input voltage or with lowering of  $R_G$ ), the device harmonic distortion will increase. Changes in  $R_F$  will have a dramatic effect on the small signal bandwidth. The output amplifier of the LMH6504 is a current feedback amplifier (CFA) and its bandwidth is determined by  $R_F$ . As with any CFA, doubling the feedback resistor will roughly cut the bandwidth of the device in half. For more about CFA's, see the basic tutorial, OA-20, "Current Feedback Myths Debunked" ([SNOA376](#)), or a more rigorous analysis, OA-13, "Current Feedback Amplifier Loop Gain Analysis and Performance Enhancements" ([SNOA366](#)).

## OTHER CONFIGURATIONS

### 1) Single Supply Operation

The LMH6504 can be configured for use in a single supply environment. Doing so requires the following:

- Bias pin 4 and  $R_G$  to a "virtual half supply" somewhere close to the middle of  $V^+$  and  $V^-$  range. The other end of  $R_G$  is tied to pin 3. The "virtual half supply" needs to be capable of sinking and sourcing the expected current flow through  $R_G$ .
- Ensure that  $V_G$  can be adjusted from 0V to 2V above the "virtual half supply".
- Bias the input (pin 2) to make sure that it stays within the range of 1.8V above  $V^-$  to 1.8V below  $V^+$  (see "Input voltage Range" specification in the Electrical Characteristics table). This can be accomplished by either DC biasing the input and AC coupling the input signal, or alternatively, by direct coupling if the output of the driving stage is also biased to half supply.

Arranged this way, the LMH6504 will respond to the current flowing through  $R_G$ . The gain control relationship will be similar to the split supply arrangement with  $V_G$  measured referenced to pin 4. Keep in mind that the circuit described above will also center the output voltage to the "virtual half supply voltage".

### 2) Arbitrarily Referenced Input Signal

Having a wide input voltage range on the input (pin 2) (+/-3.2V typical), the LMH6504 can be configured to control the gain on signals which are not referenced to ground (e.g. Half Supply biased circuits, etc.). We will call this node the "reference node". In such cases, the other end of  $R_G$  (the side not tied to pin 3) can be tied to this reference node so that  $R_G$  will "look at" the difference between the signal and this reference node only. Keep in mind that the reference node needs to source and sink the current flowing through  $R_G$ .

## Application Information

### GAIN ACCURACY

Gain accuracy is defined as the actual gain compared against the theoretical gain at a certain  $V_G$  (results expressed in dB) (See [Figure 43](#)).

Theoretical gain is given by:

$$A(V/V) = K \times \frac{R_F}{R_G} \times \frac{1}{1 + e^{\left[ \frac{N - V_G}{V_C} \right]}} \quad (3)$$

Where  $K = 0.965$  (nominal)  $N = 0.96V$  &  $V_C = 80mV$  @ room temperature

For a  $V_G$  range, the value specified in the tables represents the worst case accuracy over the entire range. The "Typical" value would be the worst case difference between the "Typical gain" and the "Theoretical gain". The "Max" value would be the worst case difference between the actual gain and the "Theoretical gain" for the entire population.

### GAIN MATCHING

Gain matching as the limit on gain variation at a certain  $V_G$  (expressed in dB) (see [Figure 43](#)) and is specified as "Max" only (no "Typical"). For a  $V_G$  range, the value specified represents the worst case matching over the entire range. The "Max" value would be the worst case difference between the actual gain and the typical gain for the entire population.

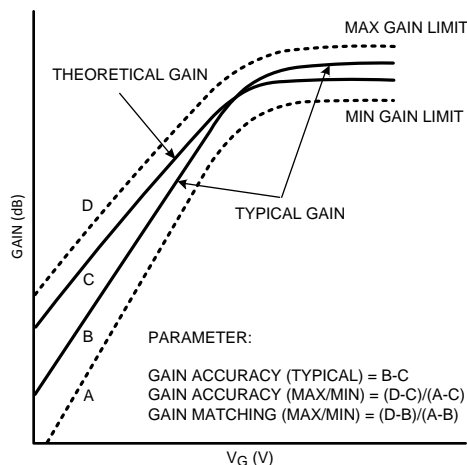


Figure 43. LMH6504 Gain Accuracy & Gain Matching Defined

**GAIN PARTITIONING**

If high levels of gain are needed, gain partitioning should be considered:

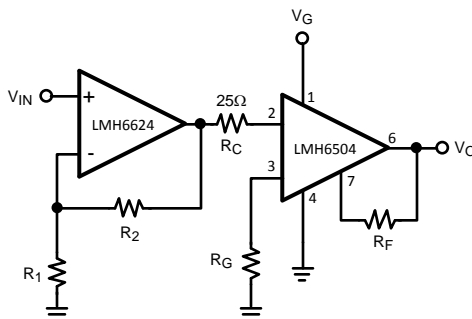


Figure 44. Gain Partitioning

The maximum gain range for this circuit is given by the following equation:

$$\text{MAXIMUM GAIN} = \left[ 1 + \frac{R_2}{R_1} \right] \cdot \left[ \frac{R_F}{R_G} \right] \cdot K \tag{4}$$

The LMH6624 is a low noise wideband voltage feedback amplifier. Setting  $R_2$  at 909Ω and  $R_1$  at 100Ω produces a gain of 20 dB. Setting  $R_F$  at 1000Ω as recommended and  $R_G$  at 50Ω, produces a gain of about 26 dB in the LMH6504. The total gain of this circuit is therefore approximately 46 dB. It is important to understand that when partitioning to obtain high levels of gain, very small signal levels will drive the amplifiers to full scale output. For example, with 46 dB of gain, a 20 mV signal at the input will drive the output of the LMH6624 to 200 mV, the output of the LMH6504 to 4V. Accordingly, the designer must carefully consider the contributions of each stage to the overall characteristics. Through gain partitioning the designer is provided with an opportunity to optimize the frequency response, noise, distortion, settling time, and loading effects of each amplifier to achieve improved overall performance.

## LMH6504 GAIN CONTROL RANGE AND MINIMUM GAIN

Before discussing Gain Control Range, it is important to understand the issues which limit it. The minimum gain of the LMH6504, theoretically, is zero, but in practical circuits is limited by the amount of feedthrough, here defined as the gain when  $V_G = 0V$ . Capacitive coupling through the board and package as well as coupling through the supplies will determine the amount of feedthrough. Even at DC, the input signal will not be completely rejected. At high frequencies feedthrough will get worse because of its capacitive nature. At frequencies below 10 MHz, the feed through will be less than  $-60$  dB and therefore, it can be said that with  $A_{VMAX} = 20$  dB, the gain control range is 80 dB.

## LMH6504 GAIN CONTROL FUNCTION

In the plot, Gain vs.  $V_G$ , we can see the gain as a function of the control voltage. The “Gain (V/V)” plot, sometimes referred to as the S-curve, is the linear (V/V) gain. This is a hyperbolic tangent relationship and is given by Equation 3. The “Gain (dB)” plots the gain in dB and is linear over a wide range of gains. Because of this, the LMH6504 gain control is referred to as “linear-in-dB.”

For applications where the LMH6504 will be used at the heart of a closed loop AGC circuit, the S-curve control characteristic provides a broad linear (in dB) control range with soft limiting at the highest gains where large changes in control voltage result in small changes in gain. For applications requiring a fully linear (in dB) control characteristic, use the LMH6504 at half gain and below ( $V_G \leq 1V$ ).

## AVOIDING OVERDRIVE OF THE LMH6504 GAIN CONTROL INPUT

There is an additional requirement for the LMH6504 Gain Control Input ( $V_G$ ):  $V_G$  must not exceed  $+2.3V$  (with  $\pm 5V$  supplies). The gain control circuitry may saturate and the gain may actually be reduced. In applications where  $V_G$  is being driven from a DAC, this can easily be addressed in the software. If there is a linear loop driving  $V_G$ , such as an AGC loop, other methods of limiting the input voltage should be implemented. One simple solution is to place a 2.2:1 resistive divider on the  $V_G$  input. If the device driving this divider is operating off of  $\pm 5V$  supplies as well, its output will not exceed 5V and through the divider  $V_G$  can not exceed 2.3V.

## IMPROVING THE LMH6504 LARGE SIGNAL PERFORMANCE

Figure 45 illustrates an inverting gain scheme for the LMH6504.

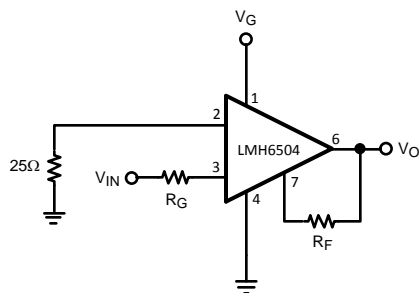


Figure 45. Inverting Amplifier

The input signal is applied through the  $R_G$  resistor. The  $V_{IN}$  pin should be grounded through a  $25\Omega$  resistor. The maximum gain range of this configuration is given in the following equation:

$$A_{VMAX} = - \left[ \frac{R_F}{R_G} \right] \cdot K \quad (5)$$

The inverting slew rate of the LMH6504 is much higher than that of the non-inverting slew rate. This 2X performance improvement comes about because in the non-inverting configuration, the slew rate of the overall amplifier is limited by the input buffer. In the inverting circuit, the input buffer remains at a fixed voltage and does not affect slew rate.

## TRANSMISSION LINE MATCHING

One method for matching the characteristic impedance of a transmission line is to place the appropriate resistor at the input or output of the amplifier. Figure 46 shows a typical circuit configuration for matching transmission lines.

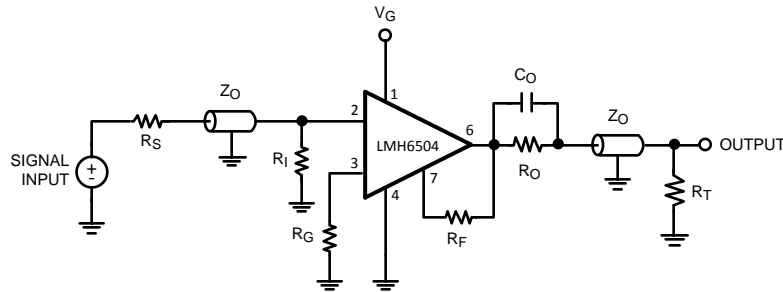


Figure 46. TRANSMISSION LINE MATCHING

The resistors  $R_S$ ,  $R_I$ ,  $R_O$ , and  $R_T$  are equal to the characteristic impedance,  $Z_O$ , of the transmission line or cable. Use  $C_O$  to match the output transmission line over a greater frequency range. It compensates for the increase of the op amp's output impedance with frequency.

## MINIMIZING PARASITIC EFFECTS ON SMALL SIGNAL BANDWIDTH

The best way to minimize parasitic effects is to use surface mount components and to minimize lead lengths and component distance from the LMH6504. For designs utilizing through-hole components, specifically axial resistors, resistor self-capacitance should be considered. Example: the average magnitude of parasitic capacitance of RN55D 1% metal film resistors is about 0.15 pF with variations of as much as 0.1 pF between lots. Given the LMH6504's extended bandwidth, these small parasitic reactance variations can cause measurable frequency response variations in the highest octave. We therefore recommend the use of surface mount resistors to minimize these parasitic reactance effects.

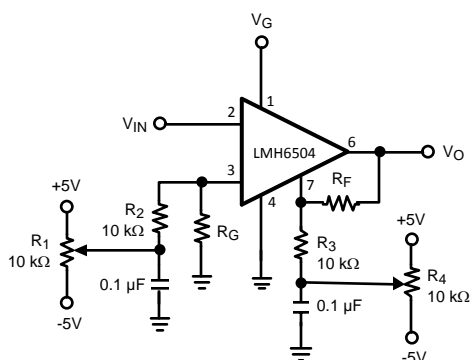
## RECOMMENDATIONS

Here are some recommendations to avoid problems and to get the best performance:

- Do not place a capacitor across  $R_F$ . However, an appropriately chosen series RC combination could be used to shape the frequency response.
- Keep traces connecting  $R_F$  separated and as short as possible
- Place a small resistor (20-50 $\Omega$ ) between the output and  $C_L$
- Cut away the ground plane, if any, under  $R_G$
- Keep decoupling capacitors as close as possible to the LMH6504.
- Connect pin 2 through a minimum resistance of 25 $\Omega$ .

## ADJUSTING OFFSETS AND DC LEVEL SHIFTING

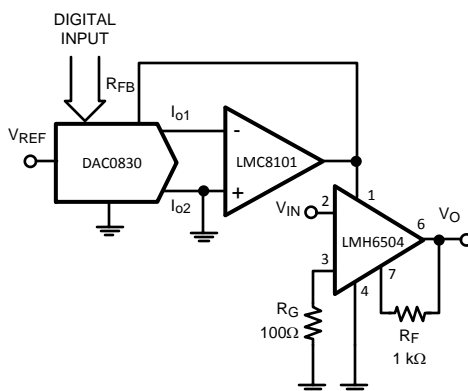
Offsets can be broken into two parts: an input-referred term and an output-referred term. These errors can be trimmed using the circuit in Figure 47. First set  $V_G$  to 0V and adjust the trim pot  $R_4$  to null the offset voltage at the output. This will eliminate the output stage offsets. Next set  $V_G$  to 2V and adjust the trim pot  $R_1$  to null the offset voltage at the output. This will eliminate the input stage offsets.



**Figure 47. OFFSET ADJUST CIRCUIT**

## DIGITAL GAIN CONTROL

Digitally variable gain control can be easily realized by driving the LMH6504's gain control input with a digital-to-analog converter (DAC). Figure 48 illustrates such an application. This circuit employs Texas Instruments' eight-bit DAC0830, the LMC8101 MOS input op-amp (Rail-to-Rail Input/Output), and the LMH6504 VGA. With  $V_{REF}$  set to 2V, the circuit provides up to 80 dB of gain control in 256 steps with up to 0.05% full scale resolution. The maximum gain of this circuit is 20 dB.



**Figure 48. Digital Gain Control**

## USING THE LMH6504 IN AGC APPLICATIONS

In AGC applications, the control loop forces the LMH6504 to have a fixed output amplitude. The input amplitude will vary over a wide range and this can be the issue that limits dynamic range. At high input amplitudes, the distortion due to the input buffer driving  $R_G$  may exceed that which is produced by the output amplifier driving the load. In the plot, Distortion vs. Gain, total harmonic distortion (THD) is plotted over a gain range of nearly 35 dB for a fixed output amplitude of  $0.25 V_{PP}$  in the specified configuration,  $R_F = 1k$ ,  $R_G = 100\Omega$ . When the gain is adjusted to -15 dB (i.e. 35 dB down from  $A_{VMAX}$ ), the input amplitude would be  $1.41 V_{PP}$  and we can see the distortion is at its worst at this gain. If the output amplitude of the AGC were to be raised above  $0.25 V_{PP}$ , the input amplitudes for gains 40 dB down from  $A_{VMAX}$  would be even higher and the distortion would degrade further. It is for this reason that we recommend lower output amplitudes if wide gain ranges are desired. Using a post-amp like the LMH6714/ 6720/ 6722 family or LMH6702 would be the best way to preserve dynamic range and yield output amplitudes much higher than  $100 mV_{PP}$ . Another way of addressing distortion performance and its limitations on dynamic range, would be to raise the value of  $R_G$ . Just like any other high-speed amplifier, by increasing the load resistance, and therefore decreasing the demanded load current, the distortion performance will be improved in most cases. With an increased  $R_G$ ,  $R_F$  will also have to be increased to keep the same  $A_{VMAX}$  and this will decrease the overall bandwidth. It may be possible to insert a series RC combination across  $R_F$  in order to counteract the negative effect on BW when a large  $R_F$  is used.

## AUTOMATIC GAIN CONTROL (AGC) #1

### Fast Response AGC Loop

The AGC circuit shown in [Figure 49](#) will correct a 6 dB input amplitude step in 100 ns. The circuit includes a two op-amp precision rectifier amplitude detector (U1 and U2), and an integrator (U3) to provide high loop gain at low frequencies. The output amplitude is set by  $R_9$ . Some notes on building fast AGC loops: Precision rectifiers work best with large output signals. Accuracy is improved by blocking DC offsets, as shown in [Figure 49](#).

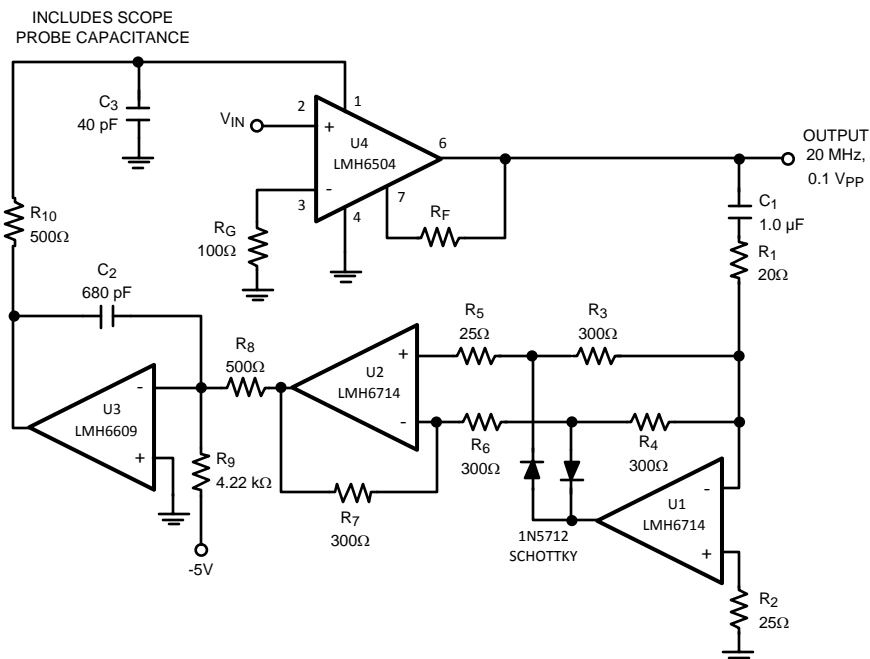


Figure 49. Automatic Gain Control Circuit #1

Signal frequencies must not reach the gain control port of the LMH6504, or the output signal will be distorted (modulated by itself). A fast settling AGC needs additional filtering beyond the integrator stage to block signal frequencies. This is provided in [Figure 49](#) by a simple R-C filter ( $R_{10}$  and  $C_3$ ); better distortion performance can be achieved with a more complex filter. These filters should be scaled with the input signal frequency. Loops with slower response time (longer integration time constants) may not need the  $R_{10} - C_3$  filter.

Checking the loop stability can be done by monitoring the  $V_G$  voltage while applying a step change in input signal amplitude. Changing the input signal amplitude can be easily done with an arbitrary waveform generator.

## AUTOMATIC GAIN CONTROL (AGC) #2

[Figure 50](#) illustrates an automatic gain control circuit that employs two LMH6504's. In this circuit, U1 receives the input signal and produces an output signal of constant amplitude. U2 is configured to provide negative feedback. U2 generates a rectified gain control signal that works against an adjustable bias level which may be set by the potentiometer and  $R_B$ .  $C_1$  integrates the bias and negative feedback. The resultant gain control signal is applied to the U1 gain control input  $V_G$ . The bias adjustment allows the U1 output to be set at an arbitrary level less than the maximum output specification of the amplifier. Rectification is accomplished in U2 by driving both the amplifier input and the gain control input with the U1 output signal. The voltage divider that is formed by  $R_1$  and  $R_2$ , sets the rectifier gain.

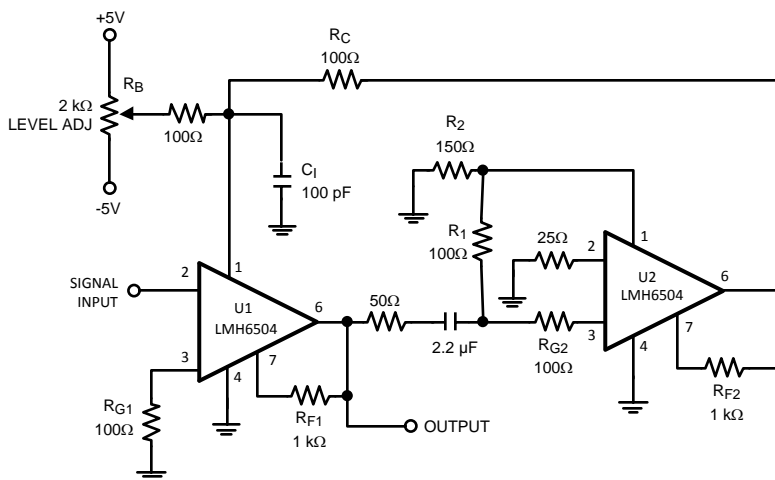


Figure 50. Automatic Gain Control Circuit #2

**CIRCUIT LAYOUT CONSIDERATIONS & EVALUATION BOARD**

A good high frequency PCB layout including ground plane construction and power supply bypassing close to the package are critical to achieving full performance. The amplifier is sensitive to stray capacitance to ground at the input (pin 7); keep node trace area small. Shunt capacitance across the feedback resistor should not be used to compensate for this effect. Capacitance to ground should be minimized by removing the ground plane from under the body of  $R_G$ . Parasitic or load capacitance directly on the output (pin 6) degrades phase margin leading to frequency response peaking.

The LMH6504 is fully stable when driving a 100Ω load. With reduced load (e.g. 1k.) there is a possibility of instability at very high frequencies beyond 400 MHz especially with a capacitive load. When the LMH6504 is connected to a light load as such, it is recommended to add a snubber network to the output (e.g. 100Ω and 39 pF in series tied between the LMH6504 output and ground).  $C_L$  can also be isolated from the output by placing a small resistor in series with the output (pin 6).

Component parasitics also influence high frequency results. Therefore it is recommended to use metal film resistors such as RN55D or leadless components such as surface mount devices. High profile sockets are not recommended.

Texas Instruments suggests the following evaluation board as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6504	SOIC	CLC730066

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**REVISION HISTORY**

<b>Changes from Revision C (March 2013) to Revision D</b>	<b>Page</b>
<hr/> <ul style="list-style-type: none"><li>• Changed layout of National Data Sheet to TI format .....</li></ul>	<hr/> <a href="#">20</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6504MA/NOPB	NRND	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH6504MA	
LMH6504MAX/NOPB	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH6504MA	
LMH6504MM/NOPB	NRND	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A93A	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6504MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6504MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6504MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6504MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

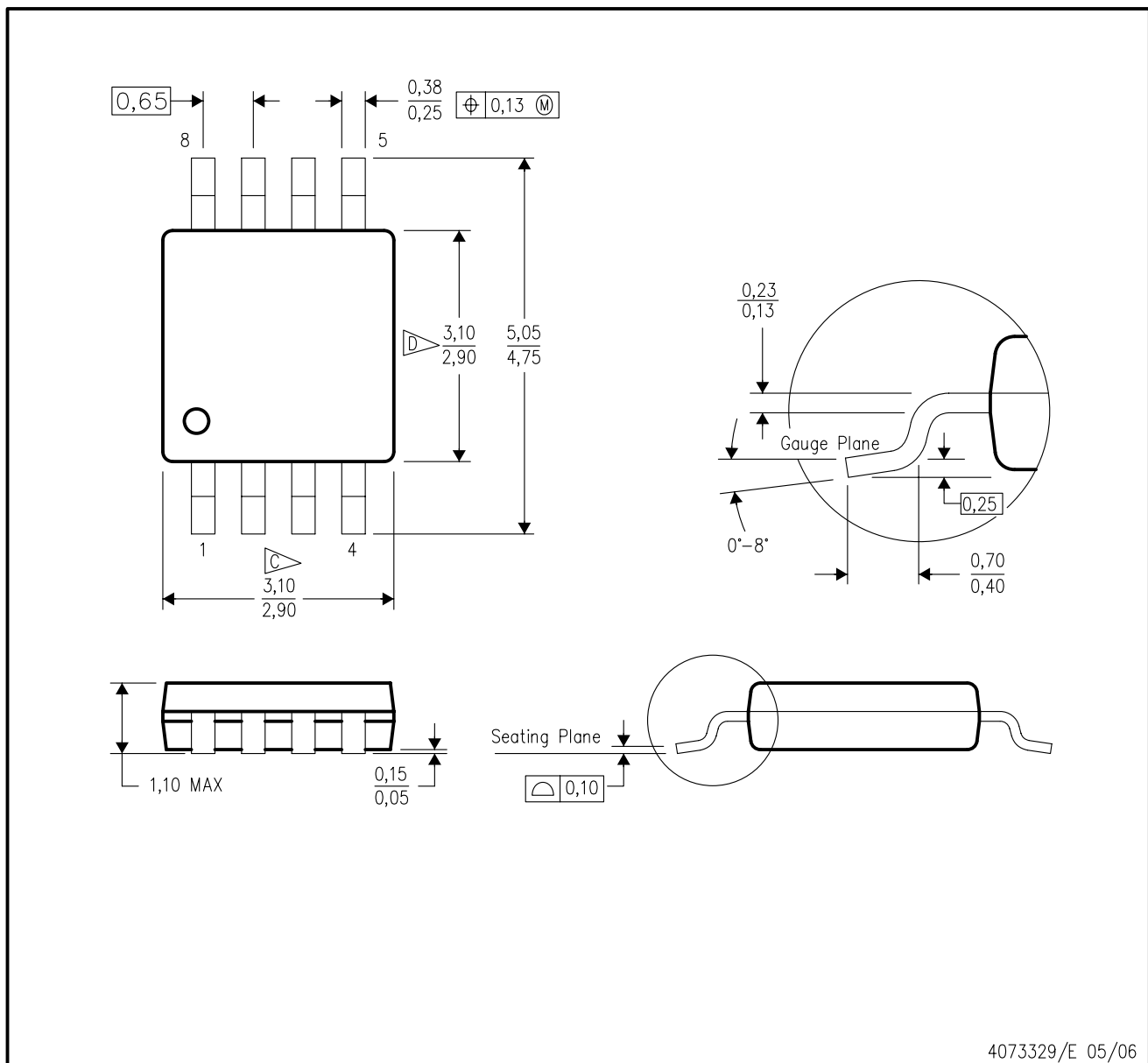
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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