THE DATASHEET OF

LMH1251MT/NOPB

LMH1251 YP_BP_R to RGBHV Converter and 2:1 Video Switch

Check for Samples: LMH1251

FEATURES

- **YP_BP_R to RGBHV Conversion**
- **YP_BP_R Path: 70 MHz, −3 dB, 700 mV_{PP} Bandwidth**
- **RGB Path: 400 MHz, −3 dB, 700 mV_{PP} Bandwidth**
- **Supports PC Video Display Resolutions up to UXGA (1600 x 1200 @ 75 Hz)**
- **Supports 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p**
- **Smart Video Format Detection for SD and HD**
- **Power Save Mode**

APPLICATIONS

- **TFT LCD Monitor**
- **CRT Monitor**
- **Set-Top Box**
- **Display Projector**

DESCRIPTION

The LMH1251 is a wideband 2:1 analog video switch with an integrated YP_BP_R to RGBHV converter. The device accepts one set of YP_BP_R inputs and one set of RGB/HSYNC/VSYNC inputs. Based on the input selected, the output will be either a decoded TV or buffered PC video signal.

The LMH1251 has a SYNC separator and processor that is capable of extracting sync timing information from both Standard Definition Television (SDTV) and High Definition Television (HDTV) inputs. It provides bi-level sync, and tri-level sync separation.

The color space conversion from YP_BP_R to RGB in the LMH1251 is realized with a very high precision fully analog dematrixer which provides superior chroma accuracy that is less than 2.5% of amplitude and 1.5° of phase error on a vectorscope. It is equipped with a smart video detection circuit which automatically senses SDTV and HDTV video formats and applies the appropriate color space conversion.

The LMH1251 is capable of handling SDTV, HDTV, XGA, SXGA, and UXGA video formats, which makes it an ideal solution for enhancing value in applications ranging from LCD monitors, to set-top boxes, to projectors. The LMH1251 is part of the LMH™ high speed amplifier family, and is offered in a 24-pin TSSOP package.

Connection Diagram

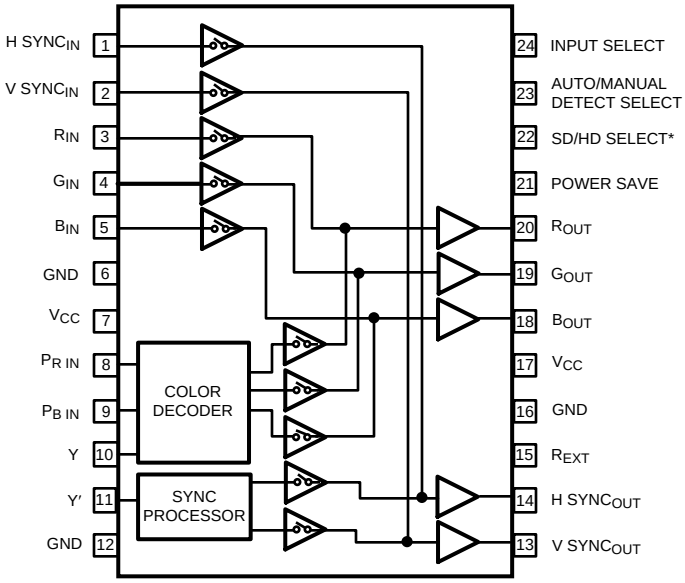


Figure 1. 24-Pin TSSOP - Top View
See PW Package

Truth Table-Input Select

Pin 24	OUT
0	RGBHV input Ch
1	YP_BP_R input Ch

Truth Table- Format/Conversion Select

Pin 23	Pin 22	SYNC	Format Detection	Conversion Scheme
0	0	Bi-Level	Manual	480i/480p
0	1	Tri-Level	Manual	720p/1080i
1	Outputs 0 (1)	Bi-Level	Auto	480i/480p
1	Outputs 1 (1)	Tri-Level	Auto	720p/1080i

(1) When Pin 23 is set high, the LMH1251 is in Auto Mode, in which it can detect the incoming video format (SD or HD) and apply the appropriate color conversion and sync processing. With Auto Mode, Pin 22 becomes an output pin, and will either output a logic high or low to notify the user of the format that is being detected by the LMH1251. If Pin 23 is set low, the LMH1251 is in Manual Mode, in which the user must specify the format with Pin 22. With Manual Mode, Pin 22 is an input pin. Since Pin 22 is a bi-directional pin, care must be given not to apply any voltages to it when it is in the Auto Mode, in which it functions as an output pin. The use of the Auto Mode with Pin 22 left floating is typically recommended.

Truth Table-Power Save

Pin 21	Low Power Mode
0	Disable
1	Enabled

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

ESD Tolerance	Susceptibility(4)	4.0 kV
	Machine Model (5)	400V
Supply Voltage V_{CC}, Pins 7 and 17		5.5V
Voltage at any Input Pin (V_{IN})		V_{CC} −0.5 ≥ V_{IN} ≥ 0V
Video Inputs (pk-pk)		0.0V ≤ V_{IN} ≤ 1.2V
Thermal Resistance to Ambient (θ_{JA})		110°C/W
Thermal Resistance to Case (θ_{JC})		25°C/W
Junction Temperature (T_J)		+150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (soldering 10 sec.)		265°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) All voltages are measured with respect to GND, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(5) The Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200 pF cap is charged to the specific voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

Operating Ratings (1)

Operating Temperature Range (2)	−20°C to +80°C
Supply Voltage (V_{CC})	4.75V ≤ V_{CC} ≤ 5.25V
RGB Video Inputs (pk-pk)	0.0V ≤ V_{IN} ≤ 0.7V
Y Video Inputs (incl. Sync)	-0.3V ≤ V_{IN} ≤ 0.7V
P_BP_R Video Inputs	-0.35V ≤ V_{IN} ≤ 0.35V

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. All video inputs must be properly terminated.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Video Signal Electrical Characteristics

Unless otherwise noted: T_A = 25°C, V_{CC} = +5.0V, RGB $Video_{IN}$ = 0.7 V_{PP}, Y $Video_{IN}$ = 0.7 V_{PP}, P_BP_R $Video_{IN}$ = ±350 mV, C_L = 8 pF, Video Outputs = 0.7 V_{PP}.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
$I_{S,\ RGB}$	Supply Current	No Output Loading, 80 kHz	28	34	41	mA
$I_{S,\ YP_BP_R}$	Supply Current	No Output Loading, 480p see (3)	60	70	80	mA
$I_{S\text{-}PS}$	Supply Current, Power Save Mode	Power Save Mode, No Output Loading, 80 kHz, see (3)	4	8	12	mA
I_{OUT}	Output Current			3		mA
$V_{O\ BLK}$	Typical DC Active Video Black Level Output Voltage		1.8	2.1	2.4	VDC
$Gain_{RGB}$	RGB Video Unity Gain	RGB $Video_{IN}$ = 0.7 V_{PP}		0.07		dB
Ch-Ch $Match_{RGB}$	RGB Ch to Ch Matching	RGB $Video_{IN}$ = 0.7 V_{PP}		0.02		dB
LE_{RGB}	RGB Input: Linearity Error	Staircase Input Signal see (4)		0		%
Video Time Domain Response						
RGB t_r	RGB Input: Video Rise Time	10% to 90%, AC Input Signal (5)		1.55		ns
RGB OS_R	RGB Input: Rising Edge Overshoot	AC Input Signal (5)		3		%
RGB t_f	RGB Input: Video Fall Time	90% to 10%, AC Input Signal (5)		1.55		ns
RGB OS_F	RGB Input: Rising Edge Overshoot	AC Input Signal (5)		3		%
SD YP_BP_R t_r	SD YP_BP_R Input: Video Rise Time	10% to 90%, AC Input Signal (5)		1.54		ns
RGB OSF	RGB Input: Falling Edge Overshoot	(5), AC Input Signal		3		%
SD YP_BP_R t_r	SD YP_BP_R Input: Video Rise Time	10% to 90%, AC Input Signal (5)		15.4		ns
SD YP_BP_R OS_R	SD YP_BP_R Input: Rising Edge Overshoot	AC Input Signal (5)		3		%
SD YP_BP_R t_f	SD YP_BP_R: Video Fall Time	90% to 10%, AC Input Signal (5)		15.4		ns
SD YP_BP_R OS_F	SD YP_BP_R: Falling Edge Overshoot	AC Input Signal (5)		3		%
HD YP_BP_R t_r	HD YP_BP_R Input: Video Rise Time	10% to 90%, AC Input Signal (5)		8.4		ns
HD YP_BP_R OS_R	HD YP_BP_R Input: Rising Edge Overshoot	AC Input Signal (5)		3		%
HD YP_BP_R t_f	HD YP_BP_R: Video Fall Time	90% to 10%, AC Input Signal (5)		8.4		ns
HD YP_BP_R OS_F	HD YP_BP_R: Falling Edge Overshoot	AC Input Signal (5)		3		%

(1) Datasheet min/max specification limits are specified by design, test, or statistical analysis. The ensured specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) The supply current specified is the quiescent current for V_{CC} and 5V with R_L = ∞. Load resistors are not required and are not used in the test circuit; therefore, all the supply current is used by the device.
(4) Linearity Error is the maximum variation in step height of a 16 step staircase input signal waveform with a 0.7 V_{PP} level at the input. All 16 are steps equal, with each at least 100 ns in duration.
(5) Input from RGB signal generator: t_r, t_f = 1.5 ns. Input from SDTV YP_BP_R signal generator: t_r, t_f = 15 ns. Input from HDTV YP_BP_R signal generator: t_r, t_f = 8 ns.

Video Signal Electrical Characteristics (continued)

Unless otherwise noted: T_A = 25°C, V_{CC} = +5.0V, RGB $Video_{IN}$ = 0.7 V_{PP}, Y $Video_{IN}$ = 0.7 V_{PP}, P_BP_R $Video_{IN}$ = ±350 mV, C_L = 8 pF, Video Outputs = 0.7 V_{PP}.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Video Frequency Domain Response						
RGB BW	RGB Input: Channel Bandwidth (−3 dB)	Large Signal BW		400		MHz
YP_BP_R BW	YP_BP_R Input (SD & HD): Channel Bandwidth (−3 dB)	Large Signal BW		70		MHz
$V_{SEP\ Ch\text{-}Ch}$ 10 MHz	Video Amplifier 10 MHz Isolation RGB Channel to Channel	(6)		−50		dB
$V_{SEP\ INPUT\text{-}INPUT}$ 10 MHz	Video Amplifier 10 MHz Isolation RGB Input to YP_BP_R Input	(6)		−55		dB
SNR	Signal to Noise Ratio	AC Input Signal, C_L = 8 pF (6)		55		dB

(6) Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for V_{SEP} 10 MHz.

Color Conversion Accuracy

Unless otherwise noted: T_A = 25°C, V_{CC} = +5.0V, Y $Video_{IN}$ = 0.7 V_{PP}, P_BP_R $Video_{IN}$ = ±350 mV, C_L = 8 pF, Video Outputs = 0.7 V_{PP}.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
$V_{COLOR\ ERROR}$	$\lvert P_BP_R \rvert$ Amplitude (Calculated from RGB Outputs)	YP_BP_R Video Input, 100% Color Bar (any 3 colors), (3)		±0.3	±2.5	%
$\theta_{COLOR\ ERROR}$	P_BP_R Phase Angle (Calculated from RGB Outputs)	YP_BP_R Video Input, 100% Color Bar (any 3 colors), (3)		±0.2	±1.5	deg

(1) Datasheet min/max specification limits are specified by design, test, or statistical analysis. The ensured specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Any three color bar signals can be used as test signals. The RGB outputs shall be used to calculate the amplitudes and phases of the chroma results. These should fall within the limits specified.

Sync Signal Electrical Characteristics

Unless otherwise noted: T_A = 25°C, V_{CC} = +5.0V, Y $Video_{IN}$ = 0.7 V_{PP}, P_BP_R $Video_{IN}$ = ±350 mV, C_L = 8 pF, Video Outputs = 0.7 V_{PP}.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{SYNCL}	H & V SYNC Low Input	Pins 1 & 2	−0.5		1.5	V
V_{SYNCH}	H & V SYNC High Input	Pins 1 & 2	3.0		V_{CC} +0.5	V
$I_{O\text{-}SYNCH}$	H & V SYNC Current Sink/Source Capability	5 kΩ Load		3		mA
$t_{R/F\text{-}SYNC}$	H & V SYNC Rise/Fall Time			15		ns
$t_{SYNC\text{-}WIDTH}$	H & V SYNC Width Error Relative to H & V SYNC Input	H & V SYNC Input		5		%
$t_{Y\text{-}SYNC\text{-}WIDTH}$	H & V SYNC Width Error Relative to Composite SYNCS on Y	Composite SYNC on Y Input		5		%
$t_{SYNC\text{-}DELAY}$	50% of H & V SYNC Input to Output	H & V SYNC Input		40		ns
$t_{Y\text{-}HSYNC\text{-}DELAY}$	50% of H SYNC Input to Output	Composite SYNC on Y Input (Not During Vertical Period)		70		ns

(1) Datasheet min/max specification limits are specified by design, test, or statistical analysis. The ensured specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

System Interface Signal Characteristics

Unless otherwise noted: $_{TA}$ = 25°C, V_{CC} = +5.0V, Y $Video_{IN}$ = 0.7 V_{PP}, P_BP_R $Video_{IN}$ = ±350 mV, C_L = 8 pF, Video Outputs = 0.7 V_{PP}.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{IL}	Logic Low Input Voltage (Pins 24, 23, 22, 21)		−0.5		1.5	V
V_{IH}	Logic High Input Voltage (Pins 24, 23, 22, 21)		3.0		V_{CC} +0.5	V
I_L	Logic Low Input Current (Pins 24, 23, 22, 21)	Input Voltage = 0.4V		±10		µA
I_H	Logic High Input Current (Pins 24, 23, 22, 21)	Input Voltage = 0.4V		±10		µA
V_{OL}	Logic Low Output Voltage (Pins 24, 23, 22, 21)	I_O = 3 mA		0.5		V

(1) Datasheet min/max specification limits are specified by design, test, or statistical analysis. The ensured specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

Typical Performance Characteristics

Unless otherwise noted: T_A = 25°C, V_{CC} = +5.0V, RGB $Video_{IN}$ = 0.7 V_{PP}, Y $Video_{IN}$ = 0.7 V_{PP}, P_BP_R $Video_{IN}$ = ±350 mV, C_L = 8 pF, Video Outputs = 0.7 V_{PP}.

Large Signal Frequency Response

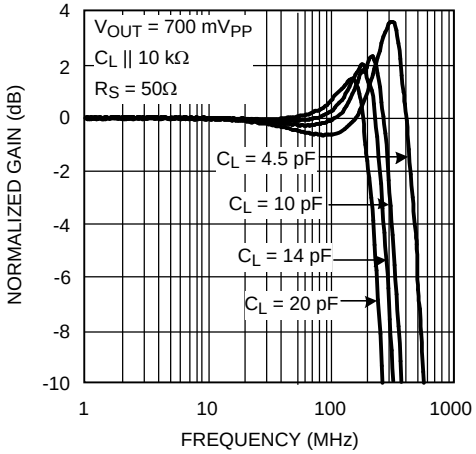


Figure 2.

Crosstalk vs. Frequency

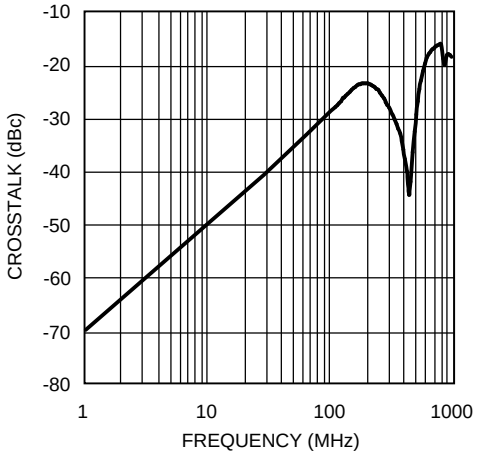


Figure 3.

Pulse Response

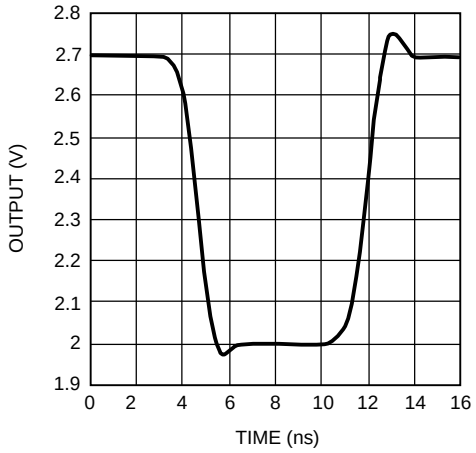


Figure 4.

Harmonic Distortion vs. Frequency

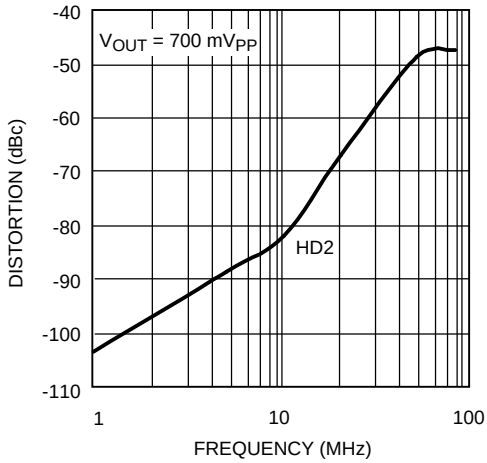


Figure 5.

720p Color Bar Vectorscope

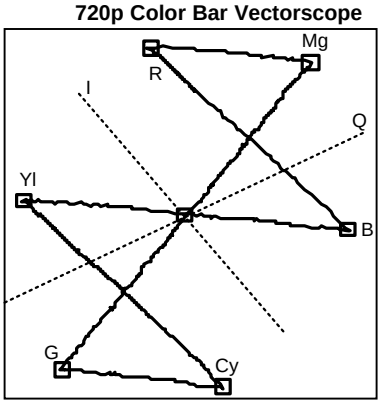


Figure 6.

APPLICATION INFORMATION

GENERAL INFORMATION

The LMH1251 is a high speed triple 2:1 video multiplexer with an integrated sync processor and color space converter. One input channel accepts standard RGBHV PC graphics video and the second input channel accepts YP_BP_R component video. If the first input of the MUX is selected, the device will output the RGBHV video from the input with unity gain. If the second input of the MUX is selected, sync processing and color space conversion will be performed on the YP_BP_R component signals to provide an equivalent RGBHV signal at the output.

YP_BP_R to RGBHV PROCESSING

The LMH1251 is capable of processing 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p YP_BP_R component video signals only. S-Video, composite NTSC, or composite PAL video will not be converted by the LMH1251. For High Definition, 720p and 1080i/1080p video, the LMH1251 will convert the luma and chroma signals into primary RGB signals according to the linear arithmetic formula specified in the EIA/CEA-770.3-C Standard for High Definition Analog Component TV. For Standard Definition video, the LMH1251 will perform the conversion according to the linear arithmetic formula specified in the EIA/CEA-770.2-C Standard for Standard Definition Analog Component TV. The advanced analog architecture that is employed to perform the color space conversion is precise to within 2.5% of amplitude and 1.5° of phase error on a vectorscope with a color bar test signal. This is illustrated with a vectorscope plot of a converted color bar signal in the 720p format shown Typical Performance Characteristics.

Note that although 480i/576i component video is supported by the LMH1251, most PC display monitors cannot handle such line rates. Typically, only 480p, 576p, 720p, and 1080i/1080p are within the displayable line rate range of LCD and CRT monitors. Furthermore, the scaler in LCD monitor systems must include a de-interlacer for it to display interlaced video such as with 1080i.

Component Video Formats Supported By The LMH1251

- 480i*
- 480p
- 576i*
- 576p
- 720p
- 1080i at 25, 29.97, and 30 Hz frame rate
- 1080p at 25, 29.97, and 30 Hz frame rate

NOTE

***These formats with Macrovision are not supported. See MACROVISION COMPATIBILITY for more information.**

AUTO/MANUAL FORMAT DETECTION

The LMH1251 can either automatically detect the input format of the component video source, or it can be put in a manual mode where the MCU has the flexibility to specify which YP_BP_R to RGBHV processing scheme for the device to apply depending on the input format. If a logic high is applied to Pin 23, the LMH1251 will be in the AUTO detection mode, which is typically recommended. In this mode, the device will appropriately use the proper YP_BP_R to RGB processing scheme based on its input format detection. If a logic low is applied to Pin 23, the LMH1251 will be in the manual detection mode. In this mode, the MCU must apply a logic low to Pin 22 if the processing scheme is for SDTV video formats, and a logic high if the processing scheme is for HDTV formats.

Note that in the AUTO mode, Pin 22 becomes an output pin, and outputs a logic low if an SD video input is detected and a logic high if an HD video input is detected, as notification to the MCU.

MACROVISION COMPATIBILITY

The LMH1251 is compatible with the Macrovision Video Copy Protection System commonly used in 480p/576p progressive-scan DVD video sources. The LMH1251 does not support 480i/576i formats with Macrovision enabled. Macrovision, which is enabled by special circuitry inside many DVD players, embeds pseudo sync pulses and pseudo video pulses into the source signal during the vertical blanking interval. This system is intended to prohibit and deter analog video recording.

For 480p/576p formats with Macrovision enabled, the internal sync processor of the LMH1251 will output the true H sync pulses only and effectively ignore the pseudo sync pulses; its video processor will apply proper SDTV color space conversion, and the pseudo video pulses will pass through to comply with Macrovision.

POWER SAVE MODE

The LMH1251 is equipped with a power saving mode which is controlled by Pin 21. This pin is a logic level input. The device will enter a low power mode when the power save pin is applied with a logic high by the MCU. Under these conditions, the IC reduces its current consumption to a minimum as specified in Video Signal Electrical Characteristics. However, the sync processor and switch will always remain active. During power save mode, the RGB video outputs are held to the blank level, while the sync signals are allowed to continue to be processed and/or passed through. Based on the absence or presence of sync signals at the output of the LMH1251, the MCU can determine whether to bring the system to a low power consumption state.

INTERNAL VOLTAGE REFERENCE

Proper operation of the LMH1251 requires a very accurate reference voltage. This voltage is generated in the V_{REF} block. The output of the V_{REF} stage goes to a number of blocks in the video sections and sets the internal bias. To insure an accurate voltage over temperature, an external resistor is used to set the current in the V_{REF} stage. The external resistor is connected to Pin 15. This resistor should be 1% and have a temperature coefficient under 100 ppm/°C.

H SYNC AND V SYNC CHARACTERISTICS

When the RGBHV input is selected, the LMH1251 will produce H and V sync output signals of the same sync polarities as the H and V sync input signals. For example, VESA standard timing input signals with positive, leading edge sync pulses will produce positive, leading edge pulses in the H and V sync output signals. However when the YP_BP_R input is selected, both sync outputs are always positive, leading edge syncs, set by the internal sync processor.

Display systems typically sync lock to negative edges of H and V sync signals, and some displays may have polarity correction to accommodate either positive or negative edges. Logic inverters can be used to invert the H and V sync output signals of the LMH1251 to satisfy the negative edge requirement.

It is worth noting that when YP_BP_R is selected with an SDTV input format, some H sync output pulses will be half the width of the normal H sync pulses due to the narrow equalization pulses in the vertical blanking interval. When the H sync signal changes from full to half width pulses, or vice versa, the H sync period or scan rate changes with respect to the negative sync edges. These brief changes in the H sync period may cause a negative-edge triggered horizontal PLL to lose sync lock momentarily, which can cause the on-screen picture to distort or blank repeatedly. This condition can be rectified using a logic inverter to produce negative, leading edge H sync pulses. When the inverted H sync signal changes from full to half width pulses, or vice versa, the H sync period will remain constant with respect to the negative edges, which is correct H sync operation for negative-edge triggered displays.

OUTPUT DRIVE CHARACTERISTICS

The LMH1251 is designed to interface with an ADC or preamplifier through an AC coupling capacitor as shown below in Figure 7. The RGB outputs of the LMH1251 are 700 mV_{PP} video signals with the black level at approximately 2.1V (typ), which is the chip's internal voltage reference level. The H sync and V sync output signals are CMOS logic outputs that swing rail-to-rail.

The RGBHV outputs cannot be used to drive standard 150Ω video loads and require high-bandwidth buffers for this kind of application. For example, if the LMH1251 is to be designed into a stand-alone converter box application, the configuration in Figure 8 is recommended. To drive a display monitor over a standard VGA cable, a wideband, low distortion triple video buffer, such as the LMH6739, can be used with a gain of +2 to drive the RGB video signals of the LMH1251, and logic inverters can be used to drive its H and V sync signals.

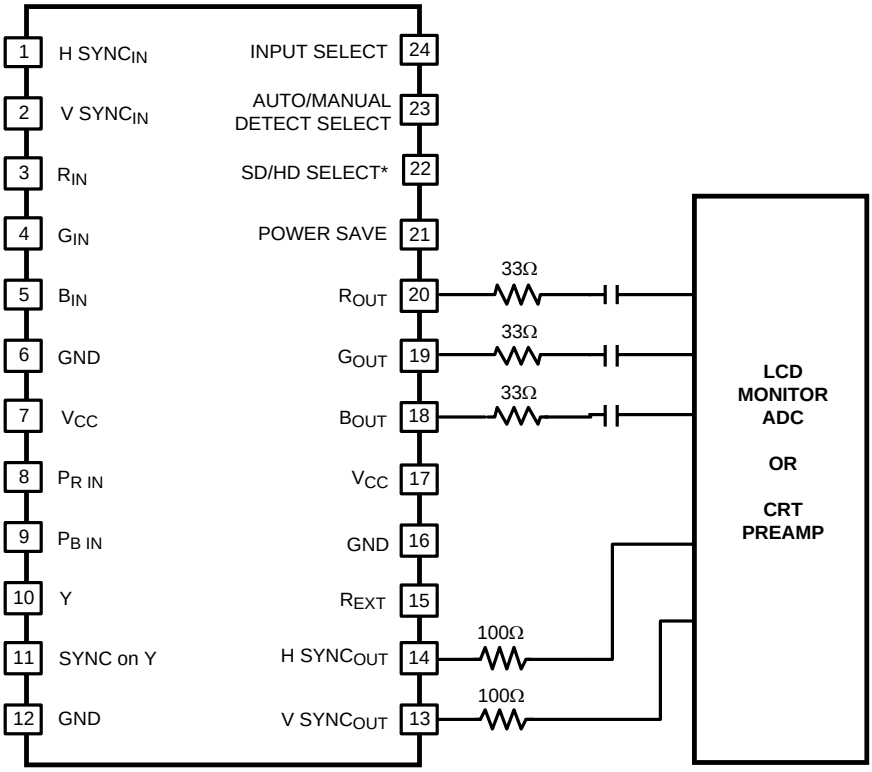


Figure 7. Typical LMH1251 Application

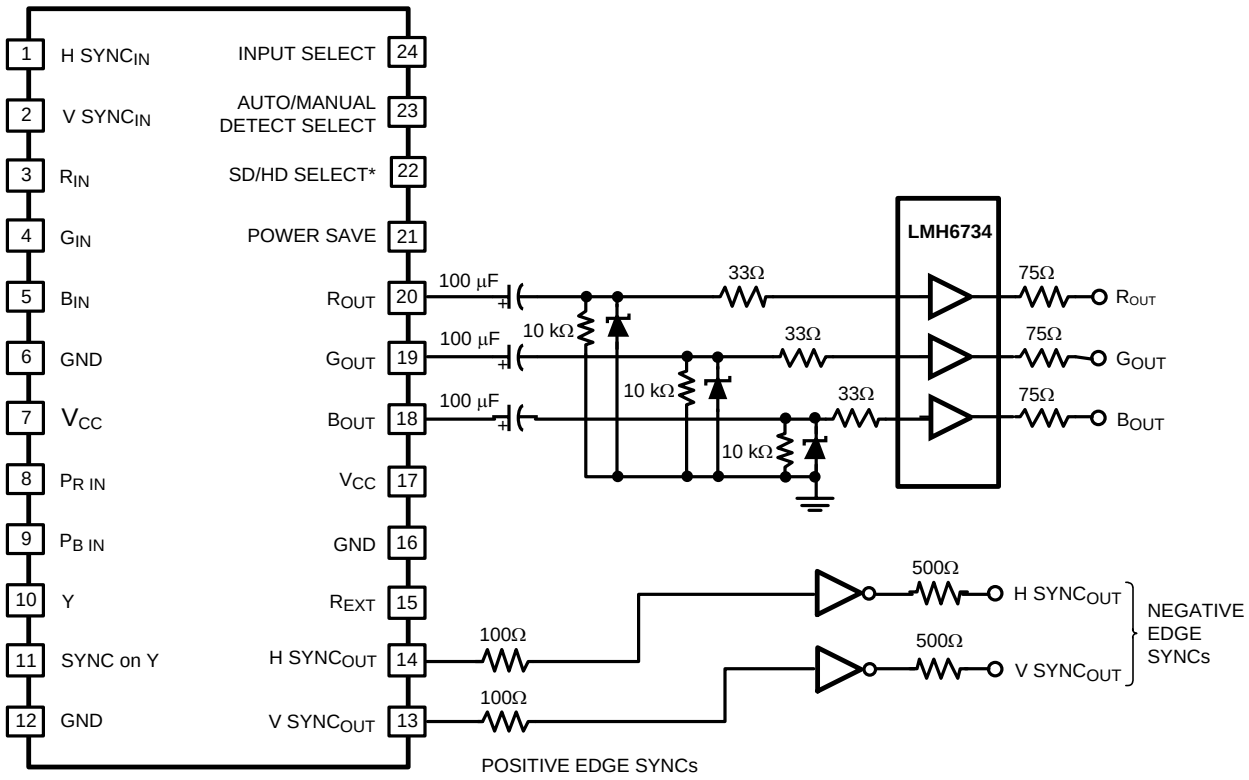


Figure 8. Simplified Application Diagram for Driving a VGA Cable

LAYOUT CONSIDERATIONS

The most important point to note regarding the layout of the LMH1251 on a PCB is that the trace length between the output pins of the LMH1251 and the input AC coupling capacitors of the next stage ADC or preamplifier must be as minimal as possible. The trace lengths of the H Sync and V Sync outputs should also be minimized, as the capacitive loading on these outputs must not exceed 6 pF. For long signal paths leading up to the input of the LMH1251, controlled impedance lines should be used, along with impedance matching elements. Bypass capacitors should be placed as close as possible to the supply pins of the device. The larger electrolytic bypass capacitor can be located farther from the device. The 10 kΩ external resistor should also be placed as close as possible to the R_{EXT} pin. All video signals must be kept away from the R_{EXT} pin (15). This pin has a very high input impedance and will pick up any high frequency signals routed near it.

Test Circuit

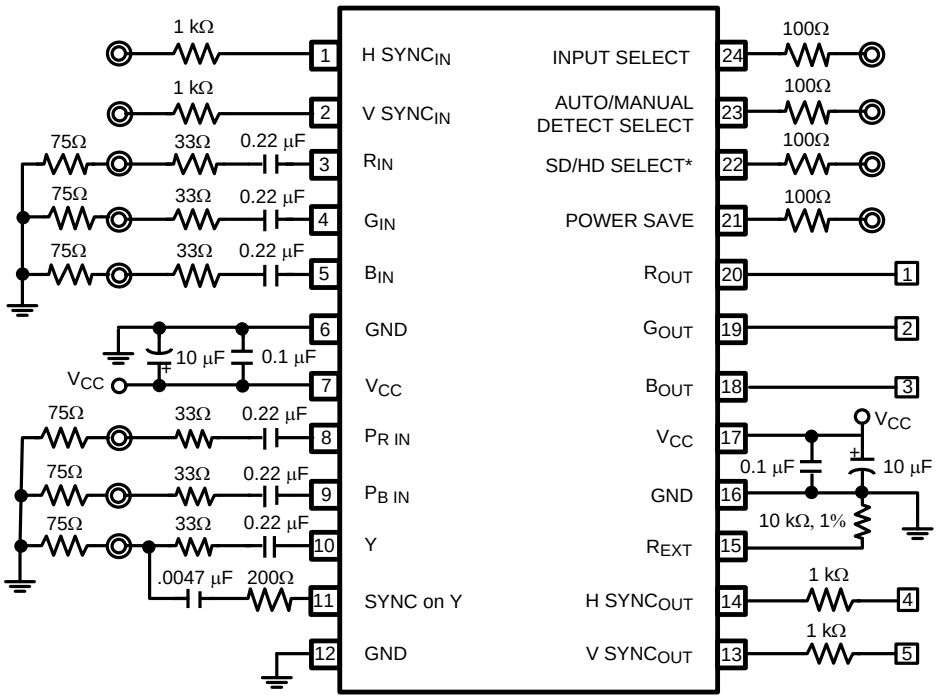


Figure 9. Test Circuit

REVISION HISTORY

Changes from Revision I (March 2013) to Revision J	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH1251MT/NOPB	ACTIVE	TSSOP	PW	24	61	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LMH1251 MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

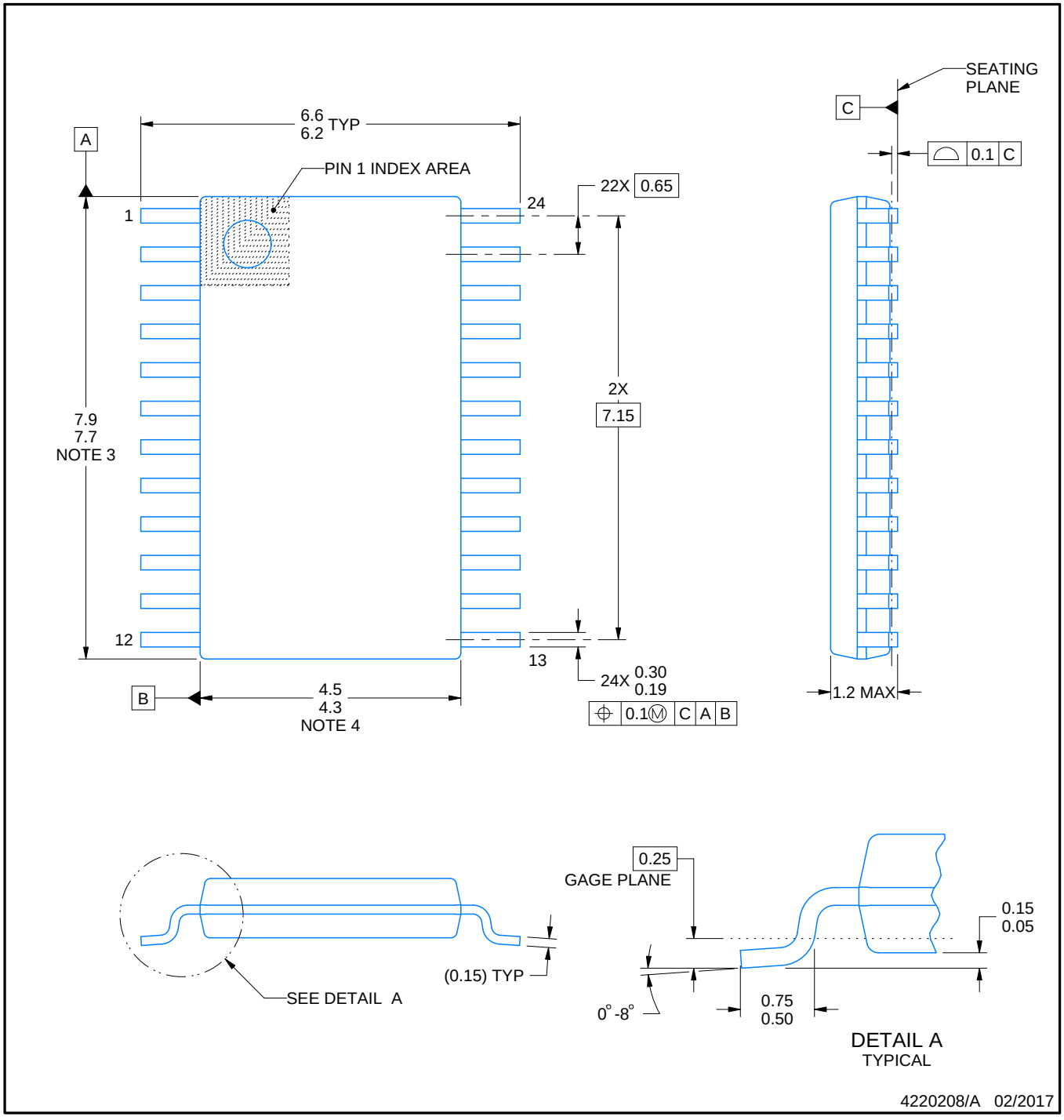
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

PW0024A

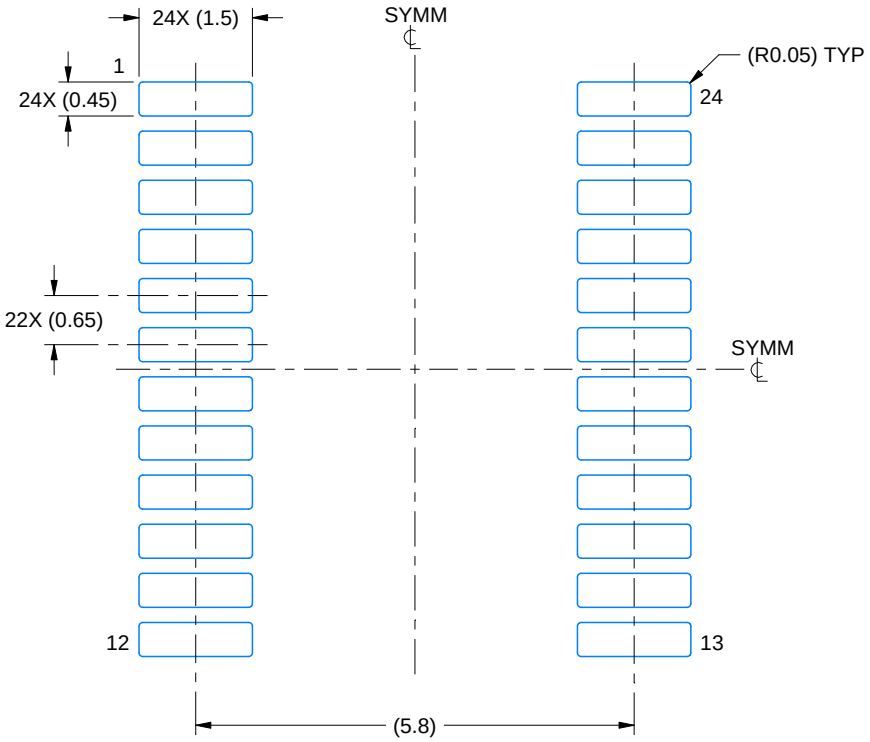
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

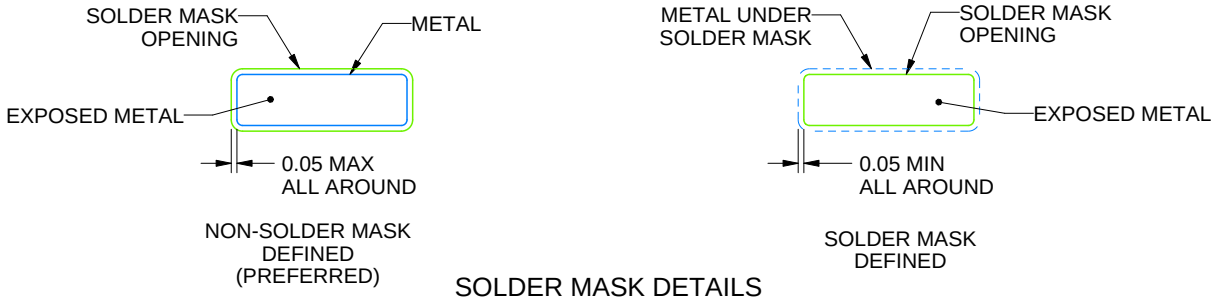


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

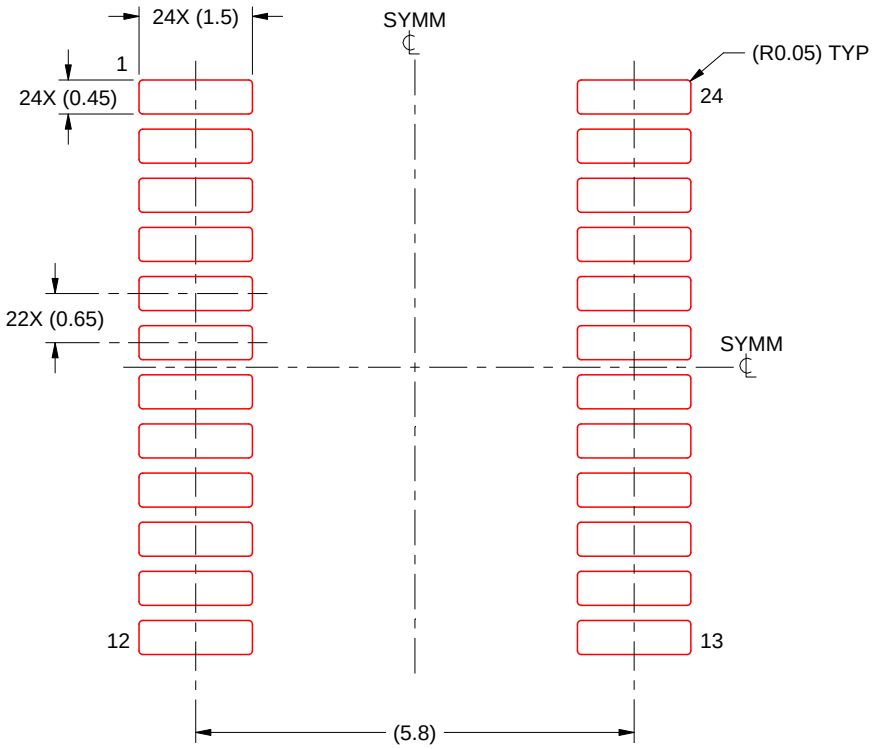


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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