THE DATASHEET OF

LM96163CISD/NOPB

www.win-source.net 0086-755-83957316

LM96163 Remote Diode Digital Temperature Sensor with Integrated Fan Control and TruTherm® BJT Transistor Beta Compensation Technology

Check for Samples: LM96163

FEATURES

- **TruTherm BJT Beta Compensation Technology Supports 45nm, 65nm and 90nm Processor Remote Diodes**
- **Factory Trimmed for Intel® 45 nm Processor Thermal Diodes**
- **Accurately Senses Diode-Connected 2N3904 Transistors or Thermal Diodes On-board Large Processors or ASIC's**
- **Accurately Senses its Own Temperature**
- **Integrated PWM Fan Speed Control Output Supports High Resolution at 22.5kHz Frequency for 4-pin Fans**
- **Acoustic Fan Noise Reduction with User-Programmable 12-Step Lookup Table**
- **LUT Transition Fine Resolution Smoothing Function**
- **Tachometer Input for Measuring Fan RPM**
- **Smart-Tach Modes for Measuring RPM of Fans with Pulse-Width-Modulated Power as Shown in Typical Application**
- **$\overline{\text{ALERT}}$ Output for Processor Event Notification**
- **$\overline{\text{TCRIT}}$ Output for Critical Temperature System Shutdown**
- **Offset Register Can Adjust for a Variety of Thermal Diodes**
- **10-Bit Plus Sign and 11-Bit Unsigned Formats, with 1/8°C Resolution**
- **Extended Resolution to 1/32°C when Digital Filter Enabled**
- **Resolves Remote Diode Temperatures up to 255.875°C**
- **SMBus 2.0 Compatible Interface, with TIMEOUT and ARA**
- **10-Pin SON Package**

APPLICATIONS

- **Processor Thermal Management**
- **Electronic Test and Office Equipment**
- **Industrial Controls**

DESCRIPTION

The LM96163 has remote and local temperature sensors with integrated fan control that includes TruTherm BJT transistor beta compensation technology for remote diode sensing. The LM96163 accurately measures: (1) its own temperature and (2) the temperature of a diode-connected transistor, such as a 2N3904, or a thermal diode commonly found on Computer Processors, Graphics Processor Units (GPU) and other ASIC's. The LM96163 has an offset register to correct for errors caused by different non-ideality factors of other thermal diodes.

The LM96163 also features an integrated, pulse-width-modulated (PWM), open-drain fan control output. Fan speed depends on a combination of the remote temperature reading, the lookup table and register settings. The 12-step Lookup Table (LUT) enables the user to program a non-linear fan speed vs. temperature transfer function often used to quiet acoustic fan noise. In addition a fully programmable ramping function has been added to allow smooth transitions between LUT setpoints.

Table 1. Key Specifications

■ Remote Temp Accuracy (includes quantization error)		
LM96163 Temp	**DiodeTemp**	**Max Error**
+25 to +85°C	+50 to +105°C	±0.75°C
+25 to +85°C	+40 to +125°C	±1.5°C
-40 to +25°C	+25 to 125°C	±3.0°C
■ Local Temp Accuracy (includes quantization error)		
LM96163 Temp 25°C to 125°C		±3.0°C (max)
■ Supply Voltage		+3.0 V to +3.6 V
■ Supply Current (0.8Hz Conversion)		456 µA (typ)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2008–2013, Texas Instruments Incorporated

Connection Diagrams

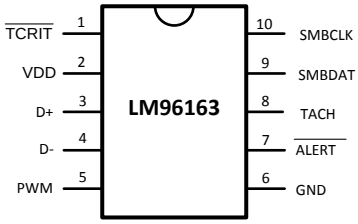


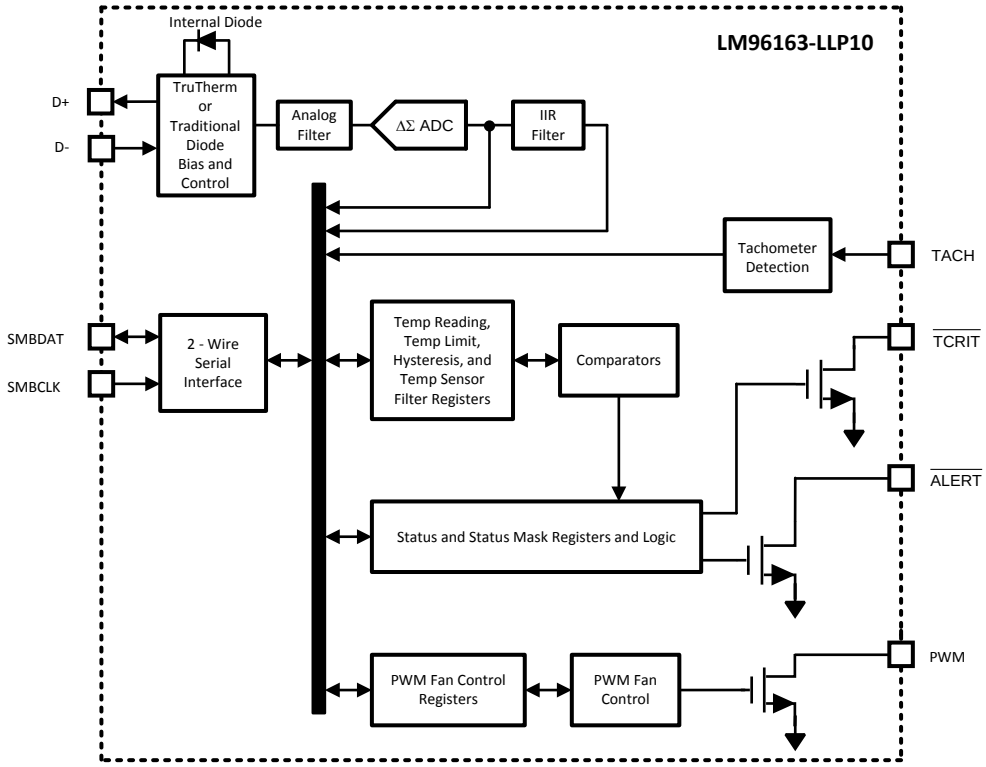
Figure 1. 10-Pin SON (TopView)
See DSC0010A Package

Pin Descriptions

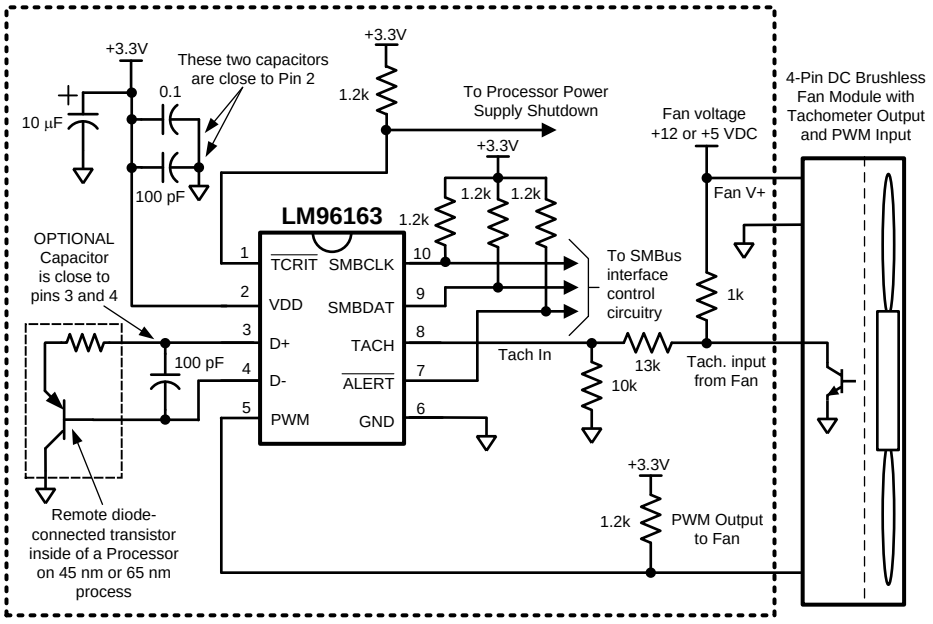
Pin	Name	Input/Output	Function and Connection
1	$\overline{\text{TCRIT}}$	Open-Drain Digital Output	Open-Drain Digital Output. Connect to system shutdown. Pin activates when temperature conversion value exceeds programmed limit. Several power-on-default limit values are available.
2	V_{DD}	Power Supply Input	Connect to a low-noise +3.3 ± 0.3 V_{DC} power supply, and bypass to GND with a 0.1 µF ceramic capacitor in parallel with a 100 pF ceramic capacitor. A bulk capacitance of 10 µF needs to be in the vicinity of the LM96163's V_{DD} pin.
3	D+	Analog Input	Connect to the anode (positive side) of the remote diode. A 100pF capacitor can be connected between pins 3 and 4.
4	D−	Analog Input	Connect to the cathode (negative side) of the remote diode. A 100pF capacitor can be connected between pins 3 and 4.
5	PWM	Open-Drain Digital Output	Open-Drain Digital Output. Connect to fan drive circuitry. The power-on default for this pin is low (pin 4 pulled to ground).
6	GND	Ground	This is the analog and digital ground return.
7	$\overline{\text{ALERT}}$	Open-Drain Digital Output	This pin is an open-drain $\overline{\text{ALERT}}$ output.
8	TACH	Digital Input	Tachometer input for measuring fan speed. Note the TACH input is disabled upon power-up and needs to be enabled for use by setting TCHEN bit 2 of Configuration Register 03h.
9	SMBDAT	Digital Input/ Open-Drain Digital Output	This is the bidirectional SMBus data line.
10	SMBCLK	Digital Input	Digital Input. This is the SMBus clock input.

Copyright © 2008–2013, Texas Instruments Incorporated

Simplified Block Diagram



Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

Supply Voltage, V_{DD}		−0.3 V to 6.0 V
Voltage on SMBDAT, SMBCLK, $\overline{ALERT}$, $\overline{TCRIT}$, TACH, PWM Pins		−0.5 V to 6.0 V
Voltage on Other Pins		−0.3 V to (V_{DD} + 0. 3 V)
Input Current, D− Pin (4)		±1 mA
Input Current at All Other Pins (4)		5 mA
Package Input Current (4)		30 mA
SMBDAT, $\overline{ALERT}$, PWM pins		
Output Sink Current		10 mA
Package Power Dissipation		See (5)
Junction Temperature		125°C
Storage Temperature		−65°C to +150°C
ESD Susceptibility (6)	Human Body Model	2500 V
	Machine Model	250 V
	Charged Device Model	1000 V

(1) All voltages are measured with respect to GND, unless otherwise noted.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V+), the current at that pin should be limited to 5 mA. Parasitic components and/or ESD protection circuitry are shown below for the LM96163's pins. Care should be taken not to forward bias the parasitic diode, D2, present on pins D+ and D−. Doing so by more than 50 mV may corrupt temperature measurements.
(5) Thermal resistance junction to ambient when attached to a 2 layer 4"x3" printed circuit board with copper thickness of 2oz. as described in JEDEC specification EIA/JESD51-3 is 137°C/W. Thermal resistance junction to ambient when attached to a 4 layer 4"x3" printed circuit board with copper thickness 2oz./1oz./1oz/2oz. and 4 thermal vias as described in JEDEC specification EIA/JESD51-7 is 40.3°C/W.
(6) Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin. Charged Device Model (CDM) simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.

Operating Ratings (1)(2)(3)(4)

Specified Temperature Range ($T_{MIN} \le T_A \le T_{MAX}$)	LM96163CISD	–40°C ≤ T_A ≤ +85°C
Remote Diode Temperature Range		-40°C ≤ T_D ≤ +140°C
Supply Voltage Range (V_{DD})		+3.0 V to +3.6 V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND, unless otherwise noted.
(3) *Soldering process must comply with Reflow Temperature Profile specifications. Refer to* www.ti.com/packaging
(4) Reflow temperature profiles are different for packages containing lead (Pb) than for those that do not.

Copyright © 2008–2013, Texas Instruments Incorporated

DC Electrical Characteristics

TEMPERATURE-TO-DIGITAL CONVERTER CHARACTERISTICS

The following specifications apply for V_{DD} = 3.0 VDC to 3.6 VDC, and all analog source impedance R_S = 50Ω unless otherwise specified in the conditions. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits T_A = +25°C; unless otherwise noted. T_D is the junction temperature of the remote thermal diode. T_J is the junction temperature of the LM96163.

Parameter	Conditions		Typical[1]	Limits[2]	Units (Limits)
Temperature Error Using the Remote Thermal Diode of an Intel Processor on 45nm.[3]	T_A = +25°C to +85°C	T_D = +50°C to +105°C T_D = Remote Diode Junction Temperature		**±0.75**	°C (max)
	T_A = +25°C to +85°C	T_D = +40°C to +125°C		**±1.5**	°C (max)
	T_A = -40°C to +25°C	T_D = +25°C to +125°C		**±3.0**	°C (max)
Temperature Error Using the Local Diode. See[4] & [5] for the thermal resistance to be used in the self-heating calculation.	T_A = +25°C to +125°C		±1	**±3**	°C (max)
	T_A = -40°C to +25°C			**±6**	°C (max)
Remote Diode Resolution			11		Bits
			0.125		°C
Local Diode Resolution			8		Bits
			1		°C
Conversion Time, All Temperature Channels	Fastest Setting		38.3	**41.1**	ms (max)
D− Source Voltage			0.4		V
Diode Source Current	(V_{D+} − V_{D-}) = +0.65 V; High Current		172	**225**	µA (max)
				100	µA (min)
	Low Current		10.75		µA
Diode Source Current Ratio			16		

(1) "Typicals" are at T_A = 25°C and represent most likely parametric norm. They are to be used as general reference values not for critical design calculations.
(2) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(3) The accuracy of the LM96163 is guaranteed when using a typical thermal diode of an Intel processor on a 45 nm process, as selected in the Remote Diode Model Select register. See Typical Performance Characteristics for performance with Intel processor on 65 nm or 90 nm process.
(4) Local temperature accuracy does not include the effects of self-heating. The rise in temperature due to self-heating is the product of the internal power dissipation of the LM96163 and the thermal resistance.
(5) Thermal resistance junction to ambient when attached to a 2 layer 4"x3" printed circuit board with copper thickness of 2oz. as described in JEDEC specification EIA/JESD51-3 is 137°C/W. Thermal resistance junction to ambient when attached to a 4 layer 4"x3" printed circuit board with copper thickness 2oz./1oz./1oz/2oz. and 4 thermal vias as described in JEDEC specification EIA/JESD51-7 is 40.3°C/W.

Operating Electrical Characteristics

Symbol	Parameter	Conditions	Typ[1]	Limits[2]	Units
V_{POR}	Power-On-Reset Threshold Voltage			**2.8**	V (max)
				1.6	V (min)
I_S	Supply Current[3]	SMBus Inactive, 13 Hz Conversion Rate	1.1	**1.6**	mA (max)
		SMBus Inactive, 0.8 Hz Conversion Rate	456	**825**	µA (max)
		STANDBY Mode	416	**700**	µA (max)

(1) "Typicals" are at T_A = 25°C and represent most likely parametric norm. They are to be used as general reference values not for critical design calculations.
(2) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(3) The supply current will not increase substantially with an SMBus transaction.

Copyright © 2008–2013, Texas Instruments Incorporated

AC Electrical Characteristics

The following specifications apply for V_{DD} = 3.0 VDC to 3.6 VDC, and all analog source impedance R_S = 50Ω unless otherwise specified in the conditions. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A= +25°C.

Symbol	Parameter	Conditions	Typical (1)	Limits (2)	Units (Limit)
TACHOMETER ACCURACY					
	Fan Count Accuracy			**±7**	% (max)
	Fan Full-Scale Count			**65535**	(max)
	Fan Counter Clock Frequency		90		kHz
	Fan Count Update Frequency		1.0		Hz
FAN PWM OUTPUT					
	Frequency Accuracy			**±7**	% (max)

(1) "Typicals" are at T_A = 25°C and represent most likely parametric norm. They are to be used as general reference values not for critical design calculations.
(2) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Digital Electrical Characteristics

Symbol	Parameter	Conditions	Typical (1)	Limits (2)	Units (Limit)
V_{IH}	Logical High Input Voltage			**2.1**	V (min)
V_{IL}	Logical Low Input Voltage			**0.8**	V (max)
I_{IH}	Logical High Input Current	$V_{IN} = V_{DD}$	0.005	**+10**	µA (max)
I_{IL}	Logical Low Input Current	V_{IN} = GND	−0.005	**−10**	µA (max)
C_{IN}	Digital Input Capacitance		5		pF
V_{OL}	$\overline{\text{ALERT}}$, $\overline{\text{TCRIT}}$ and PWM Output Saturation Voltage	I_{OUT} = 6 mA		**0.4**	V (max)
C_{OUT}	Digital Output Capacitance		5		pF

(1) "Typicals" are at T_A = 25°C and represent most likely parametric norm. They are to be used as general reference values not for critical design calculations.
(2) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

SMBus Logical Electrical Characteristics

The following specifications apply for V_{DD} = 3.0 VDC to 3.6 VDC, and all analog source impedance R_S = 50Ω unless otherwise specified in the conditions. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A = +25°C.

Symbol	Parameter	Conditions	Typical (1)	Limits (2)	Units (Limit)
SMBDAT OPEN-DRAIN OUTPUT					
V_{OL}	Logic Low Level Output Voltage	I_{OL} = 4 mA		**0.4**	V (max)
I_{OH}	High Level Output Current	$V_{OUT} = V_{DD}$	0.03	**10**	µA (max)
C_{OUT}	Digital Output Capacitance		5		pF
SMBDAT, SMBCLK INPUTS					
V_{IH}	Logical High Input Voltage			**2.1**	V (min)
V_{IL}	Logical Low Input Voltage			**0.8**	V (max)
V_{HYST}	Logic Input Hysteresis Voltage		320		mV
C_{IN}	Digital Input Capacitance		5		pF

(1) "Typicals" are at T_A = 25°C and represent most likely parametric norm. They are to be used as general reference values not for critical design calculations.
(2) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Copyright © 2008–2013, Texas Instruments Incorporated

SMBus Digital Switching Characteristics

Unless otherwise noted, these specifications apply for V_{DD} = +3.0 VDC to +3.6 VDC, C_L (load capacitance) on output lines = 80 pF. **Boldface limits apply for $T_A = T_J$; $T_{MIN} \le T_A \le T_{MAX}$;** all other limits $T_A = T_J$ = +25°C, unless otherwise noted. The switching characteristics of the LM96163 fully meet or exceed the published specifications of the SMBus version 2.0. The following parameters are the timing relationships between SMBCLK and SMBDAT signals related to the LM96163. They adhere to but are not necessarily the same as the SMBus bus specifications.

Symbol	Parameter	Conditions	Limits (1)	Units (Limit)
f_{SMB}	SMBus Clock Frequency		**10** **100**	kHz (min) kHz (max)
t_{LOW}	SMBus Clock Low Time	From $V_{IN(0)\ max}$ to $V_{IN(0)\ max}$	**4.7**	µs (min)
t_{HIGH}	SMBus Clock High Time	From $V_{IN(1)\ min}$ to $V_{IN(1)\ min}$	**4.0** **50**	µs (min) µs (max)
t_R	SMBus Rise Time	See (2)	**1**	µs (max)
t_F	SMBus Fall Time	See (3)	**0.3**	µs (max)
t_{OF}	Output Fall Time	C_L = 400 pF, I_O = 3 mA	**250**	ns (max)
$t_{TIMEOUT}$	SMBDAT and SMBCLK Time Low for Reset of Serial Interface (4)		**25** **35**	ms (min) ms (max)
$t_{SU:DAT}$	Data In Setup Time to SMBCLK High		**250**	ns (min)
$t_{HD:DAT}$	Data Out Hold Time after SMBCLK Low		**300** **1075**	ns (min) ns (max)
$t_{HD:STA}$	Hold Time after (Repeated) Start Condition. After this period the first clock is generated.		**4.0**	µs (min)
$t_{SU:STO}$	Stop Condition SMBCLK High to SMBDAT Low (Stop Condition Setup)		**100**	ns (min)
$t_{SU:STA}$	SMBus Repeated Start-Condition Setup Time, SMBCLK High to SMBDAT Low		**4.7**	µs (min)
t_{BUF}	SMBus Free Time between Stop and Start Conditions		**4.7**	µs (min)

(1) Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(2) The output rise time is measured from ($V_{IL\ max}$ - 0.15 V) to ($V_{IH\ min}$ + 0.15 V).
(3) The output fall time is measured from ($V_{IH\ min}$ + 0.15 V) to ($V_{IL\ max}$ - 0.15 V).
(4) Holding the SMBDAT and/or SMBCLK lines Low for a time interval greater than $t_{TIMEOUT}$ will reset the LM96163's SMBus state machine, therefore setting SMBDAT and SMBCLK pins to a high impedance state.

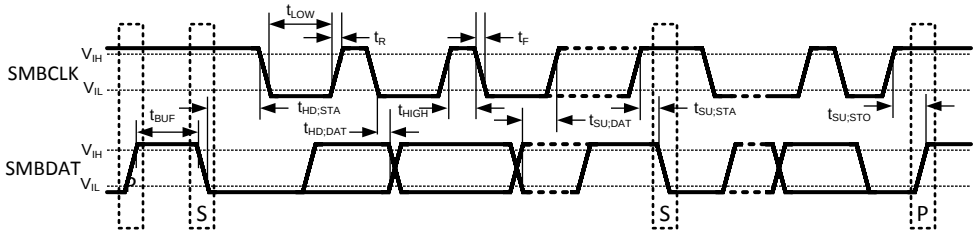
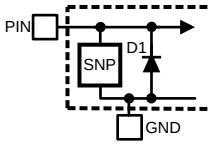
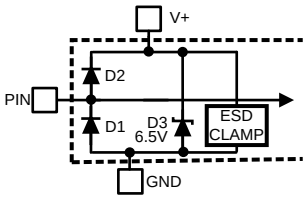


Figure 2. SMBus Timing Diagram for SMBCLK and SMBDAT Signals

Pin #	Label	Circuit	Pin ESD Protection Structure Circuits
1	$\overline{\text{TCRIT}}$	A	 **CIRCUIT A**
2	V_{DD}	B	
3	D+	B	
4	D-	B	
5	PWM	A	
6	GND	B	 **CIRCUIT B**
7	$\overline{\text{ALERT}}$	A	
8	TACH	A	
9	SMBDAT	A	
10	SMBCLK	A	

Copyright © 2008–2013, Texas Instruments Incorporated

Typical Performance Characteristics

Intel Processor on 45nm, 65nm, or 90 nm Process Thermal Diode Performance Comparison

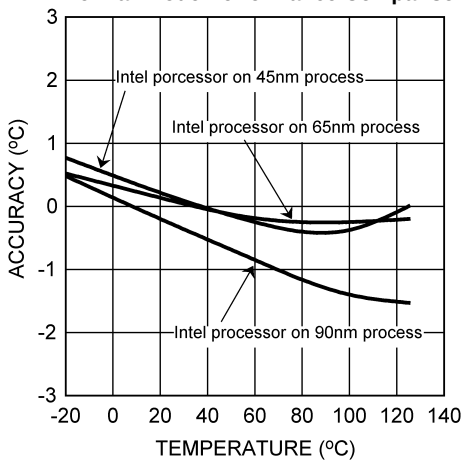


Figure 3.

Remote Temperature Reading Sensitivity to Thermal Diode Filter Capacitance, TruTherm Enabled

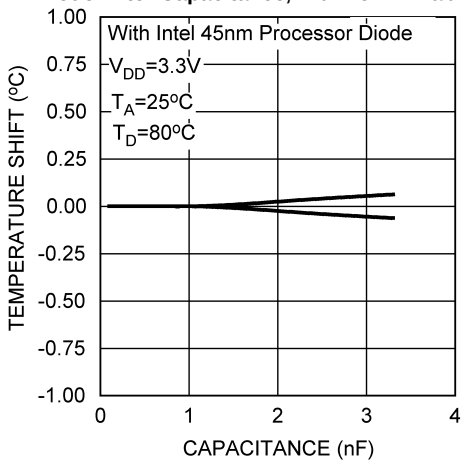


Figure 4.

Remote Temperature Reading Sensitivity to Thermal Diode Filter Capacitance, TruTherm Disabled

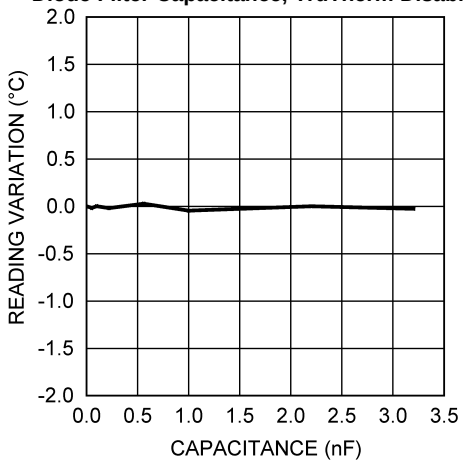


Figure 5.

Thermal Diode Capacitor or PCB Leakage Current Effect on Remote Diode Temperature Reading

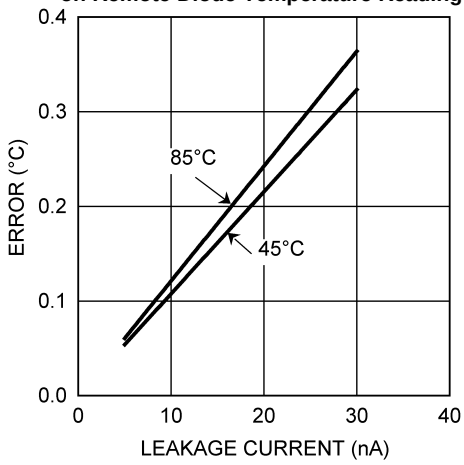


Figure 6.

Conversion Rate Effect on Average Power Supply Current

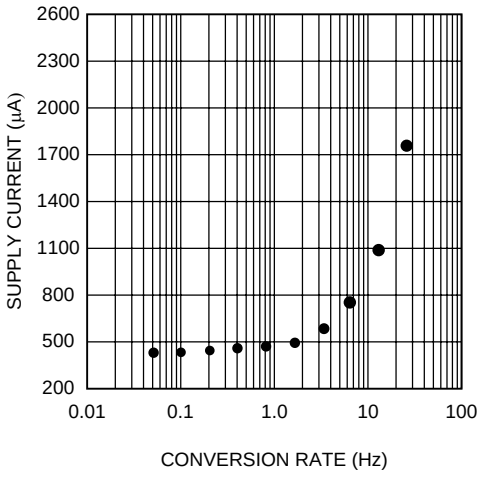


Figure 7.

FUNCTIONAL DESCRIPTION

The LM96163 Remote Diode Temperature Sensor with Integrated Fan Control incorporates a ΔV_{BE}-based temperature sensor utilizing a Local or Remote diode and a 10-bit plus sign ΔΣ ADC (Delta-Sigma Analog-to-Digital Converter). The LM96163 includes TruTherm BJT beta compensation technology that allows precision temperature sensing of remote diodes found in sub-micron processes. The pulse-width modulated (PWM) open-drain output, with a pull-up resistor, is driven by a 12-point temperature to duty cycle look-up table (LUT) and can directly drive a PWM input of a 4-pin fan in order to modulate it's speed enabling optimum system acoustic performance. The LM96163 LUT fan control algorithm also includes a smoothing function that allows the PWM duty cycle to gradually change over a programmed time interval when switching from one level to the next in the LUT. When running at a frequency of 22.5kHz the PWM output resolution is 0.39%. The LM96163 includes a TACH input that can measure the speed of a fan using the pulses from a 3 or 4 pin fan's tachometer output. The LM96163 includes a smart-tach measurement mode to accommodate the corrupted tachometer pulses when using switching transistor power drive to modulate the fan speed. The LM96163 has an $\overline{\text{ALERT}}$ open-drain output that will be pulled low when the measured temperature exceeds certain programmed limits when enabled. Details are contained in the sections below.

The LM96163's two-wire interface is compatible with the SMBus Specification 2.0 . For more information the reader is directed to www.smbus.org.

In the LM96163 digital comparators are used to compare the measured Local Temperature (LT) to the Local High Setpoint user-programmable temperature limit register. The measured Remote Temperature (RT) is digitally compared to the Remote High Setpoint (RHS), the Remote Low Setpoint (RLS), and the Remote T_CRIT Setpoint (RCS) user-programmable temperature limits. An $\overline{\text{ALERT}}$ output will occur when the measured temperature is: (1) higher than either the High Setpoint or the T_CRIT Setpoint, or (2) lower than the Low Setpoint. The ALERT Mask register allows the user to prevent the generation of these $\overline{\text{ALERT}}$ outputs. A $\overline{\text{TCRIT}}$ output will occur when the measured temperature is higher than the T_CRIT Setpoint.

The TCRIT function and the look-up table temperature hysteresis can be set separately. The hysteresis value associated with the TCRIT output is set in the Remote T_CRIT Hysteresis Register. The value associated with the look-up table function is set in the Lookup Table Hysteresis Register.

The LM96163 may be placed in a low power Standby mode by setting the Standby bit found in the Configuration Register. In the Standby mode continuous conversions are stopped. In Standby mode the user may choose to allow the PWM output signal to continue, or not, by programming the PWM Disable in Standby bit in the Configuration Register.

The Local Temperature reading and setpoint data registers are 8-bits wide. The format of the 11-bit remote temperature data is a 16-bit left justified word. Two 8-bit registers, high and low bytes, are provided for each setpoint as well as the temperature reading. A digital filter may be invoked for remote temperature readings that increases the resolution from 11-bits to 13-bits. The temperature readings are also available in an unsigned format allowing resolution above 127°C. Two Remote Temperature Offset (RTO) Registers: High Byte and Low Byte (RTOHB and RTOLB) may be used to correct the temperature readings by adding or subtracting a fixed value based on a different non-ideality factor and series resistance of the thermal diode if different from the thermal diode found in the Intel processors on 45 nm process. See section DIODE NON-IDEALITY.

$\overline{\text{ALERT}}$ and $\overline{\text{TCRIT}}$ OUTPUTS

In this section we will address the ALERT and TCRIT active-low open-drain output functions. When the ALERT Mask bit in the Configuration register is written as zero the ALERT interrupts are enabled.

The LM96163's $\overline{\text{ALERT}}$ pin is versatile and can produce three different methods of use to best serve the system designer: (1) as a temperature comparator (2) as a temperature-based interrupt flag, and (3) as part of an SMBus ALERT System. The three methods of use are further described below. The ALERT and interrupt methods are different only in how the user interacts with the LM96163.

The remote temperature (RT) reading is associated with a T_CRIT Setpoint Register, and both local and remote temperature (LT and RT) readings are associated with a HIGH setpoint register (LHS and RHS). The RT is also associated with a LOW setpoint register (RLS). At the end of every temperature reading a digital comparison determines whether that reading is above its HIGH or T_CRIT setpoint or below its LOW setpoint. If so, the corresponding bit in the ALERT Status Register is set. If the ALERT mask bit is low, any bit set in the ALERT Status Register, with the exception of Busy or RDFA, will cause the ALERT output to be pulled low. Any temperature conversion that is out of the limits defined in the temperature setpoint registers will trigger an ALERT. Additionally, the ALERT Mask Bit must be cleared to trigger an ALERT in all modes.

Copyright © 2008–2013, Texas Instruments Incorporated

The format of the Remote High limit and T_CRIT limit comparison is programmable. The USF bit found in the Enhanced Configuration register controls whether comparisons use a signed or unsigned format. The temperature format used for Remote High and T_CRIT limit comparisons is +255.875 °C to -256 °C.

The three different ALERT modes and TCRIT function will be discussed in the following sections.

$\overline{\text{ALERT}}$ Output as a Temperature Comparator

When the LM96163 is used in a system in which does not require temperature-based interrupts, the $\overline{\text{ALERT}}$ output could be used as a temperature comparator. In this mode, once the condition that triggered the $\overline{\text{ALERT}}$ to go low is no longer present, the $\overline{\text{ALERT}}$ is negated *(*Figure 8*)*. For example, if the $\overline{\text{ALERT}}$ output was activated by the comparison of LT > LHS, when this condition is no longer true, the $\overline{\text{ALERT}}$ will return HIGH. This mode allows operation without software intervention, once all registers are configured during set-up. In order for the $\overline{\text{ALERT}}$ to be used as a temperature comparator, the Comparator Mode bit in the Remote Diode Temperature Filter and Comparator Mode Register must be asserted. This is not the power-on default state.

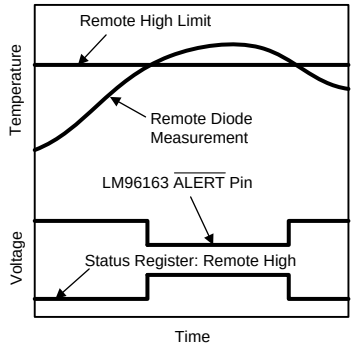


Figure 8. $\overline{\text{ALERT}}$ Output as Temperature Comparator Response Diagram

$\overline{\text{ALERT}}$ Output as an Interrupt

The LM96163's $\overline{\text{ALERT}}$ output can be implemented as a simple interrupt signal when it is used to trigger an interrupt service routine. In such systems it is desirable for the interrupt flag to repeatedly trigger during or before the interrupt service routine has been completed. Under this method of operation, during the read of the ALERT Status Register the LM96163 will set the ALERT Mask bit in the Configuration Register if any bit in the ALERT Status Register is set, with the exception of Busy and RDFA. This prevents further $\overline{\text{ALERT}}$ triggering until the master has reset the ALERT Mask bit, at the end of the interrupt service routine. The ALERT Status Register bits are cleared only upon a read command from the master (see Figure 9) and will be re-asserted at the end of the next conversion if the triggering condition(s) persist(s). In order for the $\overline{\text{ALERT}}$ to be used as a dedicated interrupt signal, the Comparator Mode bit in the Remote Diode Temperature Filter and Comparator Mode Register must be set low. This is the power-on default state. The following sequence describes the response of a system that uses the $\overline{\text{ALERT}}$ output pin as an interrupt flag:

1. Master senses $\overline{\text{ALERT}}$ low.
2. Master reads the LM96163 ALERT Status Register to determine what caused the ALERT.
3. LM96163 clears ALERT Status Register, resets the $\overline{\text{ALERT}}$ HIGH and sets the ALERT Mask bit in the Configuration Register.
4. Master attends to conditions that caused the $\overline{\text{ALERT}}$ to be triggered. The fan is started, setpoint limits are adjusted, etc.
5. Master resets the ALERT Mask bit in the Configuration Register.

Copyright © 2008–2013, Texas Instruments Incorporated

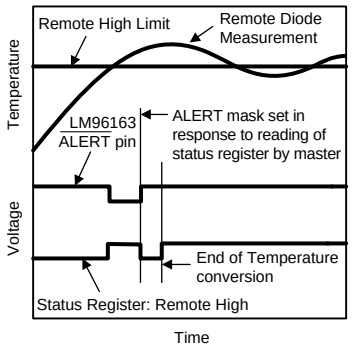


Figure 9. $\overline{\text{ALERT}}$ Output as an Interrupt Temperature Response Diagram

$\overline{\text{ALERT}}$ Output as an SMBus ALERT

An SMBus alert line is created when the $\overline{\text{ALERT}}$ output is connected to: (1) one or more $\overline{\text{ALERT}}$ outputs of other SMBus compatible devices, and (2) to a master. Under this implementation, the LM96163's $\overline{\text{ALERT}}$ should be operated using the ARA (Alert Response Address) protocol. The SMBus 2.0 ARA protocol, defined in the SMBus specification 2.0, is a procedure designed to assist the master in determining which part generated an interrupt and to service that interrupt.

The SMBus alert line is connected to the open-drain ports of all devices on the bus, thereby AND'ing them together. The ARA method allows the SMBus master, with one command, to identify which part is pulling the SMBus alert line LOW. It also prevents the part from pulling the line LOW again for the same triggering condition. When an ARA command is received by all devices on the bus, the devices pulling the SMBus alert line LOW: (1) send their address to the master and (2) release the SMBus alert line after acknowledgement of their address.

The SMBus Specifications 1.1 and 2.0 state that in response to and ARA (Alert Response Address) “after acknowledging the slave address the device must disengage its ALERT pulldown”. Furthermore, “if the host still sees ALERT low when the message transfer is complete, it knows to read the ARA again.” This SMBus “disengaging ALERT requirement prevents locking up the SMBus alert line. Competitive parts may address the “disengaging of ALERT” differently than the LM96163 or not at all. SMBus systems that implement the ARA protocol as suggested for the LM96163 will be fully compatible with all competitive parts.

The LM96163 fulfills “disengaging of ALERT” by setting the ALERT Mask Bit in the Configuration Register after sending out its address in response to an ARA and releasing the $\overline{\text{ALERT}}$ output pin. Once the ALERT Mask bit is activated, the $\overline{\text{ALERT}}$ output pin will be disabled until enabled by software. In order to enable the ALERT the master must read the ALERT Status Register, during the interrupt service routine and then reset the ALERT Mask bit in the Configuration Register to 0 at the end of the interrupt service routine.

The following sequence describes the ARA response protocol.

1. Master senses SMBus alert line low
2. Master sends a START followed by the Alert Response Address (ARA) with a Read Command.
3. Alerting Device(s) send ACK.
4. Alerting Device(s) send their address. While transmitting their address, alerting devices sense whether their address has been transmitted correctly. (The LM96163 will reset its $\overline{\text{ALERT}}$ output and set the ALERT Mask bit once its complete address has been transmitted successfully.)
5. Master/slave NoACK
6. Master sends STOP
7. Master attends to conditions that caused the ALERT to be triggered. The ALERT Status Register is read and fan started, setpoints adjusted, etc.
8. Master resets the ALERT Mask bit in the Configuration Register.

The ARA, 000 1100, is a general call address. No device should ever be assigned to this address.

The ALERT Configuration bit in the Remote Diode Temperature Filter and Comparator Mode Register must be set low in order for the LM96163 to respond to the ARA command.

Copyright © 2008–2013, Texas Instruments Incorporated

The $\overline{\text{ALERT}}$ output can be disabled by setting the ALERT Mask bit in the Configuration Register. The power-on default is to have the ALERT Mask bit and the ALERT Configuration bit low.

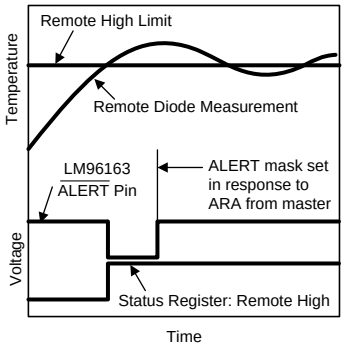


Figure 10. $\overline{\text{ALERT}}$ Output as an SMBus ALERT Temperature Response Diagram

$\overline{\text{TCRIT}}$ Function

The $\overline{\text{TCRIT}}$ output will be activated whenever the RCRIT bit in the ALERT Status register is set. This occurs whenever the remote temperature exceeds the value set by the Remote T_CRIT Setpoint register. There is a hysteresis associated with the T_CRIT Setpoint that is set by the value in the Remote T_CRIT Hysteresis register. The RCRIT bit will be reset when the remote temperature equals or is less than the value defined by Remote T_CRIT Setpoint minus T_CRIT Hysteresis. The resolution of the comparison is 1 °C. For example if T_CRIT = 110 °C and THYST = 5 °C the TCRIT output will activate when the temperature reading is 111 °C and deactivate when the temperature reading is 105 °C.

When the LM96163 powers up the T_CRIT limit is locked to the default value. It may be changed after the T_CRIT Limit Override bit (TCRITOV) bit, found in the Configuration Register, is set.

The format of the Remote T_CRIT setpoint register is controlled by the USF bit found in the Enhanced configuration register. The temperature reading format used for the T_CRIT comparisons is +255 °C to -256°C.

SMBus INTERFACE

Since the LM96163 operates as a slave on the SMBus the SMBCLK line is an input and the SMBDAT line is bidirectional. The LM96163 never drives the SMBCLK line and it does not support clock stretching. According to SMBus specifications, the LM96163 has a 7-bit slave address. All bits, A6 through A0, are internally programmed and cannot be changed by software or hardware.

The complete slave address is:

A6	A5	A4	A3	A2	A1	A0
1	0	0	1	1	0	0

POWER-ON RESET (POR) DEFAULT STATES

For information on the POR default states see Register Map in Functional Order.

TEMPERATURE DATA FORMAT

Temperature data can only be read from the Local and Remote Temperature value registers. The data format for all temperature values is left justified 16-bit word available in two 8-bit registers. Unused bits will always report "0". All temperature data is clamped and will not roll over when a temperature exceeds full-scale value.

Remote temperature and remote high setpoint temperature data can be represented by an 11-bit, two's complement word or unsigned binary word with an LSb (Least Significant Bit) equal to 0.125°C.

Copyright © 2008–2013, Texas Instruments Incorporated

Table 2. 11-bit, 2's complement (10-bit plus sign)

Temperature	Digital Data	
	Binary	Hex
+125°C	0111 1101 0000 0000	7D00h
+25°C	0001 1001 0000 0000	1900h
+1°C	0000 0001 0000 0000	0100h
+0.125°C	0000 0000 0010 0000	0020h
0°C	0000 0000 0000 0000	0000h
−0.125°C	1111 1111 1110 0000	FFE0h
−1°C	1111 1111 0000 0000	FF00h
−25°C	1110 0111 0000 0000	E700h
−55°C	1100 1001 0000 0000	C900h

Table 3. 11-bit, unsigned binary

Temperature	Digital Data	
	Binary	Hex
+255.875°C	1111 1111 1110 0000	FFE0h
+255°C	1111 1111 0000 0000	FF00h
+201°C	1100 1001 0000 0000	C900h
+125°C	0111 1101 0000 0000	7D00h
+25°C	0001 1001 0000 0000	1900h
+1°C	0000 0001 0000 0000	0100h
+0.125°C	0000 0000 0010 0000	0020h
0°C	0000 0000 0000 0000	0000h

When the digital filter is enabled on the remote channel, temperature data is represented by a 13-bit unsigned binary or 12-bit plus sign (two's complement) word with an LSb equal to 0.03125°C.

Table 4. 13-bit, 2's complement (12-bit plus sign)

Temperature	Digital Data	
	Binary	Hex
+125°C	0111 1101 0000 0000	7D00h
+25°C	0001 1001 0000 0000	1900h
+1°C	0000 0001 0000 0000	0100h
+0.03125°C	0000 0000 0000 1000	0008h
0°C	0000 0000 0000 0000	0000h
−0.03125°C	1111 1111 1111 1000	FFF8h
−1°C	1111 1111 0000 0000	FF00h
−25°C	1110 0111 0000 0000	E700h
−55°C	1100 1001 0000 0000	C900h

Table 5. 13-bit, unsigned binary

Temperature	Digital Data	
	Binary	Hex
+255.875°C	1111 1111 1110 0000	FFE0h
+255°C	1111 1111 0000 0000	FF00h
+201°C	1100 1001 0000 0000	C900h
+125°C	0111 1101 0000 0000	7D00h
+25°C	0001 1001 0000 0000	1900h
+1°C	0000 0001 0000 0000	0100h

Copyright © 2008–2013, Texas Instruments Incorporated

Table 5. 13-bit, unsigned binary (continued)

Temperature	Digital Data	
	Binary	Hex
+0.03125°C	0000 0000 0000 1000	0008h
0°C	0000 0000 0000 0000	0000h

Local Temperature and Remote T_CRIT setpoint data is represented by an 8-bit, two's complement, word with an LSb equal to 1°C.

Table 6. 8-bit, 2's complement (7-bit plus sign)

Temperature	Digital Data	
	Binary	Hex
+125°C	0111 1101	7Dh
+25°C	0001 1001	19h
+1°C	0000 0001	01h
0°C	0000 0000	00h
−1°C	1111 1111	FFh
−25°C	1110 0111	E7h
−55°C	1100 1001	C9h

Remote T_CRIT setpoint data can also be represented by an 8-bit, unsigned, word with an LSb equal to 1°C.

Table 7. 8-bit, unsigned binary

Temperature	Digital Data	
	Binary	Hex
+255°C	1111 1111	FFh
+150°C	1001 0110	96h
+125°C	0111 1101	7Dh
+25°C	0001 1001	19h
+1°C	0000 0001	01h
0°C	0000 0000	00h

OPEN-DRAIN OUTPUTS

The SMBDAT, $\overline{\text{ALERT}}$, $\overline{\text{TCRIT}}$ and PWM outputs are open-drain outputs and do not have internal pull-ups. A “High” level will not be observed on these pins until pull-up current is provided by an internal source, typically through a pull-up resistor. Choice of resistor value depends on several factors but, in general, the value should be as high as possible consistent with reliable operation. This will lower the power dissipation of the LM96163 and avoid temperature errors caused by self-heating of the device. The maximum value of the pull-up resistor to provide the 2.1 V high level is 88.7 kΩ.

DIODE FAULT DETECTION

The LM96163 is equipped with operational circuitry designed to detect remote diode fault conditions:

- D+ shorted to V_{DD}
- D+ open or floating
- D+ shorted to GND.

Copyright © 2008–2013, Texas Instruments Incorporated

In the event that the D+ pin is grounded the Remote Temperature reading is forced to –128.000 °C if signed format is read and 0 °C if unsigned format is read. When the D+ pin is detected as shorted to V_{DD} or floating, the Remote Temperature reading is forced to +127.000 °C if signed format is read and +255.000 °C is unsigned format is read. In addition, the ALERT Status register bit RDFA is set. Setting of the RDFA bit will not cause ALERT or TCRIT to activate. Under fault conditions remote diode setpoint comparisons will use these forced temperature values therefore other bits in the ALERT Status Register may be set thus activating the ALERT or TCRIT outputs unless these bits are masked. The function of the ALERT and TCRIT is fully described in Section ALERT and TCRIT OUTPUTS.

COMMUNICATING WITH THE LM96163

Each data register in the LM96163 falls into one of four types of user accessibility:

1. Read Only
2. Write Only
3. Read/Write same address
4. Read/Write different address

A Write to the LM96163 is comprised of an address byte and a command byte. A write to any register requires one data byte.

Reading the LM96163 Registers can take place after the requisite register setup sequence takes place. See Required Initial Fan Control Register Sequence.

The data byte has the Most Significant Bit (MSB) first. At the end of a read, the LM96163 can accept either Acknowledge or No-Acknowledge from the Master. Note that the No-Acknowledge is typically used as a signal for the slave indicating that the Master has read its last byte.

DIGITAL FILTER

In order to suppress erroneous remote temperature readings due to noise as well as increase the resolution of the temperature, the LM96163 incorporates a digital filter for remote temperature readings. The filter is accessed in the Remote Diode Temperature Filter and Comparator Mode Register. The filter can be set according to the following table.

RDTF[1:0]		Filter Setting
0	0	No Filter
0	1	Filter (equivalent to Level 2 filter of the LM86/LM89)
1	0	Reserved
1	1	Enhanced Filter (Filter with transient noise clipping)

Figure 11 describes the filter output in response to a step input and an impulse input.

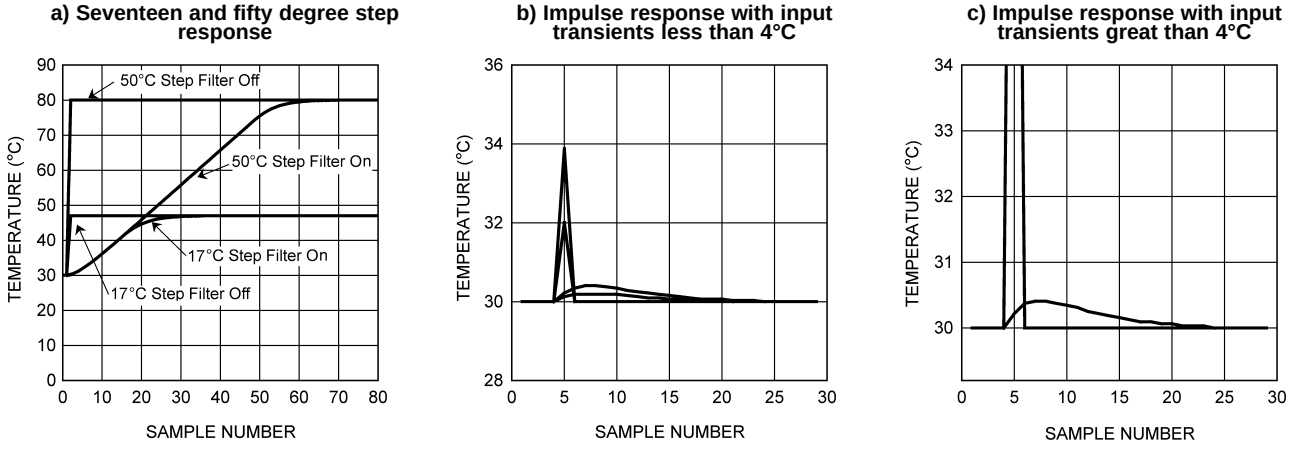
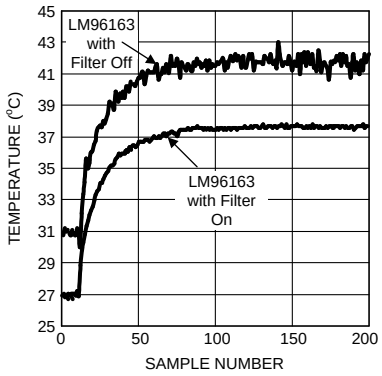


Figure 11.

Copyright © 2008–2013, Texas Instruments Incorporated



The filter curves were purposely offset for clarity.

Figure 12. Digital Filter Response in a typical Intel processor on a 65 nm or 90 nm process

Figure 12 shows the filter in use in a typical Intel processor on a 65/90 nm process system. Note that the two curves have been purposely offset for clarity. Inserting the filter does not induce an offset as shown.

FAULT QUEUE

The LM96163 incorporates a Fault Queue to suppress erroneous ALERT triggering . The Fault Queue prevents false triggering by requiring three consecutive out-of-limit HIGH or LOW temperature readings. See Figure 13. The Fault Queue defaults to OFF upon power-up and may be activated by setting the RDTS Fault Queue bit in the Configuration Register to a 1.

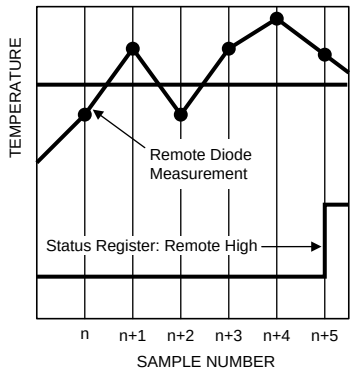


Figure 13. Fault Queue Temperature Response Diagram

ONE-SHOT REGISTER

The One-Shot Register is used to initiate a single conversion and comparison cycle when the device is in standby mode, after which the data returns to standby. This is not a data register. A write operation causes the one-shot conversion. The data written to this address is irrelevant and is not stored. A zero will always be read from this register.

SERIAL INTERFACE RESET

In the event that the SMBus Master is reset while the LM96163 is transmitting on the SMBDAT line, the LM96163 must be returned to a known state in the communication protocol. This may be done in one of two ways:

1. When SMBDAT is Low, the LM96163 SMBus state machine resets to the SMBus idle state if either SMBDAT or SMBCLK are held Low for more than 35 ms ($t_{TIMEOUT}$). Devices are to timeout when either the SMBCLK or SMBDAT lines are held Low for 25 ms – 35 ms. Therefore, to insure a timeout of devices on the bus, either the SMBCLK or the SMBDAT line must be held Low for at least 35 ms.

Copyright © 2008–2013, Texas Instruments Incorporated

2. With both SMBDAT and SMBCLK High, the master can initiate an SMBus start condition with a High to Low transition on the SMBDAT line. The LM96163 will respond properly to an SMBus start condition at any point during the communication. After the start the LM96163 will expect an SMBus Address address byte.

LM96163 REGISTERS

The following pages include: LM96163 REGISTER MAP IN HEXADECIMAL ORDER, which shows a summary of all registers and their bit assignments, LM96163 REGISTER MAP IN FUNCTIONAL ORDER, and LM96163 DETAILED REGISTER DESCRIPTIONS IN FUNCTIONAL ORDER, a detailed explanation of each register. Do not address the unused or manufacturer's test registers.

LM96163 REGISTER MAP IN HEXADECIMAL ORDER

The following is a Register Map grouped in hexadecimal address order. Some address locations have been left blank to maintain compatibility with LM86, LM63 and LM64. Addresses in parenthesis are mirrors of "Same As" address for backwards compatibility with some older software. Reading or writing either address will access the same 8-bit register.

Register 0x[HEX]	R/W	POR Val	Register Name	DATA BITS							
				D7	D6	D5	D4	D3	D2	D1	D0
00	R	–	Local Temperature (Signed MSB)	LT7 SIGN	LT6 64	LT5 32	LT4 16	LT3 8	LT2 4	LT1 2	LT0 1
01	R	–	Rmt Temp MSB	RT12 SIGN	RT11 64	RT10 32	RT9 16	RT8 8	RT7 4	RT6 2	RT5 1
02	R	–	ALERT Status	BUSY	LHIGH	0	RHIGH	RLOW	RDFA	RCRIT	TACH
03	R/W	00	Configuration	ALTMSK	STBY	PWMDIS	0	0	TCHEN	TCRITOV	FLTQUE
04	R/W	08	Conversion Rate	0	0	0	0	CONV3	CONV2	CONV1	CONV0
05	R/W	46	Local High Setpoint	LHS7 SIGN	LHS6 64	LHS5 32	LHS4 16	LHS3 8	LHS2 4	LHS1 2	LHS0 1
06			[Reserved]	**Not Used**							
07	R/W	55	Rmt High Setpoint MSB	RHS10 SIGN /128	RHS9 64	RHS8 32	RHS7 16	RHS6 8	RHS5 4	RHS4 2	RHS3 1
08	R/W	00	Rmt Low Setpoint MSB	RLS10 SIGN	RLS9 64	RLS8 32	RLS7 16	RLS6 8	RLS5 4	RLS4 2	RLS3 1
(09)	R/W	00	Same as 03	ALTMSK	STBY	PWMDIS	0	0	TCHEN	TCRITOV	FLTQUE
(0A)	R/W	08	Same as 04	0	0	0	0	CONV3	CONV2	CONV1	CONV0
(0B)	R/W	46	Same as 05	LHS7 SIGN	LHS6 64	LHS5 32	LHS4 16	LHS3 8	LHS2 4	LHS1 2	LHS0 1
0C	R	00	[Reserved]	**Not Used**							
(0D)	R/W	55	Same as 07	RHS10 SIGN /128	RHS9 64	RHS8 32	RHS7 16	RHS6 8	RHS5 4	RHS4 2	RHS3 1
(0E)	R/W	00	Same as 08	RLS10 SIGN	RLS9 64	RLS8 32	RLS7 16	RLS6 8	RLS5 4	RLS4 2	RLS3 1
0F	W	–	One Shot	**Write Only. Write command triggers one temperature conversion cycle.**							
10	R	–	Rmt Temp LSB (Dig Filter On or Reg 45h STFBE bit set)	RT4 ½	RT3 ¼	RT2 ⅛	RT1 1/16	RT0 1/32	0	0	0
			Rmt Temp LSB (Dig Filter Off)				0	0			
11	R/W	00	Rmt Temp Offset MSB	RTO10 SIGN	RTO9 64	RTO8 32	RTO7 16	RTO7 8	RTO5 4	RTO4 2	RTO3 1
12	R/W	00	Rmt Temp Offset LSB	RTO2 ½	RTO1 ¼	RTO0 ⅛	0	0	0	0	0

Copyright © 2008–2013, Texas Instruments Incorporated

Register 0x[HEX]	R/W	POR Val	Register Name	DATA BITS							
				D7	D6	D5	D4	D3	D2	D1	D0
13	R/W	00	Rmt High Setpoint LSB	RHS2 ½	RHS1 ¼	RHS0 ⅛	0	0	0	0	0
14	R/W	00	Rmt Low Setpoint LSB	RLS2 ½	RLS1 ¼	RLS0 ⅛	0	0	0	0	0
15	R	00	[Reserved]	**Not Used**							
16	R/W	A4	ALERT Mask	1	LHAM	1	RHAM	RLAM	1	RTAM	TCHAM
17-18	R	00	[Reserved]	**Not Used**							
19	R/W	6E	Rmt T_CRIT Setpoint	RCS7 SIGN /128	RCS6 64	RCS5 32	RCS4 16	RCS3 8	RCS2 4	RCS1 2	RCS0 1
1A–20	R	00	[Reserved]	**Not Used**							
21	R/W	0A	Rmt T_CRIT Hysteresis	RTH7 0	RTH6 64	RTH5 32	RTH4 16	RTH3 8	RTH2 4	RTH1 2	RTH0 1
22–2F	R	00	[Reserved]	**Not Used**							
30	R/W	02	Remote Diode TruTherm Enable	0	0	0	0	0	0	RDTE	0
31	R	–	Rmt Temp U-S MSB	RTU12 128	RTU11 64	RTU10 32	RTU9 16	RTU8 8	RTU7 4	RTU6 2	RTU5 1
32	R	–	Rmt Temp U-S LSB Dig Filter On	RTU4 ½	RTU3 ¼	RTU2 ⅛	RTU1 1/16	RTU0 1/32	0	0	0
			Rmt Temp U-S LSB Dig Filter Off				0	0			
33	R	-	POR Status	NR	0	0	0	0	0	0	0
34–44	R	00	[Reserved]	**Not Used**							
45	R/W	00	Enhanced Config	0	STFBE	LRES	PHR	USF	RRS1	RRS0	PSRR
46	R	–	Tach Count LSB	TAC5	TAC4	TAC3	TAC2	TAC1	TAC0	TEDGE1	TEDGE0
47	R	–	Tach Count MSB	TAC13	TAC12	TAC11	TAC10	TAC9	TAC8	TAC7	TAC6
48	R/W	FF	Tach Limit LSB	TACL5	TACL4	TACL3	TACL2	TACL1	TACL0	Not Used 0	Not Used -
49	R/W	FF	Tach Limit MSB	TACL13	TACL12	TACL11	TACL10	TACL9	TACL8	TACL7	TACL6
4A	R/W	20	PWM and RPM Config	0	0	PWPGM	PWOP	PWCKSL	0	TACH1	TACH0
4B	R/W	3F	Fan Spin-Up Config	0	0	SPINUP	SPNDTY 1	SPNDTY 0	SPNTIM2	SPNTIM1	SPNTIM0
4C	R/W	00	PWM Value	HPWVAL 7	HPWVAL 6	PWVAL5	PWVAL4	PWVAL3	PWVAL2	PWVAL1	PWVAL0
4D	R/W	17	PWM Frequency	0	0	0	PWMF4	PWMF3	PWMF2	PWMF1	PWMF0
4E	R/W	00	Lookup Table Temp Offset	0	0	TO5 32	TO4 16	TO3 8	TO2 4	TO1 2	TO0 1
4F	R/W	04	Lookup Table Hysteresis	0	0	0	LOOKH4 16	LOOKH3 8	LOOKH2 4	LOOKH1 2	LOOKH0 1
50–67	R/W	3F, 7F	Lookup Table	**Lookup Table of up to 12 PWM (3F) and Temp Pairs in 8-bit Registers (7F)**							
68–BE	R	00	[Reserved]	**Not Used**							
BF	R/W	00	Rmt Diode Temp Filter	0	0	0	0	0	RDTF1	RDTF0	ALT/CMP
C0–FD	R	00	[Reserved]	**Not Used**							
FE	R	01	Manufacturer's ID	0	0	0	0	0	0	0	1
FF	R	49	Step/Die Rev. ID	0	1	0	0	1	0	0	1

Copyright © 2008–2013, Texas Instruments Incorporated

LM96163 REGISTER MAP IN FUNCTIONAL ORDER

The following is a Register Map grouped in Functional Order. Some address locations have been left blank to maintain compatibility with LM86. Addresses in parenthesis are mirrors of named address. Reading or writing either address will access the same 8-bit register. The Fan Control and Configuration Registers are listed first, as there is a required order to setup these registers first and then setup the others. The detailed explanations of each register will follow the order shown below. POR = Power-On-Reset.

Register [HEX]	Register Name	Read/Write	POR Default [HEX]
FAN CONTROL REGISTERS			
45	Enhanced Configuration	R/W	00
4A	PWM and RPM Configuration	R/W	20
4B	Fan Spin-Up Configuration	R/W	3F
4D	PWM Frequency	R/W	17
4C	PWM Value	Read Only (R/W if Override Bit is Set)	00
4E	Lookup Table Temperature Offset	R/W	00
4F	Lookup Table Hysteresis Temperature	R/W	04
50–67	Lookup Table	R/W	See Table
CONFIGURATION REGISTER			
03 (09)	Configuration	R/W	00
TACHOMETER COUNT AND LIMIT REGISTERS			
46	Tach Count LSB	Read Only	N/A
47	Tach Count MSB	Read Only	N/A
48	Tach Limit LSB	R/W	FF
49	Tach Limit MSB	R/W	FF
LOCAL TEMPERATURE AND LOCAL SETPOINT REGISTERS			
00	Local Temperature	Read Only	N/A
05 (0B)	Local High Setpoint	R/W	46 (70°)
REMOTE DIODE TEMPERATURE AND SETPOINT REGISTERS			
01	Remote Temperature Signed MSB	Read Only	N/A
10	Remote Temperature Signed LSB	Read Only	N/A
31	Remote Temperature Unsigned MSB	Read Only	N/A
32	Remote Temperature Unsigned LSB	Read Only	N/A
11	Remote Temperature Offset MSB	R/W	00
12	Remote Temperature Offset LSB	R/W	00
07 (0D)	Remote High Setpoint MSB	R/W	55 (85°C)
13	Remote High Setpoint LSB	R/W	00
08 (0E)	Remote Low Setpoint MSB	R/W	00 (0°C)
14	Remote Low Setpoint LSB	R/W	00
19	Remote T_CRIT Setpoint	R/W	6E (110°C)
21	Remote T_CRIT Hyst	R/W	0A (10°C)
30	Remote Diode TruTherm Enable	R/W	02
BF	Remote Diode Temperature Filter and Comparator Mode	R/W	00
CONVERSION AND ONE-SHOT REGISTERS			
04 (0A)	Conversion Rate	R/W	08
0F	One-Shot	Write Only	N/A
STATUS AND MASK REGISTERS			
02	ALERT Status	Read Only	N/A
16	ALERT Mask	R/W	A4
33	Power On Reset Status	Read Only	N/A

Copyright © 2008–2013, Texas Instruments Incorporated

Register [HEX]	Register Name	Read/Write	POR Default [HEX]
ID AND TEST REGISTERS			
FE	Manufacturer ID	Read Only	01
FF	Stepping/Die Rev. ID	Read Only	49
[RESERVED] REGISTERS—NOT USED			
06	Not Used	N/A	N/A
0C	Not Used	N/A	N/A
15	Not Used	N/A	N/A
17-18	Not Used	N/A	N/A
1A–20	Not Used	N/A	N/A
22–29	Not Used	N/A	N/A
34–44	Not Used	N/A	N/A
68–BE	Not Used	N/A	N/A
C0–FD	Not Used	N/A	N/A

LM96163 REQUIRED INITIAL FAN CONTROL REGISTER SEQUENCE

Important! The BIOS or firmware must follow the sequence below to configure the following Fan Registers for the LM96163 before using any of the Fan or Tachometer or PWM registers:

Step	$[Register]_{HEX}$ and Setup Instructions(1)
1	After power up check to make sure that the Not Ready bit is cleared in the POR Status register [33] bit 7.
2	Enable or disable Remote Diode TruTherm mode, [30] bit 1.
3	[4A] Write bits 0 and 1; 3 and 4. This includes tach settings if used, PWM internal clock select (1.4 kHz or 360 kHz) and PWM Output Polarity.
4	[4B] Write bits 0 through 5 to program the spin-up settings.
5	[4D] Write bits 0 through 4 to set the frequency settings. This works with the PWM internal clock select. If 22.5 kHz is selected then enhanced fan control functions such as Lookup Table transition smoothing with extended PWM duty cycle resolution is available and should be setup [45].
6	Choose, then write, **only one** of the following: A. [4F–67] the Lookup Table and [4E] the Lookup Table Offset, [45] Lookup Table Temperature Resolution can also be modified **or** B. [4C] the PWM value bits 0 through 5 or bits 0 through 7 if extended duty cycle resolution is selected.
7	If Step 4A, Lookup Table, was chosen and written then write [4A] bit 5 PWPGM = 0. PWPGM should be set to 1 to enable writing to the fan control registers listed in this table.

(1) All other registers can be written at any time after the above sequence.

Copyright © 2008–2013, Texas Instruments Incorporated

LM96163 DETAILED REGISTER DESCRIPTIONS IN FUNCTIONAL ORDER

The following is a Register Map grouped in functional and sequence order. New register addresses have been added to maintain compatibility with the LM63 and LM64 register sets. Addresses in parenthesis are mirrors of named address for backwards compatibility with some older software. Reading or writing either address will access the same 8-bit register.

Fan Control Registers

Address Hex	Read/ Write	Bits	POR Value	Name	Description
45_{HEX} ENHANCED CONFIGURATION					
45	R	7	0	[Reserved]	This bit is unused and always read as 0.
	R/W	6	0	STFBE	Signed Temperature Filter Bits Enable 0: external signed temperature LSbs [4:3] will always read "0" (backwards compatible with the LM63) 1: when the digital filter is enabled the external signed temperature LSbs [4:3] (1/16 and 1/32 resolution) are enabled
	R/W	5	0	LRES	Lookup Table Resolution Extension 0: LUT temperature resolution 7-bits (LSb = 1°C, backwards compatible with the LM63) 1: enable 8-bit LUT temperature resolution (LSb extended to 0.5°C)
	R/W	4	0	PHR	22.5kHz PWM High Resolution Control (only effective when PWM frequency set to 22.5kHz) 0: PWM resolution 6.25% (backwards compatible with the LM63) 1: enable high resolution (0.39%)
	R/W	3	0	USF	Unsigned High and T_CRIT Setpoint Format 0: enable signed format for High and T_CRIT setpoints (11-bit is -128.000°C to 127.875°C or 8-bit is -128°C to 127°C) 1: enable unsigned format for High and T_CRIT setpoints (11-bit is 0°C to 255.875°C or 8-bit is 0°C to 255°C)
	R/W	2:1	00	RRS1:RRS0	PWM Smoothing Ramp Rate Setting (these bits can modified only when PWM Programming is enabled, 0x4A[5]=1) 00: 0.023 s per step (5.45 seconds for 0 to 100% duty cycle transition with 0.39% resolution) 01: 0.046 s per step (10.9 seconds for 0 to 100% duty cycle transition with 0.39% resolution) 10: 0.91 s per step (21.6 seconds for 0 to 100% duty cycle transition with 0.39% resolution) 11: 0.182 s per step (43.7 seconds for 0 to 100% duty cycle transition with 0.39% resolution) Note: PWM smoothing is disabled for PWM spinup and for duty cycle setting override caused by a TCRIT event, thus it is only enabled during LUT transitions. PWM smoothing is only effective when PWM frequency is set to 22.5kHz.
	R/W	0	0	PSRR	PWM Smoothing Ramp Rate Control (this bit can modified only when the PWM Programming is enabled, 0x4A[5]=1) 0: PWM smoothing disabled (LM63 backwards compatible) 1: enable ramp rate control (as controlled by 0x45[2:1]) Note: PWM smoothing is disabled for PWM spinup and for duty cycle setting override caused by a TCRIT event, thus it is only enabled during LUT transitions. PWM smoothing is only effective when PWM frequency is set to 22.5kHz

Copyright © 2008–2013, Texas Instruments Incorporated

Address Hex	Read/ Write	Bits	POR Value	Name	Description
$4A_{HEX}$ FAN PWM AND TACHOMETER CONFIGURATION REGISTER					
4A	R	7:6	00	[Reserved]	These bits are unused and always read as 0.
	R/W	5	1	PWPGM	PWM Programming enable 0: the PWM Value (register 0x4C), the PWM Smoothing (0x45[2:0]) and the Lookup Table (Registers 0x50–0x67) are read-only. The PWM value (0 to 100%) is determined by the current remote diode temperature and the Lookup Table, and can be read from the PWM value register. 1: the PWM value (register 0x4C), the PWM Smoothing (0x45[2:0]) and the Lookup Table (Registers 0x50–0x67) are read/write enabled. Writing the PWM Value register will set the PWM output. This is also the state during which the Lookup Table can be written.
		4	0	PWOP	PWM Output Polarity 0: the PWM output pin will be 0V for fan OFF and open for fan ON. 1: the PWM output pin will be open for fan OFF and 0V for fan ON.
		3	0	PWCLSL	PWM Master Clock Select 0: the master PWM clock is 360 kHz 1: the master PWM clock is 1.4 kHz.
		2	0	[Reserved]	Always write 0 to this bit.
		1:0	00	TACH1:TACH0	Tachometer Mode 00: Traditional tach input monitor, false readings when under minimum detectable RPM. (Smart-TACH mode disabled) 01: Traditional tach input monitor, FFFFh reading when under minimum detectable RPM. Smart-TACH mode enabled, PWM duty cycle not affected. Use with direct PWM drive of fan power. TACH readings can cause an error event if TACH setpoint register is set to less than FFFFh even though fan may be spinning properly. 10: Most accurate readings, FFFFh reading when under minimum detectable RPM. Smart-TACH mode enabled, PWM duty cycle modified. Use with direct PWM drive of fan power. This mode extends the TACH monitoring low RPM sensitivity. 11: Least effort on programmed PWM of fan, FFFF reading when under minimum detectable RPM. Smart-TACH mode enabled. Use with direct PWM drive of fan power. This mode extends the TACH monitoring low RPM sensitivity the most. Note: If the PWM Master Clock is 360 kHz, mode 00 is used regardless of the setting of these two bits.
$4B_{HEX}$ FAN SPIN-UP CONFIGURATION REGISTER					
4B	R	7:6	0	[Reserved]	These bits are unused and always read as 0
	R/W	5	1	SPINUP	Fast Tachometer Spin-up If 0, the fan spin-up uses the duty cycle and spin-up time, bits 0–4. If 1, the LM96163 sets the PWM output to 100% until the spin-up times out (per bits 0–2) or the minimum desired RPM has been reached (per the Tachometer Setpoint setting) using the tachometer input, whichever happens first. This bit overrides the PWM Spin-Up Duty Cycle register (bits 4:3)—PWM output is always 100%. Register x03, bit 2 = 1 for Tachometer mode. If PWM Spin-Up Time (bits 2:0) = 000, the Spin-Up cycle is bypassed, regardless of the state of this bit.
		4:3	11	SPNDTY1:SPNDTY0	PWM Spin-Up Duty Cycle 00: Spin-Up cycle bypassed (no Spin-Up), unless Fast Tachometer Terminated Spin-Up (bit 5) is set. 01: 50% 10: 75%–81% Depends on PWM Frequency. See Applications Notes. 11: 100%
		2:0	111	SPNTIM2:SPNTIM0	PWM Spin-Up Time Interval 000: Spin-Up cycle bypassed (No Spin-Up) 001: 0.05 seconds 010: 0.1 s 011: 0.2 s 100: 0.4 s 101: 0.8 s 110: 1.6 s 111: 3.2 s

Copyright © 2008–2013, Texas Instruments Incorporated

Address Hex	Read/ Write	Bits	POR Value	Name	Description
$4C_{HEX}$ PWM VALUE REGISTER					
4C	Read (Write only if reg 4A bit 5 = 1.)	7:6	00	HPWVAL7:HPWVAL6	PWM High Resolution and Low Resolution Values If PWM Program (register 4A, bit 5) = 0 this register is read only, this register reflects the LM96163's current PWM value from the Lookup Table. If PWM Program (register 4A, bit 5) = 1, this register is read/write and the desired PWM value is written directly to this register, instead of from the Lookup Table, for direct fan speed control. This register will read 0 during the Spin-Up cycle. See Application Notes section at the end of this datasheet for more information regarding the PWM Value and Duty Cycle in %.
		5:0	0x00	PWVAL5:PWVAL0	
$4D_{HEX}$ FAN PWM FREQUENCY REGISTER					
4D	R	7:5	000	[Reserved]	These bits are unused and always read as 0
	R/W	4:0	0x17	PWMF4:PWMF0	PWM Output Frequency The PWM Frequency = PWM_Clock / 2n, where PWM Master Clock = 360 kHz or 1.4 kHz (per the PWM Master Clock Select bit in Register 4A), and n = value of the register. Note: n = 0 is mapped to n = 1. See the Application Note at the end of this datasheet.
$4E_{HEX}$ LOOKUP TABLE TEMPERATURE OFFSET					
4E	R	7:6	00	[Reserved]	These bits are unused and always read as 0.
	R/W	5:0	0x00	TO5:TO0	The temperature offset applied to the temperature values of the lookup table. This offset allows the lookup table temperature settings to be extended above 127°C. The value, which is always positive, has an unsigned format with 1°C resolution. The maximum offset that can be programmed is +63°C.
$4F_{HEX}$ LOOKUP TABLE HYSTERESIS					
4F	R	7:5	000	[Reserved]	These bits are unused and always read as 0
	R/W	4:0	0x04	LOOKH4:LOOKH0	Lookup Table Hysteresis The amount of hysteresis applied to the Lookup Table. (1 LSb = 1°C, max value 31°C, default value 10°C).
50_{HEX} to 67_{HEX} LOOKUP TABLE (7/8 Bits for Temperature and 6/8 Bits for PWM for each Temperature/PWM Pair)					
50	Read. (Write only if reg 4A bit 5 = 1)	7	0	E1T7	Lookup Table Temperature Entry 1 Bit 7 is unused and always set to 0 in the low resolution temperature LUT mode. In the high resolution temperature LUT mode bit 7 in conjunction with bits 6:0 of this register are used to determine the limit temperature that the remote diode temperature is compared to. In high resolution the range is 0°C to 127.5°C. In low resolution mode the range is 0°C to 127°C. If the remote diode temperature exceeds this value, the PWM output will be the value in Register 0x51. Only 9-bits of the temperature reading are used in high resolution and 8-bits in low resolution. Only positive temperature values can be programed in this register and in all cases the sign bit is assumed to be zero. Temperatures greater than 127 °C or 127.5 °C can be programmed through the use of the Lookup Table Temperature Offset Register (4Eh).
		6:0	0x7F	E1T6:E1T0	
51		7:6	00	E1D7:E1D6	Lookup Table PWM Duty Cycle Extended Entry 1 These bits are unused and always set to 0 in the low resolution duty cycle LUT mode. In the high resolution duty cycle LUT mode these bits in association with bits 5:0 of this register are used for the PWM value associated with the temperature limit in register 0x50. These bits can only be activated when PWM frequency of 22.5kHz is chosen.
		5:0	0x3F	E1D5:E1D0	Lookup Table PWM Duty Cycle Entry 1 The PWM value corresponding to the temperature limit in register 0x50 for the low resolution PWM mode.

Copyright © 2008–2013, Texas Instruments Incorporated

Address Hex	Read/ Write	Bits	POR Value	Name	Description
52	Read. (Write only if reg 4A bit 5 = 1)	7	0	E2T7	Lookup Table Temperature Entry 2 Bit 7 is unused and always set to 0 in the low resolution temperature LUT mode. In the high resolution temperature LUT mode bit 7 in conjunction with bits 6:0 of this register are used to determine the limit temperature that the remote diode temperature is compared to. In high resolution the range is 0°C to 127.5°C. In low resolution mode the range is 0°C to 127°C. If the remote diode temperature exceeds this value, the PWM output will be the value in Register 0x53. Only 9-bits of the temperature reading are used in high resolution and 8-bits in low resolution. Only positive temperature values can be programed in this register and in all cases the sign bit is assumed to be zero. Temperatures greater than 127 °C or 127.5 °C can be programmed through the use of the Lookup Table Temperature Offset Register (4Eh).
		6:0	0x7F	E2T6:E2T0	
53		7:6	00	E2D7:E2D6	Lookup Table PWM Duty Cycle Extended Entry 2 These bits are unused and always set to 0 in the low resolution duty cycle LUT mode. In the high resolution duty cycle LUT mode these bits in association with bits 5:0 of this register are used for the PWM value associated with the temperature limit in register 0x52. These bits can only be activated when PWM frequency of 22.5kHz is chosen.
		5:0	0x3F	E2D5:E2D0	Lookup Table PWM Duty Cycle Entry 2 The PWM value corresponding to the temperature limit in register 0x52 for the low resolution PWM mode.
54	Read. (Write only if reg 4A bit 5 = 1)	7	0	E3T7	Lookup Table Temperature Entry 3 Bit 7 is unused and always set to 0 in the low resolution temperature LUT mode. In the high resolution temperature LUT mode bit 7 in conjunction with bits 6:0 of this register are used to determine the limit temperature that the remote diode temperature is compared to. In high resolution the range is 0°C to 127.5°C. In low resolution mode the range is 0°C to 127°C. If the remote diode temperature exceeds this value, the PWM output will be the value in Register 0x55. Only 9-bits of the temperature reading are used in high resolution and 8-bits in low resolution. Only positive temperature values can be programed in this register and in all cases the sign bit is assumed to be zero. Temperatures greater than 127 °C or 127.5 °C can be programmed through the use of the Lookup Table Temperature Offset Register (4Eh).
		6:0	0x7F	E3T6:E3T0	
55		7:6	00	E3D7:E3D6	Lookup Table PWM Duty Cycle Extended Entry 3 These bits are unused and always set to 0 in the low resolution duty cycle LUT mode. In the high resolution duty cycle LUT mode these bits in association with bits 5:0 of this register are used for the PWM value associated with the temperature limit in register 0x54. These bits can only be activated when PWM frequency of 22.5kHz is chosen.
		5:0	0x3F	E3D5:E3D0	Lookup Table PWM Duty Cycle Entry 3 The PWM value corresponding to the temperature limit in register 0x54 for the low resolution PWM mode.
56	Read. (Write only if reg 4A bit 5 = 1)	7	0	E4T7	Lookup Table Temperature Entry 4 Bit 7 is unused and always set to 0 in the low resolution temperature LUT mode. In the high resolution temperature LUT mode bit 7 in conjunction with bits 6:0 of this register are used to determine the limit temperature that the remote diode temperature is compared to. In high resolution the range is 0°C to 127.5°C. In low resolution mode the range is 0°C to 127°C. If the remote diode temperature exceeds this value, the PWM output will be the value in Register 0x57. Only 9-bits of the temperature reading are used in high resolution and 8-bits in low resolution. Only positive temperature values can be programed in this register and in all cases the sign bit is assumed to be zero. Temperatures greater than 127 °C or 127.5 °C can be programmed through the use of the Lookup Table Temperature Offset Register (4Eh).
		6:0	0x7F	E4T6:E4T0	
57		7:6	00	E4D7:E4D6	Lookup Table PWM Duty Cycle Extended Entry 4 These bits are unused and always set to 0 in the low resolution duty cycle LUT mode. In the high resolution duty cycle LUT mode these bits in association with bits 5:0 of this register are used for the PWM value associated with the temperature limit in register 0x56. These bits can only be activated when PWM frequency of 22.5kHz is chosen.
		5:0	0x3F	E4D5:E4D0	Lookup Table PWM Duty Cycle Entry 4 The PWM value corresponding to the temperature limit in register 0x56 for the low resolution PWM mode.

Copyright © 2008–2013, Texas Instruments Incorporated

Address Hex	Read/ Write	Bits	POR Value	Name	Description
58	Read. (Write only if reg 4A bit 5 = 1)	7	0	E5T7	Lookup Table Temperature Entry 5 Bit 7 is unused and always set to 0 in the low resolution temperature LUT mode. In the high resolution temperature LUT mode bit 7 in conjunction with bits 6:0 of this register are used to determine the limit temperature that the remote diode temperature is compared to. In high resolution the range is 0°C to 127.5°C. In low resolution mode the range is 0°C to 127°C. If the remote diode temperature exceeds this value, the PWM output will be the value in Register 0x59. Only 9-bits of the temperature reading are used in high resolution and 8-bits in low resolution. Only positive temperature values can be programed in this register and in all cases the sign bit is assumed to be zero. Temperatures greater than 127 °C or 127.5 °C can be programmed through the use of the Lookup Table Temperature Offset Register (4Eh).
		6:0	0x7F	E5T6:E5T0	
59		7:6	00	E5D7:E5D6	Lookup Table PWM Duty Cycle Extended Entry 5 These bits are unused and always set to 0 in the low resolution duty cycle LUT mode. In the high resolution duty cycle LUT mode these bits in association with bits 5:0 of this register are used for the PWM value associated with the temperature limit in register 0x58. These bits can only be activated when PWM frequency of 22.5kHz is chosen.
		5:0	0x3F	E5D5:E5D0	Lookup Table PWM Duty Cycle Entry 5 The PWM value corresponding to the temperature limit in register 0x58 for the low resolution PWM mode.
5A	Read. (Write only if reg 4A bit 5 = 1)	7	0	E6T7	Lookup Table Temperature Entry 6 Bit 7 is unused and always set to 0 in the low resolution temperature LUT mode. In the high resolution temperature LUT mode bit 7 in conjunction with bits 6:0 of this register are used to determine the limit temperature that the remote diode temperature is compared to. In high resolution the range is 0°C to 127.5°C. In low resolution mode the range is 0°C to 127°C. If the remote diode temperature exceeds this value, the PWM output will be the value in Register 0x5B. Only 9-bits of the temperature reading are used in high resolution and 8-bits in low resolution. Only positive temperature values can be programed in this register and in all cases the sign bit is assumed to be zero. Temperatures greater than 127 °C or 127.5 °C can be programmed through the use of the Lookup Table Temperature Offset Register (4Eh).
		6:0	0x7F	E6T6:E6T0	
5B		7:6	00	E6D7:E6D6	Lookup Table PWM Duty Cycle Extended Entry 6 These bits are unused and always set to 0 in the low resolution duty cycle LUT mode. In the high resolution duty cycle LUT mode these bits in association with bits 5:0 of this register are used for the PWM value associated with the temperature limit in register 0x5A. These bits can only be activated when PWM frequency of 22.5kHz is chosen.
		5:0	0x3F	E6D5:E6D0	Lookup Table PWM Duty Cycle Entry 6 The PWM value corresponding to the temperature limit in register 0x5A for the low resolution PWM mode.
5C	Read. (Write only if reg 4A bit 5 = 1)	7	0	E7T7	Lookup Table Temperature Entry 7 Bit 7 is unused and always set to 0 in the low resolution temperature LUT mode. In the high resolution temperature LUT mode bit 7 in conjunction with bits 6:0 of this register are used to determine the limit temperature that the remote diode temperature is compared to. In high resolution the range is 0°C to 127.5°C. In low resolution mode the range is 0°C to 127°C. If the remote diode temperature exceeds this value, the PWM output will be the value in Register 0x5D. Only 9-bits of the temperature reading are used in high resolution and 8-bits in low resolution. Only positive temperature values can be programed in this register and in all cases the sign bit is assumed to be zero. Temperatures greater than 127 °C or 127.5 °C can be programmed through the use of the Lookup Table Temperature Offset Register (4Eh).
		6:0	0x7F	E7T6:E7T0	
5D		7:6	00	E7D7:E7D6	Lookup Table PWM Duty Cycle Extended Entry 7 These bits are unused and always set to 0 in the low resolution duty cycle LUT mode. In the high resolution duty cycle LUT mode these bits in association with bits 5:0 of this register are used for the PWM value associated with the temperature limit in register 0x5C. These bits can only be activated when PWM frequency of 22.5kHz is chosen.
		5:0	0x3F	E7D5:E7D0	Lookup Table PWM Duty Cycle Entry 7 The PWM value corresponding to the temperature limit in register 0x5C for the low resolution PWM mode.

Copyright © 2008–2013, Texas Instruments Incorporated

Address Hex	Read/ Write	Bits	POR Value	Name	Description
5E	Read. (Write only if reg 4A bit 5 = 1)	7	0	E8T7	Lookup Table Temperature Entry 8 Bit 7 is unused and always set to 0 in the low resolution temperature LUT mode. In the high resolution temperature LUT mode bit 7 in conjunction with bits 6:0 of this register are used to determine the limit temperature that the remote diode temperature is compared to. In high resolution the range is 0°C to 127.5°C. In low resolution mode the range is 0°C to 127°C. If the remote diode temperature exceeds this value, the PWM output will be the value in Register 0x5F. Only 9-bits of the temperature reading are used in high resolution and 8-bits in low resolution. Only positive temperature values can be programed in this register and in all cases the sign bit is assumed to be zero. Temperatures greater than 127 °C or 127.5 °C can be programmed through the use of the Lookup Table Temperature Offset Register (4Eh).
		6:0	0x7F	E8T6:E8T0	
5F		7:6	00	E8D7:E8D6	Lookup Table PWM Duty Cycle Extended Entry 8 These bits are unused and always set to 0 in the low resolution duty cycle LUT mode. In the high resolution duty cycle LUT mode these bits in association with bits 5:0 of this register are used for the PWM value associated with the temperature limit in register 0x5E. These bits can only be activated when PWM frequency of 22.5kHz is chosen.
		5:0	0x3F	E8D5:E8D0	Lookup Table PWM Duty Cycle Entry 8 The PWM value corresponding to the temperature limit in register 0x5E for the low resolution PWM mode.
60	Read. (Write only if reg 4A bit 5 = 1)	7	0	E9T7	Lookup Table Temperature Entry 9 Bit 7 is unused and always set to 0 in the low resolution temperature LUT mode. In the high resolution temperature LUT mode bit 7 in conjunction with bits 6:0 of this register are used to determine the limit temperature that the remote diode temperature is compared to. In high resolution the range is 0°C to 127.5°C. In low resolution mode the range is 0°C to 127°C. If the remote diode temperature exceeds this value, the PWM output will be the value in Register 0x61. Only 9-bits of the temperature reading are used in high resolution and 8-bits in low resolution. Only positive temperature values can be programed in this register and in all cases the sign bit is assumed to be zero. Temperatures greater than 127 °C or 127.5 °C can be programmed through the use of the Lookup Table Temperature Offset Register (4Eh).
		6:0	0x7F	E9T6:E9T0	
61		7:6	00	E9D7:E9D6	Lookup Table PWM Duty Cycle Extended Entry 9 These bits are unused and always set to 0 in the low resolution duty cycle LUT mode. In the high resolution duty cycle LUT mode these bits in association with bits 5:0 of this register are used for the PWM value associated with the temperature limit in register 0x60. These bits can only be activated when PWM frequency of 22.5kHz is chosen.
		5:0	0x3F	E9D5:E9D0	Lookup Table PWM Duty Cycle Entry 9 The PWM value corresponding to the temperature limit in register 0x60 for the low resolution PWM mode.
62	Read. (Write only if reg 4A bit 5 = 1)	7	0	E10T7	Lookup Table Temperature Entry 10 Bit 7 is unused and always set to 0 in the low resolution temperature LUT mode. In the high resolution temperature LUT mode bit 7 in conjunction with bits 6:0 of this register are used to determine the limit temperature that the remote diode temperature is compared to. In high resolution the range is 0°C to 127.5°C. In low resolution mode the range is 0°C to 127°C. If the remote diode temperature exceeds this value, the PWM output will be the value in Register 0x63. Only 9-bits of the temperature reading are used in high resolution and 8-bits in low resolution. Only positive temperature values can be programed in this register and in all cases the sign bit is assumed to be zero. Temperatures greater than 127 °C or 127.5 °C can be programmed through the use of the Lookup Table Temperature Offset Register (4Eh).
		6:0	0x7F	E10T6:E10T0	
63		7:6	00	E10D7:E10D6	Lookup Table PWM Duty Cycle Extended Entry 10 These bits are unused and always set to 0 in the low resolution duty cycle LUT mode. In the high resolution duty cycle LUT mode these bits in association with bits 5:0 of this register are used for the PWM value associated with the temperature limit in register 0x62. These bits can only be activated when PWM frequency of 22.5kHz is chosen.
		5:0	0x3F	E10D5:E10D0	Lookup Table PWM Duty Cycle Entry 10 The PWM value corresponding to the temperature limit in register 0x62 for the low resolution PWM mode.

Copyright © 2008–2013, Texas Instruments Incorporated

Address Hex	Read/ Write	Bits	POR Value	Name	Description
64	Read. (Write only if reg 4A bit 5 = 1)	7	0	E11T7	Lookup Table Temperature Entry 11 Bit 7 is unused and always set to 0 in the low resolution temperature LUT mode. In the high resolution temperature LUT mode bit 7 in conjunction with bits 6:0 of this register are used to determine the limit temperature that the remote diode temperature is compared to. In high resolution the range is 0°C to 127.5°C. In low resolution mode the range is 0°C to 127°C. If the remote diode temperature exceeds this value, the PWM output will be the value in Register 0x65. Only 9-bits of the temperature reading are used in high resolution and 8-bits in low resolution. Only positive temperature values can be programed in this register and in all cases the sign bit is assumed to be zero. Temperatures greater than 127 °C or 127.5 °C can be programmed through the use of the Lookup Table Temperature Offset Register (4Eh).
		6:0	0x7F	E11T6:E11T0	
65		7:6	00	E11D7:E11D6	Lookup Table PWM Duty Cycle Extended Entry 11 These bits are unused and always set to 0 in the low resolution duty cycle LUT mode. In the high resolution duty cycle LUT mode these bits in association with bits 5:0 of this register are used for the PWM value associated with the temperature limit in register 0x64. These bits can only be activated when PWM frequency of 22.5kHz is chosen.
		5:0	0x3F	E11D5:E11D0	Lookup Table PWM Duty Cycle Entry 11 The PWM value corresponding to the temperature limit in register 0x64 for the low resolution PWM mode.
66	Read. (Write only if reg 4A bit 5 = 1)	7	0	E12T7	Lookup Table Temperature Entry 12 Bit 7 is unused and always set to 0 in the low resolution temperature LUT mode. In the high resolution temperature LUT mode bit 7 in conjunction with bits 6:0 of this register are used to determine the limit temperature that the remote diode temperature is compared to. In high resolution the range is 0°C to 127.5°C. In low resolution mode the range is 0°C to 127°C. If the remote diode temperature exceeds this value, the PWM output will be the value in Register 0x67. Only 9-bits of the temperature reading are used in high resolution and 8-bits in low resolution. Only positive temperature values can be programed in this register and in all cases the sign bit is assumed to be zero. Temperatures greater than 127 °C or 127.5 °C can be programmed through the use of the Lookup Table Temperature Offset Register (4Eh).
		6:0	0x7F	E12T6:E12T0	
67		7:6	00	E12D7:E12D6	Lookup Table PWM Duty Cycle Extended Entry 12 These bits are unused and always set to 0 in the low resolution duty cycle LUT mode. In the high resolution duty cycle LUT mode these bits in association with bits 5:0 of this register are used for the PWM value associated with the temperature limit in register 0x66. These bits can only be activated when PWM frequency of 22.5kHz is chosen.
		5:0	0x3F	E12D5:E12D0	Lookup Table PWM Duty Cycle Entry 12 The PWM value corresponding to the temperature limit in register 0x66 for the low resolution PWM mode.

Copyright © 2008–2013, Texas Instruments Incorporated

Configuration Register

Address Hex	Read/ Write	Bits	POR Value	Name	Description
03 (09)$_{HEX}$ CONFIGURATION REGISTER					
03 (09)	R/W	7	0	ALTMSK	ALERT Mask 0: ALERT interrupts are enabled. 1: ALERT interrupts are masked, and the $\overline{\text{ALERT}}$ pin is always in a high impedance (open) state.
		6	0	STBY	Standby 0: the LM96163 is in operational mode, converting, comparing, and updating the PWM output continuously. 1: the LM96163 enters a low power standby mode. In standby, continuous conversions are stopped, but a conversion/comparison cycle may be initiated by writing any value to register 0x0F the One-shot Register. Operation of the PWM output in standby depends on the setting of bit 5 in this register.
		5	0	PWMDIS	PWM Disable in Standby 0: the LM96163's PWM output continues to output the current fan control signal while in STANDBY. 1: the PWM output is disabled (as defined by the PWM polarity bit) while in STANDBY.
	R	4:3	00	[Reserved]	This bit is unused and always read as 0.
	R/W	2	0	TCHEN	TACH Enable 0: disables the TACH input 1: enables the TACH input
		1	0	TCRITOV	T_CRIT Limit Override 0: locks the T_CRIT limit for the remote diode, POR setting is nominally 110°C 1: unlocks the T_CRIT limit and allows it to be reprogrammed multiple times
		0	0	FLTQUE	RDTS Fault Queue 0: an ALERT will be generated if any Remote Diode conversion result is above the **Remote High Set Point or below the Remote Low Setpoint**. 1: an ALERT will be generated only if three consecutive Remote Diode conversions are above the **Remote High Set Point or below the Remote Low Setpoint**.

Tachometer Count and Limit Registers

Address Hex	Read/ Write	Bits	POR Value	Name	Description		
47$_{HEX}$ TACHOMETER COUNT (MSB) and 46$_{HEX}$ TACHOMETER COUNT (LSB) REGISTERS (16 bits: Read LSB first to lock MSB and ensure MSB and LSB are from the same reading)							
47	R	7:0	N/A	TAC13:TAC6	Tachometer Count (MSB and LSB) These registers contain the current 16-bit Tachometer Count, representing the period of time between tach pulses. Note that the 16-bit tachometer MSB and LSB register addresses are in reverse order from the 16 bit temperature readings.		
46	R	7:2	N/A	TAC5:TAC0			
	R	1:0	00	TEDGE1:TEDGE0	Tachometer Edge Programming		
					Bits	**Edges Used**	**Tach_Count_Multiple**
					00:	Reserved - do not use	
					01:	2	4
					10:	3	2
					11:	5	1
					Note: If PWM_Clock_Select = 360 kHz, then Tach_Count_Multiple = 1 regardless of the setting of these bits.		

Copyright © 2008–2013, Texas Instruments Incorporated

Address Hex	Read/ Write	Bits	POR Value	Name	Description
49_{HEX} TACHOMETER LIMIT (MSB) and 48_{HEX} TACHOMETER LIMIT (LSB) REGISTERS					
49	R/W	7:0	0xFF	TACL13:TACL6	Tachometer Limit (MSB and LSB) These registers contain the current 14-bit Tachometer Count, representing the period of time between tach pulses. Fan RPM = (f * 5,400,000) / (Tachometer Count), where f = 1 for 2 pulses/rev fan; f = 2 for 1 pulse/rev fan; and f = 2/3 for 3 pulses/rev fan. See the Applications Notes section for more tachometer information. Note that the 16-bit tachometer MSB and LSB register addresses are in reverse order from the 16 bit temperature readings.
48	R/W	7:2	0xFF	TACHL5:TACL0	
	R/W	1:0		[Reserved]	These bits are not used and write 0 or 1.

Local Temperature and Local High Setpoint Registers

Address Hex	Read/ Write	Bits	POR Value	Name	Description
00_{HEX} LOCAL TEMPERATURE REGISTER (8-bits)					
00	R	7:0	N/A	LT7:LT0	Local Temperature Reading (8-bit) 8-bit integer representing the temperature of the LM96163 die. LT7 is the SIGN bit LT6 has a bit weight of 64°C LT5 has a bit weight of 32°C LT4 has a bit weight of 16°C LT3 has a bit weight of 8°C LT2 has a bit weight of 4°C LT1 has a bit weight of 2°C LT0 has a bit weight of 1°C
05 $(0B)_{HEX}$ LOCAL HIGH SETPOINT REGISTER (8-bits)					
05	R/W	7:0	0x46 (70°)	LHS7:LHS0	Local HIGH Setpoint High Setpoint for the internal diode. LHS7 is the SIGN bit LHS6 has a bit weight of 64°C LHS5 has a bit weight of 32°C LHS4 has a bit weight of 16°C LHS3 has a bit weight of 8°C LHS2 has a bit weight of 4°C LHS1 has a bit weight of 2°C LHS0 has a bit weight of 1°C

Remote Diode Temperature, Offset and Setpoint Registers

Address Hex	Read/ Write	Bits	POR Value	Name	Description
01_{HEX} AND 10_{HEX} SIGNED REMOTE DIODE TEMPERATURE REGISTERS					
01	R	7:0	N/A	RT12:RT5	Most Significant Byte of the Signed Remote Diode Temperature Reading The most significant 8-bits of the 2's complement value, representing the temperature of the remote diode connected to the LM96163. Bit 7 is the sign bit, bit 6 has a weight of 64°C, and bit 0 has a weight of 1°C. This byte to be read before the LSB.
10	R	7:3	N/A	RT4:RT0	Least Significant Byte of the Signed Remote Diode Temperature Reading This is the LSB of the 2's complement value, representing the temperature of the remote diode connected to the LM96163. RT4 has a weight 0.5°C, RT3 has a weight of 0.25°C, and RT2 has a weight of 0.125°C. If the digital filter is turned off RT1:RT0 have a value of 00 unless extended resolution (Reg 45h STFBE bit set) is enabled. If extended resolution is chosen, for readings greater than 127.875 RT1:RT0=11 and for other cases RT1:RT0=00. When the digital filter is turned on and extended resolution enabled: RT1 has a weight of 0.0625 and RT0 has a weight of 0.03125°C
		2:0	00	[Reserved]	These bits are unused and always read as 0.

Copyright © 2008–2013, Texas Instruments Incorporated

Address Hex	Read/ Write	Bits	POR Value	Name	Description
31_{HEX} AND 32_{HEX} UNSIGNED REMOTE DIODE TEMPERATURE REGISTERS					
31	R	7:0	N/A	RTU12:RTU5	Most Significant Byte of the Unsigned Format Remote Diode Temperature Reading The most significant 8-bits of the unsigned format value, representing the temperature of the remote diode connected to the LM96163. Bit 7 has a weight of 128°C, bit 6 has a weight of 64°C, and bit 0 has a weight of 1°C. This byte to be read before the LSB.
32	R	7:3	N/A	RUT4:RUT0	Least Significant Byte of the Unsigned Format Remote Diode Temperature Reading This is the LSB of the unsigned value, representing the temperature of the remote diode connected to the LM96163. Bit 4 has a weight 0.5°C, bit 3 has a weight of 0.25°C, and bit 2 has a weight of 0.125°C. if the digital filter is turned off RUT1:RUT0 have a value of 00. When the digital filter is turned on: bit 1 has a weight of 0.0625 and bit 0 has a weight of 0.03125°C
		2:0	00	[Reserved]	These bits are unused and always read as 0.
11_{HEX} AND 12_{HEX} REMOTE TEMPERATURE OFFSET REGISTERS					
11	R/W	7:0	0x00	RTO10:RTO3	Remote Temperature Offset (MSB and LSB) These registers contain the value added to or subtracted from the remote diode's reading to compensate for the different non-ideality factors of different processors, diodes, etc. The 2's complement value, in these registers is added to the output of the LM96163's ADC to form the temperature reading contained in registers 01 and 10. These registers have the same format as the MSB and LSB Remote Diode Temperature Reading registers with the digital filter off.
12	R/W	7:5	000	RTO2:RTO1	
	R	4:0	000	[Reserved]	These bits are not used and always read as 0.
07 $(0D)_{HEX}$ AND 13_{HEX} REMOTE HIGH SETPOINT REGISTERS					
07 (0D)	R/W	7:0	0x55 (85°C)	RHS10:RHS3	Remote HIGH Setpoint (MSB and LSB) High setpoint temperature for remote diode. Same format as **Unsigned Remote Temperature Reading** (registers 31 and 32) or **Signed Remote Temperature Reading** (registers 01 and 10) with the digital filter off. Is it programmable by the USF bit found in the Enhanced configuration Register.
13	R/W	7:5	000	RHS2:RHS0	
	R	4:0	0x00	[Reserved]	These bits are not used and always read as 0.
08 $(0E)_{HEX}$ AND 14_{HEX} REMOTE LOW SETPOINT REGISTERS					
08 (0E)	R/W	7:0	00 (0°C)	RTS10:RTS3	Remote LOW Setpoint (MSB and LSB) Low setpoint temperature for remote diode. Same format as **Signed Remote Temperature Reading** (registers 01 and 10) with the digital filter off.
14	R/W	7:5	000	RTS2:RTS0	
	R	4:0	0x00	[Reserved]	These bits are not used and always read as 0.
19_{HEX} REMOTE DIODE T_CRIT SETPOINT REGISTER					
19	R/W	7:0	0x6E (110° C)	RCS7:RCS0	Remote Diode T_CRIT Setpoint Limit This 8-bit integer stores the T_CRIT limit and is nominally 110°C. The value of this register can be locked by setting T_CRIT Limit Override (bit 1) in the Configuration register to a 0, then programming a new T_CRIT value into this register. The format of this register is programmable. When the USF bit in the Enhanced Configuration register is cleared: LCS7 is the SIGN bit LCS6 has a bit weight of 64°C LCS5 has a bit weight of 32°C LCS4 has a bit weight of 16°C LCS3 has a bit weight of 8°C LCS2 has a bit weight of 4°C LCS1 has a bit weight of 2°C LCS0 has a bit weight of 1°C

Copyright © 2008–2013, Texas Instruments Incorporated

Address Hex	Read/ Write	Bits	POR Value	Name	Description
21_{HEX} T_CRIT HYSTERESIS REGISTER					
21	R/W	7	0x0A (10°C)	RTH7	This bit is unused. OK to write 1 or 0.
		6:0		RTH6:RTH0	Remote Diode T_CRIT Hysteresis T_CRIT stays activated until the remote diode temperature goes below [(T_CRIT Limit)—(T_CRIT Hysteresis)]. RTH6 has a bit weight of 64°C RTH5 has a bit weight of 32°C RTH4 has a bit weight of 16°C RTH3 has a bit weight of 8°C RTH2 has a bit weight of 4°C RTH1 has a bit weight of 2°C RTH0 has a bit weight of 1°C
30_{HEX} REMOTE DIODE TruTherm ENABLE REGISTER					
30	R	7:2	0x00	[Reserved]	These bits are unused and always read as 0.
	R/W	1	1	RDTE	Remote Diode TruTherm Enable 0: TruTherm beta compensation technology is turned off. Use this mode when using an MMBT3904 as a thermal diode. 1: TruTherm beta compensation technology is turned on. Use this mode when sensing a thermal diode in an Intel processor on 45 nm or 65 nm process.
	R	0	0	[Reserved]	This bit is unused and always read as 0.
BF_{HEX} REMOTE DIODE TEMPERATURE FILTER AND COMPARATOR MODE					
BF	R/W	7:6	00	[Reserved]	These bits are unused and always write 0.
	R	5:3	000	[Reserved]	These bits are unused and always read as 0.
	R/W	2:1	00	RDTF1:RDTF0	Remote Diode Temperature Filter Control 00: Filter Disabled 01: Filter Level 2 (minimal filtering, same as 10; Like LM63, LM63 Level 1 not supported) 10: Filter Level 2 (minimal filtering, same as 01; like LM63, LM63 Level 1 not supported) 11: Filter Enhanced Level 2 (maximum filtering)
		0	0	ALT/CMP	Comparator Mode 0: the $\overline{\text{ALERT}}$ pin functions normally. 1: the $\overline{\text{ALERT}}$ pin behaves as a comparator, asserting itself when an ALERT condition exists, de-asserting itself when the ALERT condition goes away.

Copyright © 2008–2013, Texas Instruments Incorporated

ALERT Status and Mask Registers

Address Hex	Read/ Write	Bits	POR Value	Name	Description
02_{HEX} ALERT STATUS REGISTER (8-bits) (All Alarms are latched until read, then cleared if alarm condition was removed at the time of the read.)					
0x02	R	7	0	BUSY	Busy 0: the ADC is not converting. 1: the ADC is performing a conversion. This bit does not affect ALERT status.
		6	0	LHIGH	Local High Alarm 0: the internal temperature of the LM96163 is at or below the Local High Setpoint. 1: the internal temperature of the LM96163 is above the Local High Setpoint, and an ALERT is triggered.
		5	0	[Reserved]	This bit is unused and always read as 0.
		4	0	RHIGH	Remote High Alarm 0: the temperature of the Remote Diode is at or below the Remote High Setpoint. 1: the temperature of the Remote Diode is above the Remote High Setpoint, and an ALERT is triggered.
		3	0	RLOW	Remote Low Alarm 0: the temperature of the Remote Diode is at or above the Remote Low Setpoint. 1: the temperature of the Remote Diode is below the Remote Low Setpoint, and an ALERT is triggered.
		2	0	RDFA	Remote Diode Fault Alarm 0: the Remote Diode appears to be correctly connected. 1: the Remote Diode may be disconnected or shorted to ground. This Alarm does not trigger an ALERT or a TCRIT.
		1	0	RCRIT	Remote T_CRIT Alarm When this bit is a 0, the temperature of the Remote Diode is at or below the T_CRIT Limit. When this bit is a 1, the temperature of the Remote Diode is above the T_CRIT Limit, ALERT and TCRIT are triggered.
		0	0	TACH	Tach Alarm When this bit is a 0, the Tachometer count is lower than or equal to the Tachometer Limit (the RPM of the fan is greater than or equal to the minimum desired RPM). When this bit is a 1, the Tachometer count is higher than the Tachometer Limit (the RPM of the fan is less than the minimum desired RPM), and an ALERT is triggered.
16_{HEX} ALERT MASK REGISTER (8-bits)					
16	R	7	1	[Reserved]	This bit is unused and always read as 1.
	R/W	6	0	LHAM	Local High Alarm Mask 0: a Local High Alarm event will generate an ALERT. 1: a Local High Alarm will not generate an ALERT
	R	5	1	[Reserved]	This bit is unused and always read as 1.
	R/W	4	0	RHAM	Remote High Alarm Mask 0: Remote High Alarm event will generate an ALERT. 1: a Remote High Alarm event will not generate an ALERT.
		3	0	RLAM	Remote Low Alarm Mask 0: a Remote Low Alarm event will generate an ALERT. 1: a Remote Low Alarm event will not generate an ALERT.
	R	2	1	[Reserved]	This bit is unused and always read as 1.
	R/W	1	0	RTAM	Remote T_CRIT Alarm Mask 0: a Remote T_CRIT event will generate an ALERT. 1: a Remote T_CRIT event will not generate an ALERT.
		0	0	TCHAM	TACH Alarm Mask When this bit is a 0, a Tach Alarm event will generate an ALERT. When this bit is a 1, a Tach Alarm event will not generate an ALERT.
33_{HEX} POWER ON RESET STATUS REGISTER					
33	R	7	—	NR	Power On Reset Status 0: Power On Reset cycle over part ready 1: Power On Reset cycle in progress part not ready
		6:0		[Reserved]	These bits are unused and will always report 0.

Copyright © 2008–2013, Texas Instruments Incorporated

Conversion Rate and One-Shot Registers

Address Hex	Read/ Write	Bits	POR Value	Name	Description
04 (0A)$_{HEX}$ CONVERSION RATE REGISTER (8-bits)					
04 (0A)	R	7:4	0x08	[Reserved]	These bits are unused and will always be set to 0.
	R/W	3:0		CONV3:CONV0	Conversion Rate Sets the conversion rate of the LM96163. 0000 = 0.05 Hz 0001 = 0.1 Hz 0010 = 0.204 Hz 0011 = 0.406 Hz 0100 = 0.813 Hz 0101 = 1.625 Hz 0110 = 3.25 Hz 0111 = 6.5 Hz 1000 = 13 Hz 1001 = 26 Hz All other values = 26 Hz
0F$_{HEX}$ ONE-SHOT REGISTER (8-bits)					
0F	Write Only	7:0	N/A		One Shot Trigger With the LM96163 in the STANDBY mode a single write to this register will initiate one complete temperature conversion cycle. Any value may be written.

ID Registers

Address Hex	Read/ Write	Bits	POR Value	Name	Description
FE$_{HEX}$ MANUFACTURER'S ID REGISTER (8-bits)					
FE	R	7:0	0x01	Manufacturer's ID	0x01 = National Semiconductor
FF$_{HEX}$ STEPPING / DIE REVISION ID REGISTER (8-bits)					
FF	R	7:0	0x49	Stepping/Die Revision ID	Version of LM96163

Copyright © 2008–2013, Texas Instruments Incorporated

APPLICATION NOTES

FAN CONTROL DUTY CYCLE VS. REGISTER SETTINGS AND FREQUENCY

NOTE

The following table is true only when the 22.5 kHz PWM frequency high resolution duty cycle is not selected.

PWM Freq 4D [4:0]	Step Resolution, %	PWM Value 4C [5:0] for 100%	PWM Value 4C [5:0] for about 75%	PWM Value 4C [5:0] for 50%	PWM Freq at 360 kHz Internal Clock, kHz	PWM Freq at 1.4 kHz Internal Clock, Hz	Actual Duty Cycle, % When 75% is Selected
0	Address 0 is mapped to Address 1						
1	50	2	1	1	180.0	703.1	50.0
2	25	4	3	2	90.00	351.6	75.0
3	16.7	6	5	3	60.00	234.4	83.3
4	12.5	8	6	4	45.00	175.8	75.0
5	10.0	10	8	5	36.00	140.6	80.0
6	8.33	12	9	6	30.00	117.2	75.0
7	7.14	14	11	7	25.71	100.4	78.6
8	6.25	16	12	8	22.50	87.9	75.0
9	5.56	18	14	9	20.00	78.1	77.8
10	5.00	20	15	10	18.00	70.3	75.0
11	4.54	22	17	11	16.36	63.9	77.27
12	4.16	24	18	12	15.00	58.6	75.00
13	3.85	26	20	13	13.85	54.1	76.92
14	3.57	28	21	14	12.86	50.2	75.00
15	3.33	30	23	15	12.00	46.9	76.67
16	3.13	32	24	16	11.25	43.9	75.00
17	2.94	34	26	17	10.59	41.4	76.47
18	2.78	36	27	18	10.00	39.1	75.00
19	2.63	38	29	19	9.47	37.0	76.32
20	2.50	40	30	20	9.00	35.2	75.00
21	2.38	42	32	21	8.57	33.5	76.19
22	2.27	44	33	22	8.18	32.0	75.00
23	2.17	46	35	23	7.82	30.6	76.09
24	2.08	48	36	24	7.50	29.3	75.00
25	2.00	50	38	25	7.20	28.1	76.00
26	1.92	52	39	26	6.92	27.0	75.00
27	1.85	54	41	27	6.67	26.0	75.93
28	1.79	56	42	28	6.42	25.1	75.00
29	1.72	58	44	29	6.21	24.2	75.86
30	1.67	60	45	30	6.00	23.4	75.00
31	1.61	62	47	31	5.81	22.7	75.81

Copyright © 2008–2013, Texas Instruments Incorporated

NOTE

The following table is true only when the 22.5 kHz PWM frequency with high resolution duty cycle is selected by setting bit 4 (PHR) of the Enhanced Configuration register (0x45), clearing bit 3 (PWCKSL) of the PWM and RPM Configuration register (0x4A) and setting PWM Frequency (0x4D) register to 0x08.

PWM Freq 4D [4:0]	Step Resolution, %	PWM Value 4C [7:0] for 100% (Hex)	PWM Value 4C [7:0] for about 75% (Hex)	PWM Value 4C [7:0] for 50% (Hex)	PWM Freq at 360 kHz Internal Clock, kHz	PWM Freq at 1.4 kHz Internal Clock, Hz	Actual Duty Cycle, % When Approximately 75% is Selected
8	0.392	FF	BF	80	22.50	Not Available	74.902

Computing Duty Cycles for a Given Frequency

Select a PWM Frequency from the first column corresponding to the desired actual frequency in columns 6 or 7. Note the PWM Value for 100% Duty Cycle.

Find the Duty Cycle by taking the PWM Value of Register 4C and computing:

$$DutyCycle\ _(\%) = \frac{PWM\ _Value}{PWM\ _Value\ _\ for\ _100\%} \times 100\% \quad (1)$$

Example: For a PWM Frequency of 24, a PWM Value at 100% = 48 and PWM Value actual = 28, then the Duty Cycle is (28/48) × 100% = **58.3%**.

LUT FAN CONTROL

The LM96163 fan control uses a temperature to duty cycle look-up table (LUT) that has 12 indexes. High resolution duty cycle (0.392%) is available when the PWM frequency is set to 22.5 kHz. In addition ramp rate control is available to acoustically smooth the duty cycle transition between LUT steps.

Shown in Figure 14 (a) is an example of the 12-point LUT temperature to PWM transfer function that can be realized without smoothing enabled. The table is comprised of twelve Duty-Cycle and Temperature set-point pairs. Notice that the transitions between one index of the LUT to the next happen instantaneously. If the PWM levels are set far enough apart this can be acoustically very disturbing. The typical acoustical threshold of change in duty cycle is 2%. Figure 14 (b) has an overlaid curve (solid line) showing what occurs at the transitions when smoothing is enabled. The dashed lines shown in Figure 14 (b) are there to point out that multiple slopes can be realized easily. At the transitions the duty cycle increments in LSb (0.39% for the case shown) steps. In the example shown in Figure 14 (b) the first pair is set for a duty-cycle of 31.25% and a temperature of 0°C. For temperatures less than 0°C the duty cycle is set to 0. When the temperature is greater than 0 °C but is less than 91 °C the duty cycle will remain at 31.25%. The next pair is set at 37.5% and 91°C. Once the temperature exceeds 91°C the duty cycle on the PWM output will gradually transition from 31.25% to 37.5% in 0.39% steps at the programmed time interval. The LUT comparison temperature resolution is programmable to either 1 °C or 0.5 °C. For the curves of Figure 14 the comparison resolution is set to 0.5 °C that is why the actual duty cycle transitions happen 0.5 °C higher than the actual LUT entry. The duty cycle transition time interval is programmable and is shown in the table titled Table 8. Care should be taken so that the LUT PWM and Temperature values are setup in ascending weight.

Copyright © 2008–2013, Texas Instruments Incorporated

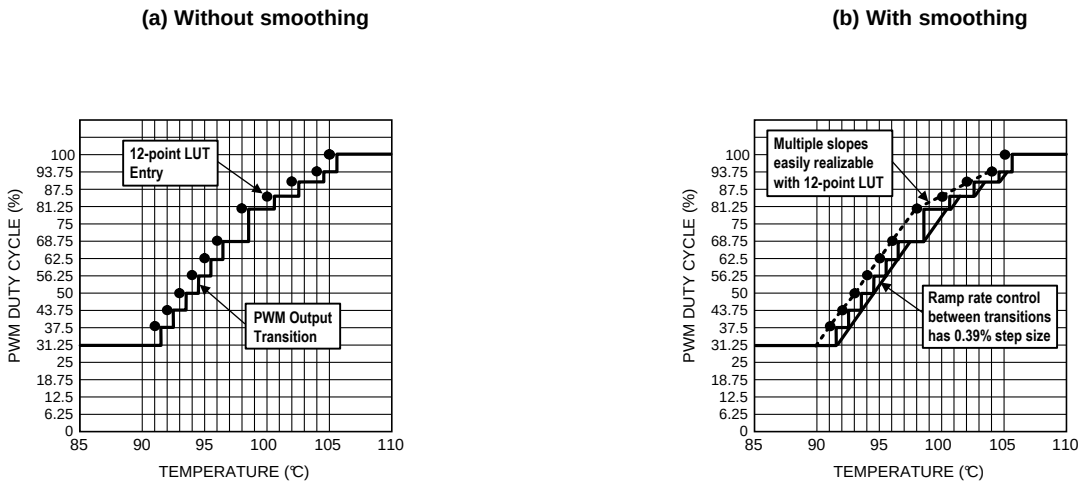


Figure 14. Fan Control Transfer Function Example

Also included is programmable hysteresis that is not described by the curves of Figure 14. The hysteresis takes effect as temperature is decreasing and moves all the temperature set-points down by the programmed amount. For the example shown here if the hysteresis is set to 1°C and if the temperature is decreasing from 96.5°C the duty cycle will remain at 68.75% and will not transition to 62.5% until the temperature drops below 95.5°C.

If at any time the TCRIT output were to activate the PWM duty cycle will be instantaneously forced to 100% thus forcing the fans to full on.

Table 8. PWM Smoothing Time Intervals

Time Interval (seconds)	0-100% DC Time	
	w/ 6.25% resolution (seconds)	w/ 0.39% resolution Seconds
0.182	2.913	43.7
0.091	1.456	21.6
0.046	0.728	10.9
0.023	0.364	5.45

The Table 8 table describes the programmable time interval preventing abrupt changes in the PWM output duty cycle and thus preventing abrupt acoustical noise changes as well. The threshold of acoustically detecting fan noise transition is at about a 2% duty cycle change. The table describes the time intervals that can be programmed and the total amount of time it will take for the PWM output to change from 0% to 100% for each time interval. For example if the time interval for each step is set to 0.091 seconds the time it will take to make a 0 to 100% duty cycle change will be 21.6 seconds when the duty cycle resolution is set to 0.39% or 1.46 seconds when the resolution is 6.25%. One setting will apply to all LUT transitions.

COMPUTING RPM OF THE FAN FROM THE TACH COUNT

The Tach Count Registers 46_{HEX} and 47_{HEX} count the number of periods of the 90 kHz tachometer clock in the LM96163 for the tachometer input from the fan assuming a 2 pulse per revolution fan tachometer, such as the fans supplied with the Intel boxed processors. The RPM of the fan can be computed from the Tach Count Registers 46_{HEX} and 47_{HEX}. This can best be shown through an example.

Example:

Given: the fan used has a tachometer output with 2 per revolution.

Let:

Register 46 (LSB) is BF_{HEX} = Decimal (11 x 16) + 15 = 191 and

Register 47 (MSB) is 7_{HEX} = Decimal (7 x 256) = 1792.

The total Tach Count, in decimal, is 191 + 1792 = **1983**.

The RPM is computed using the formula

$$Fan_RPM = \frac{f \times 5,400,000}{Total_Tach_Count_(Decimal)}, \quad (2)$$

where

f = 1 for 2 pulses/rev fan tachometer output;

f = 2 for 1 pulse/rev fan tachometer output, and

f = 2 / 3 for 3 pulses/rev fan tachometer output

For our example

$$Fan_RPM = \frac{1 \times 5,400,000}{1983} = 2723_RPM \quad (3)$$

DIODE NON-IDEALITY

The LM96163 can be applied easily in the same way as other integrated-circuit temperature sensors, and its remote diode sensing capability allows it to be used in new ways as well. It can be soldered to a printed circuit board, and because the path of best thermal conductivity is between the die and the pins, its temperature will effectively be that of the printed circuit board lands and traces soldered to the LM96163's pins. This presumes that the ambient air temperature is almost the same as the surface temperature of the printed circuit board; if the air temperature is much higher or lower than the surface temperature, the actual temperature of the LM96163 die will be at an intermediate temperature between the surface and air temperatures. Again, the primary thermal conduction path is through the leads, so the circuit board temperature will contribute to the die temperature much more strongly than will the air temperature.

The LM96163 incorporates remote diode temperature sensing technology allowing the measurement of remote temperatures. This diode can be located on the die of a target IC, allowing measurement of the IC's temperature, independent of the LM96163's die temperature. A discrete diode can also be used to sense the temperature of external objects or ambient air. Remember that a discrete diode's temperature will be affected, and often dominated, by the temperature of its leads. Most silicon diodes do not lend themselves well to this application. It is recommended that an MMBT3904 transistor base emitter junction be used with the collector tied to the base.

The LM96163's TruTherm BJT beta compensation technology allows accurate sensing of integrated thermal diodes, such as those found on most processors. With TruTherm technology turned off, the LM96163 can measure a diode-connected transistor such as the MMBT3904 or the thermal diode found in an AMD processor.

The LM96163 has been optimized to measure the remote thermal diode integrated in a typical Intel processor on 45nm, 65 nm or 90 nm process or an MMBT3904 transistor. Using the Remote Diode TruTherm Enable register the remote input can be optimized for a typical Intel processor on 45nm, 65 nm or 90 nm process or an MMBT3904.

Diode Non-Ideality Factor Effect on Accuracy

When a transistor is connected as a diode, the following relationship holds for variables V_{BE}, T and I_F:

$$I_F = I_S \times \left[e^{\left(\frac{V_{BE}}{\eta \times V_t} \right)} - 1 \right] \quad (4)$$

where:

$$V_t = \frac{kT}{q} \quad (5)$$

Copyright © 2008–2013, Texas Instruments Incorporated

- q = 1.6×10^{-19} Coulombs (the electron charge),
- T = Absolute Temperature in Kelvin
- k = 1.38×10^{-23} joules/K (Boltzmann's constant),
- η is the non-ideality factor of the process the diode is manufactured on,
- I_S = Saturation Current and is process dependent,
- I_f = Forward Current through the base-emitter junction
- V_{BE} = Base-Emitter Voltage drop

In the active region, the -1 term is negligible and may be eliminated, yielding the following equation

$$I_F = I_S \times \left[e^{\left(\frac{V_{BE}}{\eta \times V_t} \right)} \right] \tag{6}$$

In Equation 6, η and I_S are dependant upon the process that was used in the fabrication of the particular diode. By forcing two currents with a very controlled ratio(I_{F2} / I_{F1}) and measuring the resulting voltage difference, it is possible to eliminate the I_S term. Solving for the forward voltage difference yields the relationship:

$$\Delta V_{BE} = \eta \times \left(\frac{kT}{q} \right) \times \ln \left(\frac{I_{F2}}{I_{F1}} \right) \tag{7}$$

Solving Equation 7 for temperature yields:

$$T = \frac{q \times \Delta V_{BE}}{\eta \times k \times \ln \left(\frac{I_{F2}}{I_{F1}} \right)} \tag{8}$$

Equation 8 holds true when a diode connected transistor such as the MMBT3904 is used. When this “diode” equation is applied to an integrated diode such as a processor transistor with its collector tied to GND as shown in Figure 15 it will yield a wide non-ideality spread. This wide non-ideality spread is not due to true process variation but due to the fact that Equation 8 is an approximation.

TruTherm BJT beta compensation technology uses the transistor equation, Equation 9, which is a more accurate representation of the topology of the thermal diode found in an FPGA or processor.

$$T = \frac{q \times \Delta V_{BE}}{\eta \times k \times \ln \left(\frac{I_{C2}}{I_{C1}} \right)} \tag{9}$$

TruTherm should only be enabled when measuring the temperature of a transistor integrated as shown in the processor of Figure 15, because Equation 9 only applies to this topology.

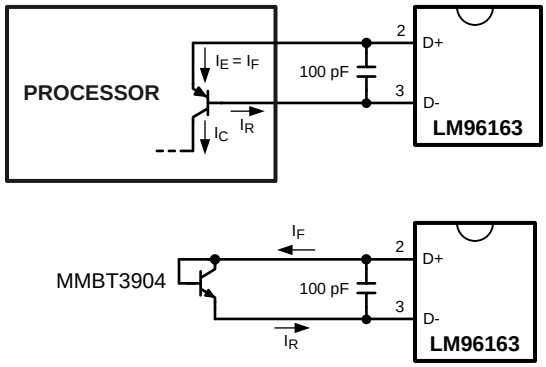


Figure 15. Thermal Diode Current Paths

Calculating Total System Accuracy

The voltage seen by the LM96163 also includes the $I_F R_S$ voltage drop of the series resistance. The non-ideality factor, η, is the only other parameter not accounted for and depends on the diode that is used for measurement. Since ΔV_{BE} is proportional to both η and T, the variations in η cannot be distinguished from variations in temperature. Since the non-ideality factor is not controlled by the temperature sensor, it will directly add to the inaccuracy of the sensor. For the for Intel processor on 65nm process, Intel specifies a +4.06%/−0.897% variation in η from part to part when the processor diode is measured by a circuit that assumes diode equation, Equation 8, as true. As an example, assume a temperature sensor has an accuracy specification of ±1.0°C at a temperature of 80°C (353 Kelvin) and the processor diode has a non-ideality variation of +4.06%/−0.89%. The resulting system accuracy of the processor temperature being sensed will be:

$$T_{ACC} = + 1.0°C + (+4.06\% \text{ of } 353 \text{ K}) = +15.3 °C \quad (10)$$

and

$$T_{ACC} = - 1.0°C + (-0.89\% \text{ of } 353 \text{ K}) = -4.1 °C \quad (11)$$

TruTherm technology uses the transistor equation, Equation 8, resulting in a non-ideality spread that truly reflects the process variation which is very small. The transistor equation non-ideality spread is ±0.39% for the 65nm thermal diode. The resulting accuracy when using TruTherm technology improves to:

$$T_{ACC} = \pm 0.75°C + (\pm 0.39\% \text{ of } 353 \text{ K}) = \pm 2.16 °C \quad (12)$$

Intel does not specify the diode model ideality and series resistance of the thermal diodes on 45nm so a similar comparison cannot be calculated, but lab experiments have shown similar improvement. For the 45nm processor the ideality spread as specified by Intel is -0.399% to +0.699%. The resulting spread in accuracy when using TruTherm technology with the thermal diode on Intel processors with 45nm process is:

$$T_{ACC} = -0.75°C + (-0.39\% \text{ of } 353 \text{ K}) = -2.16 °C \quad (13)$$

to

$$T_{ACC} = +0.75°C + (+0.799\% \text{ of } 353 \text{ K}) = +4.32 °C \quad (14)$$

The next error term to be discussed is that due to the series resistance of the thermal diode and printed circuit board traces. The thermal diode series resistance is specified on most processor data sheets. For Intel processors in 45 nm process, this is specified at 4.5Ω typical with a minimum of 3Ω and a maximum of 7Ω. The LM96163 accommodates the typical series resistance of Intel Processor on 45 nm process. The error that is not accounted for is the spread of the processor's series resistance. The equation used to calculate the temperature error due to series resistance (T_{ER}) for the LM96163 is simply:

$$T_{ER} = \left(0.62 \frac{°C}{\Omega}\right) \text{x } R_{PCB} \quad (15)$$

Solving Equation 15 for R_{PCB} equal to -1.5Ω to 2.5Ω results in the additional error due to the spread in this series resistance of -0.93°C to +1.55°C. The spread in error cannot be canceled out, as it would require measuring each individual thermal diode device. This is quite difficult and impractical in a large volume production environment.

Equation 15 can also be used to calculate the additional error caused by series resistance on the printed circuit board. Since the variation of the PCB series resistance is minimal, the bulk of the error term is always positive and can simply be cancelled out by subtracting it from the output readings of the LM96163 using the Remote Temperature Offset register.

Processor Family	Transistor Equation η_T, non-ideality			Series R,Ω
	min	typ	max	
Intel Processor on 45 nm process	0.997	1.001	1.008	4.5
Intel Processor on 65 nm process	0.997	1.001	1.005	4.52

Copyright © 2008–2013, Texas Instruments Incorporated

PCB LAYOUT FOR MINIMIZING NOISE

Figure 16. Ideal Diode Trace Layout

In a noisy environment, such as a processor mother board, layout considerations are very critical. Noise induced on traces running between the remote temperature diode sensor and the LM96163 can cause temperature conversion errors. Keep in mind that the signal level the LM96163 is trying to measure is in microvolts. The following guidelines should be followed:

1. Use a low-noise +3.3VDC power supply, and bypass to GND with a 0.1 µF ceramic capacitor in parallel with a 100 pF ceramic capacitor. The 100 pF capacitor should be placed as close as possible to the power supply pin. A bulk capacitance of 10 µF needs to be in the vicinity of the LM96163's V_{DD} pin.
2. A 100 pF diode bypass capacitor is recommended to filter high frequency noise but may not be necessary. Place the recommended 100 pF diode capacitor as close as possible to the LM96163's D+ and D− pins. Make sure the traces to the 100 pF capacitor are matched. The LM96163 can handle capacitance up to 3 nF placed between the D+ and D- pins, see Typical Performance Characteristics curves titled *Remote Temperature Reading Sensitivity to Thermal Diode Filter Capacitance*.
3. Ideally, the LM96163 should be placed within 10 cm of the Processor diode pins with the traces being as straight, short and identical as possible. Trace resistance of 1 Ω can cause as much as 0.62°C of error. This error can be compensated by using the Remote Temperature Offset Registers, since the value placed in these registers will automatically be subtracted from or added to the remote temperature reading.
4. Diode traces should be surrounded by a GND guard ring to either side, above and below if possible. This GND guard should not be between the D+ and D− lines. In the event that noise does couple to the diode lines it would be ideal if it is coupled common mode. That is equally to the D+ and D− lines.
5. Avoid routing diode traces in close proximity to power supply switching or filtering inductors.
6. Avoid running diode traces close to or parallel to high speed digital and bus lines. Diode traces should be kept at least 2 cm apart from the high speed digital traces.
7. If it is necessary to cross high speed digital traces, the diode traces and the high speed digital traces should cross at a 90 degree angle.
8. The ideal place to connect the LM96163's GND pin is as close as possible to the Processor's GND associated with the sense diode.
9. Leakage current between D+ and GND should be kept to a minimum. Thirteen nano-amperes of leakage can cause as much as 0.2°C of error in the diode temperature reading. Keeping the printed circuit board as clean as possible will minimize leakage current.

Noise coupling into the digital lines greater than 400 mVp-p (typical hysteresis) and undershoot less than 500 mV below GND, may prevent successful SMBus communication with the LM96163. SMBus no acknowledge is the most common symptom, causing unnecessary traffic on the bus. Although the SMBus maximum frequency of communication is rather low (100 kHz max), care still needs to be taken to ensure proper termination within a system with multiple parts on the bus and long printed circuit board traces. An RC lowpass filter with a 3 dB corner frequency of about 40 MHz is included on the LM96163's SMBCLK input. Additional resistance can be added in series with the SMBDAT and SMBCLK lines to further help filter noise and ringing. Minimize noise coupling by keeping digital traces out of switching power supply areas as well as ensuring that digital lines containing high speed data communications cross at right angles to the SMBDAT and SMBCLK lines.

Copyright © 2008–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision C (May 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	41

Copyright © 2008–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM96163CISD/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	T63C	Samples
LM96163CISDX/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	T63C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

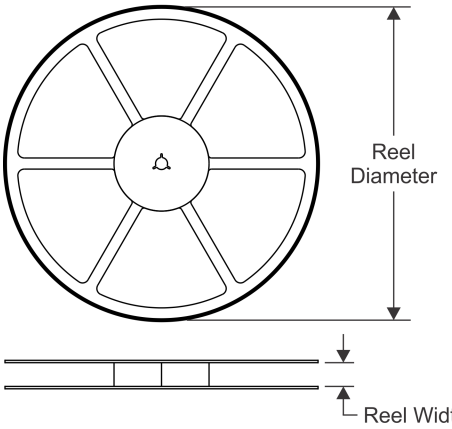
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

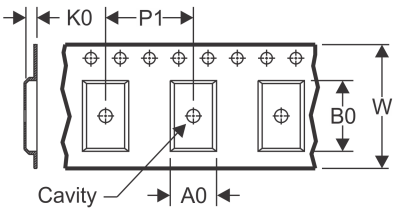
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

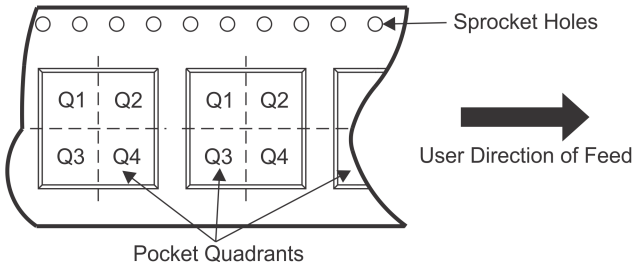


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

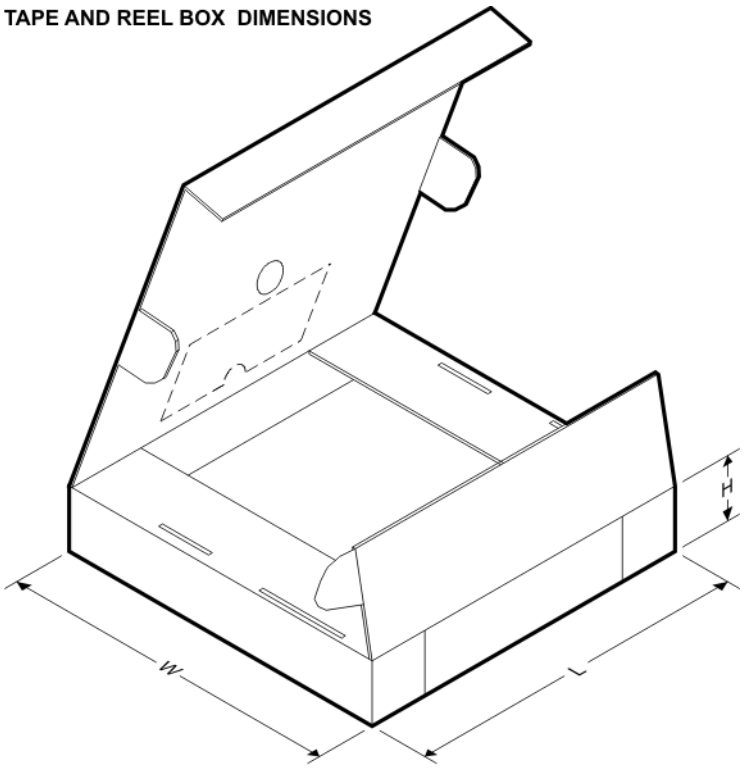
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM96163CISD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM96163CISDX/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

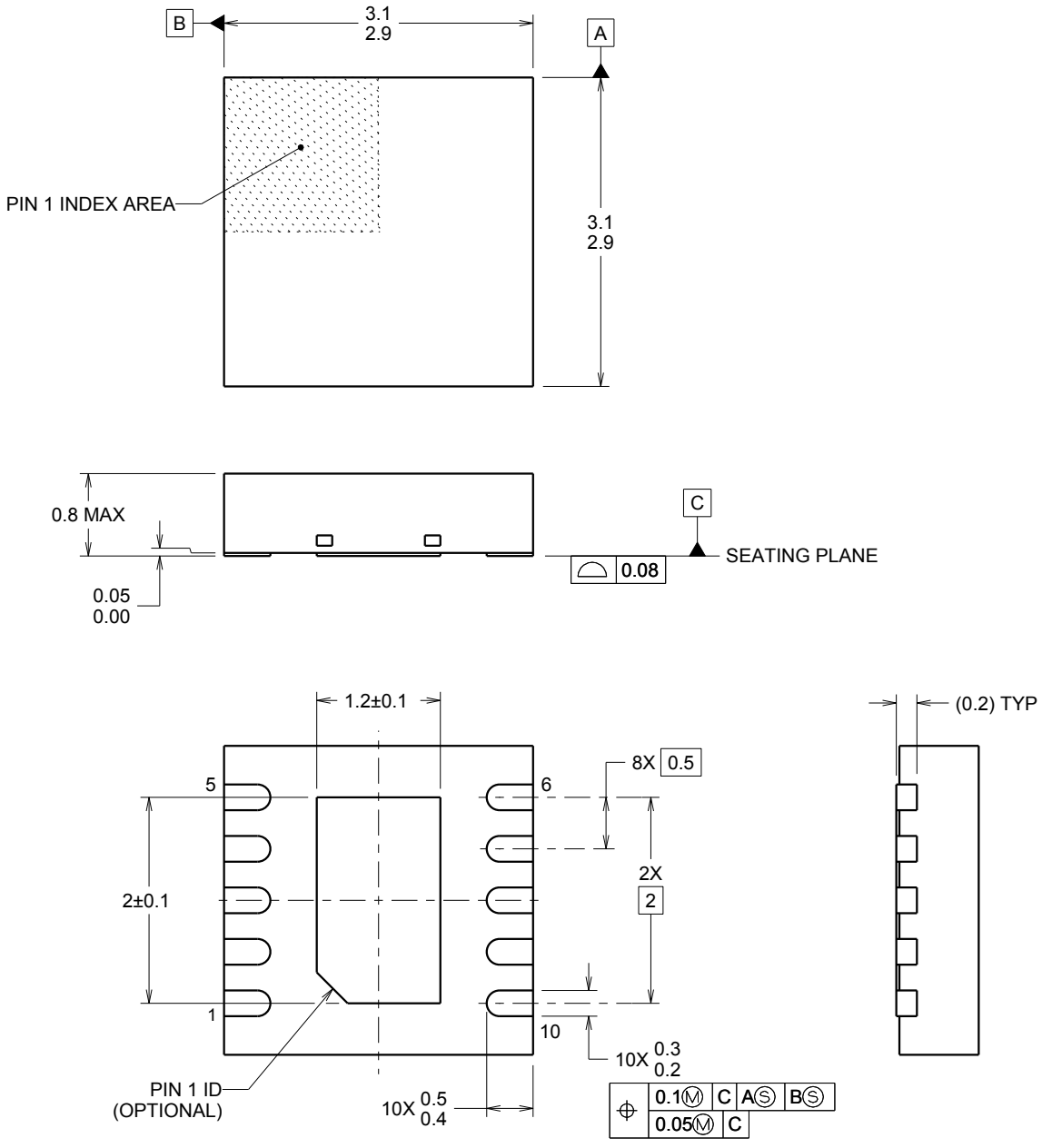
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM96163CISD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LM96163CISDX/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0

PACKAGE OUTLINE

DSC0010B

WSON - 0.8 mm max height

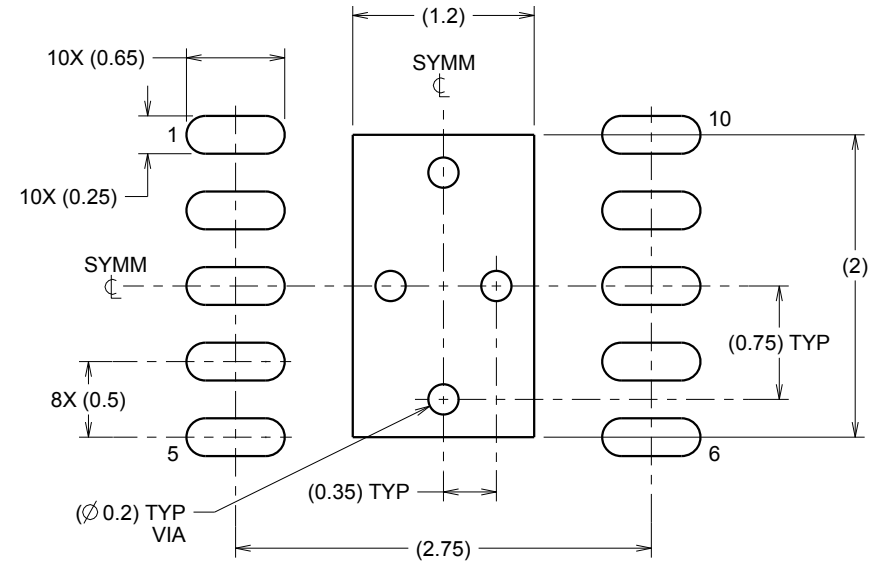
PLASTIC SMALL OUTLINE - NO LEAD



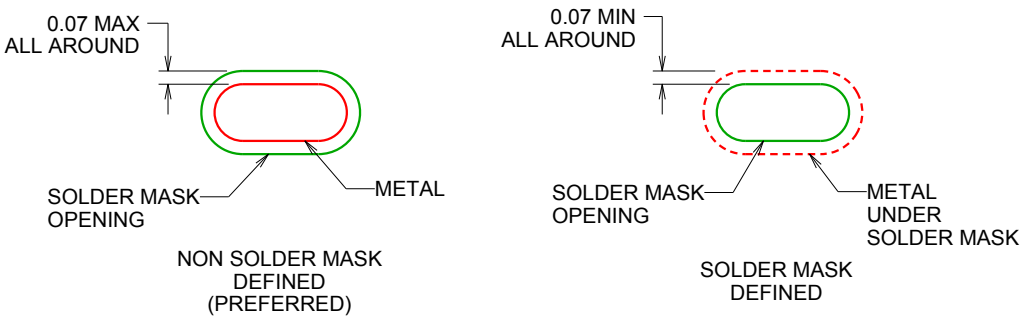
4214926/A 07/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

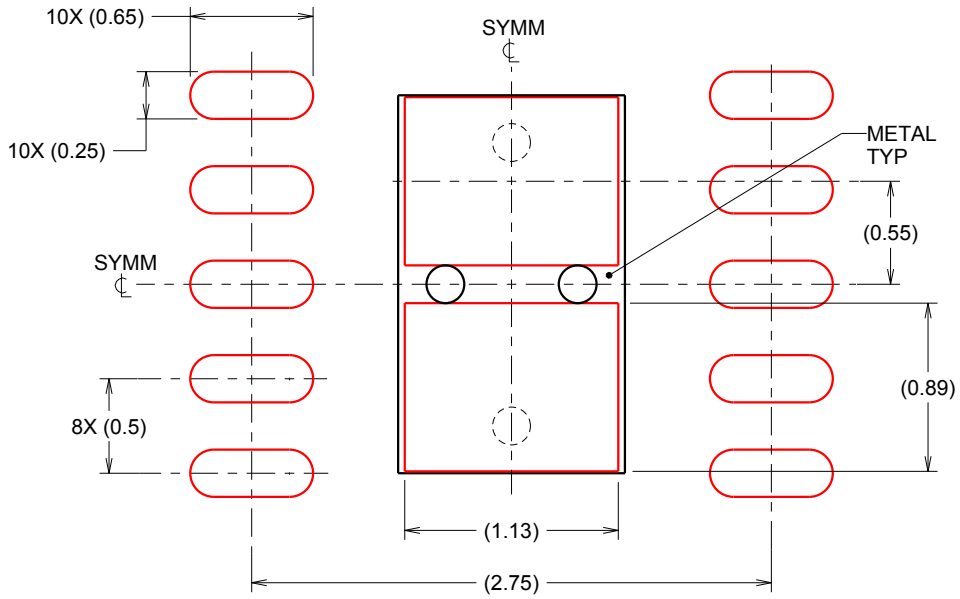


SOLDER MASK DETAILS

4214926/A 07/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4214926/A 07/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View LM96163CISD/NOPB on WIN SOURCE
- Texas Instruments Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management