



**THE DATASHEET OF  
LM810M3X-2.93**





## LM809/LM810 3-Pin Microprocessor Reset Circuits

### 1 Features

- Precision Monitoring of Supply Voltages
  - Available Threshold Options:  
2.63 V, 2.93 V, 3.08 V, 4.38 V, 4.63 V
- Superior Upgrade to MAX809 and MAX810
- Fully Specified Over Temperature
- 140-ms Minimum Power-On Reset Pulse Width, 240-ms Typical
  - Active-Low  $\overline{\text{RESET}}$  Output (LM809)
  - Active-High RESET Output (LM810)
- Ensured RESET Output Valid for  $V_{CC} \geq 1 \text{ V}$
- Low Supply Current, 15- $\mu\text{A}$  Typical
- Power Supply Transient Immunity

### 2 Applications

- Factory Automation
- Building Automation
- Programmable Logic Control
- Renewable Energy
- Microprocessor Systems
- Computers
- Controllers
- Intelligent Instruments
- Portable/Battery-Powered Equipment
- Automotive

### 3 Description

The LM809 and LM810 microprocessors supervisory circuits can be used to monitor the power supplies in microprocessor and digital systems. They provide a reset to the microprocessor during power-up, power-down and brown-out conditions.

The function of the LM809 and LM810 are to monitor the  $V_{CC}$  supply voltage, and assert a reset signal whenever this voltage declines below the factory-programmed reset threshold. The reset signal remains asserted for 240 ms after  $V_{CC}$  rises above the threshold. The LM809 has an active-low  $\overline{\text{RESET}}$  output, while the LM810 has an active-high RESET output.

Seven standard reset voltage options are available, suitable for monitoring 5-V, 3.3-V, and 3-V supply voltages.

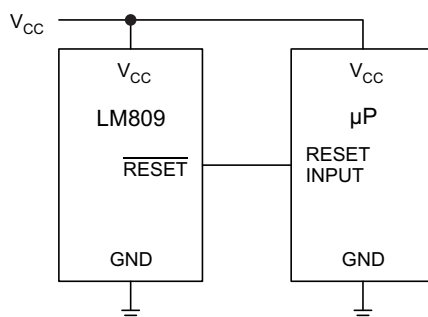
With a low supply current of only 15  $\mu\text{A}$ , the LM809 and LM810 are ideal for use in portable equipment.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM809, LM810	SOT-23 (3)	2.92 mm x 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Typical Application for Microprocessor Reset Circuit



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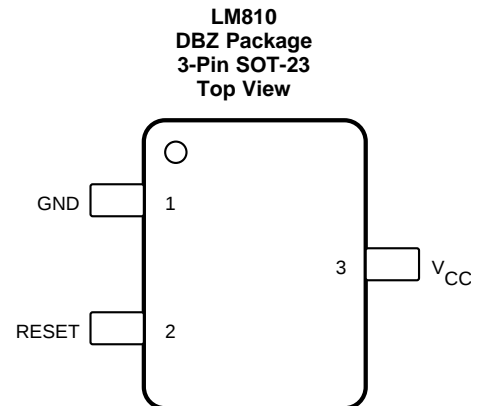
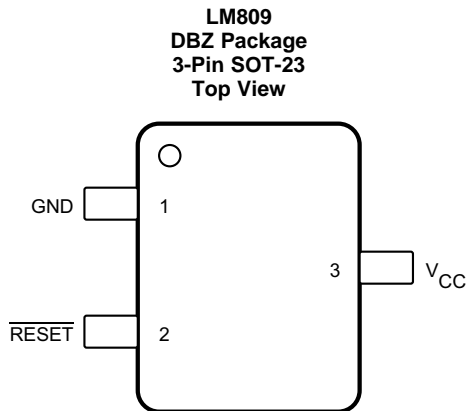
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (May 2013) to Revision E</b>	<b>Page</b>
• Removed the SON package.....	1
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....	1

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	LM809	LM810		
	$\overline{\text{RESET}}$	2		
RESET	—	2	O	Active-high output. RESET remains high while $V_{CC}$ is below the reset threshold, and for 240 ms after $V_{CC}$ rises above the reset threshold.
$V_{CC}$	3	3	I	Supply voltage
GND	1	1	—	Ground reference

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 see <sup>(1)(2)</sup>

		MIN	MAX	UNIT
Input supply voltage	$V_{CC}$	-0.3	6	V
Output voltage	RESET, $\overline{\text{RESET}}$	-0.3	$V_{CC} + 0.3$	V
Input current	$V_{CC}$		20	mA
Output current	RESET, $\overline{\text{RESET}}$		20	mA
Rate of rise	$V_{CC}$		100	V/ $\mu$ s
Continuous power dissipation			320	mW
Lead temperature (soldering, 10 s)			300	$^{\circ}$ C
Ambient temperature range, $T_A$		-40	105	$^{\circ}$ C
Maximum junction temperature, $T_{J(\text{MAX})}$			125	$^{\circ}$ C
Storage temperature, $T_{\text{stg}}$		-65	160	$^{\circ}$ C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(\text{ESD})}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 2000$
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	$\pm 200$

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as  $\pm 2000$  V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as  $\pm 200$  V may actually have higher performance.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT	
$V_{CC}$	Input voltage range	$T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C}$	1.0		5.5	V	
		$T_A = -40^{\circ}\text{C to } 105^{\circ}\text{C}$	1.2		5.5		
$I_{CC}$	Supply Current	$V_{CC} < 5.5$ V, LM8xx: 4.63, 4.38, 4.00	$T_A = -40^{\circ}\text{C to } 85^{\circ}\text{C}$		18	$\mu$ A	
			$T_A = 85^{\circ}\text{C to } 105^{\circ}\text{C}$		100		
		$V_{CC} < 3.6$ V, LM8xx: 3.08, 2.93, 2.63, 2.45	$T_A = -40^{\circ}\text{C to } 85^{\circ}\text{C}$		15		50
			$T_A = 85^{\circ}\text{C to } 105^{\circ}\text{C}$				100

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM809, LM810	UNIT
		DBZ (SOT-23)	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	252.0	$^{\circ}\text{C/W}$
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	113.3	$^{\circ}\text{C/W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	53.5	$^{\circ}\text{C/W}$
$\Psi_{JT}$	Junction-to-top characterization parameter	9.9	$^{\circ}\text{C/W}$
$\Psi_{JB}$	Junction-to-board characterization parameter	52.6	$^{\circ}\text{C/W}$
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	—	$^{\circ}\text{C/W}$

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

$V_{CC}$  = full range,  $T_A$  =  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ , unless otherwise noted. Typical values are at  $T_A = 25^{\circ}\text{C}$ ,  $V_{CC} = 5\text{ V}$  for 4.63, 4.38, and 4.00 versions,  $V_{CC} = 3.3\text{ V}$  for 3.08 and 2.93 versions, and  $V_{CC} = 3\text{ V}$  for 2.63 and 2.45 version<sup>(1)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
$V_{TH}$	Reset Threshold <sup>(2)</sup>	LM8xx: 4.63 V	$T_A = 25^{\circ}\text{C}$	4.56	4.63	4.70	V	
			$T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	4.50		4.75		
			$T_A = 85^{\circ}\text{C}$ to $105^{\circ}\text{C}$	4.40		4.86		
		LM8xx: 4.38 V	$T_A = 25^{\circ}\text{C}$	4.31	4.38	4.45		
			$T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	4.25		4.50		
			$T_A = 85^{\circ}\text{C}$ to $105^{\circ}\text{C}$	4.16		4.56		
		LM8xx: 4.00 V	$T_A = 25^{\circ}\text{C}$	3.93	4.00	4.06		
			$T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	3.89		4.10		
			$T_A = 85^{\circ}\text{C}$ to $105^{\circ}\text{C}$	3.80		4.20		
	LM8xx: 3.08 V	$T_A = 25^{\circ}\text{C}$	3.04	3.08	3.11			
		$T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	3.00		3.15			
		$T_A = 85^{\circ}\text{C}$ to $105^{\circ}\text{C}$	2.92		3.23			
	LM8xx: 2.93 V	$T_A = 25^{\circ}\text{C}$	2.89	2.93	2.96			
		$T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	2.85		3.00			
		$T_A = 85^{\circ}\text{C}$ to $105^{\circ}\text{C}$	2.78		3.08			
	LM8xx: 2.63 V	$T_A = 25^{\circ}\text{C}$	2.59	2.63	2.66			
		$T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	2.55		2.70			
		$T_A = 85^{\circ}\text{C}$ to $105^{\circ}\text{C}$	2.50		2.76			
	LM8xx: 2.45 V	$T_A = 25^{\circ}\text{C}$	2.41	2.45	2.49			
		$T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	2.38		2.52			
		$T_A = 85^{\circ}\text{C}$ to $105^{\circ}\text{C}$	2.33		2.57			
	Reset Threshold Temperature Coefficient				30			ppm/ $^{\circ}\text{C}$
	$V_{CC}$ to Reset Delay <sup>(2)</sup>		$V_{CC} = V_{TH}$ to $(V_{TH} - 100\text{ mV})$		20			$\mu\text{s}$
	Reset Active Timeout Period		$T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	140	240	560		ms
$T_A = 85^{\circ}\text{C}$ to $105^{\circ}\text{C}$			100		840			
$V_{OL}$	RESE $\overline{T}$ Output Voltage Low (LM809)	$V_{CC} = V_{TH(\text{min})}$ , $I_{\text{SINK}} = 1.2\text{ mA}$ , LM809: 2.45, 2.63, 2.93, 3.08			0.3	V		
		$V_{CC} = V_{TH(\text{min})}$ , $I_{\text{SINK}} = 3.2\text{ mA}$ , LM809: 4.63, 4.38, 4.00			0.4			
		$V_{CC} > 1\text{ V}$ , $I_{\text{SINK}} = 50\text{ }\mu\text{A}$			0.3			
	RESET Output Voltage Low (LM810)	$V_{CC} = V_{TH(\text{max})}$ , $I_{\text{SINK}} = 1.2\text{ mA}$ , LM810: 2.63, 2.93, 3.08			0.3			
$V_{CC} = V_{TH(\text{max})}$ , $I_{\text{SINK}} = 3.2\text{ mA}$ , LM810: 4.63, 4.38, 4.00				0.4				
$V_{OH}$	RESE $\overline{T}$ Output Voltage High (LM809)	$V_{CC} > V_{TH(\text{max})}$ , $I_{\text{SOURCE}} = 500\text{ }\mu\text{A}$ , LM809: 2.45, 2.63, 2.93, 3.08	$0.8 \times V_{CC}$			V		
		$V_{CC} > V_{TH(\text{max})}$ , $I_{\text{SOURCE}} = 800\text{ }\mu\text{A}$ , LM809: 4.63, 4.38, 4.00	$V_{CC} - 1.5$					
	RESET Output Voltage High (LM810)	$1.8\text{ V} < V_{CC} < V_{TH(\text{min})}$ , $I_{\text{SOURCE}} = 150\text{ }\mu\text{A}$	$0.8 \times V_{CC}$					

(1) Production testing done at  $T_A = 25^{\circ}\text{C}$ , over temperature limits specified by design only.

(2) RESE $\overline{T}$  Output for LM809, RESET output for LM810.

## 6.6 Typical Characteristics



**Figure 1. Supply Current vs Temperature (No Load, LM8xx: 2.63, 2.93, 3.08)**



**Figure 2. Supply Current vs Temperature (No Load, LM8xx: 4.63, 4.38)**



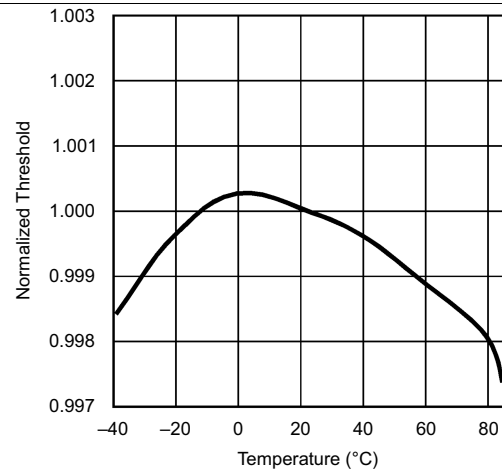
**Figure 3. Power-Down Reset Delay vs Temp (LM8xx: 2.63, 2.93, 3.08)**



**Figure 4. Power-Down Reset Delay vs Temperature (LM8xx: 4.63, 4.38)**



**Figure 5. Power-Up Reset Timeout vs Temperature**



**Figure 6. Normalized Reset Threshold vs Temperature**

## 7 Detailed Description

### 7.1 Overview

The LM809 and LM810 microprocessor supervisory circuits provide a simple solution to monitor the power supplies in microprocessor and digital systems and provide a reset during power-up, power-down, and brown-out conditions. The reset signal is controlled by the factory-programmed reset threshold on the  $V_{CC}$  supply voltage pin. When the voltage declines below the reset threshold, the reset signal is asserted and remains asserted for 240 ms after  $V_{CC}$  rises above the threshold. The LM809 has an active-low  $\overline{\text{RESET}}$  output, while the LM810 has an active-high RESET output. The available threshold options are 2.63 V, 2.93 V, 3.08 V, 4.38 V, and 4.63 V to provide precision monitoring of supply voltages.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Benefits of Precision Reset Thresholds

A microprocessor supply supervisor must provide a reset output within a predictable range of the supply voltage. A common threshold range is between 5% and 10% below the nominal supply voltage. The 4.63-V and 3.08-V options of the LM809 and LM810 use highly accurate circuitry to ensure that the reset threshold occurs only within this range (for 5-V and 3.3-V supplies). The other voltage options have the same tight tolerance to ensure a reset signal for other narrow monitor ranges. See [Table 1](#) for examples of how the standard reset thresholds apply to 3-V, 3.3-V, and 5-V nominal supply voltages.

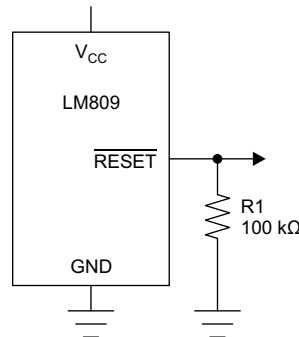
**Table 1. Reset Thresholds Related to Common Supply Voltages**

Reset Threshold	3 V	3.3 V	5 V
4.63 ± 3%			90 – 95%
4.38 ± 3%			85 – 90%
4.00 ± 3%			78 – 82%
3.08 ± 3%		90 – 95%	
2.93 ± 3%		86 – 90%	
2.63 ± 3%	85 – 90%	77 – 81%	
2.45 ± 3%	79 – 84%	72 – 76%	

### 7.3.1.1 Ensuring a Valid Reset Output Down to $V_{CC} = 0\text{ V}$

When  $V_{CC}$  falls below 1 V, the LM809  $\overline{\text{RESET}}$  output no longer sinks current. A high-impedance CMOS logic input connected to  $\overline{\text{RESET}}$  can therefore drift to undetermined voltages. To prevent this situation, a 100-k $\Omega$  resistor should be connected from the  $\overline{\text{RESET}}$  output to ground, as shown in Figure 7.

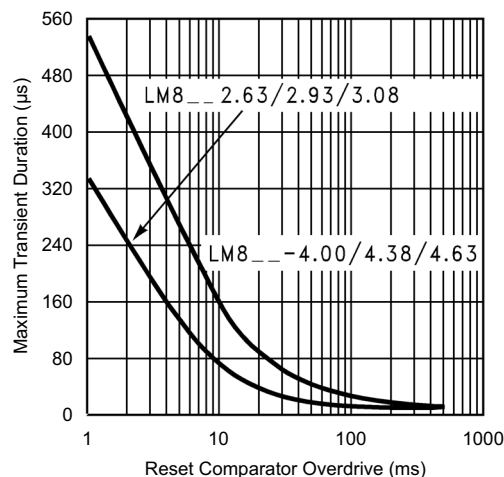
A 100-k $\Omega$  pullup resistor to  $V_{CC}$  is also recommended for the LM810, if  $\overline{\text{RESET}}$  is required to remain valid for  $V_{CC} < 1\text{ V}$ .



**Figure 7.  $\overline{\text{RESET}}$  Valid to  $V_{CC} = \text{Ground}$  Circuit**

### 7.3.1.2 Negative-Going $V_{CC}$ Transients

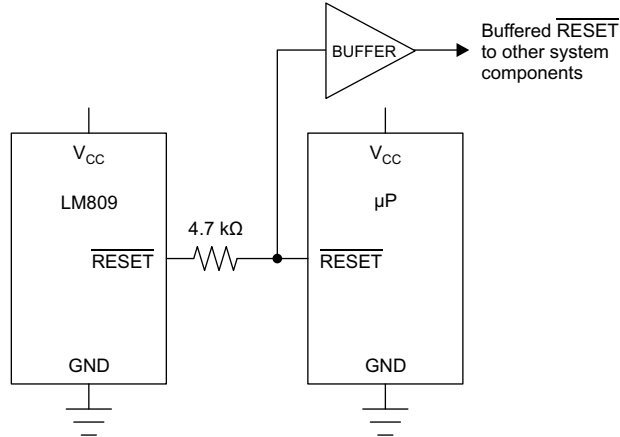
The LM809 and LM810 are relatively immune to short negative-going transients or glitches on  $V_{CC}$ . Figure 8 shows the maximum pulse width a negative-going  $V_{CC}$  transient can have without causing a reset pulse. In general, as the magnitude of the transient increases, going further below the threshold, the maximum allowable pulse width decreases. Typically, for the 4.63-V and 4.38-V version of the LM809 or LM810, a  $V_{CC}$  transient that goes 100 mV below the reset threshold and lasts 20  $\mu\text{s}$  or less will not cause a reset pulse. A 0.1- $\mu\text{F}$  bypass capacitor mounted as close as possible to the  $V_{CC}$  pin will provide additional transient rejection.



**Figure 8. Maximum Transient Duration without Causing a Reset Pulse vs Reset Comparator Overdrive**

### 7.3.1.3 Interfacing to $\mu$ Ps with Bidirectional Reset Pins

Microprocessors with bidirectional reset pins, such as the Motorola 68HC11 series, can be connected to the LM809 RESET output. To ensure a correct output on the LM809 even when the microprocessor reset pin is in the opposite state, connect a 4.7-k $\Omega$  resistor between the LM809 RESET output and the  $\mu$ P reset pin, as shown in Figure 9. Buffer the LM809 RESET output to other system components.



**Figure 9. Interfacing to Microprocessors with Bidirectional Reset I/O**

## 7.4 Device Functional Modes

### 7.4.1 V<sub>CC</sub> Supply Voltage Low

When V<sub>CC</sub> supply voltage declines below the reset threshold, the RESET output is asserted. For LM809, the active-low RESET output is low. For LM810, the active-high RESET output is high.

### 7.4.2 V<sub>CC</sub> Supply Voltage High

When the V<sub>CC</sub> supply voltage rises above the reset threshold, the RESET output resets after 240 ms. For LM809, the active-low RESET output rises high. For LM810, the active-high RESET output drops low.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LM809 and LM810 are a supervisor circuit for microprocessor and digital systems. With a low supply current of only 15  $\mu$ A, the LM809 and LM810 are ideal for use in portable equipment.

### 8.2 Typical Application



**Figure 10. Microprocessor  $\overline{\text{RESET}}$  Circuit**

#### 8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 2](#) as the input parameters.

**Table 2. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input supply voltage range	1 V to 5.5 V
Reset output voltage (high)	Input supply
Reset output voltage (low)	0 V

#### 8.2.2 Detailed Design Procedure

For the typical application circuit, all that is required is the LM809 or LM810 IC, but TI recommends an input capacitor to help with input voltage transients. A typical input capacitor value is 0.1  $\mu$ F and must be rated for the highest expected input voltage.

### 8.2.3 Application Curve

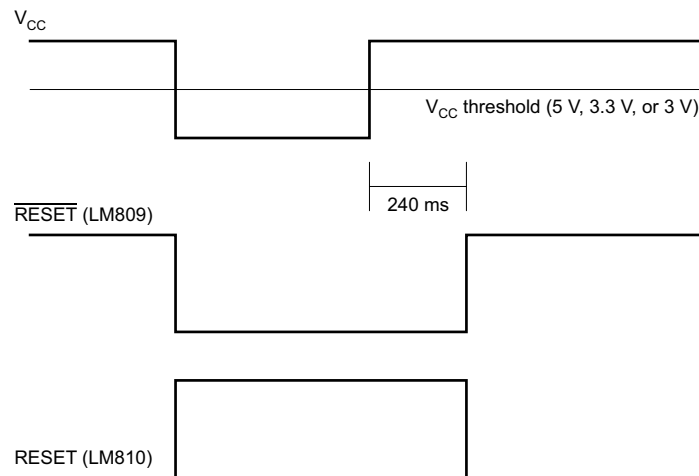


Figure 11. Reset Active Timeout

## 9 Power Supply Recommendations

The input of the LM809 is designed to handle up to the supply voltage absolute maximum rating of 6.5 V. If the input supply is susceptible to any large transients above the maximum rating, then extra precautions should be taken. An input capacitor is recommended to avoid false reset output triggers due to noise.

## 10 Layout

### 10.1 Layout Guidelines

Place the input capacitor as close as possible to the IC.

### 10.2 Layout Example

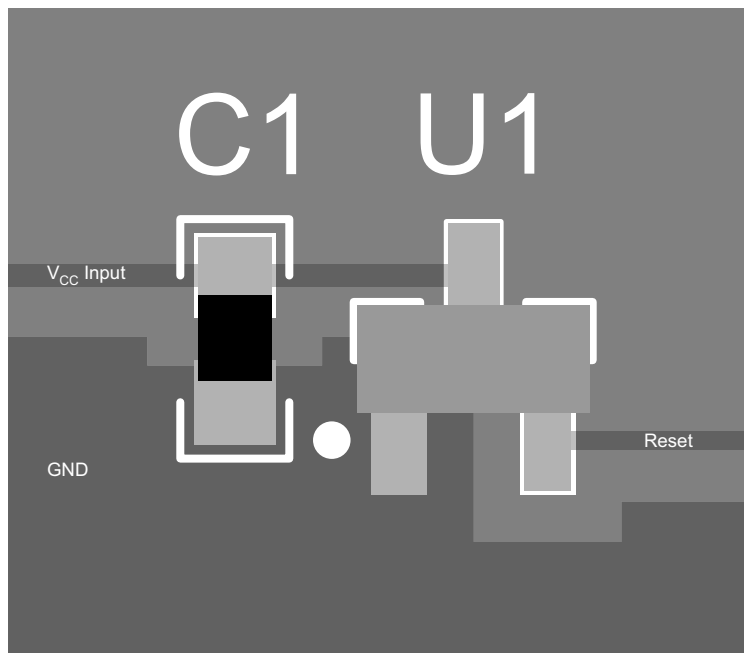


Figure 12. Layout Example

## 11 Device and Documentation Support

### 11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 3. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM809	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM810	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM809M3-2.63/NOPB	ACTIVE	SOT-23	DBZ	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	S3B	<a href="#">Samples</a>
LM809M3-2.93	NRND	SOT-23	DBZ	3	1000	TBD	Call TI	Call TI	-40 to 105	S4B	
LM809M3-2.93/NOPB	ACTIVE	SOT-23	DBZ	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	S4B	<a href="#">Samples</a>
LM809M3-3.08	NRND	SOT-23	DBZ	3	1000	TBD	Call TI	Call TI	-40 to 105	S5B	
LM809M3-3.08/NOPB	ACTIVE	SOT-23	DBZ	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	S5B	<a href="#">Samples</a>
LM809M3-4.38/NOPB	ACTIVE	SOT-23	DBZ	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	S7B	<a href="#">Samples</a>
LM809M3-4.63/NOPB	ACTIVE	SOT-23	DBZ	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	S8B	<a href="#">Samples</a>
LM809M3X-2.63/NOPB	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	S3B	<a href="#">Samples</a>
LM809M3X-2.93/NOPB	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	S4B	<a href="#">Samples</a>
LM809M3X-3.08/NOPB	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	S5B	<a href="#">Samples</a>
LM809M3X-4.38/NOPB	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		S7B	<a href="#">Samples</a>
LM809M3X-4.63/NOPB	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	S8B	<a href="#">Samples</a>
LM810M3-4.63	NRND	SOT-23	DBZ	3	1000	TBD	Call TI	Call TI	-40 to 105	SEB	
LM810M3-4.63/NOPB	ACTIVE	SOT-23	DBZ	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	SEB	<a href="#">Samples</a>
LM810M3X-4.63/NOPB	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	SEB	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

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(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM809M3-2.63/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM809M3-2.93	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM809M3-2.93/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM809M3-3.08	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM809M3-3.08/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM809M3-4.38/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM809M3-4.63/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM809M3X-2.63/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM809M3X-2.93/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM809M3X-3.08/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM809M3X-4.38/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM809M3X-4.63/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM810M3-4.63	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM810M3-4.63/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM810M3X-4.63/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

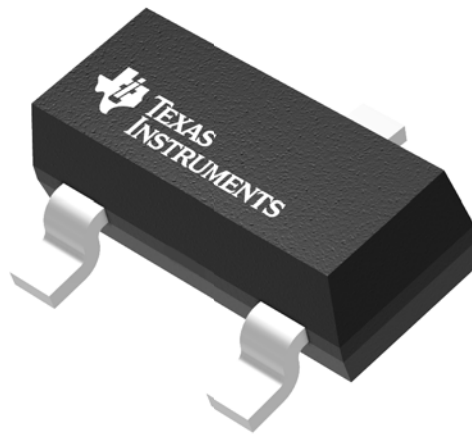
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM809M3-2.63/NOPB	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM809M3-2.93	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM809M3-2.93/NOPB	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM809M3-3.08	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM809M3-3.08/NOPB	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM809M3-4.38/NOPB	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM809M3-4.63/NOPB	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM809M3X-2.63/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM809M3X-2.93/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM809M3X-3.08/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM809M3X-4.38/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM809M3X-4.63/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM810M3-4.63	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM810M3-4.63/NOPB	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LM810M3X-4.63/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

**DBZ 3**

**SOT-23 - 1.12 mm max height**

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203227/C

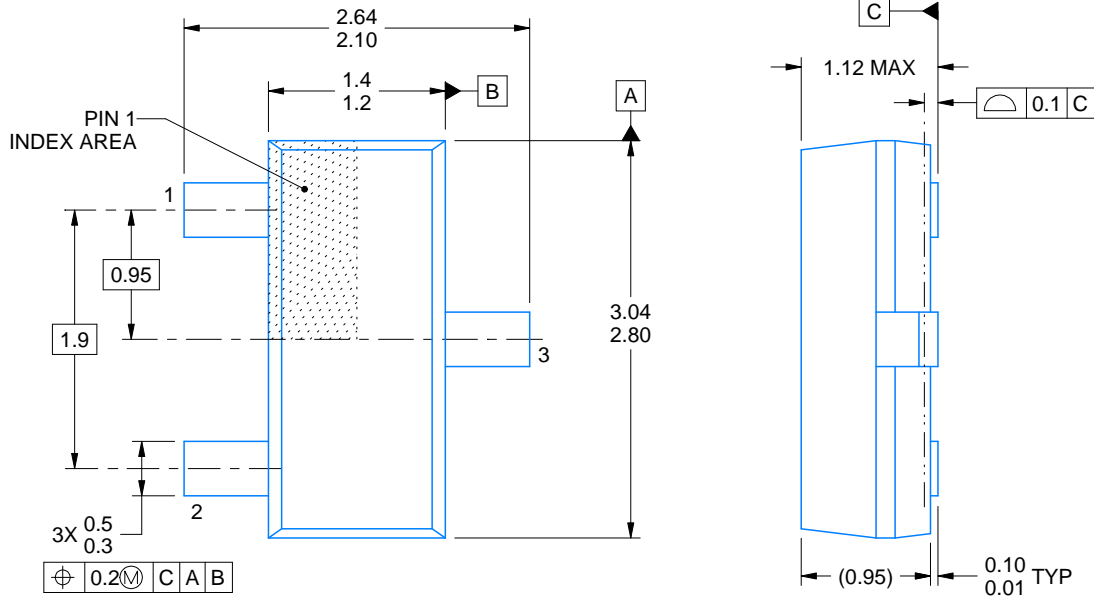
DBZ0003A



# PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

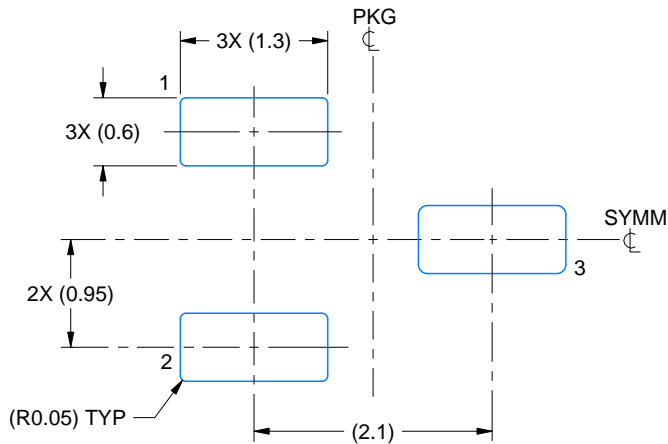
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.

# EXAMPLE BOARD LAYOUT

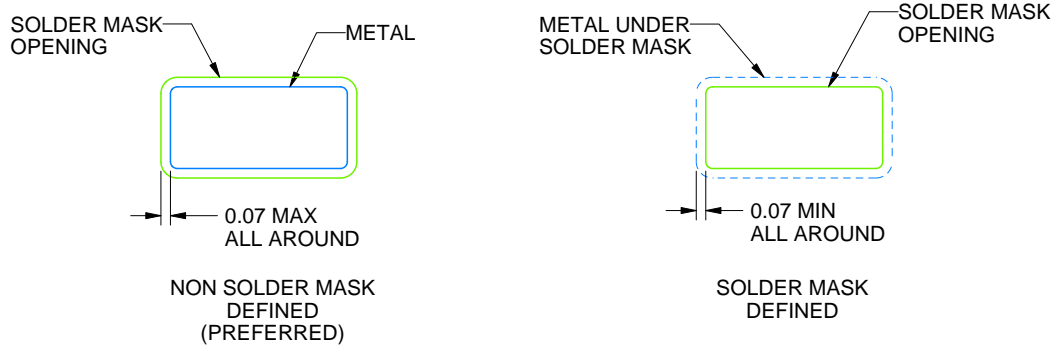
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

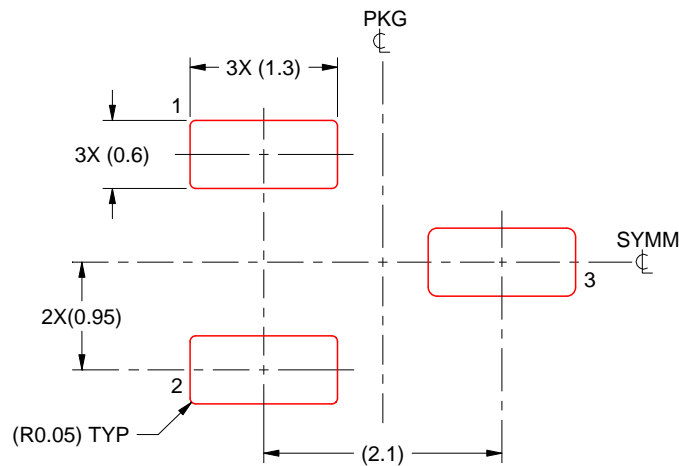
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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