THE DATASHEET OF

LM7321MFX

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TEXAS INSTRUMENTS

LM7321, LM7322

SNOSAW8E – MAY 2008 – REVISED SEPTEMBER 2015

LM7321x Single and LM7322x Dual Rail-to-Rail Input and Output ±15-V, High-Output Current and Unlimited Capacitive Load Operational Amplifier

1 Features

- (V_S = ±15, T_A = 25°C, Typical Values Unless Specified.)
- Wide Supply Voltage Range 2.5 V to 32 V
- Output Current +65 mA/−100 mA
- Gain Bandwidth Product 20 MHz
- Slew Rate 18 V/µs
- Capacitive Load Tolerance Unlimited
- Input Common-Mode Voltage 0.3-V Beyond Rails
- Input Voltage Noise 15 nV/√Hz
- Input Current Noise 1.3 pA/√Hz
- Supply Current/Channel 1.1 mA
- Distortion THD+Noise −86 dB
- Temperature Range −40°C to 125°C
- Tested at −40°C, 25°C and 125°C at 2.7 V, ±5 V, ±15 V.
- LM732xx are Automotive Grade Products that are AEC-Q100 Grade 1 Qualified.

2 Applications

- Driving MOSFETs and Power Transistors
- Capacitive Proximity Sensors
- Driving Analog Optocouplers
- High-Side Sensing
- Below Ground Current Sensing
- Photodiode Biasing
- Driving Varactor Diodes in PLLs
- Wide Voltage Range Power supplies
- Automotive
- International Power Supplies

3 Description

The LM732xx devices are rail-to-rail input and output amplifiers with wide operating voltages and high-output currents. The LM732xx family is efficient, achieving 18-V/µs slew rate and 20-MHz unity gain bandwidth while requiring only 1 mA of supply current per op amp. The LM732xx device performance is fully specified for operation at 2.7 V, ±5 V and ±15 V.

The LM732xx devices are designed to drive unlimited capacitive loads without oscillations. All LM7321x and LM7322x parts are tested at −40°C, 125°C, and 25°C, with modern automatic test equipment. High performance from −40°C to 125°C, detailed specifications, and extensive testing makes them suitable for industrial, automotive, and communications applications.

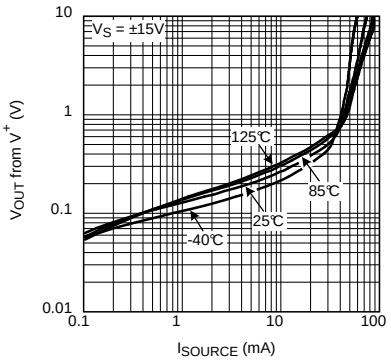
Greater than rail-to-rail input common-mode voltage range with 50 dB of common-mode rejection across this wide voltage range, allows both high-side and low-side sensing. Most device parameters are insensitive to power supply voltage, and this makes the parts easier to use where supply voltage may vary, such as automotive electrical systems and battery powered equipment. These amplifiers have true rail-to-rail output and can supply a respectable amount of current (15 mA) with minimal head- room from either rail (300 mV) at low distortion (0.05% THD+Noise).

Device Information(1)

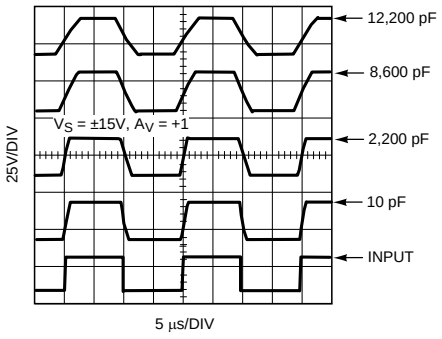
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM7321 LM7322	SOIC (8)	4.90 mm × 3.91 mm
	SOT (5)	2.90 mm × 1.60 mm
LM7322	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Output Swing vs. Sourcing Current



Large Signal Step Response



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (May 2008) to Revision D — **Page**

- Changed layout of National Data Sheet to TI format ... 25

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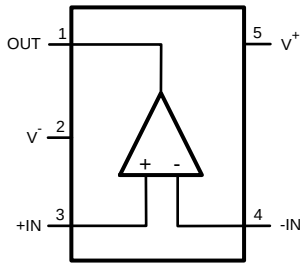
5 Description continued

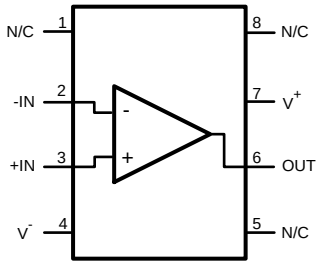
There are several package options for each part. Standard SOIC versions of both parts make upgrading existing designs easy. LM7322x are offered in a space-saving 8-Pin VSSOP package. The LM7321x are offered in small SOT-23 package, which makes it easy to place this part close to sensors for better circuit performance.

6 Pin Configuration and Functions

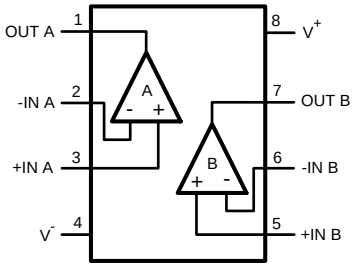
DBV Package
5-Pin SOT-23
Top View



D Package
8-Pin SOIC
Top View



DGK Package
8-Pin VSSOP or SOIC
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	SOT-23 NO.	SOIC NO.	VSSOP, SOIC NO.		
OUT	1	6	—	O	Output
OUT A	—	—	1	O	Output for Amplifier A
OUT B	—	—	7	O	Output for Amplifier B
V+	5	7	7	P	Positive Supply
V–	2	4	4	P	Negative Supply
+IN	3	3	—	I	Noninverting Input
–IN	4	2	—	I	Inverting Input
+IN A	—	—	3	I	Noninverting Input for Amplifier A
–IN A	—	—	2	I	Inverting Input for Amplifier A
+IN B	—	—	5	I	Noninverting Input for Amplifier B
–IN B	—	—	6	I	Inverting Input for Amplifier B
N/C	—	1, 5, 8	—	—	No connection

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{IN} Differential			±10	V
Output Short Circuit Current			See (3)	
Supply Voltage ($V_S = V^+ - V^-$)			35	V
Voltage at Input/Output pins		V^+ + 0.8	V^- − 0.8	V
Junction Temperature(4)			150	°C
Soldering Information:	Infrared or Convection (20 sec.)		235	°C
	Wave Soldering (10 sec.)		260	°C
Storage Temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S \leq 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5 ms.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}) – T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	
		Machine Model	200	

(1) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltage ($V_S = V^+ - V^-$)	2.5	32	V
Temperature Range(1)	−40	125	°C

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}) – T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.4 Thermal Information

THERMAL METRIC(1)		LM7321			UNIT
		D (SOIC)	DBV (SOT)	DGK (VSSOP)	
		8 PINS	5 PINS	8 PINS	
$R_{\theta JA}$(2)	Junction-to-ambient thermal resistance	165	325	235	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}) – T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

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7.5 2.7-V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 0.5 V, V_{OUT} = 1.35 V, and R_L > 1 MΩ to 1.35 V.(1)

PARAMETER		TEST CONDITION		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 0.5 V and V_{CM} = 2.2 V		−5	±0.7	+5	mV
			T_A = –40°C to +125°C	−6		+6	
TC V_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = 0.5 V and V_{CM} = 2.2 V(4)			±2		µV/C
I_B	Input Bias Current	V_{CM} = 0.5 V(5)		−2	−1.2		µA
			T_A = –40°C to +125°C	−2.5			
		V_{CM} = 2.2 V(5)			0.45	1	
			T_A = –40°C to +125°C			1.5	
I_{OS}	Input Offset Current	V_{CM} = 0.5 V and V_{CM} = 2.2 V			20	200	nA
			T_A = –40°C to +125°C			300	
CMRR	Common-Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 1 V		70	100		dB
			T_A = –40°C to +125°C	60			
		0 V ≤ V_{CM} ≤ 2.7 V		55	70		
			T_A = –40°C to +125°C	50			
PSRR	Power Supply Rejection Ratio	2.7 V ≤ V_S ≤ 30 V		78	104		dB
			T_A = –40°C to +125°C	74			
CMVR	Common-Mode Voltage Range (Min)	CMRR > 50 dB			−0.3	−0.1	V
			T_A = –40°C to +125°C			0	
	Common-Mode Voltage Range (Max)	CMRR > 50 dB		2.8	3		
			T_A = –40°C to +125°C	2.7			
A_{VOL}	Open-Loop Voltage Gain	0.5 V ≤ V_O ≤ 2.2 V R_L = 10 kΩ to 1.35 V		65	72		dB
			T_A = –40°C to +125°C	62			
		0.5 V ≤ V_O ≤ 2.2 V R_L = 2 kΩ to 1.35V		59	66		
			T_A = –40°C to +125°C	55			
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to 1.35 V V_{ID} = 100 mV			50	150	mV from either rail
			T_A = –40°C to +125°C			160	
		R_L = 2 kΩ to 1.35 V V_{ID} = 100 mV			100	250	
			T_A = –40°C to +125°C			280	
	Output Voltage Swing Low	R_L = 10 kΩ to 1.35 V V_{ID} = −100 mV			20	120	
			T_A = –40°C to +125°C			150	
		R_L = 2 kΩ to 1.35 V V_{ID} = −100 mV			40	120	
			T_A = –40°C to +125°C			150	
I_{OUT}	Output Current	Sourcing V_{ID} = 200 mV, V_{OUT} = 0 V(6)		30	48		mA
			T_A = –40°C to +125°C	20			
		Sinking V_{ID} = −200 mV, V_{OUT} = 2.7 V(6)		40	65		
			T_A = –40°C to +125°C	30			

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Short circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ 6 V at room temperature and below. For V_S > 6 V, allowable short circuit duration is 1.5 ms.

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2.7-V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 0.5 V, V_{OUT} = 1.35 V, and R_L > 1 MΩ to 1.35 V.(1)

PARAMETER		TEST CONDITION		MIN(2)	TYP(3)	MAX(2)	UNIT
I_S	Supply Current	LM7321			0.95	1.3	mA
			T_A = –40°C to +125°C			1.9	
		LM7322			2	2.5	
			T_A = –40°C to +125°C			3.8	
SR	Slew Rate(7)	A_V = +1, V_I = 2-V Step			8.5		V/µs
f_u	Unity Gain Frequency	R_L = 2 kΩ, C_L = 20 pF			7.5		MHz
GBW	Gain Bandwidth	f = 50 kHz			16		MHz
e_n	Input Referred Voltage Noise Density	f = 2 kHz			11.9		nV/√Hz
i_n	Input Referred Current Noise Density	f = 2 kHz			0.5		pA/√Hz
THD+N	Total Harmonic Distortion + Noise	V^+ = 1.9 V, V^- = −0.8 V f = 1 kHz, R_L = 100 kΩ, A_V = +2 V_{OUT} = 210 mV_{PP}			−77		dB
CT Rej.	Crosstalk Rejection	f = 100 kHz, Driver R_L = 10 kΩ			60		dB

(7) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

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7.6 ±5-V Electrical Characteristics

Unless otherwise specified, all limited ensured for T_A = 25°C, V^+ = 5 V, V^- = −5V, V_{CM} = 0 V, V_{OUT} = 0 V, and R_L > 1 MΩ to 0 V.(1)

PARAMETER		TEST CONDITION		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = −4.5 V and V_{CM} = 4.5 V		−5	±0.7	+5	mV
			T_A = –40°C to +125°C	−6		+6	
TC V_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = −4.5 V and V_{CM} = 4.5 V(4)			±2		µV/°C
I_B	Input Bias Current	V_{CM} = −4.5 V(5)		−2.0	−1.2		µA
			T_A = –40°C to +125°C	−2.5			
		V_{CM} = 4.5 V(5)			0.45	1	
			T_A = –40°C to +125°C			1.5	
I_{OS}	Input Offset Current	V_{CM} = −4.5 V and V_{CM} = 4.5 V			20	200	nA
			T_A = –40°C to +125°C			300	
CMRR	Common Mode Rejection Ratio	−5 V ≤ V_{CM} ≤ 3 V		80	100		dB
			T_A = –40°C to +125°C	70			
		−5 V ≤ V_{CM} ≤ 5 V		65	80		
			T_A = –40°C to +125°C	62			
PSRR	Power Supply Rejection Ratio	2.7 V ≤ V_S ≤ 30 V, V_{CM} = −4.5 V		78	104		dB
			T_A = –40°C to +125°C	74			
CMVR	Common-Mode Voltage Range (Min)	CMRR > 50 dB			−5.3	−5.1	V
			T_A = –40°C to +125°C			−5	
	Common-Mode Voltage Range (Max)	CMRR > 50 dB		5.1	5.3		
			T_A = –40°C to +125°C	5			
A_{VOL}	Open-Loop Voltage Gain	−4 V ≤ V_O ≤ 4 V, R_L = 10 kΩ to 0 V		74	80		dB
			T_A = –40°C to +125°C	70			
		−4 V ≤ V_O ≤ 4 V, R_L = 2 kΩ to 0 V		68	74		
			T_A = –40°C to +125°C	65			
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to 0 V, V_{ID} = 100 mV			100	250	mV from either rail
			T_A = –40°C to +125°C			280	
		R_L = 2 kΩ to 0 V, V_{ID} = 100 mV			160	350	
			T_A = –40°C to +125°C			450	
	Output Voltage Swing Low	R_L = 10 kΩ to 0 V, V_{ID} = −100 mV			35	200	
			T_A = –40°C to +125°C			250	
		R_L = 2 kΩ to 0 V, V_{ID} = −100 mV			80	200	
			T_A = –40°C to +125°C			250	
I_{OUT}	Output Current	Sourcing V_{ID} = 200 mV, V_{OUT} = −5 V(6)		35	70		mA
			T_A = –40°C to +125°C	20			
		Sinking V_{ID} = −200 mV, V_{OUT} = 5 V(6)		50	85		
			T_A = –40°C to +125°C	30			

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Short circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ 6 V at room temperature and below. For V_S > 6 V, allowable short circuit duration is 1.5 ms.

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±5-V Electrical Characteristics (continued)

Unless otherwise specified, all limited ensured for T_A = 25°C, V^+ = 5 V, V^- = −5V, V_{CM} = 0 V, V_{OUT} = 0 V, and R_L > 1 MΩ to 0 V.(1)

PARAMETER		TEST CONDITION			MIN(2)	TYP(3)	MAX(2)	UNIT
I_S	Supply Current	V_{CM} = −4.5 V	LM7321			1.0	1.3	mA
				T_A = –40°C to +125°C			2	
			LM7322			2.3	2.8	
				T_A = –40°C to +125°C			3.8	
SR	Slew Rate(7)	A_V = +1, V_I = 8-V Step				12.3		V/µs
f_u	Unity Gain Frequency	R_L = 2 kΩ, C_L = 20 pF				9		MHz
GBW	Gain Bandwidth	f = 50 kHz				16		MHz
e_n	Input Referred Voltage Noise Density	f = 2 kHz				14.3		nV/√Hz
i_n	Input Referred Current Noise Density	f = 2 kHz				1.35		pA/√Hz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, R_L = 100 kΩ, A_V = +2 V_{OUT} = 8 V_{PP}				−79		dB
CT Rej.	Crosstalk Rejection	f = 100 kHz, Driver R_L = 10 kΩ				60		dB

(7) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

7.7 ±15-V Electrical Characteristics

Unless otherwise specified, all limited ensured for T_A = 25°C, V^+ = 15 V, V^- = −15 V, V_{CM} = 0 V, V_{OUT} = 0 V, and R_L > 1 MΩ to 15 V.(1)

PARAMETER		TEST CONDITION		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = −14.5 V and V_{CM} = 14.5 V		−6	±0.7	+6	mV
			–40°C to +125°C	−8		+8	
TC V_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = −14.5 V and V_{CM} = 14.5 V(4)			±2		µV/°C
I_B	Input Bias Current	V_{CM} = −14.5 V(5)		−2	−1.1		µA
			–40°C to +125°C	−2.5			
		V_{CM} = 14.5 V(5)			0.45	1	
			–40°C to +125°C			1.5	
I_{OS}	Input Offset Current	V_{CM} = −14.5 V and V_{CM} = 14.5 V			30	300	nA
			–40°C to +125°C			500	
CMRR	Common-Mode Rejection Ratio	−15 V ≤ V_{CM} ≤ 12 V		80	100		dB
			–40°C to +125°C	75			
		−15 V ≤ V_{CM} ≤ 15 V		72	80		
			–40°C to +125°C	70			
PSRR	Power Supply Rejection Ratio	2.7 V ≤ V_S ≤ 30 V, V_{CM} = −14.5 V		78	100		dB
			–40°C to +125°C	74			

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.

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±15-V Electrical Characteristics (continued)

Unless otherwise specified, all limited ensured for T_A = 25°C, V^+ = 15 V, V^- = −15 V, V_{CM} = 0 V, V_{OUT} = 0 V, and R_L > 1 MΩ to 15 V.(1)

PARAMETER		TEST CONDITION			MIN(2)	TYP(3)	MAX(2)	UNIT
CMVR	Common-Mode Voltage Range (Min)	CMRR > 50 dB				−15.3	−15.1	V
			–40°C to +125°C				−15	
	Common-Mode Voltage Range (Max)	CMRR > 50 dB			15.1	15.3		
			–40°C to +125°C		15			
A_{VOL}	Open-Loop Voltage Gain	−13 V ≤ V_O ≤ 13 V, R_L = 10 kΩ to 0 V			75	85		dB
			–40°C to +125°C		70			
		−13 V ≤ V_O ≤ 13 V, R_L = 2 kΩ to 0 V			70	78		
			–40°C to +125°C		65			
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to 0 V, V_{ID} = 100 mV				150	300	mV from either rail
			–40°C to +125°C				350	
		R_L = 2 kΩ to 0 V, V_{ID} = 100 mV				250	550	
			–40°C to +125°C				650	
	Output Voltage Swing Low	R_L = 10 kΩ to 0 V, V_{ID} = −100 mV				60	200	
			–40°C to +125°C				250	
		R_L = 2 kΩ to 0 V, V_{ID} = −100 mV				130	300	
			–40°C to +125°C				400	
I_{OUT}	Output Current	Sourcing, V_{ID} = 200 mV, V_{OUT} = −15 V(6)			40	65		mA
		Sinking, V_{ID} = −200 mV, V_{OUT} = 15 V(6)			60	100		
I_S	Supply Current	V_{CM} = −14.5 V	LM7321			1.1	1.7	mA
				–40°C to +125°C			2.4	
			LM7322			2.5	4	
				–40°C to +125°C			5.6	
SR	Slew Rate(7)	A_V = +1, V_I = 20-V Step				18		V/µs
f_u	Unity Gain Frequency	R_L = 2 kΩ, C_L = 20 pF				11.3		MHz
GBW	Gain Bandwidth	f = 50 kHz				20		MHz
e_n	Input Referred Voltage Noise Density	f = 2 kHz				15		nV/√H
i_n	Input Referred Current Noise Density	f = 2 kHz				1.3		pA/√H
THD+N	Total Harmonic Distortion +Noise	f = 1 kHz, R_L 100 kΩ, A_V = +2, V_{OUT} = 23 V_{PP}				−86		dB
CT Rej.	Crosstalk Rejection	f = 100 kHz, Driver R_L = 10 kΩ				60		dB

(6) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Short circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ 6 V at room temperature and below. For V_S > 6 V, allowable short circuit duration is 1.5 ms.
(7) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

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7.8 Typical Characteristics

Unless otherwise specified: T_A = 25°C.

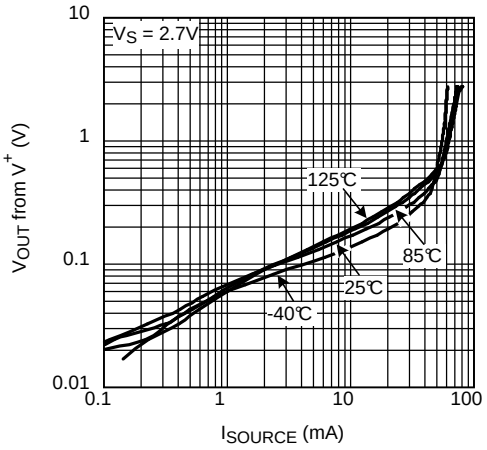

Figure 1. Output Swing vs. Sourcing Current

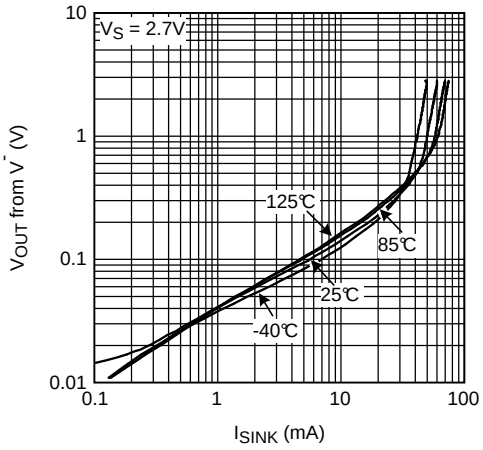

Figure 2. Output Swing vs. Sinking Current

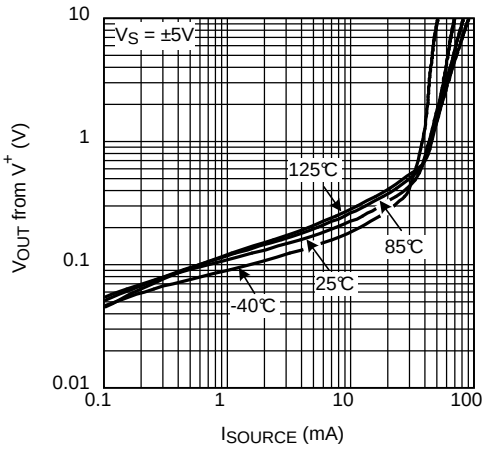

Figure 3. Output Swing vs. Sourcing Current

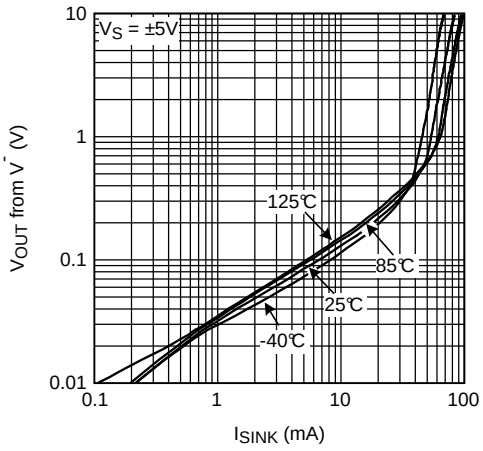

Figure 4. Output Swing vs. Sinking Current

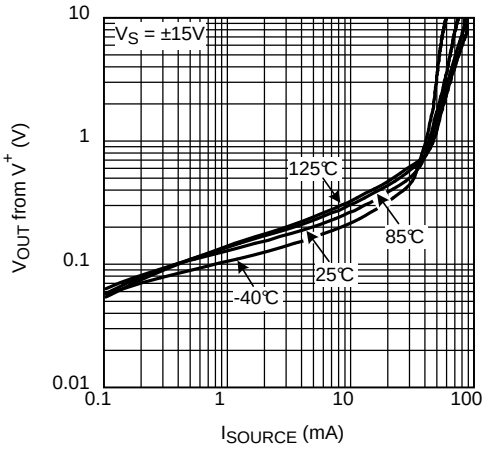

Figure 5. Output Swing vs. Sourcing Current

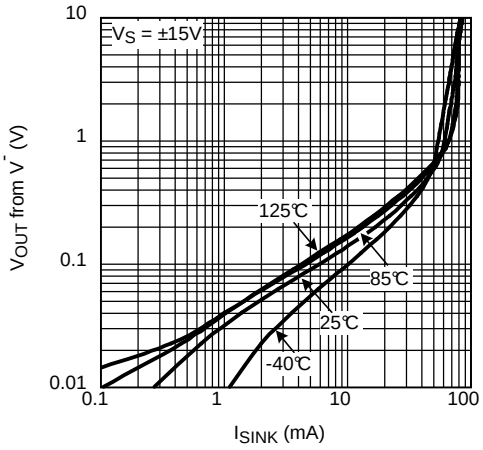

Figure 6. Output Swing vs. Sinking Current

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Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

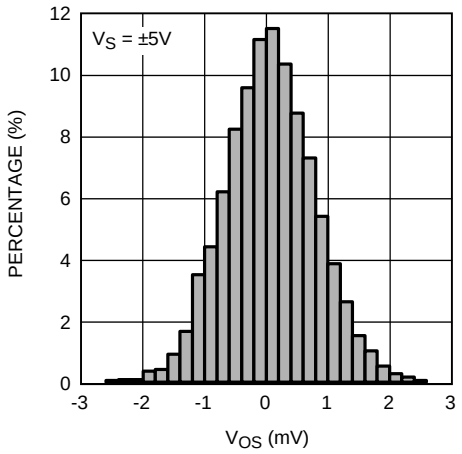

Figure 7. V_{OS} Distribution

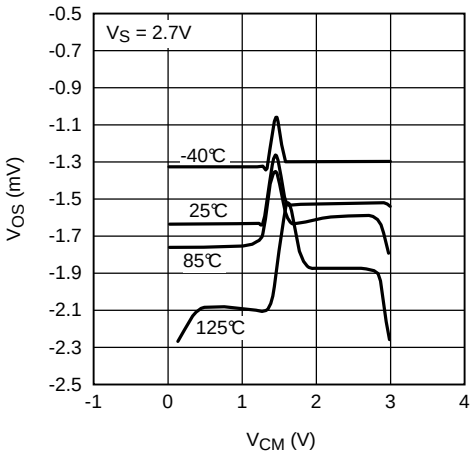

Figure 8. V_{OS} vs. V_{CM} (Unit 1)

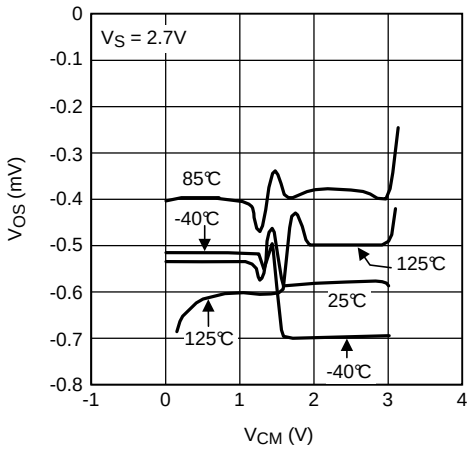

Figure 9. V_{OS} vs. V_{CM} (Unit 2)

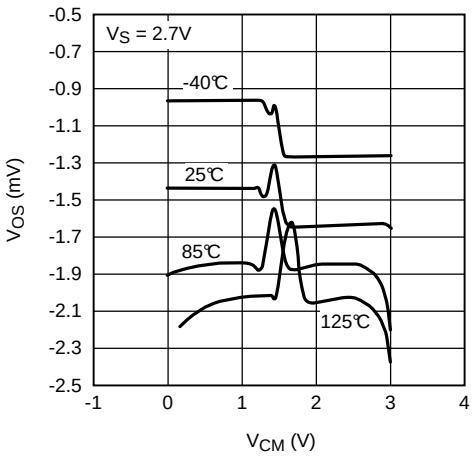

Figure 10. V_{OS} vs. V_{CM} (Unit 3)

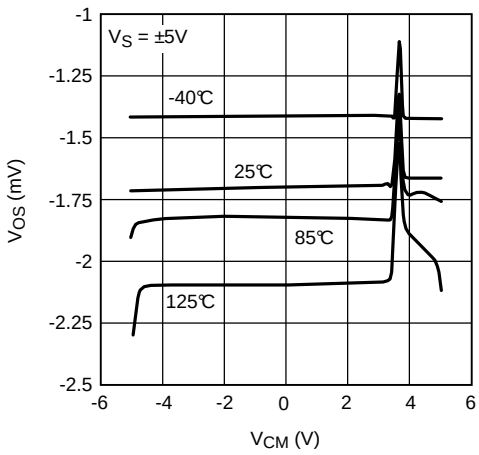

Figure 11. V_{OS} vs. V_{CM} (Unit 1)

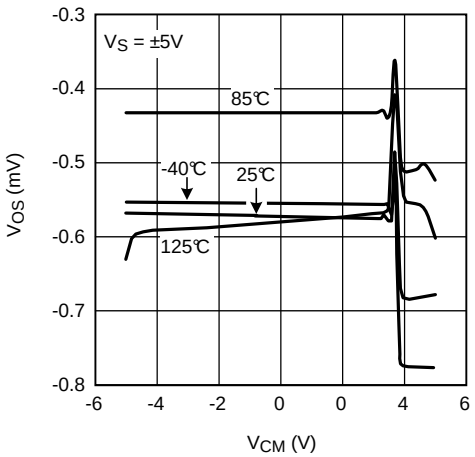

Figure 12. V_{OS} vs. V_{CM} (Unit 2)

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Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

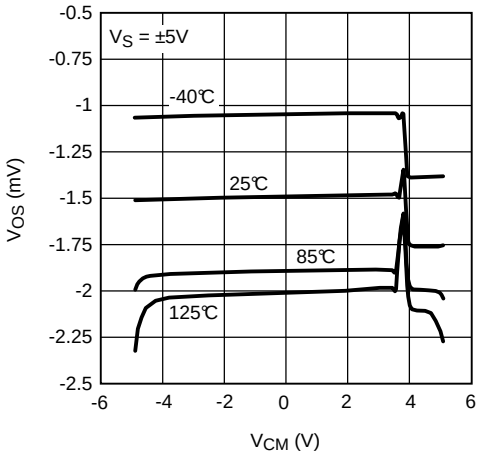

Figure 13. V_{OS} vs. V_{CM} (Unit 2)

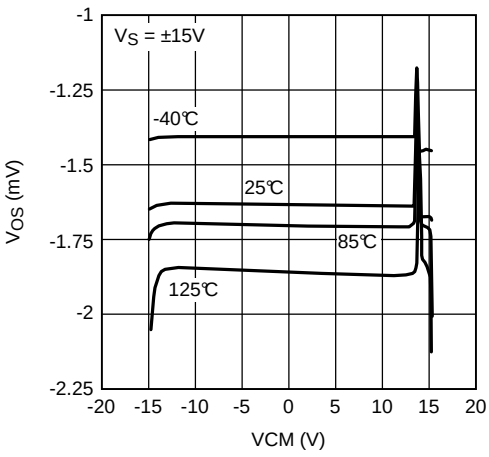

Figure 14. V_{OS} vs. V_{CM} (Unit 1)

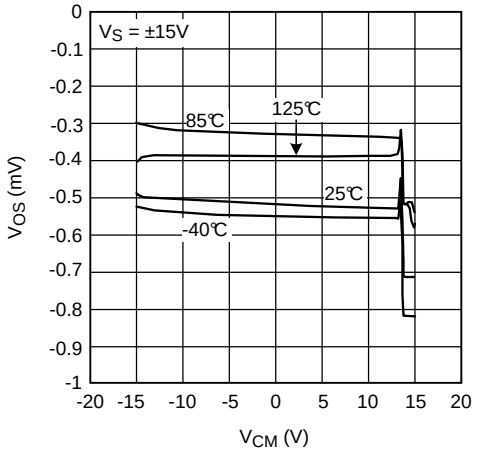

Figure 15. V_{OS} vs. V_{CM} (Unit 2)

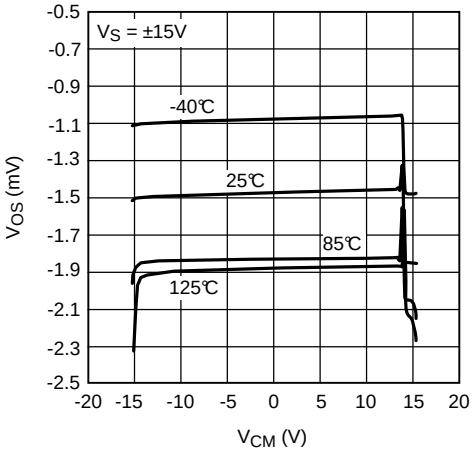

Figure 16. V_{OS} vs. V_{CM} (Unit 3)

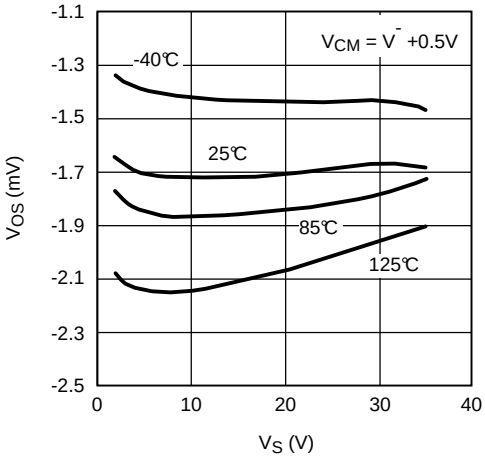

Figure 17. V_{OS} vs. V_S (Unit 1)

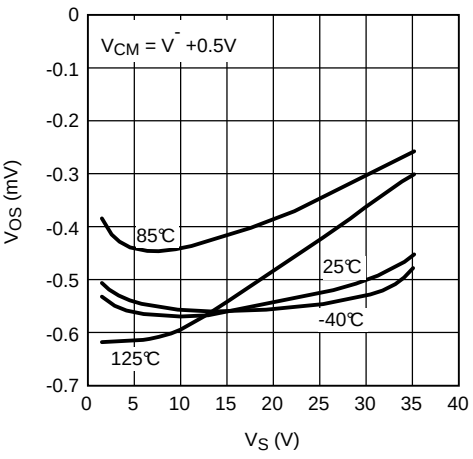

Figure 18. V_{OS} vs. V_S (Unit 2)

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Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

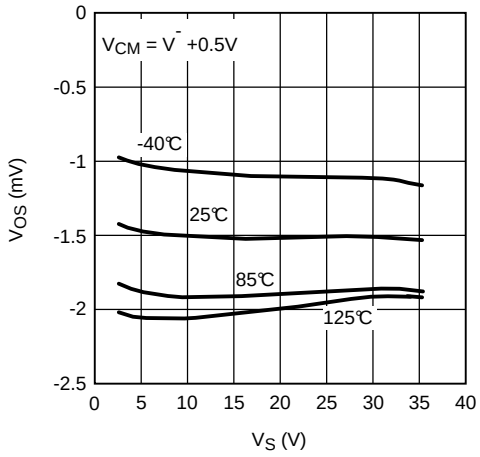

Figure 19. V_{OS} vs. V_S (Unit 3)

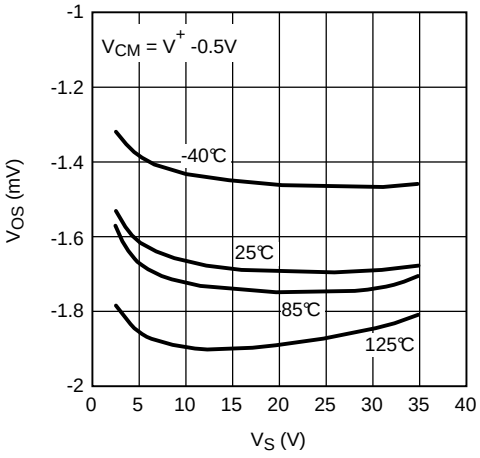

Figure 20. V_{OS} vs. V_S (Unit 1)

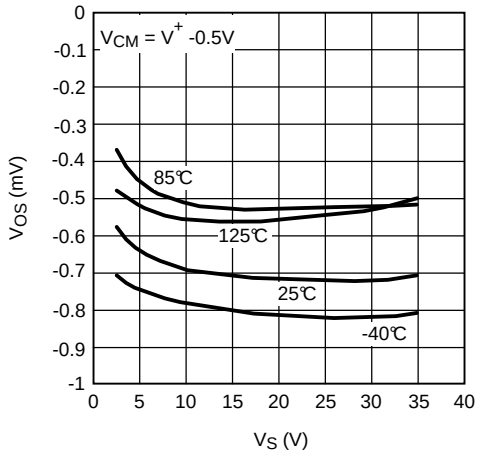

Figure 21. V_{OS} vs. V_S (Unit 2)

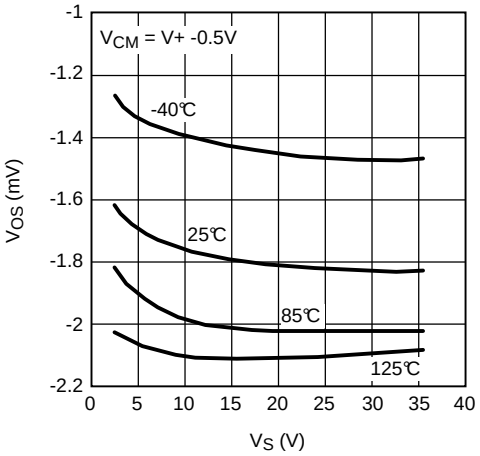

Figure 22. V_{OS} vs. V_S (Unit 3)

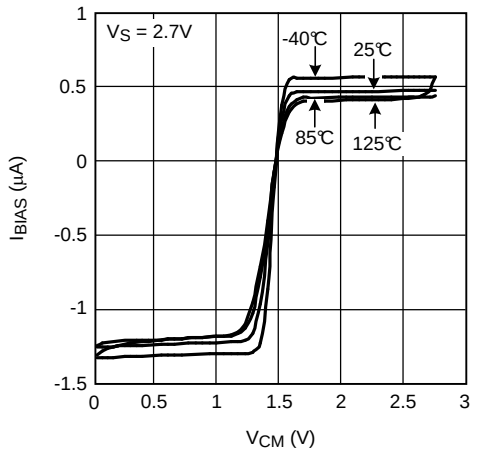

Figure 23. I_{BIAS} vs. V_{CM}

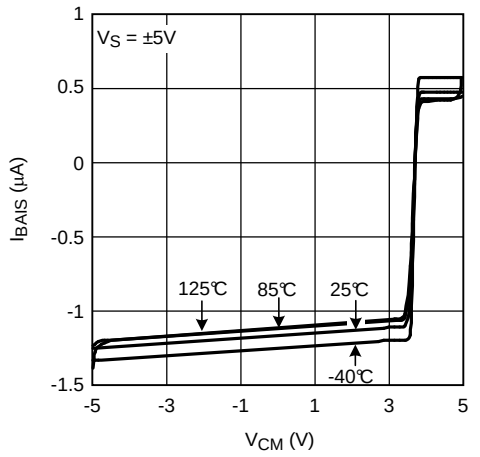

Figure 24. I_{BIAS} vs. V_{CM}

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Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

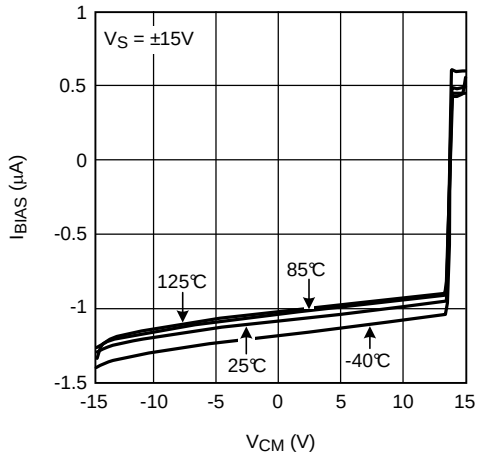

Figure 25. I_{BIAS} vs. V_{CM}

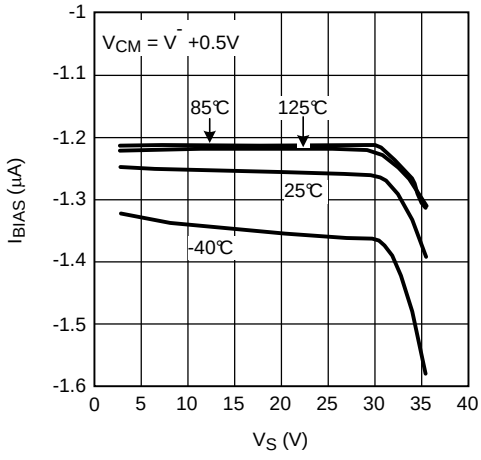

Figure 26. I_{BIAS} vs. V_S

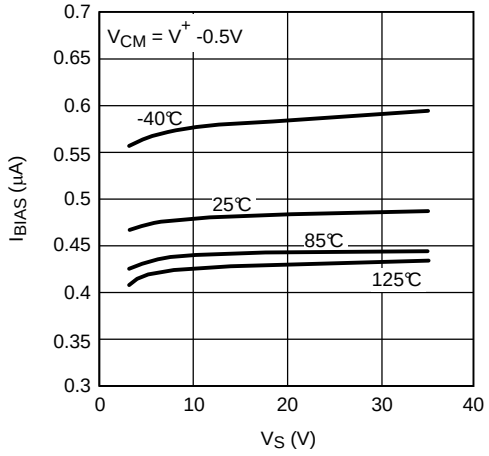

Figure 27. I_{BIAS} vs. V_S

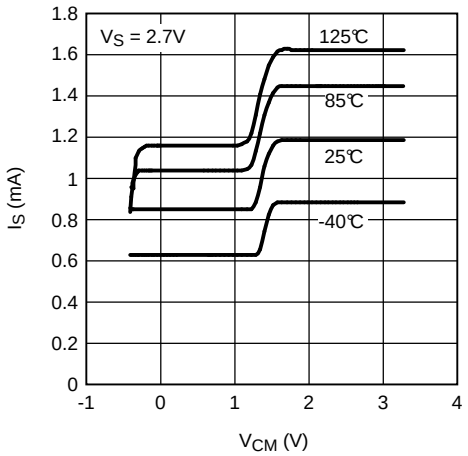

Figure 28. I_S vs. V_{CM} (LM7321)

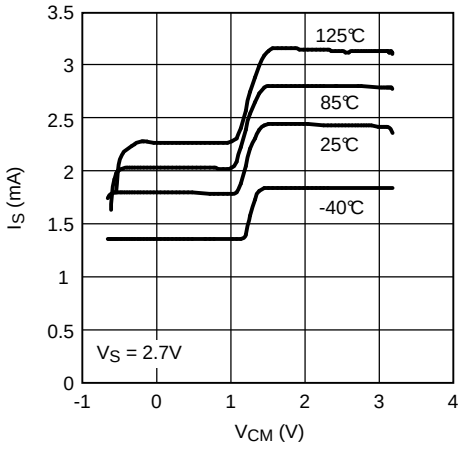

Figure 29. I_S vs. V_{CM} (LM7322)

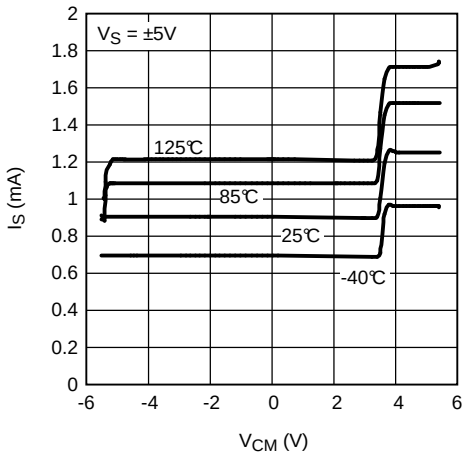

Figure 30. I_S vs. V_{CM} (LM7321)

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Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

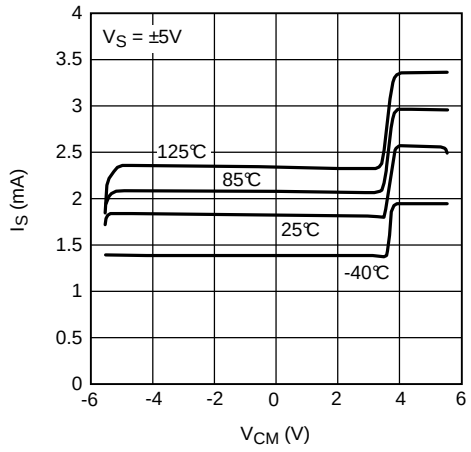

Figure 31. I_S vs. V_{CM} (LM7322)

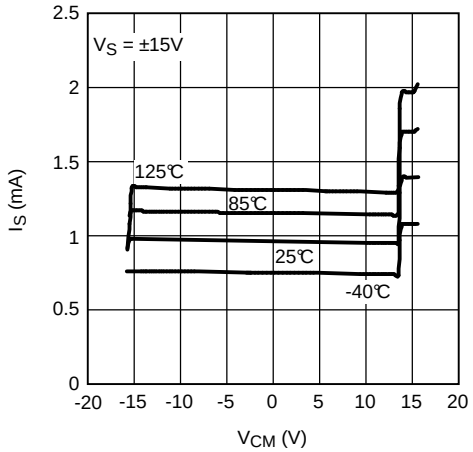

Figure 32. I_S vs. V_{CM} (LM7321)

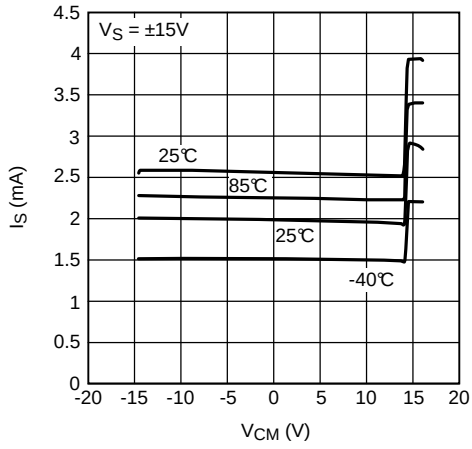

Figure 33. I_S vs. V_{CM} (LM7322)

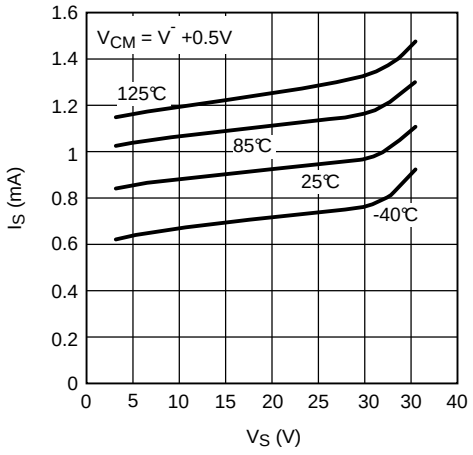

Figure 34. I_S vs. V_S (LM7321)

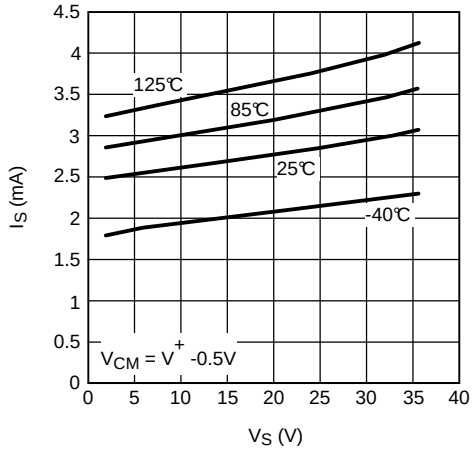

Figure 35. I_S vs. V_S (LM7322)

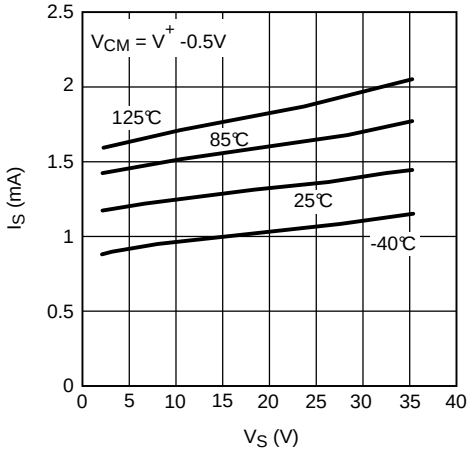

Figure 36. I_S vs. V_S (LM7321)

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

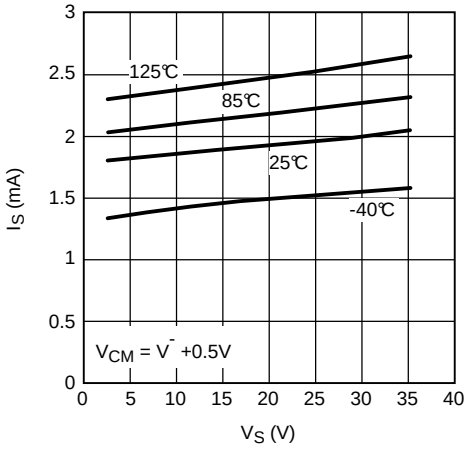

Figure 37. I_S vs. V_S (LM7322)

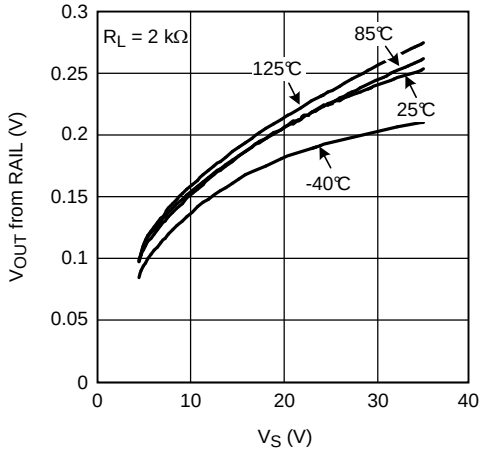

Figure 38. Positive Output Swing vs. Supply Voltage

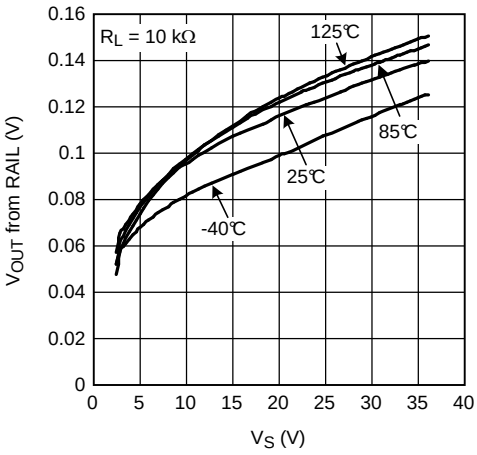

Figure 39. Positive Output Swing vs. Supply Voltage

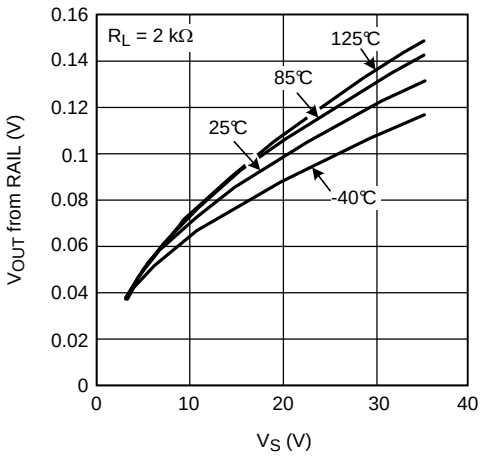

Figure 40. Negative Output Swing vs. Supply Voltage

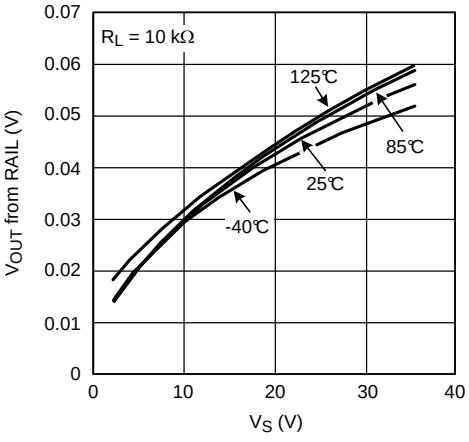

Figure 41. Negative Output Swing vs. Supply Voltage

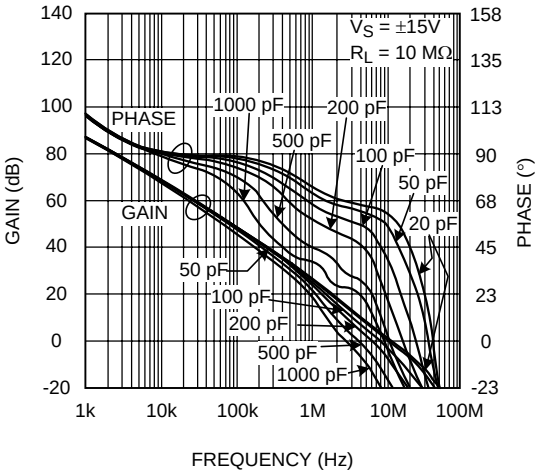

Figure 42. Open-Loop Frequency Response with Various Capacitive Load

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Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

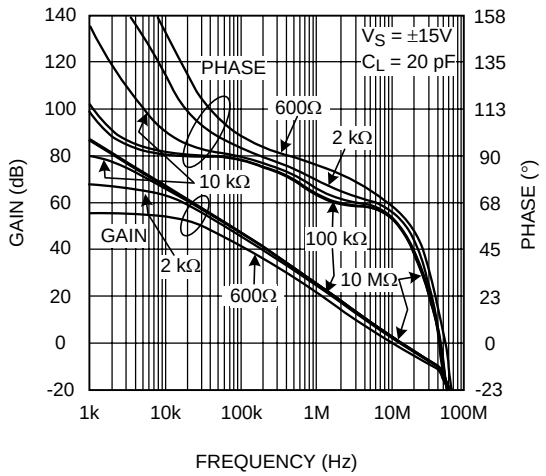

Figure 43. Open-Loop Frequency Response with Various Resistive Load

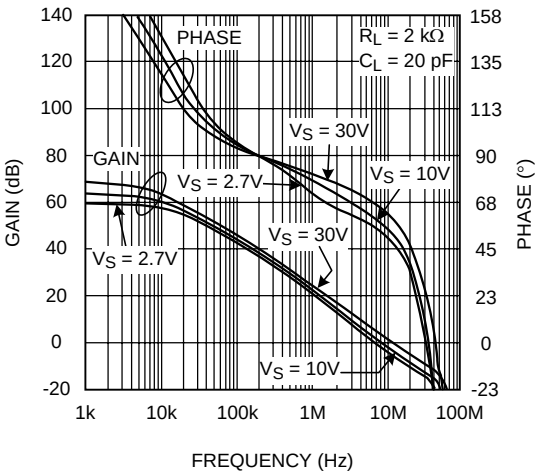

Figure 44. Open-Loop Frequency Response with Various Supply Voltage

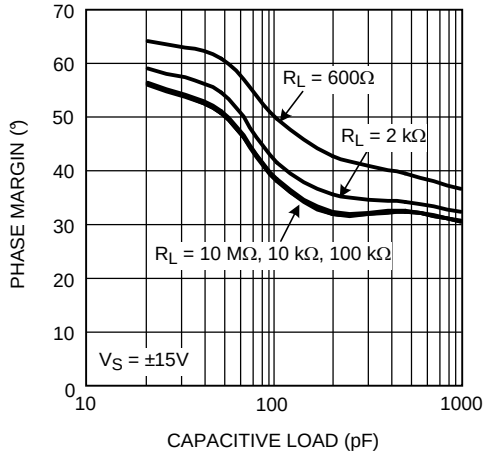

Figure 45. Phase Margin vs. Capacitive Load

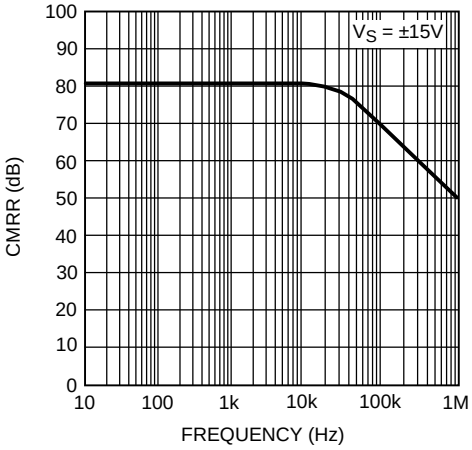

Figure 46. CMRR vs. Frequency

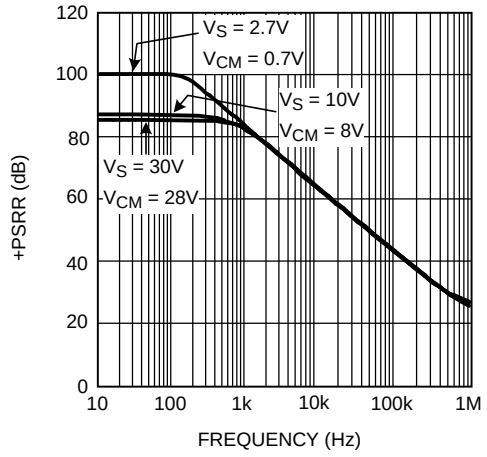

Figure 47. +PSRR vs. Frequency

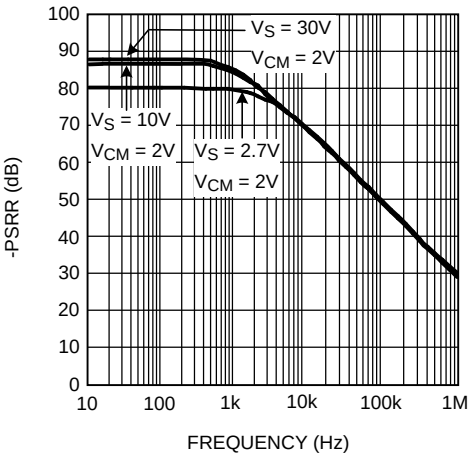

Figure 48. −PSRR vs. Frequency

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Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

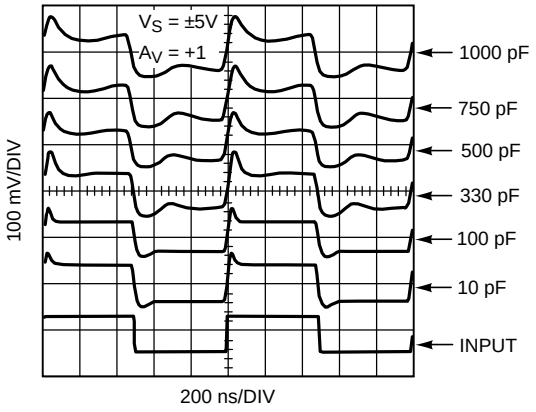

Figure 49. Small Signal Step Response

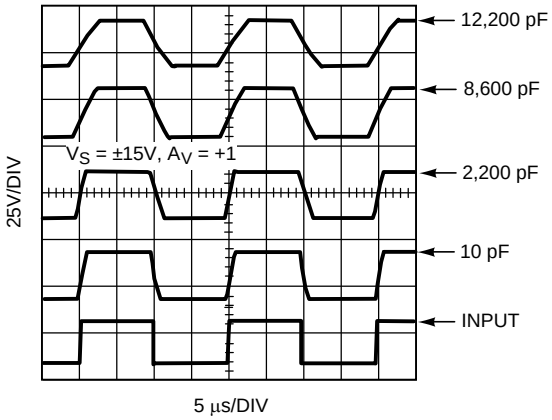

Figure 50. Large Signal Step Response

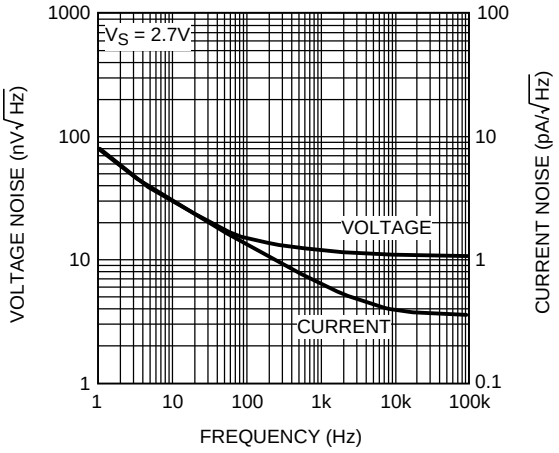

Figure 51. Input Referred Noise Density vs. Frequency

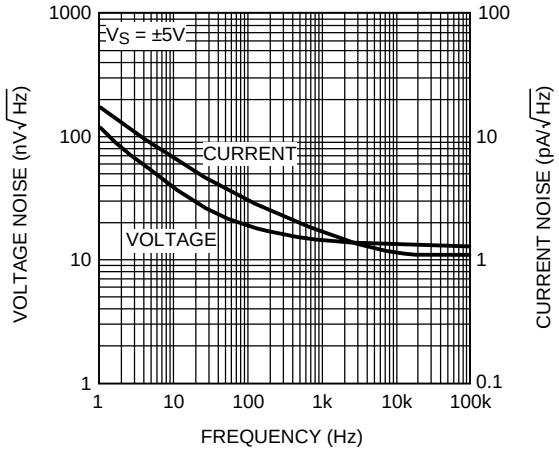

Figure 52. Input Referred Noise Density vs. Frequency

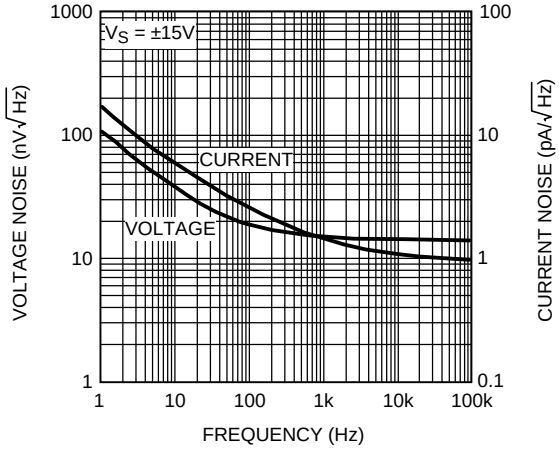

Figure 53. Input Referred Noise Density vs. Frequency

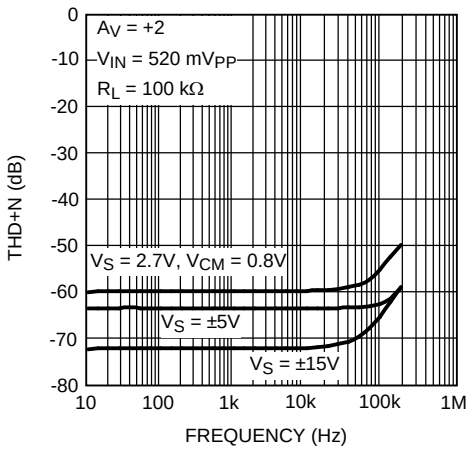

Figure 54. THD+N vs. Frequency

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Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

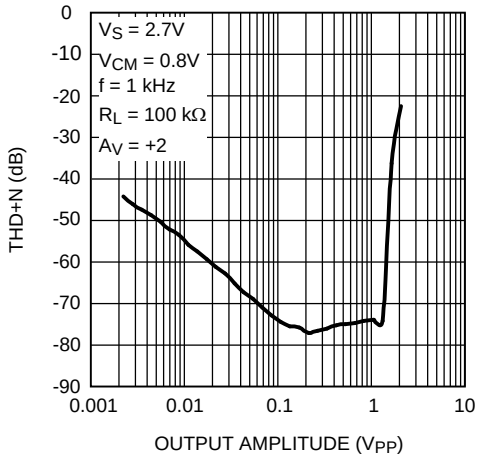


Figure 55. THD+N vs. Output Amplitude

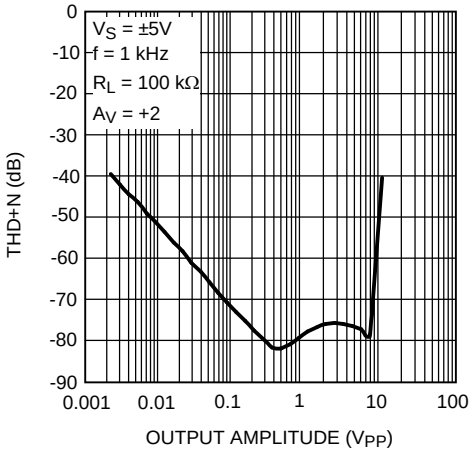


Figure 56. THD+N vs. Output Amplitude

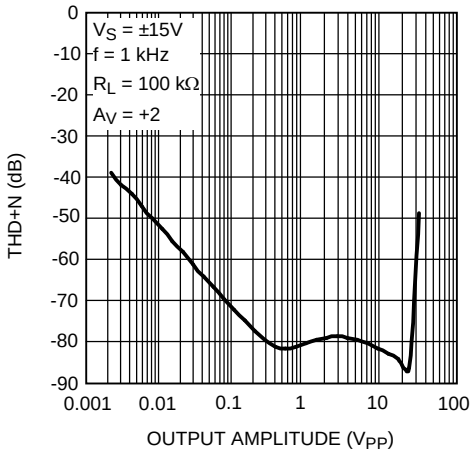


Figure 57. THD+N vs. Output Amplitude

8 Detailed Description

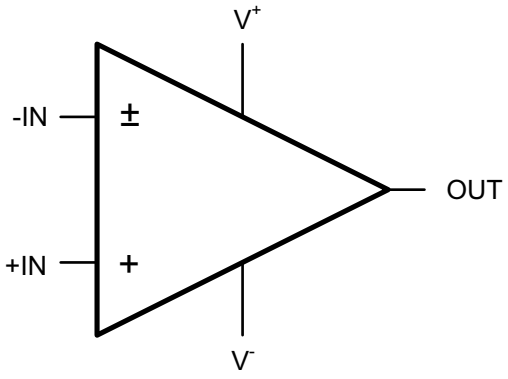
8.1 Overview

The LM732xx devices are rail-to-rail input and output amplifiers with wide operating voltages and high-output currents. The LM732xx family is efficient, achieving 18-V/µs slew rate and 20-MHz unity gain bandwidth while requiring only 1 mA of supply current per op amp. The LM732xx device performance is fully specified for operation at 2.7 V, ±5 V and ±15 V.

The LM732xx devices are designed to drive unlimited capacitive loads without oscillations. All LM7321x and LM7322x parts are tested at −40°C, 125°C, and 25°C, with modern automatic test equipment. High performance from −40°C to 125°C, detailed specifications, and extensive testing makes them suitable for industrial, automotive, and communications applications.

Greater than rail-to-rail input common-mode voltage range with 50 dB of common-mode rejection across this wide voltage range, allows both high-side and low-side sensing. Most device parameters are insensitive to power supply voltage, and this makes the parts easier to use where supply voltage may vary, such as automotive electrical systems and battery-powered equipment. These amplifiers have true rail-to-rail output and can supply a respectable amount of current (15 mA) with minimal head room from either rail (300 mV) at low distortion (0.05% THD+Noise).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Output Short Circuit Current and Dissipation Issues

The LM732xx output stage is designed for maximum output current capability. Even though momentary output shorts to ground and either supply can be tolerated at all operating voltages, longer lasting short conditions can cause the junction temperature to rise beyond the absolute maximum rating of the device, especially at higher supply voltage conditions. Below supply voltage of 6 V, the output short circuit condition can be tolerated indefinitely.

With the op amp tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power itself could include an average value (due to a DC load current) and an AC component. DC load current would flow if there is an output voltage offset, or the output AC average current is non-zero, or if the op amp operates in a single supply application where the output is maintained somewhere in the range of linear operation.

Therefore,

$$P_{TOTAL} = P_Q + P_{DC} + P_{AC} \quad (1)$$

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Feature Description (continued)

The Op Amp Quiescent Power Dissipation is calculated as:

$$P_Q = I_S \times V_S$$

where

- I_S: Supply Current
- V_S: Total Supply Voltage ($V^+ - V^-$) (2)

The DC Load Power is calculated as:

$$P_{DC} = I_O \times (V_r - V_o)$$

where

- V_O: Average Output Voltage
- V_r: V^+ for sourcing and V^- for sinking current (3)

The AC Load Power is calculated as P_{AC} = See Table 1.

Table 1 shows the maximum AC component of the load power dissipated by the op amp for standard Sinusoidal, Triangular, and Square Waveforms:

Table 1. Normalized AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} ($W.\Omega/V^2$)		
Sinusoidal	Triangular	Square
50.7×10^{-3}	46.9×10^{-3}	62.5×10^{-3}

The table entries are normalized to V_S^2/R_L. To figure out the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor V_S^2/R_L. For example, with ±12-V supplies, a 600-Ω load, and triangular waveform power dissipation in the output stage is calculated as:

$$P_{AC} = (46.9 \times 10{-}^{3}) \times (242/600) = 45.0 \text{ mW} \quad (4)$$

The maximum power dissipation allowed at a certain temperature is a function of maximum die junction temperature ($T_{J(MAX)}$) allowed, ambient temperature T_A, and package thermal resistance from junction to ambient, θ_{JA}.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (5)$$

For the LM732xx, the maximum junction temperature allowed is 150°C at which no power dissipation is allowed. The power capability at 25°C is given by the following calculations:

For VSSOP package:

$$P_{D(MAX)} = \frac{150℃ - 25℃}{235℃/W} = 0.53 \text{ W} \quad (6)$$

For SOIC package:

$$P_{D(MAX)} = \frac{150℃ - 25℃}{165℃/W} = 0.76 \text{ W} \quad (7)$$

Similarly, the power capability at 125°C is given by:

For VSSOP package:

$$P_{D(MAX)} = \frac{150℃ - 125℃}{235℃/W} = 0.11 \text{ W} \quad (8)$$

For SOIC package:

$$P_{D(MAX)} = \frac{150℃ - 125℃}{165℃/W} = 0.15 \text{ W} \quad (9)$$

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Figure 58 shows the power capability vs. temperature for VSSOP and SOIC packages. The area under the maximum thermal capability line is the operating area for the device. When the device works in the operating area where P_{TOTAL} is less than $P_{D(MAX)}$, the device junction temperature will remain below 150°C. If the intersection of ambient temperature and package power is above the maximum thermal capability line, the junction temperature will exceed 150°C and this should be strictly prohibited.

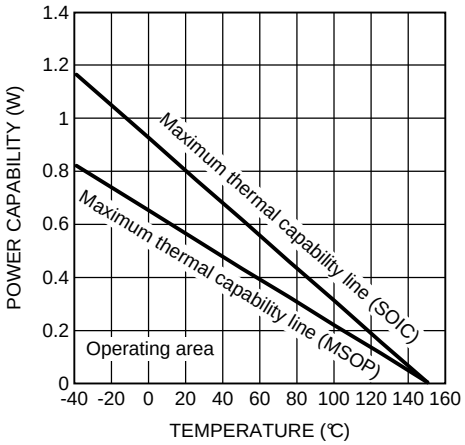

Figure 58. Power Capability vs. Temperature

When high power is required and ambient temperature can't be reduced, providing air flow is an effective approach to reduce thermal resistance therefore to improve power capability.

8.3.2 Estimating the Output Voltage Swing

It is important to keep in mind that the steady-state output current will be less than the current available when there is an input overdrive present. For steady-state conditions, the Output Voltage vs. Output Current plot (*Typical Characteristics* section) can be used to predict the output swing. Figure 59 and Figure 60 show this performance along with several load lines corresponding to loads tied between the output and ground. In each cases, the intersection of the device plot at the appropriate temperature with the load line would be the typical output swing possible for that load. For example, a 1-kΩ load can accommodate an output swing to within 250 mV of V^- and to 330 mV of V^+ (V_S = ±15 V) corresponding to a typical 29.3 V_{PP} unclipped swing.

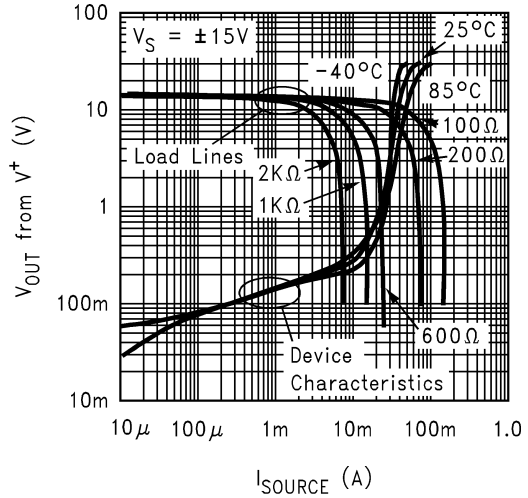

Figure 59. Output Sourcing Characteristics With Load Lines

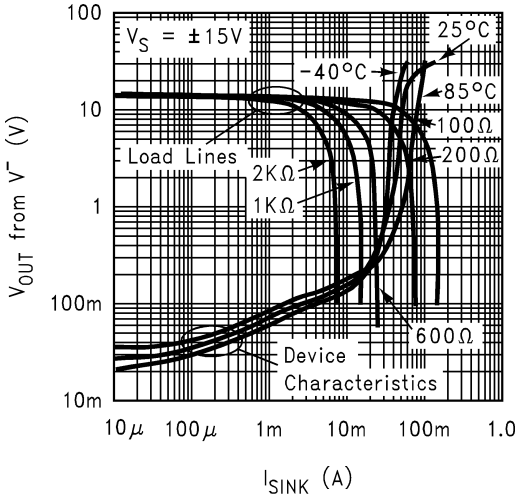

Figure 60. Output Sinking Characteristics With Load Lines

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8.4 Device Functional Modes

8.4.1 Driving Capacitive Loads

The LM732xx are specifically designed to drive unlimited capacitive loads without oscillations as shown in Figure 61.

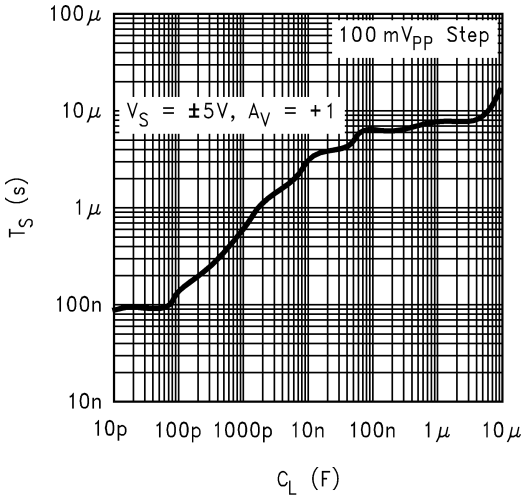

Figure 61. ±5% Settling Time vs. Capacitive Load

In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads as shown in Figure 62 and Figure 63.

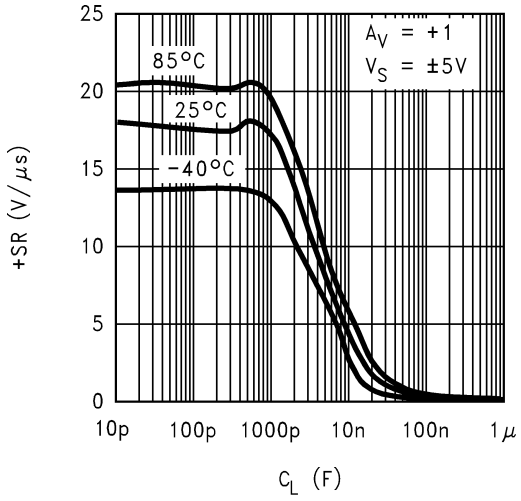

Figure 62. +SR vs. Capacitive Load

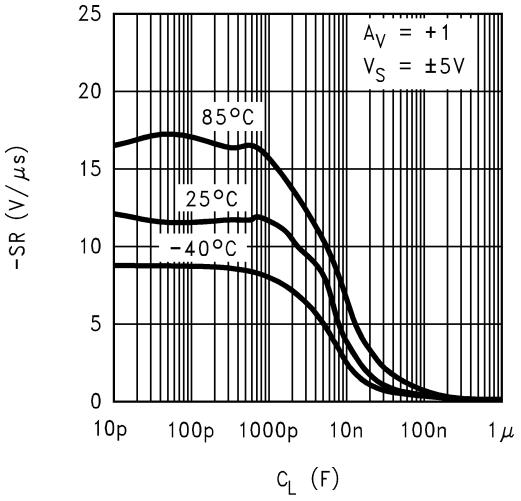

Figure 63. −SR vs. Capacitive Load

The combination of these features is ideal for applications such as TFT flat panel buffers, A/D converter input amplifiers, and so forth.

However, as in most op amps, addition of a series isolation resistor between the op amp and the capacitive load improves the settling and overshoot performance.

Output current drive is an important parameter when driving capacitive loads. This parameter will determine how fast the output voltage can change. Referring to the Slew Rate vs. Capacitive Load Plots (*Typical Characteristics* section), two distinct regions can be identified. Below about 10,000 pF, the output Slew Rate is solely determined by the compensation capacitor value of the op amp and available current into that capacitor. Beyond 10 nF, the Slew Rate is determined by the available output current of the op amp.

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Device Functional Modes (continued)

NOTE

Because of the lower output sourcing current compared to the sinking one, the Slew Rate limit under heavy capacitive loading is determined by the positive transitions.

An estimate of positive and negative slew rates for loads larger than 100 nF can be made by dividing the short circuit current value by the capacitor.

For the LM732xx, the available output current increases with the input overdrive. Referring to Figure 64 and Figure 65, it can be seen that both sourcing and sinking short circuit current increase as input overdrive increases. In a closed-loop amplifier configuration, during transient conditions while the fed back output has not quite caught up with the input, there will be an overdrive imposed on the input allowing more output current than would normally be available under steady-state condition. Because of this feature, the output stage quiescent current of the op amp can be kept to a minimum, thereby reducing power consumption, while enabling the device to deliver large output current when the need arises (such as during transients).

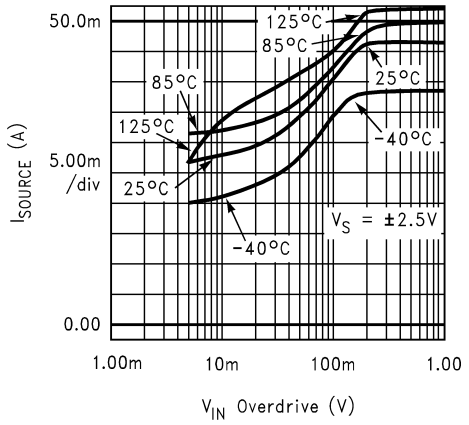

Figure 64. Output Short Circuit Sourcing Current vs. Input Overdrive

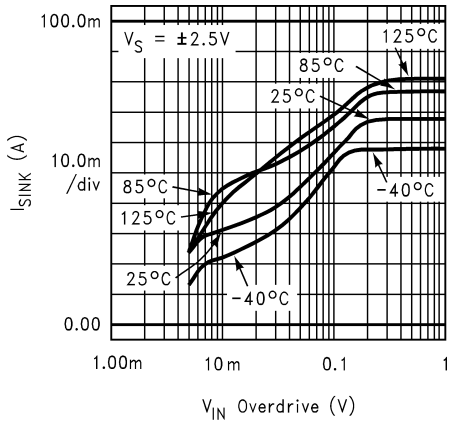

Figure 65. Output Short Circuit Sinking Current vs. Input Overdrive

Figure 66 shows the output voltage, output current, and the resulting input overdrive with the device set for A_V = +1 and the input tied to a 1-V_{PP} step function driving a 47-nF capacitor. As can be seen, during the output transition, the input overdrive reaches 1-V peak and is more than enough to cause the output current to increase to its maximum value (see Figure 64 and Figure 65 plots).

NOTE

Because of the larger output sinking current compared to the sourcing one, the output negative transition is faster than the positive one.

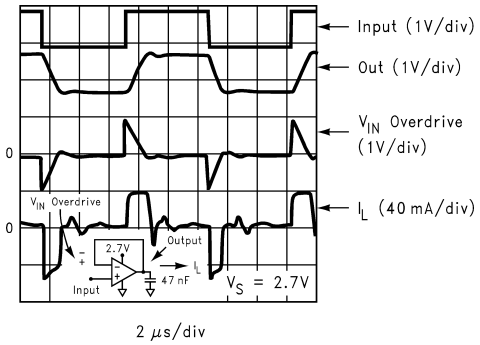

Figure 66. Buffer Amplifier Scope Photo

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Similar High-Output Devices

The LM7332 is a dual rail-to-rail amplifier with a slightly lower GBW capable of sinking and sourcing 100 mA. It is available in SOIC and VSSOP packages.

The LM4562 is dual op amp with very low noise and 0.7-mV voltage offset.

The LME49870 and LME49860 are single and dual low-noise amplifiers that can work from ±22-V supplies.

9.1.2 Other High Performance SOT-23 Ampliers

The LM7341 is a 4-MHz rail-to-rail input and output part that requires only 0.6 mA to operate, and can drive unlimited capacitive load. It has a voltage gain of 97 dB, a CMRR of 93 dB, and a PSRR of 104 dB.

The LM6211 is a 20-MHz part with CMOS input, which runs on ±12-V or 24-V single supplies. It has rail-to-rail output and low noise.

The LM7121 has a gain bandwidth of 235 MHz.

Detailed information on these parts can be found at www.ti.com.

9.2 Typical Application

Figure 67 shows a typical application where the LM732xx is used as a buffer amplifier for the V_{COM} signal employed in a TFT LCD flat panel:

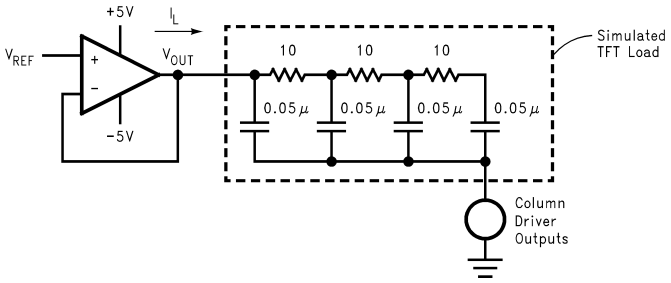

Figure 67. V_{COM} Driver Application Schematic

9.2.1 Design Requirements

For this example application, the supply voltage is +5 V, and noninverting gain is necessary.

Typical Application (continued)

9.2.2 Detailed Design Procedure

Figure 68 shows the time domain response of the amplifier when used as a V_{COM} buffer/driver with V_{REF} at ground. In this application, the op amp loop will try and maintain its output voltage based on the voltage on its noninverting input (V_{REF}) despite the current injected into the TFT simulated load. As long as this load current is within the range tolerable by the LM732xx (45-mA sourcing and 65-mA sinking for ±5-V supplies), the output will settle to its final value within less than 2 µs.

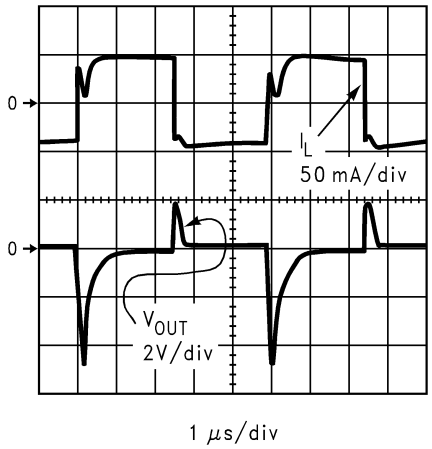

Figure 68. V_{COM} Driver Performance Scope Photo

9.2.3 Application Curve

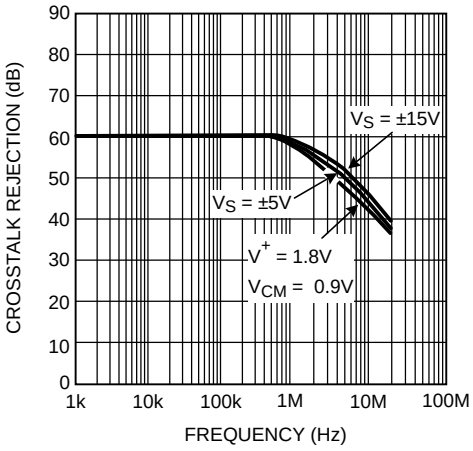

Figure 69. Crosstalk Rejection vs. Frequency

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10 Power Supply Recommendations

The use of supply decoupling is mandatory in most applications. As with most relatively high-speed or high-output current op amps, best results are achieved when each supply line is decoupled with two capacitors; a small value ceramic capacitor (about 0.01 µF) placed very close to the supply lead in addition to a large value Tantalum or Aluminum (> 4.7 µF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at high frequencies while the large capacitor will act as the charge *bucket* for fast load current spikes at the op amp output. The combination of these capacitors will provide supply decoupling and will help keep the op amp oscillation free under any load.

11 Layout

11.1 Layout Guidelines

Take care to minimize the loop area formed by the bypass capacitor connection between supply pins and ground. A ground plane underneath the device is recommended; any bypass components to ground should have a nearby via to the ground plane. The optimum bypass capacitor placement is closest to the corresponding supply pin. Use of thicker traces from the bypass capacitors to the corresponding supply pins will lower the power supply inductance and provide a more stable power supply.

The feedback components should be placed as close to the device as possible to minimize stray parasitics.

11.2 Layout Example

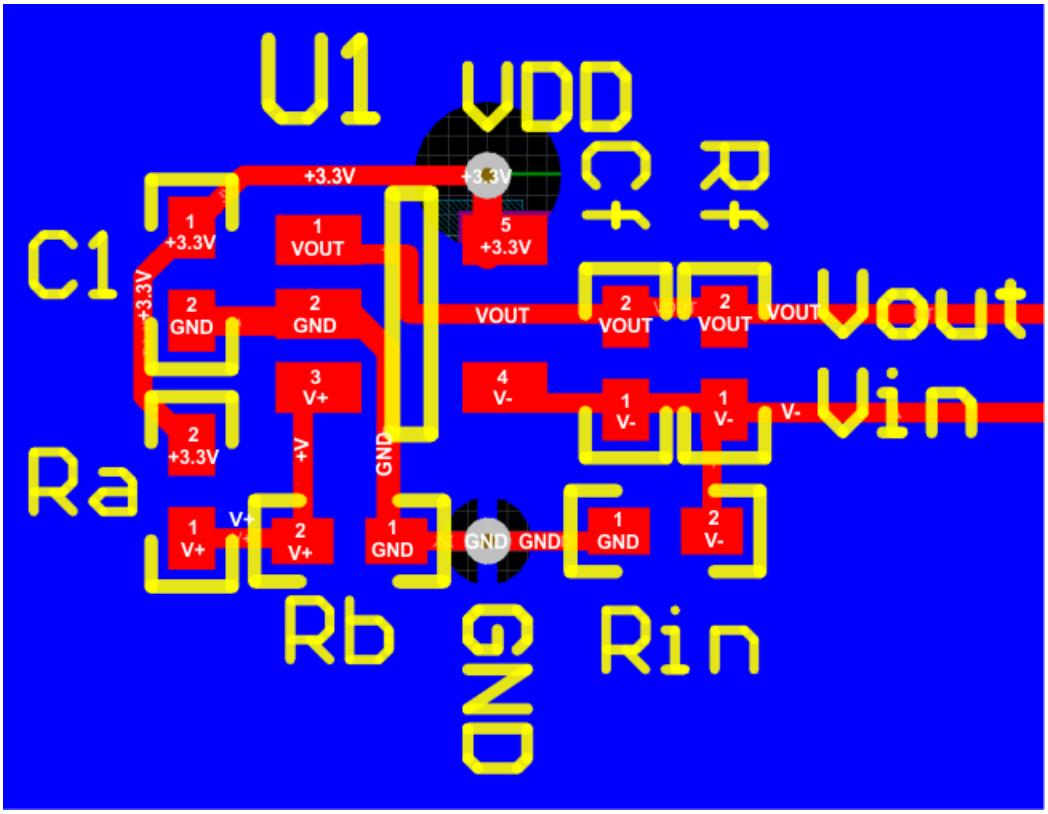

Figure 70. LM732xx Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM7321	Click here	Click here	Click here	Click here	Click here
LM7322	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM7321MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM732 1MA	Samples
LM7321MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AU4A	Samples
LM7321QMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AR8A	Samples
LM7322MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM732 2MA	Samples
LM7322MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AZ4A	Samples
LM7322QMAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM732 2QMA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LM7321, LM7321-Q1, LM7322, LM7322-Q1 :

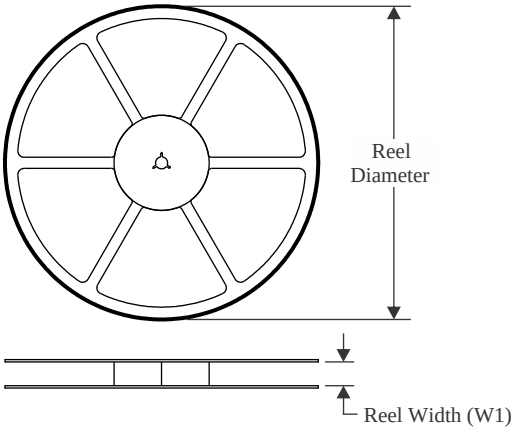
- Catalog : LM7321, LM7322
- Automotive : LM7321-Q1, LM7322-Q1

NOTE: Qualified Version Definitions:

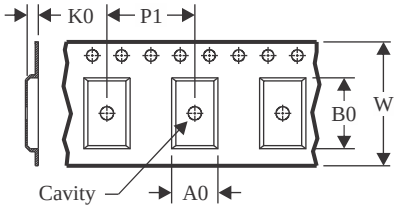
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

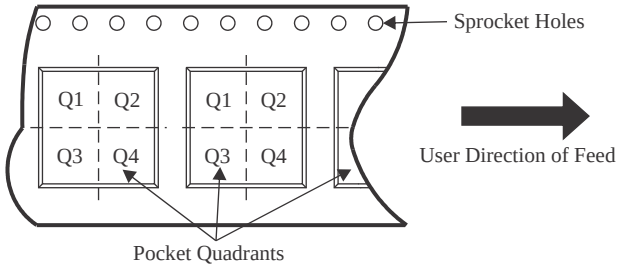


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

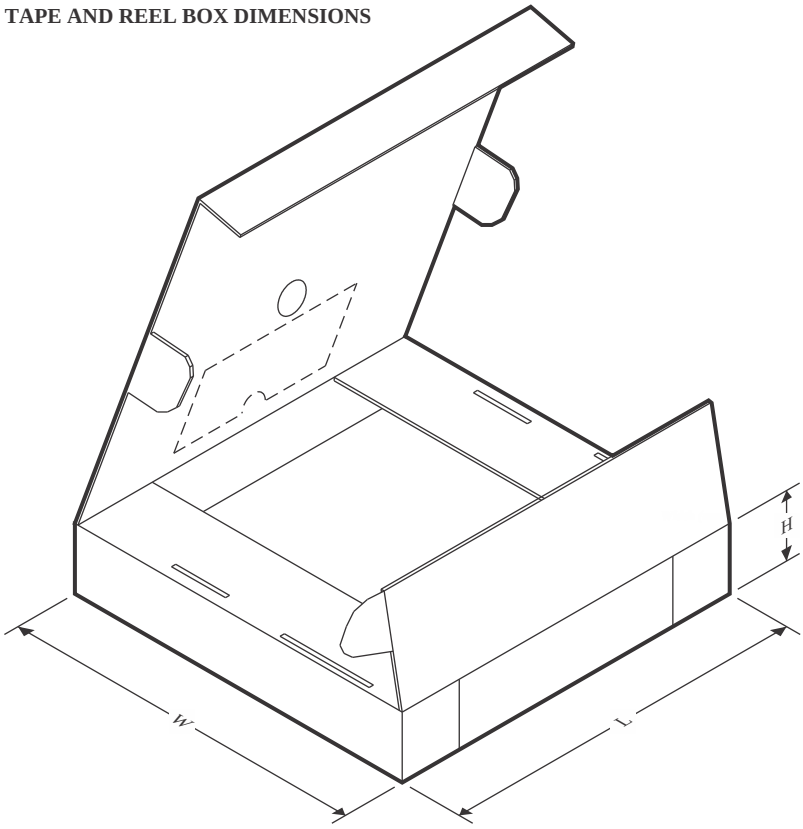
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7321MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM7321MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7321QMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7322MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM7322MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM7322QMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

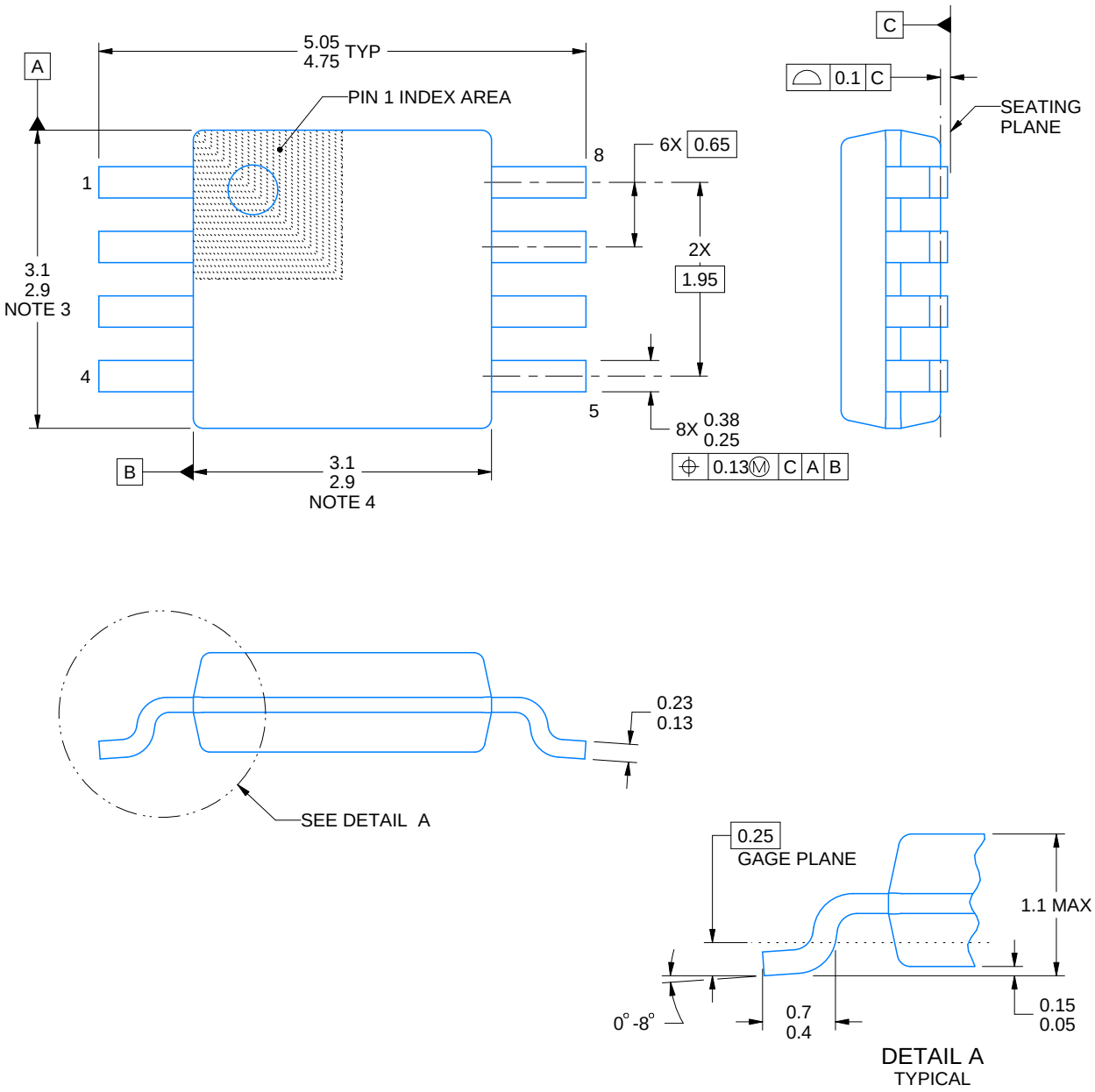
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7321MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM7321MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM7321QMFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM7322MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM7322MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM7322QMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

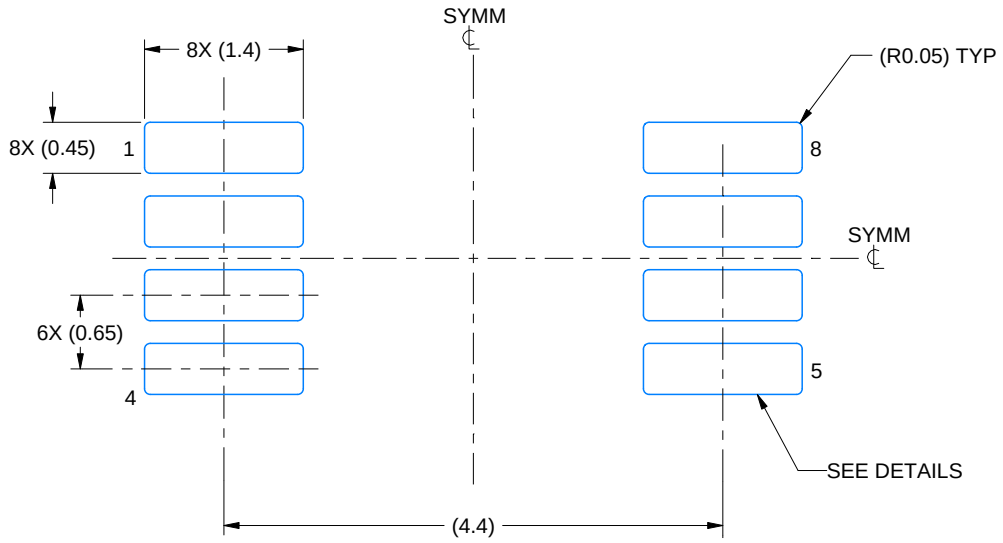
SMALL OUTLINE PACKAGE



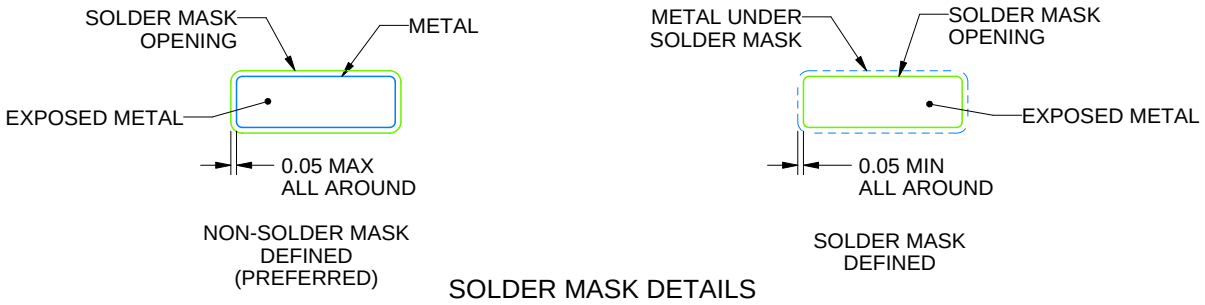
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

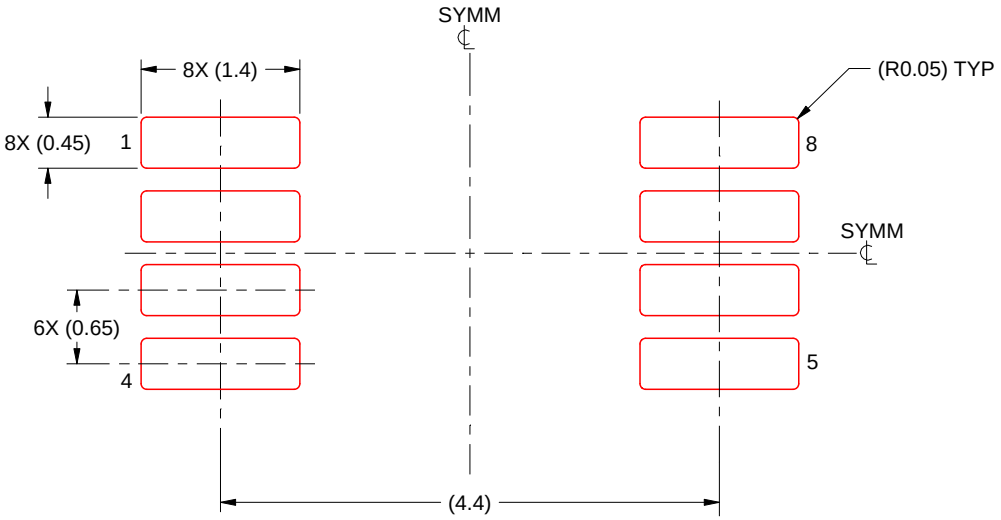


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

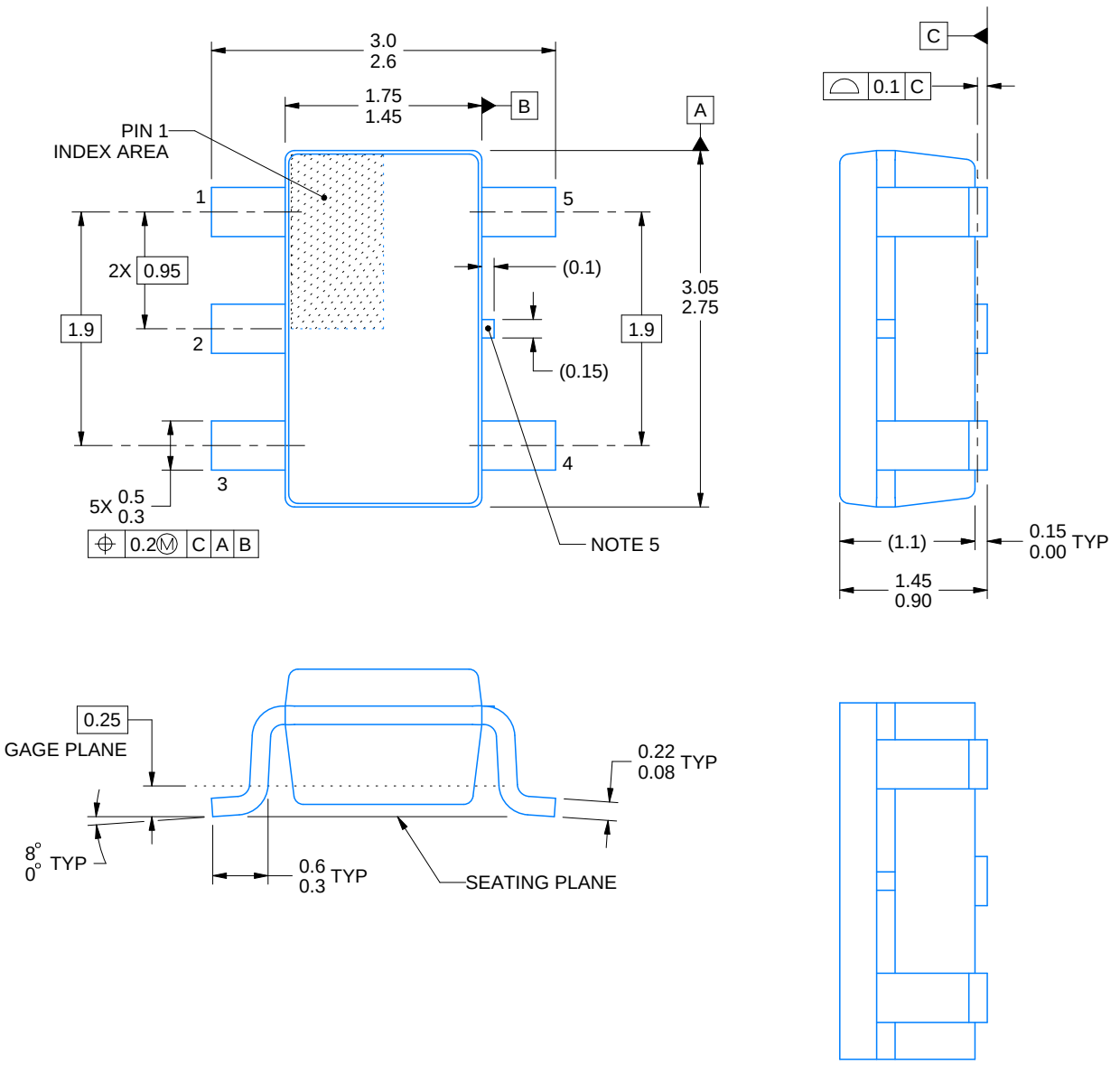
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

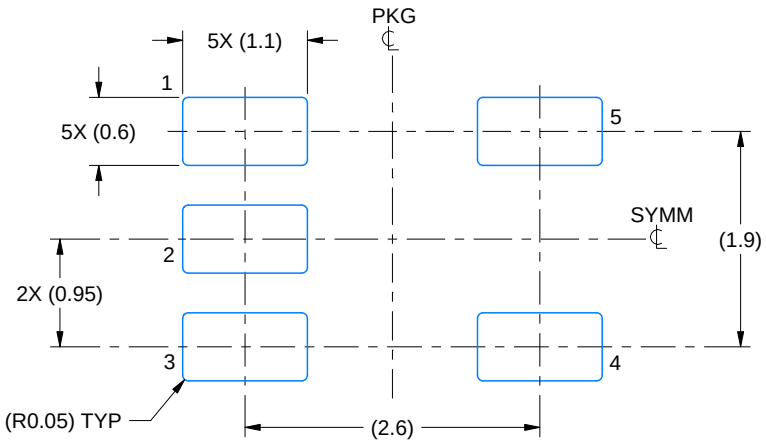


ALTERNATIVE PACKAGE SINGULATION VIEW

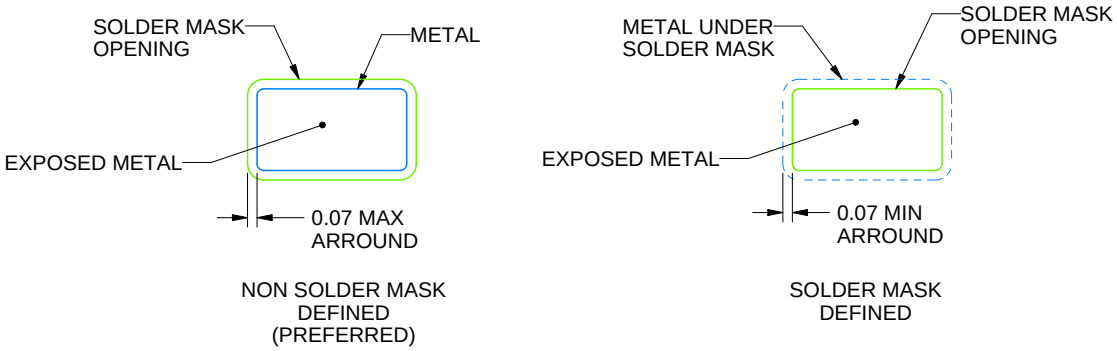
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

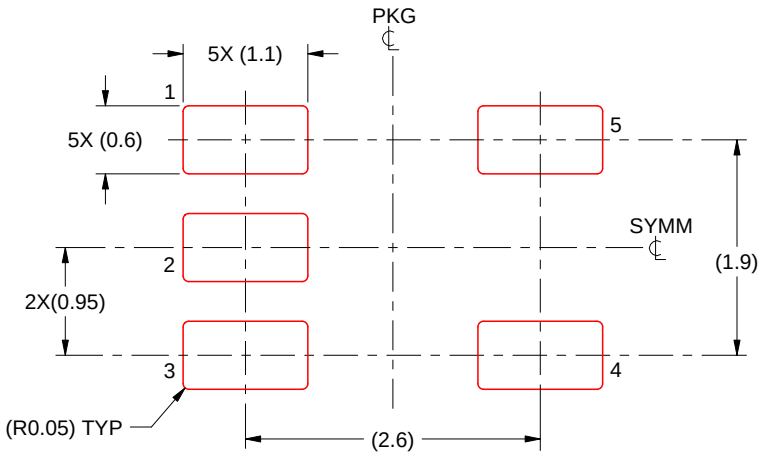


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

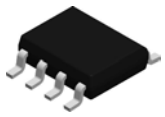


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

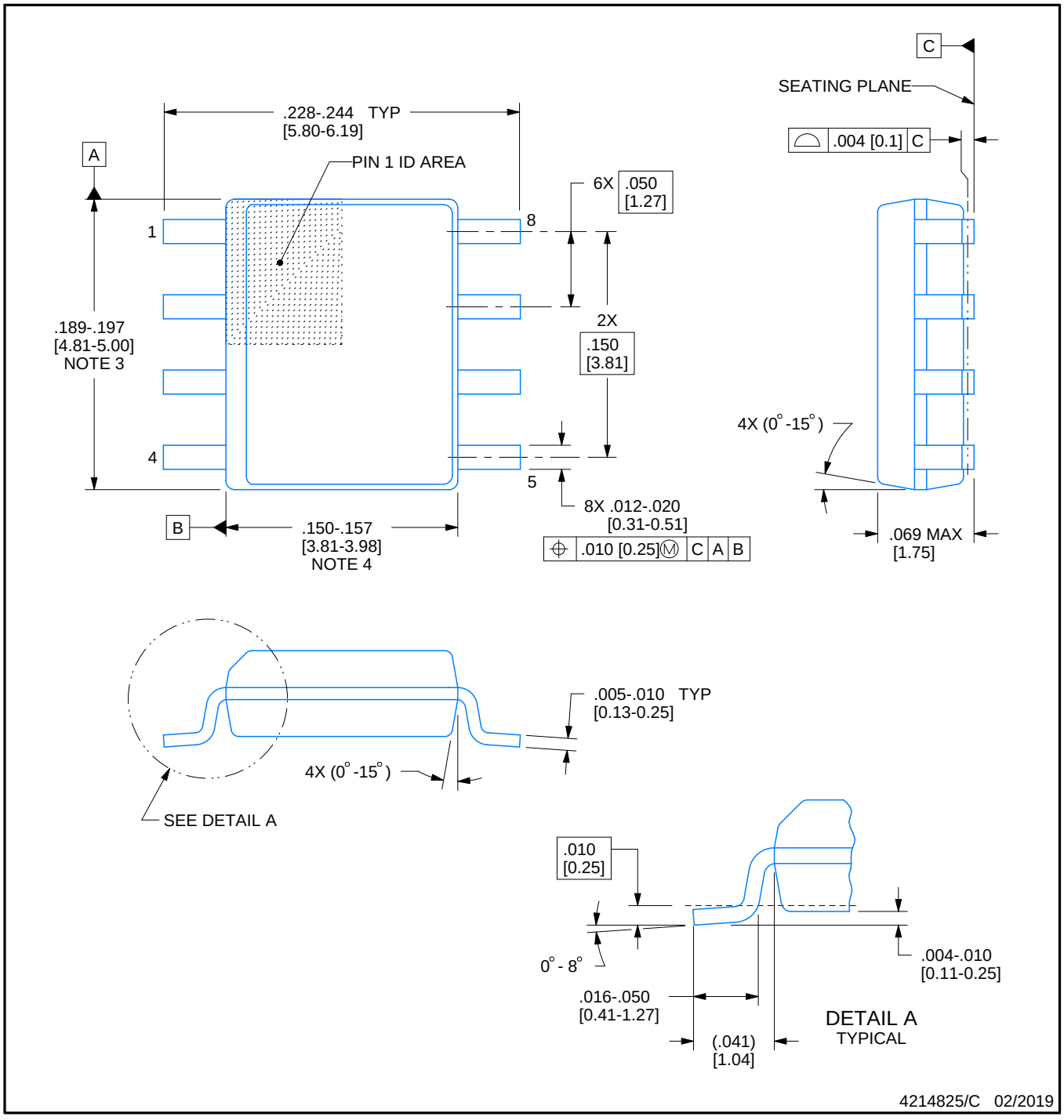


PACKAGE OUTLINE

D0008A

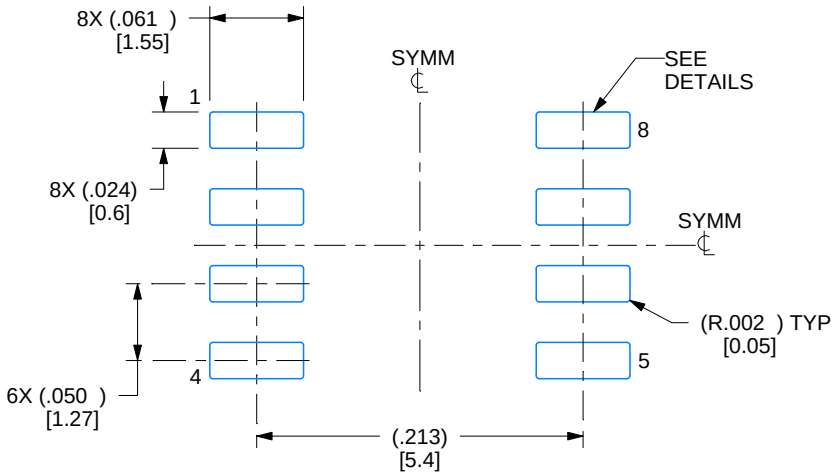
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

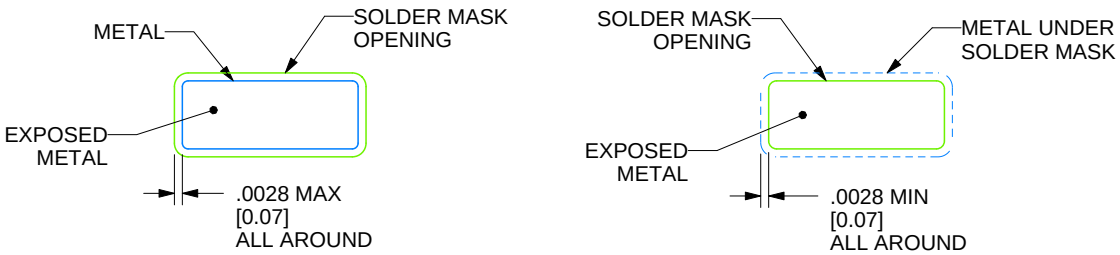


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

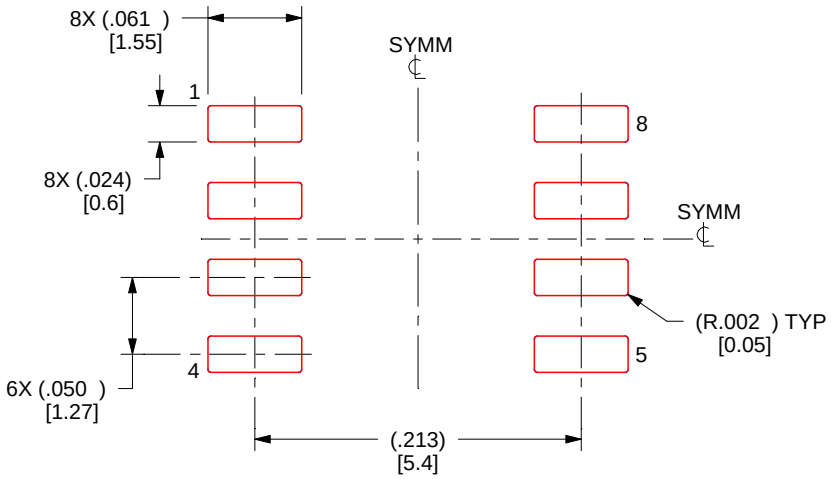
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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