



THE DATASHEET OF LM6142BIM



LM6142/LM6144 17 MHz Rail-to-Rail Input-Output Operational Amplifiers

 Check for Samples: [LM6142](#), [LM6144](#)

FEATURES

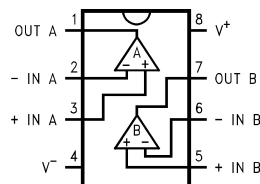
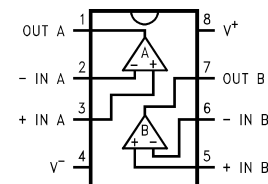
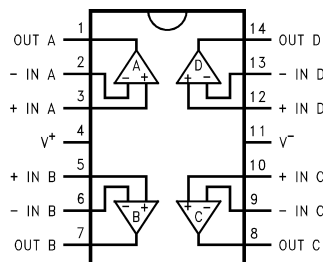
 At $V_S = 5V$. Typ Unless Noted.

- Rail-to-rail Input CMVR $-0.25V$ to $5.25V$
- Rail-to-Rail Output Swing $0.005V$ to $4.995V$
- Wide Gain-Bandwidth: $17MHz$ at $50kHz$ (typ)
- Slew Rate:
 - Small Signal, $5V/\mu s$
 - Large Signal, $30V/\mu s$
- Low Supply Current $650\mu A/Amplifier$
- Wide Supply Range $1.8V$ to $24V$
- CMRR $107dB$
- Gain $108dB$ with $R_L = 10k$
- PSRR $87dB$

APPLICATIONS

- Battery Operated Instrumentation
- Depth Sounders/Fish Finders
- Barcode Scanners
- Wireless Communications
- Rail-to-Rail in-out Instrumentation Amps

Connection Diagrams


**Figure 1. 8-Pin CDIP
Top View**

**Figure 2. 8-Pin PDIP/SOIC
Top View**

**Figure 3. 14-Pin PDIP/SOIC
Top View**

DESCRIPTION

Using patent pending new circuit topologies, the LM6142/LM6144 provides new levels of performance in applications where low voltage supplies or power limitations previously made compromise necessary. Operating on supplies of $1.8V$ to over $24V$, the LM6142/LM6144 is an excellent choice for battery operated systems, portable instrumentation and others.

The greater than rail-to-rail input voltage range eliminates concern over exceeding the common-mode voltage range. The rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

High gain-bandwidth with $650\mu A/Amplifier$ supply current opens new battery powered applications where previous higher power consumption reduced battery life to unacceptable levels. The ability to drive large capacitive loads without oscillating functionally removes this common problem.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

| | |
|---|--|
| ESD Tolerance ⁽³⁾ | 2500V |
| Differential Input Voltage | 15V |
| Voltage at Input/Output Pin | (V ⁺) + 0.3V, (V ⁻) - 0.3V |
| Supply Voltage (V ⁺ - V ⁻) | 35V |
| Current at Input Pin | ±10mA |
| Current at Output Pin ⁽⁴⁾ | ±25mA |
| Current at Power Supply Pin | 50mA |
| Lead Temperature (soldering, 10 sec) | 260°C |
| Storage Temp. Range | -65°C to +150°C |
| Junction Temperature ⁽⁵⁾ | 150°C |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human body model, 1.5kΩ in series with 100pF.
- (4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
- (5) The maximum power dissipation is a function of T_{J(MAX)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A)/θ_{JA}. All numbers apply for packages soldered directly into a PC board.

Operating Ratings⁽¹⁾

| | | |
|---------------------------------------|--------------------------------|---------|
| Supply Voltage | 1.8V ≤ V ⁺ ≤ 24V | |
| Temperature Range LM6142, LM6144 | -40°C ≤ T _A ≤ +85°C | |
| Thermal Resistance (θ _{JA}) | P Package, 8-Pin PDIP | 115°C/W |
| | D Package, 8-Pin SOIC | 193°C/W |
| | NFF Package, 14-Pin PDIP | 81°C/W |
| | D Package, 14-Pin SOIC | 126°C/W |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

5.0V DC Electrical Characteristics⁽¹⁾

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V⁺ = 5.0V, V⁻ = 0V, V_{CM} = V_O = V⁺/2 and R_L > 1 MΩ to V⁺/2.

Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ ⁽²⁾ | LM6144AI LM6142AI Limit ⁽³⁾ | LM6144BI LM6142BI Limit ⁽³⁾ | Units |
|-------------------|---------------------------------------|---------------------------|--------------------|--|--|-------|
| V _{OS} | Input Offset Voltage | | 0.3 | 1.0 | 2.5 | mV |
| | | | | 2.2 | 3.3 | max |
| TCV _{OS} | Input Offset Voltage Average Drift | | 3 | | | μV/°C |
| I _B | Input Bias Current | | 170 | 250 | 300 | nA |
| | | 0V ≤ V _{CM} ≤ 5V | 180 | 280 | | max |
| | | | | 526 | 526 | |

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of the internal self heating where T_J > T_A.
- (2) Typical values represent the most likely parametric norm.
- (3) All limits are guaranteed by testing or statistical analysis.

5.0V DC Electrical Characteristics⁽¹⁾ (continued)

Unless otherwise specified, all limits guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 5.0\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{M}\Omega$ to $V^+/2$. **Boldface limits** apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ ⁽²⁾ | LM6144AI LM6142AI Limit ⁽³⁾ | LM6144BI LM6142BI Limit ⁽³⁾ | Units |
|-----------------|-------------------------------------|---|---------------------|--|--|----------------------|
| I_{OS} | Input Offset Current | | 3 | 30 80 | 30 80 | nA max |
| R_{IN} | Input Resistance, C_M | | 126 | | | M Ω |
| CMRR | Common Mode Rejection Ratio | $0\text{V} \leq V_{\text{CM}} \leq 4\text{V}$ | 107 | 84 78 | 84 78 | dB min |
| | | $0\text{V} \leq V_{\text{CM}} \leq 5\text{V}$ | 82 79 | 66 64 | 66 64 | |
| PSRR | Power Supply Rejection Ratio | $5\text{V} \leq V^+ \leq 24\text{V}$ | 87 | 80 78 | 80 78 | |
| V_{CM} | Input Common-Mode Voltage Range | | -0.25 5.25 | 0 5.0 | 0 5.0 | V |
| A_V | Large Signal Voltage Gain | $R_L = 10\text{k}$ | 270 70 | 100 33 | 80 25 | V/mV min |
| V_O | Output Swing | $R_L = 100\text{k}$ | 0.005 | 0.01 0.013 | 0.01 0.013 | V max |
| | | | 4.995 | 4.98 4.93 | 4.98 4.93 | V min |
| | | | | | | |
| | | $R_L = 10\text{k}$ | 0.02 | | | V max |
| | | | 4.97 | | | V min |
| | | $R_L = 2\text{k}$ | 0.06 | 0.1 0.133 | 0.1 0.133 | V max |
| 4.90 | 4.86 4.80 | | 4.86 4.80 | V min | | |
| I_{SC} | Output Short Circuit Current LM6142 | Sourcing | 13 | 10 4.9 35 | 8 4 35 | mA min max |
| | | | 24 | 10 5.3 35 | 10 5.3 35 | mA min max |
| | | Sinking | 8 | 6 3 35 | 6 3 35 | mA min max |
| | | | 22 | 8 4 35 | 8 4 35 | mA min max |
| I_{SC} | Output Short Circuit Current LM6144 | Sourcing | 8 | 6 3 35 | 6 3 35 | mA min max |
| | | | 22 | 8 4 35 | 8 4 35 | mA min max |
| | | Sinking | 8 | 8 4 35 | 8 4 35 | mA min max |
| | | | 650 | 800 880 | 800 880 | μA max |

5.0V AC Electrical Characteristics⁽¹⁾

Unless Otherwise Specified, All Limits Guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 5.0\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$ to $V^+/2$. **Boldface limits** apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ ⁽²⁾ | LM6144AI LM6142AI Limit ⁽³⁾ | LM6144BI LM6142BI Limit ⁽³⁾ | Units |
|----------|------------------------------|--|--------------------|--|--|--------------------------------------|
| SR | Slew Rate | 8 V_{PP} @ $V^+ 12\text{V}$ $R_S > 1\text{ k}\Omega$ | 25 | 15 | 13 | V/ μs min |
| | | | | 13 | 11 | |
| GBW | Gain-Bandwidth Product | $f = 50\text{ kHz}$ | 17 | 10 | 10 | MHz min |
| | | | | 6 | 6 | |
| ϕ_m | Phase Margin | | 38 | | | Deg |
| | Amp-to-Amp Isolation | | 130 | | | dB |
| e_n | Input-Referred Voltage Noise | $f = 1\text{ kHz}$ | 16 | | | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ |
| i_n | Input-Referred Current Noise | $f = 1\text{ kHz}$ | 0.22 | | | $\frac{\text{pA}}{\sqrt{\text{Hz}}}$ |
| T.H.D. | Total Harmonic Distortion | $f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega$, | 0.003 | | | % |

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of the internal self heating where $T_J > T_A$.
- (2) Typical values represent the most likely parametric norm.
- (3) All limits are guaranteed by testing or statistical analysis.

2.7V DC Electrical Characteristics⁽¹⁾

Unless Otherwise Specified, All Limits Guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$ to $V^+/2$. **Boldface limits** apply at the temperature extreme

| Symbol | Parameter | Conditions | Typ ⁽²⁾ | LM6144AI LM6142AI Limit ⁽³⁾ | LM6144BI LM6142BI Limit ⁽³⁾ | Units |
|-----------------|---------------------------------|---|--------------------|--|--|------------------|
| V_{OS} | Input Offset Voltage | | 0.4 | 1.8 | 2.5 | mV max |
| | | | | 4.3 | 5 | |
| I_B | Input Bias Current | | 150 | 250 | 300 | nA max |
| | | | | 526 | 526 | |
| I_{OS} | Input Offset Current | | 4 | 30 | 30 | nA max |
| | | | | 80 | 80 | |
| R_{IN} | Input Resistance | | 128 | | | $\text{M}\Omega$ |
| CMRR | Common Mode Rejection Ratio | $0\text{V} \leq V_{\text{CM}} \leq 1.8\text{V}$ | 90 | | | dB min |
| | | $0\text{V} \leq V_{\text{CM}} \leq 2.7\text{V}$ | 76 | | | |
| PSRR | Power Supply Rejection Ratio | $3\text{V} \leq V^+ \leq 5\text{V}$ | 79 | | | |
| V_{CM} | Input Common-Mode Voltage Range | | -0.25 | 0 | 0 | V min |
| | | | 2.95 | 2.7 | 2.7 | V max |
| A_V | Large Signal Voltage Gain | $R_L = 10\text{k}$ | 55 | | | V/mV min |
| V_O | Output Swing | $R_L = 100\text{k}\Omega$ | 0.019 | 0.08 | 0.08 | V max |
| | | | | 0.112 | 0.112 | |
| | | | | 2.67 | 2.66 | |
| | | | | 2.25 | 2.25 | |

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of the internal self heating where $T_J > T_A$.
- (2) Typical values represent the most likely parametric norm.
- (3) All limits are guaranteed by testing or statistical analysis.

2.7V DC Electrical Characteristics⁽¹⁾ (continued)

Unless Otherwise Specified, All Limits Guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$ to $V^+/2$.

Boldface limits apply at the temperature extreme

| Symbol | Parameter | Conditions | Typ ⁽²⁾ | LM6144AI LM6142AI Limit ⁽³⁾ | LM6144BI LM6142BI Limit ⁽³⁾ | Units |
|--------|----------------|---------------|--------------------|--|--|----------------------|
| I_S | Supply Current | Per Amplifier | 510 | 800 880 | 800 880 | μA max |

2.7V AC Electrical Characteristics⁽¹⁾

Unless Otherwise Specified, All Limits Guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$ to $V^+/2$.

Boldface limits apply at the temperature extreme

| Symbol | Parameter | Conditions | Typ ⁽²⁾ | LM6144AI LM6142AI Limit ⁽³⁾ | LM6144BI LM6142BI Limit ⁽³⁾ | Units |
|----------|------------------------|---------------------|--------------------|--|--|-------|
| GBW | Gain-Bandwidth Product | $f = 50\text{ kHz}$ | 9 | | | MHz |
| Φ_m | Phase Margin | | 36 | | | Deg |
| G_m | Gain Margin | | 6 | | | dB |

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of the internal self heating where $T_J > T_A$.

(2) Typical values represent the most likely parametric norm.

(3) All limits are guaranteed by testing or statistical analysis.

24V Electrical Characteristics⁽¹⁾

Unless Otherwise Specified, All Limits Guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 24\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$ to $V^+/2$.

Boldface limits apply at the temperature extreme

| Symbol | Parameter | Conditions | Typ ⁽²⁾ | LM6144AI LM6142AI Limit ⁽³⁾ | LM6144BI LM6142BI Limit ⁽³⁾ | Units |
|-----------------|---------------------------------|--|--------------------|--|--|------------------|
| V_{OS} | Input Offset Voltage | | 1.3 | 2 4.8 | 3.8 4.8 | mV max |
| I_B | Input Bias Current | | 174 | | | nA max |
| I_{OS} | Input Offset Current | | 5 | | | nA max |
| R_{IN} | Input Resistance | | 288 | | | $\text{M}\Omega$ |
| CMRR | Common Mode Rejection Ratio | $0\text{V} \leq V_{\text{CM}} \leq 23\text{V}$ | 114 | | | dB |
| | | $0\text{V} \leq V_{\text{CM}} \leq 24\text{V}$ | 100 | | | min |
| PSRR | Power Supply Rejection Ratio | $0\text{V} \leq V_{\text{CM}} \leq 24\text{V}$ | 87 | | | |
| V_{CM} | Input Common-Mode Voltage Range | | -0.25 | 0 | 0 | V min |
| | | | 24.25 | 24 | 24 | V max |
| A_V | Large Signal Voltage Gain | $R_L = 10\text{k}$ | 500 | | | V/mV min |
| V_O | Output Swing | $R_L = 10\text{ k}\Omega$ | 0.07 | 0.15 0.185 | 0.15 0.185 | V max |
| | | | 23.85 | 23.81 | 23.81 | V |
| | | | | 23.62 | 23.62 | min |

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of the internal self heating where $T_J > T_A$.

(2) Typical values represent the most likely parametric norm.

(3) All limits are guaranteed by testing or statistical analysis.

24V Electrical Characteristics⁽¹⁾ (continued)

Unless Otherwise Specified, All Limits Guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 24\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$ to $V^+/2$.

Boldface limits apply at the temperature extreme

| Symbol | Parameter | Conditions | Typ ⁽²⁾ | LM6144AI LM6142AI Limit ⁽³⁾ | LM6144BI LM6142BI Limit ⁽³⁾ | Units |
|--------|------------------------|---------------------|--------------------|--|--|----------------------|
| I_S | Supply Current | Per Amplifier | 750 | 1100 1150 | 1100 1150 | μA max |
| GBW | Gain-Bandwidth Product | $f = 50\text{ kHz}$ | 18 | | | MHz |

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ Unless Otherwise Specified

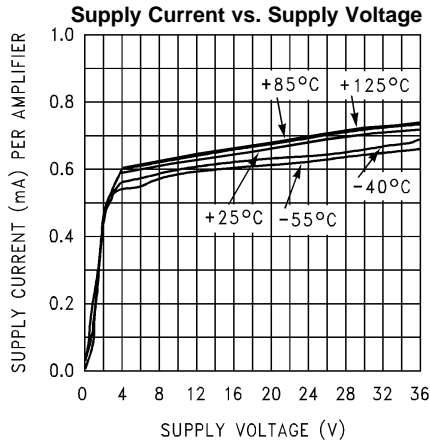


Figure 4.

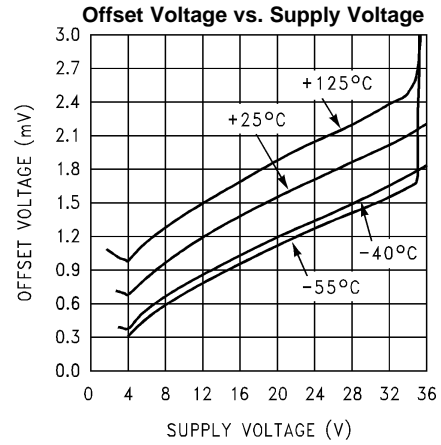


Figure 5.

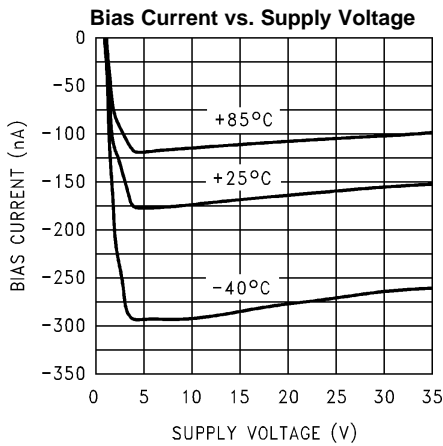


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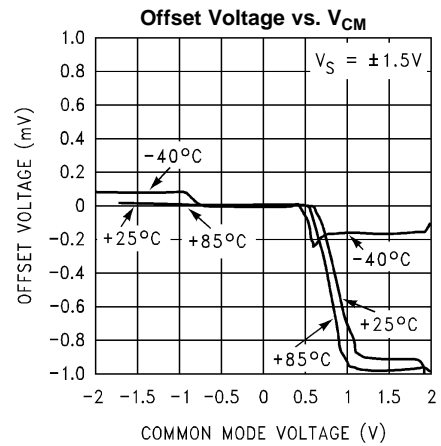


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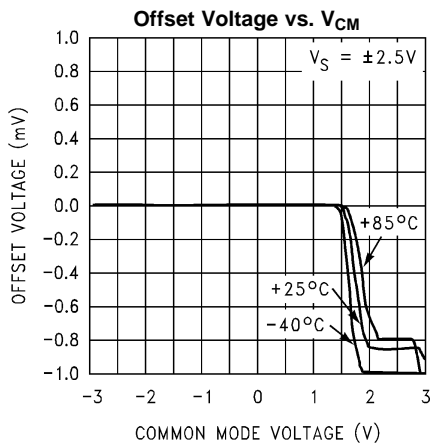


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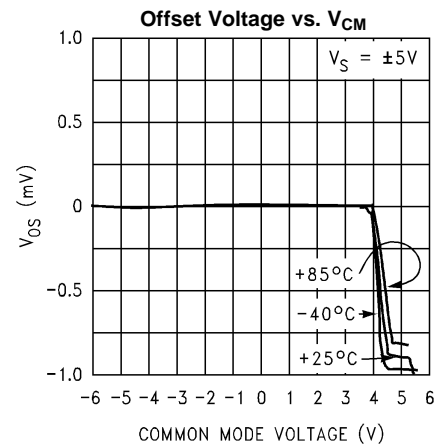


Figure 9.

Typical Performance Characteristics (continued)

$T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ Unless Otherwise Specified

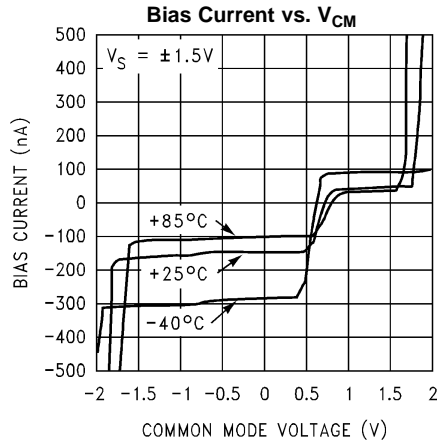


Figure 10.

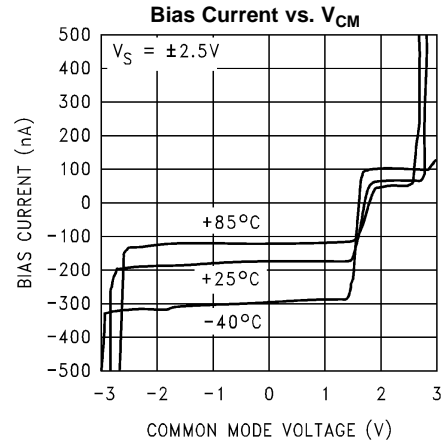


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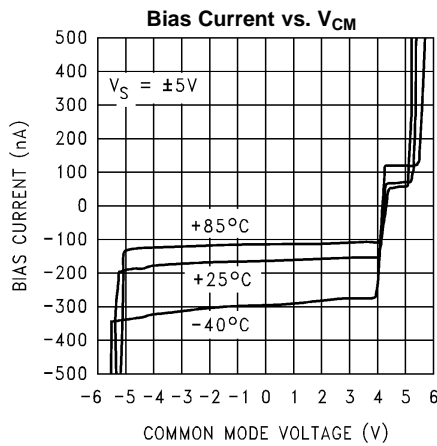


Figure 12.

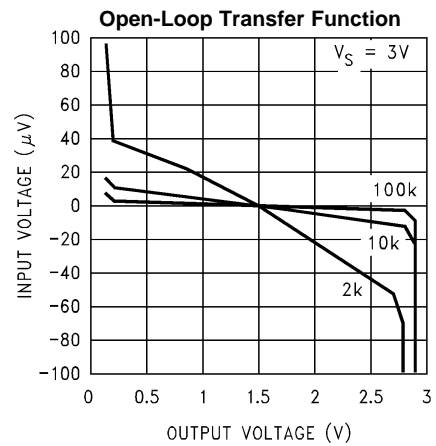


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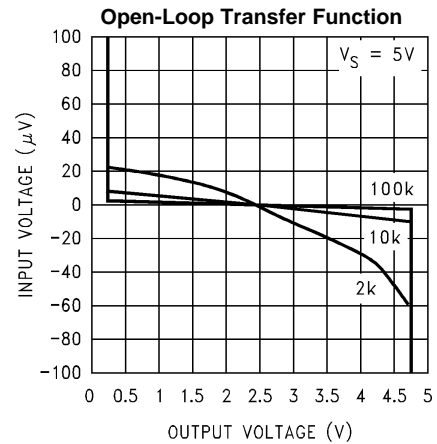


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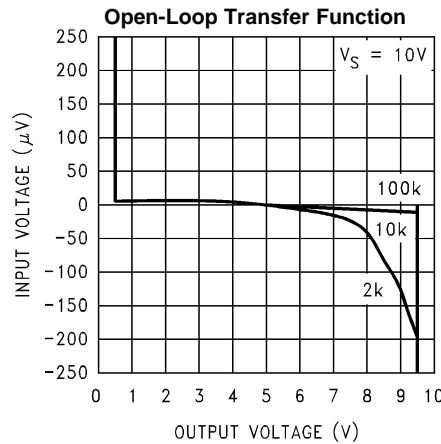


Figure 15.

Typical Performance Characteristics (continued)

T_A = 25°C, R_L = 10 kΩ Unless Otherwise Specified

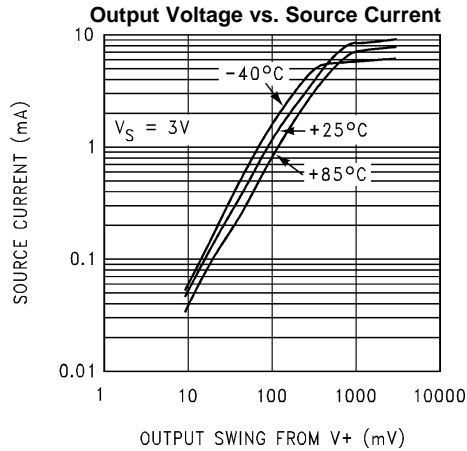


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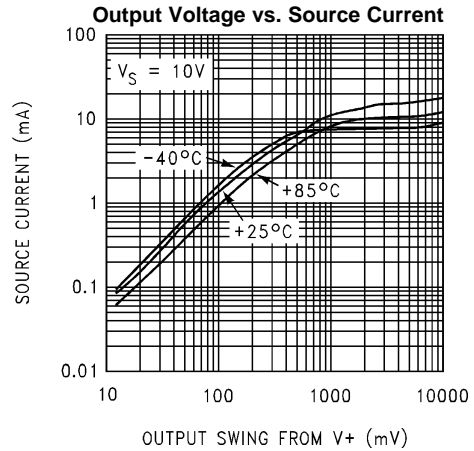


Figure 17.

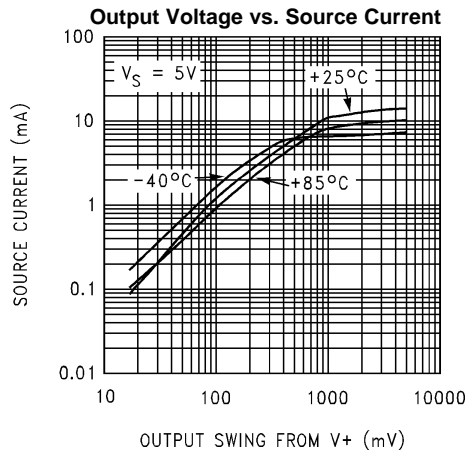


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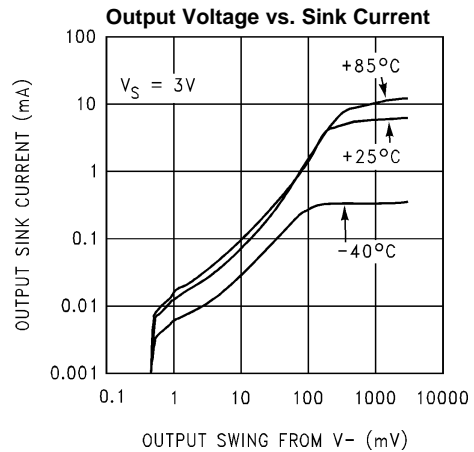


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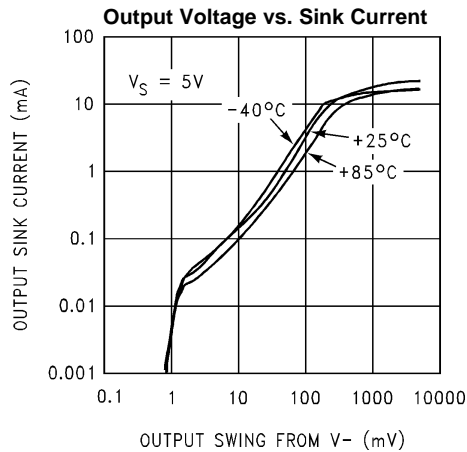


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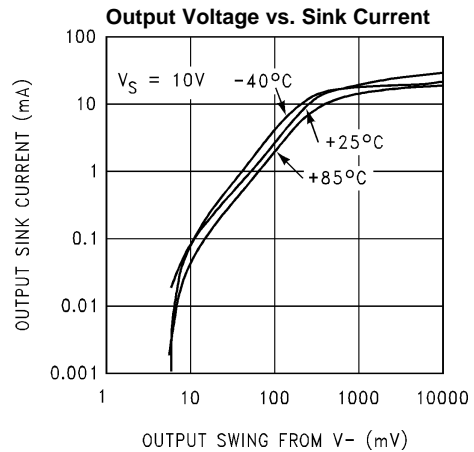


Figure 21.

Typical Performance Characteristics (continued)

$T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ Unless Otherwise Specified

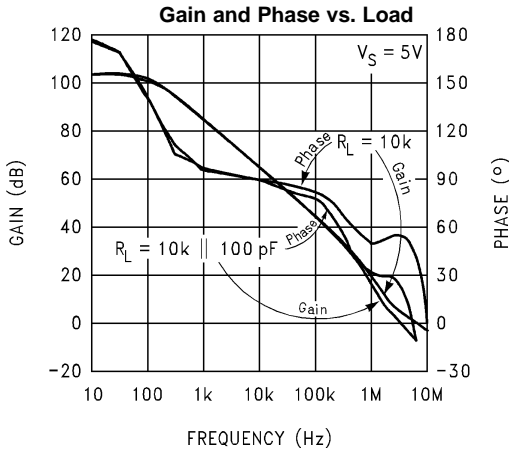


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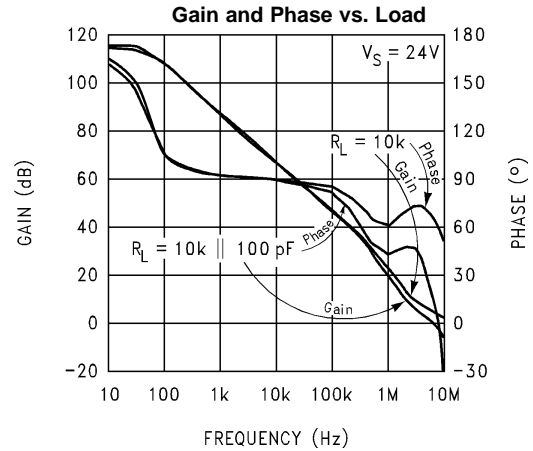


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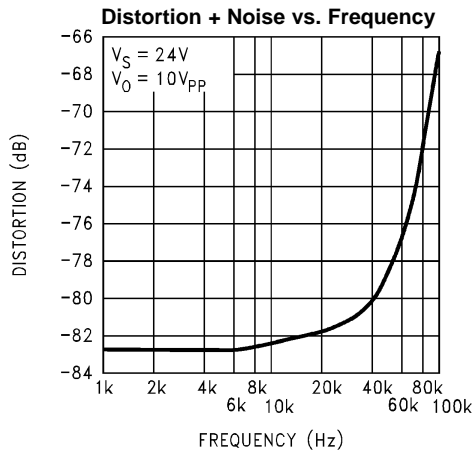


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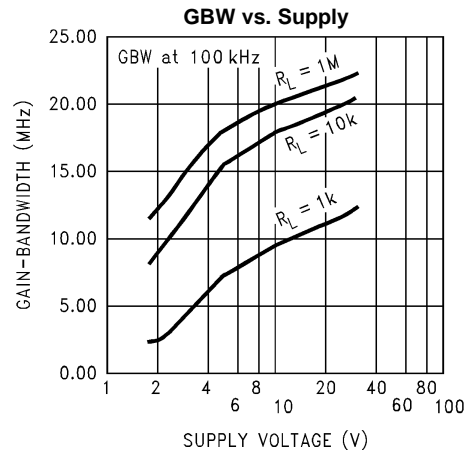


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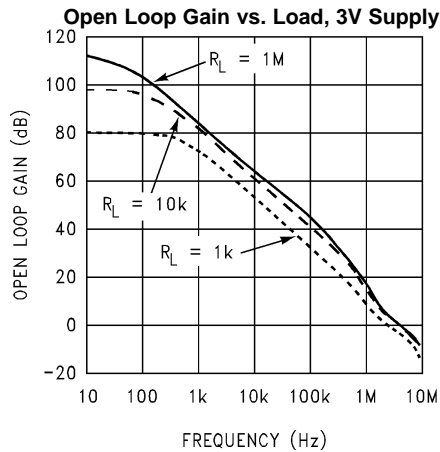


Figure 26.

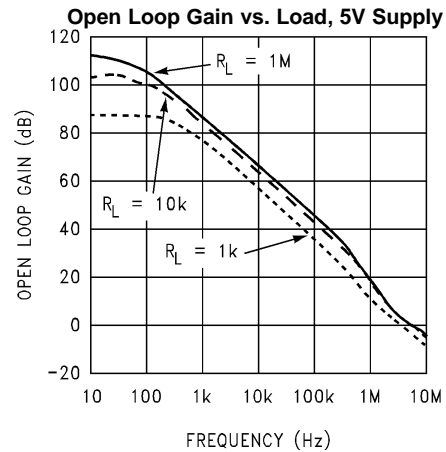


Figure 27.

Typical Performance Characteristics (continued)

T_A = 25°C, R_L = 10 kΩ Unless Otherwise Specified

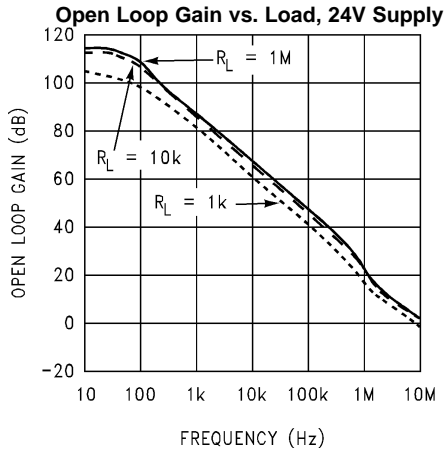


Figure 28.

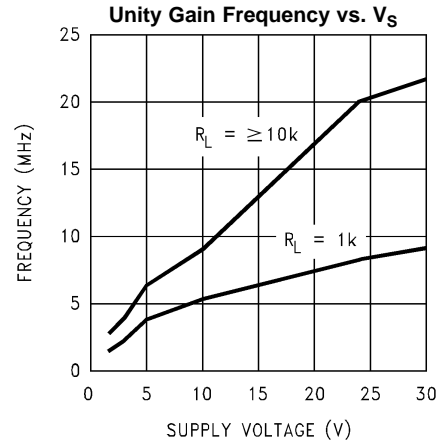


Figure 29.

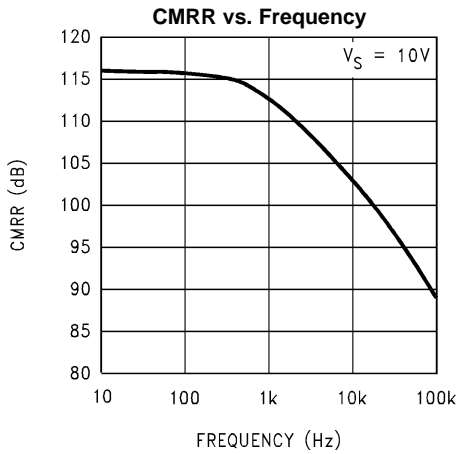


Figure 30.

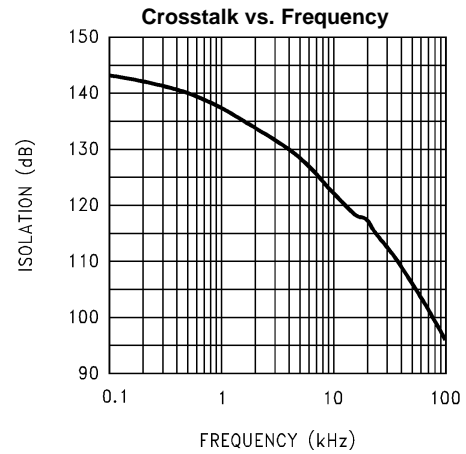


Figure 31.

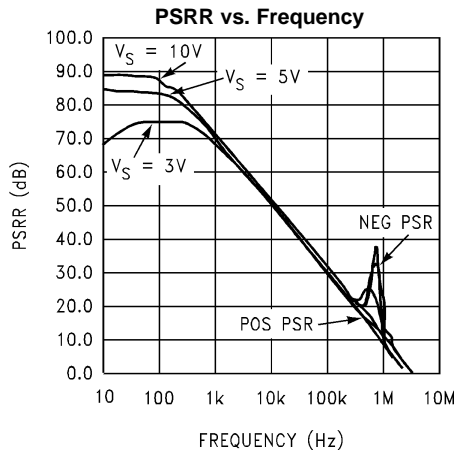


Figure 32.

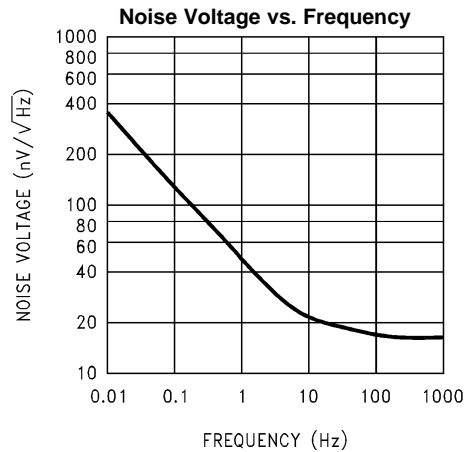
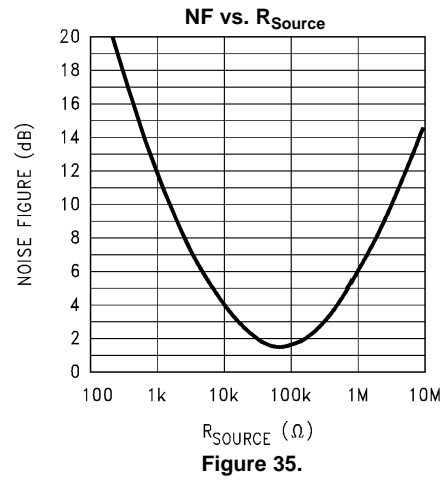
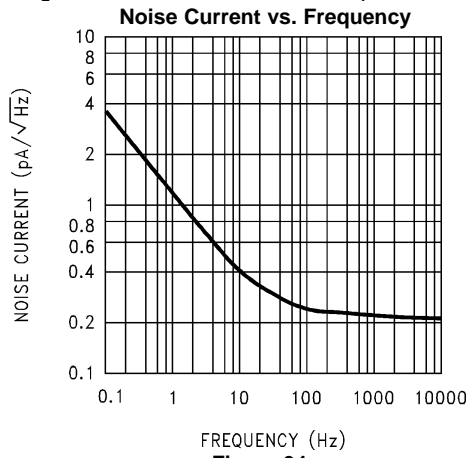


Figure 33.

Typical Performance Characteristics (continued)

$T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ Unless Otherwise Specified



LM6142/LM6144 APPLICATION IDEAS

The LM6142 brings a new level of ease of use to op amp system design.

With greater than rail-to-rail input voltage range concern over exceeding the common-mode voltage range is eliminated.

Rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The high gain-bandwidth with low supply current opens new battery powered applications, where high power consumption, previously reduced battery life to unacceptable levels.

To take advantage of these features, some ideas should be kept in mind.

ENHANCED SLEW RATE

Unlike most bipolar op amps, the unique phase reversal prevention/speed-up circuit in the input stage causes the slew rate to be very much a function of the input signal amplitude.

Figure 36 shows how excess input signal, is routed around the input collector-base junctions, directly to the current mirrors.

The LM6142/LM6144 input stage converts the input voltage change to a current change. This current change drives the current mirrors through the collectors of Q1–Q2, Q3–Q4 when the input levels are normal.

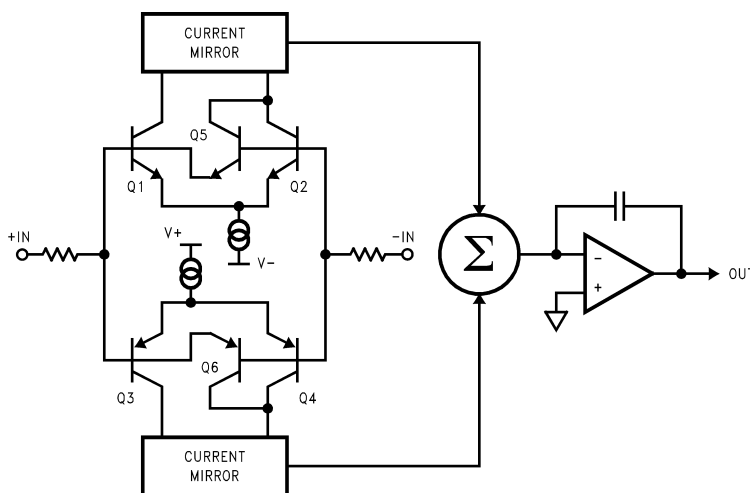


Figure 36.

If the input signal exceeds the slew rate of the input stage, the differential input voltage rises above two diode drops. This excess signal bypasses the normal input transistors, (Q1–Q4), and is routed in correct phase through the two additional transistors, (Q5, Q6), directly into the current mirrors.

This rerouting of excess signal allows the slew-rate to increase by a factor of 10 to 1 or more. (See Figure 37.)

As the overdrive increases, the op amp reacts better than a conventional op amp. Large fast pulses will raise the slew- rate to around 30V to 60V/μs.

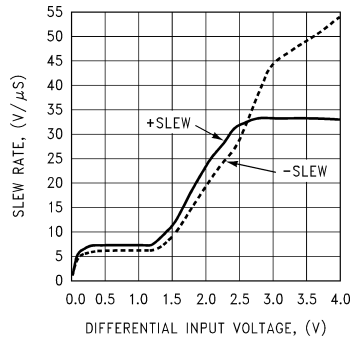


Figure 37. Slew Rate vs. ΔV_{IN}
 $V_S = \pm 5V$

This effect is most noticeable at higher supply voltages and lower gains where incoming signals are likely to be large.

This new input circuit also eliminates the phase reversal seen in many op amps when they are overdriven.

This speed-up action adds stability to the system when driving large capacitive loads.

DRIVING CAPACITIVE LOADS

Capacitive loads decrease the phase margin of all op amps. This is caused by the output resistance of the amplifier and the load capacitance forming an R-C phase lag network. This can lead to overshoot, ringing and oscillation. Slew rate limiting can also cause additional lag. Most op amps with a fixed maximum slew-rate will lag further and further behind when driving capacitive loads even though the differential input voltage raises. With the LM6142, the lag causes the slew rate to raise. The increased slew-rate keeps the output following the input much better. This effectively reduces phase lag. After the output has caught up with the input, the differential input voltage drops down and the amplifier settles rapidly.

These features allow the LM6142 to drive capacitive loads as large as 1000pF at unity gain and not oscillate. The scope photos (Figure 38 and Figure 39) above show the LM6142 driving a 1000pF load. In Figure 38, the upper trace is with no capacitive load and the lower trace is with a 1000pF load. Here we are operating on $\pm 12V$ supplies with a 20 V_{PP} pulse. Excellent response is obtained with a C_f of 10pF. In Figure 39, the supplies have been reduced to $\pm 2.5V$, the pulse is 4 V_{PP} and C_f is 39pF. The best value for the compensation capacitor is best established after the board layout is finished because the value is dependent on board stray capacity, the value of the feedback resistor, the closed loop gain and, to some extent, the supply voltage.

Another effect that is common to all op amps is the phase shift caused by the feedback resistor and the input capacitance. This phase shift also reduces phase margin. This effect is taken care of at the same time as the effect of the capacitive load when the capacitor is placed across the feedback resistor.

The circuit shown in Figure 40 was used for these scope photos.

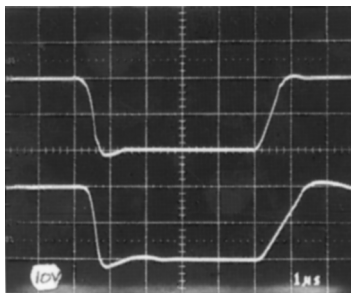


Figure 38.

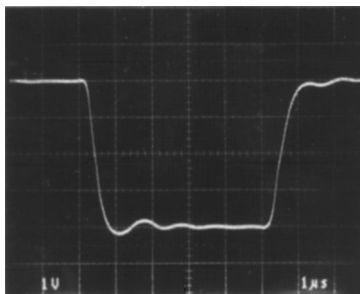


Figure 39.

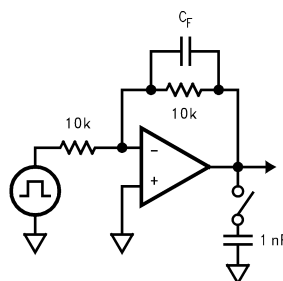


Figure 40.

Typical Applications

FISH FINDER/ DEPTH SOUNDER.

The LM6142/LM6144 is an excellent choice for battery operated fish finders. The low supply current, high gain-bandwidth and full rail to rail output swing of the LM6142 provides an ideal combination for use in this and similar applications.

ANALOG TO DIGITAL CONVERTER BUFFER

The high capacitive load driving ability, rail-to-rail input and output range with the excellent CMR of 82 dB, make the LM6142/LM6144 a good choice for buffering the inputs of A to D converters.

3 OP AMP INSTRUMENTATION AMP WITH RAIL-TO-RAIL INPUT AND OUTPUT

Using the LM6144, a 3 op amp instrumentation amplifier with rail-to-rail inputs and rail to rail output can be made. These features make these instrumentation amplifiers ideal for single supply systems.

Some manufacturers use a precision voltage divider array of 5 resistors to divide the common-mode voltage to get an input range of rail-to-rail or greater. The problem with this method is that it also divides the signal, so to even get unity gain, the amplifier must be run at high closed loop gains. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMR as well. Using the LM6144, all of these problems are eliminated.

In this example, amplifiers A and B act as buffers to the differential stage (Figure 41). These buffers assure that the input impedance is over 100MΩ and they eliminate the requirement for precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMR set by the matching of R1–R2 with R3–R4.

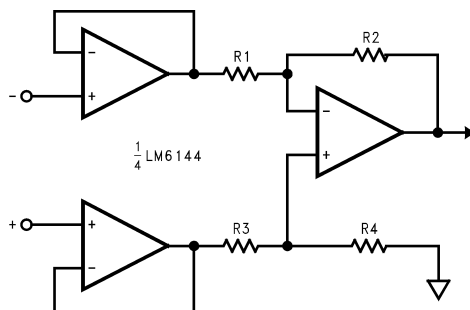


Figure 41.

The gain is set by the ratio of $R2/R1$ and $R3$ should equal $R1$ and $R4$ equal $R2$. Making $R4$ slightly smaller than $R2$ and adding a trim pot equal to twice the difference between $R2$ and $R4$ will allow the CMR to be adjusted for optimum.

With both rail to rail input and output ranges, the inputs and outputs are only limited by the supply voltages. Remember that even with rail-to-rail output, the output can not swing past the supplies so the combined common mode voltage plus the signal should not be greater than the supplies or limiting will occur.

SPICE MACROMODEL

A SPICE macromodel of this and many other Texas Instruments op amps is available http://www.ti.com/ww/en/analog/webench/index.shtml?DCMP=hpa_sva_webench&HQS=webench-bb.

REVISION HISTORY

| Changes from Revision C (March 2013) to Revision D | Page |
|--|--------------------------|
| <hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format | <hr/> 16 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LM6142AIM | NRND | SOIC | D | 8 | 95 | TBD | Call TI | Call TI | -40 to 85 | LM614 2AIM | |
| LM6142AIM/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LM614 2AIM | Samples |
| LM6142AIMX | NRND | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | -40 to 85 | LM614 2AIM | |
| LM6142AIMX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LM614 2AIM | Samples |
| LM6142BIM | NRND | SOIC | D | 8 | 95 | TBD | Call TI | Call TI | -40 to 85 | LM614 2BIM | |
| LM6142BIM/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LM614 2BIM | Samples |
| LM6142BIMX | NRND | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | -40 to 85 | LM614 2BIM | |
| LM6142BIMX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LM614 2BIM | Samples |
| LM6142BIN/NOPB | ACTIVE | PDIP | P | 8 | 40 | Green (RoHS & no Sb/Br) | CU SN | Level-1-NA-UNLIM | -40 to 85 | LM6142 BIN | Samples |
| LM6144AIM | NRND | SOIC | D | 14 | 55 | TBD | Call TI | Call TI | -40 to 85 | LM6144 AIM | |
| LM6144AIM/NOPB | ACTIVE | SOIC | D | 14 | 55 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LM6144 AIM | Samples |
| LM6144AIMX/NOPB | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LM6144 AIM | Samples |
| LM6144BIM | NRND | SOIC | D | 14 | 55 | TBD | Call TI | Call TI | -40 to 85 | LM6144 BIM | |
| LM6144BIM/NOPB | ACTIVE | SOIC | D | 14 | 55 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LM6144 BIM | Samples |
| LM6144BIMX | NRND | SOIC | D | 14 | 2500 | TBD | Call TI | Call TI | -40 to 85 | LM6144 BIM | |
| LM6144BIMX/NOPB | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LM6144 BIM | Samples |
| LM6144BIN/NOPB | ACTIVE | PDIP | NFF | 14 | 25 | Green (RoHS & no Sb/Br) | CU SN | Level-1-NA-UNLIM | -40 to 85 | LM6144BIN | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM6142AIMX | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LM6142AIMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LM6142BIMX | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LM6142BIMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LM6144AIMX/NOPB | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |
| LM6144BIMX | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |
| LM6144BIMX/NOPB | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM6142AIMX | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LM6142AIMX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LM6142BIMX | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LM6142BIMX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LM6144AIMX/NOPB | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 35.0 |
| LM6144BIMX | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 35.0 |
| LM6144BIMX/NOPB | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 35.0 |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

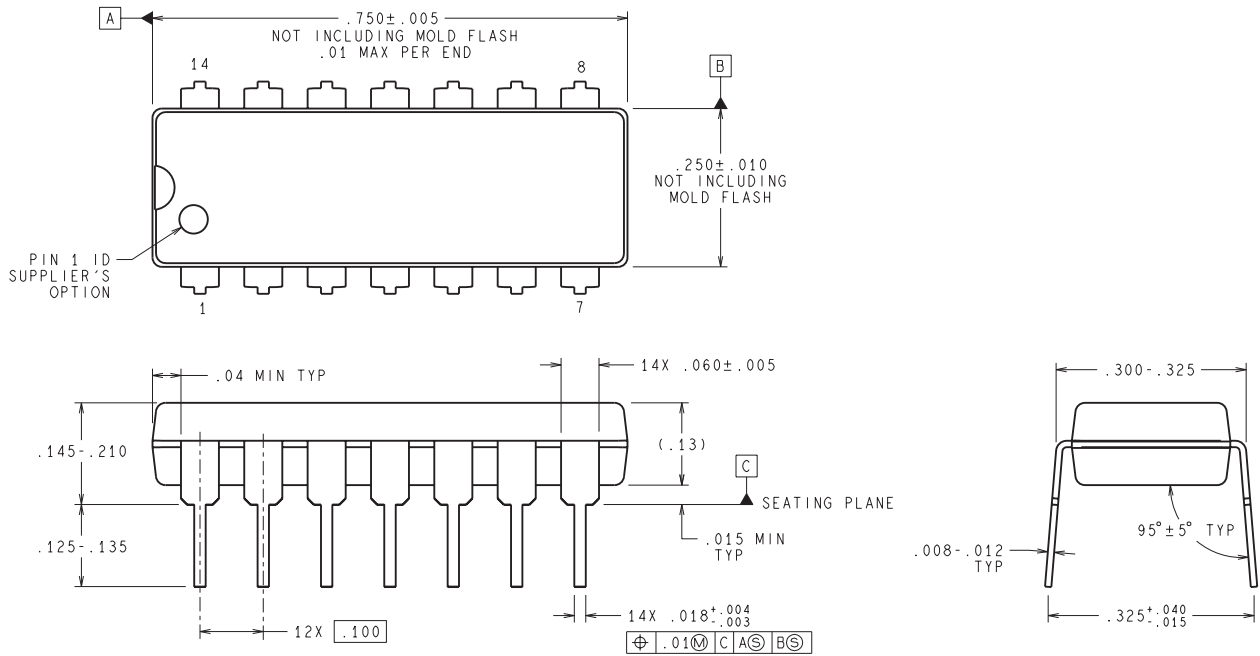
P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

N0014A



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DIMENSIONS IN () FOR REFERENCE ONLY

N14A (Rev G)

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