WINSOURCE ELECTRONICS

THE DATASHEET OF

LM5110-1SD/NOPB

LM5110 Dual 5-A Compound Gate Driver With Negative Output Voltage Capability

1 Features

- Independently Drives Two N-Channel MOSFETs
- Compound CMOS and Bipolar Outputs Reduce Output Current Variation
- 5A sink/3A Source Current Capability
- Two Channels can be Connected in Parallel to Double the Drive Current
- Independent Inputs (TTL Compatible)
- Fast Propagation Times (25-ns Typical)
- Fast Rise and Fall Times (14-ns/12-ns Rise/Fall With 2-nF Load)
- Dedicated Input Ground Pin (IN_REF) for Split Supply or Single Supply Operation
- Outputs Swing from V_{CC} to V_{EE} Which Can Be Negative Relative to Input Ground
- Available in Dual Noninverting, Dual Inverting and Combination Configurations
- Shutdown Input Provides Low Power Mode
- Supply Rail Undervoltage Lockout Protection
- Pin-Out Compatible With Industry Standard Gate Drivers
- Packages:
  - SOIC-8
  - WSON-10 (4 mm × 4 mm)

2 Applications

- Synchronous Rectifier Gate Drivers
- Switch-Mode Power Supply Gate Driver
- Solenoid and Motor Drivers

3 Description

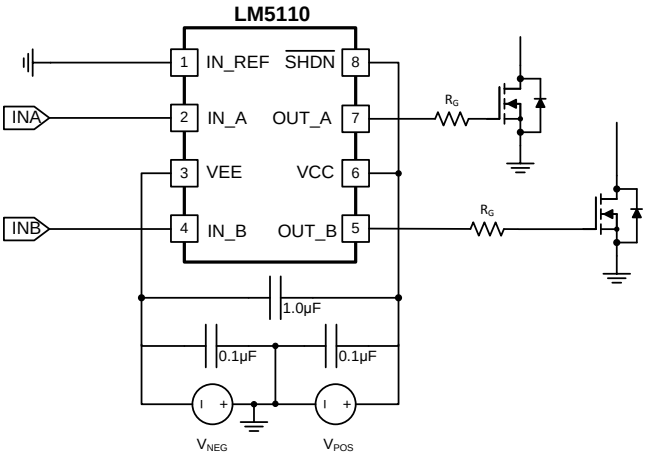
The LM5110 Dual Gate Driver replaces industry standard gate drivers with improved peak output current and efficiency. Each “compound” output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 5A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Separate input and output ground pins provide Negative Drive Capability allowing the user to drive MOSFET gates with positive and negative VGS voltages. The gate driver control inputs are referenced to a dedicated input ground (IN_REF). The gate driver outputs swing from V_{CC} to the output ground V_{EE} which can be negative with respect to IN_REF. Undervoltage lockout protection and a shutdown input pin are also provided. The drivers can be operated in parallel with inputs and outputs connected to double the drive current capability. This device is available in the SOIC-8 and the thermally-enhanced WSON-10 packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5110	SOIC (8)	4.90 mm × 3.91 mm
	WSON (10)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2012) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added *Thermal Information* table.	4

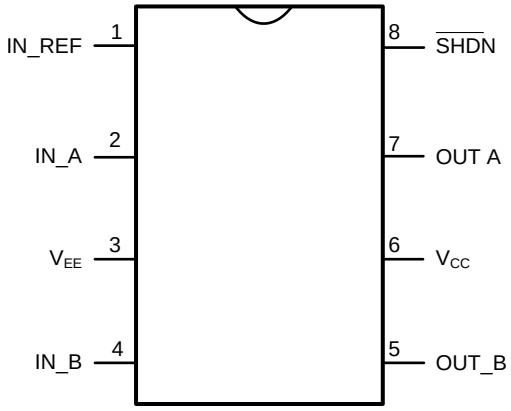
5 Device Options

Table 1. Configuration Table

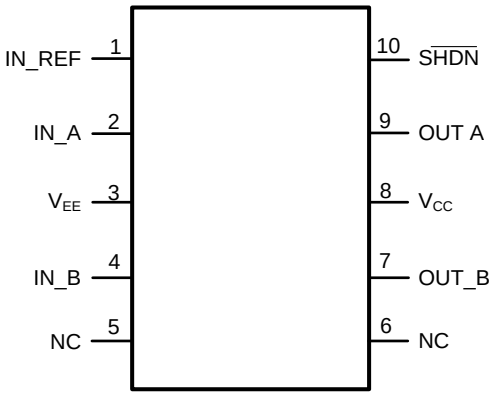
PART NUMBER	"A" OUTPUT CONFIGURATION	"B" OUTPUT CONFIGURATION	PACKAGE
LM5110-1M	Noninverting	Noninverting	SOIC- 8
LM5110-2M	Inverting	Inverting	SOIC- 8
LM5110-3M	Inverting	Noninverting	SOIC- 8
LM5110-1SD	Noninverting	Noninverting	WSON-10
LM5110-2SD	Inverting	Inverting	WSON-10
LM5110-3SD	Inverting	Noninverting	WSON-10

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



DPR Package
10-Pin WSON
Top Pin



Pin Functions

PIN			I/O(1)	DESCRIPTION	APPLICATION INFORMATION
SOIC	WSON(2)	NAME			
1	1	IN_REF	G	Ground reference for control inputs	Connect to V_{EE} for standard positive only output voltage swing. Connect to system logic ground reference for positive and negative output voltage swing.
2	2	IN_A	I	'A' side control input	TTL compatible thresholds.
3	3	V_{EE}	G	Power ground of the driver outputs	Connect to either power ground or a negative gate drive supply.
4	4	IN_B	I	'B' side control input	TTL compatible thresholds.
5	7	OUT_B	O	Output for the 'B' side driver.	Capable of sourcing 3A and sinking 5A. Voltage swing of this output is from V_{CC} to V_{EE}.
6	8	V_{CC}	P	Positive supply	Locally decouple to V_{EE} and IN_REF.
7	9	OUT_A.	O	Output for the 'A' side driver.	Capable of sourcing 3A and sinking 5A. Voltage swing of this output is from V_{CC} to V_{EE} .
8	10	nSHDN	I	Shutdown input pin	Pull below 1.5V to activate low power shutdown mode.

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output.
(2) Pins 5 and 6 are No Connect for WSON-10 packages.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
V_{CC} to V_{EE}	−0.3	15	V
V_{CC} to IN_REF	−0.3	15	V
IN to IN_REF, nSHDN to IN_REF	−0.3	15	V
IN_REF to V_{EE}	−0.3	5	V
Maximum junction temperature, (T_J(max))		150	°C
Operating junction temperature		125	°C
Storage temperature, (T_{stg})	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{CC} to V_{EE}	3.5	-	14	V
V_{CC} to IN_REF	3.5	-	14	V
IN_REF to V_{EE}	0		4	V
Junction Temperature	-40		126	°C

7.4 Thermal Information

THERMAL METRIC(1)		LM5110		UNIT
		D (SOIC)	DPR (WSON)	
		8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114	40.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.6	40.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.2	17.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.3	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.6	17.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	6.3	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

T_J = −40°C to +125°C, V_{CC} = 12V, V_{EE} = IN_REF = 0V, nSHDN = V_{CC}, No Load on OUT_A or OUT_B, unless otherwise specified.

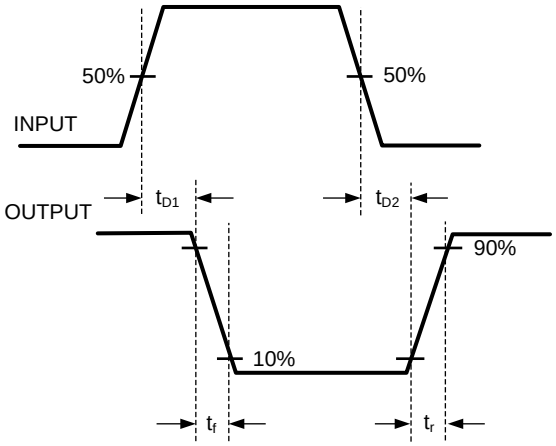
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	V_{CC} Operating Range	V_{CC}−IN_REF and V_{CC}−V_{EE}	3.5		14	V
V_{CCR}	V_{CC} Under Voltage Lockout (rising)	V_{CC}−IN_REF	2.3	2.9	3.5	V
V_{CCH}	V_{CC} Under Voltage Lockout Hysteresis			230		mV
I_{CC}	V_{CC} Supply Current (I_{CC})	IN_A = IN_B = 0 V (5110-1)		1	2	mA
		IN_A = IN_B = V_{CC} (5110-2)		1	2	
		IN_A = V_{CC}, IN_B = 0 V (5110-3)		1	2	
I_{CCSD}	V_{CC} Shutdown Current (I_{CC})	nSHDN = 0 V		18	25	µA
CONTROL INPUTS						
V_{IH}	Logic High		2.2			V
V_{IL}	Logic Low				0.8	V
HYS	Input Hysteresis			400		mV
I_{IL}	Input Current Low	IN_A=IN_B=V_{CC} (5110-1-2-3)	−1	0.1	1	µA
I_{IH}	Input Current High	IN_A=IN_B=V_{CC} (5110-1)	10	18	25	
		IN_A=IN_B=V_{CC} (5110-2)	−1	0.1	1	
		IN_A=V_{CC} (5110-3)	–1	0.1	1	
		IN_B=V_{CC} (5110-3)	10	18	25	
SHUTDOWN INPUT						
ISD	Pullup Current	nSHDN = 0 V		−18	−25	µA
VSDR	Shutdown Threshold	nSHDN rising	0.8	1.5	2.2	V
VSDH	Shutdown Hysteresis			165		mV
OUTPUT DRIVERS						
R_{OH}	Output Resistance High	I_{OUT} = −10 mA (1)		30	50	Ω
R_{OL}	Output Resistance Low	I_{OUT} = + 10 mA (1)		1.4	2.5	Ω
I_{Source}	Peak Source Current	OUTA/OUTB = V_{CC}/2, 200 ns Pulsed Current		3		A
I_{Sink}	Peak Sink Current	OUTA/OUTB = V_{CC}/2, 200 ns Pulsed Current		5		A
LATCHUP PROTECTION						
	AEC - Q100, Method 004	T_J = 150°C		500		mA

(1) The output resistance specification applies to the MOS device only. The total output current capability is the sum of the MOS and Bipolar devices.

7.6 Switching Characteristics

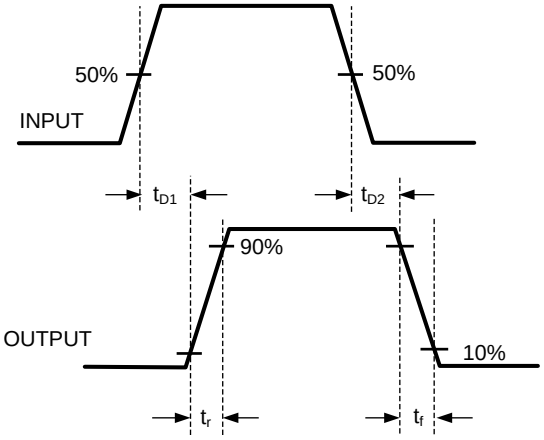
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
td1	Propagation Delay Time Low to High, IN rising (IN to OUT)	C_{LOAD} = 2 nF, see Figure 2		25	40	ns
td2	Propagation Delay Time High to Low, IN falling (IN to OUT)	C_{LOAD} = 2 nF, see Figure 2		25	40	ns
t_r	Rise Time	C_{LOAD} = 2 nF, see Figure 2		14	25	ns
t_f	Fall Time	C_{LOAD} = 2 nF, see Figure 2		12	25	ns



(a)

Figure 1. Inverting



(b)

Figure 2. Noninverting

7.7 Typical Characteristics

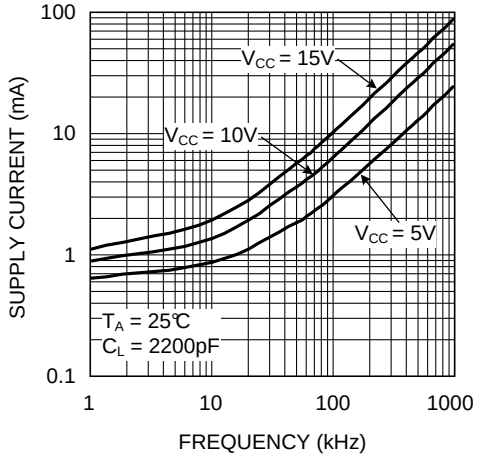


Figure 3. Supply Current vs Frequency

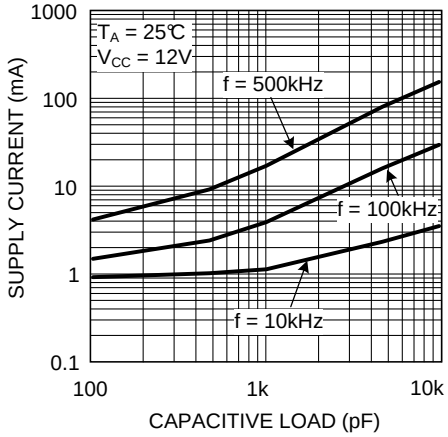


Figure 4. Supply Current vs Load

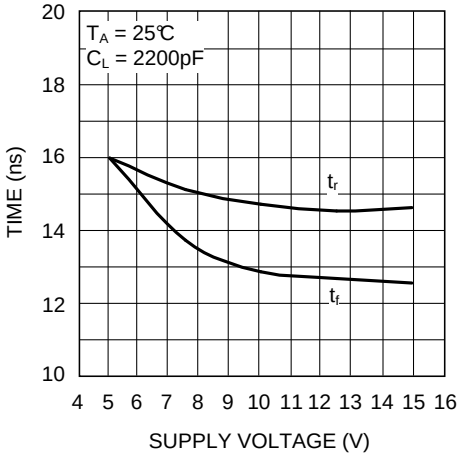


Figure 5. Rise and Fall Time vs Supply Voltage

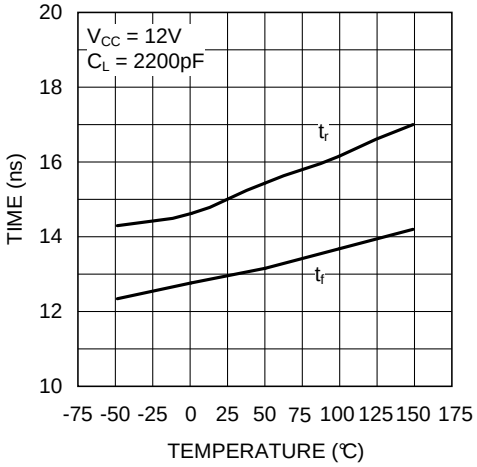


Figure 6. Rise and Fall Time vs Temperature

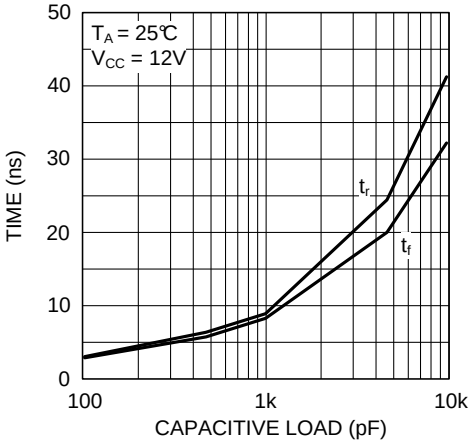


Figure 7. Rise and Fall Time vs Capacitive Load

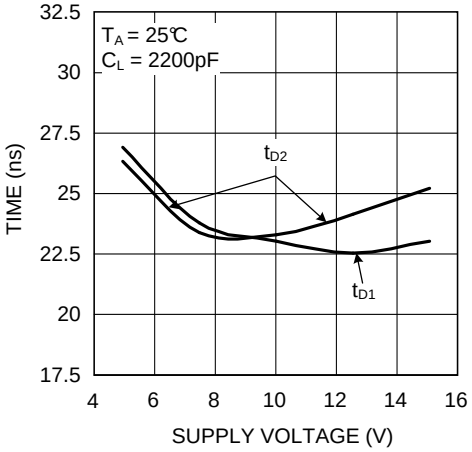


Figure 8. Delay Time vs Supply Voltage

Typical Characteristics (continued)

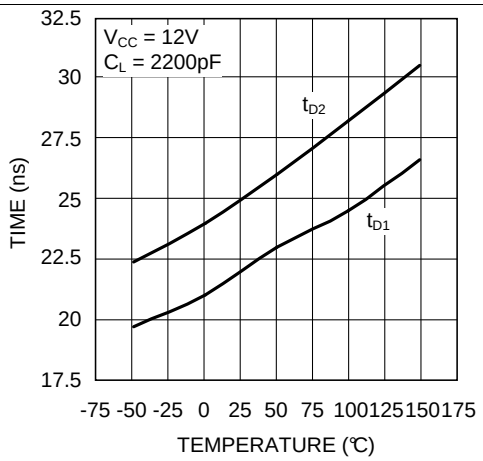


Figure 9. Delay Time vs Temperature

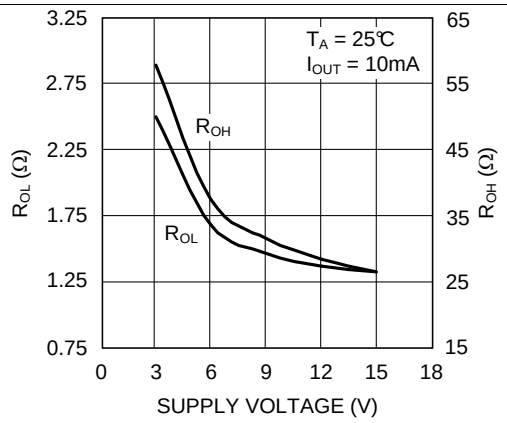


Figure 10. R_{DSON} vs Supply Voltage

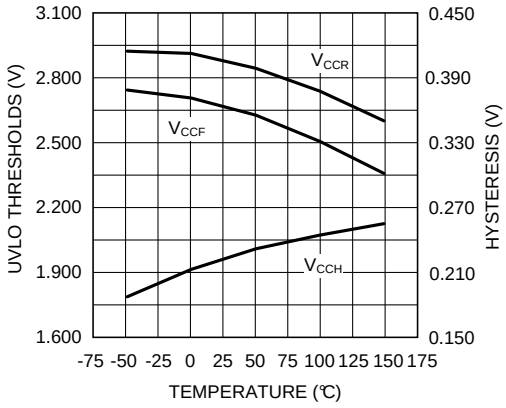


Figure 11. UVLO Thresholds and Hysteresis vs Temperature

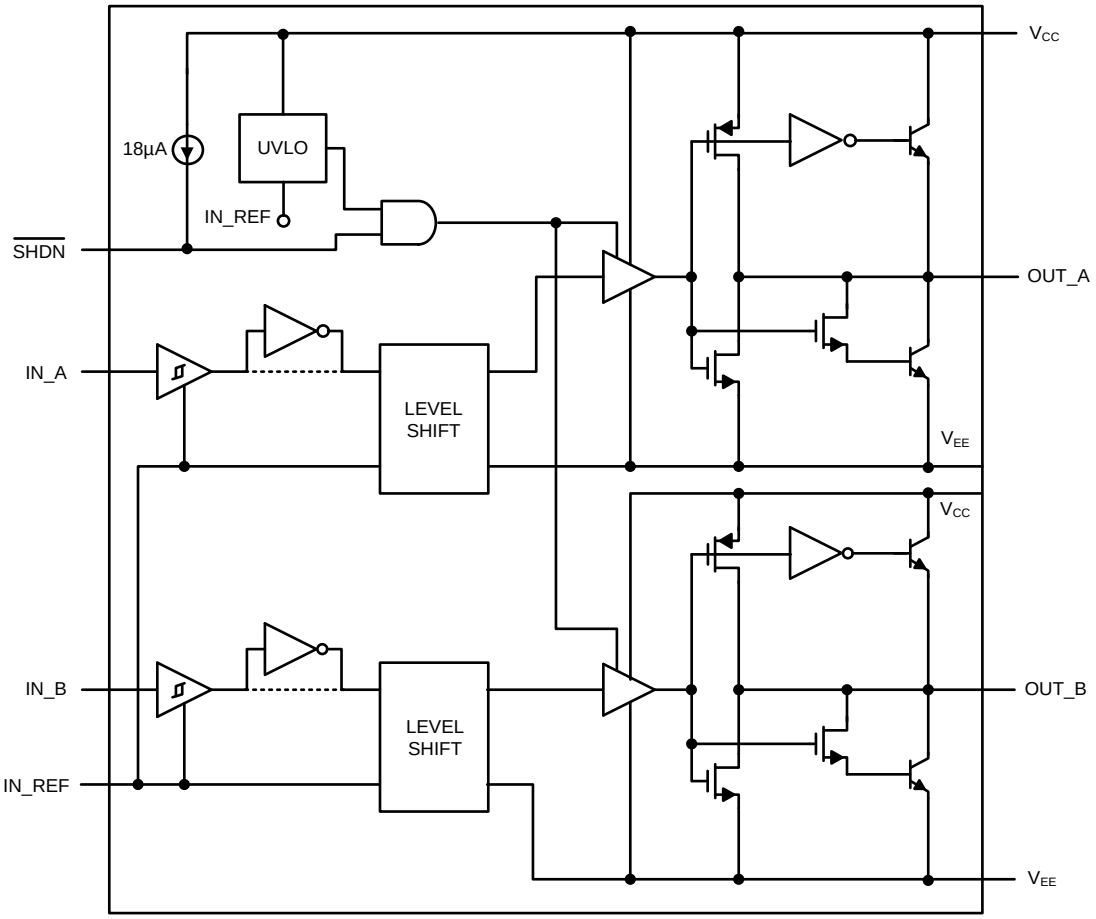
8 Detailed Description

8.1 Overview

LM5110 dual gate driver consists of two independent and identical driver channels with TTL compatible logic inputs and high current totem-pole outputs that source or sink current to drive MOSFET gates. The driver output consist of a compound structure with MOS and bipolar transistor operating in parallel to optimize current capability over a wide output voltage and operating temperature range. The bipolar device provides high peak current at the critical threshold region of the MOSFET VGS while the MOS devices provide rail-to-rail output swing. The totem pole output drives the MOSFET gate between the gate drive supply voltage V_{CC} and the power ground potential at the V_{EE} pin.

The LM5110 is available in dual noninverting (-1), dual inverting (-2) and the combination inverting plus noninverting (-3) configurations. All three configurations are offered in the SOIC-8 and WSON-10 plastic packages.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Stage and Level Shifter

The control inputs of the drivers are high impedance CMOS buffers with TTL compatible threshold voltages. The negative supply of the input buffer is connected to the input ground pin IN_REF. An internal level shifting circuit connects the logic input buffers to the totem pole output drivers. The level shift circuit and separate input/output ground pins provide the option of single supply or split supply configurations. When driving MOSFET gates from a single positive supply, the IN_REF and V_{EE} pins are both connected to the power ground. The LM5110 pinout was designed for compatibility with industry standard gate drivers in single supply gate driver applications. Pin 1 (IN_REF) on the LM5110 is a no-connect on standard driver IC's. Connecting pin 1 to pin 3 (V_{EE}) on the printed-circuit board accommodates the pin-out of both the LM5110 and competitive drivers.

The input stage of each driver should be driven by a signal with a short rise and fall time. Slow rising and falling input signals, although not harmful to the driver, may result in the output switching repeatedly at a high frequency.

The input pins of noninverting drivers have an internal 18-μA current source pull-down to IN-REF. The input pins of inverting driver channels have neither pullup nor pulldown current sources. Unused input should be tied to IN_REF or VCC and not left open.

8.3.2 Output Stage

The two driver channels of the LM5110 are designed as identical cells. Transistor matching inherent to integrated circuit manufacturing ensures that the AC and DC performance of the channels are nearly identical. Closely matched propagation delays allow the dual driver to be operated as a single driver if inputs and output pins are connected. The drive current capability in parallel operation is 2X the drive of either channel. Small differences in switching speed between the driver channels will produce a transient current (shoot-through) in the output stage when two output pins are connected to drive a single load. Differences in input thresholds between the driver channels will also produce a transient current (shoot-through) in the output stage. Fast transition input signals are especially important while operating in a parallel configuration. The efficiency loss for parallel operation has been characterized at various loads, supply voltages and operating frequencies. The power dissipation in the LM5110 increases by less than 1% relative to the dual driver configuration when operated as a single driver with inputs and outputs connected.

8.3.3 Turn-off with Negative Bias

The isolated input/output grounds provide the capability to drive the MOSFET to a negative VGS voltage for a more robust and reliable off state. In split supply configuration, the IN_REF pin is connected to the ground of the controller which drives the LM5110 inputs. The V_{EE} pin is connected to a negative bias supply that can range from the IN-REF as much as 14-V below the V_{CC} gate drive supply.

Enhancement mode MOSFETs do not inherently require a negative bias on the gate to turn off the FET. However, certain applications may benefit from the capability of negative VGS voltage during turnoff including:

1. When the gate voltages cannot be held safely below the threshold voltage due to transients or coupling in the printed-circuit-board.
2. When driving low threshold MOSFETs at high junction temperatures.
3. When high switching speeds produce capacitive gate-drain current that lifts the internal gate potential of the MOSFET.

8.3.4 UVLO and Power Supplies

An undervoltage lockout (UVLO) circuit is included in the LM5110, which senses the voltage difference between V_{CC} and the input ground pin, IN_REF. When the V_{CC} to IN_REF voltage difference falls below 2.7 V, both driver channels are disabled. The driver will resume normal operation when the V_{CC} to IN_REF differential voltage exceeds approximately 2.9 V. UVLO hysteresis prevents chattering during brown-out conditions.

The maximum recommended voltage difference between V_{CC} and IN_REF or between V_{CC} and V_{EE} is 14 V. The minimum voltage difference between V_{CC} and IN_REF is 3.5 V.

Feature Description (continued)

8.3.5 Shutdown $\overline{\text{SHDN}}$

The Shutdown pin ($\overline{\text{SHDN}}$) is a TTL compatible logic input provided to enable/disable both driver channels. When $\overline{\text{SHDN}}$ is in the logic low state, the LM5110 is switched to a low power standby mode with total supply current less than 25 µA. This function can be effectively used for start-up, thermal overload, or short circuit fault protection. TI recommends connecting this pin to V_{CC} when the shutdown function is not being used. The shutdown pin has an internal 18-µA current source pullup to V_{CC}.

8.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See Table 2 for more information on UVLO operation mode. In normal mode when the V_{CC} and $V_{IN–REF}$ are above UVLO threshold, the output stage is dependent on the states of the IN_A, IN_B and nSHDN pins. The output HO and LO will be low if input state is floating.

Table 2. INPUT/OUTPUT Logic Table

IN_A (1)	IN_B (1)	$\overline{\text{SHDN}}$	OUT_A (2)	OUT_B (2)
L	L	H or Left Open	L	L
L	H	H or Left Open	L	H
H	L	H or Left Open	H	L
H	H	H or Left Open	H	H
X	X	L	L	L

(1) IN_A and IN_B is referenced to IN_REF.
(2) OUT_A and OUT_B is referenced to VEE.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

To operate fast switching of power MOSFETs at high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3 V logic signal which cannot effectively turn on a power switch. Level shift circuit is needed to boost the 3.3 V signal to the gate-drive voltage (such as 12 V) in order to fully turn-on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise (by placing the high-current driver IC physically close to the power switch), driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

The LM5110 Dual Gate Driver replaces industry standard gate drivers with improved peak output current and efficiency. Each "compound" output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 5A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Separate input and output ground pins provide Negative Drive Capability allowing the user to drive MOSFET gates with positive and negative VGS voltages.

9.2 Typical Application

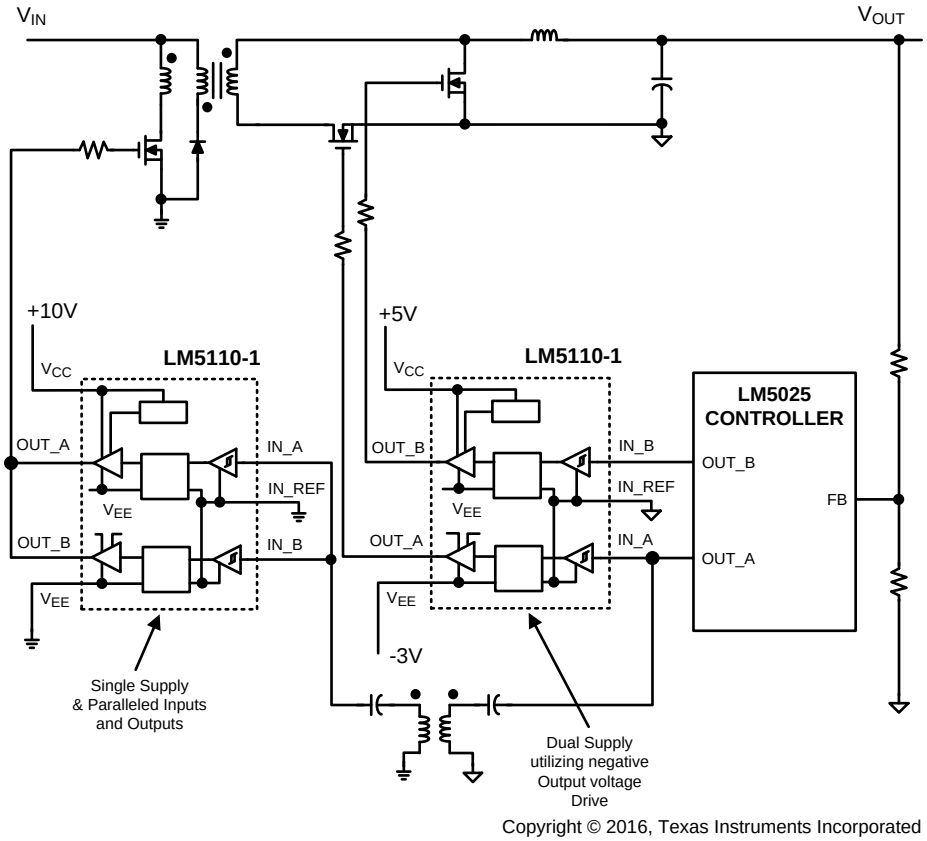


Figure 12. Simplified Power Converter Using Synchronous Rectifiers With Negative Off Gate Voltage

9.2.1 Design Requirements

To select proper device from LM5110 family, TI recommends first checking the appropriate logic for the outputs. LM5110-2 has dual inverting outputs; LM5110-1 has dual noninverting outputs; LM5110-3 have inverting channel A and noninverting channel B. Moreover, some design considerations must be evaluated first in order to make the most appropriate selection. Among these considerations are VCC, drive current, and power dissipation.

9.2.2 Detailed Design Procedure

9.2.2.1 Parallel Outputs

The A and B drivers may be combined into a single driver by connecting the INA/INB inputs together as close to the IC as possible, and the OUTA/OUTB outputs ties together if the external gate drive resistor is not used. In some cases where the external gate drive resistor is used, TI recommends that the resistor can be equally split in OUTA and OUTB respectively to reduce the parasitic inductance induce unbalance between two channels, as show in Figure 13.

Typical Application (continued)

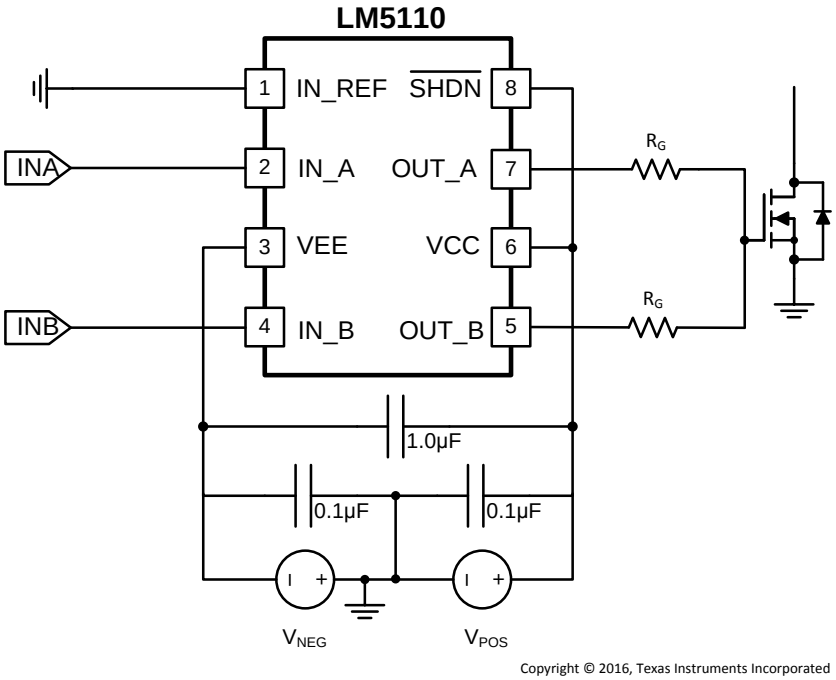


Figure 13. Parallel Operation of LM5110-1 and LM5110-2

Important consideration about paralleling two channels for LM5110 include: 1) IN_A and IN_B should be shorted in PCB layout as close to the device as possible, as well as for OUT_A and OUT_B, in which condition PCB layout parasitic mismatching between two channels could be minimized. 2) INA/B input slope signal should be fast enough to avoid mismatched V_{IH}/V_{IL}, t_{d1}/t_{d2} between channel-A and channel-B. TI recommends having input signal slope faster than 20 V/µs.

9.2.3 Application Curves

Figure 14 and Figure 15 shows the total operation current comsumption vs load and frequency.

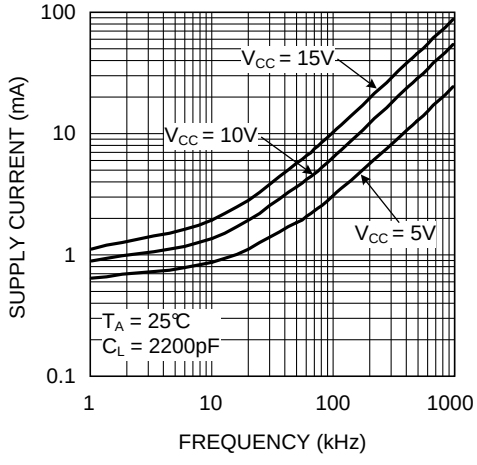


Figure 14. Operating Current vs Switching Frequency

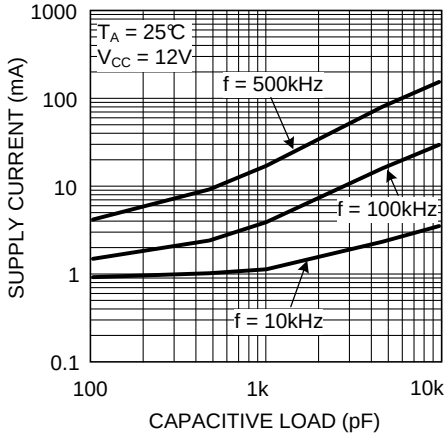


Figure 15. Operating Current vs Load Capacitance

10 Power Supply Recommendations

The recommended bias supply voltage range for LM5110 is from 3.5 V to 14 V. The upper end of this range is driven by the 15 V absolute maximum voltage rating of the VCC. TI recommends keeping proper margin to allow for transient voltage spikes.

A local bypass capacitor must be placed between the VCC and IN_REF pins, as well as between the VCC and VEE. This capacitor must be placed as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. TI recommends using 2 capacitors in parallel: a 100-nF ceramic surface-mount capacitor for high frequency filtering placed as close to VCC as possible, and another surface-mount capacitor, 220 nF to 10 µF, for IC bias requirements.

11 Layout

11.1 Layout Guidelines

Attention must be given to board layout when using LM5110. Some important considerations include:

1. A Low ESR/ESL capacitor must be connected close to the IC and between the V_{CC} and V_{EE} pins to support high peak currents being drawn from V_{CC} during turn-on of the MOSFET.
2. Proper grounding is crucial. The drivers need a very low impedance path for current return to ground avoiding inductive loops. The two paths for returning current to ground are a) between LM5110 IN-REF pin and the ground of the circuit that controls the driver inputs, b) between LM5110 V_{EE} pin and the source of the power MOSFET being driven. All these paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance. All these ground paths should be kept distinctly separate to avoid coupling between the high current output paths and the logic signals that drive the LM5110. A good method is to dedicate one copper plane in a multi-layered PCB to provide a common ground surface.
3. With the rise and fall times in the range of 10 ns to 30 ns, care is required to minimize the lengths of current carrying conductors to reduce their inductance and EMI from the high di/dt transients generated by the LM5110.
4. The LM5110 SOIC footprint is compatible with other industry standard drivers. Simply connect IN_REF pin of the LM5110 to V_{EE} (pin 1 to pin 3) to operate the LM5110 in a standard single supply configuration.
5. If either channel is not being used, the respective input pin (IN_A or IN_B) should be connected to either IN_REF or V_{CC} to avoid spurious output signals. If the shutdown feature is not used, the nSHDN pin should be connected to V_{CC} to avoid erratic behavior that would result if system noise were coupled into a floating 'nSHDN' pin.

11.2 Layout Example

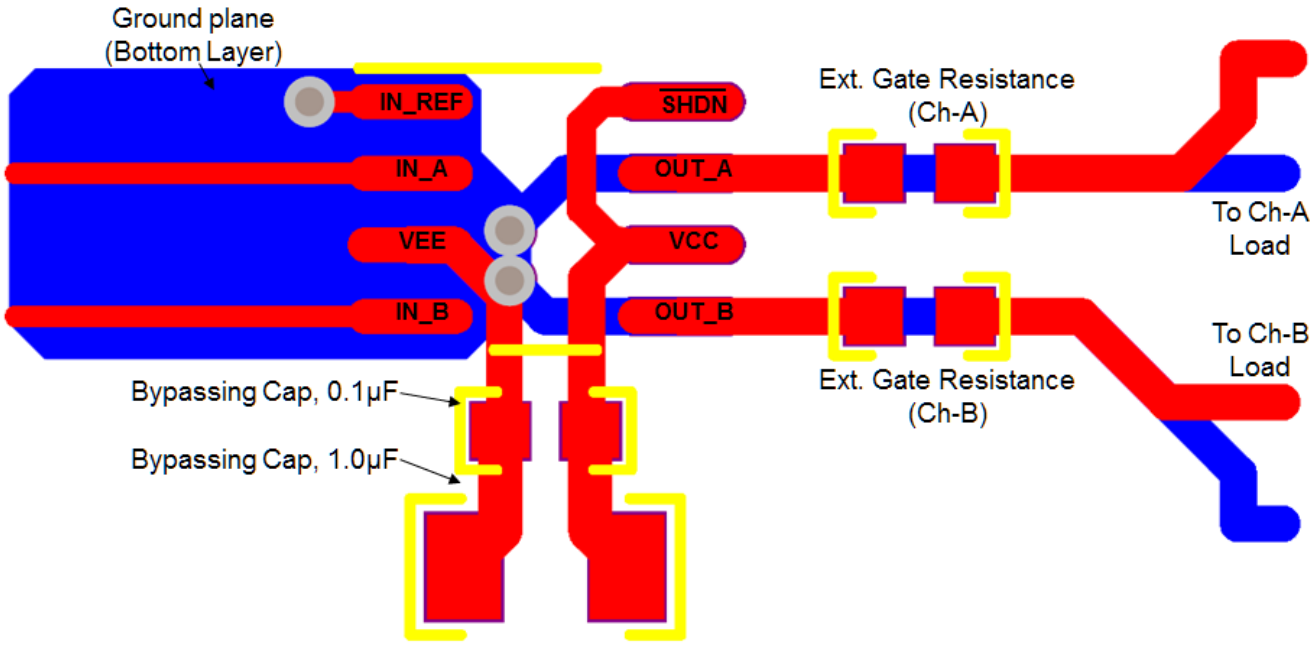


Figure 16. SOIC(8) Layout Example

11.3 Thermal Considerations

The primary goal of thermal management is to maintain the integrated circuit (IC) junction temperature (T_J) below a specified maximum operating temperature to ensure reliability. It is essential to estimate the maximum T_J of IC components in worst case operating conditions. The junction temperature is estimated based on the power dissipated in the IC and the junction to ambient thermal resistance θ_{JA} for the IC package in the application board and environment. The θ_{JA} is not a given constant for the package and depends on the printed circuit board design and the operating environment.

11.3.1 Drive Power Requirement Calculations in LM5110

The LM5110 dual low side MOSFET driver is capable of sourcing/sinking 3-A/5-A peak currents for short intervals to drive a MOSFET without exceeding package power dissipation limits. High peak currents are required to switch the MOSFET gate very quickly for operation at high frequencies.

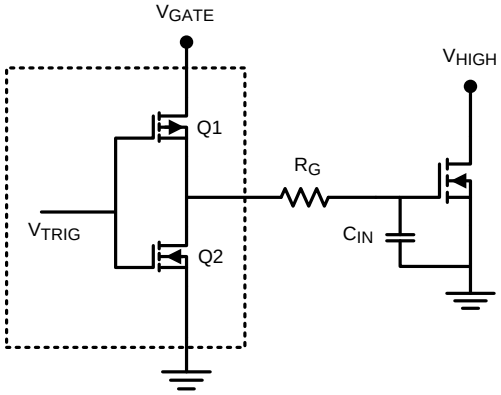


Figure 17. LM5110 drives MOSFET with Driver Output Stage and MOSFET Gate-Source Capacitance

Thermal Considerations (continued)

The schematic above shows a conceptual diagram of the LM5110 output and MOSFET load. Q1 and Q2 are the switches within the gate driver. R_G is the gate resistance of the external MOSFET, and C_{IN} is the equivalent gate capacitance of the MOSFET. The gate resistance Rg is usually very small and losses in it can be neglected. The equivalent gate capacitance is a difficult parameter to measure since it is the combination of C_{GS} (gate to source capacitance) and C_{GD} (gate to drain capacitance). Both of these MOSFET capacitances are not constants and vary with the gate and drain voltage. The better way of quantifying gate capacitance is the total gate charge Q_G in coloumbs. Q_G combines the charge required by C_{GS} and C_{GD} for a given gate drive voltage V_{GATE}.

Assuming negligible gate resistance, the total power dissipated in the MOSFET driver due to gate charge is approximated by

$$P_{DRIVER} = V_{GATE} \times Q_G \times F_{SW}$$

where

- F_{SW} = switching frequency of the MOSFET (1)

As an example, consider the MOSFET MTD6N15 whose gate charge specified as 30 nC for V_{GATE} = 12 V.

The power dissipation in the driver due to charging and discharging of MOSFET gate capacitances at switching frequency of 300 kHz and V_{GATE} of 12 V is equal to

$$P_{DRIVER} = 12\ V \times 30\ nC \times 300\ kHz = 0.108\ W. \quad (2)$$

If both channels of the LM5110 are operating at equal frequency with equivalent loads, the total losses will be twice as this value which is 0.216 W.

In addition to the above gate charge power dissipation, - transient power is dissipated in the driver during output transitions. When either output of the LM5110 changes state, current will flow from V_{CC} to V_{EE} for a very brief interval of time through the output totem-pole N and P channel MOSFETs. The final component of power dissipation in the driver is the power associated with the quiescent bias current consumed by the driver input stage and undervoltage lockout sections.

Characterization of the LM5110 provides accurate estimates of the transient and quiescent power dissipation components. At 300-kHz switching frequency and 30-nC load used in the example, the transient power will be 8 mW. The 1-mA nominal quiescent current and 12-V V_{GATE} supply produce a 12-mW typical quiescent power.

Therefore the total power dissipation

$$P_D = 0.216 + 0.008 + 0.012 = 0.236W. \quad (3)$$

We know that the junction temperature is given by

$$T_J = P_D \times \theta_{JA} + T_A \quad (4)$$

Or the rise in temperature is given by

$$T_{RISE} = T_J - T_A = P_D \times \theta_{JA} \quad (5)$$

For SOIC-8 package θ_{JA} is estimated as 114°C/W see *Thermal Information* section.

Therefore T_{RISE} is equal to

$$T_{RISE} = 0.236 \times 114 \approx 27°C \quad (6)$$

For WSON-10 package, the integrated circuit die is attached to leadframe die pad which is soldered directly to the printed circuit board. This substantially decreases the junction to ambient thermal resistance (θ_{JA}). θ_{JA} as low as 40°C/W is achievable with the WSON10 package. The resulting T_{RISE} for the dual driver example above is thereby reduced to just 9.5°.

11.3.2 Continuous Current Rating of LM5110

The LM5110 can deliver pulsed source/sink currents of 3 A and 5 A to capacitive loads. In applications requiring continuous load current (resistive or inductive loads), package power dissipation, limits the LM5110 current capability far below the 5-A sink/3-A source capability. Rated continuous current can be estimated both when sourcing current to or sinking current from the load. For example when sinking, the maximum sink current can be calculated using Equation 7.

$$I_{SINK}(MAX) := \sqrt{\frac{T_J(MAX) - T_A}{\theta_{JA} \cdot R_{DS}(ON)}}$$

Thermal Considerations (continued)

where

- R_{DS}(on) is the on resistance of lower MOSFET in the output stage of LM5110. (7)

Consider T_J(max) of 125°C and θ_{JA} of 114°C/W for an SO-8 package under the condition of natural convection and no air flow. If the ambient temperature (T_A) is 60°C, and the R_{DS}(on) of the LM5110 output at T_J(max) is 2.5 Ω, this equation yields I_{SINK}(max) of 478 mA which is much smaller than 5-A peak pulsed currents.

Similarly, the maximum continuous source current can be calculated as

$$I_{SOURCE}(MAX) := \frac{T_J(MAX) - T_A}{\theta_{JA} \cdot V_{DIODE}}$$

where

- V_{DIODE} is the voltage drop across hybrid output stage which varies over temperature and can be assumed to be about 1.1 V at T_J(max) of 125°C (8)

Assuming the same parameters as above, this equation yields I_{SOURCE}(max) of 518 mA.

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

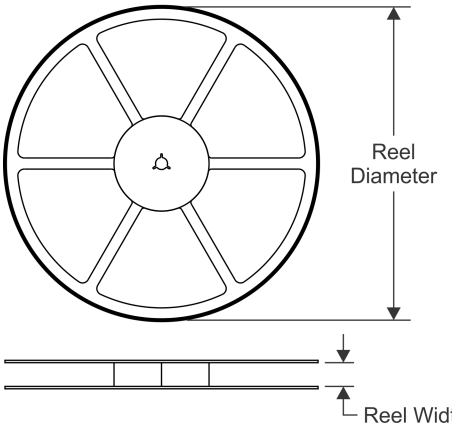
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

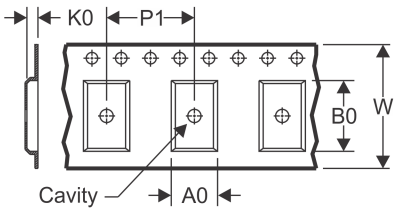
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

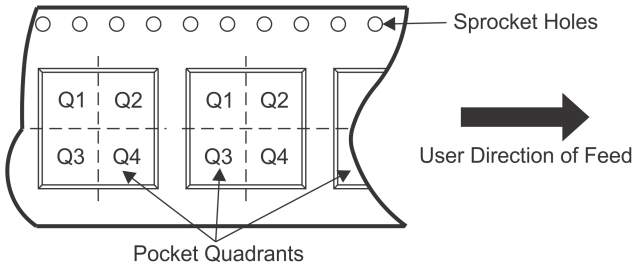


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

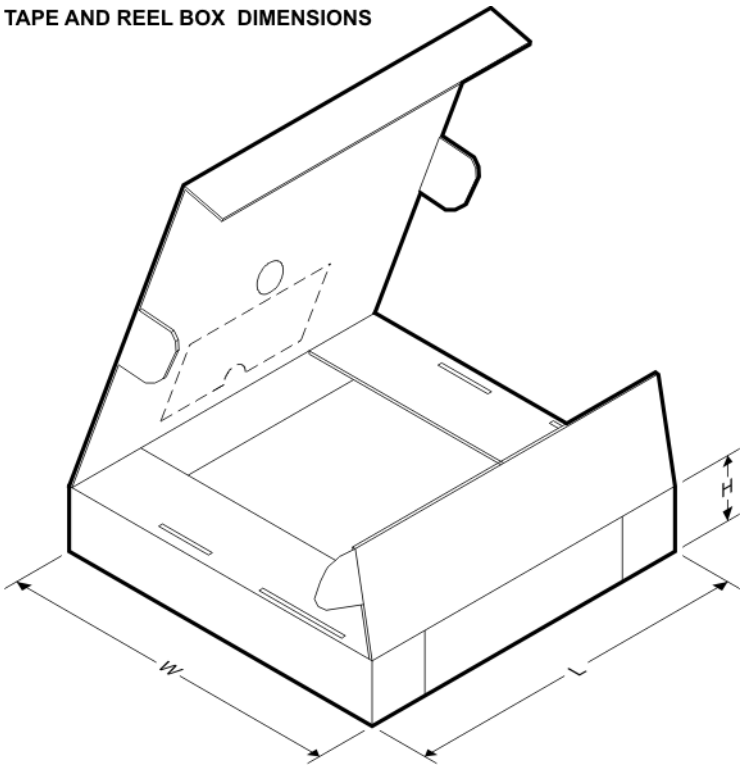
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5110-1MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5110-1SD	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5110-1SD/NOPB	WSON	DPR	10	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5110-1SDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5110-2MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5110-2SD/NOPB	WSON	DPR	10	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5110-2SD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5110-3MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5110-3SD	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5110-3SD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5110-3SDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5110-1MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5110-1SD	WSON	DPR	10	1000	210.0	185.0	35.0
LM5110-1SD/NOPB	WSON	DPR	10	1000	203.0	203.0	35.0
LM5110-1SDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0
LM5110-2MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5110-2SD/NOPB	WSON	DPR	10	1000	203.0	203.0	35.0
LM5110-2SD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5110-3MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5110-3SD	WSON	DPR	10	1000	210.0	185.0	35.0
LM5110-3SD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5110-3SDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0

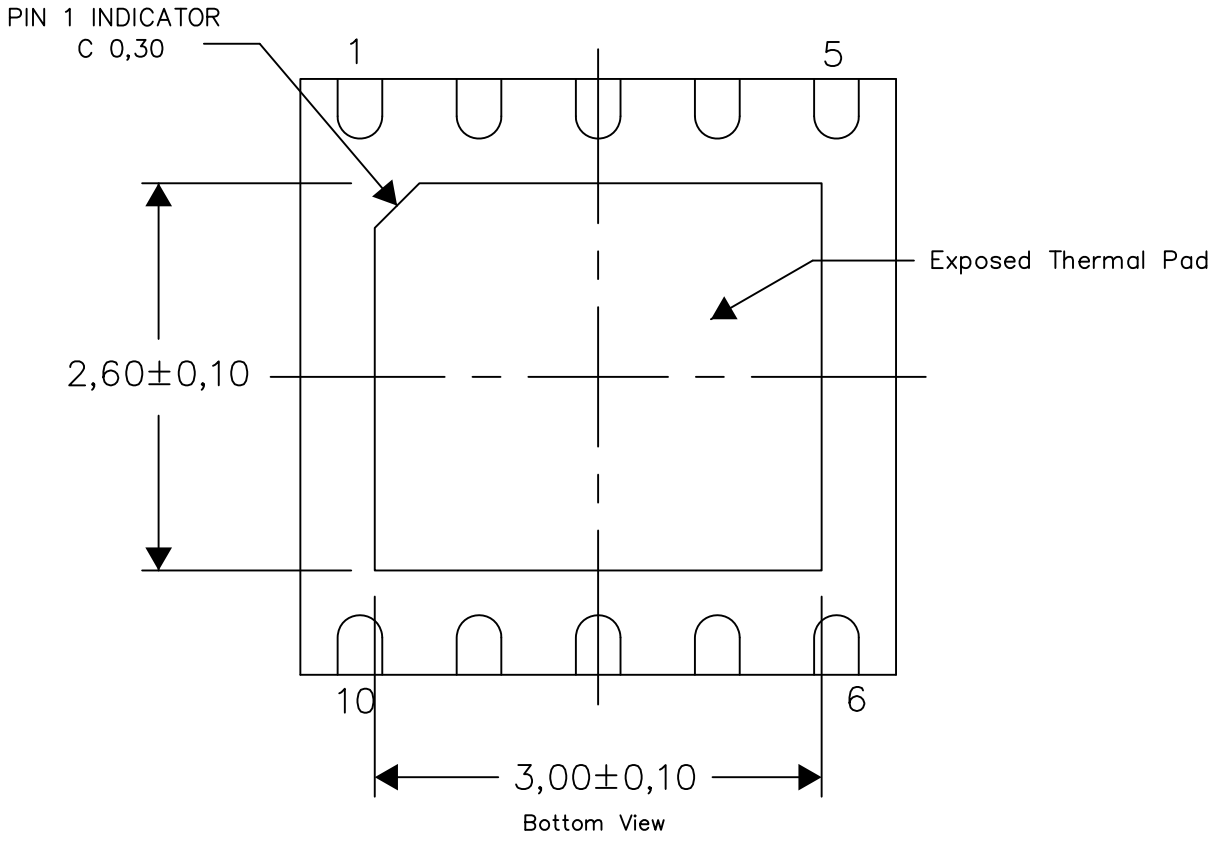
DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

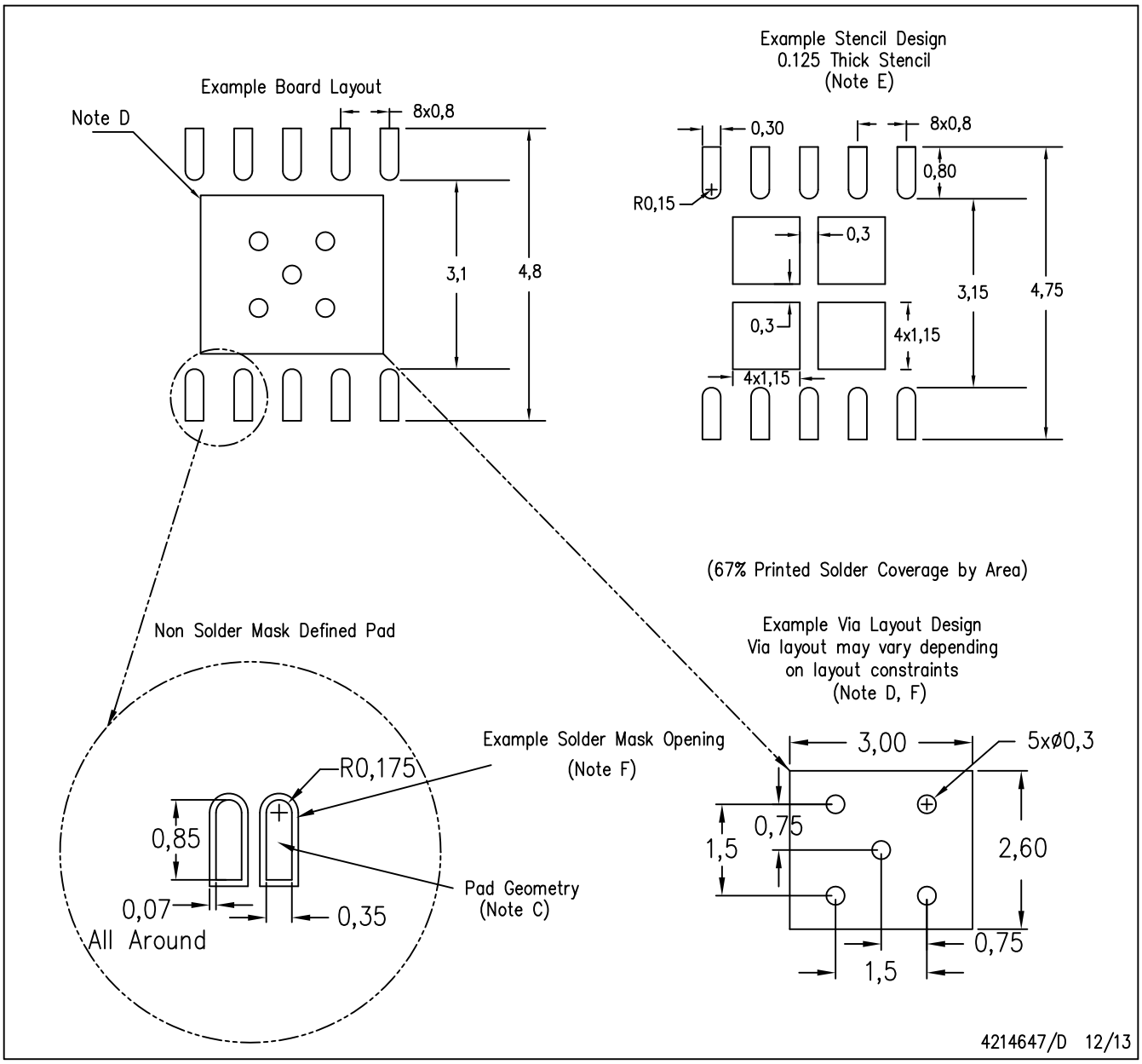


Exposed Thermal Pad Dimensions

4211551/C 12/13

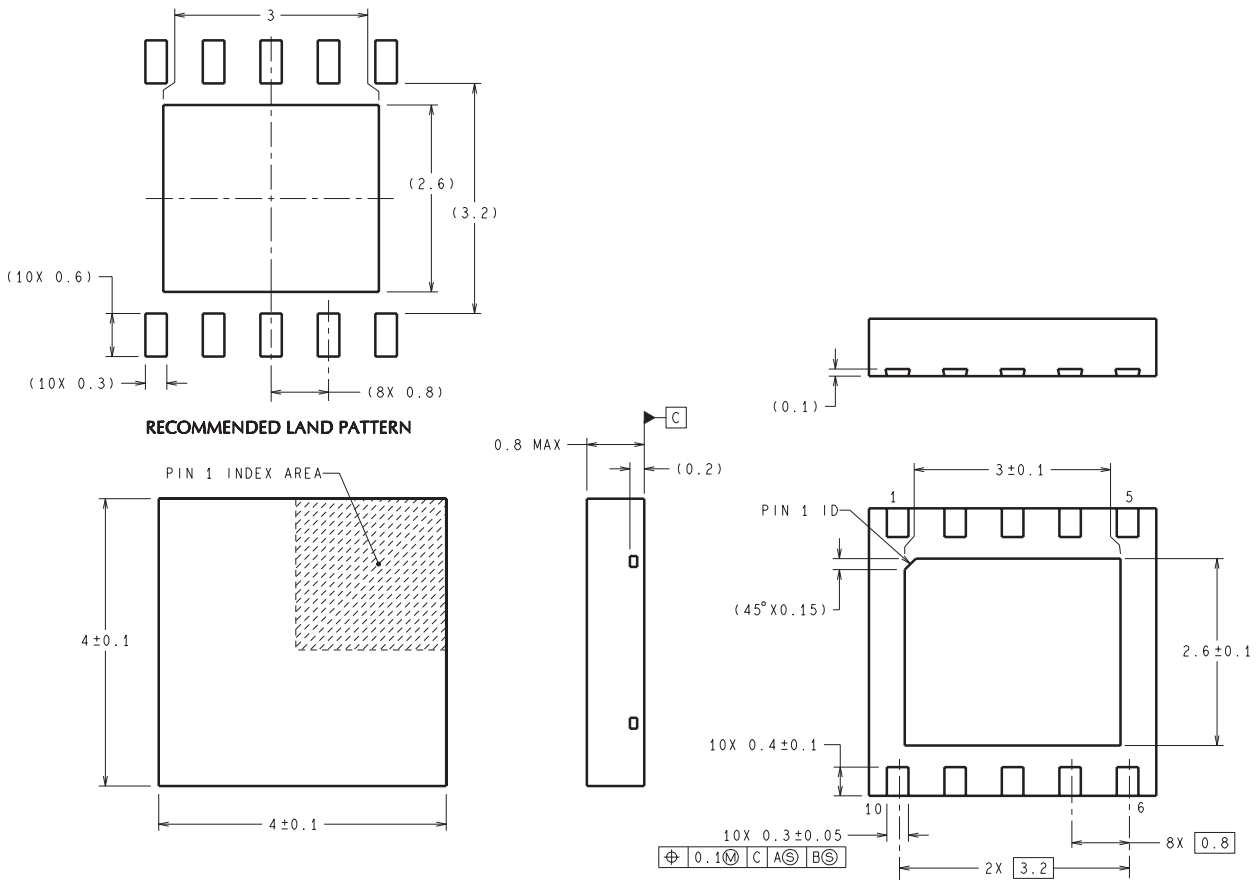
NOTES: All linear dimensions are in millimeters

DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



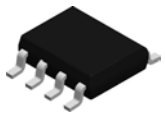
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DPR0010A



DIMENSIONS ARE IN MILLIMETERS

SDC10A (Rev A)

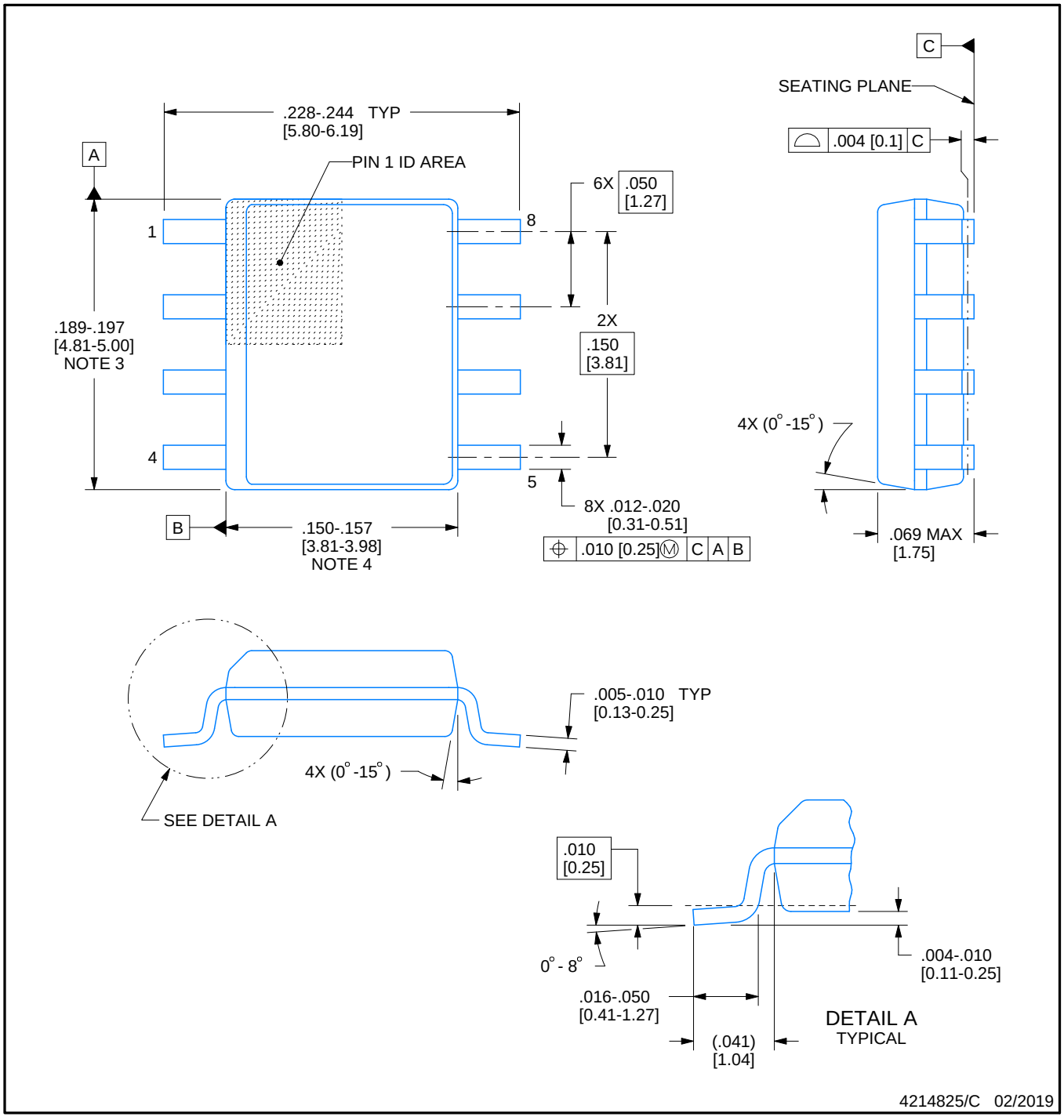


PACKAGE OUTLINE

D0008A

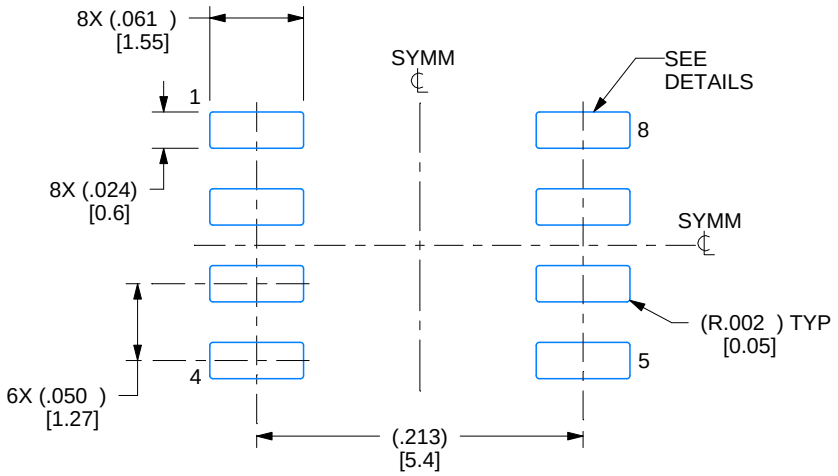
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

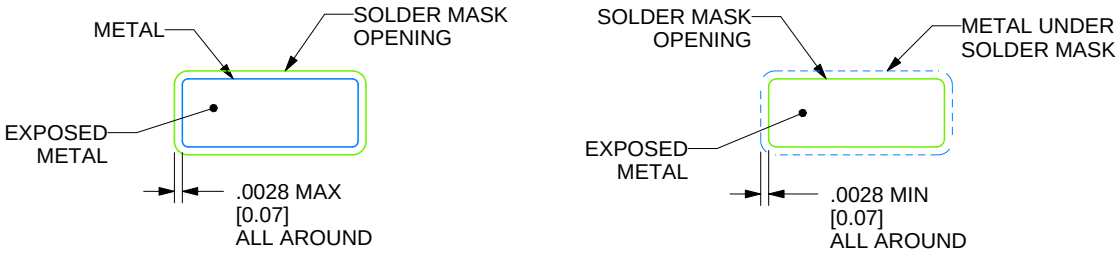


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

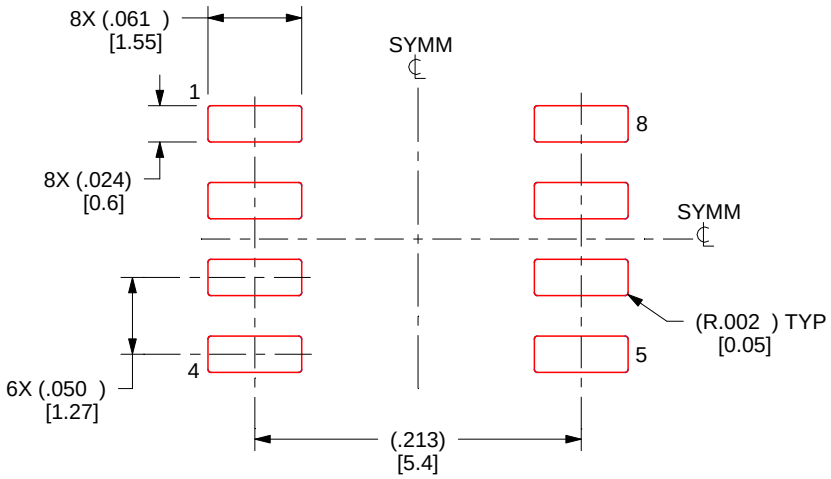
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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