THE DATASHEET OF

LM5072MH-50/NOPB

LM5072 Integrated 100V Power Over Ethernet PD Interface and PWM Controller with Aux Support

Check for Samples: LM5072

FEATURES

- **PD Interface**
  - **Fully Compliant IEEE 802.3af PD Interface**
  - **Versatile Auxiliary Power Options**
  - **9V Minimum Auxiliary Power Operating Range**
  - **100V Maximum Input Voltage Rating**
  - **Programmable DC Current Limit Up To 800mA**
  - **100V, 0.7Ω Hot Swap MOSFET**
  - **Integrated PD Signature Resistor**
  - **Integrated PoE Input UVLO**
  - **Programmable Inrush Current Limit**
  - **PD Classification Capability**
  - **Power Good Indicator**
  - **Thermal Shutdown Protection**
- **PWM Controller**
  - **Current Mode PWM Controller**
  - **100V Start-Up Regulator**
  - **Error Amplifier with 2% Voltage Reference**
  - **Supports Isolated and Non-Isolated Applications**
  - **Programmable Oscillator Frequency**
  - **Programmable Soft-Start**
  - **800 mA Peak Gate Driver**
  - **80% Maximum Duty Cycle with Built-in Slope Compensation (-80 Device)**
  - **50% Maximum Duty Cycle, No Slope Compensation (-50 Device)**

APPLICATIONS

- **IEEE 802.3af Compliant PoE Powered Devices**
- **Non-Compliant, Application Specific Devices**
- **Higher Power Ethernet Powered Devices**

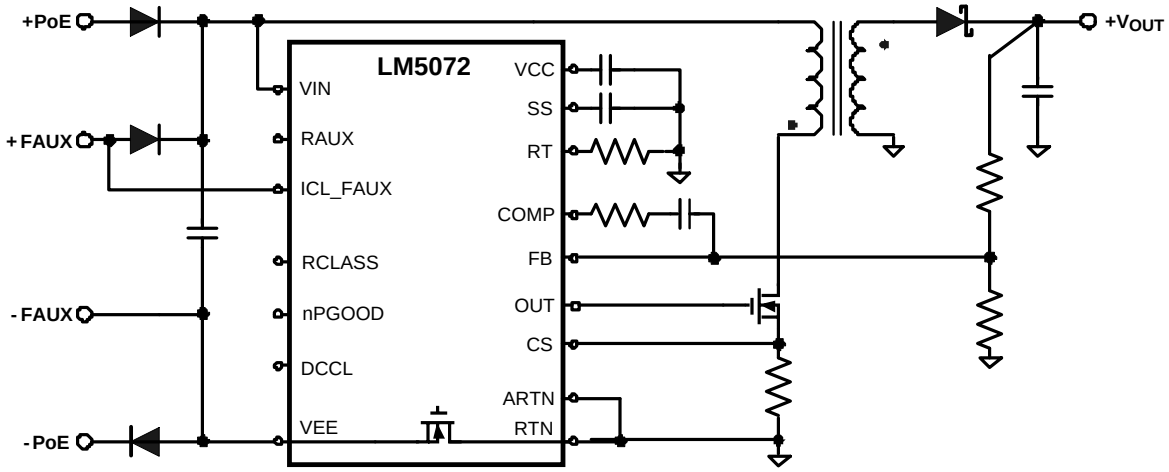
DESCRIPTION

The LM5072 Powered Device (PD) interface and Pulse-Width-Modulation (PWM) controller provides a complete power solution, fully compliant to IEEE 802.3af, for the PD connecting into Power over Ethernet (PoE) networks. This controller integrates all functions necessary to implement both a PD powered interface and DC-DC converter with a minimum number of external components. The LM5072 provides the flexibility for the PD to also accept power from auxiliary sources such as AC adapters in a variety of configurations. The low RDS(ON) PD interface hot swap MOSFET and programmable DC current limit extend the range of LM5072 applications up to twice the power level of 802.3af compliant PD devices. The 100V maximum voltage rating simplifies selection of the transient voltage suppressor that protects the PD from network transients. The LM5072 includes an easy-to-use PWM controller that facilitates the various single-ended power supply topologies including the flyback, forward and buck. The PWM control scheme is based on peak current mode control, which provides inherent advantages including line feed-forward, cycle-by-cycle current limit, and simplified feedback loop compensation. Two versions of the LM5072 provide either an 80% maximum duty cycle (-80 suffix), or a 50% maximum duty cycle (-50 suffix).

PACKAGES

- **TSSOP-16 EP (Exposed Pad)**

Simplified Application Diagram



Connection Diagram

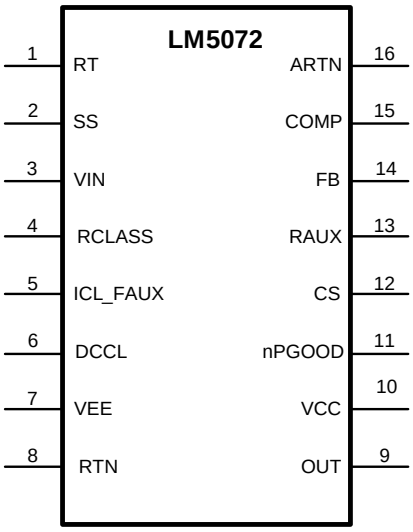


Figure 1. 16 Lead TSSOP-EP

PIN DESCRIPTIONS

Pin Number	Name	Description
1	RT	PWM controller oscillator frequency programming pin.
2	SS	Soft-start programming pin.
3	VIN	Positive supply pin for the PD interface and the internal PWM controller start-up regulator.
4	RCLASS	PD classification programming pin.
5	ICL_FAUX	Inrush current limit programming pin; also the front auxiliary power enable pin.
6	DCCL	PD interface DC current limit programming pin.
7	VEE	Negative supply pin for PD interface; connected to PoE and/or front auxiliary power return path.
8	RTN	PWM controller power return; connected to the drain of the internal PD interface hot swap MOSFET; should be externally connected to the reference ground of the PWM controller.
9	OUT	PWM controller gate driver output pin.
10	VCC	PWM controller start-up regulator output pin.
11	nPGOOD	PD interface Power Good indicator and delay timer pin; active low state indicates PoE interface is in normal operation.
12	CS	PWM controller current sense input pin.
13	RAUX	Rear auxiliary power enable pin; can be programmed for auxiliary power dominance over PoE power.
14	FB	PWM controller voltage feedback pin and inverting input of the internal error amplifier; connect to ARTN to disable the error amplifier in isolated dc-dc converter applications.
15	COMP	Output of the internal error amplifier and control input to the PWM comparator. In isolated applications, COMP is controlled by the secondary side error amplifier via an opto-coupler.
16	ARTN	PWM controller reference ground pin; should be shorted externally to the RTN pin as a single point ground connection to improve noise immunity.
	EP	Exposed metal pad on the underside of the device. It is recommended to connect this pad to a PC Board plane connected to the VEE pin to improve heat dissipation.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

VIN , RTN to VEE(3)		-0.3V to 100V
RAUX to ARTN		-0.3V to 100V
ICL_FAUX to VEE		-0.3V to 100V
DCCL, RCLASS to VEE		-0.3V to 7V
nPGOOD to ARTN		-0.3V to 16V
ARTN to RTN		-0.3V to 0.3V
VCC, OUT to ARTN		-0.3V to 16V
CS, FB, RT to ARTN		-0.3V to 7V
COMP, SS to ARTN		-0.3V to 5.5V
ESD Rating	Human Body Model(4)	2000V
Lead Soldering Temp.(5)	Wave (4 seconds)	260°C
	Infrared (10 seconds)	240°C
	Vapor Phase (75 seconds)	219°C
Storage Temperature		-55°C to 150°C
Junction Temperature		150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) During rear auxiliary operation, the RTN pin can be approximately -0.4V with respect to VEE. This is caused by normal internal bias currents, and will not harm the device. Application of external voltage or current must not cause the absolute maximum rating to be exceeded.
(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.
(5) For detailed information on soldering the plastic TSSOP package, refer to the Packaging Databook available from Texas Instruments.

Operating Ratings

V_{IN} voltage	9V to 70V
External voltage applied to V_{CC}	8V to 15V
Operating Junction Temperature	-40°C to 125°C

Electrical Characteristics(1)

Specifications in standard type face are for T_J = +25°C and those in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified: V_{IN} = 48V, F_{OSC} = 250kHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Detection and Classification						
	V_{IN} Signature Startup Voltage				**1.5**	V
	Signature Resistance		**23.25**	24.5	**26**	kΩ
	Signature Resistor Disengage/ Classification Engage	V_{IN} Rising	**11.0**	12.0	**12.6**	V
	Hysteresis			1.9		V
	Classification Current Turn Off	V_{IN} Rising	**22**	23.5	**25**	V
	Classification Voltage		**1.213**	1.25	**1.287**	V
	Supply Current During Classification	V_{IN} = 17V		0.7	**1.1**	mA
Line Under Voltage Lock-Out						
	UVLO Release	V_{IN} Rising	**36**	38.5	**40**	V
	UVLO Lock out	V_{IN} Falling	**29.5**	31.0	**32.5**	V
	UVLO Hysteresis		**6**			V
	UVLO Filter			300		µs

(1) Minimum and Maximum limits are ensured through test, design, or statistical correlation using Statistical Quality Control (SQC) methods. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purpose only. Limits are used to calculate Texas Instruments' Average Outgoing Quality Level (AOQL).

Electrical Characteristics[1] (continued)

Specifications in standard type face are for T_J = +25°C and those in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified: V_{IN} = 48V, F_{OSC} = 250kHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Power Good						
	VDS Required for Power Good Status		**1.3**	1.5	**1.7**	V
	VDS Hysteresis of Power Good Status		**0.8**	1.0	**1.2**	V
	VGS Required for Power Good Status		**4.5**	5.5	**6.5**	V
	Default Delay Time of Loss-of Power Good Status			30		µs
	nPGOOD current Source		**45**	55	**65**	µA
	nPGOOD Pull Down Resistance			130	**250**	Ω
	nPGOOD Threshold		**2.3**	2.5	**2.7**	V
Hot Swap						
RDS(ON)	Hot Swap MOSFET Resistance			0.7	**1.2**	Ω
	Hot Swap MOSFET Leakage				**110**	µA
	Default Inrush Current Limit	V_{DS} = 4.0V	**120**	150	**180**	mA
	Default DC Current Limit	V_{DS} = 4.0V	**380**	440	**510**	mA
	Front Auxiliary DC Current Limit	V_{DS} = 4.0V	**470**	540	**610**	mA
	Inrush Current Limit Programming Accuracy	V_{DS} = 4.0V	**-15**		**15**	%
	DC Current Limit Programming Accuracy	V_{DS} = 4.0V	**-12**		**12**	%
Auxiliary Power Option						
	ICL_FAUX Threshold	ICL_FAUX Pin Rising	**8.1**	8.7	**9.3**	V
	ICL_FAUX Pull Down Current			50		µA
	RAUX Lower Threshold (I = 22 µA)	RAUX Pin Rising	**2.3**	2.5	**3.0**	V
	RAUX Lower Threshold Hysteresis			0.8		V
	RAUX Upper Threshold (I = 250 µA)	RAUX Pin Rising	**5.4**	6.0	**6.9**	V
	RAUX Lower Threshold Current		**16**	22	**28**	µA
	RAUX Upper Threshold Current		**187**	250	**313**	µA
VCC Regulator						
VccReg	VCC Regulation (VccReg)		**7.4**	7.7	**8**	V
	VCC Current Limit		**15**			mA
	VCC UVLO (Rising)		**VccReg – 210 mV**	VccReg – 100 mV		mV
	VCC UVLO (Falling)		**5.9**	6.2	**6.5**	V
	VIN Supply Current	V_{CC} = 10V			**2.0**	mA
	Supply Current (Icc)	V_{CC} = 10V			**3**	mA
	VCC Regulator Dropout	$V_{IN} – V_{CC}$[2]			**6.5**	V
Error Amplifier						
	Gain Bandwidth			3		MHz
	DC Gain			67		dB
	Input Voltage		**1.225**		**1.275**	V
	COMP Sink Capability		**5**	10		mA
Current Limit						
	ILIM Delay to Output			30		ns
	Cycle by Cycle Current Limit Threshold Voltage		**0.45**	0.5	**0.55**	V
	Leading Edge Blanking Time			65		ns
	CS Sink Impedance (clocked)			35	**55**	Ω

(2) The VCC regulator is intended for use solely as a bias supply for the LM5072, dropout assumes 3mA of external V_{CC} current.

Electrical Characteristics[1] (continued)

Specifications in standard type face are for T_J = +25°C and those in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified: V_{IN} = 48V, F_{OSC} = 250kHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Soft-start						
	Soft-start Current Source		**8**	10	**12**	µA
Oscillator						
	Frequency1 (R_T = 26.1 kΩ)		**175**	200	**225**	KHz
	Frequency2 (R_T = 8.7 kΩ)		**515**	580	**645**	KHz
	Sync threshold		**2.6**	3.2	**3.8**	V
PWM Comparator						
	Delay to Output			25		ns
	Min Duty Cycle				**0**	%
	Max Duty Cycle (-80 Device)		**75**	80	**85**	%
	Max Duty Cycle (-50 Device)		**47**	50	**53**	%
	COMP to PWM Comparator Gain			0.33		
	COMP Open Circuit Voltage		**4.3**	5.2	**6.1**	V
	COMP Short Circuit Current		**0.6**	1.0	**1.4**	mA
Slope Compensation (LM5072-80 Device Only)						
	Slope Comp Amplitude		**70**	90	**110**	mV
Output Section						
	Output High Saturation			0.25	**0.75**	V
	Output Low Saturation			0.25	**0.75**	V
t_r	Rise time	C_{LOAD} = 1nF		18		ns
t_f	Fall time	C_{LOAD} = 1nF		15		ns
PDI Thermal Shutdown[3]						
	Thermal Shutdown Temp.			165		°C
	Thermal Shutdown Hysteresis			25		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient	PWP package		40		°C/W

(3) Device thermal limitations may limit usable range.

Typical Performance Characteristics

UVLO Threshold vs Temperature

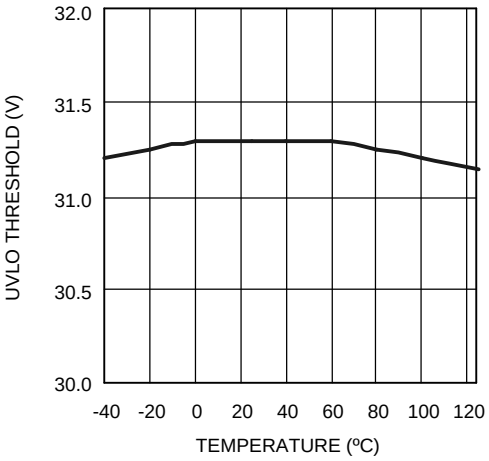


Figure 2.

Default Current Limit vs Temperature

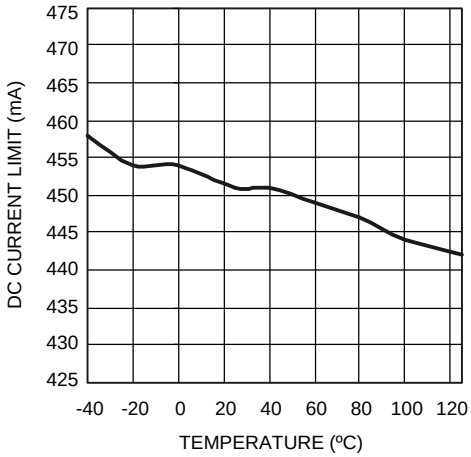


Figure 3.

Inrush Current Limit vs ICL_FAUX Resistor

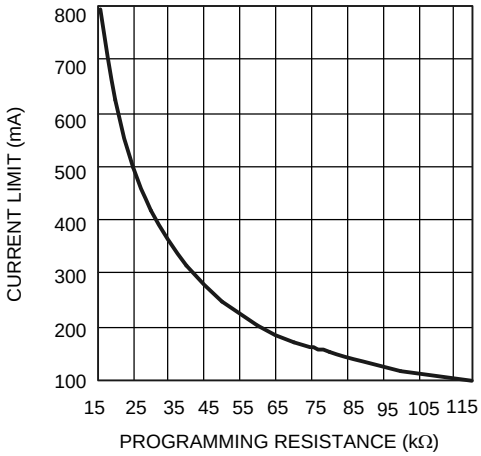


Figure 4.

DC Current Limit vs DCCL Resistor

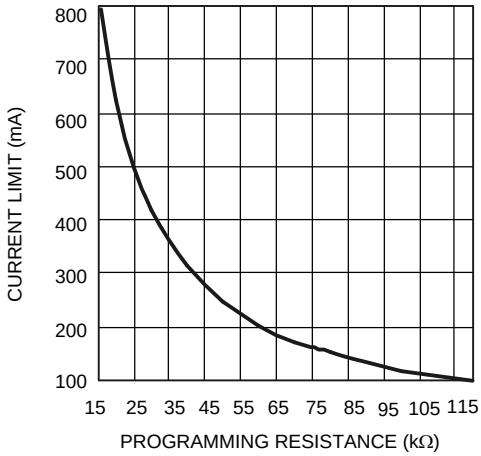


Figure 5.

Programmed DC Current Limit vs Temperature

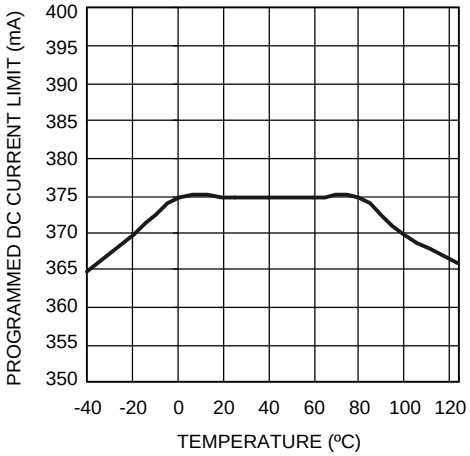


Figure 6.

Oscillator Frequency vs Temperature

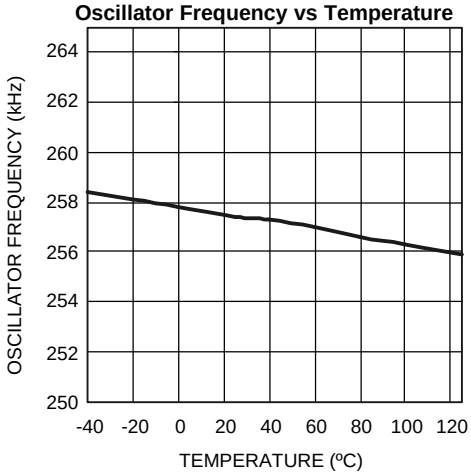


Figure 7.

Typical Performance Characteristics (continued)

Oscillator Frequency vs RT Resistance

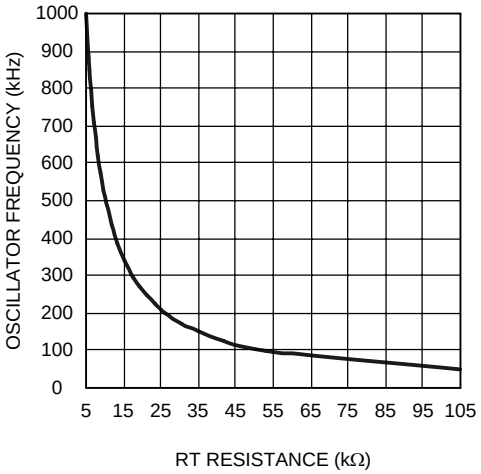


Figure 8.

Error Amplifier Reference Voltage vs Temperature

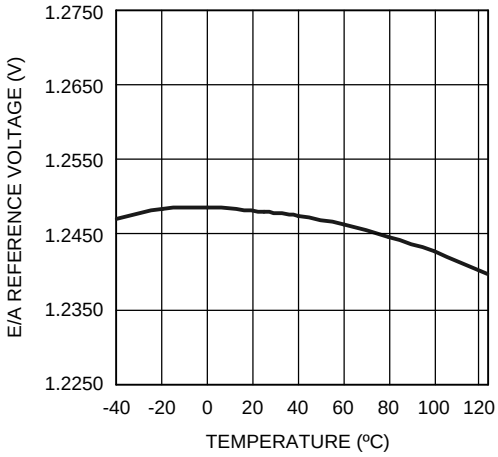


Figure 9.

V_{CC} vs I_{CC}

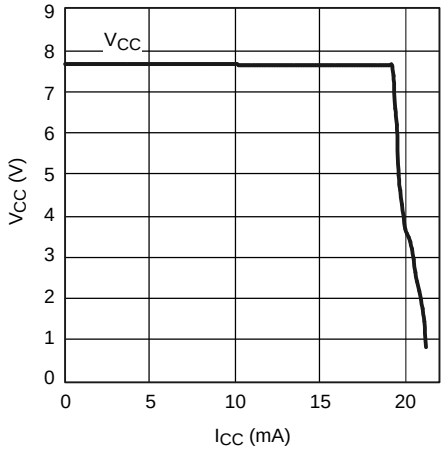


Figure 10.

Input Current vs Input Voltage

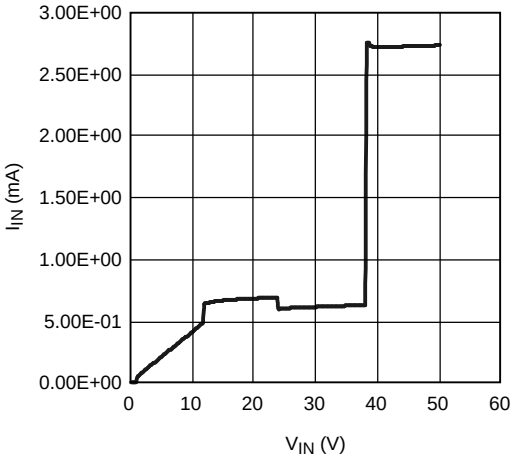


Figure 11.

Maximum Duty Cycle vs Temperature

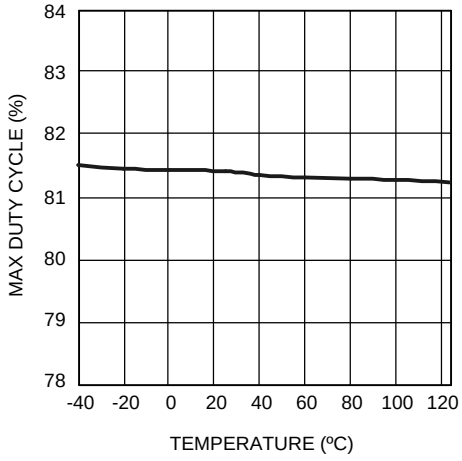


Figure 12.

Soft-start Current vs Temperature

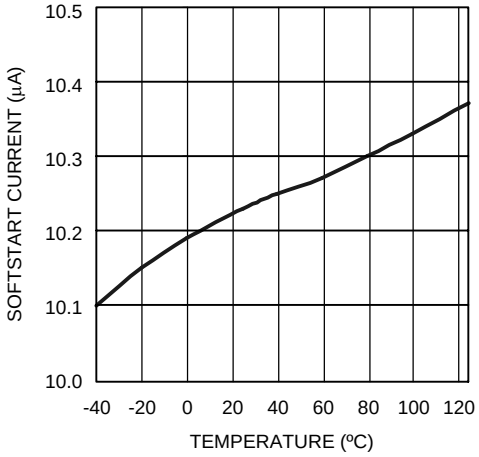


Figure 13.

Specialized Block Diagrams

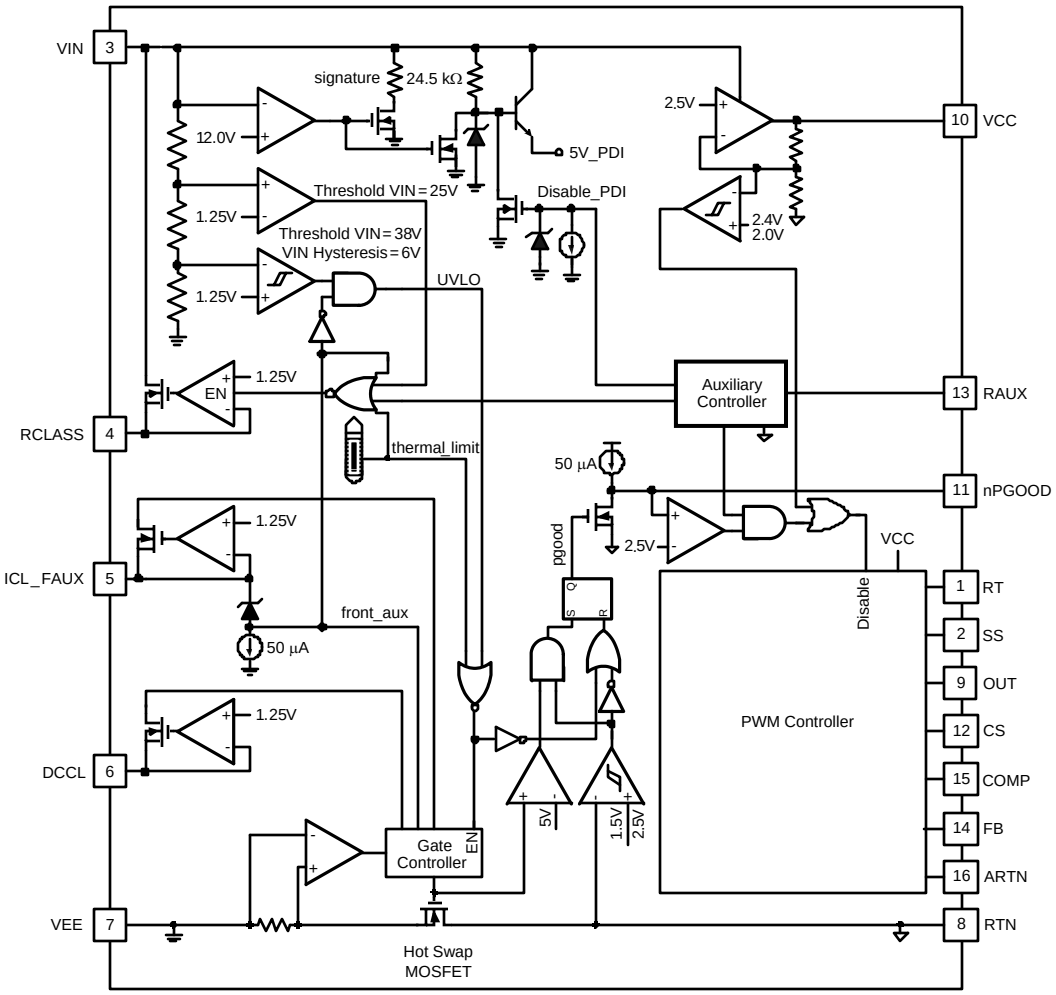


Figure 14. Top Level Block Diagram

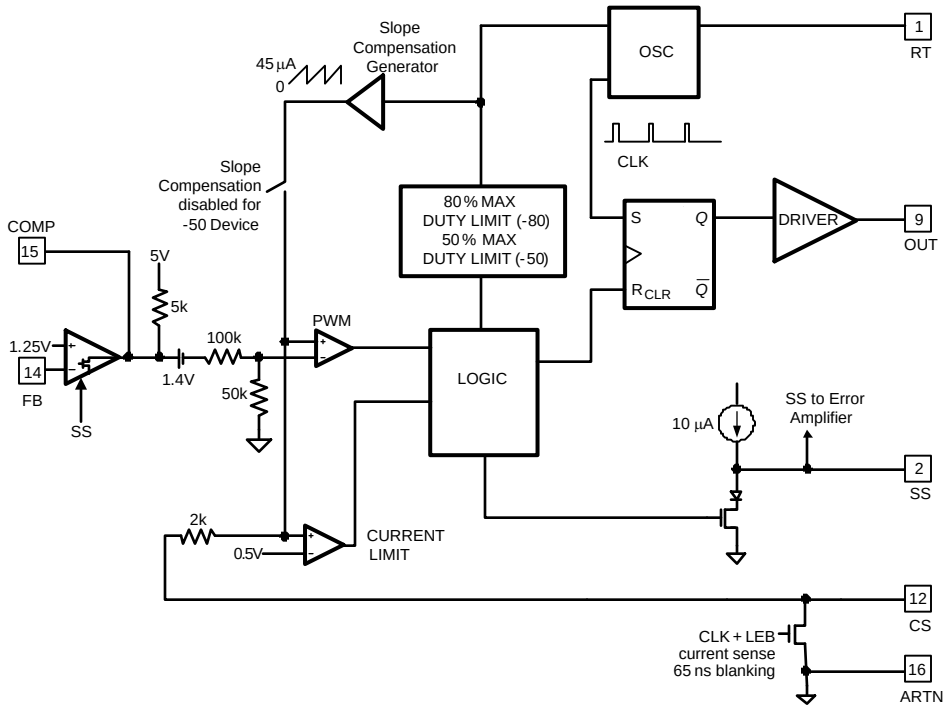


Figure 15. PWM Controller Block Diagram

DESCRIPTION OF OPERATION AND APPLICATIONS INFORMATION

The LM5072 integrates a fully IEEE 802.3af compliant PD interface and PWM controller in a single integrated circuit, providing a complete and low cost power solution for devices that connect to PoE systems. The implementation requires a minimal number of external components.

The LM5072's Hot Swap PD interface provides four major advantages:

1. An input voltage rating up to 100V that allows greater flexibility when selecting a transient surge suppressor to protect the PD from voltage transients encountered in PoE applications.
2. The integration of the PD signature resistor and other functions including programmable inrush current limit, input voltage under-voltage lock-out (UVLO), PD classification, and thermal shutdown simplifies PD implementation.
3. The PD interface and PWM controller accept power from auxiliary sources including AC adapters and solar cells in various configurations and over a wide range of input voltages. Auxiliary power input can be programmed to be dominant over PoE power.
4. DC current limit is programmable and adjustable to support PoE applications requiring input currents up to 700 mA.

The LM5072 includes an easy to use PWM controller based on the peak current mode control technique. Current mode control provides inherent advantages such as line voltage feed-forward, cycle-by-cycle current limit, and simplified closed-loop compensation. The controller's PWM gate driver is capable of sourcing and sinking peak currents of 800 mA to directly drive the power MOSFET switch of the DC-DC converter. The PWM controller also contains a high gain, high bandwidth error amplifier, a high voltage startup bias regulator, a programmable oscillator for a switching frequency between 50 kHz to 500 kHz, a bias supply (V_{CC}) under-voltage lock-out circuit, and a programmable soft-start circuit. These features greatly simplify the design and implementation of single ended topologies like the flyback, forward and buck.

The LM5072 is available in two versions, the LM5072-50 and LM5072-80. As indicated in the suffix of the part number, the maximum duty cycle of each device is limited to 50% and 80%, respectively. Internal PWM controller slope compensation is provided in the LM5072-80 version.

Modes of Operation

Per the IEEE 802.3af specification, when a PD is connected to a PoE system it transitions through several operating modes in sequence including detection, classification (optional), turn on, normal operation, and power removal. Each operating mode corresponds to a specific PoE voltage range fed through the Ethernet cable. Figure 16 shows the IEEE 802.3af specified sequence of operating modes and the corresponding PD input voltages.

Current steering diode-bridges are required for the PD interface to accept all allowable connections and polarities of PoE voltage from the RJ-45 connector (see the example application circuits in Figure 31, Figure 32, Figure 33 and Figure 34). The bridge will cause some reduction of the input voltage sensed by the LM5072. To ensure full compliance to the specification in all operating modes, the LM5072 takes into account the voltage drop across the bridge diodes and responds appropriately to the voltage received from the PoE cable. Table 1 presents the response in each operating mode to voltages across the VIN and VEE pins.

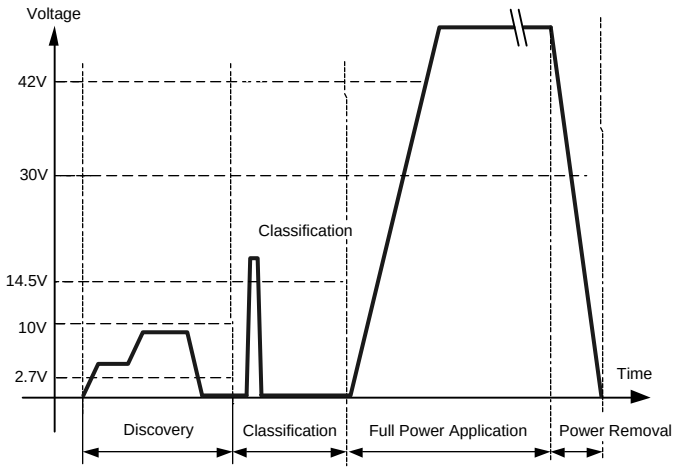


Figure 16. Sequence of PoE Operating Modes

Table 1. Operating Modes With Respect To Input Voltage

Mode of Operation	Voltage from PoE Cable per IEEE 802.3af	LM5072 Input Voltage (V_{IN} pin to V_{EE} pin)
Detection (Signature)	2.7V to 10.0V	1.5V to 10.0V
Classification	14.5V to 20.5V	12V to 23.5V
Startup	42V max	38V (UVLO Release, V_{IN} Rising)
Normal Operation	57V to 36V	70V to 32V (UVLO, V_{IN} Falling)

Detection Signature

During detection mode, a PD must present a signature resistance between 23.75 kΩ and 26.25 kΩ to the PoE power sourcing equipment. This signature impedance distinguishes the PD from non-PoE capable equipment to protect the latter from being accidentally damaged by inadvertent application of PoE voltage levels. To simplify the circuit implementation, the LM5072 integrates the 24.5 kΩ signature resistor, as shown in Figure 17.

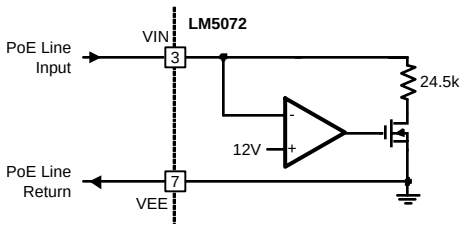


Figure 17. Detection Circuit With Integrated PD Signature Resistor

During detection mode, the voltage across the VIN and VEE pins is less than 10V. Once signature mode is complete, the LM5072 will disengage the signature resistor to reduce power loss in all other modes.

Classification

Classification is an optional feature of the IEEE802.3af specification. It is primarily used to identify the power requirements of a particular PD device. This feature will allow the PSE to allocate the appropriate available power to each device on the network. Classification is performed by measuring the current flowing into the PD during this mode. IEEE 802.3af specifies five power classes, each corresponding to a unique range of classification current, as presented in Table 2. The LM5072 simplifies the classification implementation by requiring a single external resistor connected between the RCLASS and VEE pins to program the classification current. The resistor value required for each class is also given in Table 2.

Table 2. Classification Levels and Required External Resistor Value

Class	PD Max Power Level		ICLASS Range		LM5072 RCLASS Value
	From	To	From	To	
0 (Default)	0.44W	12.95W	0 mA	4 mA	Open
1	0.44W	3.84W	9 mA	12 mA	130Ω
2	3.84W	6.49W	17 mA	20 mA	71.5Ω
3	6.49W	12.95W	26 mA	30 mA	46.4Ω
4	Reserved	Reserved	36 mA	44 mA	31.6Ω

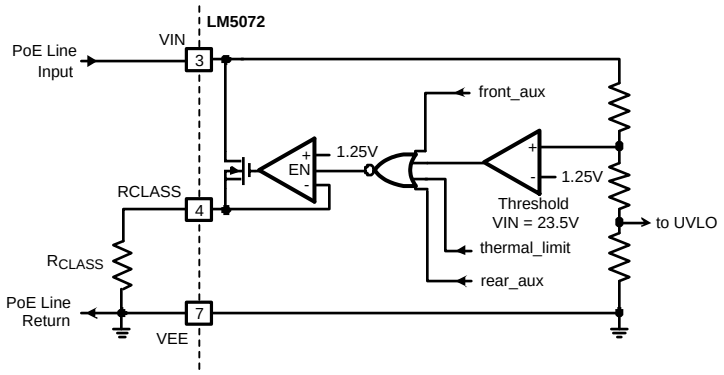


Figure 18. PD Classification – Fulfilled With a Single External Resistor

Figure 18 shows the LM5072's implementation of PD classification using an external resistor connected to the RCLASS pin. During classification, the voltage across the VIN and VEE pins is between 13V and 23.5V. In this voltage range, the class resistor RCLASS is engaged by enabling the 1.25V buffer amplifier and MOSFET. After classification is complete, the voltage from the PSE will increase to the normal operating voltage of the PoE system (48V nominal). When V_{IN} rises above 23.5V, the LM5072 will disengage the RCLASS resistor to reduce on-chip power dissipation.

The classification feature is disabled when either the front or rear auxiliary power options are selected, as the classification function is not required when power is supplied from an auxiliary source. The classification function is also disabled when the LM5072 reaches the thermal shutdown temperature threshold (nominally 165°C). This may occur if the LM5072 is operated at elevated ambient temperatures and the classification time exceeds the IEEE802.3af limit of 75 ms.

When the classification option is not required, simply leave the RCLASS pin open to set the PD to the default Class 0 state. Class 0 requires that the PSE allocate the maximum IEEE802.3af specified power of 15.4 W (12.95 W at the PD input terminals) to the PD.

Undervoltage Lockout (UVLO)

The LM5072's internal preset UVLO circuit continuously monitors the PoE input voltage between the VIN and VEE pins. When the V_{IN} voltage rises above 38V nominal, the UVLO circuit will release the hot swap MOSFET and initiate the startup inrush sequence. When the V_{IN} voltage falls below 31V nominal during normal operating mode, the LM5072 disables the PD by shutting off the hot swap MOSFET.

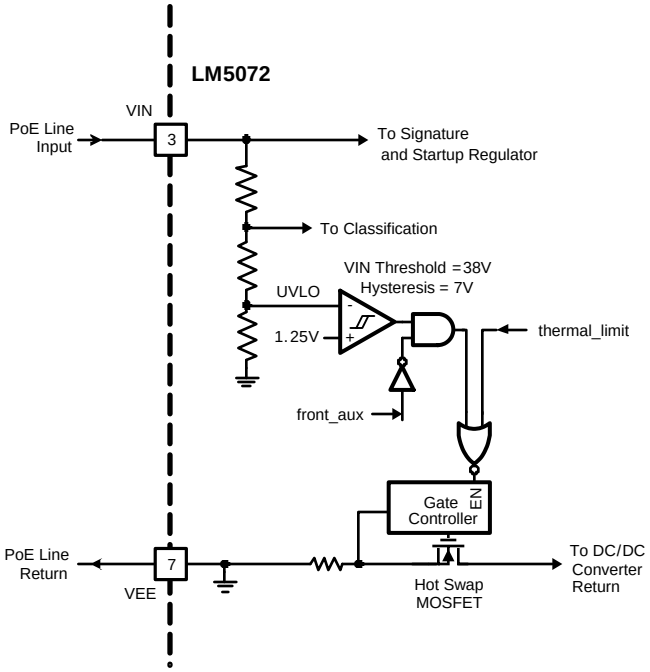


Figure 19. Preset Input UVLO Function

Figure 19 illustrates the block diagram of the LM5072 UVLO circuit. This function requires no external components. The UVLO signal can be over-ridden by the front auxiliary power option (see details in the RAUX Option section) to allow the hot swap MOSFET of the LM5072 to pass power from front auxiliary power sources at voltage levels below the PoE operating voltage. In the rear auxiliary power application (see RAUX Option section), the auxiliary power source bypasses the hot swap MOSFET and is applied directly to the input of the DC-DC converter. The UVLO function does not need to be over-ridden in this configuration.

The PD can draw a maximum current of 400 mA during standard 802.3af PoE operation. This current will cause a voltage drop of up to 8V over a 100m long Ethernet cable. The PD front-end current steering diode bridges may introduce an additional 2V drop. In order to ensure successful startup at the minimum PoE voltage of 42V, and to continue operation at the minimum requirement of 36V as specified by IEEE 802.3af, these voltage drops must be taken into account. Therefore, the LM5072 UVLO thresholds have been set to 38V on the rising edge of VIN, and 31V on the falling edge of VIN. The 7V nominal hysteresis of the UVLO function, in addition to the inrush current limit (discussed in the next section), prevents false starts and chattering during startup.

Inrush Current Limit Programming

According to IEEE 802.3af, the input capacitance of the PD power supply must be at least 5 µF (between the VIN and RTN pins). Considering the capacitor tolerance and the effects of voltage and temperature, a nominal capacitor value of at least 10 µF is recommended to ensure 5 µF minimum under all conditions. A greater amount of capacitance may be needed to filter the input ripple of the DC-DC converter. The input capacitors remain discharged during detection and classification modes of the PD interface. The hot swap MOSFET is turned on after the VIN minus VEE voltage difference rises above the UVLO release threshold of 38V nominal. When enabled, the hot swap MOSFET delivers a regulated inrush current to charge the input capacitors of the DC-DC converter. To prevent excessive inrush current, the LM5072 will turn on the hot swap MOSFET in a constant current mode. The default, pre-programmed inrush current of 150 mA can be selected by simply leaving the ICL_FAUX pin open.

To adjust the capacitor charging time for a particular application requirement, the inrush limit can be programmed to any value between 150 and 400 mA with an external resistor (R_{ICL}) between the ICL_FAUX and VEE pins, as shown in Figure 20. The relationship between the R_{ICL} value and the desired inrush current limit I_{INRUSH} satisfies the following equation:

$$R_{ICL}(k\Omega) = \frac{100\ mA}{I_{INRUSH\ (mA)}} \times 127.5\ k\Omega \quad (1)$$

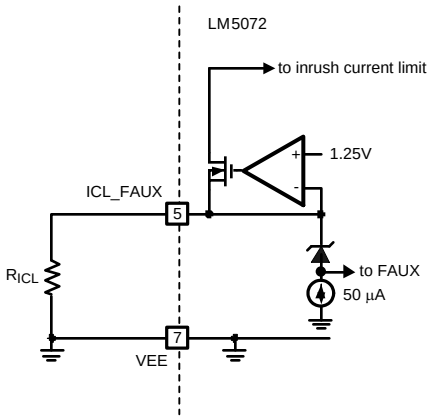


Figure 20. Input Inrush Limit Programming via R_{ICL}

The inrush current causes a voltage drop along the PoE Ethernet cable (20Ω maximum) that reduces the input voltage sensed by the LM5072. To avoid erratic turn-on (hiccups), I_{INRUSH} should be programmed such that the input voltage drop due to cable resistance does not exceed the $V_{IN-UVLO}$ hysteresis (6V minimum).

DC Current Limit Programming

The LM5072 provides a default DC current limit of 440 mA nominal. This default limit can be selected by leaving the DCCL pin open.

The LM5072 allows the DC current limit to be programmed within the range from 150 mA to 800 mA. Figure 21 shows the method to program the DC current limit with an external resistor, R_{DCCL}. The relationship between the R_{DCCL} value and the desired DC current limit I_{DC} satisfies the following equation:

$$R_{DCCL}(k\Omega) = \frac{100\ mA}{I_{DC\ (mA)}} \times 127.5\ k\Omega \quad (2)$$

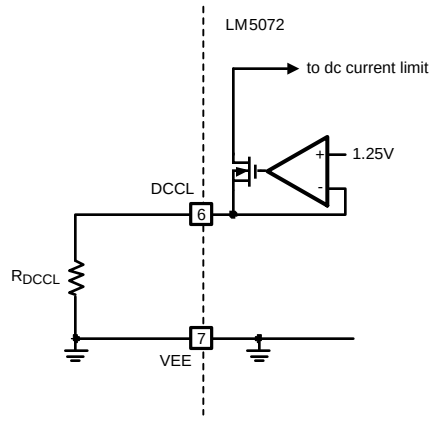


Figure 21. Input DC Current Limit Programming via R_{DCCL}

The maximum recommended DC current limit is 800 mA. While thermal analysis should be a standard part of the module development process, it may warrant additional attention if the DC current limit is programmed to values in excess of 400 mA. This analysis should include evaluations of the dissipation capability of LM5072 package, heat sinking properties of the PC Board, ambient temperature, and other heat dissipation factors of the operating environment.

Power Good and Regulator Startup

The Power Good status indicates that the circuit is ready for PWM controller startup to occur. It is established when the input capacitors are fully charged through the hot swap MOSFET. Since the hot swap MOSFET is in series with the input capacitors of the DC-DC converter, its drain-to-source voltage decreases as the charging occurs. Power Good is indicated when the following two conditions are met: the MOSFET drain-to-source voltage drops below 1.5V (with 1V hysteresis), and the gate-to-source voltage is greater than 5V. Circuitry internal to the LM5072 monitors both the drain and gate voltages (see Figure 14), and issues the Power Good status flag by pulling down the nPGOOD pin to a logic low level relative to the ARTN pin.

The nPGOOD circuitry consists of a 2.5V comparator, a 130Ω pull down MOSFET, and a 50 µA pull up current source, as shown in Figure 22. Once the Power Good status is established, the nPGOOD pin voltage will be pulled down quickly by the MOSFET, and the PWM controller will start as soon as the nPGOOD pin voltage drops below the 2.5V threshold.

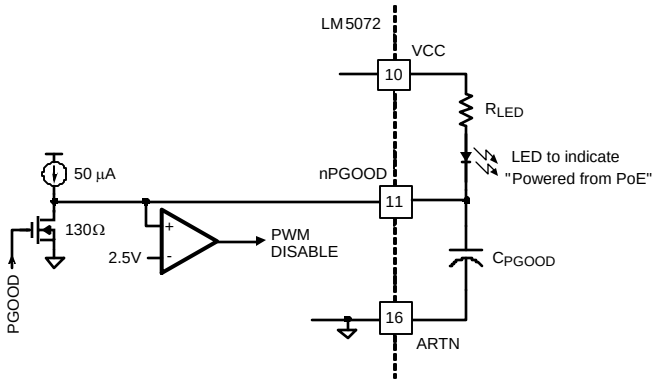


Figure 22. "Powered-from-PoE" Indictor and Power Good Delay Timer

The nPGOOD pin can be configured to perform multiple functions. As shown in Figure 22, it can be used to implement a “Powered from PoE” indicator using an LED with a series current limiting resistor connected to the VCC pin. This may be useful when the auxiliary power source is directly connected to the DC-DC converter stage, a situation known as “RAUX” (see Auxiliary Power Options below). In such a configuration, the nPGOOD pin will be active when the PD is operating from PoE power but not when it is powered from the auxiliary source. However, the “Powered from PoE” indicator is not applicable in systems implementing the front auxiliary power configuration “FAUX” (see Auxiliary Power Options below) because both PoE and auxiliary supply current pass through the hot swap MOSFET. In this configuration, the nPGOOD pin is active when either PoE power or auxiliary power is applied. The designer should ensure that the current drawn by the LED is not more than a few milliamps, as the V_{CC} regulator’s output current is limited to 15 mA and must also supply the LM5072’s bias current and external MOSFET’s gate charging current. Supplying an external V_{CC} that is higher than the regulated level with a bench supply is an easy way to measure VCC load during normal operation. It should also be noted that an external load on the V_{CC} line will increase the dropout voltage of the V_{CC} regulator. This may be a concern when operating from a low voltage rear auxiliary supply.

The nPGOOD pin can also be used to implement a delay timer by adding a capacitor from the nPGOOD pin to the ARTN pin. This delay timer will prevent the interruption of the PWM controller’s operation in the event of an intermittent loss of Power Good status. This can be caused by PoE line voltage transients that may occur when switching between normal PoE power and a backup supply system (e.g. a battery or UPS). This condition will create a new “hot swap” event if there is a voltage difference between the backup supply and PoE supply. Since the hot swap MOSFET will likely limit current during such a sudden input voltage change, the nPGOOD pin will momentarily switch to the ”pull up” state. A capacitor on this pin will delay the transition of the nPGOOD pin state in order to provide continuous operation of the PWM controller during such transients. The Power Good filter delay time and capacitor value can be selected with the following equation:

$$C_{PGOOD}(nF) = \frac{0.05mA + I_{LED\ (mA)}}{1mA} \times \frac{t_{PG\_Delay\ (ms)}}{0.25\ ms} \times 100\ nF \quad (3)$$

For example, selecting 1000 nF for C_{PGOOD}, the delay time will be 50 ms if no LED is used and about 0.83 ms when an LED, drawing 3 mA, is used. The delay required for continued operation will depend on the amplitude of the transient, the DC current limit, the load, and the total amount of input capacitance. Note that this delay does not ensure continued operation. If the hot swap MOSFET is in current limit for an extended period, it may cause a thermal limit condition. This will result in a complete shutdown of the switching regulator, though no elements in the system will be permanently damaged and normal operation will resume momentarily.

The Power Good status will also affect the default DC current limit. Should the sensed drain to source voltage of the hot swap MOSFET (from ARTN to V_{EE}) exceed 2.5V, the LM5072 will increase the DC current limit from the default 440 mA to 540 mA, thus allowing the PD to continue operation through the transient event. This higher current limit will remain in effect until one of the following events occur:

1. the duration of loss of Power Good status exceeds t_{PG_Delay}, at which time the PWM controller will be disabled,
2. the increased power dissipation in the hot swap MOSFET causes a thermal limit condition as previously discussed, or
3. the MOSFET drain to source voltage falls below 1.5V to re-establish Power Good status. Under this condition, the LM5072 will revert back to the default 440 mA DC current limit once Power Good status is restored. Note that if the DC current limit has been programmed externally with R_{DCCL} (see the DC Current Limit Programming section), the DC current limit will remain at the programmed level even when the Power Good status is lost.

Auxiliary Power Options

The LM5072 based PD can receive power from auxiliary sources like AC adapters and solar cells in addition to the PoE enabled network. This is a desirable feature when the total system power requirements exceed the PSE's load capacity. Furthermore, with the auxiliary power option the PD can be used in a standard Ethernet (non-PoE) system.

For maximum versatility, the LM5072 accepts two different auxiliary power configurations. The first one, shown in Figure 23, is the front auxiliary (FAUX) configuration in which the auxiliary source is "diode OR'd" with the PoE potential received from the Ethernet connector. The second configuration, shown in Figure 24, is the rear auxiliary (RAUX) option in which the auxiliary power bypasses the PoE interface and is connected directly to the input of the DC-DC converter through a diode. The FAUX option is desirable if the auxiliary power voltage is similar to the PoE input voltage. However, when the auxiliary supply voltage is much lower than the PoE input voltage, the RAUX option is more favorable because the current from the auxiliary supply is not limited by the hot swap MOSFET DC current limit. A comparison of the FAUX and RAUX options is presented in Table 3. Note the ICL_FAUX and RAUX pins are not reverse voltage protected. If complete reverse protection is desired, series blocking diodes are necessary.

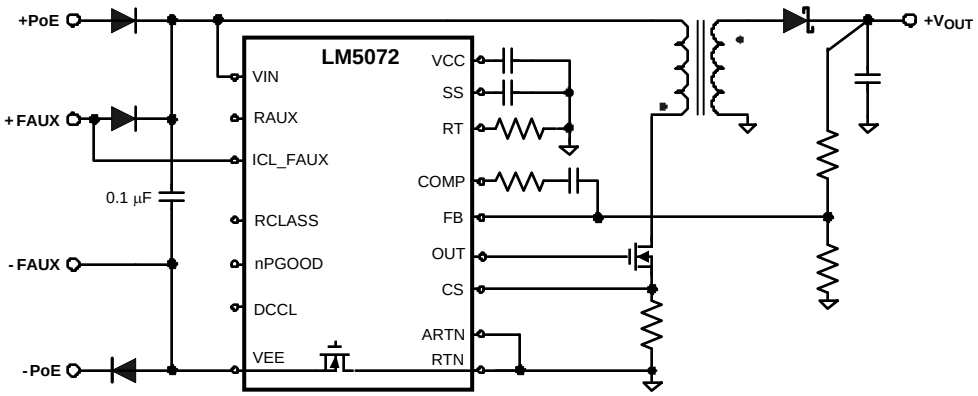


Figure 23. The FAUX Configuration

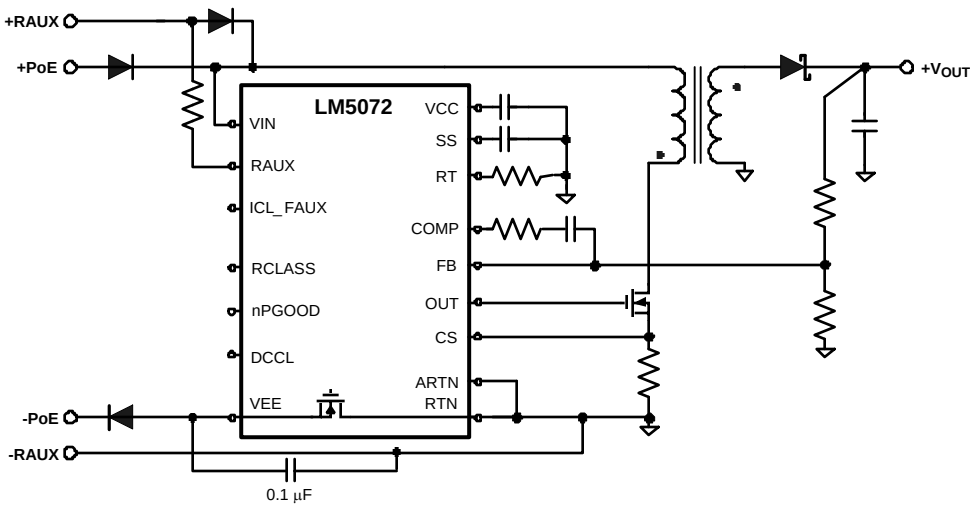


Figure 24. The RAUX Configuration

Table 3. Comparison Between FAUX and RAUX Operation

Tradeoff	FAUX Operation	RAUX Operation
Hot Swap Protection / Current Limit Protection	Automatically provided by the hot swap MOSFET.	Requires a series resistor to limit the inrush current during hot swap.
Minimum Auxiliary Voltage (at the IC pins)	Limited to 18V by the signature detection mode, or by the power requirement (current limit).	Only limited by 9V minimum input requirement.
Auxiliary Dominance Over PoE	Cannot be forced without external components.	Can be forced with appropriate RAUX pin configuration.
Use of nPGOOD Pin as “Powered from PoE” Indicator	Not applicable as power is delivered through the hot swap interface in both PoE and FAUX modes.	Supported.
Transient Protection	Excellent due to active MOSFET current limit.	Fair due to passive resistor current limit.

The term “Auxiliary Dominance” mentioned in Table 3 means that when the auxiliary power source is connected, it will always power the PD regardless of the state of PoE power. “Aux dominance” is achievable only with the RAUX option, as noted in the table.

If the PD is not designed for aux dominance, either the FAUX or RAUX power sources will deliver power to the PD only under the following two conditions:

1. If auxiliary power is applied before PoE power, it will prevent the PD’s detection by the PSE and will supply power indefinitely. This occurs because the PoE input bridge rectifiers will be reverse biased, so no detection signature will be observed. Under this condition, when the auxiliary supply is removed, power will not be maintained because it will take some time for the PSE to perform signature detection and classification before it will supply power.
2. If auxiliary power is applied after PoE power is already present but has a higher voltage than PoE, it may assume power delivery responsibility. Under the second case, if the supplied voltages are comparable, the load current may be shared inversely proportional to the respective output impedances of each supply. (The output impedance of the PSE supply is increased by the cable series resistance).

If PoE power is applied first and has a higher voltage than the non-dominant aux power source, it will continue powering the PD even when the aux power source becomes available. In this case, should PoE power be removed, the auxiliary source will assume power delivery and supply the DC-DC loads without interruption.

If either FAUX or RAUX power is supplied prior to PoE power, it will prevent the recognition of the PD by the PSE. Consequently, continuity of power delivery cannot be ensured because the PoE supply will not be present when auxiliary power is removed.

FAUX Option

With the FAUX option, the LM5072 hot swap MOSFET provides inrush and DC current limit protection for the auxiliary power source. To select the FAUX configuration for an auxiliary voltage lower than nominal PoE voltages, the ICL_FAUX pin must be forced above its high threshold to override the VIN UVLO function. Note that when the ICL_FAUX pin is pulled high to override VIN UVLO, it also overrides the inrush current limit programmed by R_{ICL}, if present. In this case, the inrush current will revert back to the default 150 mA limit.

Pulling up the ICL_FAUX pin will increase the default DC current limit to 540 mA. This increase in DC current limit is necessary because higher current is required to support the PD output power at the lower input potentials observed with auxiliary sources. In cases where the auxiliary supply voltage is comparable to the PoE voltage, there is no need to pull-up the ICL_FAUX pin to override VIN UVLO, and the default DC current limit remains at 440 mA. However, if the DC current limit is externally programmed with R_{DCCL}, the condition of the ICL_FAUX pin will not affect the programmed DC current limit. In other words, programmed DC current limit can be considered a “hard limit” that will not vary in any configuration.

RAUX Option

The RAUX option is desirable when the auxiliary supply voltage is significantly lower than the PoE voltage or when aux dominance is desired. The inrush and DC current limits of the LM5072 do not protect or limit the RAUX power source, and an additional resistor in the RAUX input path will be needed to provide transient protection.

To select the RAUX option without aux dominance, simply pull up the RAUX pin to the auxiliary power supply voltage through a high value resistor. Depending on the auxiliary supply voltage, the resistor value should be selected such that the current flowing into the RAUX pin is approximately 100 µA when the pin is mid-way between the lower and upper RAUX thresholds (approximately 4V). For example, with an 18V non-dominant rear auxiliary supply, the pull up resistor should be:

$$\frac{V_{AUX} - V_{RAUX}}{100\ \mu A} = \frac{18V - 4V}{100\ \mu A} = 140\ k\Omega \quad (4)$$

If the PSE load capacity is limited and insufficient, aux dominance will be a desired feature to off load PoE power for other PDs that do not have auxiliary power available. Aux dominance is achieved by pulling the RAUX pin up to the auxiliary supply voltage through a lower value (~5 kΩ) resistor that delivers at least 250 µA into the RAUX pin. When this higher RAUX current level is detected, the LM5072 shuts down the PD interface. In aux dominant mode, the auxiliary power source will supply the PD system as soon as it is applied. PD operation will not be interrupted when the aux power source is connected. The PoE source may or may not actually be removed by the PSE, although the DC current from the network cable is effectively reduced to zero (< 150 µA). IEEE 802.3af requires the AC input impedance to be greater than 2 MΩ to ensure PoE power removal. This condition is not satisfied when the auxiliary power source is applied. The PSE may remove power from a port based on the reduction in DC current. This is commonly known as DC Maintain Power Signature (DC MPS), a common feature in many PSE systems.

The high voltage startup regulator of the PWM controller does not have low dropout capability and will not be able to provide V_{CC} when the potential from VIN to RTN is less than 14.5V (no external V_{CC} load). In this case, the auxiliary voltage should supply V_{CC} directly via diode OR-ing to ensure successful startup.

When using the RAUX configuration, the positive potential connection of the 0.1 µF signature capacitor should be moved from VIN to RTN/ARTN as shown in Figure 24. This provides a high frequency, low impedance path for the IC's substrate during rear auxiliary operation. Placing the capacitor here will not affect signature mode.

It should be noted that rear auxiliary non-dominance does not imply PoE dominance. PoE dominance is difficult to achieve in any PoE system if continuity of power is desired. When the PoE voltage appears, the PSE and PD interface must continue delivering load current in addition to charging the input capacitor bank from the auxiliary voltage to the PoE voltage. The situation is further complicated by the fact that for a given delivered power level, the load current is much higher at the lower input voltages typically used in auxiliary supplies. As is the case during any inrush sequence, very high power is dissipated in the hot swap MOSFET. Consequently, attempting to achieve inrush completion while delivering load current is highly ill advised. Lastly, current delivered to the system may be limited by the PSE, the PD, or both.

A Note About FAUX and RAUX Pin False Input State Detection

The ICL_FAUX and RAUX pins are used to sense the presence of auxiliary power sources. The input voltage of each pin must remain low when the auxiliary power sources are absent. However, the Or-ing diodes feeding the auxiliary power are not ideal and leak reverse current that can flow from the PoE input to both the ICL_FAUX and RAUX pins. When PoE power is applied, these leakage currents may elevate the potentials of the ICL_FAUX and RAUX pins to false logic states.

One of two failure modes may be observed when the power diode feeding the front auxiliary input leaks excessively. First, the current may corrupt the inrush current limit programming, if that feature has been implemented. Second, the leakage current may elevate the voltage on the pin to the ICL_FAUX input threshold, which will force UVLO release. This would certainly interrupt any attempt by the LM5072 PD interface to perform the signature or classification functions.

When the power diode that feeds the rear auxiliary input leaks, the false signal could imply a rear auxiliary supply is present. In this case, the internal hot swap MOSFET will be turned off. This would of course block PoE power flow and cause the circuit to prevent startup.

This leakage problem at the control input pins can be easily solved. As shown in Figure 25, an additional pull-down resistor (Rpd) across each auxiliary power control input provides a path for the diode leakage current so that it will not create false states on the ICL_FAUX or RAUX pins.

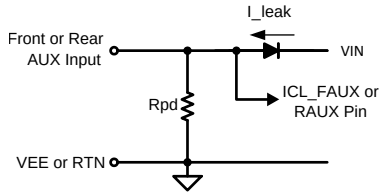


Figure 25. Bypassing Resistor – Prevents False ICL_FAUX and RAUX Pin Signaling

High Voltage Startup Regulator

The LM5072 contains a startup bias regulator that allows the VIN pin to be connected directly to PoE network voltages as high as 100V. The regulator output is connected to the VCC pin, providing an initial DC bias voltage of 7.7V nominal to start the PWM controller. The regulator is internally current limited to no less than 15 mA to prevent excessive power dissipation. For V_{CC} voltage stability and noise immunity, a capacitor ranging between 0.1 µF to 10 µF is required between the VCC and ARTN pins. Though the current capability of the regulator exceeds the requirements of the IC, no external DC load drawing more than 3 mA should be applied to the output. A small amount of current for a “Powered from PoE” indicator LED (see Power Good and Regulator Startup section) is acceptable. After the DC-DC converter reaches steady state operation, the V_{CC} voltage is typically elevated by an auxiliary winding of the power transformer. The sustained V_{CC} voltage should be greater than 8.1V to ensure the current supplied by the startup regulator is reduced to zero. Increasing the VCC pin voltage above the regulation level of the startup regulator automatically disables the regulator, thus reducing the power dissipation inside the LM5072. The power savings can be significant as many high voltage MOSFETs require a relatively large amount of gate charge and the gate drive current adds directly to the V_{CC} current draw.

A V_{CC} under-voltage lock-out circuit monitors the V_{CC} voltage to prevent the PWM controller from operating as the V_{CC} voltage rises during startup or falls during shutdown. The PWM controller is enabled when the V_{CC} voltage rising edge exceeds 7.6V and disabled when the V_{CC} voltage falling edge drops below 6.25V.

Error Amplifier

The LM5072 contains a wide-bandwidth, high-gain error amplifier to regulate the output voltage in non-isolated applications. The amplifier’s non-inverting input is set to a fixed reference voltage of 1.25V, while the inverting input is connected to the FB pin. The open-drain output of the amplifier is connected to the COMP pin, which is pulled up internally through a 5 kΩ resistor to an internal 5V bias voltage. Feedback loop compensation can be easily implemented by placing the compensation network, represented by “Zcomp”, between the FB and COMP pins as shown in Figure 26.

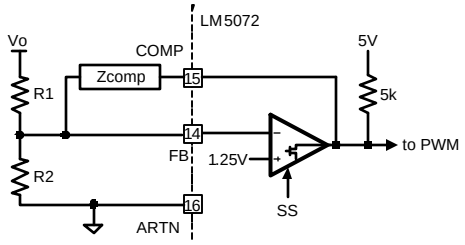


Figure 26. Internal Error Amplifier – Used for Non-isolated Output Applications

For isolated applications, the error amplifier function is located on the isolated secondary side. The LM5072's error amplifier can be disabled by connecting the FB pin to the ARTN pin. As shown in Figure 27, an opto-coupler is normally used to send the feedback signal across the isolation boundary to the COMP pin. The internal pull-up resistor on the COMP pin now serves as the pull-up bias for the opto-coupler transistor.

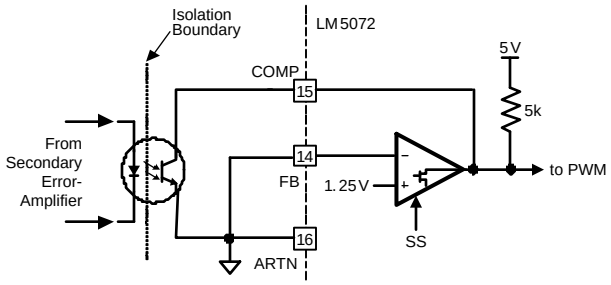


Figure 27. The Internal Error Amplifier – Bypassed in Isolated Output Applications

Current Sense and Limit

The LM5072 CS pin senses the transformer primary current signal for current mode control and current limiting of the supply. As shown in Figure 28, the current sense function can be fulfilled by a simple sense resistor R_{SENSE} inserted between the RTN and the source of the primary MOSFET switch.

The R_{SENSE} resistor should be non-inductive, and a low pass filter should be used to reject the switching noise on the sensed signal. A simple RC filter using 100Ω and 1 nF is typically sufficient. The filter capacitor must be located close to the CS and ARTN pins. In order to prevent noise propagation and to improve the noise immunity of the current sense, it is very important to minimize the return path of the current sense signal. This is accomplished with direct connection to the ARTN pin and a single point connection to the RTN pin on the PC Board layout.

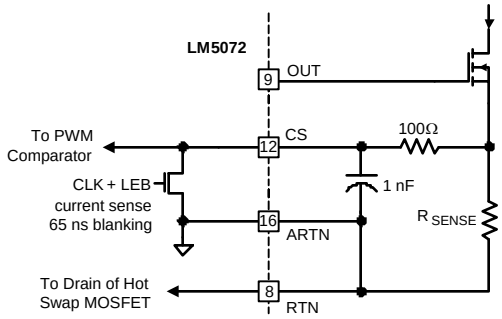


Figure 28. Current Sense Schemes

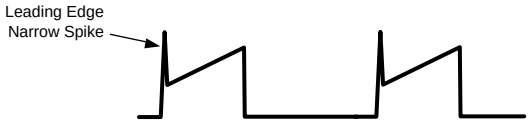


Figure 29. Typical Current Sense Waveform Having a Leading Edge Spike

The current sense signal is also used for cycle-by-cycle over-current protection. When the CS pin signal exceeds 0.5V, the PWM pulse of that cycle will be immediately terminated. The desired cycle-by-cycle over-current protection level is achieved by selecting the proper value of current sense resistor that produces 0.5V at the CS pin. For the LM5072-80, the slope compensation reduces the current limit threshold by about 20% maximum at the 80% maximum duty cycle.

The typical current sense waveform as shown in Figure 29 has a spike at the leading edge. This spike is mainly caused by the large gate drive current that flows through the current sense resistor at turn-on (up to 0.8A). The reverse recovery of the rectifier diode on the secondary side and the cross conduction of the primary MOSFET and sync MOSFET (if used) may also contribute to this leading edge spike. With a relatively small external RC filter, this spike can still cause a false over-current condition that terminates the PWM output pulse. To avoid this problem, an internal blanking circuit is provided within the LM5072 as shown in Figure 28. An internal MOSFET is turned on to short the CS pin to ARTN at the end of each cycle. This MOSFET switch remains on for an additional 65ns after the beginning of the next PWM cycle, thus blanking out the leading edge spike on the current sense signal.

Soft-Start

The LM5072 incorporates a soft-start feature which forces the PWM duty cycle to grow progressively during startup such that the output voltage increases gradually to the steady state level. The soft-start process reduces or prevents both the surge of inrush current and the associated overshoot of the output voltage during startup. The LM5072 achieves soft-start using an internal 10 µA current source to charge an external capacitor connected to the SS pin. The capacitor voltage limits the voltage at the COMP pin which directly controls the PWM duty cycle. The rate of the soft-start ramp can be adjusted by varying the value of the external capacitor. Note that the slope of the supply's output voltage is influenced by the load condition and the total output capacitance of the supply, as well as the soft-start programming. The supply should be started slowly enough such that the input current is limited below the hot swap MOSFET DC current limit.

Gate Driver and Maximum Duty Cycle Limit

The LM5072's gate drive (OUT) pin can source and sink a peak current of 800 mA directly to the gate of the DC-DC converter's power MOSFET switch. To serve a variety of applications, the LM5072 is available with two options for maximum PWM duty cycle. The LM5072-80 operates at duty cycles up to 80% while the LM5072-50 limits the PWM duty cycle to 50%.

Oscillator, Shutdown and Sync Capability

The LM5072 requires a single external resistor connected between the RT and ARTN pins to set the oscillator frequency (F_{OSC}). The R_T timing resistor should be located very close to the IC and connected directly to the RT and ARTN pins. The following equation describes the relationship between F_{OSC} and the R_T resistor value:

$$R_T(k\Omega) = \frac{200\ kHz}{F_{OSC}\ (kHz)} \times 26.2\ k\Omega \quad (5)$$

The LM5072 can also be synchronized to an external clock signal with a frequency higher than the programmed oscillator frequency determined by the R_T resistor. The clock signal should be coupled into the RT pin through a 100 pF capacitor, as shown in Figure 30. Successful synchronization requires the peak voltage of the sync pulse signal to be greater than 3.7V at the RT pin, and pulse width between 15 and 150 ns (set by external components). The R_T resistor is always required, whether the oscillator is operated in "free-running" mode or with external synchronization.

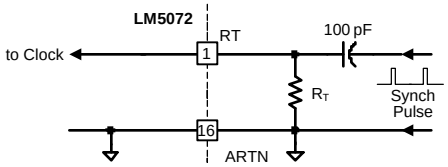


Figure 30. Oscillator Synchronization Implementation

Special attention should be paid to the relationship between the oscillator frequency and the PWM switching frequency. For the LM5072-50 version, the programmed oscillator frequency is internally divided by two in order to facilitate the 50% duty cycle limit. The PWM output switching frequency is therefore one half of the programmed oscillator frequency. The frequency divider is not used in the LM5072-80 and therefore the PWM output frequency is the same as the oscillator frequency. These relationships also apply to external synchronization frequency versus PWM output frequency.

PWM Comparator / Slope Compensation

The PWM comparator produces the PWM duty cycle by comparing the current sense ramp signal with an error voltage derived from the error amplifier output. The error amplifier output voltage at the COMP pin is offset by 1.4V and then further attenuated by a 3:1 resistor divider before it is presented to the PWM comparator input.

The PWM duty cycle increases with the voltage at the COMP pin. The controller output duty cycle reduces to zero when the COMP pin voltage drops below approximately 1.4V.

For duty cycles greater than 50%, current mode control loops are subject to sub-harmonic oscillation. This instability can be eliminated by adding an additional fixed slope voltage ramp signal to the current sense signal. This technique is commonly known as “slope compensation”. For the LM5072-80 version with its maximum duty cycle of 80%, slope compensation is integrated by injecting a 45 µA current ramp from the oscillator into the current sense signal path (see Figure 15). The 45 µA peak ramping current flows through an internal 2 kΩ resistor to produce a fixed voltage ramp at the PWM comparator input. Additional slope compensation may be added by increasing the source impedance of the current sense signal with an external resistor between the CS pin and the source of the current sense signal. The feature is disabled for the LM5072-50 version because the duty cycle is limited to 50% and slope compensation is not required.

Thermal Protection

The LM5072 includes internal thermal shutdown circuitry to protect the IC in the event the maximum junction temperature is exceeded. This circuit prevents catastrophic overheating due to accidental overload of the hot swap MOSFET or other circuitry. Typically, thermal shutdown is activated at 165°C, causing the hot swap MOSFET and classification regulator to be disabled. The PWM controller is disabled after the PGOOD timer has expired. Thermal limit is not enabled unless the module is being powered through the front end and the hot swap MOSFET is enhanced. V_{CC} current limit provides an adequate level of protection for this 15 mA regulator. The thermal protection is non-latching, therefore after the temperature drops by the 25°C nominal hysteresis, the hot swap MOSFET is re-activated and a soft-start is initiated to restore the LM5072 to normal operation. If the cause of overheating has not been eliminated, the circuit will hiccup in and out of the thermal shutdown mode.

PCB Layout Guidelines

Before processing the Printed Circuit Board (PCB) layout, the engineer should make all necessary adjustments to the schematic to suite the application. The reader may notice that the LM5072 evaluation board is designed with dual outputs, both FAUX and RAUX power options, and some re-configuration flexibility features (refer to Figure 32). However, many devices can be removed for a particular application. Recommendations on simplifying Figure 32 to suit a given application are as follows:

1. When selecting the FAUX power option only, delete C3, D1, D2, J3, P3, P4, R1, R2, R13, and R29.
2. When selecting the RAUX power option only, delete R30, D3, D7, J2, P1, P2 and R6.
3. When neither FAUX nor RAUX power options are selected, delete all the parts mentioned in (1) and (2) above.
4. When only a single output is required, delete C11 through C14, C17, D8, J6, J7, L2, R10 and Z4. Modify T1 design to delete the unwanted second output winding and increase the copper used for the single output

winding. This re-configuration should make use of the spare pins of the transformer.

5. R24 should be deleted from the schematic completely, being replaced by a short connection for an isolated application, or by an open for a non-isolated application.
6. Jumpers P5 and P6 (Figure 33) should be deleted from the schematic completely, being replaced by a short connection for an isolated application, or by an open for a non-isolated application.
7. When the output is non-isolated, delete C20, C22, C25, R7, R11, R16, R17, R24, U2, and U3. Replace C28 with a short connection, and replace P5 and P6 with short connections.
8. One may also modify the number of input and output capacitors to achieve a more optimized design.

Consider the following when starting the PCB design:

1. Try to use both sides of the PCB for part placement to facilitate both layout and routing.
2. Place the power components in a pattern that minimizes the lengths of the high current paths on the PCB.
3. Place the LM5072 and its critical peripheral parts closely. Bypass capacitors and transient protection elements should be near the LM5072.
4. Route the critical traces first, including both power and signal traces. Make the length of the trace as short as possible, and avoid excessive use of via holes.
5. Pay attention to grounding issues. Each reference ground should be a copper plane or island. Use via holes if necessary for direct connections of devices to their appropriate return ground plane or island. Identify the following ground returns:
   - Primary power return COM: C4, C5, C6, R14, R15, R29, C3, P4, J3-pins 2 and 3, U1-pin 8, C28, and C29 are all returned to the COM ground plane.
   - Primary control signal return, a ground return island: C19, T1-pin 2, C23, U2-pin 3, R24, C26, C21, and U1-pin 16 are all returned to this island, and the island should be single point connected to the COM ground plane.
   - Secondary power return IGND: T1-pins 6 and 7, C7 through C10, C12 through C17, C28, Z4, J5, and J7 are all returned to the IGND ground plane.
   - Secondary control signal return, a ground return island: R18, U3 and C20 are all returned to this island, and the island should be single point connected to the IGND ground plane.

Also consider the following during PCB layout and routing.

1. Place the following power components in each group as close as possible:
   - C4, C5 (if used), the primary winding of T1, Q1, and R14/R15. The high frequency switching current (pulse current) flows through these parts in a loop. The physical area enclosed by the loop should be as small as possible.
   - D5, C7 through C10, and the secondary winding of T1 for the main output. The high frequency switching current for the main output rail flows through these parts in a loop. The physical area enclosed by the loop should be as small as possible.
   - D8, C12 and C13, and the secondary winding of T1 for the second output, if used. The high frequency switching current for the second output rail flows through these parts in a loop. The physical area enclosed by the loop should be as small as possible.
   - L3, C15, C16, J4 and J5 (if posts are used). L3 should also be as close as possible to the capacitor bank consisting of C7 through C10 in order to minimize the conduction losses on the PCB. Ceramic capacitor C15 should be placed directly at the output port.
   - L2, C14, C17, Z4, J6 and J7 (if posts are used) for the second output rail. L2 should also be as close as possible to C12 and C13 in order to minimize the conduction losses on the PCB. Ceramic capacitor C14 should be directly placed at the output port
2. U1 (LM5072) should be placed close to Q1 in the orientation such that the gate drive output pin (OUT, Pin 9) is close to Q1's gate.
3. Z2 and C27 must be placed directly across the VIN and VEE pins for best protection against input transients. In a rear auxiliary application, C27 should be removed and C29 should be installed very close to the RTN and VEE pins.
4. C19 should be placed directly across the VCC and ARTN pins.
5. C23 should be placed directly across the CS and ARTN pins.
6. R21 should be placed directly across the RT and ARTN pins.

7. C26 should be placed directly across the SS and ARTN pins.
8. C21 should be placed directly across the nPGOOD and ARTN pins.
9. R25 should be directly routed from the output port.
10. R9 should be directly routed from R14/R15.
11. D6 and Z1 should be placed to achieve the shortest connection from C4 or C5 to the drain pad(s) of Q1 for better snubbing.
12. C2 and R4 should be placed to achieve the shortest connection across D5.
13. Q1, D5, D8, and U1 (LM5072) should be installed on thermal pads having adequate thermal vias down through all PCB Layers and an exposed thermal pad on the other side of the PCB.
14. Avoid spiral trace pattern.
15. Avoid placing switching traces near any traces in the regulator feedback loop.
16. Pay attention to trace width. Try to make the power traces as wide as possible. Conversely, do not make signal traces wider than needed.

After the first placement and routing is completed, make necessary modifications to optimize the design.

Application Example #1

Figure 31 shows an application example of a single isolated output solution for the PD. Both front auxiliary (FAUX) and rear auxiliary (RAUX) power options are given, although only one option may be needed in practice. Note that for the RAUX option, D2 is only installed when the supply voltage of the auxiliary power source would cause the V_{IN} voltage to be below 14.5V.

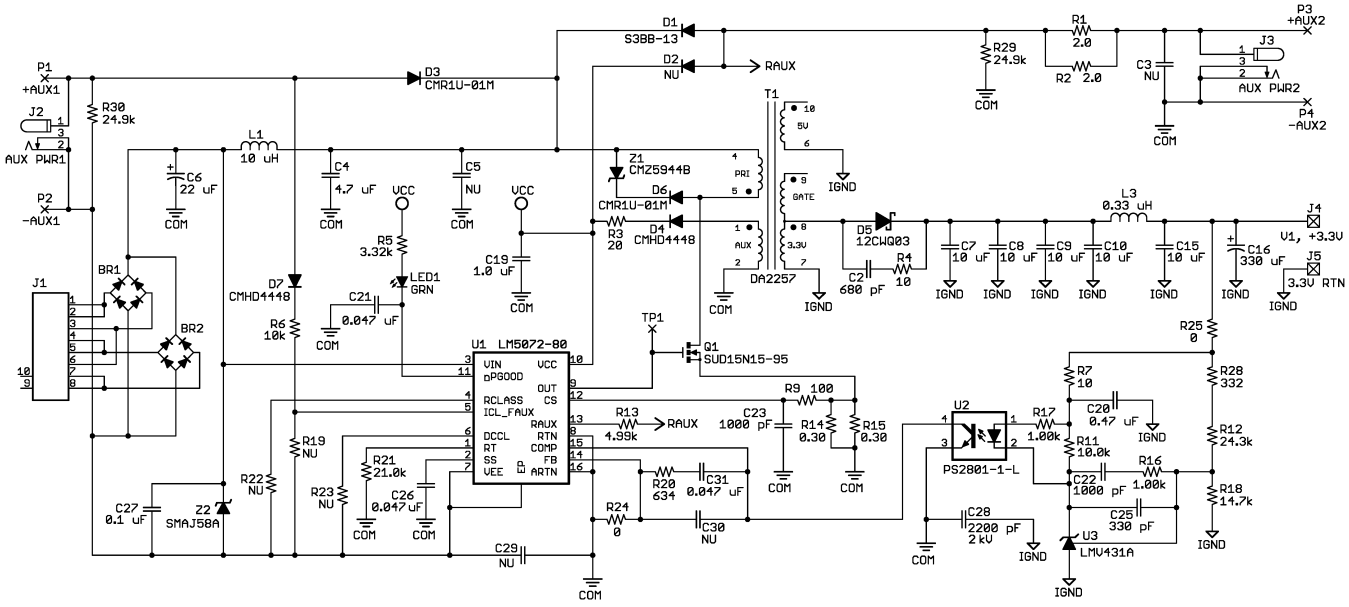


Figure 31. PD with Isolated, Single Output Solution

Application Example #2

Figure 32 shows an example of an isolated, dual-output solution for the PD. The 3.3V output is tightly regulated while the 5V output is cross-regulated. Both front auxiliary (FAUX) and rear auxiliary (RAUX) power options are given, although only one option may be needed in practice. Note that for the RAUX option, D2 is only installed when the supply voltage of the auxiliary power source is lower than 14.5V.

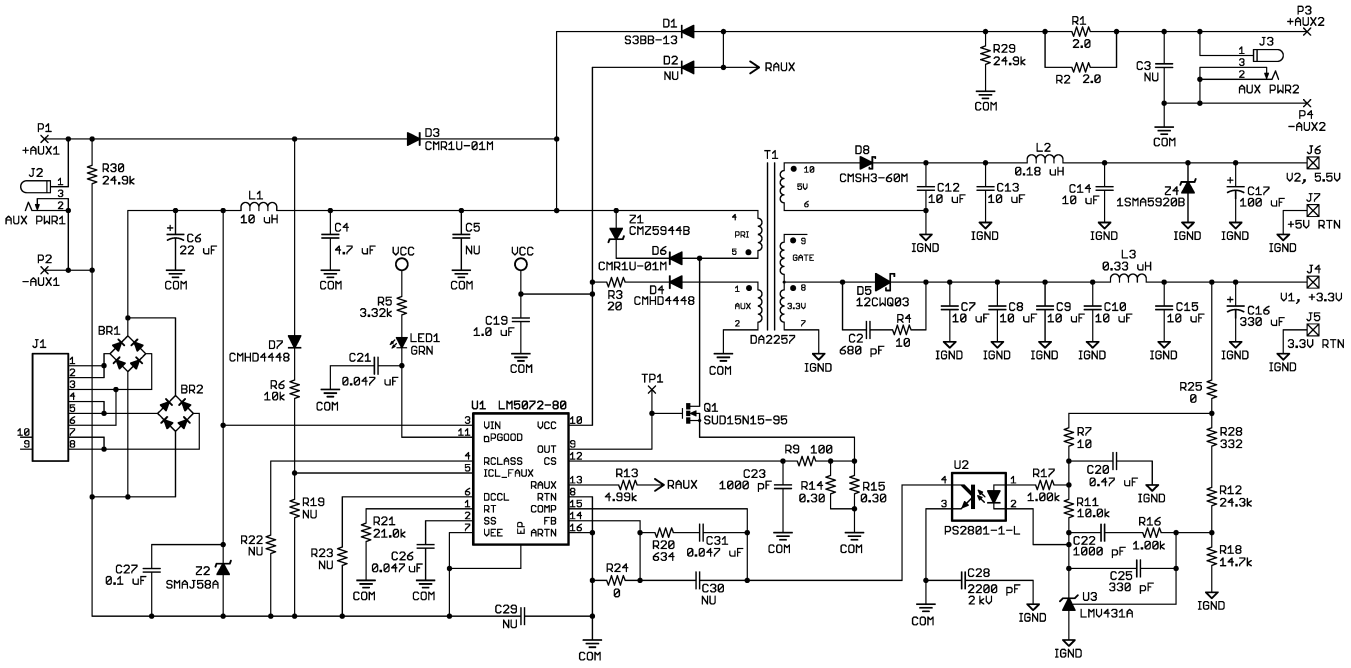


Figure 32. PD with Isolated, Dual Output Solution

Application Example #3:

Figure 33 shows an application example of the non-isolated version of Figure 31. This non-isolated version saves many parts used in the isolated feedback example shown in Figure 31. Similar simplification also applies to the non-isolated version of Figure 32.

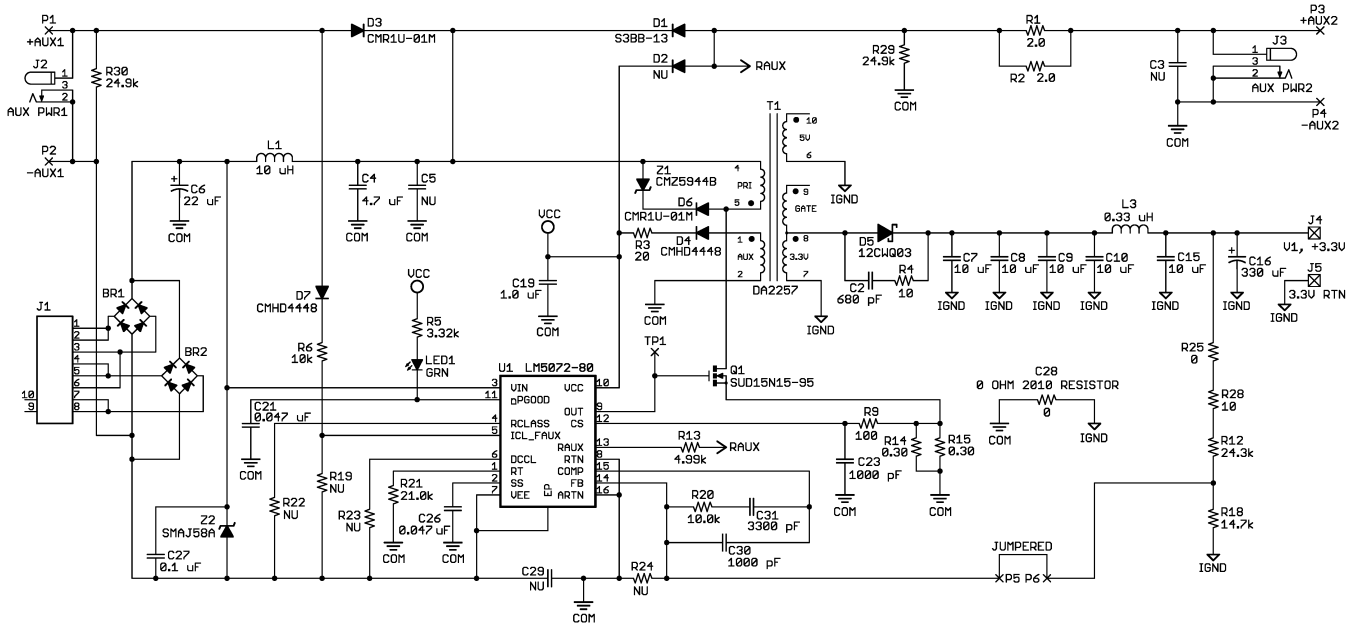


Figure 33. PD Solution with Non-Isolated Flyback Topology

Application Example #4

Figure 34 shows an application example of a PD solution using the buck topology. Q2, a dual PNP transistor, is employed in the output voltage sensing to achieve temperature compensation for the regulated output.

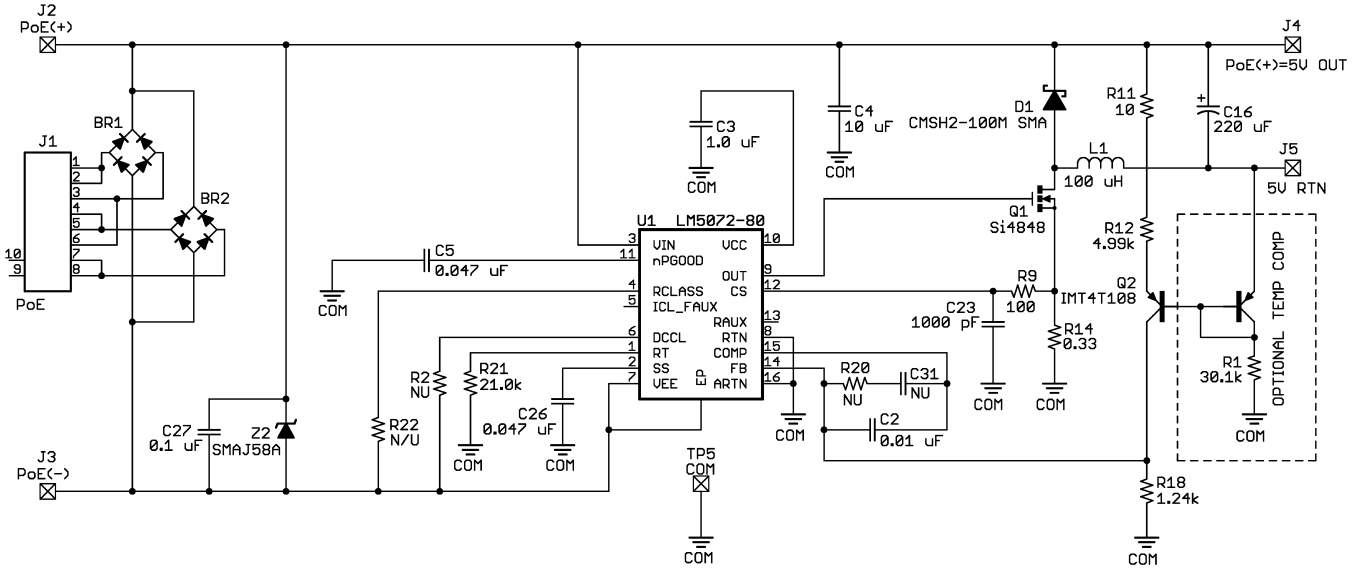


Figure 34. PD Solution with Buck Topology

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	27

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5072MH-80/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5072 MH-80	Samples
LM5072MHX-80/NOPB	ACTIVE	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5072 MH-80	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

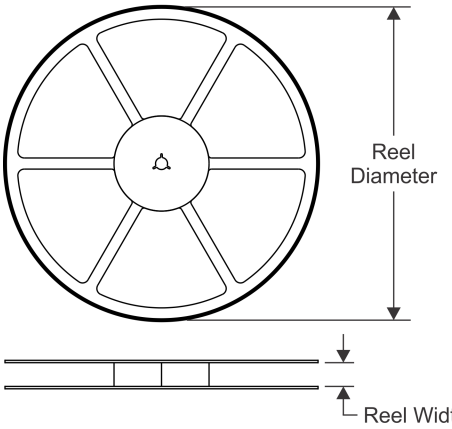
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

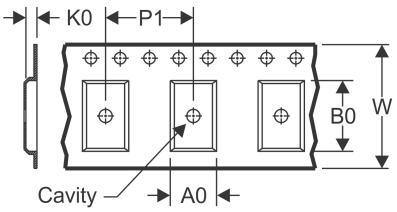
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

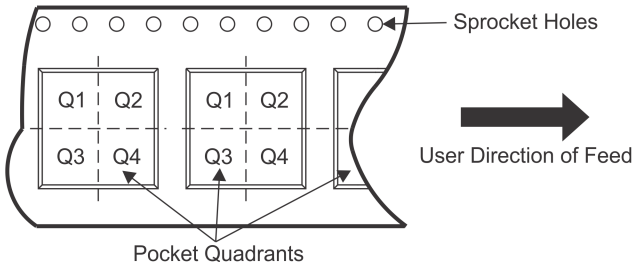


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

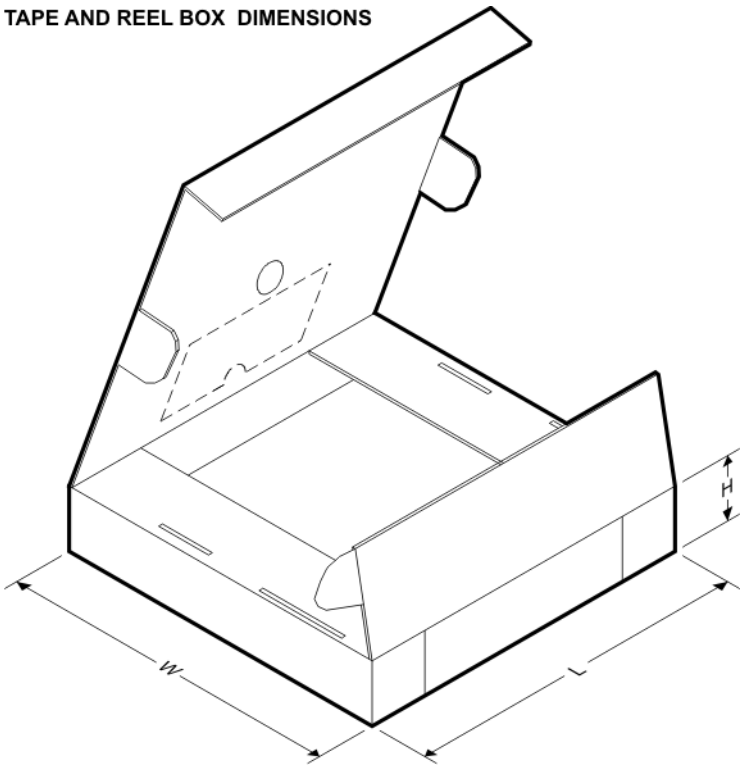
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

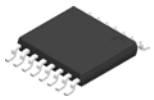
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5072MHX-80/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5072MHX-80/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0

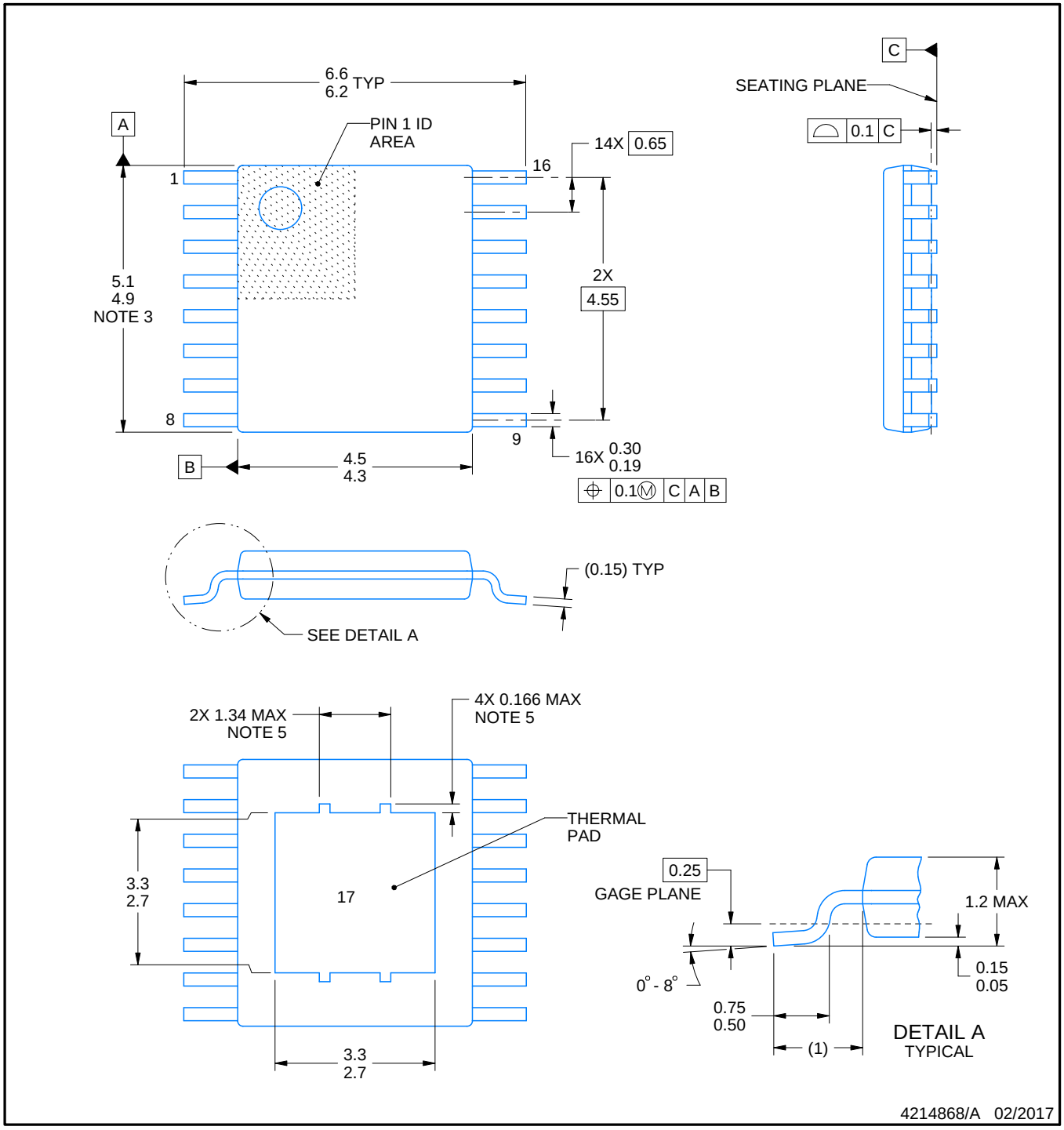


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

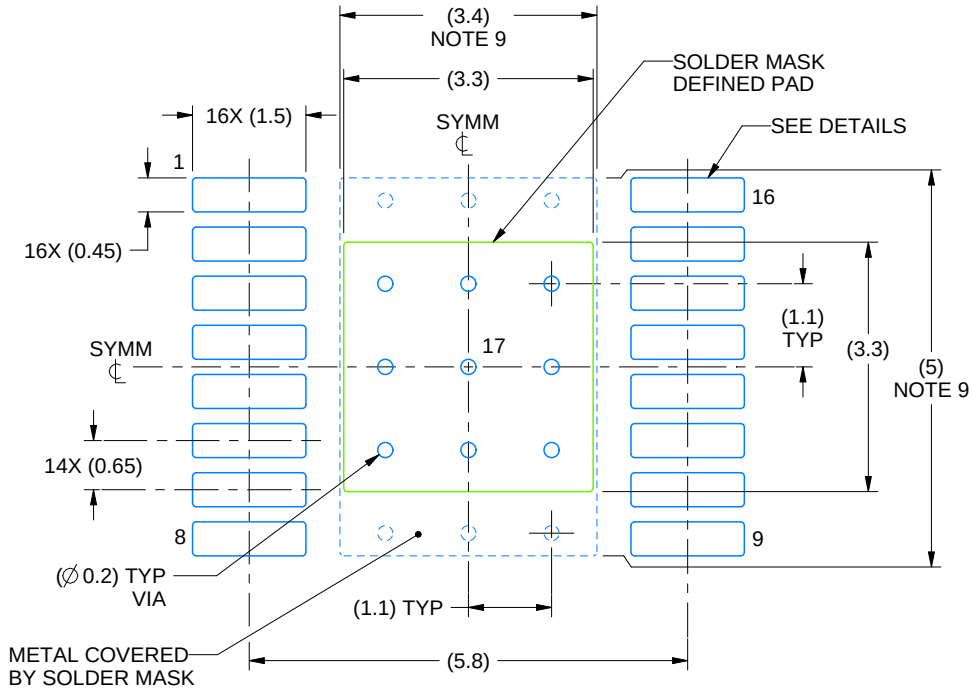
PLASTIC SMALL OUTLINE



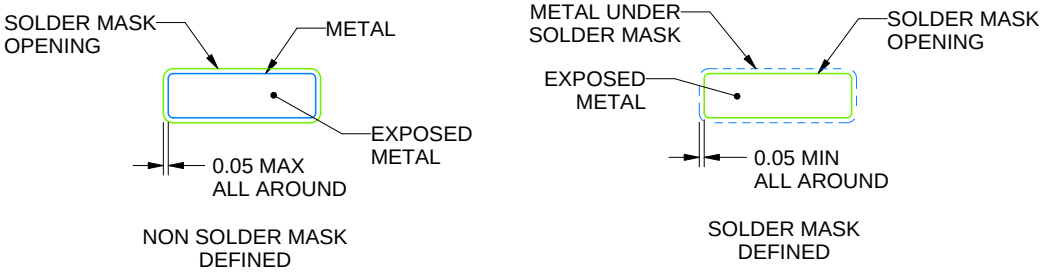
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

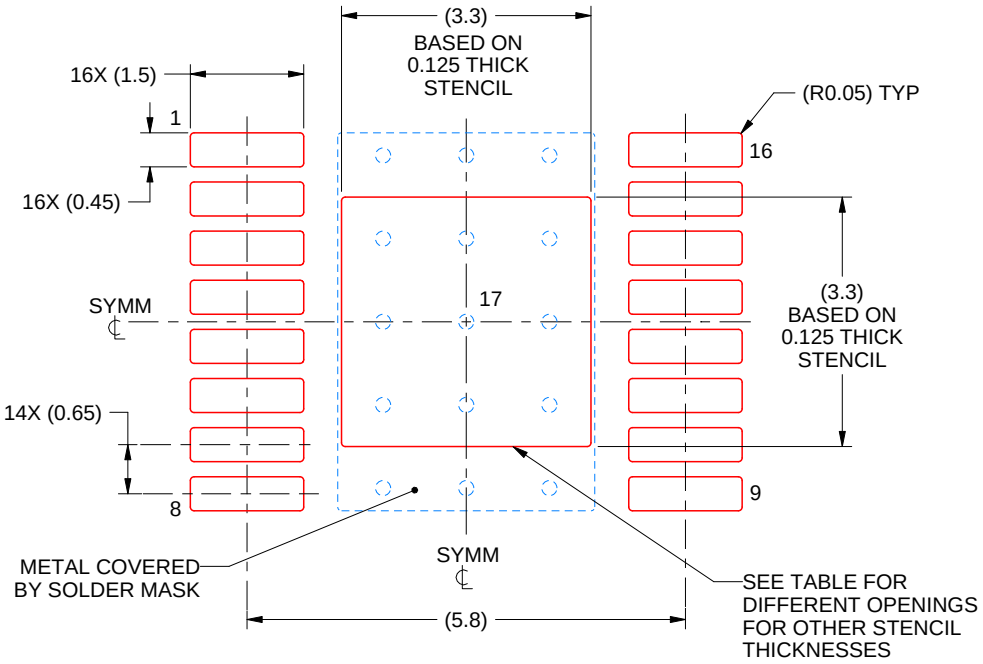


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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