THE DATASHEET OF

LM4935RLX

LM4935 Boomer™ Audio Power Amplifier Series Audio Sub-System with Dual-Mode Stereo Headphone & Mono High Efficiency Loudspeaker Amplifiers and Multi-Purpose ADC

Check for Samples: LM4935, LM4935RLEVAL

1 Introduction

1.1 Features

- 18-Bit Stereo DAC
- 16-Bit Mono ADC
- 12-Bit 4 Input Multipurpose SAR ADC
- 8 kHz to 48 kHz Stereo Audio Playback
- 8 kHz to 48 kHz Mono Recording
- 1 Hz to 13.888 kHz Sample Rate on all 4 SAR Channels
- Bidirectional PCM/I^2S Compatible Audio Interface
- Sigma-Delta PLL for Operation from any Clock at any Sample Rate
- Low Power Clock Network Operation if 12 MHz System Clock is Available
- Read/write I^2C or SPI Compatible Control Interface
- 33mW Stereo Headphone Amplifier at 3.3V
- OCL or AC-coupled Headphone Operation
- Automatic Headphone & Microphone Detection
- Support for Internal and External Microphones
- Automatic Gain Control for Microphone Input
- High Efficiency BTL 8Ω Amplifier, 600 mW @ 3.3V
- 115 mW Earpiece Amplifier at 3.3V
- Differential Audio I/O for External Cellphone Module
- Mono Differential Auxiliary Output
- Stereo Auxiliary Inputs
- Differential Microphone Input for Internal Microphone
- Flexible Audio Routing from Input to Output
- 32 Step Volume Control for Mixers with 1.5 dB Steps
- 16 Step Volume Control for Microphone in 2 dB Steps
- Programmable Sidetone Attenuation in 3 dB Steps
- DC Volume Control
- Two Configurable GPIO Ports
- Programmable Voltage Triggers on SAR Channels
- Multi-function IRQ Output
- Micro-power Shutdown Mode
- Available in the 4 x 4 mm 49-Bump DSBGA Package

1.2 Key Specifications

- $P_{HP\ (AC\text{-}COUP)}$ @ A_V_{DD} = 3.3V, 32Ω, 1% THD: 33 mW
- $P_{HP\ (OCL)}$ @ A_V_{DD} = 3.3V, 32Ω, 1% THD: 31 mW
- P_{LS} @ LS_V_{DD} = 5V, 8Ω, 1% THD: 1.3 W
- P_{LS} @ LS_V_{DD} = 4.2V, 8Ω, 1% THD: 900 mW
- Supply Voltage Range
  - BB_V_{DD} = 1.8V to 4.5V,
  - D_V_{DD} & PLL_V_{DD} = 2.7V to 4.5V
  - LS_V_{DD} & A_V_{DD} = 2.7V to 5.5V
- P_{LS} @ LS_V_{DD} = 3.3V, 8Ω, 1% THD: 600 mW
- Shutdown Current: 1.1 µA
- PSRR @ 217 Hz, A_V_{DD} = 3.3V, (Headphone): 60 dB
- SNR (Stereo DAC to AUXOUT): 88 dB (typ)
- SNR (Mono ADC from Cell Phone In): 90 dB (typ)
- SNR (Aux In to Headphones): 98 dB (typ)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Boomer is a trademark of Texas Instruments.
I^2C is a trademark of NXP.
All other trademarks are the property of their respective owners.
Boomer is a trademark of Texas Instruments.
I^2C is a trademark of NXP.
All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2005–2013, Texas Instruments Incorporated

1.3 Applications

- **Smartphones**
- **Mobile Phones and Multimedia Terminals**
- **PDAs, Internet Appliances and Portable Gaming**
- **Portable DVD/CD/AAC/MP3 Players**
- **Digital Cameras/Camcorders**

1.4 Description

The LM4935 is an integrated audio subsystem that supports both analog and digital audio functions. The LM4935 includes a high quality stereo DAC, a mono ADC, a multi-purpose SAR ADC, a stereo headphone amplifier, which supports output cap-less (OCL) or AC-coupled (SE)modes of operation, a mono earpiece amplifier and a mono high efficiency loudspeaker amplifier. It is designed for demanding applications in mobile phones and other portable devices.

The LM4935 features a bi-directional I^2S serial interface for full range audio and an I^2C™ or SPI compatible interface for control. The stereo DAC path features an SNR of 88 dB with an 18-bit 48 kHz input. In SE mode the headphone amplifier delivers at least 33 mW_{RMS} to a 32Ω single-ended stereo load with less than 1% distortion (THD+N) when A_V_{DD} = 3.3V. The mono earpiece amplifier delivers at least 115 mW_{RMS} to a 32Ω bridged-tied load with less than 1% distortion (THD+N) when A_V_{DD} = 3.3V. The mono speaker amplifier delivers up to 600 mW into an 8Ω load with less than 1% distortion when LS_V_{DD} = 3.3V and up to 1.3W when LS_V_{DD} = 5.0V. The LM4935 also contains a general purpose SAR ADC for housekeeping duties such as battery and temperature monitoring. This can also be used for analog volume control of the output stages and can trigger interrupt events.

The LM4935 employs advanced techniques to reduce power consumption, to reduce controller overhead to speed development time and to eliminate click and pop. Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. It is therefore ideally suited for mobile phone and other low voltage applications where minimal power consumption, PCB area and cost are primary requirements.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Copyright © 2005–2013, Texas Instruments Incorporated

1 Introduction **1**
1.1 Features 1
1.2 Key Specifications 1
1.3 Applications 2
1.4 Description 2
2 Device Information **4**
2.1 LM4935 Overview 4
2.2 Typical Application 5
2.3 Connection Diagrams 5
2.4 PIN TYPE DEFINITIONS 7
3 Electrical Specifications **8**
3.1 Absolute Maximum Ratings 8
3.2 Operating Ratings 8
3.3 Electrical Characteristics 9
4 Application Information **15**
4.1 System Control 15
4.2 Status & Control Registers 18
5 Typical Performance Characteristics **46**
6 Board Schematic Diagrams **82**
6.1 LM4935 Demonstration Board Schematic Diagram 82
6.2 Demoboard PCB Layout 82
6.3 Product Status Definitions 84
6.4 Revision History 85

Copyright © 2005–2013, Texas Instruments Incorporated

2 Device Information

2.1 LM4935 Overview

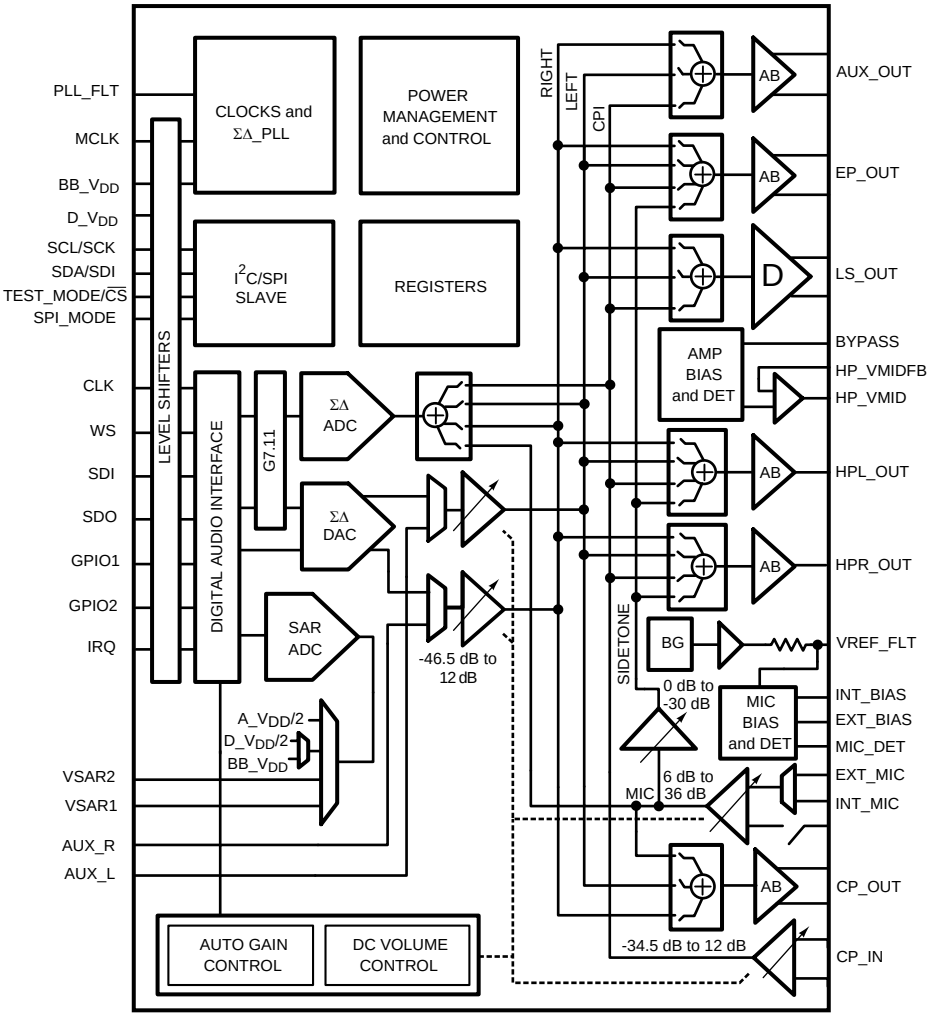


Figure 2-1. Conceptual Schematic

Copyright © 2005–2013, Texas Instruments Incorporated

2.2 Typical Application

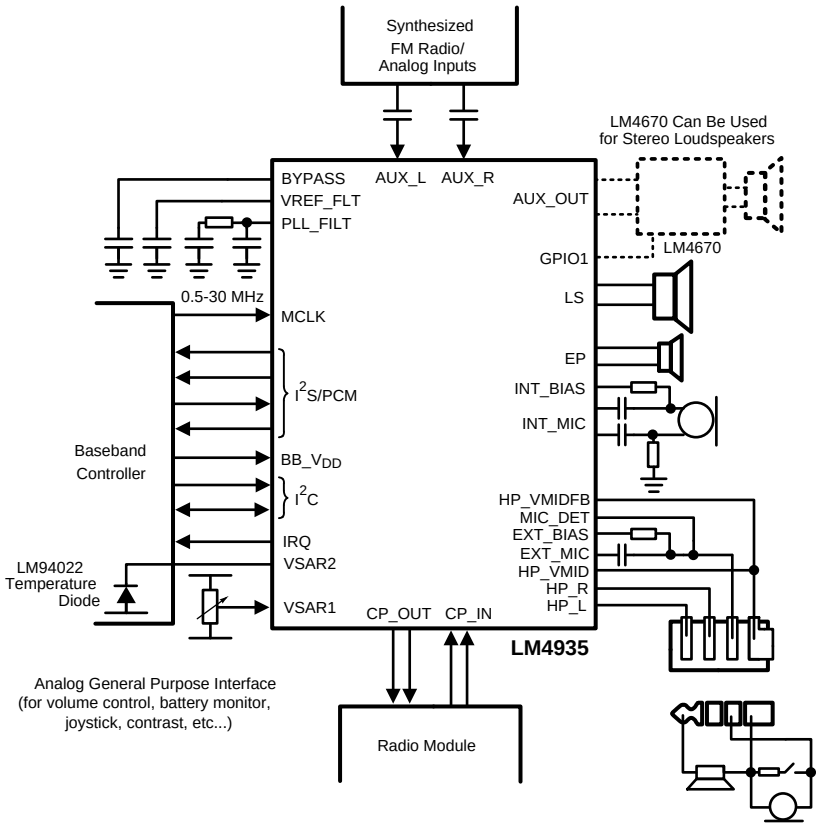


Figure 2-2. Example Application in Multimedia Mobile Phone

2.3 Connection Diagrams

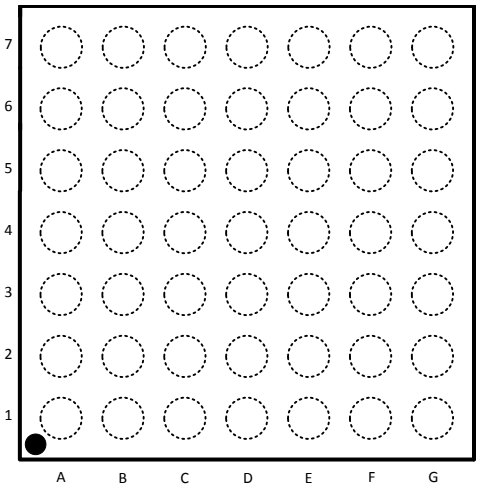


Figure 2-3. 49-Bump DSBGA (Top View) (Bump Side Down)
See YPG0049 Package

Table 2-1. PIN DESCRIPTIONS

Pin	Pin Name	Type	Direction	Description
A1	EP_NEG	Analog	Output	Earpiece negative output
A2	A_V_{DD}	Supply	Input	Headphone and mixer V_{DD}
A3	INT_MIC_POS	Analog	Input	Internal microphone positive input
A4	EXT_MIC	Analog	Input	External microphone input
A5	VSAR2	Analog	Input	Input to SAR channel 2
A6	VSAR1	Analog	Input	Input to SAR channel 1
A7	PLL_V_{SS}	Supply	Input	PLL V_{SS}
B1	A_V_{SS}	Supply	Input	Headphone and mixer V_{SS}
B2	EP_POS	Analog	Output	Earpiece positive output
B3	INT_MIC_NEG	Analog	Input	Internal microphone negative input
B4	BYPASS	Analog	Inout	A_V_{DD}/2 filter point
B5	TEST_MODE/$\overline{CS}$	Digital	Input	If SPI_MODE = 1, then this pin becomes $\overline{CS}$. If SPI_MODE = 0, and TEST_MODE/$\overline{CS}$ = 1, then this places the LM4935 into test mode.
B6	PLL_FILT	Analog	Inout	Filter point for PLL VCO input
B7	PLL_V_{DD}	Supply	Input	PLL V_{DD}
C1	HP_R	Analog	Output	Headphone Right Output
C2	EXT_BIAS	Analog	Output	External microphone supply (2.0/2.5/2.8/3.3V)
C3	INT_BIAS	Analog	Output	2.0V/2.5V ultra-clean supply for internal microphone
C4	AUX_R	Analog	Input	Right Analog Input
C5	GPIO_2	Digital	Inout	General Purpose I/O 2
C6	SDA	Digital	Inout	Control Data, I2C_SDA or SPI_SDI
C7	SCL	Digital	Input	Control Clock, I2C_SCL or SPI_SCK
D1	HP_L	Analog	Output	Headphone Left Output
D2	VREF_FLT	Analog	Inout	Filter point for the microphone power supply
D3	AUX_L	Analog	Input	Left Analog Input
D4	SPI_MODE	Digital	Input	Control mode select 1 = SPI, 0 = I2C (or test)
D5	GPIO_1	Digital	Inout	General Purpose I/O 1
D6	BB_V_{DD}	Supply	Input	Baseband V_{DD} for the digital I/Os
D7	D_V_{DD}	Supply	Input	Digital V_{DD}
E1	HP_VMID	Analog	Inout	Virtual Ground for Headphones in OCL mode, otherwise 1st headset detection input
E2	HP_VMID_FB	Analog	Inout	VMID Feedback in OCL mode, otherwise a 2nd headset detection input
E3	MIC_DET	Analog	Input	Headset insertion/removal and Microphone presence detection input
E4	CPI_NEG	Analog	Input	Cell Phone analog input negative
E5	IRQ	Digital	Output	Interrupt request signal (NOT open drain)
E6	I2S_SDO	Digital	Output	I2S Serial Data Out
E7	I2S_SDI	Digital	Input	I2S Serial Data Input
F1	LS_V_{DD}	Supply	Input	Loudspeaker V_{DD}
F2	LS_V_{DD}	Supply	Input	Loudspeaker V_{DD}
F3	CPI_POS	Analog	Input	Cell Phone analog input positive
F4	CPO_NEG	Analog	Output	Cell Phone analog output negative
F5	AUX_OUT_NEG	Analog	Output	Auxiliary analog output negative
F6	I2S_WS	Digital	Inout	I2S Word Select Signal (can be master or slave)
F7	I2S_CLK	Digital	Inout	I2S Clock Signal (can be master or slave)
G1	LS_POS	Analog	Output	Loudspeaker positive output
G2	LS_V_{SS}	Supply	Input	Loudspeaker V_{SS}
G3	LS_NEG	Analog	Output	Loudspeaker negative output

Copyright © 2005–2013, Texas Instruments Incorporated

Table 2-1. PIN DESCRIPTIONS (continued)

Pin	Pin Name	Type	Direction	Description
G4	CPO_POS	Analog	Output	Cell Phone analog output positive
G5	AUX_OUT_POS	Analog	Output	Auxiliary analog output positive
G6	D_V_{SS}	Supply	Input	Digital V_{SS}
G7	MCLK	Digital	Input	Input clock from 0.5 MHz to 30 MHz

2.4 PIN TYPE DEFINITIONS

Analog Input— A pin that is used by the analog and is never driven by the device. Supplies are part of this classification.

Analog Output— A pin that is driven by the device and should not be driven by external sources.

Analog Inout— A pin that is typically used for filtering a DC signal within the device, Passive components can be connected to these pins.

Digital Input— A pin that is used by the digital but is never driven.

Digital Output— A pin that is driven by the device and should not be driven by another device to avoid contention.

Digital Inout— A pin that is either open drain (I2C_SDA) or a bidirectional CMOS in/out. In the later case the direction is selected by a control register within the LM4935.

Copyright © 2005–2013, Texas Instruments Incorporated

3 Electrical Specifications

3.1 Absolute Maximum Ratings(1)(2)(3)

Analog Supply Voltage (A_V_{DD} & LS_V_{DD})		6.0V
Digital Supply Voltage (BB_V_{DD} & D_V_{DD} & PLL_V_{DD})		6.0V
Storage Temperature		−65°C to +150°C
Power Dissipation(4)		Internally Limited
ESD Susceptibility	Human Body Model(5)	2500V
	Machine Model(6)	200V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} – DSBGA (soldered down to PCB with $2in^2$ 1oz. copper plane)	60°C/W
Soldering Information		

(1) All voltages are measured with respect to the relevant V_{SS} pin unless otherwise specified. All grounds should be coupled as close as possible to the device.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation must be de-rated at elevated temperatures and is dictated by TJ_{MAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} – T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.
(5) Human body model: 100pF discharged through a 1.5kΩ resistor.
(6) Machine model: 220pF – 240pF discharged through all pins.

3.2 Operating Ratings

Temperature Range		−40°C to +85°C
Supply Voltage	D_V_{DD}/PLL_V_{DD}	2.7V to 4.5V
	BB_V_{DD}	1.8V to 4.5V
	LS_V_{DD}/A_V_{DD}	2.7V to 5.5V

Copyright © 2005–2013, Texas Instruments Incorporated

3.3 Electrical Characteristics[1][2][3]

Unless otherwise stated **PLL_V_{DD} = 3.3V, D_V_{DD} = 3.3V, BB_V_{DD} = 1.8V, A_V_{DD} = 3.3V, LS_V_{DD} = 3.3V.** The following specifications apply for the circuit shown in Figure 2-2 unless otherwise stated. Limits apply for 25°C.

Symbol	Parameter	Conditions	LM4935		Units
			Typical[4]	Limit[5]	
DC CURRENT CONSUMPTION					
DI_{SD}	Digital Shutdown Current[6]	Chip Mode '00', f_{MCLK} = 13MHz	0.7		µA
		Chip Mode '00', f_{MCLK} = 19.2MHz	0.7	5	µA (max)
DI_{ST}	Digital Standby Current	Chip Mode '01', f_{MCLK} = 13MHz	1.5		mA
		Chip Mode '01', f_{MCLK} = 19.2MHz	2.2	3	mA (max)
DI_{DD}	Digital Active Current	Chip Mode '10', f_{MCLK} = 13MHz, DAC, ADC, SAR OFF	1.5		mA
		Chip Mode '10', f_{MCLK} = 19.2MHz, DAC, ADC, SAR OFF	2.2		mA
		Chip Mode '10', f_{MCLK} = 13MHz DAC, ADC, SAR ON	11.2		mA
		Chip Mode '10', f_{MCLK} = 19.2MHz, DAC, ADC, SAR ON	16.2	20	mA (max)
AI_{SD}	Analog Shutdown Current	Chip Mode '00'	0.2	3	µA (max)
AI_{ST}	Analog Standby Current	Chip Mode '01', No headset inserted	0.2	3	µA (max)
AI_{DD}	Analog Active Current	All Outputs OFF, SE MODE	6.1		mA
		All Outputs OFF, OCL MODE	5.7		mA
		All Outputs ON, SE MODE	18.3		mA
		All Outputs ON, OCL MODE	18.7	28	mA (max)
$PLLI_{DD}$	PLL Active Current	f_{MCLK} = 13 MHz f_{PLLOUT} = 12 MHz, PLL ON only	4.2		mA
		f_{MCLK} = 19.2 MHz f_{PLLOUT} = 12 MHz, PLL ON only	6.2		mA
$ADCI_{DD}$	ADC Active Current	f_{MCLK} = 13MHz, ADC ON only	2.5		mA
		f_{MCLK} = 19.2MHz, ADC ON only	3.6		mA
$DACI_{DD}$	DAC Active Current	f_{MCLK} = 13MHz, DAC ON only; PLL OFF, f_S = 48kHz	7.4		mA
		f_{MCLK} = 19.2MHz, DAC ON only PLL OFF; f_S = 48kHz	10.7		mA
$SARI_{DD}$	SAR Active Current	f_{MCLK} = 13MHz, SAR ON only	1.6		mA
		f_{MCLK} = 19.2MHz, SAR ON only	2.3		mA
LSI_{DD}	Loudspeaker Quiescent Current	LS ON only	8.8		mA
HPI_{DD}	Headphone Quiescent Current	HP ON only, SE MODE	3.5		mA
		HP ON only, OCL MODE	3.9		mA
EPI_{DD}	Earpiece Quiescent Current	EP ON only	4.4		mA
$AUXI_{DD}$	AUXOUT Quiescent Current	AUXOUT ON only	4.8		mA
$CPOUTI_{DD}$	CPOUT Quiescent Current	CPOUT ON only	4.8		mA

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the relevant V_{SS} pin unless otherwise specified. All grounds should be coupled as close as possible to the device.
(3) Best operation is achieved by maintaining 3.0V < A_V_{DD} < 5.0 and 3.0V < D_V_{DD} < 3.6V and A_V_{DD} > D_V_{DD}.
(4) Typical values are measured at 25°C and represent the parametric norm.
(5) Limits are specified to AOQL (Average Outgoing Quality Level).
(6) Digital shutdown current is measured with system clock set for PLL output while the PLL is disabled.

Copyright © 2005–2013, Texas Instruments Incorporated

Electrical Characteristics[1][2][3] *(continued)*

Unless otherwise stated **PLL_V_{DD} = 3.3V, D_V_{DD} = 3.3V, BB_V_{DD} = 1.8V, A_V_{DD} = 3.3V, LS_V_{DD} = 3.3V.** The following specifications apply for the circuit shown in Figure 2-2 unless otherwise stated. Limits apply for 25°C.

Symbol	Parameter	Conditions	LM4935		Units
			Typical[4]	Limit[5]	
LOUDSPEAKER AMPLIFIER					
P_{LS}	Max Loudspeaker Power	8Ω load, LS_V_{DD} = 5V	1.3		W
		8Ω load, LS_V_{DD} = 4.2V	0.9		W
		8Ω load, LS_V_{DD} = 3.3V	0.6	0.44	W (min)
LS_{THD+N}	Loudspeaker Harmonic Distortion	8Ω load, LS_V_{DD} = 3.3V, P_O = 400mW	0.4		%
LS_{EFF}	Efficiency	0 dB Input MCLK = 12.000 MHz	84		%
$PSRR_{LS}$	Power Supply Rejection Ration (Loudspeaker)	AUX inputs terminated C_{BYPASS} = 1.0 µF V_{RIPPLE} = 200 mV_{P-P} f_{RIPPLE} = 217 Hz	54		dB
SNR_{LS}	Signal to Noise Ratio	From 0 dB Analog AUX input at 1 kHz, A-weighted	76		dB
e_N	Output Noise	A-weighted	350		µV
V_{OS}	Offset Voltage		7		mV
HEADPHONE AMPLIFIER					
P_{HP}	Headphone Power	32Ω load, 3.3V, SE	33	20	mW (min)
		16Ω load, 3.3V, SE	52		mW
		32Ω load, 3.3V, OCL, VCM = 1.5V	31		mW
		32Ω load, 3.3V, OCL, VCM = 1.2V	20		mW
		16Ω load, 3.3V, OCL, VCM = 1.5V	50		mW
		16Ω load, 3.3V, OCL, VCM = 1.2V	32		mW
$PSRR_{HP}$	Power Supply Rejection Ratio (Headphones)	AUX inputs terminated C_{BYPASS} = 1.0 µF V_{RIPPLE} = 200 mV_{P-P} f_{RIPPLE} = 217 Hz			
		SE Mode	60		dB
		OCL Mode VCM = 1.2V	68		dB
		OCL Mode VCM = 1.5V	65		dB
SNR_{HP}	Signal to Noise Ratio	From 0dB Analog AUX input A-weighted			
		SE Mode	98		dB
		OCL Mode VCM = 1.2V	97		dB
		OCL Mode VCM = 1.5V	96		dB
HP_{THD+N}	Headphone Harmonic Distortion	32Ω load, 3.3V, P_O = 7.5mW	0.05		%
e_N	Output Noise	A-weighted	12		µV
ΔA_{CH-CH}	Stereo Channel-to-Channel Gain Mismatch		0.3		dB
X_{TALK}	Stereo Crosstalk	SE Mode	61		dB
		OCL Mode	63		dB
EARPIECE AMPLIFIER					
P_{EP}	Earpiece Power	32Ω load, 3.3V	115	100	mW (min)
		16Ω load, 3.3V	150		mW

Copyright © 2005–2013, Texas Instruments Incorporated

Electrical Characteristics[1][2][3] *(continued)*

Unless otherwise stated **PLL_V_{DD} = 3.3V, D_V_{DD} = 3.3V, BB_V_{DD} = 1.8V, A_V_{DD} = 3.3V, LS_V_{DD} = 3.3V.** The following specifications apply for the circuit shown in Figure 2-2 unless otherwise stated. Limits apply for 25°C.

Symbol	Parameter	Conditions	LM4935		Units
			Typical[4]	Limit[5]	
$PSRR_{EP}$	Power Supply Rejection Ratio (Earpiece)	AUX inputs terminated C_{BYPASS} = 1.0 µF V_{RIPPLE} = 200 mV_{P-P} F_{RIPPLE} = 217 Hz	65		dB
SNR_{EP}	Signal to Noise Ratio	From 0dB Analog AUX input, A-weighted	98		dB
EP_{THD+N}	Earpiece Harmonic Distortion	32Ω load, 3.3V, P_O = 50mW	0.04		%
e_N	Output Noise	A-weighted	24		µV
V_{OS}	Offset Voltage		15		mV
AUXOUT AMPLIFIER					
THD+N	Total Harmonic Distortion + Noise	V_O = 1V_{RMS}, 5kΩ load	0.02		%
PSRR	Power Supply Rejection Ratio	AUX inputs terminated C_{BYPASS} = 1.0µF V_{RIPPLE} = 200mVPP f_{RIPPLE} = 217Hz	70		dB
CP_OUT AMPLIFIER					
THD+N	Total Harmonic Distortion + Noise	V_O = 1V_{RMS}, 5kΩ load	0.02		%
PSRR	Power SUpply Rejection Ratio	C_{BYPASS} = 1.0µF V_{RIPPLE} = 200mVPP f_{RIPPLE} = 217Hz	68		dB
MONO ADC					
R_{ADC}	ADC Ripple		±0.25		dB
PB_{ADC}	ADC Passband	Lower (HPF Mode 1), f_S = 8 kHz	300		Hz
		Upper	3470		Hz
SBA_{ADC}	ADC Stopband Attenuation	Above Passband	60		dB
		HPF Notch, 50 Hz/60 Hz (worst case)	58		dB
SNR_{ADC}	ADC Signal to Noise Ratio	From CPI, A-weighted	90		dB
ADC_{LEVEL}	ADC Full Scale Input Level		1		V_{RMS}
STEREO DAC					
R_{DAC}	DAC Ripple		0.1		dB
PB_{DAC}	DAC Passband		20		kHz
SBA_{DAC}	DAC Stopband Attenuation		70		dB
SNR_{DAC}	DAC Signal to Noise Ratio	A-weighted, AUXOUT	88		dB
DR_{DAC}	DAC Dynamic Range		96		dB
DAC_{LEVEL}	DAC Full Scale Output Level		1		V_{RMS}
PLL[7]					
F_{IN}	Input Frequency Range	Min	0.5		MHz
		Max	30		MHz
I2S/PCM					
f_{I2SCLK}	I2S CLK Frequency	f_S = 48kHz; 16 bit mode	1.536		MHz
		f_S = 48kHz; 25 bit mode	2.4		MHz
		f_S = 8kHz; 16 bit mode	0.256		MHz
		f_S = 8kHz; 25 bit mode	0.4		MHz
f_{PCMCLK}	PCM CLK Frequency	f_S = 48kHz; 16 bit mode	0.768		MHz
		f_S = 48kHz; 25 bit mode	1.2		MHz
		f_S = 8kHz; 16 bit mode	0.128		MHz
		f_S = 8kHz; 25 bit mode	0.2		MHz

(7) Disabling or bypassing the PLL will usually result in an improvement in noise measurements.

Copyright © 2005–2013, Texas Instruments Incorporated

Electrical Characteristics[1][2][3] *(continued)*

Unless otherwise stated **PLL_V_{DD} = 3.3V, D_V_{DD} = 3.3V, BB_V_{DD} = 1.8V, A_V_{DD} = 3.3V, LS_V_{DD} = 3.3V.** The following specifications apply for the circuit shown in Figure 2-2 unless otherwise stated. Limits apply for 25°C.

Symbol	Parameter	Conditions	LM4935		Units
			Typical[4]	Limit[5]	
DC_{I2S_CLK}	I2S_CLK Duty Cycle	Min		40	% (min)
		Max		60	% (max)
DC_{I2S_WS}	I2S_WS Duty Cycle		50		%
I2C					
T_{I2CSET}	I2C Data Setup Time	Refer to Section 4.1.5 for more details		100	ns (min)
$T_{I2CHOLD}$	I2C Data Hold Time	Refer to Section 4.1.5 for more details		300	ns (min)
SPI					
$T_{SPISETENB}$	Enable Setup Time			100	ns (min)
$T_{SPIHOLD-ENB}$	Enable Hold Time			100	ns (min)
$T_{SPISETD}$	Data Setup Time			100	ns (min)
$T_{SPIHOLDD}$	Data Hold Time			100	ns (min)
T_{SPICL}	Clock Low Time			500	ns (min)
T_{SPICH}	Clock High Time			500	ns (min)
VOLUME CONTROL					
VCR_{AUX}	AUX Volume Control Range	Minimum Gain w/ AUX_BOOST OFF	–46.5		dB
		Maximum Gain w/ AUX_BOOST OFF	0		dB
		Minimum Gain w/ AUX_BOOST ON	–34.5		dB
		Maximum Gain w/ AUX_BOOST ON	12		dB
VCR_{DAC}	DAC Volume Control Range	Minimum Gain w/ DAC_BOOST OFF	–46.5		dB
		Maximum Gain w/ DAC_BOOST OFF	0		dB
		Minimum Gain w/ DAC_BOOST ON	–34.5		dB
		Maximum Gain w/ DAC_BOOST ON	12		dB
VCR_{CPIN}	CPIN Volume Control Range	Minimum Gain	–34.5		dB
		Maximum Gain	12		dB
VCR_{MIC}	MIC Volume Control Range	Minimum Gain	6		dB
		Maximum Gain	36		dB
VCR_{SIDE}	SIDETONE Volume Control Range	Minimum Gain	–30		dB
		Maximum Gain	0		dB
SS_{AUX}	AUX VCR Stepsize		1.5		dB
SS_{DAC}	DAC VCR Stepsize		1.5		dB
SS_{CPIN}	CPIN VCR Stepsize		1.5		dB
SS_{MIC}	MIC VCR Stepsize		2		dB
SS_{SIDE}	SIDETONE VCR Stepsize		3		dB
AUDIO PATH GAIN W/ STEREO (bit 6 of 0x00h) ENABLED (AUX_L & AUX_R signals identical and selected onto mixer)					
	Loudspeaker Audio Path Gain	Minimum Gain from AUX input, BOOST OFF	–34.5		dB
		Maximum Gain from AUX input, BOOST OFF	12		dB
		Minimum Gain from CPI input	–22.5		dB
		Maximum Gain from CPI input	24		dB

Copyright © 2005–2013, Texas Instruments Incorporated

Electrical Characteristics[1][2][3] *(continued)*

Unless otherwise stated **PLL_V_{DD} = 3.3V, D_V_{DD} = 3.3V, BB_V_{DD} = 1.8V, A_V_{DD} = 3.3V, LS_V_{DD} = 3.3V.** The following specifications apply for the circuit shown in Figure 2-2 unless otherwise stated. Limits apply for 25°C.

Symbol	Parameter	Conditions	LM4935		Units
			Typical[4]	Limit[5]	
	Headphone Audio Path Gain	Minimum Gain from AUX input, BOOST OFF	–52.5		dB
		Maximum Gain from AUX input, BOOST OFF	–6		dB
		Minimum Gain from CPI input	–40.5		dB
		Maximum Gain from CPI input	6		dB
		Minimum Gain from MIC input using SIDETONE path w/ VCR_{MIC} gain = 6dB	–30		dB
		Maximum Gain from MIC input using SIDETONE path w/ VCR_{MIC} gain = 6dB	0		dB
	Earpiece Audio Path Gain	Minimum Gain from AUX input, BOOST OFF	–40.5		dB
		Maximum Gain from AUX input, BOOST OFF	6		dB
		Minimum Gain from CPI input	–28.5		dB
		Maximum Gain from CPI input	18		dB
		Minimum Gain from MIC input using SIDETONE path w/ VCR_{MIC} gain = 6dB	–18		dB
		Maximum Gain from MIC input using SIDETONE path w/ VCR_{MIC} gain = 6dB	12		dB
	AUXOUT Audio Path Gain	Minimum Gain from AUX input, BOOST OFF	–46.5		dB
		Maximum Gain from AUX input, BOOST OFF	0		dB
		Minimum Gain from CPI input	–34.5		dB
		Maximum Gain from CPI input	12		dB
	CPOUT Audio Path Gain	Minimum Gain from AUX input, BOOST OFF	–46.5		dB
		Maximum Gain from AUX input, BOOST OFF	0		dB
		Minimum Gain from MIC input	6		dB
		Maximum Gain from MIC input	36		dB
Total DC Power Dissipation					
	MP3 Mode Power Dissipation	DAC (f_S = 48kHz) and HP ON			
		f_{MCLK} = 12MHz, PLL OFF	57		mW
		f_{MCLK} = 13MHz, PLL ON f_{PLLOUT} = 12MHz	63		mW
		f_{MCLK} = 19.2MHz, PLL ON f_{PLLOUT} = 12MHz	64		mW
	FM Mode Power Dissipation	AUX Inputs selected and HP ON			
		f_{MCLK} = 12MHz, PLL OFF	24		mW
		f_{MCLK} = 13MHz, PLL OFF	25		mW
		f_{MCLK} = 19.2MHz, PLL OFF	27		mW
	VOICE CODEC Mode Power Dissipation	PCM DAC (f_S = 8kHz) + ADC (f_S = 8kHz) and EP ON			
		f_{MCLK} = 12MHz, PLL OFF	49		mW
		f_{MCLK} = 13MHz, PLL OFF	50		mW
		f_{MCLK} = 19.2MHz, PLL ON f_{PLLOUT} = 12MHz	56		mW

Copyright © 2005–2013, Texas Instruments Incorporated

Electrical Characteristics[1][2][3] *(continued)*

Unless otherwise stated **PLL_V_{DD} = 3.3V, D_V_{DD} = 3.3V, BB_V_{DD} = 1.8V, A_V_{DD} = 3.3V, LS_V_{DD} = 3.3V.** The following specifications apply for the circuit shown in Figure 2-2 unless otherwise stated. Limits apply for 25°C.

Symbol	Parameter	Conditions	LM4935		Units
			Typical[4]	Limit[5]	
	VOICE Module Mode Power Dissipation	CP IN selected. EP and CPOUT ON			
		f_{MCLK} = 12MHz, PLL OFF	30		mW
		f_{MCLK} = 13MHz, PLL OFF	31		mW
		f_{MCLK} = 19.2MHz, PLL OFF	33		mW

Copyright © 2005–2013, Texas Instruments Incorporated

4 Application Information

4.1 System Control

Method 1. I²C Compatible Interface

4.1.1 I²C SIGNALS

In I²C mode the LM4935 pin SCL is used for the I²C clock SCL and the pin SDA is used for the I²C data signal SDA. Both these signals need a pull-up resistor according to I²C specification. The I²C slave address for LM4935 is **0011010_2**.

4.1.2 I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW.

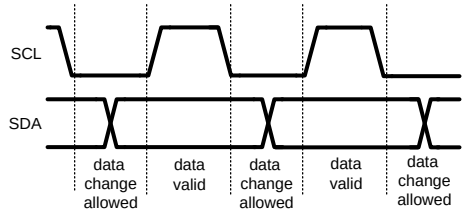
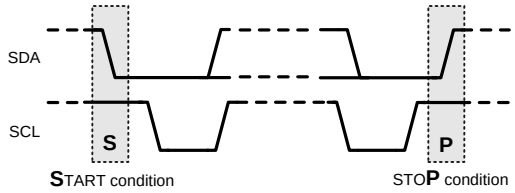


Figure 4-1. I²C Signals: Data Validity

4.1.3 I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



4.1.4 TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM4935 address is **0011010_2**. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

Copyright © 2005–2013, Texas Instruments Incorporated

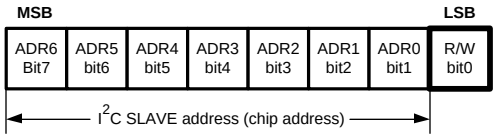
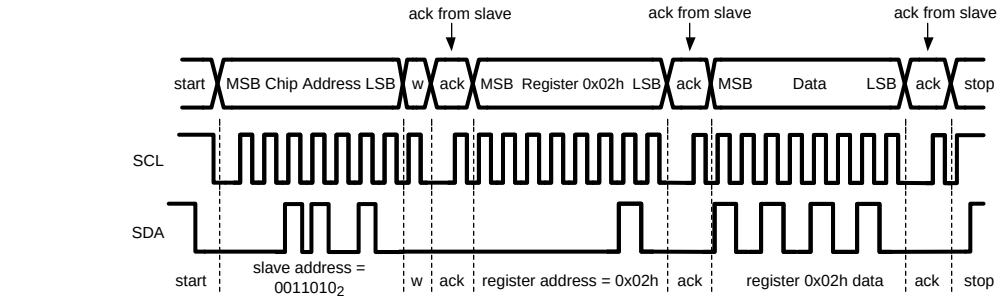


Figure 4-2. I²C Chip Address

Register changes take an effect at the SCL rising edge during the last ACK from slave.



w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled down by slave)
rs = repeated start

Figure 4-3. Example I²C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.

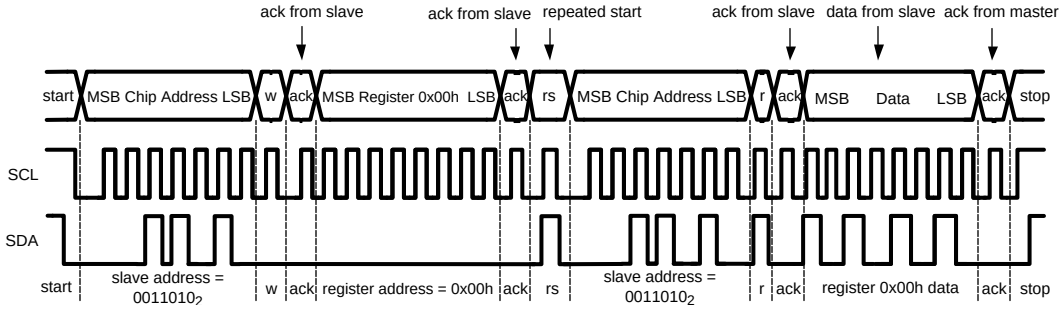


Figure 4-4. Example I²C Read Cycle

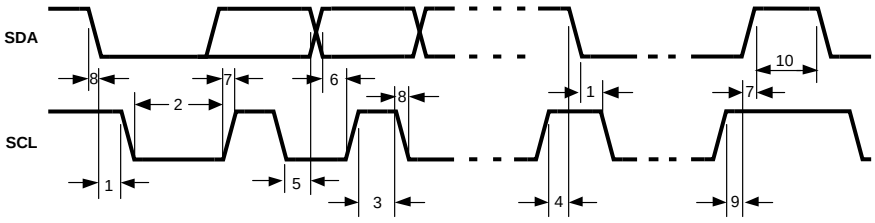


Figure 4-5. I²C Timing Diagram

4.1.5 I²C TIMING PARAMETERS

Symbol	Parameter	Limit		Units
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns

Copyright © 2005–2013, Texas Instruments Incorporated

5	Data Hold Time (Output direction, delay generated by LM4935)	300	900	ns
5	Data Hold Time (Input direction, delay generated by the Master)	0	900	ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	$20+0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15+0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load for Each Bus Line	10	200	pF

Method 2. SPI/Microwire Control/3–wire Control

The LM4935 can be controlled via a three wire interface consisting of a clock, data and an active low chip_select. To use this control method connect SPI_MODE to BB_V_{DD} and use TEST_MODE/$\overline{CS}$ as the chip_select as follows:

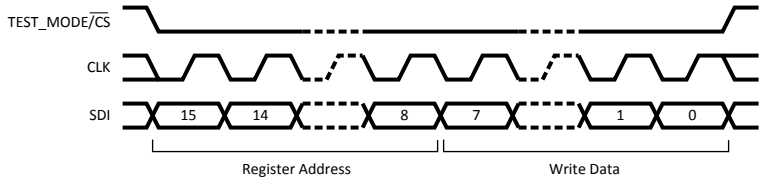


Figure 4-6. SPI Write Transaction

If the application requires read access to the register set; for example to determine the cause of an interrupt request or to read back a SAR data field, the GPIO2 pin can be configured as an SPI format serial data output by setting the GPIO_SEL in the GPIO configuration register (0x1Ah) to SPI_SDO. To perform a read rather than a write to a particular address the MSB of the register address field is set to a 1, this effectively mirrors the contents of the register field to read-only locations above 0x80h:

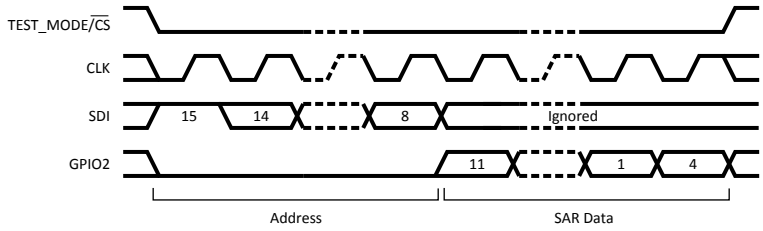


Figure 4-7. SPI Read Transaction

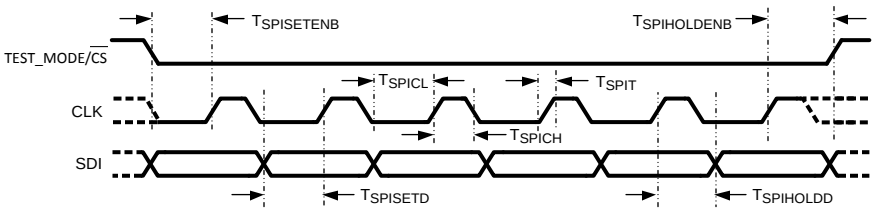


Figure 4-8. SPI Timing - Three Wire Mode Write Bus Timing

Copyright © 2005–2013, Texas Instruments Incorporated

4.2 Status & Control Registers

Table 4-1. Register Map

Address	Register	7	6	5	4	3	2	1	0
0x00h	BASIC	OCL	STEREO	CAP_SIZE		USE_OSC	PLL_ENB	CHP_MODE	
0x01h	CLOCKS	R_DIV						ADCLK	DACCLK
0x02h	PLL_M	PLLINPUT	PLL_M						RSVD
0x03h	PLL_N	PLL_N							
0x04h	PLL_P	RSVD	Q_DIV			PLL_P			RSVD
0x05h	PLL_MOD	RSVD	DITHER_LEVEL		PLL_N_MOD				
0x06h	ADC_1	HPF_MODE		SAMPLE_RATE		RIGHT	LEFT	CPI	MIC
0x07h	ADC_2	IF216	ADC_I2SM	AGC_FRAME_TIME			ADCMUTE	COMPND	U/ALAW
0x08h	AGC_1	NOISE_GATE_THRESHOLD			NG_ON	AGC_TARGET			AGC_ENB
0x09h	AGC_2	AGC_TIGHT	AGC_DECAY			AGC_MAX_GAIN			
0x0Ah	AGC_3	AGC_ATTACK			AGC_HOLD_TIME				
0x0Bh	MIC_1		INT_EXT	SE_DIFF	MUTE	PREAMP_GAIN			
0x0Ch	MIC_2			BTN_DEBOUNCE_TIME		BTNTYPE	MIC_BIAS_VOLTAGE		VCMVOLT
0x0Dh	SIDETONE					SIDETONE_ATTEN			
0x0Eh	CP_INPUT			MUTE	CPI_LEVEL				
0x0Fh	AUX_LEFT	AUX_DAC	MUTE	BOOST	AUX_LEFT_LEVEL				
0x10h	AUX_RIGHT	AUX_DAC	MUTE	BOOST	AUX_RIGHT_LEVEL				
0x11h	DAC	DACMUTE	BOOST	USAXLVL	DAC_LEVEL				
0x12h	CP_OUTPUT				MICGATE	MUTE	LEFT	RIGHT	MIC
0x13h	AUX OUTPUT					MUTE	LEFT	RIGHT	CPI
0x14h	LS_OUTPUT					MUTE	LEFT	RIGHT	CPI
0x15h	HP_OUTPUT				MUTE	LEFT	RIGHT	CPI	SIDE
0x16h	EP_OUTPUT				MUTE	LEFT	RIGHT	CPI	SIDE
0x17h	DETECT		HS_DBNC_TIME				TEMP_INT	BTN_INT	DET_INT
0x18h	STATUS	GPIN	TEMP	SARTRG2	SARTRG1	BTN	MIC	STEREO	HEADSET
0x19h	AUDIO_IF	I2S_SDO_DATA		PCMCLMS	PCMSYMS	I2SCLKMS	I2SWSMS	AUDIO_IF_MODE	
0x1Ah	GPIO	GPIODATA	PCM_LNG	I2S_MODE	SAR_CH_SEL		GPIO_SEL		
0x1Bh	SAR_SLT0/1	SLT1ENB	SLOT1_FS			SLT0ENB	SLOT0_FS		
0x1Ch	SAR_SLT2/3			SLT2VBB	SLT3ENB	SLT2ENB	SLOT2_FS		
0x1Dh	SAR_DATA_0	SLOT0_DATA							
0x1Eh	SAR_DATA_1	SLOT1_DATA							
0x1Fh	SAR_DATA_2	SLOT2_DATA							
0x20h	SAR_DATA_3	SLOT3_DATA							
0x21h	DC_VOL					MAX_LVL		EFFECT	DCVLENB
0x22h	TRIG_1	TRIG_1 [3:0]				SOURCE		DIR	ENB
0x23h	TRIG_1_MSB	TRIG_1 [11:4]							

Copyright © 2005–2013, Texas Instruments Incorporated

Table 4-1. Register Map (continued)

Address	Register	7	6	5	4	3	2	1	0
0x24h	TRIG_2	TRIG_2 [3:0]				SOURCE		DIR	ENB
0x25h	TRIG_2_MSB	TRIG_2 [11:4]							
0x26h	DEBUG	GPIO_TEST_MODE	RSVD	RSVD	RSVD	SOFT RESET	RSVD	RSVD	RSVD
For all registers, the default setting of data bits 7 through 0 are all set to zero.									
RESERVED bits should always be set to zero.									

4.2.1 BASIC CONFIGURATION REGISTER

This register is used to control the basic function of the chip.

Table 4-2. BASIC (0x00h)

Bits	Field	Description			
1:0	CHIP_MODE	The LM4935 can be placed in one of four modes which dictate its basic operation. When a new mode is selected the LM4935 will change operation silently and will re-configure the power management profile automatically. The modes are described as follows:			
		CHIP MODE	Audio System	Detection System	Typical Application
		00_2	Off	Off	Power-down Mode
		01_2	Off	On	Stand-by mode with headset event detection
		10_2	On	Off	Active without headset event detection
		11_2	On	On	Active with headset event detection
2	PLL_ENABLE	If set the PLL can be used.			
3	USE_OSC	If set the power management and control circuits will assume that no external clock is available and will resort to using an on-chip oscillator for SAR, headset detection and analog power management functions such as click and pop.			
5:4	CAP_SIZE	Programs the extra delays required to stabilize once charge/discharge is complete, based on the size of the bypass capacitor.			
		CAP_SIZE	Bypass Capacitor Size		Turn-off/on time
		00_2	0.1 µF		45 ms/75 ms
		01_2	1 µF		45 ms/140 ms
		10_2	2.2 µF		45 ms/260 ms
		11_2	4.7 µF		45 ms/500 ms
6	STEREO	If set, the mixers assume that the signals on the left and right internal busses are highly correlated and when these signals are combined their levels are reduced by 6 dB to allow enough headroom for them to be summed at the Loudspeaker, Earpiece, CPOUT, and AUXOUT amplifiers. For the Headphone amplifier, if this bit is set, the left and right signal levels are routed to the corresponding left or right headphone output; if this bit is cleared, the left and the right signals are added and routed to both headphone outputs and their levels are reduced by 6dB to allow enough headroom.			
7	OCL	If set the part is placed in OCL (Output Capacitor Less) mode.			

For reliable headset / push button detection the following bits should be defined before enabling the headset detection system by setting bit 0 of CHIP_MODE:

The OCL-bit (Cap / Capless headphone interface; bit 7 of this register)

The headset insert/removal debounce settings (bits 6:3 of DETECT (0x17h))

The BTN_TYPE-bit (Parallel / Series push button type; bit 3 MIC_2 register (0x0Ch))

The parallel push button debounce settings (bits 5:4 of MIC_2 register (0x0Ch))

All register fields controlling the audio system should be defined before setting bit 1 of CHIP_MODE and should not be altered while the audio sub-system is active.

Copyright © 2005–2013, Texas Instruments Incorporated

If the analog or digital levels are below −12 dB then it is not necessary to set the stereo bit allowing greater output levels to be obtained for such signals.

4.2.2 CLOCKS CONFIGURATION REGISTER

This register is used to control the clocks throughout the chip.

Table 4-3. CLOCKS (0x01h)

Bits	Field	Description	
0	DAC_CLK	Selects the clock to be used by the audio DAC system.	
		DAC_CLK	DAC Input Source
		0	PLL Input (MCLK or I2S_CLK)
		1	PLL Output
1	ADC_CLK	Selects the clock to be used by the audio ADC system.	
		ADC_CLK	Audio ADC Input Source
		0	MCLK
		1	PLL Output
7:2	R_DIV	Programs the R divider (divides from an expected 12.000 MHz input).	
		R_DIV	Divide Value
		0	Bypass
		1	Bypass
		2	1.5
		3	2
		4	2.5
		5	3
		6	3.5
		7	4
		8	4.5
		9	5
		10	5.5
		11	6
		12	6.5
		13 to 61	7 to 31
		62	31.5
		63	32

4.2.3 LM4935 CLOCK NETWORK

The audio ADC operates at 125*fs, so it requires a 1.000 MHz clock to sample at 8 kHz (at point **C** as marked on the following diagram). The stereo DAC operates at 250*fs, i.e. 12.000 MHz (at point **B**) for 48 kHz data. It is expected that the PLL is used to drive the audio system unless a 12.000 MHz master clock is supplied and the sample rate is always a multiple of 8 kHz, in which case the PLL can be bypassed to reduce power, clock division instead being performed by the Q and R dividers. The PLL can also use the I2S clock input as a source. In this case, the audio DAC uses the clock from the output of the PLL and the audio ADC either uses the PLL output divided by 2*FSDAC/FSADC or a system clock divided by Q, this allows n*8 kHz recording and 44.1 kHz playback.

MCLK must be less than or equal to 30 MHz, the I2S clock should be an integer multiple of the DAC's sampling frequency and should be below 6 MHz.

When using the Class D amplifier with the DAC the Class D clock generator will assume 12 MHz at point **A**, if this is not the case then the DAC and power stage may become unsynchronized and SNR performance may be reduced.

Copyright © 2005–2013, Texas Instruments Incorporated

The LM4935 is designed to work from a 12.000 MHz or 11.025 MHz clock at point **A**. This is used to drive the power management and control logic. Performance may not meet the electrical specifications if the frequency at this point deviates significantly beyond this range.

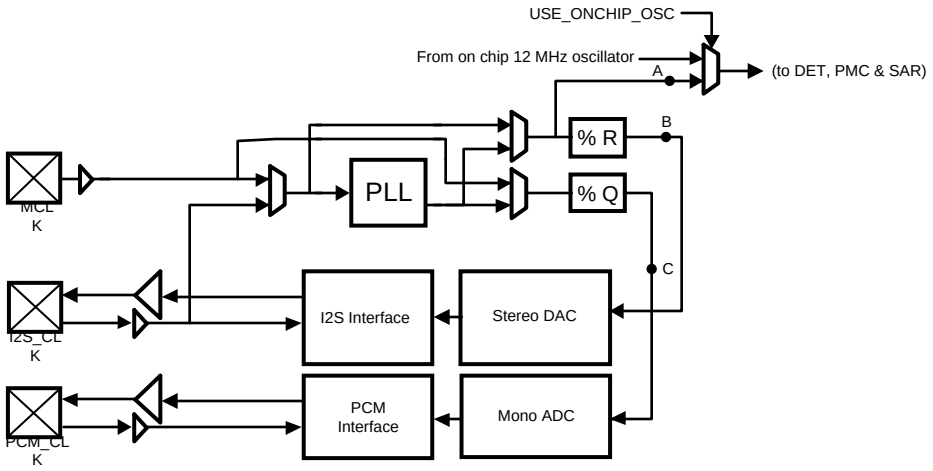


Figure 4-9. LM4935 Clock Network

4.2.4 COMMON CLOCK SETTINGS FOR THE DAC & ADC

The DAC has an over sampling rate of 125 but requires a 250*fs clock at point **B**. This allows a simple clocking solution as it will work from 12.000 MHz (common in most systems with Bluetooth or USB) at 48 kHz exactly, the following table describes the clock required at point **B** for various clock sample rates in the different DAC modes:

Table 4-4. Common DAC Clock Frequencies

DAC Sample Rate (kHz)	Clock Required at B (MHz)
8	2
11.025	2.75625
12	3
16	4
22.05	5.5125
24	6
32	8
44.1	11.025
48	12

The ADC has an over sampling ratio of 125 so the table below shows the required clock frequency at point **C**.

Copyright © 2005–2013, Texas Instruments Incorporated

Table 4-5. Common ADC Clock Frequencies

ADC Sample Rate (kHz)	Clock Required at C (MHz)
8	1
11.025	1.378125
12	1.5
16	2
22.05	2.75625
24	3

Methods for producing these clock frequencies are described in the PLL Section.

4.2.5 PLL M DIVIDER CONFIGURATION REGISTER

This register is used to control the input section of the PLL.

Table 4-6. PLL_M (0x02h)

Bits	Field	Description	
0	RSVD	RESERVED	
6:1	PLL_M	PLL_M	Input Divider Value
		0	1
		1	2
		2	3
		3	4
		4...62	5...63
		63	64
7	PLL_INPUT	Programs the PLL input multiplexer to select between:	
		PLL_INPUT	PLL Input Source
		0	MCLK
		1	I2S_CLK

The M divider should be set such that the output of the divider is between 0.5 MHz and 5 MHz.

The division of the M divider is derived from PLL_M such that:

$$M = PLL_M + 1 \quad (1)$$

NOTE

See Section 4.2.9 for more detail.

Copyright © 2005–2013, Texas Instruments Incorporated

4.2.6 PLL N DIVIDER CONFIGURATION REGISTER

This register is used to control the feedback divider of the PLL.

Table 4-7. PLL_N (0x03h)

Bits	Field	Description	
7:0	PLL_N	Programs the PLL feedback divider as follows:	
		PLL_N	Feedback Divider Value
		0 to 10	10
		11	11
		12	12
		13	13
		14	14
		…	…
		249	249
		250 to 255	250

The N divider should be set such that the output of the divider is between 0.5 MHz and 5 MHz. (Fin/M)*N will be the target resting VCO frequency, F_{VCO}. The N divider should be set such that 40 MHz < (Fin/M)*N < 60 MHz. Fin/M is often referred to as F_{comp} (comparison frequency) or F_{ref} (reference frequency), in this document F_{comp} is used.

The integer division of the N divider is derived from PLL_N such that:

For 9 < PLL_N < 251: N = PLL_N (2)

NOTE

See Section 4.2.9 for further details.

4.2.7 PLL P DIVIDER CONFIGURATION REGISTER

This register is used to control the output divider of the PLL.

Table 4-8. PLL_P (0x04h)

Bits	Field	Description	
0	RSVD	RESERVED	
3:1	PLL_P	PLL_P	Output Divider Value
		000_2	1
		001_2	2
		010_2	3
		011_2	4
		100_2	5
		101_2	6
		110_2	7
		111_2	8

Copyright © 2005–2013, Texas Instruments Incorporated

Table 4-8. PLL_P (0x04h) (continued)

Bits	Field	Description	
6:4	Q_DIV	Programs the Q Divider (divides from an expected 12.000 MHz input).	
		Q_DIV	Divide Value
		000_2	2
		001_2	3
		010_2	4
		011_2	6
		100_2	8
		101_2	10
		110_2	12
		111_2	13
7	RSVD	RESERVED	

The division of the P divider is derived from PLL_P such that:

$$P = PLL_P + 1 \quad (3)$$

NOTE

See Section 4.2.9 for more details.

4.2.8 PLL N MODULUS CONFIGURATION REGISTER

This register is used to control the modulation applied to the feedback divider of the PLL.

Table 4-9. PLL_N_MOD (0x05h)

Bits	Field	Description	
4:0	PLL_N_MOD	Programs the PLL N divider's fractional component:	
		PLL_N_MOD	Fractional Addition
		0	0/32
		1	1/32
		2 to 30	2/32 to 30/32
		31	31/32
6:5	DITHER_LEVEL	Allows control over the dither used by the N divider:	
		DITHER_LEVEL	Value
		00_2	Medium
		01_2	Small
		10_2	Large
		11_2	Off
7	RSVD	RESERVED	

The complete N divider is a fractional divider as such:

$$N = PLL_N + PLL_N_MOD/32 \quad (4)$$

If the modulus input is zero then the N divider is simply an integer N divider. The output from the PLL is determined by the following formula:

$$F_{out} = (F_{in}*N)/(M*P) \quad (5)$$

NOTE

See Section 4.2.9 for more details.

Copyright © 2005–2013, Texas Instruments Incorporated

4.2.9 FURTHER NOTES ON PLL PROGRAMMING

The sigma-delta PLL is designed to drive audio circuits requiring accurate clock frequencies of up to 30 MHz with frequency errors noise-shaped away from the audio band. The 5 bits of modulus control provide exact synchronization of 48 kHz and 44.1 kHz sample rates from any common system clock. In systems where an isochronous I2S data stream is the source of data to the DAC a clock synchronous to the sample rate should be used as input to the PLL (typically the I2S clock). If no isochronous source is available then the PLL can be used to obtain a clock that is accurate to within 1 Hz of the correct sample rate although this is highly unlikely to be a problem.

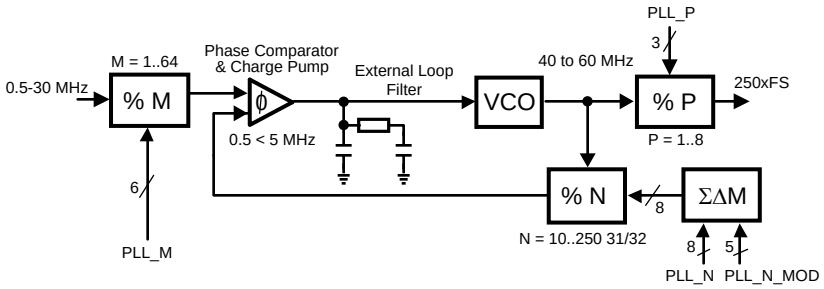


Figure 4-10. PLL Overview

Table 4-10. Example PLL Settings for 48 kHz and 44.1 kHz Sample Rates

F_{in} (MHz)	F_S (kHz)	M	N	P	PLL_M	PLL_N	PLL_N_MOD	PLL_P	F_{out} (MHz)
11	48	11	60	5	10	60	0	4	12
12.288	48	4	19.53125	5	3	19	17	4	12
13	48	13	60	5	12	60	0	4	12
14.4	48	9	37.5	5	8	37	16	4	12
16.2	48	27	100	5	26	100	0	4	12
16.8	48	14	50	5	13	50	0	4	12
19.2	48	13	40.625	5	12	40	20	4	12
19.44	48	27	100	6	26	100	0	5	12
19.68	48	21	64.03125	5	20	64	1	4	12
19.8	48	17	51.5	5	16	51	16	4	12
11	44.1	11	55.125	5	10	55	4	4	11.025
11.2896	44.1	8	39.0625	5	7	39	2	4	11.025
12	44.1	5	22.96875	5	4	22	31	4	11.025
13	44.1	13	55.125	5	12	55	4	4	11.025
14.4	44.1	12	45.9375	5	11	45	30	4	11.025
16.2	44.1	9	30.625	5	8	9	20	4	11.025
16.8	44.1	17	55.78125	5	16	30	25	4	11.025
19.2	44.1	16	45.9375	5	15	45	30	4	11.025
19.44	44.1	14	39.6875	5	13	39	22	4	11.025
19.68	44.1	21	47.0625	4	20	47	2	3	11.025
19.8	44.1	11	30.625	5	10	30	204	4	11.025

These tables cover the most common applications, obtaining clocks for derivative sample rates such as 22.05 kHz should be done by increasing the P divider value or using the R/Q dividers.

If the user needs to obtain a clock unrelated to those described above, the following method is advised. An example of obtaining 12.000 MHz from 1.536 MHz is shown below (this is typical for deriving DAC clocks from I2S datastreams).

Copyright © 2005–2013, Texas Instruments Incorporated

Choose a small range of P so that the VCO frequency is swept between 40 MHz and 60 MHz. So for P = 3 to 5, sweep the M inputs from 1 to 3. The most accurate N and N_MOD can be calculated by:

$$N = FLOOR(((Fout/Fin)*(P*M)),1) \quad (6)$$

$$N_MOD = ROUND(32*((((Fout)/Fin)*(P*M)-N),0) \quad (7)$$

This shows that setting M = 1, N = 39+1/16, P = 5 (i.e. PLL_M = 0, PLL_N = 39, PLL_N_MOD = 2, & PLL_P = 4) gives a comparison frequency of 1.5 MHz, a VCO frequency of 60 MHz and an output frequency of 12.000 MHz. The same settings can be used to get 11.025 from 1.4112 MHz for 44.1 kHz sample rates.

Care must be taken when synchronization of isochronous data is not possible, i.e. when the PLL has to be used but an exact frequency match cannot be found. The I2S should be master on the LM4935 so that the data source can support appropriate SRC as required. This method should only be used with data being read on demand to eliminate sample rate mismatch problems.

Where a system clock exists at an integer multiple of the required ADC or DAC clock rate it is preferable to use this rather than the PLL. The LM4935 is designed to work in 8, 12, 16, 24, 48 kHz modes from a 12 MHz clock and 8, 13, 26, 52 kHz modes from a 13 MHz clock without the use of the PLL. This saves power and reduces clock jitter which can affect SNR.

The actual ADC and DAC sample rates are set up by the PLL and internal clock dividers.

4.2.10 ADC_1 CONFIGURATION REGISTER

This register is used to control the LM4935's audio ADC.

Table 4-11. ADC_1 (0x06h)

Bits	Field	Description	
0	MIC_SELECT	If set the microphone preamp output is added to the ADC input signal.	
1	CPI_SELECT	If set the cell phone input is added to the ADC input signal.	
2	LEFT_SELECT	If set the left stereo bus is added to the ADC input signal.	
3	RIGHT_SELECT	If set the right stereo bus is added to the ADC input signal.	
5:4	ADC_SAMPLE_RATE	Programs the closest expected sample rate of the mono ADC, which is a variable required by the AGC algorithm whenever the AGC is in use. This does not set the sample rate of the mono ADC.	
		ADC_SAMPLE_RATE	Sample Rate
		00_2	8 kHz
		01_2	12 kHz
		10_2	16 kHz
		11_2	24 kHz
7:6	HPF_MODE	Sets the HPF of the ADC	
		HPF-MODE	HPF Response
		00_2	No HPF
		01_2	F_S = 8 kHz, −0.5 dB @ 300 Hz, Notch @ 55 Hz F_S = 12 kHz, −0.5 dB @ 450 Hz, Notch @ 82 Hz F_S = 16 kHz, −0.5 dB @ 600 Hz, Notch @ 110 Hz
		10_2	F_S = 8 kHz, −0.5 dB @ 150 Hz, Notch @ 27 Hz F_S = 12 kHz, −0.5 dB @ 225 Hz, Notch @ 41 Hz F_S = 16 kHz, −0.5 dB @ 300 Hz, Notch @ 55 Hz
		11_2	No HPF

Copyright © 2005–2013, Texas Instruments Incorporated

4.2.11 ADC_2 CONFIGURATION REGISTER

This register is used to control the LM4935's audio ADC.

Table 4-12. ADC_2 (0x07h)

Bits	Field	Description	
0	ULAW/ALAW	If COMPAND is set then the data across the PCM interface to the DAC and from the ADC is companded as follows:	
		ULAW/ALAW	Commanding Type
		0	μ-law
		1	A-law
1	COMPAND	If set the 16 bit PCM data from the ADC is companded before the PCM interface and the PCM data to the DAC is treated as companded data.	
2	ADC_MUTE	If set the analog inputs to the ADC are muted.	
5:3	AGC_FRAME_TIME	This sets the frame time to be used by the AGC algorithm. In a given frame, the AGC's peak detector determines the peak value of the incoming microphone audio signal and compares this value to the target value of the AGC defined by AGC_TARGET (bits [3:1] of register (0x08h)) in order to adjust the microphone preamplifiers gain accordingly. AGC_FRAME_TIME basically sets the sample rate of the AGC to adjust for a wide variety of speech patterns. (Note 15)	
		AGC_FRAME_TIME	Time (ms)
		000_2	96
		001_2	128
		010_2	192
		011_2	256
		100_2	384
		101_2	512
		110_2	768
		111_2	1000
6	ADC_I2S_M	If set the DAC clock system is enabled to drive the I2S in master mode. The Point B frequency should be double that at Point C. This bit should be set when using the I2S interface in master mode to read SAR information whenever both the audio ADC and DAC are inactive.	
7	AUDIO_IF_2_16BIT	If set the PCM and I2S interfaces are 16 bits per word in master mode. The 2 last clock cycles per word are 25% shorter to allow generation.	

4.2.12 AGC_1 CONFIGURATION REGISTER

This register is used to control the LM4935's Automatic Gain Control. (Note 16)

Table 4-13. AGC_1 (0x08h)

Bits	Field	Description	
0	AGC_ENABLE	If set the AGC controls the analog microphone preamplifier gain into the system. The microphone input must be passed to the ADC.	
3:1	AGC_TARGET	Programs the target level of the AGC. This will depend on the expected transients and desired headroom. Refer to AGC_TIGHT (bit 7 of 0x09h) for more detail.	
		AGC_TARGET	Target Level
		000_2	−6 dB
		001_2	−8 dB
		010_2	−10 dB
		011_2	−12 dB
		100_2	−14 dB
		101_2	−16 dB
		110_2	−18 dB
		111_2	−20 dB

Copyright © 2005–2013, Texas Instruments Incorporated

Table 4-13. AGC_1 (0x08h) (continued)

Bits	Field	Description	
4	NOISE_GATE_ON	If set, signals below the noise gate threshold are muted.The noise gate is only activated after a set period of signal absence.	
7:5	NOISE_ GATE_ THRES	This field sets the expected background noise level relative to the peak signal level. The sole presence of signals below this level will not result in an AGC gain change of the input and will be gated from the ADC output if the NOISE_GATE_ON is set. This level must be set even if the noise gate is not in use as it is required by the AGC algorithm.	
		NOISE_GATE_THRES	Level
		000_2	−72 dB
		001_2	−66 dB
		010_2	−60 dB
		011_2	−54 dB
		100_2	−48 dB
		101_2	−42 dB
		110_2	−36 dB
		111_2	−30 dB

4.2.13 AGC_2 CONFIGURATION REGISTER

This register is used to control the LM4935's Automatic Gain Control.

Table 4-14. AGC_2 (0x09h)

Bits	Field	Description	
3:0	AGC_MAX_GAIN	This programs the maximum gain that the AGC algorithm can apply to the microphone preamplifier.	
		AGC_MAX_GAIN	Max Preamplifier Gain
		0000_2	6 dB
		0001_2	8 dB
		0010_2	10 dB
		0011_2	12 dB
		0100_2 to 1100_2	14 dB to 30 dB
		1101_2	32 dB
		1110_2	34 dB
		1111_2	36 dB
6:4	AGC_DECAY	Programs the speed at which the AGC will increase gains if it detects the input level is a quiet signal.	
		AGC_DECAY	Step Time (ms)
		000_2	32
		001_2	64
		010_2	128
		011_2	256
		100_2	512
		101_2	1024
		110_2	2048
		111_2	4096

Copyright © 2005–2013, Texas Instruments Incorporated

Table 4-14. AGC_2 (0x09h) (continued)

Bits	Field	Description		
7	AGC_TIGHT	If set the AGC algorithm controls the microphone preamplifier more exactly. (Note 17)		
	AGC_TIGHT = 0	AGC_TARGET	Min Level	Max Level
		000_2	−6 dB	−3 dB
		001_2	−8 dB	−4 dB
		010_2	−10 dB	−5 dB
		011_2	−12 dB	−6 dB
		100_2	−14 dB	−7 dB
		101_2	−16 dB	−8 dB
		110_2	−18 dB	−9 dB
		111_2	−20 dB	−10 dB
	AGC_TIGHT = 1	000_2	−6 dB	−3 dB
		001_2	−8 dB	−5 dB
		010_2	−10 dB	−7 dB
		011_2	−12 dB	−9 dB
		100_2	−14 dB	−11 dB
		101_2	−16 dB	−13 dB
		110_2	−18 dB	−15 dB
		111_2	−20 dB	−17 dB

4.2.14 AGC_3 CONFIGURATION REGISTER

This register is used to control the LM4935's Automatic Gain Control. (Note 18)

Table 4-15. AGC_3 (0x0Ah)

Bits	Field	Description	
4:0	AGC_HOLDTIME	Programs the amount of delay before the AGC algorithm begins to adjust the gain of the microphone preamplifier.	
		AGC_HOLDTIME	No. of speech segments
		00000_2	0
		00001_2	1
		00010_2	2
		00011_2	3
		00100_2 to 11100_2	4 to 28
		11101_2	29
		11110_2	30
		11111_2	31
7:5	AGC_ATTACK	Programs the speed at which the AGC will reduce gains if it detects the input level is too large.	
		AGC_ATTACK	Step Time (ms)
		000_2	32
		001_2	64
		010_2	128
		011_2	256
		100_2	512
		101_2	1024
		110_2	2048
		111_2	4096

Copyright © 2005–2013, Texas Instruments Incorporated

4.2.15 AGC OVERVIEW

The Automatic Gain Control (AGC) system can be used to optimize the dynamic range of the ADC for voice data when the level of the source is unknown. A target level for the output is set so that any transients on the input won't clip during normal operation. The AGC circuit then compares the output of the ADC to this level and increases or decreases the gain of the microphone preamplifier to compensate. If the audio from the microphone is to be output digitally through the ADC then the full dynamic range of the ADC can be used automatically. If the output is through the analog mixer then the ADC is used to monitor the microphone level. In this case, the analog dynamic range is less important than the absolute level, so *AGC_TIGHT* should be set to tie transients closely to the target level.

To ensure that the system doesn't reduce the quality of the speech by constantly modulating the microphone preamplifier gain, the ADC output is passed through an envelope detector. This frames the output of the ADC into time segments roughly equal to the phonemes found in speech *(AGC_FRAME_TIME)*. To calculate this, the circuit must also know the sample rate of the data from the ADC *(ADC_SAMPLERATE)*. If after a programmable number of these segments *(AGC_HOLDTIME)*, the level is consistently below target, the gain will be increased at a programmable rate *(AGC_DECAY)*. If the signal ever exceeds the target level (AGC_TARGET) then the gain of the microphone is reduced immediately at a programmable rate *(AGC_ATTACK)*. This is demonstrated below:

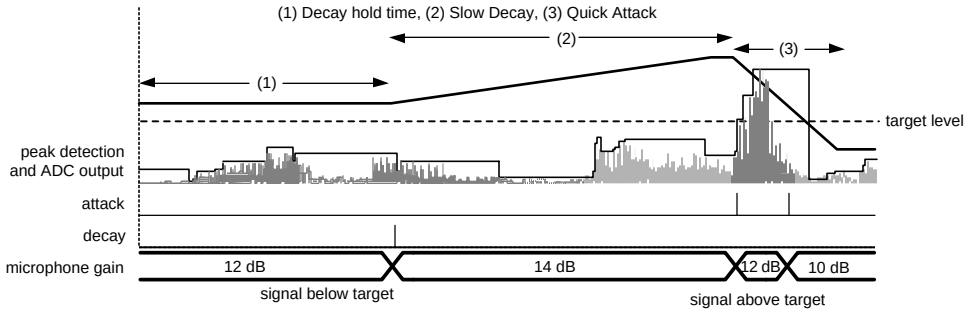


Figure 4-11. AGC Operation Example

The signal in the above example starts with a small analog input which, after the hold time has timed out, triggers a rise in the gain ((1) → (2)). After some time the real analog input increases and it reaches the threshold for a gain reduction which decreases the gain at a faster rate ((2) → (3)) to allow the elimination of typical popping noises.

Only ADC outputs that are considered signal (rather than noise) are used to adjust the microphone preamplifier gain. The signal to noise ratio of the expected input signal is set by *NOISE_GATE_THRESHOLD*. In some situations it is preferable to remove audio considered to be consisting solely of background noise from the audio output; for example conference calls. This can be done by setting *NOISE_GATE_ON*. This does not affect the performance of the AGC algorithm.

The AGC algorithm should not be used where very large background noise is present. If the type of input data, application and microphone is known then the AGC will typically not be required for good performance, it is intended for use with inputs with a large dynamic range or unknown nominal level. When setting *NOISE_GATE_THRESHOLD* be aware that in some mobile phone scenarios the ADC SNR will be dictated by the microphone performance rather than the ADC or the signal. Gain changes to the microphone are performed on zero crossings. To eliminate DC offsets, wind noise, and pop sounds from the output of the ADC, the ADC's HPF should always be enabled.

4.2.16 MIC_1 CONFIGURATION REGISTER

This register is used to control the microphone configuration.

Copyright © 2005–2013, Texas Instruments Incorporated

Table 4-16. MIC_1 (0x0Bh)

Bits	Field	Description	
3:0	PREAMP_GAIN	Programs the gain applied to the microphone preamplifier if the AGC is not in use.	
		PREAMP_GAIN	Gain
		0000_2	6 dB
		0001_2	8 dB
		0010_2	10 dB
		0011_2	12 dB
		0100_2 to 1100_2	14 dB to 30 dB
		1101_2	32 dB
		1110_2	34 dB
		1111_2	36 dB
4	MIC_MUTE	If set the microphone preamplifier is muted.	
5	INT_SE_DIFF	If set the internal microphone is assumed to be single ended and the negative connection is connected to the ADC common mode point internally. This allows a single-ended internal microphone to be used.	
6	INT_EXT	If set the single ended external microphone is used and the negative microphone input is grounded internally, otherwise internal microphone operation is assumed. (Note 19)	

4.2.17 MIC_2 CONFIGURATION REGISTER

This register is used to control the microphone configuration.

Table 4-17. MIC_2 (0x0Ch)

Bits	Field	Description		
0	OCL_ VCM_ VOLTAGE	Selects the voltage used as virtual ground (HP_VMID pin) in OCL mode. This will depend on the available supply and the power output requirements of the headphone amplifiers.		
		OCL_VCM_VOLTAGE	Voltage	
		0	1.2V	
		1	1.5V	
2:1	MIC_ BIAS_ VOLTAGE	Selects the voltage as a reference to the internal and external microphones. Only one bias pin is driven at once depending on the INT_EXT bit setting found in the MIC_1 (0x0Bh) register. MIC_BIAS_VOLTAGE should be set to '11' only if A_V_{DD} > 3.4V. In OCL mode, MIC_BIAS_VOLTAGE = '00' (EXT_BIAS = 2.0V) should not be used to generate the EXT_BIAS supply for a cellular headset external microphone. Please refer to Table 4-18 for more detail.		
		MIC_BIAS_VOLTAGE	EXT_BIAS	INT_BIAS
		00_2	2.0V	2.0V
		01_2	2.5V	2.5V
		10_2	2.8V	2.8V
		11_2	3.3V	3.3V
3	BUTTON_TYPE	If set the LM4935 assumes that the button (if used) in the headset is in series (series push button) with the microphone, opening the circuit when pressed. The default is for the button to be in parallel (parallel push button), shorting out the microphone when pressed.		
5:4	BUTTON_ DEBOUNCE_ TIME	Sets the time used for debouncing the pushing of the button on a headset with a parallel push button.		
		BUTTON_DEBOUNCE_TIME	Time (ms)	
		00_2	0	
		01_2	8	
		10_2	16	
		11_2	32	

Copyright © 2005–2013, Texas Instruments Incorporated

In OCL mode there is a trade-off between the external microphone supply voltage (EXT_MIC_BIAS - OCL_VCM_ VOLTAGE) and the maximum output power possible from the headphones. A lower OCL_VCM_VOLTAGE gives a higher microphone supply voltage but a lower maximum output power from the headphone amplifiers due to the lower OCL_VCM_VOLTAGE - A_V_{SS}.

Table 4-18. External MIC Supply Voltages in OCL Mode

Available A_V_{DD}	Recommended EXT_MIC_BIAS	Supply to Microphone	
		OCL_VCM_VOLT = 1.5V	OCL_VCM_VOLT = 1.2V
> 3.4V	3.3V	1.8V	2.1V
2.9V to 3.4V	2.8V	1.3V	1.6V
2.8V to 2.9V	2.5V	1.0V	1.3V
2.7V to 2.8V	2.5V	-	1.3V

4.2.18 SIDETONE ATTENUATION REGISTER

This register is used to control the analog sidetone attenuation. (Note 20)

Table 4-19. SIDETONE (0x0Dh)

Bits	Field	Description	
3:0	SIDETONE_ ATTEN	Programs the attenuation applied to the microphone preamp output to produce a sidetone signal.	
		SIDETONE_ATTEN	Attenuation
		0000_2	-Inf
		0001_2	−30 dB
		0010_2	−27 dB
		0011_2	−24 dB
		0100_2	−21 dB
		0101_2 to 1010_2	−18 dB to −3 dB
		1011_2 to 1111_2	0 dB

4.2.19 CP_INPUT CONFIGURATION REGISTER

This register is used to control the differential cell phone input.

Table 4-20. CP_INPUT (0x0Eh)

Bits	Field	Description	
4:0	CPI_LEVEL	Programs the gain/attenuation applied to the cell phone input.	
		CPI_LEVEL	Level
		00000_2	−34.5 dB
		00001_2	−33 dB
		00010_2	−31.5 dB
		00011_2	−30 dB
		00100 to 11100_2	−28.5 dB to +7.5 dB
		11101_2	+9 dB
		11110_2	+10.5 dB
		11111_2	+12 dB
5	CPI_MUTE	If set the CPI input is muted at source.	

Copyright © 2005–2013, Texas Instruments Incorporated

4.2.20 AUX_LEFT CONFIGURATION REGISTER

This register is used to control the left aux analog input.

Table 4-21. AUX_LEFT (0x0Fh)

Bits	Field	Description		
4:0	AUX_ LEFT_ LEVEL	Programs the gain/attenuation applied to the AUX LEFT analog input to the mixer. (Note 21)		
		AUX_LEFT_LEVEL	Level (With Boost)	Level (Without Boost)
		00000_2	−34.5 dB	−46.5 dB
		00001_2	−33 dB	−45 dB
		00010_2	−31.5 dB	−43.5 dB
		00011_2	−30 dB	−42 dB
		00100 to 11100_2	−28.5 dB to +7.5 dB	−40.5 dB to −4.5 dB
		11101_2	+9 dB	−3 dB
		11110_2	+10.5 dB	−1.5 dB
		11111_2	+12 dB	0 dB
5	AUX_ LEFT_ BOOST	If set the gain of the AUX_LEFT input to the mixer is increased by 12 dB (see above).		
6	AUX_L_MUTE	If set the AUX LEFT input is muted.		
7	AUX_OR_DAC_L	If set the AUX LEFT input is passed to the mixer, the default is for the DAC LEFT output to be passed to the mixer.		

4.2.21 AUX_RIGHT CONFIGURATION REGISTER

This register is used to control the right aux analog input.

Table 4-22. AUX_RIGHT (0x10h)

Bits	Field	Description		
4:0	AUX_ RIGHT_ LEVEL	Programs the gain/attenuation applied to the AUX RIGHT analog input to the mixer. (Note 22)		
		AUX_RIGHT_LEVEL	Level (With Boost)	Level (Without Boost)
		00000_2	−34.5 dB	−46.5 dB
		00001_2	−33 dB	−45 dB
		00010_2	−31.5 dB	−43.5 dB
		00011_2	−30 dB	−42 dB
		00100 to 11100_2	−28.5 dB to +7.5 dB	−40.5 dB to −4.5 dB
		11101_2	+9 dB	−3 dB
		11110_2	+10.5 dB	−1.5 dB
		11111_2	+12 dB	0 dB
5	AUX_ RIGHT_BOOST	If set the gain of the AUX_RIGHT input to the mixer is increased by 12 dB (see above).		
6	AUX_R_MUTE	If set the AUX RIGHT input is muted.		
7	AUX_OR_DAC_R	If set the AUX RIGHT input is passed to the mixer, the default is for the DAC RIGHT output to be passed to the mixer.		

Copyright © 2005–2013, Texas Instruments Incorporated

4.2.22 DAC CONFIGURATION REGISTER

This register is used to control the DAC levels to the mixer.

Table 4-23. DAC (0x11h)

Bits	Field	Description		
4:0	DAC_LEVEL	Programs the gain/attenuation applied to the DAC input to the mixer. (Note 23)		
		DAC_LEVEL	Level (With Boost)	Level (Without Boost)
		00000_2	−34.5 dB	−46.5 dB
		00001_2	−33 dB	−45 dB
		00010_2	−31.5 dB	−43.5 dB
		00011_2	−30 dB	−42 dB
		00100 to 11100_2	−28.5 dB to +7.5 dB	−40.5 dB to −4.5 dB
		11101_2	+9 dB	−3 dB
		11110_2	+10.5 dB	−1.5 dB
		11111_2	+12 dB	0 dB
5	USE_AUX_ LEVELS	If set the gain of the DAC inputs is controlled by the AUX_LEFT and AUX_RIGHT registers, allowing a stereo balance to be applied.		
6	BOOST	If set the gain of the DAC inputs to the mixer is increased by 12 dB (see above).		
7	DAC_MUTE	If set the stereo DAC input is muted on the next zero crossing.		

4.2.23 CP_OUTPUT CONFIGURATION REGISTER

This register is used to control the differential cell phone output. (Note 24)

Table 4-24. CP_OUTPUT (0x12h)

Bits	Field	Description
0	MIC_SELECT	If set the microphone channel of the mixer is added to the cellphone output signal.
1	RIGHT_SELECT	If set the right channel of the mixer is added to the cellphone output signal.
2	LEFT_SELECT	If set the left channel of the mixer is added to the cellphone output signal.
3	CPO_MUTE	If set the CPOUT output is muted.
4	MIC_NOISE_GAT E	If this is set and NOISE_GATE_ON (register 0x08h) is enabled, the MIC to CPO path will be gated if the signal is determined to be noise by the AGC (that is, if the signal is below the set noise threshold).

4.2.24 AUX_OUTPUT CONFIGURATION REGISTER

This register is used to control the differential auxiliary output. (Note 25)

Table 4-25. AUX_OUTPUT (0x13h)

Bits	Field	Description
0	CPI_SELECT	If set the cell phone input channel of the mixer is added to the aux output signal.
1	RIGHT_SELECT	If set the right channel of the mixer is added to the aux output signal.
2	LEFT_SELECT	If set the left channel of the mixer is added to the aux output signal.
3	AUX_MUTE	If set the aux output is muted.

Copyright © 2005–2013, Texas Instruments Incorporated

4.2.25 LS_OUTPUT CONFIGURATION REGISTER

This register is used to control the loudspeaker output. (Note 26)

Table 4-26. LS_OUTPUT (0x14h)

Bits	Field	Description
0	CPI_SELECT	If set the cell phone input channel of the mixer is added to the loudspeaker output signal.
1	RIGHT_SELECT	If set the right channel of the mixer is added to the loudspeaker output signal.
2	LEFT_SELECT	If set the left channel of the mixer is added to the loudspeaker output signal.
3	LS_MUTE	If set the loudspeaker output is muted.

4.2.26 HP_OUTPUT CONFIGURATION REGISTER

This register is used to control the stereo headphone output. (Note 27)

Table 4-27. HP_OUTPUT (0x15h)

Bits	Field	Description
0	SIDETONE_SELECT	If set the sidetone channel of the mixer is added to both of the headphone output signals.
1	CPI_SELECT	If set the cell phone input channel of the mixer is added to both of the headphone output signals.
2	RIGHT_SELECT	If set the right channel of the mixer is added to the headphone output. If the STEREO bit (0x00h) is set, the right channel is added to the right headphone output signal only. If the STEREO bit (0x00h) is cleared, it is added to both the right and left headphone output signals.
3	LEFT_SELECT	If set the left channel of the mixer is added to the headphone output. If the STEREO bit (0x00h) is set, the left channel is added to the left headphone output signal only. If the STEREO bit (0x00h) is cleared, it is added to both the right and left headphone output signals.
4	HP_MUTE	If set the headphone output is muted.

4.2.27 EP_OUTPUT CONFIGURATION REGISTER

This register is used to control the mono earpiece output. (Note 28)

Table 4-28. EP_OUTPUT (0x16h)

Bits	Field	Description
0	SIDETONE_SELECT	If set the sidetone channel of the mixer is added to the earpiece output signal.
1	CPI_SELECT	If set the cell phone input channel of the mixer is added to the earpiece output signal.
2	RIGHT_SELECT	If set the right channel of the mixer is added to the earpiece output signal.
3	LEFT_SELECT	If set the left channel of the mixer is added to the earpiece output signal.
4	EP_MUTE	If set the earpiece output is muted.

4.2.28 DETECT CONFIGURATION REGISTER

This register is used to control the headset detection system.

Table 4-29. DETECT (0x17h)

Bits	Field	Description
0	DET_INT	If set an IRQ is raised when a change is detected in the headset status. Clearing this bit will clear an IRQ that has been triggered by the headset detect.
1	BTN_INT	If set an IRQ is raised when the headset button is pressed. Clearing this bit will clear an IRQ that has been triggered by a button event.
2	TEMP_INT	If set an IRQ is raised during a temperature event. If cleared, the LM4935 will still automatically cycle the power amplifiers off if the internal temperature is too high. This bit should not be set whenever the loudspeaker amplifier is turned on. Clearing this bit will clear an IRQ that has been triggered by a temperature event.

Copyright © 2005–2013, Texas Instruments Incorporated

Table 4-29. DETECT (0x17h) (continued)

Bits	Field	Description	
6:3	HS_ DBNC_TIME	Sets the time used for debouncing the analog signals from the detection inputs used to sense the insertion/removal of a headset.	
		HS_DBNC_TIME	Time (ms)
		0000_2	0
		0001_2	8
		0010_2	16
		0011_2	32
		0100_2	48
		0101_2	64
		0110_2	96
		0111_2	128
		1000_2	192
		1001_2	256
		1010_2	384
		1011_2	512
		1100_2	768
		1101_2	1024
		1110_2	1536
		1111_2	2048

4.2.29 HEADSET DETECT OVERVIEW

The LM4935 has built in monitors to automatically detect headset insertion or removal. The detection scheme can differentiate between mono, stereo, mono-cellular and stereo-cellular headsets. Upon detection of headset insertion or removal, the LM4935 updates read-only bit 0 - headset absence/presence, bit 1- mono/stereo headset and bit 2 - headset without mic / with mic, of the STATUS register (0x18h). Headset insertion/removal and headset type can also be detected in standby mode; this consumes no analog supply current when the headset is absent.

The LM4935 can be programmed to raise an interrupt (set the IRQ pin high) when headset insert/removal is sensed by setting bit 0 of DETECT (0x17h). When headset detection is enabled in active mode and a headset is not detected, the HPL_OUT and HPR_OUT amplifiers will be disabled (switched off for capless mode and muted for AC-coupled mode) and the EXT_BIAS pin will be disconnected from the MIC_BIAS amplifier, irrespective of control register settings.

The LM4935 also has the capability to detect button press, when a button is present on the headset microphone. Both parallel button-type (in parallel with the headset microphone, default value) and series button-type (in series with the headset microphone) can be detected; the button type used needs to be defined in bit 3 of MIC_2 (0x0Ch). Button press can also be detected in stand-by mode; this consumes 10 µA of analog supply current for a series type push button and 100 µA for a parallel type push button. Upon button press, the LM4935 updates bit 3 of STATUS (0x18h). In active OCL mode, with internal microphone selected (INT_EXT = 0; (reg 0x0Bh)), if a parallel pushbutton headset is inserted into the system, INT_EXT must be set high before BTN (bit 3 of STATUS (0x18h)) can be read. The LM4935 can also be programmed to raise an interrupt on the IRQ pin when button press is sensed by setting bit 1 of DETECT.

The LM4935 provides debounce programmability for headset and button detect. Debounce programmability can be used to reject glitches generated, and hence avoid false detection, while inserting/removing a headset or pressing a button.

Headset insert/removal debounce time is defined by HS_DBNC_TIME; bits 6:3 of DETECT (0x17h). Parallel button press debounce time is defined by BTN_DBNC_TIME; bits 5:4 of MIC_2 (0x0Ch).

Copyright © 2005–2013, Texas Instruments Incorporated

Note that since the first effect of a series button press (microphone disconnected) is indistinguishable from headset removal, the debounce time for series button press in defined by HS_DBNC_TIME.

Headset and push button detection can be enabled by setting CHIP_MODE 0; bit 0 of BASIC (0x00h). For reliable headset / push button detection all following bits should be defined before enabling the headset detection system:

1) the OCL-bit (AC-Coupled / Capless headphone interface (bit 7 of BASIC (0x00h))

2) the headset insert/removal debounce settings (bit 6:3 of DETECT (0x17h))

3) the BTN_TYPE-bit (Parallel / Series push button type (bit 3 of MIC_2 (0x0Ch))

4) the parallel push button debounce settings (bit 5:4 of MIC_2 (0x0Ch))

Figure 4-12 shows terminal connections and jack configuration for various headsets. Care should be taken to avoid any DC path from the MIC_DET pin to ground when a headset is not inserted.

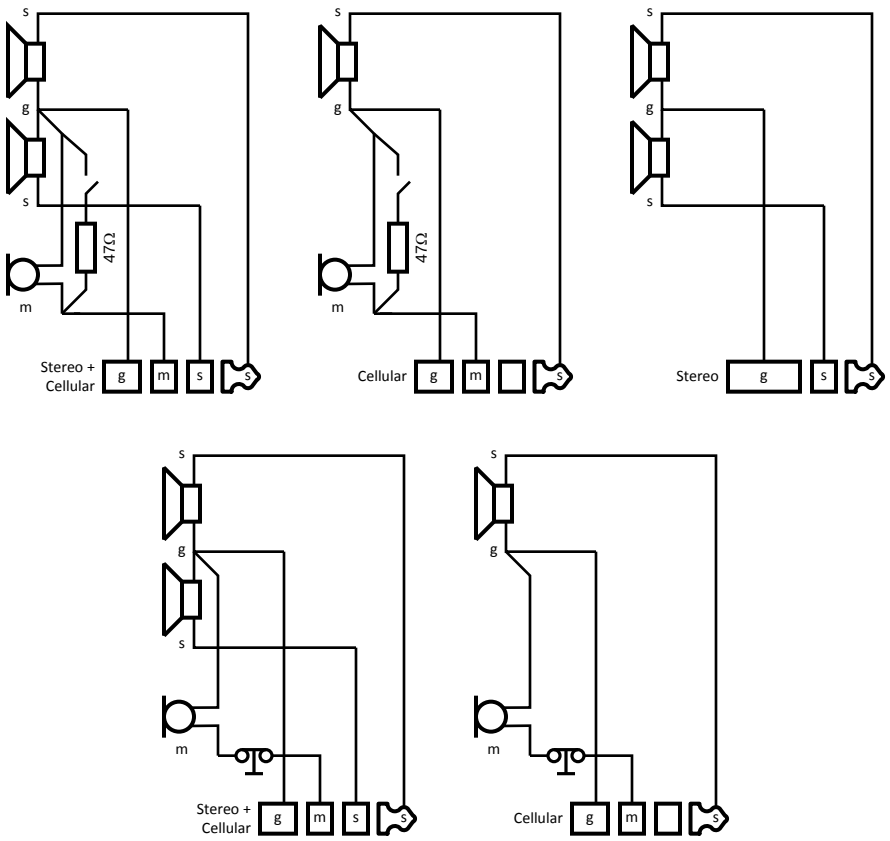


Figure 4-12. Headset Configurations Supported by the LM4935

The wiring of the headset jack to the LM4935 will depend on the intended mode of the headphone amplifier:

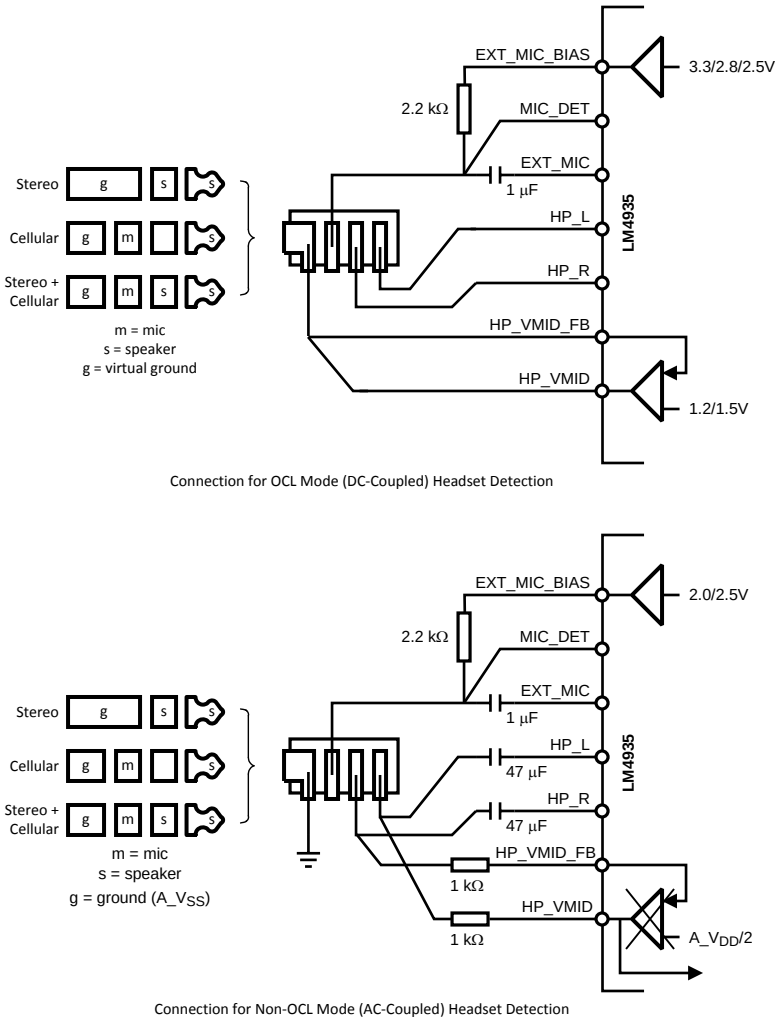


Figure 4-13. Connection of Headset Jack to LM4935 Depends on the Mode of the Headphone Amplifier.

4.2.30 STATUS REGISTER

This register is used to report the status of the device.

Table 4-30. STATUS (0x18h)

Bits	Field	Description
0	HEADSET	This field is high when headset presence is detected (only valid if the detection system is enabled). (Note 29)
1	STEREO_ HEADSET	This field is high when a headset with stereo speakers is detected (only valid if the detection system is enabled). (Note 29)
2	MIC	This field is high when a headset with a microphone is detected (only valid if the detection system is enabled). (Note 29)
3	BTN	This field is high when the button on the headset is pressed (only valid if the detection system is enabled). IRQ is cleared when the button has been released **and** this register has been written to.
4	SAR TRIG 1	If this field is high then an event has happened on SAR trigger 1 (write to this register to clear IRQ).
5	SAR TRIG 2	If this field is high then an event has happened on SAR trigger 2 (write to this register to clear IRQ).
6	TEMP	If this field is high then a temperature event has occurred (write to this register to clear IRQ). This field will stay high even when the IRQ is cleared so long as the event occurs. This bit is only valid whenever the loudspeaker amplifier is turned off.
7	GPIN	When GPIO_SEL is set to a readable configuration a digital input on GPIO1 can be read back here.

Copyright © 2005–2013, Texas Instruments Incorporated

4.2.31 AUDIO INTERFACE CONFIGURATION REGISTER

This register is used to control the configuration of the audio data interfaces.

Table 4-31. AUDIO_IF (0x19h)

Bits	Field	Description						
1:0	AUDIO_IF_MODE	Selects the function of the 6 audio interface IOs.						
		AUDIO_IF_MODE	**I2S_ CLK pin**	**I2S_ WS pin**	**I2S_ SDI pin**	**I2S_ SDO pin**	**GPIO_1 pin**	**GPIO_2 pin**
		00_2	I^2S CLK	I^2S WS	I^2S SDI	I^2S SDO	GPIO 1	GPIO 2
		01_2	PCM CLK	PCM SYNC	-	PCM SDO	GPIO 1	GPIO 2
		10_2	PCM CLK	PCM SYNC	PCM SDI	PCM SDO	GPIO 1	GPIO 2
		11_2	I^2S CLK	I^2S WS	I^2S SDI	PCM SDO	PCM CLK	PCM SYNC
2	I2S_WS_MS	If set the I^2S_WS is produced by the LM4935 and the I^2S_WS pin will be an output.						
3	I2S_CLK_MS	If set the I^2S_CLK is produced by the LM4935 and the I^2S_CLK pin will be an output.						
4	PCM_SYNC_MS	If set the PCM_SYNC is produced by the LM4935 and the relevant pin will be an output.						
5	PCM_CLK_MS	If set the PCM_CLK is produced by the LM4935 and the relevant pin will be an output.						
7:6	I2S_SDO_DATA	The two ADCs on the LM4935 can both be read via the isochronous I2S interface. The most recent valid sample is output from the following source: (Please refer to Table 4-32 for more information on SAR_CH_SEL)						
		I2S_SDO_DATA			LEFT		RIGHT	
		00_2			AUDIO ADC		SAR_CH_SEL	
		01_2			SAR VSAR 1		SAR_CH_SEL	
		10_2			SAR VSAR 2		SAR_CH_SEL	
		11_2			$A_V_{DD}/2$		SAR_CH_SEL	

4.2.32 DIGITAL AUDIO DATA FORMATS

I2S master mode can only be used when the DAC is enabled unless the ADC_I2S_M bit is set. PCM Master mode can only be used when the ADC is enabled. If the PCM receiver interface is operated in slave mode the clock and sync should be enabled at the same time as the PCM receiver uses the first PCM frame to calculate the PCM interface format. This format can not be changed unless a soft reset is issued. It is strongly recommended that the LM4935 is operated in master mode as this eliminates the risk of sample rate mismatch between the data converters and the audio interfaces.

In master mode the I2S_CLK has a 60/40 duty cycle and a frequency of 50*fs. In slave mode the PCM and I2S receivers only record the 1st 16 and 18 bits of the serial words respectively. The I2S format is as follows:

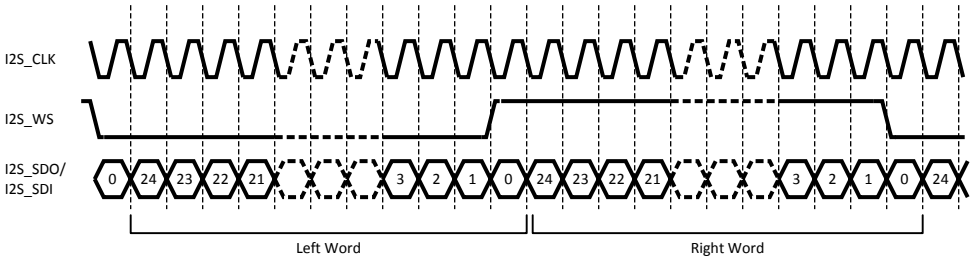


Figure 4-14. I^2S Serial Data Format (Default Mode)

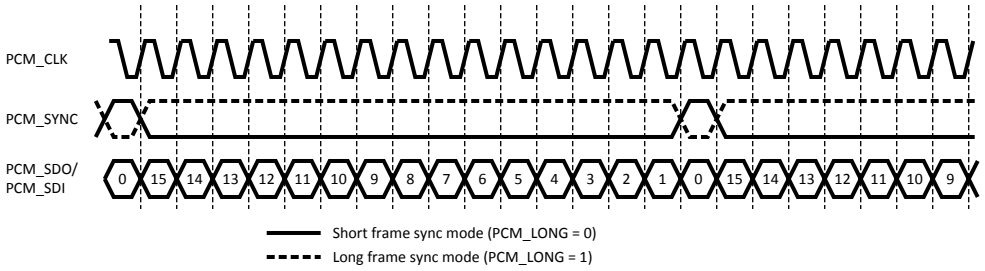


Figure 4-15. PCM Serial Data Format (16 bit Slave Example)

When SAR SDO data is passed to the I2S, it is left aligned (MSB aligned) to allow lower I2S resolutions to be used.

If the DAC is driven from the PCM interface then the left channel of the DAC is used and the right channel is inactive.

4.2.33 GPIO CONFIGURATION REGISTER

This register is used to control the GPIO system.

Table 4-32. GPIO (0x1Ah)

Bits	Field	Description		
2:0	GPIO_SEL	This sets the function of the GPIOs when the Audio Interface is not using them.		
		GPIO_SEL	GPIO 1	GPIO 2
		000_2	0	0
		001_2	READABLE	SPI_SDO
		010_2	LS_AMP_ENABLE	SPI_SDO
		011_2	GPIO_DATA	SPI_SDO
		100_2	0	SPI_SDO
		101_2	READABLE	SAR_SDO
		110_2	LS_AMP_ENABLE	SAR_SDO
		111_2	GPIO_DATA	SAR_SDO
		Setting GPIO_SEL = “010” with the GPIO_TEST_MODE bit (register 0X26h) set configures the GPIOs for digital mic operation. With this setting, GPI01 will output VADC_CLK_OUT to provide a clock for the digital mic. GPIO2 will accept digital mic data. GPIO1's LS_AMP_ENABLE setting will be logic high whenever the loudspeaker amplifier is enabled. This is useful for enabling an external amplifier for stereo loudspeaker applications.		
4:3	SAR_CH_SEL	This field selects the SAR output channel for the 2nd (Right) I^2S channel or for SAR_SDO via GPIO2.		
		SAR_CH_SEL	Selected Channel	
		00_2	VSAR_1	
		01_2	VSAR_2	
		10_2	$D_V_{DD}/2$ or BB_V_{DD}	
		11_2	$A_V_{DD}/2$	
5	I2S_MODE	If set the I2S operates in left justified mode (sometimes referred to as DSP mode). See example below. (Note 30)		
6	PCM_LONG	If set the PCM interface uses LONG frame sync which is essentially an inverted short frame sync.		
7	GPIO_DATA	If GPIO_SEL is set to GPIO_DATA then the content of this field is passed to GPIO1 as an output.		

Copyright © 2005–2013, Texas Instruments Incorporated

4.2.34 SAR CHANNELS 0 & 1 CONFIGURATION REGISTER

This register is used to control channel 0 and 1 of the SAR system. (Note 31)

Table 4-33. SAR_SLOT01 (0x1Bh)

Bits	Field	Description	
2:0	SLOT_0_FS	Programs the sampling frequency of SAR channel 0:	
		SLOT_0_FS	Sample Rate @ 12.000 MHz (point **A**)
		000_2	13.888 kHz
		001_2	3.472 kHz
		010_2	0.868 kHz
		011_2	217 Hz
		100_2	54 Hz
		101_2	14 Hz
		110_2	4 Hz
		111_2	1 Hz
3	SLOT_0_ENB	If set then VSAR 1 is sampled into SAR slot 0 which also activates the SAR ADC.	
6:4	SLOT_1_FS	Programs the sampling frequency of SAR channel 1:	
		SLOT_1_FS	Sample Rate @ 12.000 MHz (point **A**)
		000_2	13.888 kHz
		001_2	3.472 kHz
		010_2	0.868 kHz
		011_2	217 Hz
		100_2	54 Hz
		101_2	14 Hz
		110_2	4 Hz
		111_2	1 Hz
7	SLOT_1_ENB	If set then VSAR 2 is sampled into SAR slot 1 which also activates the SAR ADC.	

4.2.35 SAR CHANNELS 2 & 3 CONFIGURATION REGISTER

This register is used to control channel 2 and 3 of the SAR system. (Note 31)

Table 4-34. SAR_SLOT23 (0x1Ch)

Bits	Field	Description	
2:0	SLOT_2_FS	Programs the sampling frequency of SAR channels 2 and 3:	
		SLOT_2_FS	Sample Rate @ 12.000 MHz (point **A**)
		000_2	13.888 kHz
		001_2	3.472 kHz
		010_2	0.868 kHz
		011_2	217 Hz
		100_2	54 Hz
		101_2	14 Hz
		110_2	4 Hz
		111_2	1 Hz
3	SLOT_2_ENB	If set then D_V_{DD} / 2 or BB_V_{DD} (depending on $SLOT2_V_{BB}$) is sampled into SAR slot 2 which also activates the SAR ADC.	
4	SLOT_3_ENB	If set then A_V_{DD} / 2 is sampled into SAR slot 3 which also activates the SAR ADC.	
5	SLOT_2_VBB	If set then BB_V_{DD} input is used as input to SAR slot 2 rather than the D_V_{DD}.	

Copyright © 2005–2013, Texas Instruments Incorporated

4.2.36 SAR DATA 0 TO 3 REGISTERS

These registers are used to read the 8 MSBs from the 4 SAR channels.

Table 4-35. SAR_DATA_0 Register (0x1Dh)

Bits	Field	Description
7:0	SLOT_0_DATA	Latest slot 0 sample bits 11:4.

Table 4-36. SAR_DATA_1 Register (0x1Eh)

Bits	Field	Description
7:0	SLOT_1_DATA	Latest slot 1 sample bits 11:4.

Table 4-37. SAR_DATA_2 Register (0x1Fh)

Bits	Field	Description
7:0	SLOT_2_DATA	Latest slot 2 sample bits 11:4.

Table 4-38. SAR_DATA_3 Register (0x20h)

Bits	Field	Description
7:0	SLOT_3_DATA	Latest slot 3 sample bits 11:4.

4.2.37 SAR OVERVIEW

The SAR controller works via a scheduler that allocates time slots for each of the four channels. All four channels can operate up to the same maximum frequency. When the sampling frequency of a channel is to be reduced the time slot allocated to that channel is simply enabled less often. For example if one slot is to work at a quarter of the frequency of the others then only one in four of its allocated slot triggers the SAR to activate:

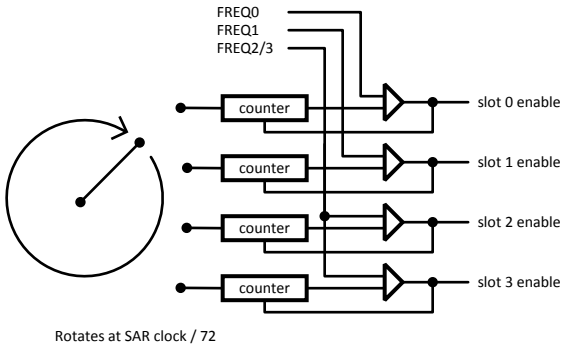


Figure 4-16. Internal SAR Control Signals to SAR Module

Each time slot is used to sample a single fixed input, slot 0 is used for VSAR 1, slot 1 for VSAR 2, slot 2 for either D_V_{DD} or BB_V_{DD}* and slot 3 for the A_V_{DD}. When a particular time slot is activated the correct mux, clock and enable controls to the ADC module are produced and the output sampled when ready. If the D_V_{DD} or the A_V_{DD} are being sampled then a voltage divider is used to half the input to below the full scale reference of 2.5V. As this results in a current path to ground it is only inserted while the ADC is settling to reduce power consumption.

Using this method, samples can be taken using as little power as possible while allowing sample rates as low as 1 Hz. The data can either be read directly or used to trigger interrupts when set voltages are passed. This reduces the baseband controllers software overhead and IO bandwidth, further reducing system power.

Copyright © 2005–2013, Texas Instruments Incorporated

The full scale digital output from the SAR is equal to 2.5V. The A_V_{DD} and D_V_{DD} inputs are divided by two during sampling. The SAR ADC can be activated at any time, even while the chip is in shutdown mode (chip mode '00'). This allows the LM4935 to perform housekeeping duties such as voltage monitoring with minimal power consumption.

*Depending on SLOT_2_VBB in SAR_SLOT23 (0x1Ch).

Only the 8 MSBS [11:4] from the 12 bits of SAR output data can be read back using the I^2C interface.

The SPI interface can be used to access all 12 bits of the SAR output data. In this case, GPIO2 should be set to SAR_SDO by setting GPIO_SEL in register (0x1Ah). The SAR channel selected by SAR_CH_SEL in the GPIO register is then output onto GPIO2 as follows:

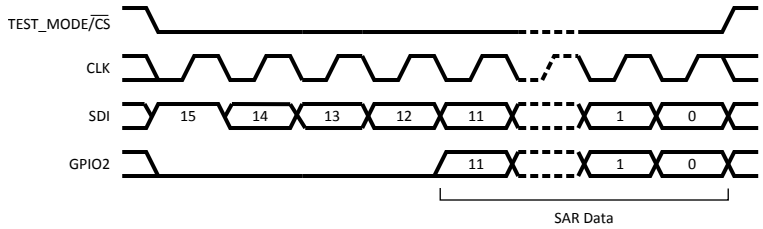


Figure 4-17. SPI SAR Read Transaction (GPIO2 set to SAR_SDO)

In applications where the 8 MSBS [11:4] from the SAR output data is enough resolution, GPIO2 should be set to SPI_SDO by setting GPIO_SEL in register (0x1Ah). The SAR data is then output on GPIO2 as follows:

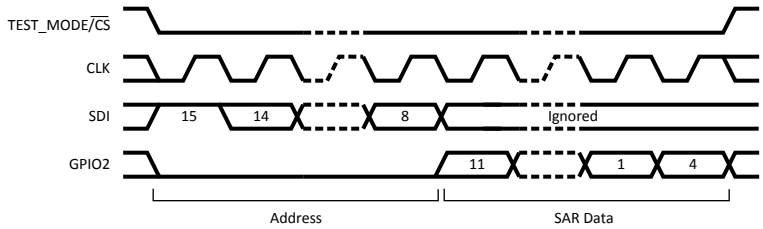


Figure 4-18. SPI SAR Read Transaction (GPIO2 set to SPI_SDO)

If the user performs a write to the GPIO register the changes will not take effect until the next SPI operation so SAR data can be read while the next channel is being selected. The SAR data is sampled at the start of the SPI transaction to ensure that the data is stable during the read operation.

All 12 bits of the SAR output data for up to 2 SAR channels can be read back simultaneously through the bi-directional I^2S interface. This is accomplished by setting I2S_SDO_DATA (bit [7:6] of (0x19h)) to the desired SAR channel(s).

As mentioned previously in the Section 4.2.32 section, when SAR SDO is passed to the I^2S bus, the SAR SDO's MSB is aligned with the MSB of I2S_SDO.

Copyright © 2005–2013, Texas Instruments Incorporated

4.2.38 DC VOLUME CONFIGURATION REGISTER

This register is used to control the DC volume control system.

Table 4-39. DC_VOLUME (0x21h)

Bits	Field	Description	
0	DC_VOL_ENB	Enables the DC volume control system to use the voltage applied on the VSAR 1 pin to set the gain of the DC volume control. (Note 32)	
1	DC_VOL_EFFECT	Selects which volume is altered:	
		DC_VOL_EFFECT	Source
		0	AUX/DAC
		1	CPI
3:2	MAX_LEVEL	Programs the maximum level that can be applied by the system	
		MAX_LEVEL	LEVEL
		00_2	0 dB
		01_2	−3 dB
		10_2	−6 dB
		11_2	−12 dB

4.2.39 SAR TRIGGER 1 CONFIGURATION REGISTER

This register is used to setup a voltage trigger on one of the SAR outputs.

Table 4-40. TRIG_1 (0x22h)

Bits	Field	Description	
0	TRIG_1_ENB	Enables the 1st SAR trigger interrupt, if cleared will clear the IRQ.	
1	TRIG_1_DIR	Selects the direction the voltage should be moving:	
		TRIG_1_DIR	Trigger if signal passes:
		0	Above Threshold
		1	Below Threshold
3:2	TRIG_1_SOURCE	Programs the channel used by the trigger.	
		TRIG_1_SOURCE	Source
		00_2	VSAR_1
		01_2	VSAR_2
		10_2	D_V_{DD}/2 or BB_V_{DD}
		11_2	A_V_{DD}/2
7:4	TRIG_1_LSB	Sets bits 3:0 of the threshold used by the trigger.	

4.2.40 SAR TRIGGER 1 MSBs CONFIGURATION REGISTER

This register is used to setup the threshold of a voltage trigger on one of the SAR outputs.

Table 4-41. TRIG_1_MSB (0x23h)

Bits	Field	Description
7:0	TRIG_1_MSB	Sets bits 11:4 of the threshold used by the trigger.

Copyright © 2005–2013, Texas Instruments Incorporated

4.2.41 SAR TRIGGER 2 CONFIGURATION REGISTER

This register is used to setup a voltage trigger on one of the SAR outputs.

Table 4-42. TRIG_2 (0x24h)

Bits	Field	Description	
0	TRIG_2_ENB	Enables the 2nd SAR trigger interrupt, if cleared will clear the IRQ.	
1	TRIG_2_DIR	Selects the direction the voltage should be moving:	
		TRIG_2_DIR	Trigger if signal passes:
		0	Above Threshold
		1	Below Threshold
3:2	TRIG_2_SOURCE	Programs the channel used by the trigger	
		TRIG_2_SOURCE	Source
		00_2	VSAR_1
		01_2	VSAR_2
		10_2	D_V_{DD}/2 or BB_V_{DD}
		11_2	A_V_{DD}/2
7:4	TRIG_2_LSB	Sets bits 3:0 of the threshold used by the trigger.	

4.2.42 SAR TRIGGER 2 MSBs CONFIGURATION REGISTER

This register is used to setup the threshold of a voltage trigger on one of the SAR outputs.

Table 4-43. TRIG_2_MSB (0x25h)

Bits	Field	Description
7:0	TRIG_2_MSB	Sets bits 11:4 of the threshold used by the trigger.

4.2.43 DEBUG REGISTER

This register is used to set test modes within the device.

Table 4-44. DEBUG (0x26h)

Bits	Field	Description		
0	RSVD	Reserved		
1	RSVD	Reserved		
2	RSVD	Reserved		
3	SOFT_RESET	This field can be used to reset the chip without a power cycle.		
4	RSVD	Reserved		
5	RSVD	Reserved		
6	RSVD	Reserved		
7	GPIO_TEST_MODE	If set and GPIO_SEL = '010', then the GPIOs are configured to interface with the LMV1026 digital microphone as long as AUDIO_IF_MODE (0x19h) is not set to '11'.		
		GPIO_SEL	GPIO 1	GPIO 2
		000_2	RSVD	RSVD
		001_2	RSVD	RSVD
		010_2	VADC_CLOCK_OUT	DIG_MIC_IN
		011_2	RSVD	RSVD
		100_2	RSVD	RSVD
		101_2	RSVD	RSVD
		110_2	RSVD	RSVD
		111_2	RSVD	RSVD

Copyright © 2005–2013, Texas Instruments Incorporated

5 Typical Performance Characteristics

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Stereo DAC Frequency Response
f_S = 8kHz

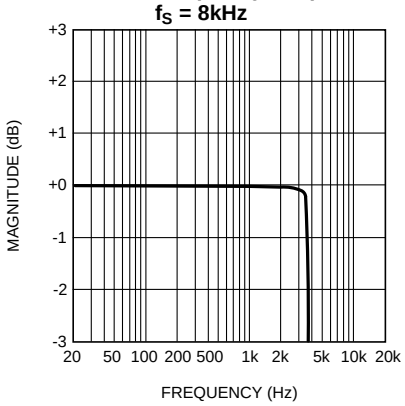


Figure 5-1.

Stereo DAC Frequency Response Zoom
f_S = 8kHz

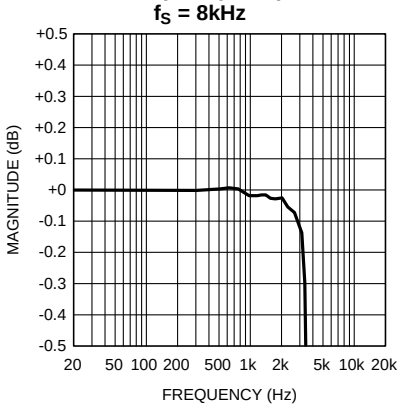


Figure 5-2.

Stereo DAC Frequency Response
f_S = 16kHz

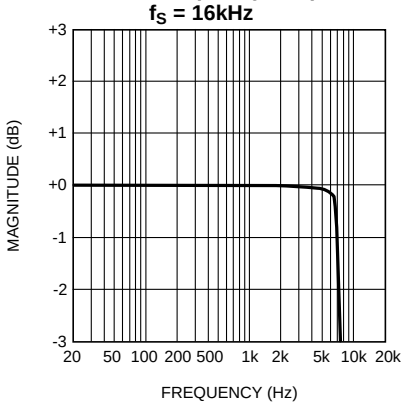


Figure 5-3.

Stereo DAC Frequency Response Zoom
f_S = 16kHz

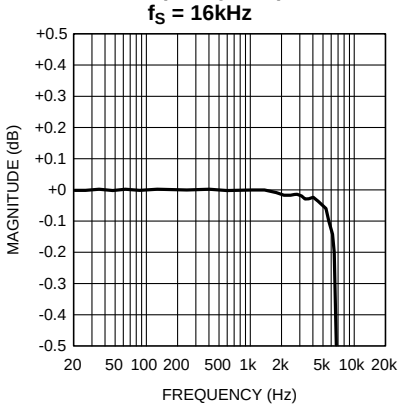


Figure 5-4.

Stereo DAC Frequency Response
f_S = 24kHz

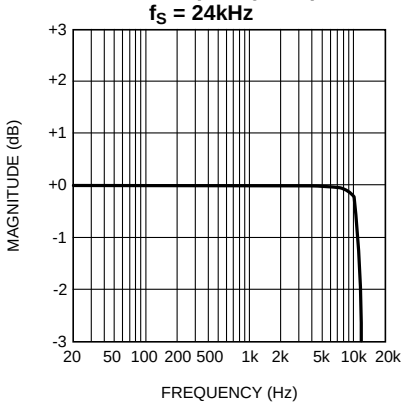


Figure 5-5.

Stereo DAC Frequency Response Zoom
f_S = 24kHz

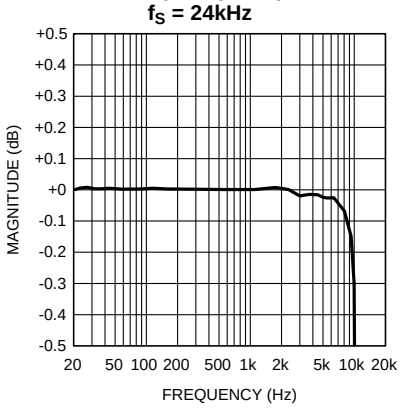


Figure 5-6.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Stereo DAC Frequency Response
f_S = 32kHz

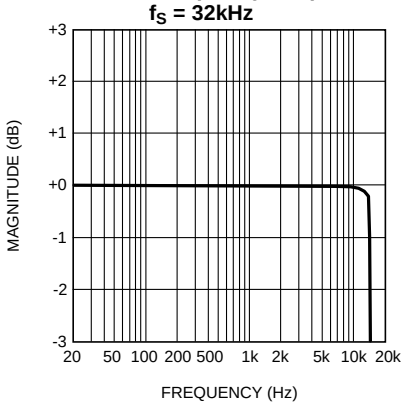


Figure 5-7.

Stereo DAC Frequency Response Zoom
f_S = 32kHz

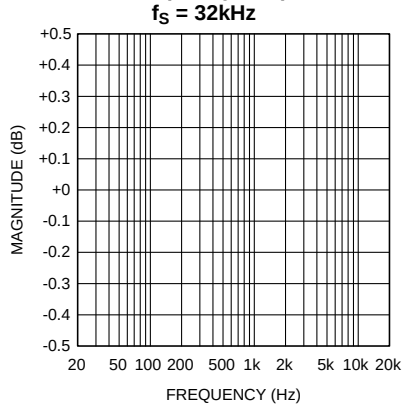


Figure 5-8.

Stereo DAC Frequency Response
f_S = 48kHz

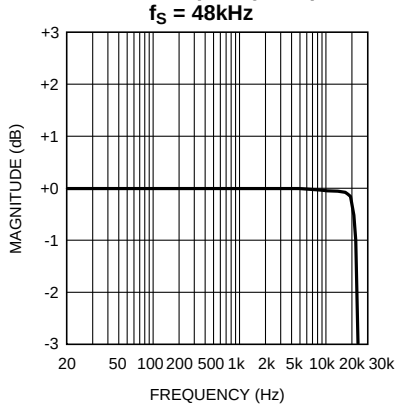


Figure 5-9.

Stereo DAC Frequency Response Zoom
f_S = 48kHz

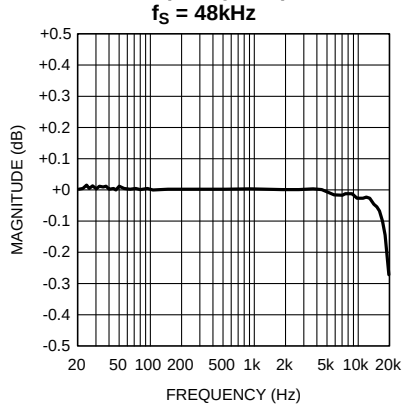


Figure 5-10.

THD+N
vs
Stereo DAC Input Voltage
(0dB DAC, AUXOUT)

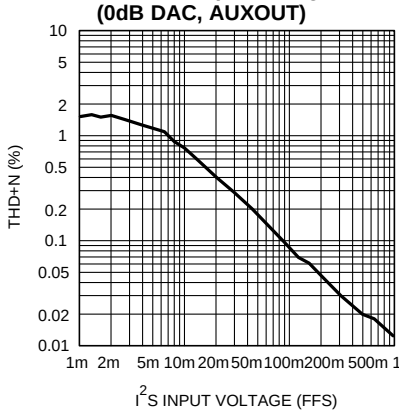


Figure 5-11.

Stereo DAC Crosstalk
(0dB DAC, HP SE)

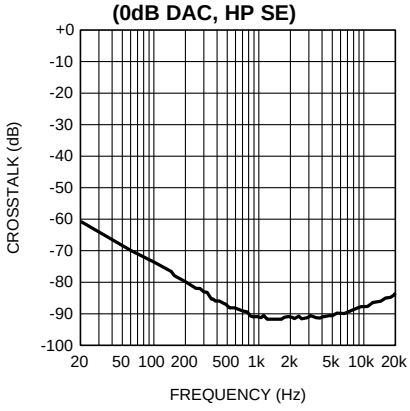


Figure 5-12.

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

MONO ADC Frequency Response
f_S = 8kHz, 6dB MIC

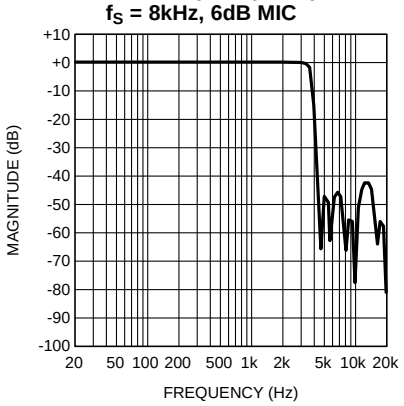


Figure 5-13.

MONO ADC Frequency Response Zoom
f_S = 8kHz, 6dB MIC

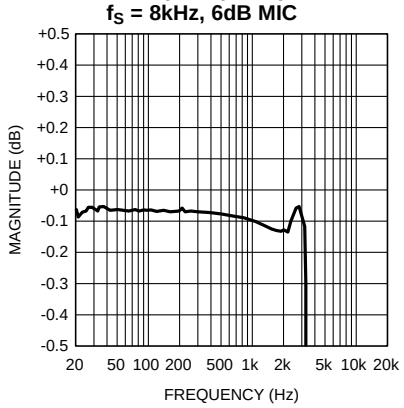


Figure 5-14.

MONO ADC Frequency Response
f_S = 8kHz, 36dB MIC

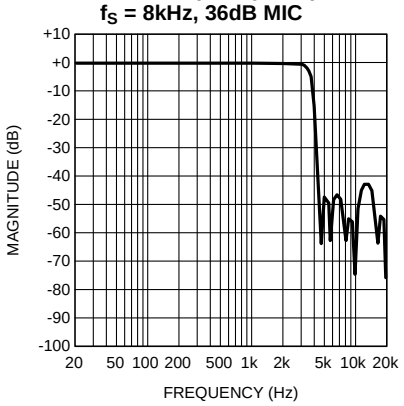


Figure 5-15.

MONO ADC Frequency Response Zoom
f_S = 8kHz, 36dB MIC

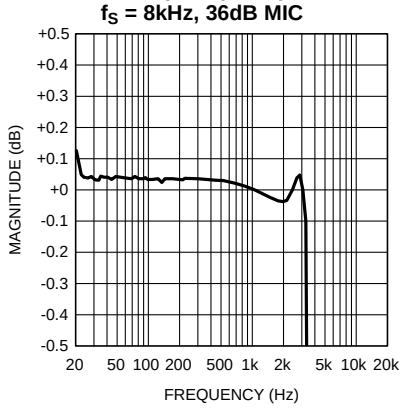


Figure 5-16.

MONO ADC Frequency Response
f_S = 16kHz, 6dB MIC

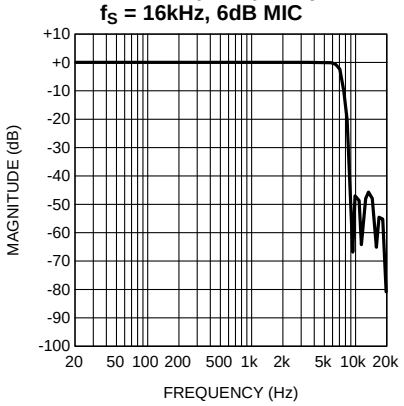


Figure 5-17.

MONO ADC Frequency Response Zoom
f_S = 16kHz, 6dB MIC

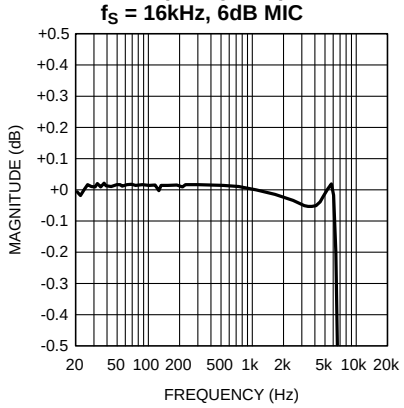


Figure 5-18.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

MONO ADC Frequency Response
f_S = 16kHz, 36dB MIC

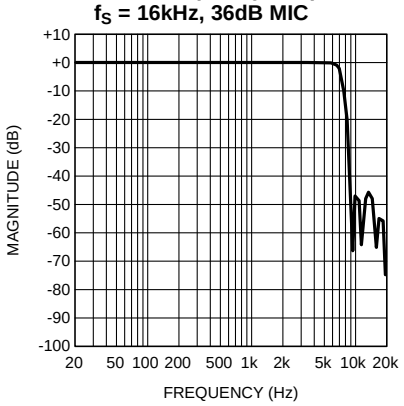


Figure 5-19.

MONO ADC Frequency Response Zoom
f_S = 16kHz, 36dB MIC

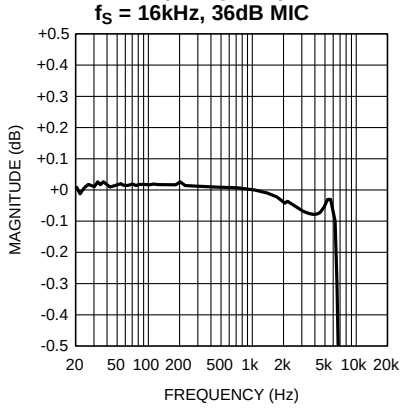


Figure 5-20.

MONO ADC Frequency Response
f_S = 24kHz, 6dB MIC

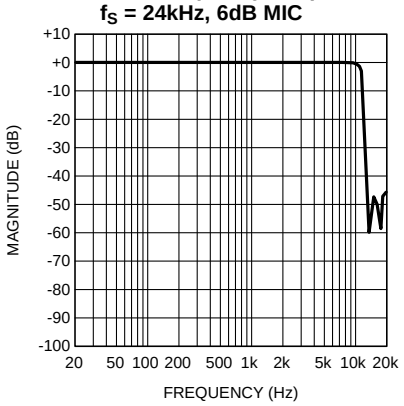


Figure 5-21.

MONO ADC Frequency Response Zoom
f_S = 24kHz, 6dB MIC

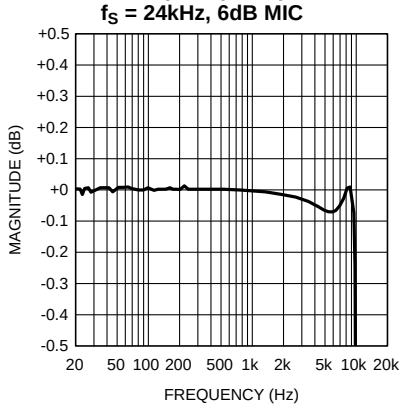


Figure 5-22.

MONO ADC Frequency Response
f_S = 24kHz, 36dB MIC

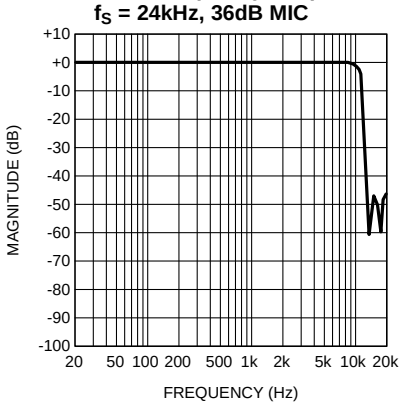


Figure 5-23.

MONO ADC Frequency Response Zoom
f_S = 24kHz, 36dB MIC

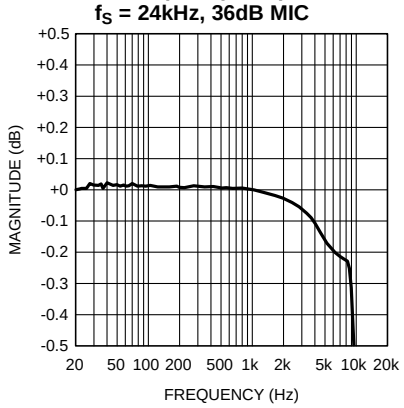


Figure 5-24.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

MONO ADC Frequency Response
f_S = 32kHz, 6dB MIC

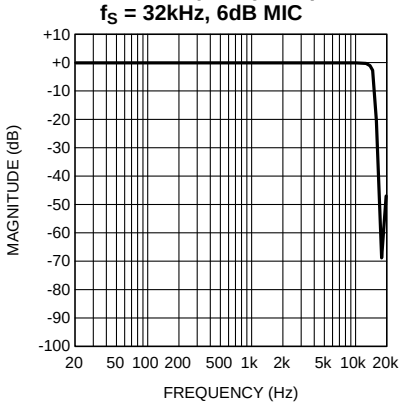


Figure 5-25.

MONO ADC Frequency Response Zoom
f_S = 32kHz, 6dB MIC

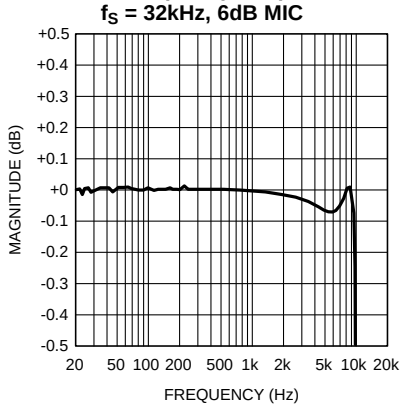


Figure 5-26.

MONO ADC Frequency Response
f_S = 32kHz, 36dB MIC

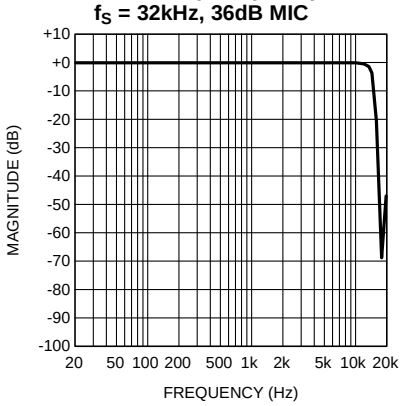


Figure 5-27.

MONO ADC Frequency Response Zoom
f_S = 32kHz, 36dB MIC

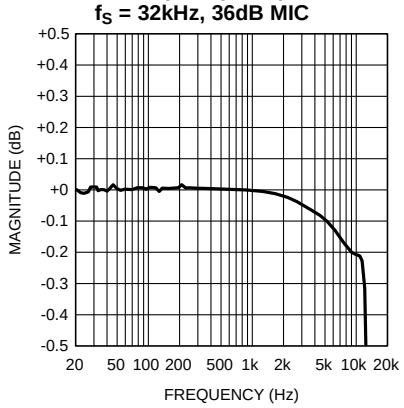


Figure 5-28.

MONO ADC HPF Frequency Response
f_S = 8kHz, 36dB MIC
(from left to right: HPF_MODE '00', '10', '01')

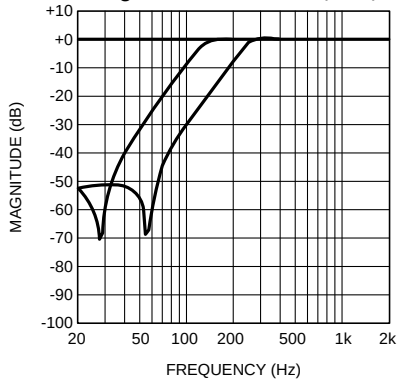


Figure 5-29.

MONO ADC HPF Frequency Response
f_S = 16kHz, 36dB MIC
(from left to right: HPF_MODE '00', '10', '01')

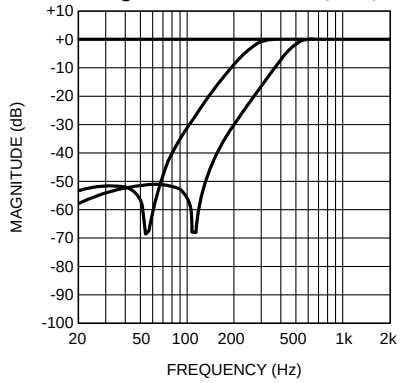


Figure 5-30.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

MONO ADC HPF Frequency Response
f_S = 24kHz, 36dB MIC
(from left to right: HPF_MODE '00', '10', '01')

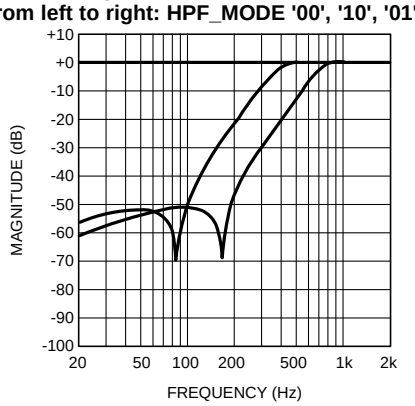


Figure 5-31.

MONO ADC HPF Frequency Response
f_S = 32kHz, 36dB MIC
(from left to right: HPF_MODE '00', '10', '01')

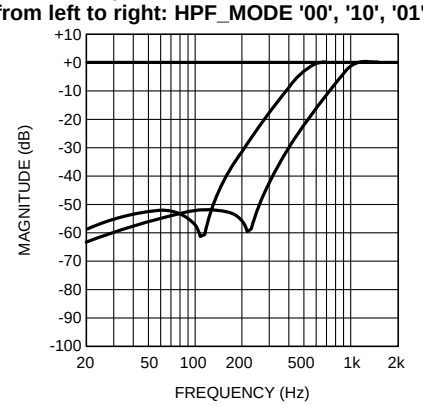


Figure 5-32.

MONO ADC THD+N
vs MIC Input Voltage
(f_S = 8kHz, 6dB MIC)

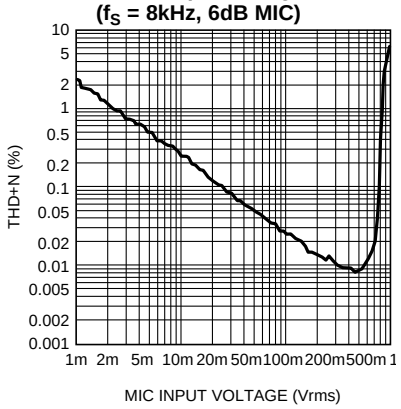


Figure 5-33.

MONO ADC THD+N
vs MIC Input Voltage
(f_S = 8kHz, 36dB MIC)

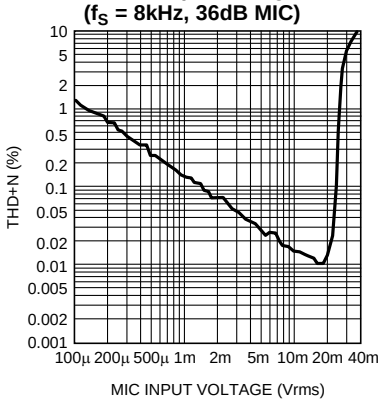


Figure 5-34.

MONO ADC PSRR
vs Frequency
AV_{DD} = 3.3V, 6dB MIC

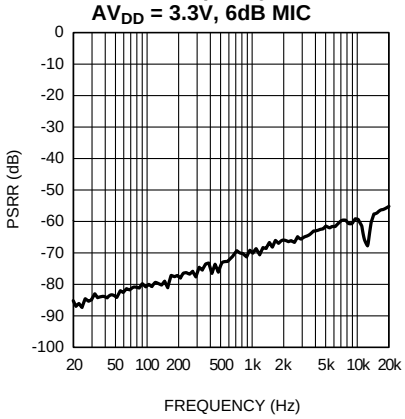


Figure 5-35.

MONO ADC PSRR
vs Frequency
AV_{DD} = 5V, 6dB MIC

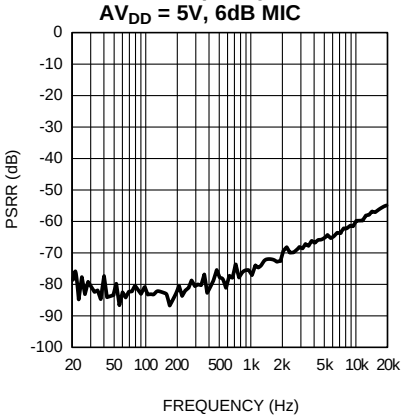


Figure 5-36.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

MONO ADC PSRR vs Frequency AV_{DD} = 3.3V, 36dB MIC

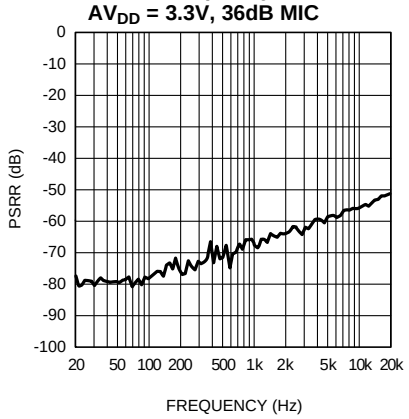


Figure 5-37.

MONO ADC PSRR vs Frequency AV_{DD} = 5V, 36dB MIC

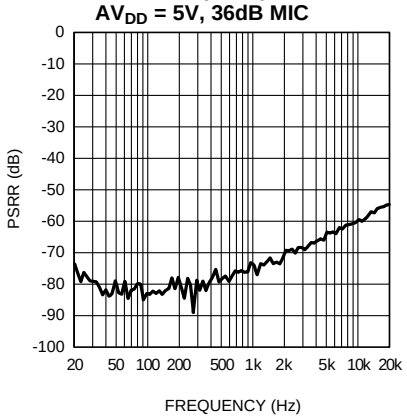


Figure 5-38.

AUXOUT PSRR vs Frequency AV_{DD} = 3.3V, 0dB AUX (AUX inputs terminated)

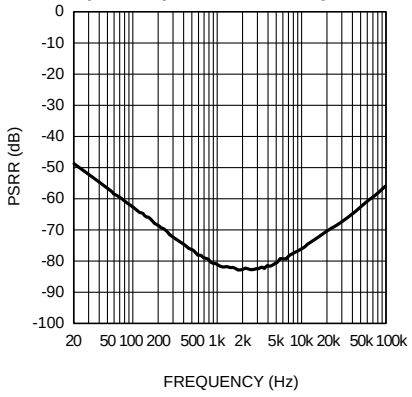


Figure 5-39.

AUXOUT PSRR vs Frequency AV_{DD} = 5V, 0dB AUX (AUX inputs terminated)

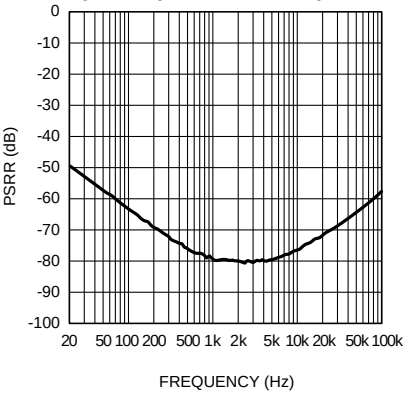


Figure 5-40.

AUXOUT PSRR vs Frequency AV_{DD} = 3.3V, 0dB CPI (CPI inputs terminated)

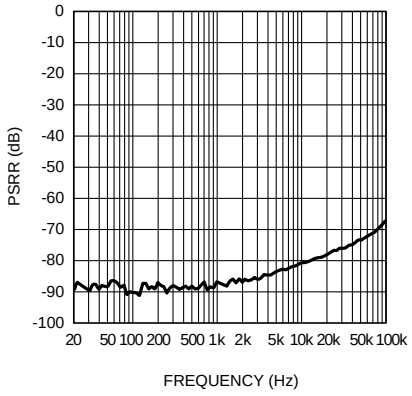


Figure 5-41.

AUXOUT PSRR vs Frequency AV_{DD} = 5V, 0dB CPI (CPI inputs terminated)

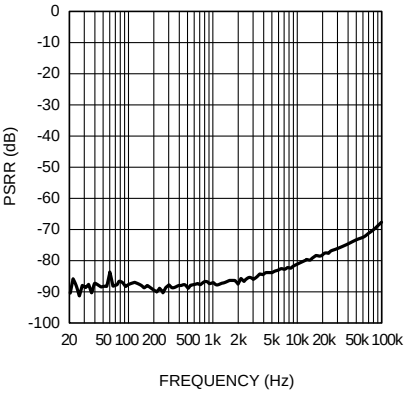


Figure 5-42.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

AUXOUT PSRR vs Frequency
AV_{DD} = 3.3V, 0dB DAC
(DAC inputs selected)

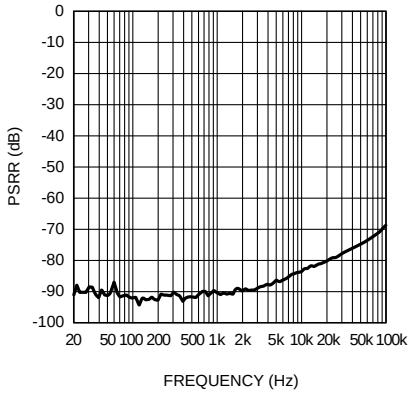


Figure 5-43.

AUXOUT PSRR vs Frequency
AV_{DD} = 5V, 0dB DAC
(DAC inputs selected)

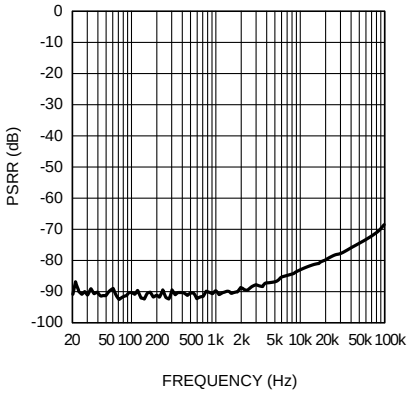


Figure 5-44.

CPOUT PSRR vs Frequency
AV_{DD} = 3.3V, 0dB AUX
(AUX inputs terminated)

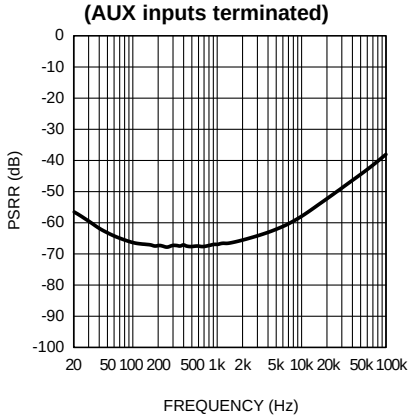


Figure 5-45.

CPOUT PSRR vs Frequency
AV_{DD} = 5V, 0dB AUX
(AUX inputs terminated)

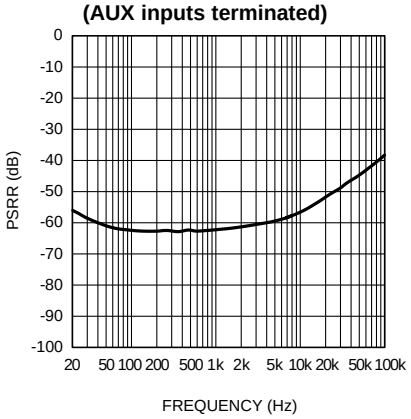


Figure 5-46.

CPOUT PSRR vs Frequency
AV_{DD} = 3.3V, 0dB DAC
(DAC inputs selected)

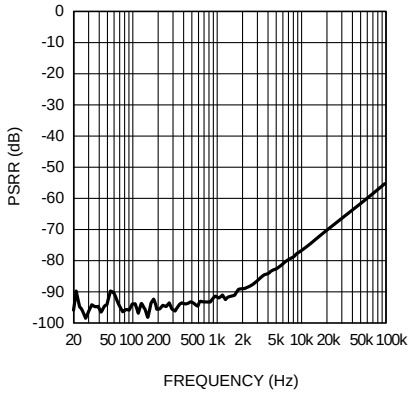


Figure 5-47.

CPOUT PSRR vs Frequency
AV_{DD} = 5V, 0dB DAC
(DAC inputs selected)

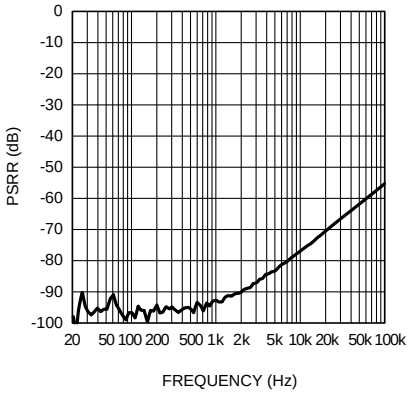


Figure 5-48.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

CPOUT PSRR vs Frequency
AV_{DD} = 3.3V, 36dB MIC
(EXTMIC inputs terminated, AGC on)

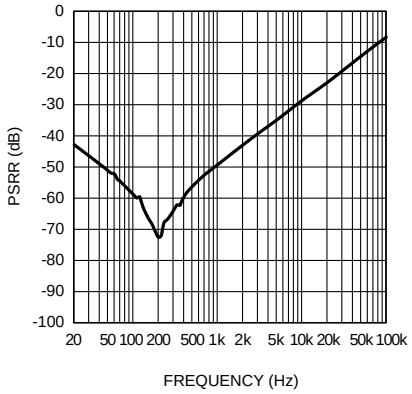


Figure 5-49.

CPOUT PSRR vs Frequency
AV_{DD} = 5V, 36dB MIC
(EXTMIC inputs terminated, AGC on)

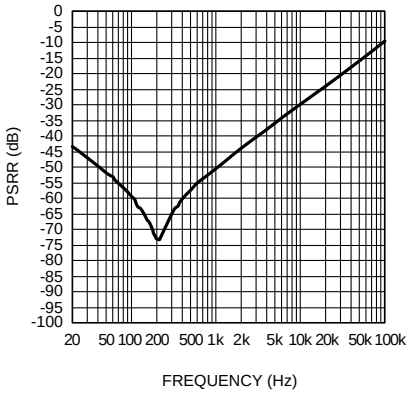


Figure 5-50.

CPOUT PSRR vs Frequency
AV_{DD} = 3.3V, 36dB MIC, MICBIAS = 2.0V
(INTMIC DIFF inputs terminated, AGC off)

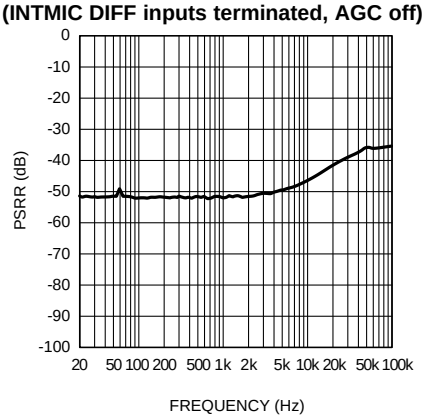


Figure 5-51.

CPOUT PSRR vs Frequency
AV_{DD} = 3.3V, 36dB MIC, MICBIAS = 2.0V
(INTMIC DIFF inputs terminated, AGC on)

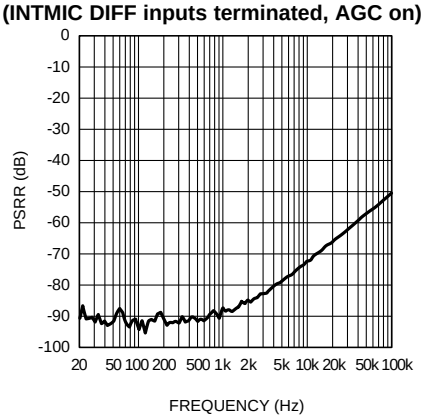


Figure 5-52.

CPOUT PSRR vs Frequency
AV_{DD} = 3.3V, 36dB MIC, MICBIAS = 2.5V
(INTMIC DIFF inputs terminated, AGC off)

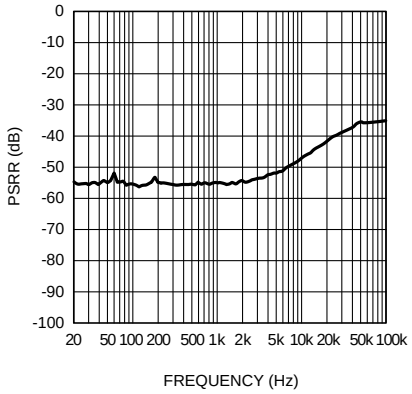


Figure 5-53.

CPOUT PSRR vs Frequency
AV_{DD} = 3.3V, 36dB MIC, MICBIAS = 2.5V
(INTMIC DIFF inputs terminated, AGC on)

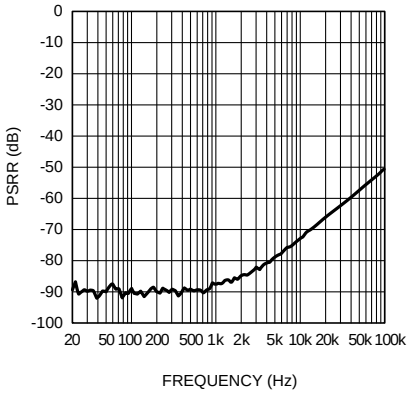


Figure 5-54.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

CPOUT PSRR vs Frequency
AV_{DD} = 3.3V, 36dB MIC, MICBIAS = 2.8V
(INTMIC DIFF inputs terminated, AGC off)

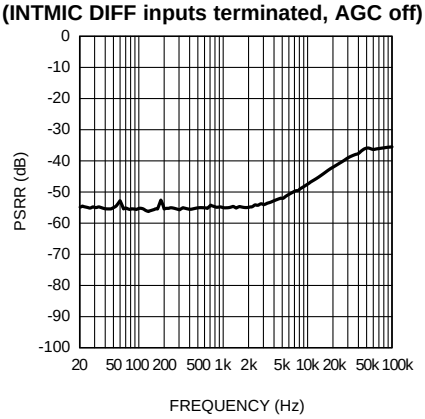


Figure 5-55.

CPOUT PSRR vs Frequency
AV_{DD} = 3.3V, 36dB MIC, MICBIAS = 2.8V
(INTMIC DIFF inputs terminated, AGC on)

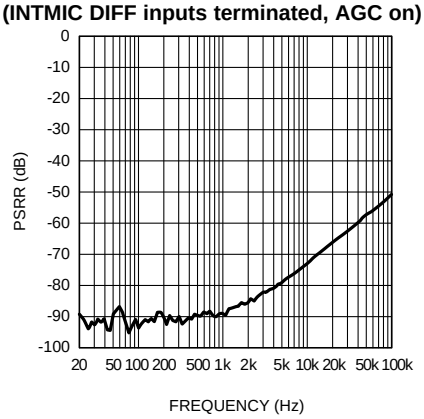


Figure 5-56.

CPOUT PSRR vs Frequency
AV_{DD} = 5V, 36dB MIC, MICBIAS = 2.0V
(INTMIC DIFF inputs terminated, AGC off)

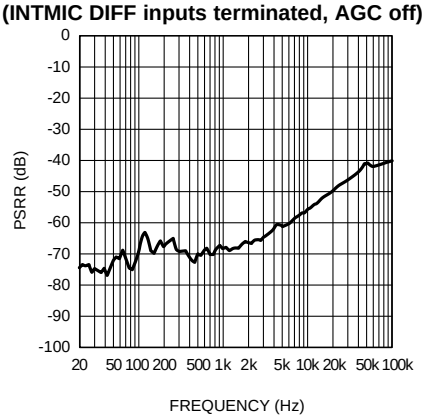


Figure 5-57.

CPOUT PSRR vs Frequency
AV_{DD} = 5V, 36dB MIC, MICBIAS = 2.0V
(INTMIC DIFF inputs terminated, AGC on)

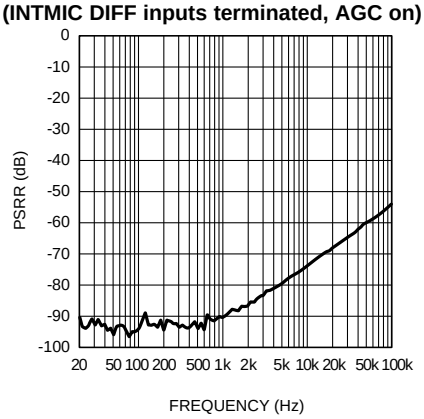


Figure 5-58.

CPOUT PSRR vs Frequency
AV_{DD} = 5V, 36dB MIC, MICBIAS = 2.5V
(INTMIC DIFF inputs terminated, AGC off)

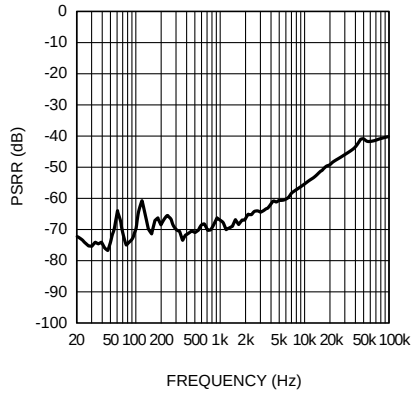


Figure 5-59.

CPOUT PSRR vs Frequency
AV_{DD} = 5V, 36dB MIC, MICBIAS = 2.5V
(INTMIC DIFF inputs terminated, AGC on)

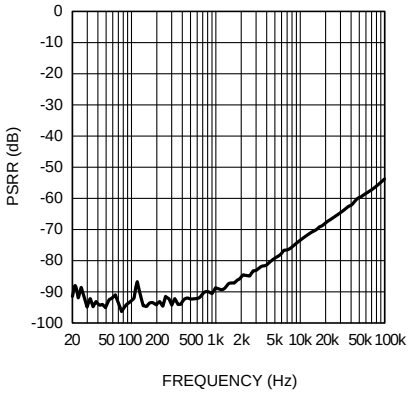


Figure 5-60.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

CPOUT PSRR vs Frequency
AV_{DD} = 5V, 36dB MIC, MICBIAS = 2.8V
(INTMIC DIFF inputs terminated, AGC off)

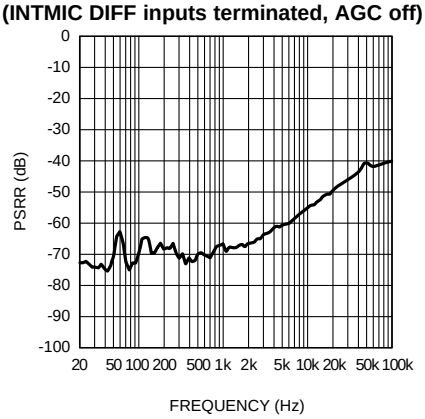


Figure 5-61.

CPOUT PSRR vs Frequency
AV_{DD} = 5V, 36dB MIC, MICBIAS = 2.8V
(INTMIC DIFF inputs terminated, AGC on)

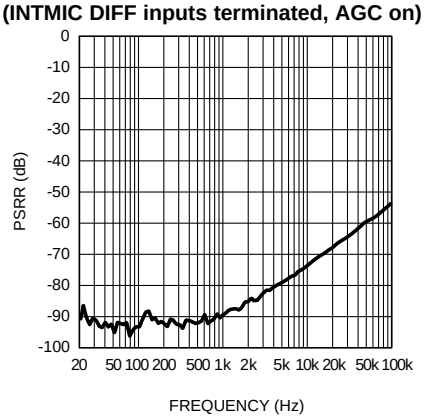


Figure 5-62.

CPOUT PSRR vs Frequency
AV_{DD} = 5V, 36dB MIC, MICBIAS = 3.3V
(INTMIC DIFF inputs terminated, AGC off)

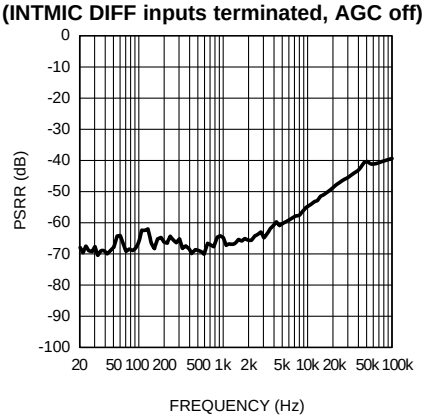


Figure 5-63.

CPOUT PSRR vs Frequency
AV_{DD} = 5V, 36dB MIC, MICBIAS = 3.3V
(INTMIC DIFF inputs terminated, AGC on)

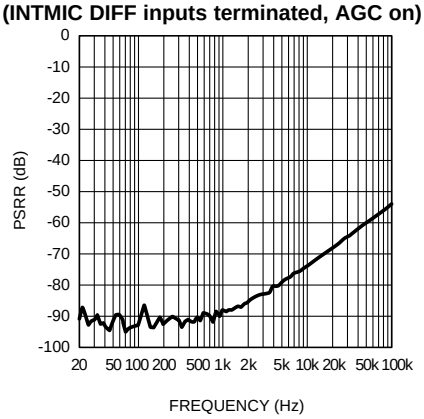


Figure 5-64.

CPOUT PSRR vs Frequency
AV_{DD} = 3.3V, 36dB MIC
(INTMIC SE input terminated, AGC on)

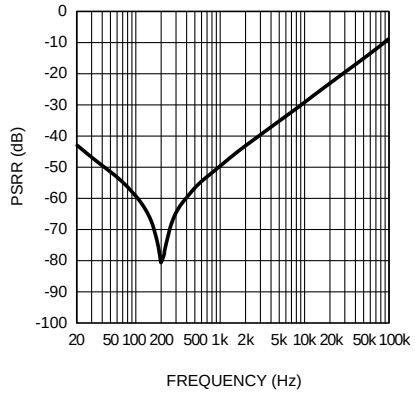


Figure 5-65.

CPOUT PSRR vs Frequency
AV_{DD} = 5V, 36dB MIC
(INTMIC SE input terminated, AGC on)

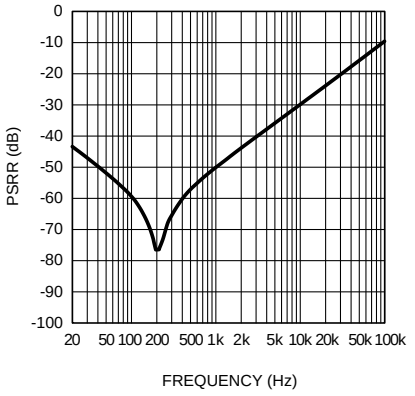


Figure 5-66.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Earpiece PSRR vs Frequency
AV_{DD} = 3.3V, 0dB AUX
(AUX inputs terminated)

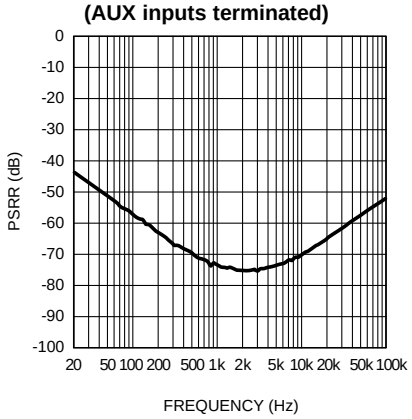


Figure 5-67.

Earpiece PSRR vs Frequency
AV_{DD} = 5V, 0dB AUX
(AUX inputs terminated)

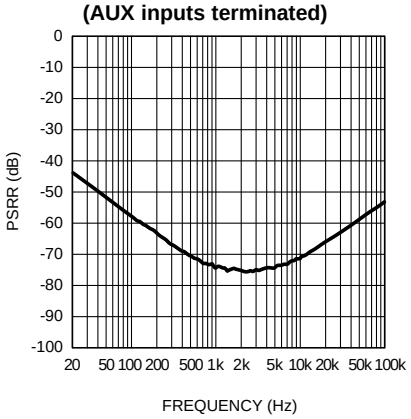


Figure 5-68.

Earpiece PSRR vs Frequency
AV_{DD} = 3.3V, 0dB CPI
(CPI input terminated)

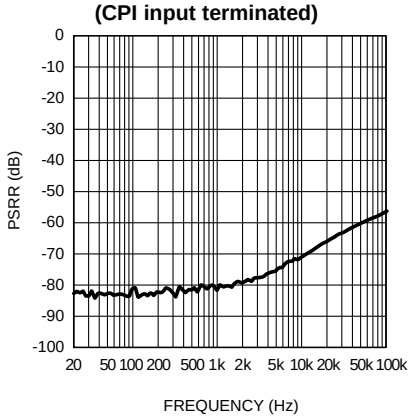


Figure 5-69.

Earpiece PSRR vs Frequency
AV_{DD} = 5V, 0dB CPI
(CPI input terminated)

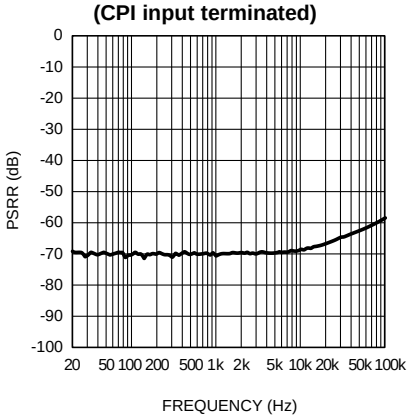


Figure 5-70.

Earpiece PSRR vs Frequency
AV_{DD} = 3.3V, 0dB DAC
(DAC input selected)

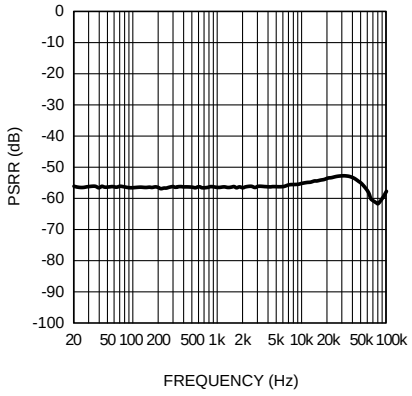


Figure 5-71.

Earpiece PSRR vs Frequency
AV_{DD} = 5V, 0dB DAC
(DAC input selected)

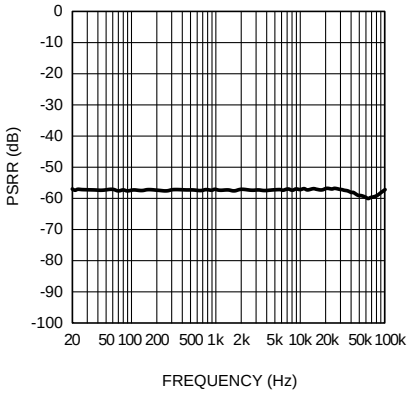


Figure 5-72.

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Headphone PSRR vs Frequency
AV_{DD} = 3.3V, 0dB AUX, OCL 1.2V
(AUX inputs terminated)

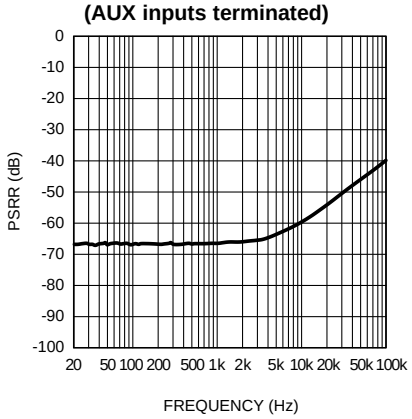


Figure 5-73.

Headphone PSRR vs Frequency
AV_{DD} = 5V, 0dB AUX, OCL 1.2V
(AUX inputs terminated)

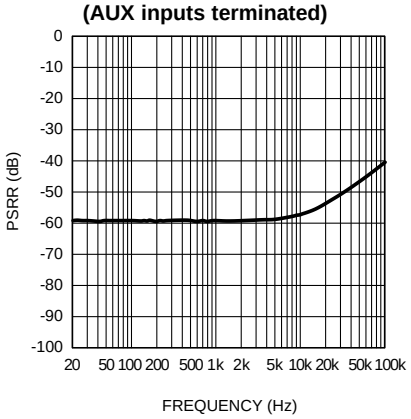


Figure 5-74.

Headphone PSRR vs Frequency
AV_{DD} = 3.3V, 0dB CPI, OCL 1.2V
(CPI input terminated)

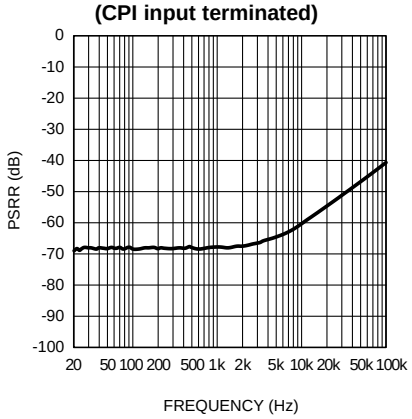


Figure 5-75.

Headphone PSRR vs Frequency
AV_{DD} = 5V, 0dB CPI, OCL 1.2V
(CPI input terminated)

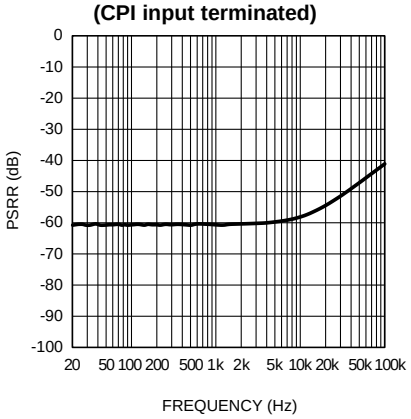


Figure 5-76.

Headphone PSRR vs Frequency
AV_{DD} = 3.3V, 0dB ADC, OCL 1.2V
(DAC input selected)

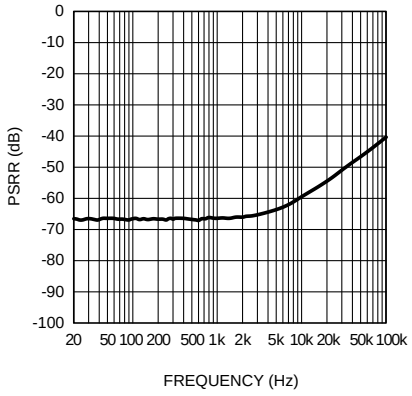


Figure 5-77.

Headphone PSRR vs Frequency
AV_{DD} = 5V, 0dB ADC, OCL 1.2V
(DAC input selected)

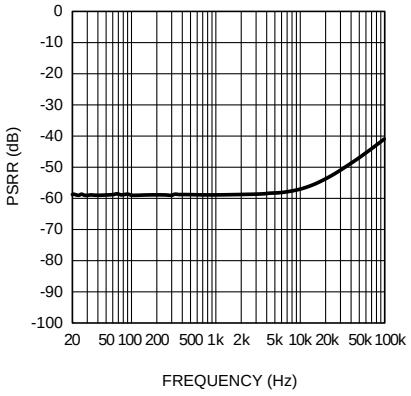


Figure 5-78.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Headphone PSRR vs Frequency
AV_{DD} = 3.3V, 0dB AUX, OCL 1.5V
(AUX inputs terminated)

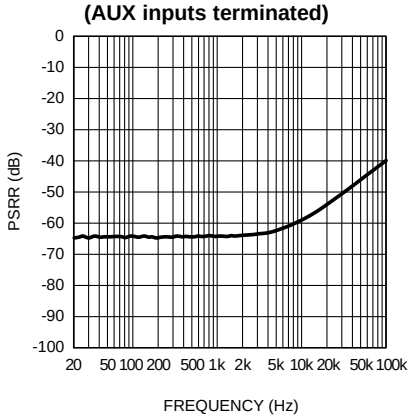


Figure 5-79.

Headphone PSRR vs Frequency
AV_{DD} = 5V, 0dB AUX, OCL 1.5V
(AUX inputs terminated)

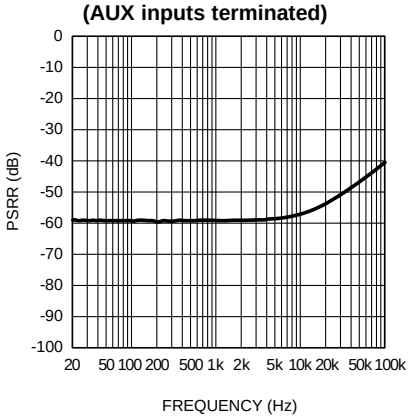


Figure 5-80.

Headphone PSRR vs Frequency
AV_{DD} = 3.3V, 0dB CPI, OCL 1.5V
(CPI input terminated)

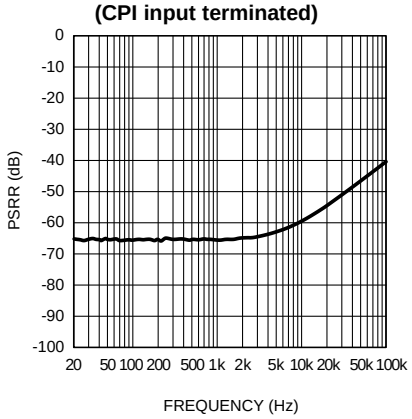


Figure 5-81.

Headphone PSRR vs Frequency
AV_{DD} = 5V, 0dB CPI, OCL 1.5V
(CPI input terminated)

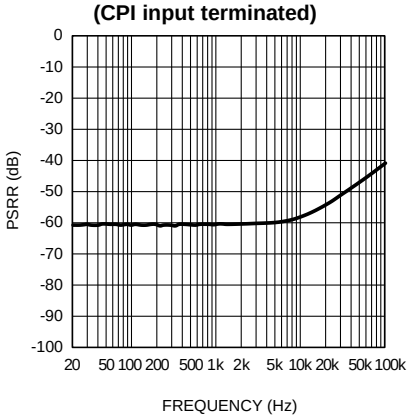


Figure 5-82.

Headphone PSRR vs Frequency
AV_{DD} = 3.3V, 0dB DAC, OCL 1.5V
(DAC input selected)

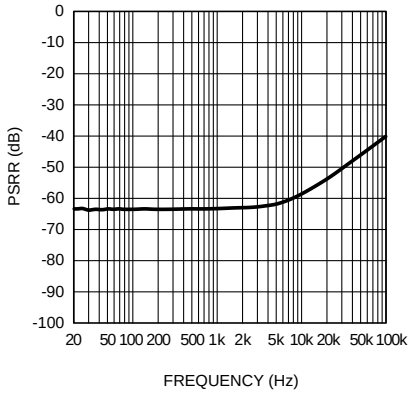


Figure 5-83.

Headphone PSRR vs Frequency
AV_{DD} = 5V, 0dB DAC, OCL 1.5V
(DAC input selected)

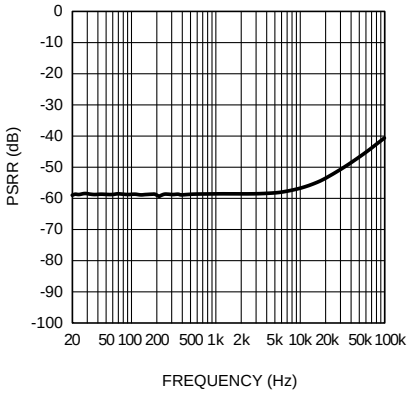


Figure 5-84.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Headphone PSRR vs Frequency
AV_{DD} = 3.3V, 0dB AUX, SE
(AUX inputs terminated)

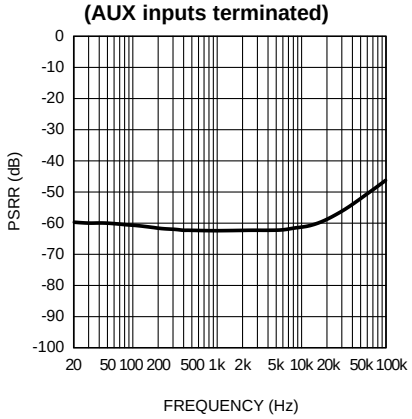


Figure 5-85.

Headphone PSRR vs Frequency
AV_{DD} = 5V, 0dB AUX, SE
(AUX inputs terminated)

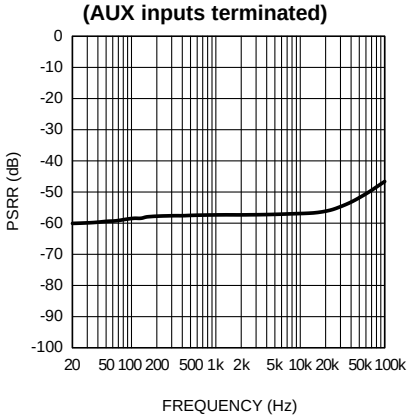


Figure 5-86.

Headphone PSRR vs Frequency
AV_{DD} = 3.3V, 0dB CPI, SE
(CPI input terminated)

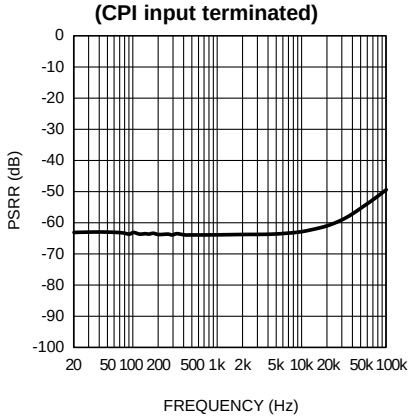


Figure 5-87.

Headphone PSRR vs Frequency
AV_{DD} = 5V, 0dB CPI, SE
(CPI input terminated)

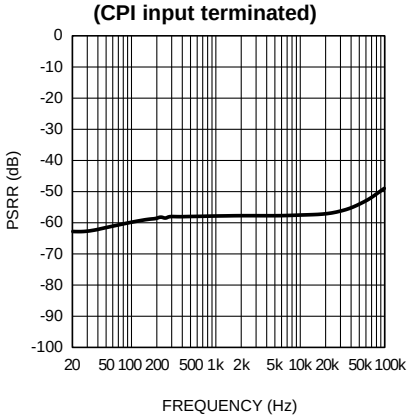


Figure 5-88.

Headphone PSRR vs Frequency
AV_{DD} = 3.3V, 0dB DAC, SE
(DAC input selected)

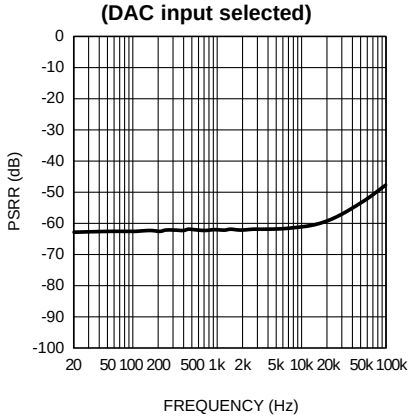


Figure 5-89.

Headphone PSRR vs Frequency
AV_{DD} = 5V, 0dB DAC, SE
(DAC input selected)

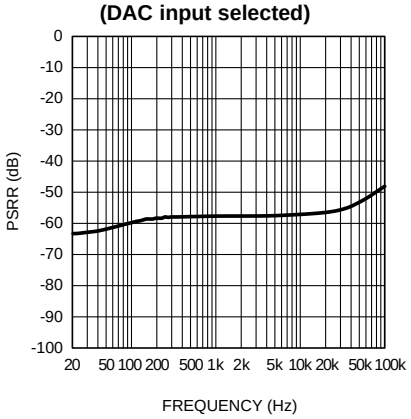


Figure 5-90.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Loudspeaker PSRR vs Frequency
AV_{DD} = 3.3V, 0dB AUX
(AUX inputs terminated)

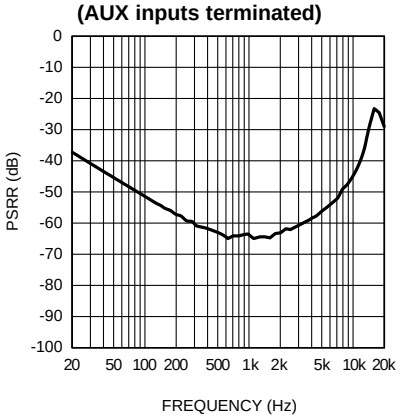


Figure 5-91.

Loudspeaker PSRR vs Frequency
AV_{DD} = 5V, 0dB AUX
(AUX inputs terminated)

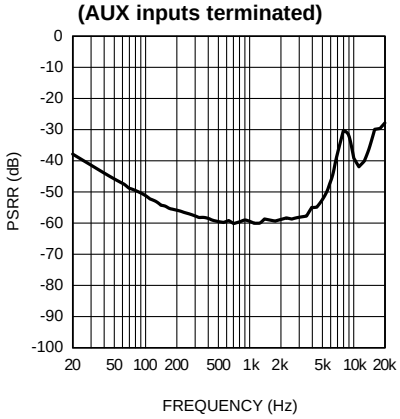


Figure 5-92.

Loudspeaker PSRR vs Frequency
AV_{DD} = 3.3V, 0dB CPI
(CPI input terminated)

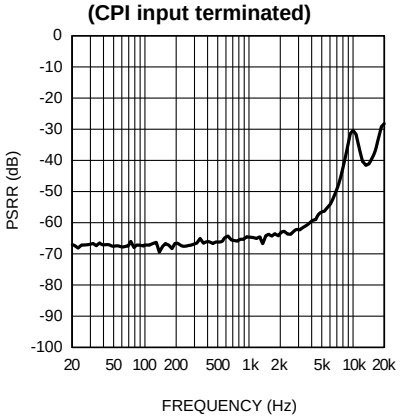


Figure 5-93.

Loudspeaker PSRR vs Frequency
AV_{DD} = 5V, 0dB CPI
(CPI input terminated)

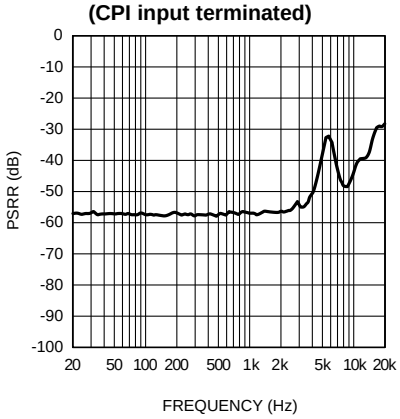


Figure 5-94.

Loudspeaker PSRR vs Frequency
AV_{DD} = 3.3V, 0dB DAC
(DAC input selected)

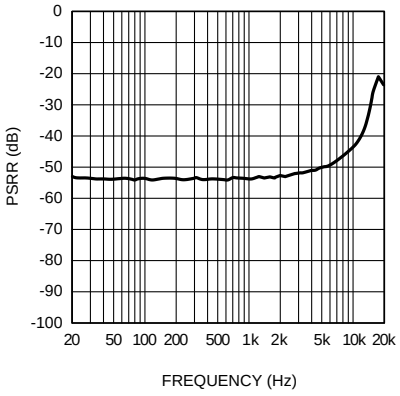


Figure 5-95.

Loudspeaker PSRR vs Frequency
AV_{DD} = 5V, 0dB DAC
(DAC input selected)

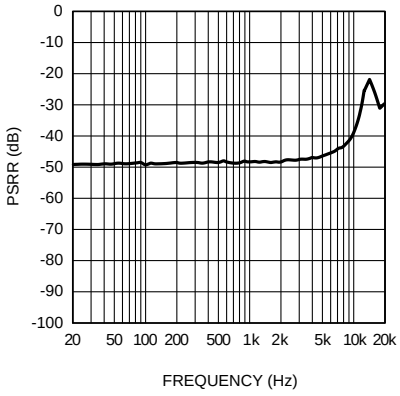


Figure 5-96.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

INT/EXT MICBIAS PSRR vs Frequency
AV_{DD} = 3.3V, MICBIAS = 2.0V

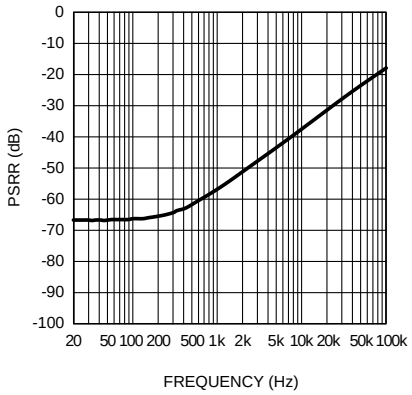


Figure 5-97.

INT/EXT MICBIAS PSRR vs Frequency
AV_{DD} = 5V, MICBIAS = 2.0V

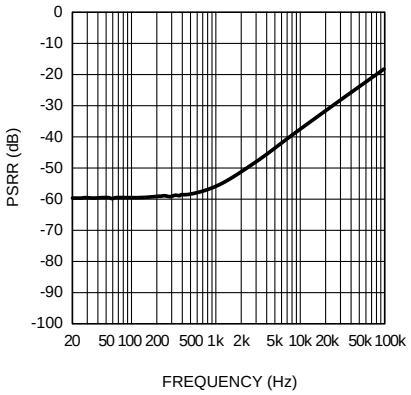


Figure 5-98.

INT/EXT MICBIAS PSRR vs Frequency
AV_{DD} = 3.3V, MICBIAS = 2.5V

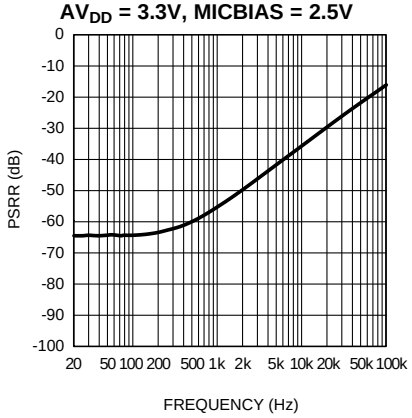


Figure 5-99.

INT/EXT MICBIAS PSRR vs Frequency
AV_{DD} = 5V, MICBIAS = 2.5V

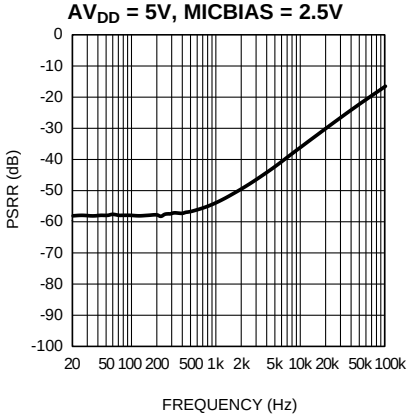


Figure 5-100.

INT/EXT MICBIAS PSRR
vs Frequency
AV_{DD} = 3.3V, MICBIAS = 2.8V

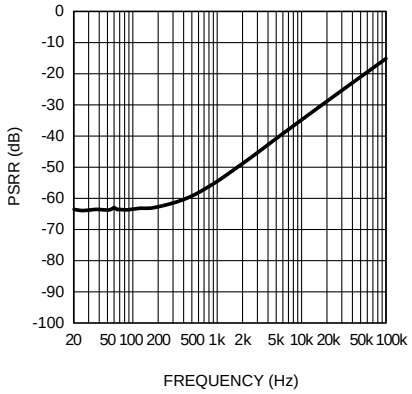


Figure 5-101.

INT/EXT MICBIAS PSRR
vs Frequency
AV_{DD} = 5V, MICBIAS = 2.8V

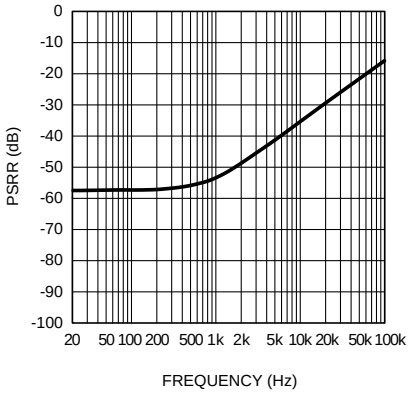


Figure 5-102.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

INT/EXT MICBIAS PSRR vs Frequency
AV_{DD} = 5V, MICBIAS = 3.3V

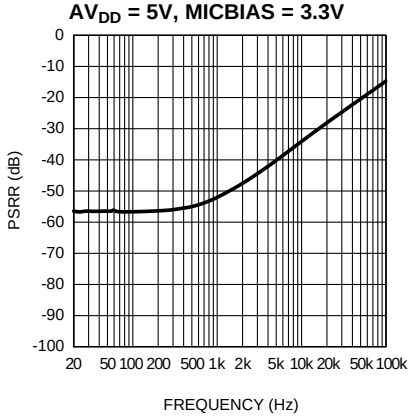


Figure 5-103.

AUXOUT THD+N vs Frequency
AV_{DD} = 3.3V, 0dB, V_{OUT} = 1V_{RMS}, 5kΩ

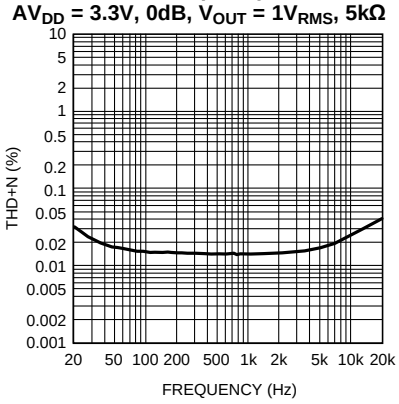


Figure 5-104.

AUXOUT THD+N vs Frequency
AV_{DD} = 5V, 0dB, V_{OUT} = 1V_{RMS}, 5kΩ

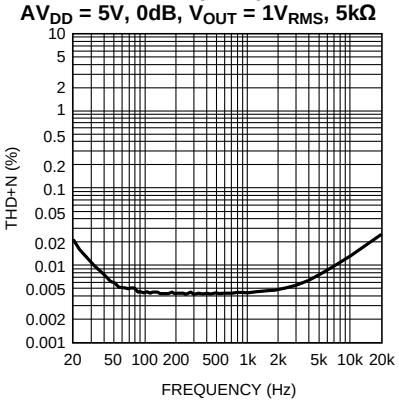


Figure 5-105.

CPOUT THD+N vs Frequency
AV_{DD} = 3.3V, 0dB, V_{OUT} = 1V_{RMS}, 5kΩ

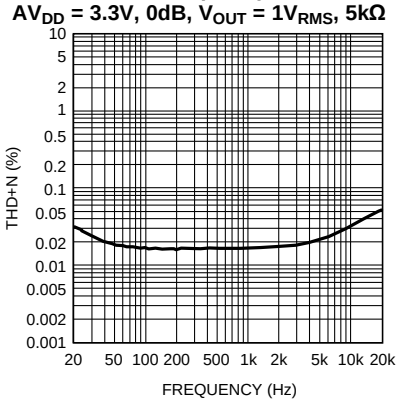


Figure 5-106.

CPOUT THD+N vs Frequency
AV_{DD} = 5V, 0dB, V_{OUT} = 1V_{RMS}, 5kΩ

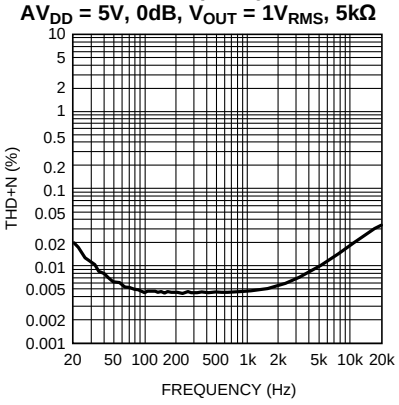


Figure 5-107.

Earpiece THD+N vs Frequency
AV_{DD} = 3.3V, 0dB, P_{OUT} = 500mW, 32Ω

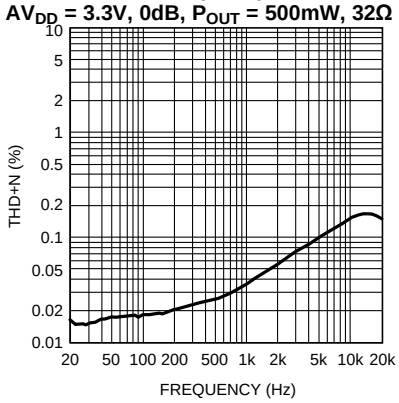


Figure 5-108.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Earpiece THD+N vs Frequency AV_{DD} = 5V, 0dB, P_{OUT} = 50mW, 32Ω

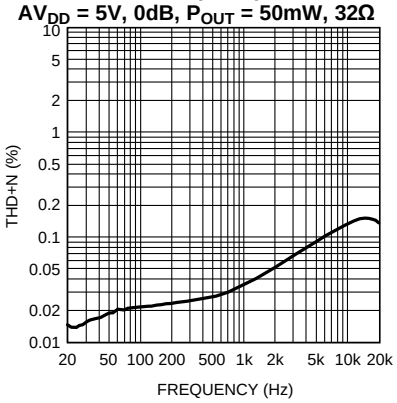


Figure 5-109.

Headphone THD+N vs Frequency AV_{DD} = 3.3V, OCL 1.5V, 0dB P_{OUT} = 7.5mW, 32Ω

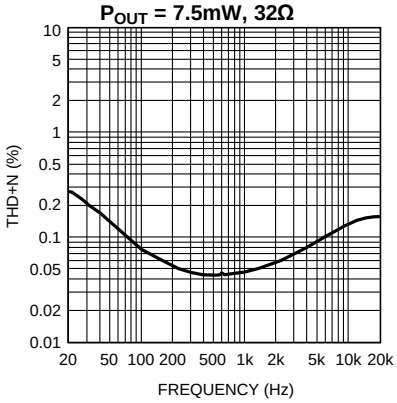


Figure 5-110.

Headphone THD+N vs Frequency AV_{DD} = 5V, OCL 1.5V, 0dB P_{OUT} = 10mW, 32Ω

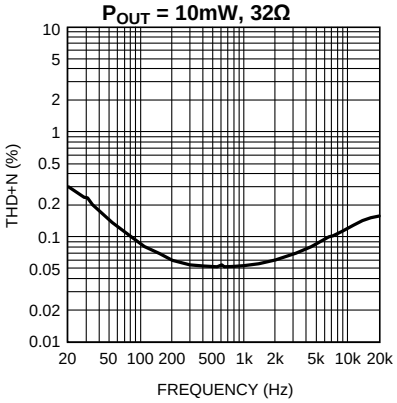


Figure 5-111.

Headphone THD+N vs Frequency AV_{DD} = 3.3V, OCL 1.2V, 0dB P_{OUT} = 7.5mW, 32Ω

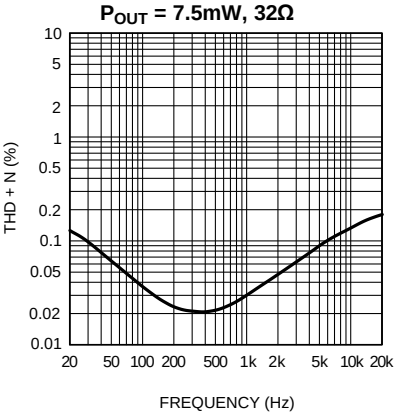


Figure 5-112.

Headphone THD+N vs Frequency AV_{DD} = 5V, OCL 1.2V, 0dB P_{OUT} = 10mW, 32Ω

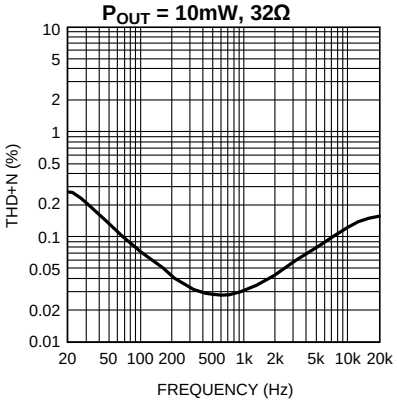


Figure 5-113.

Headphone THD+N vs Frequency AV_{DD} = 3.3V, SE, 0dB P_{OUT} = 7.5mW, 32Ω

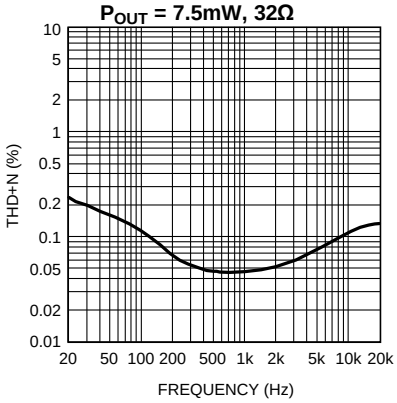


Figure 5-114.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Headphone THD+N vs Frequency AV_{DD} = 5V, SE, 0dB P_{OUT} = 10mW, 32Ω

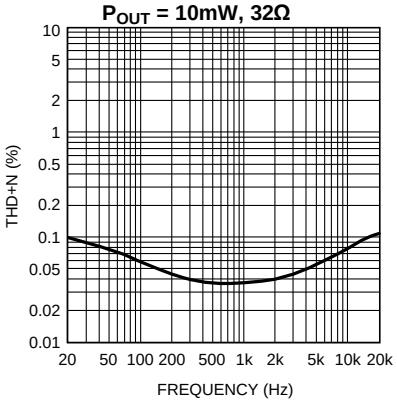


Figure 5-115.

Loudspeaker THD+N vs Frequency AV_{DD} = 3.3V, P_{OUT} = 400mW 15µH+8Ω+15µH

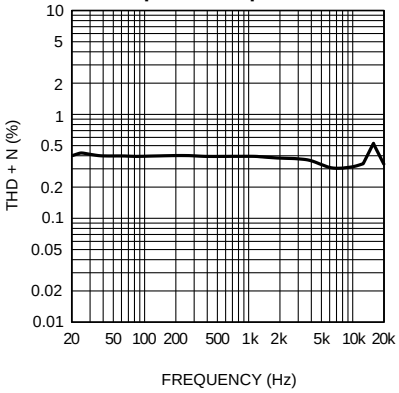


Figure 5-116.

Loudspeaker THD+N vs Frequency AV_{DD} = 5V, P_{OUT} = 400mW 15µH+8Ω+15µH

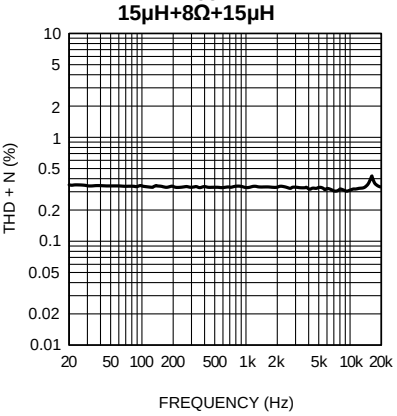


Figure 5-117.

Earpiece THD+N vs Output Power AV_{DD} = 3.3V, 0dB AUX f_{OUT} = 1kHz, 16Ω

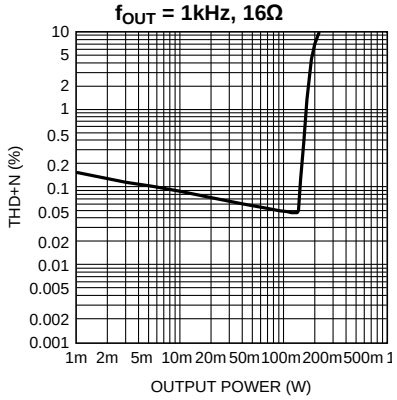


Figure 5-118.

Earpiece THD+N vs Output Power AV_{DD} = 5V, 0dB AUX f_{OUT} = 1kHz, 16Ω

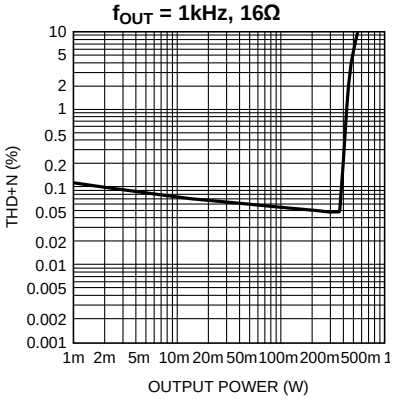


Figure 5-119.

Earpiece THD+N vs Output Power AV_{DD} = 3.3V, 0dB AUX f_{OUT} = 1kHz, 32Ω

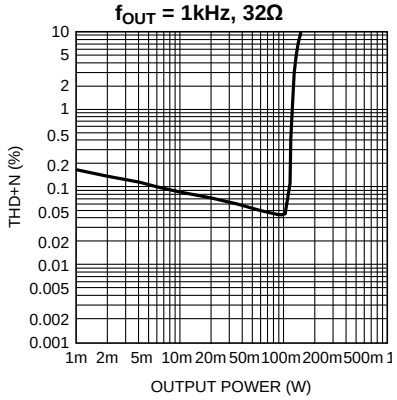


Figure 5-120.

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Earpiece THD+N vs Output Power AV_{DD} = 5V, 0dB AUX f_{OUT} = 1kHz, 32Ω

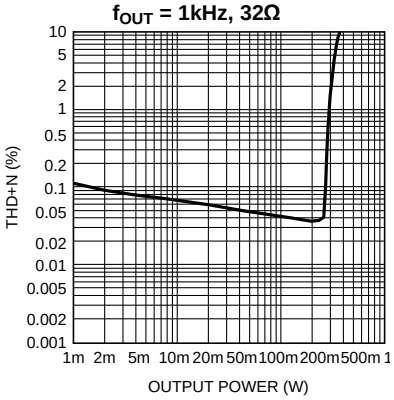


Figure 5-121.

Earpiece THD+N vs Output Power AV_{DD} = 3.3V, 0dB CPI f_{OUT} = 1kHz, 16Ω

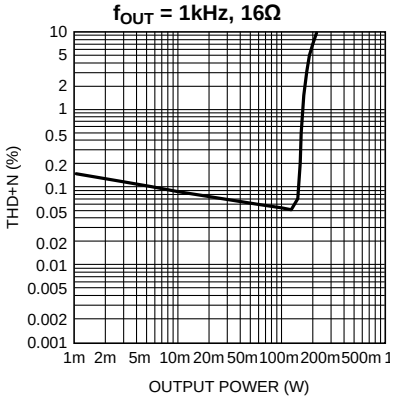


Figure 5-122.

Earpiece THD+N vs Output Power AV_{DD} = 5V, 0dB CPI f_{OUT} = 1kHz, 16Ω

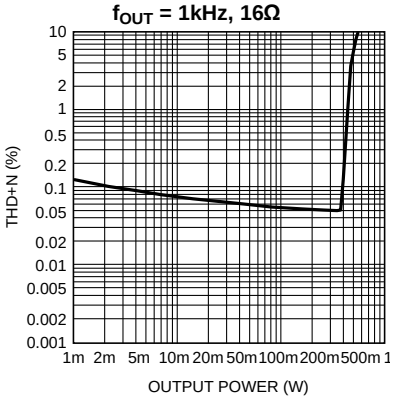


Figure 5-123.

Earpiece THD+N vs Output Power AV_{DD} = 3.3V, 0dB CPI f_{OUT} = 1kHz, 32Ω

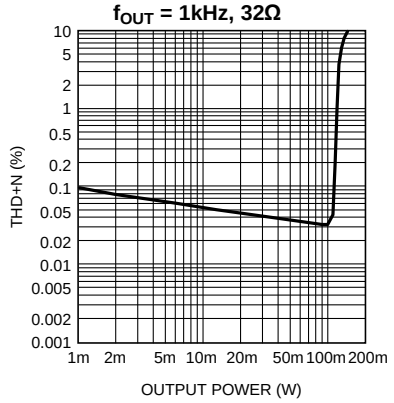


Figure 5-124.

Earpiece THD+N vs Output Power AV_{DD} = 5V, 0dB CPI f_{OUT} = 1kHz, 32Ω

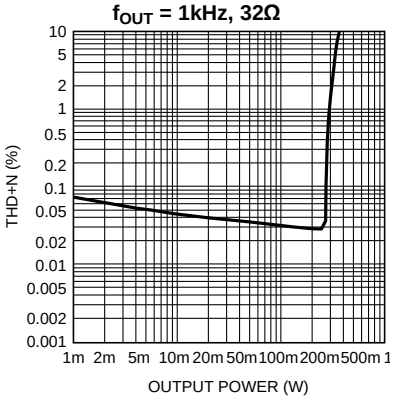


Figure 5-125.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 0dB DAC f_{OUT} = 1kHz, 16Ω

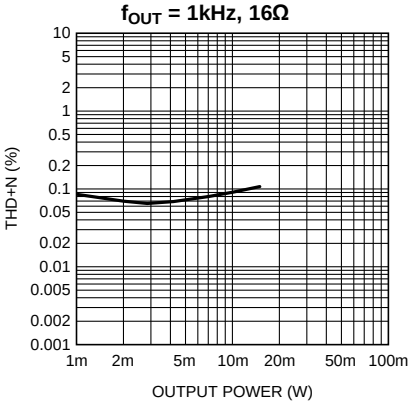


Figure 5-126.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 0dB DAC f_{OUT} = 1kHz, 16Ω

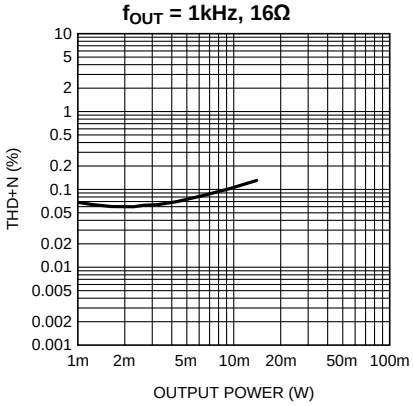


Figure 5-127.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 0dB DAC f_{OUT} = 1kHz, 32Ω

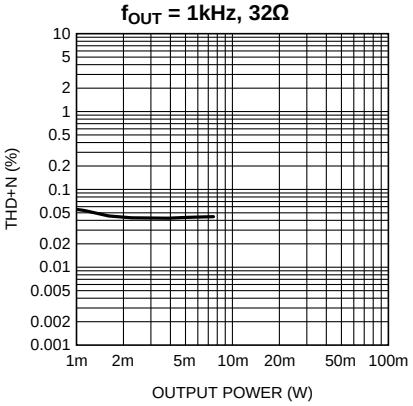


Figure 5-128.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 0dB DAC f_{OUT} = 1kHz, 32Ω

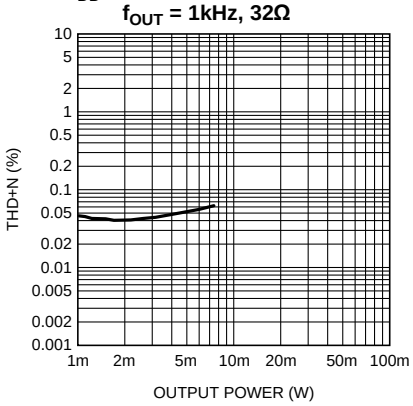


Figure 5-129.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 12dB DAC f_{OUT} = 1kHz, 16Ω

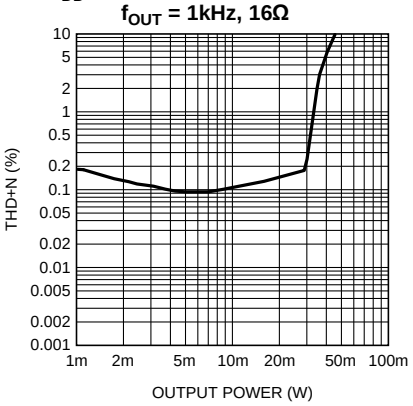


Figure 5-130.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 12dB DAC f_{OUT} = 1kHz, 16Ω

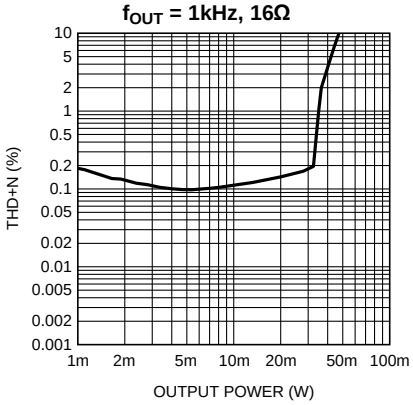


Figure 5-131.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 12dB DAC f_{OUT} = 1kHz, 32Ω

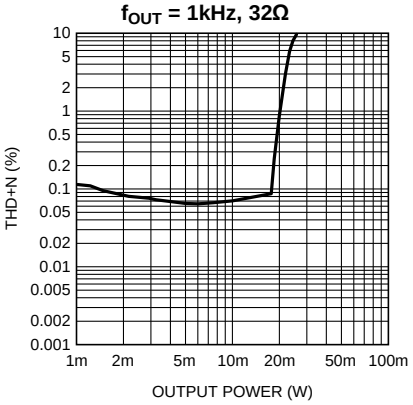


Figure 5-132.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 12dB DAC f_{OUT} = 1kHz, 32Ω

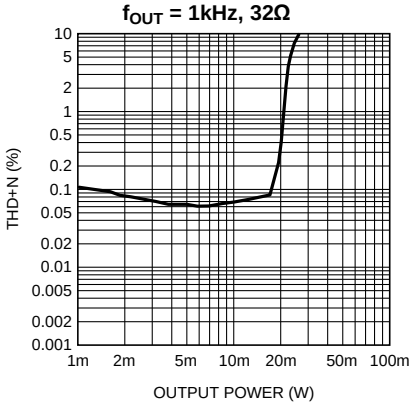


Figure 5-133.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 0dB DAC f_{OUT} = 1kHz, 16Ω

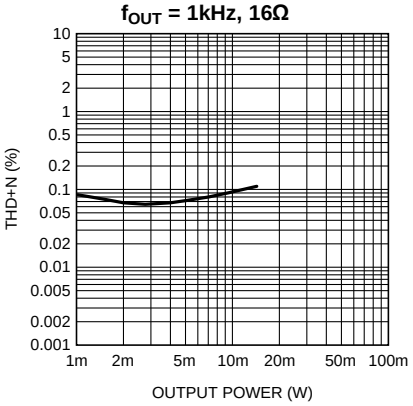


Figure 5-134.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 0dB DAC f_{OUT} = 1kHz, 16Ω

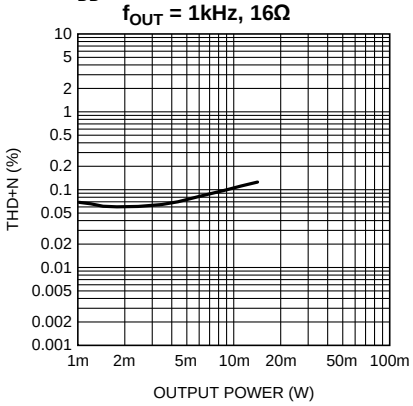


Figure 5-135.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 0dB DAC f_{OUT} = 1kHz, 32Ω

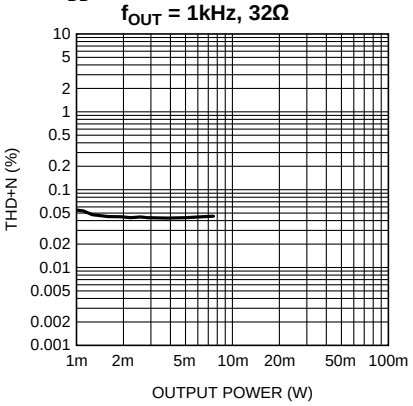


Figure 5-136.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 0dB DAC f_{OUT} = 1kHz, 32Ω

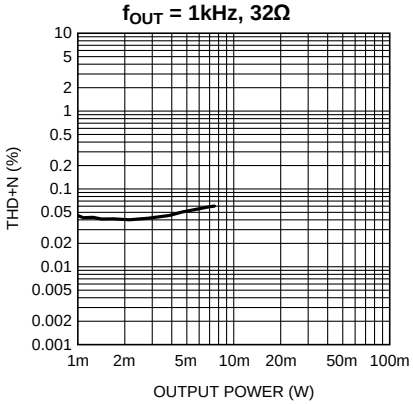


Figure 5-137.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 12dB DAC f_{OUT} = 1kHz, 16Ω

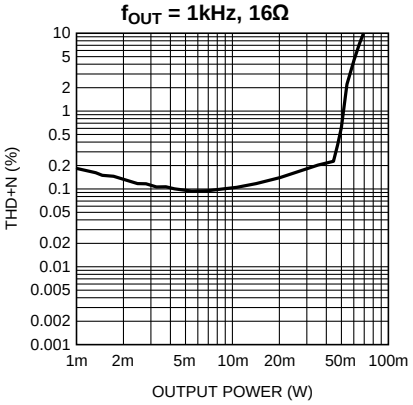


Figure 5-138.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 12dB DAC f_{OUT} = 1kHz, 16Ω

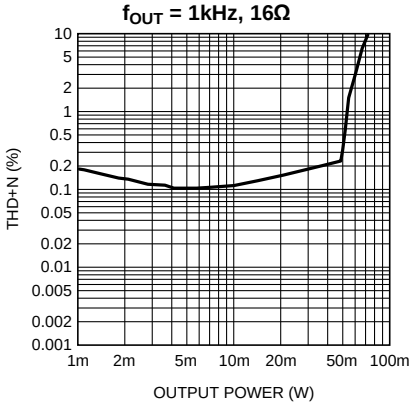


Figure 5-139.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 12dB DAC f_{OUT} = 1kHz, 32Ω

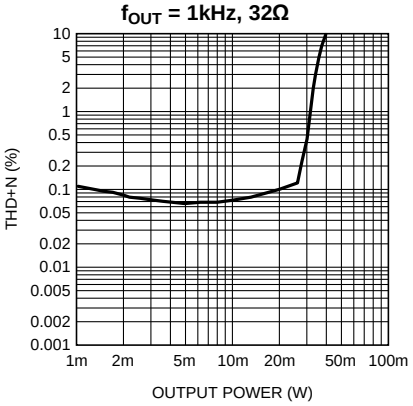


Figure 5-140.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 12dB DAC f_{OUT} = 1kHz, 32Ω

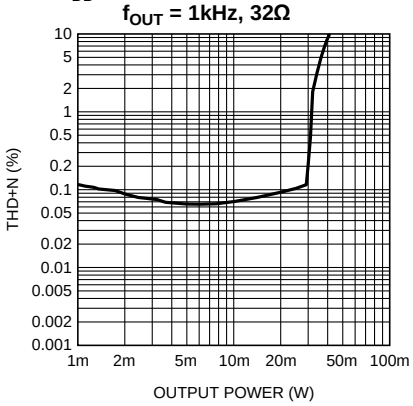


Figure 5-141.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 0dB DAC f_{OUT} = 1kHz, 16Ω

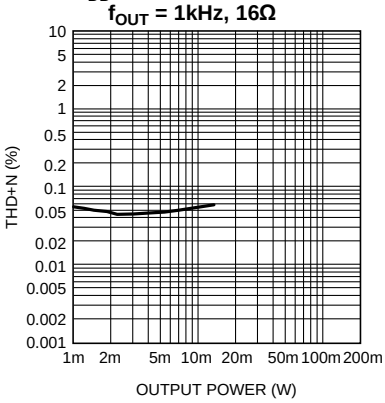


Figure 5-142.

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 0dB DAC f_{OUT} = 1kHz, 16Ω

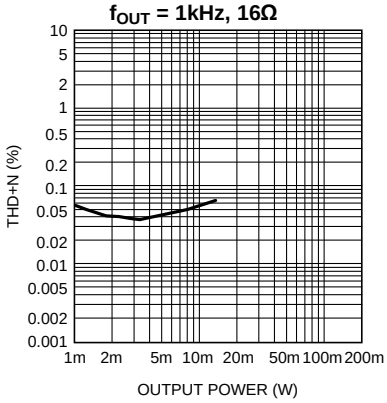


Figure 5-143.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 0dB DAC f_{OUT} = 1kHz, 32Ω

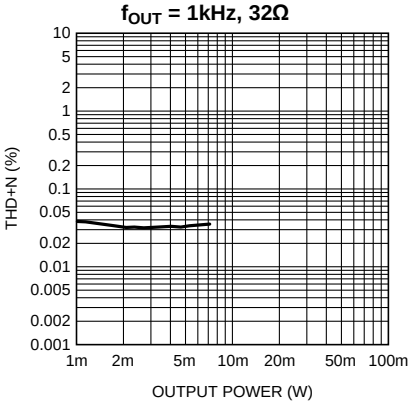


Figure 5-144.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Headphone THD+N F vs Output Power AV_{DD} = 5V, SE, 0dB DAC f_{OUT} = 1kHz, 32Ω

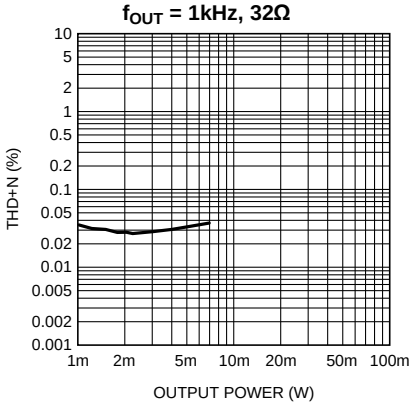


Figure 5-145.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 12dB DAC f_{OUT} = 1kHz, 16Ω

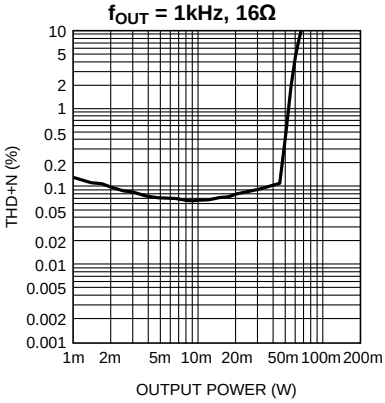


Figure 5-146.

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 12dB DAC f_{OUT} = 1kHz, 16Ω

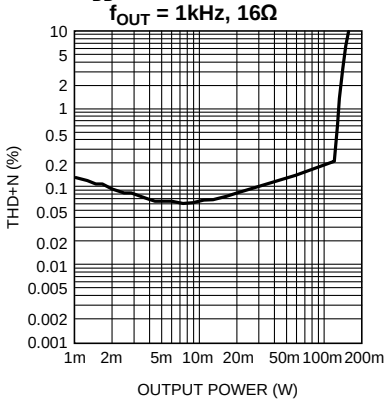


Figure 5-147.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 12dB DAC f_{OUT} = 1kHz, 32Ω

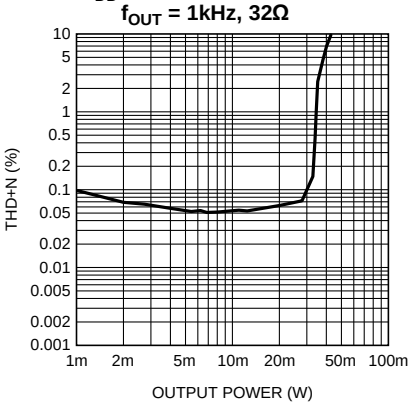


Figure 5-148.

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 12dB DAC f_{OUT} = 1kHz, 32Ω

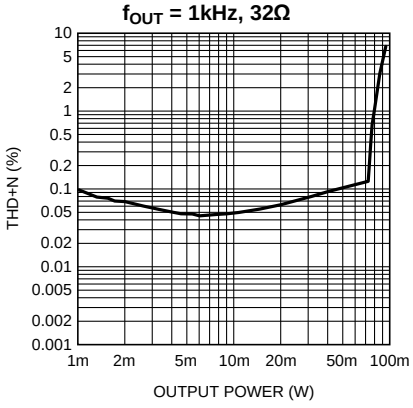


Figure 5-149.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 0dB AUX f_{OUT} = 1kHz, 16Ω

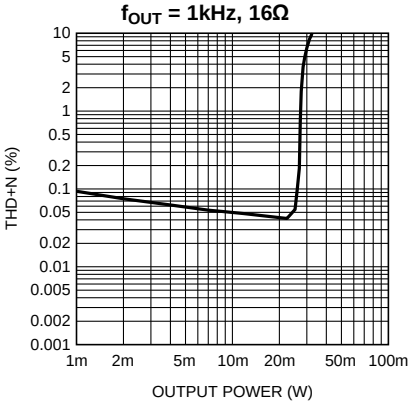


Figure 5-150.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 12dB AUX f_{OUT} = 1kHz, 16Ω

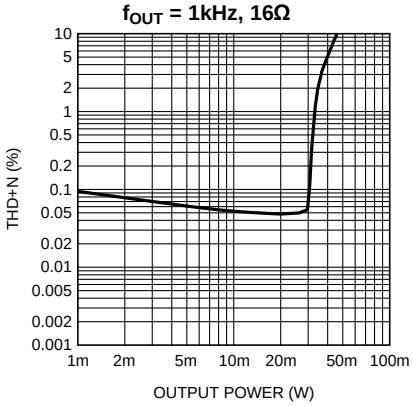


Figure 5-151.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 0dB AUX f_{OUT} = 1kHz, 16Ω

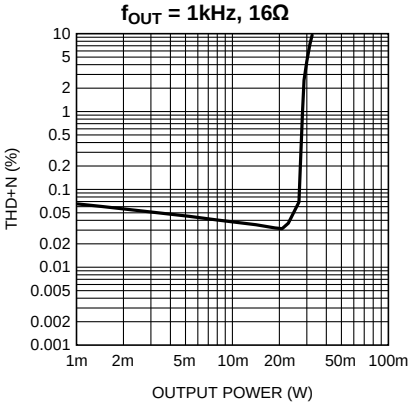


Figure 5-152.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 12dB AUX f_{OUT} = 1kHz, 16Ω

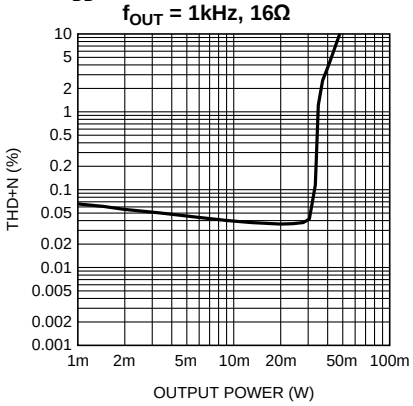


Figure 5-153.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 0dB AUX f_{OUT} = 1kHz, 32Ω

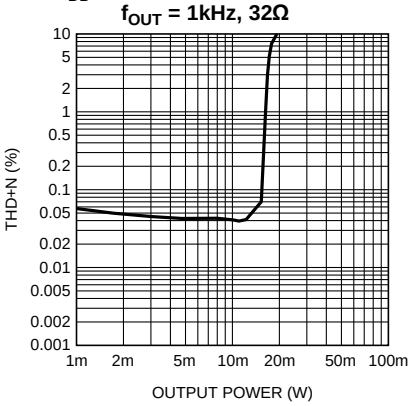


Figure 5-154.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 12dB AUX f_{OUT} = 1kHz, 32Ω

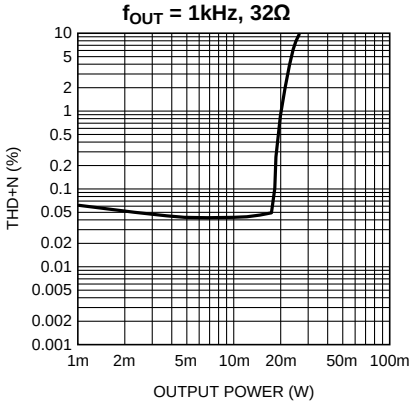


Figure 5-155.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 0dB AUX f_{OUT} = 1kHz, 32Ω

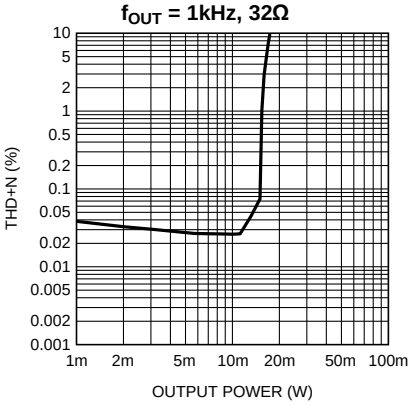


Figure 5-156.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 12dB AUX f_{OUT} = 1kHz, 32Ω

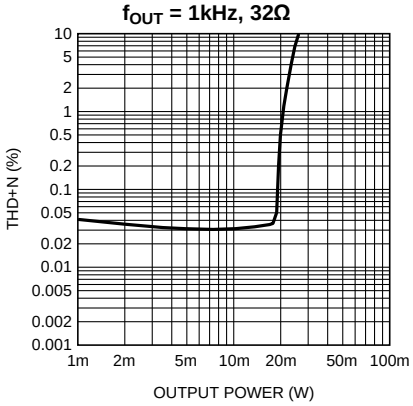


Figure 5-157.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 0dB CPI f_{OUT} = 1kHz, 16Ω

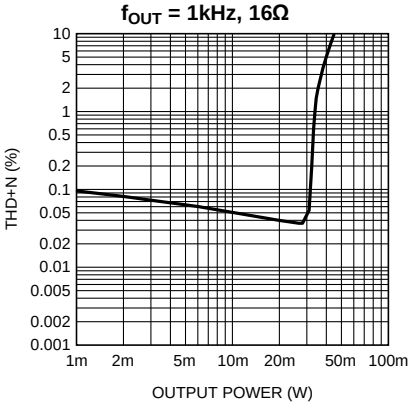


Figure 5-158.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 0dB CPI f_{OUT} = 1kHz, 16Ω

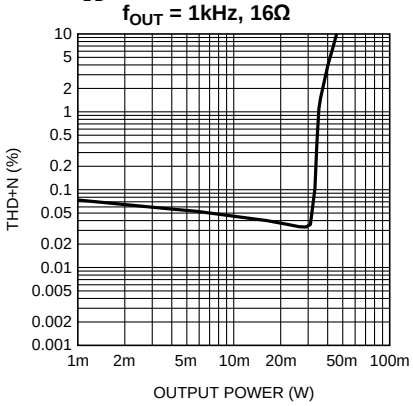


Figure 5-159.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 0dB CPI f_{OUT} = 1kHz, 32Ω

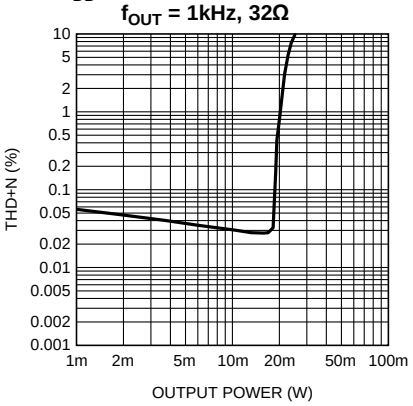


Figure 5-160.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 0dB CPI f_{OUT} = 1kHz, 32Ω

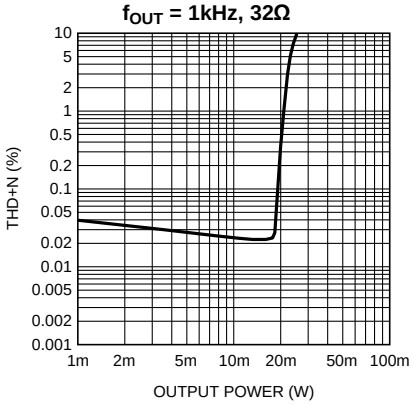


Figure 5-161.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 0dB AUX f_{OUT} = 1kHz, 16Ω

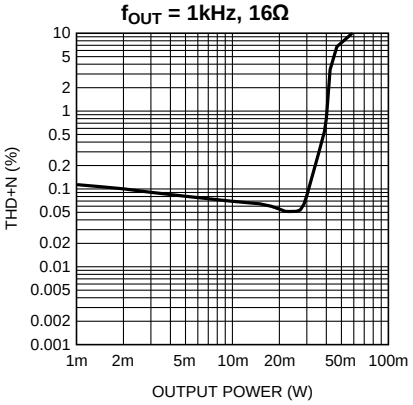


Figure 5-162.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 12dB AUX f_{OUT} = 1kHz, 16Ω

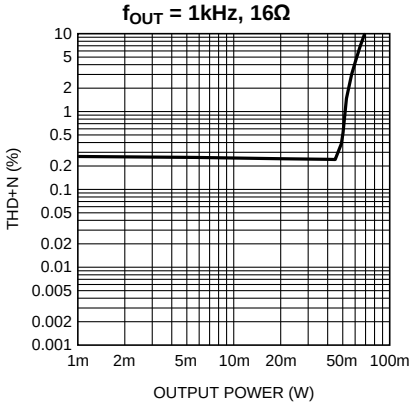


Figure 5-163.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 0dB AUX f_{OUT} = 1kHz, 16Ω

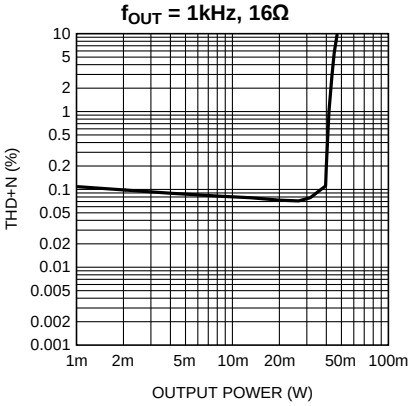


Figure 5-164.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 12dB AUX f_{OUT} = 1kHz, 16Ω

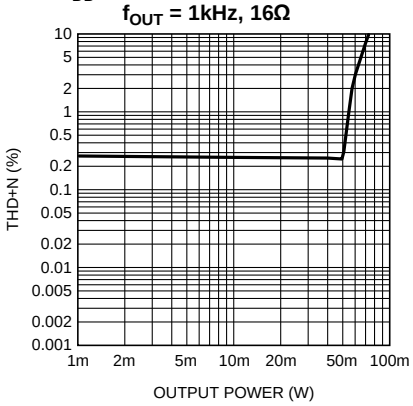


Figure 5-165.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 0dB AUX f_{OUT} = 1kHz, 32Ω

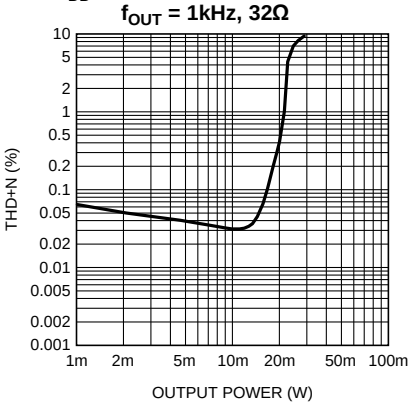


Figure 5-166.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 12dB AUX f_{OUT} = 1kHz, 32Ω

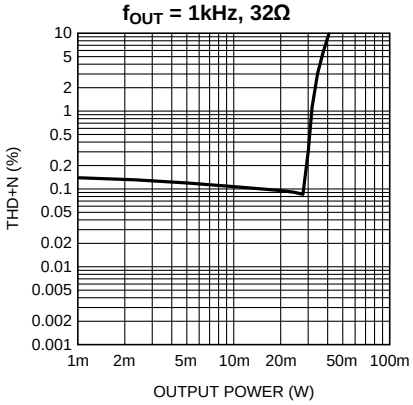


Figure 5-167.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 0dB AUX f_{OUT} = 1kHz, 32Ω

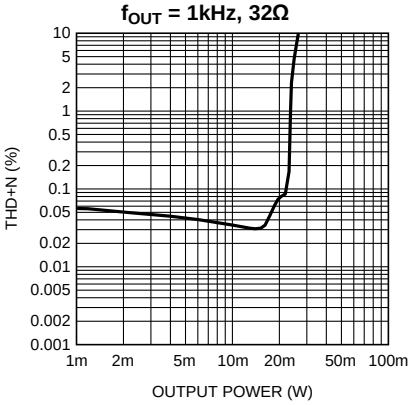


Figure 5-168.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Headphone THD+N vs Output Power
AV_{DD} = 5V, OCL 1.5V, 12dB AUX
f_{OUT} = 1kHz, 32Ω

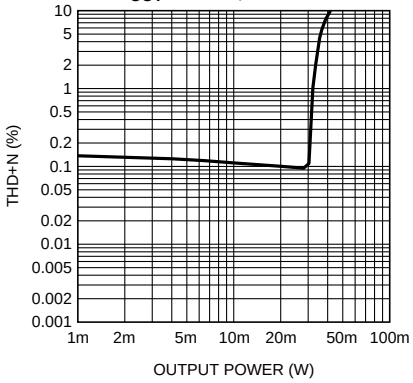


Figure 5-169.

Headphone THD+N vs Output Power
AV_{DD} = 3.3V, OCL 1.5V, 0dB CPI
f_{OUT} = 1kHz, 16Ω

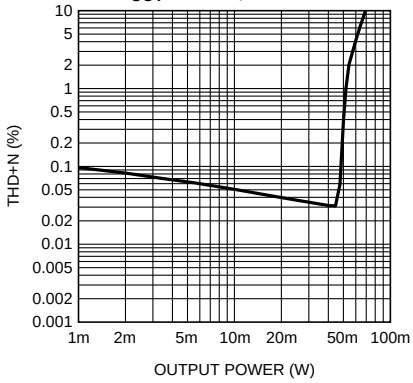


Figure 5-170.

Headphone THD+N vs Output Power
AV_{DD} = 5V, OCL 1.5V, 0dB CPI
f_{OUT} = 1kHz, 16Ω

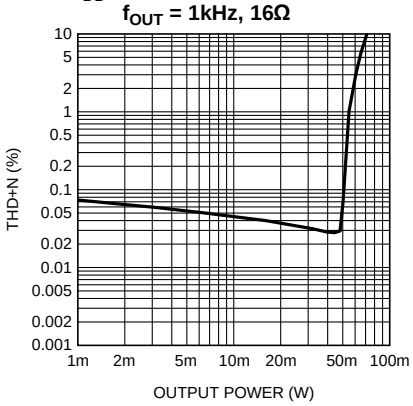


Figure 5-171.

Headphone THD+N vs Output Power
AV_{DD} = 3.3V, OCL 1.5V, 0dB CPI
f_{OUT} = 1kHz, 32Ω

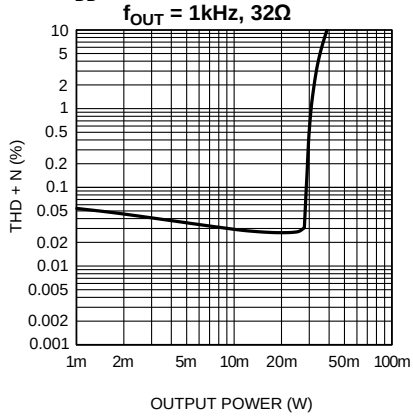


Figure 5-172.

Headphone THD+N vs Output Power
AV_{DD} = 5V, OCL 1.5V, 0dB CPI
f_{OUT} = 1kHz, 32Ω

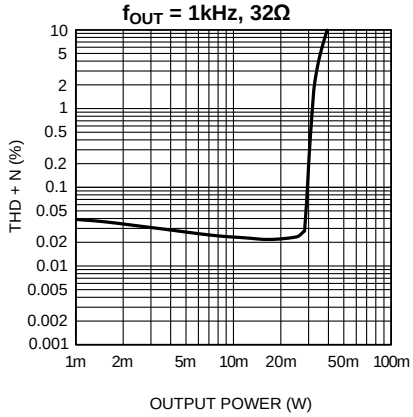


Figure 5-173.

Headphone THD+N vs Output Power
AV_{DD} = 3.3V, SE, 0dB AUX
f_{OUT} = 1kHz, 16Ω

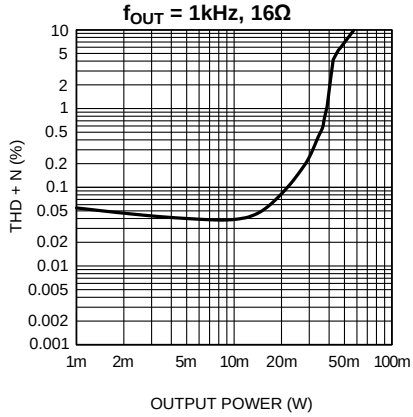


Figure 5-174.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 0dB AUX f_{OUT} = 1kHz, 16Ω

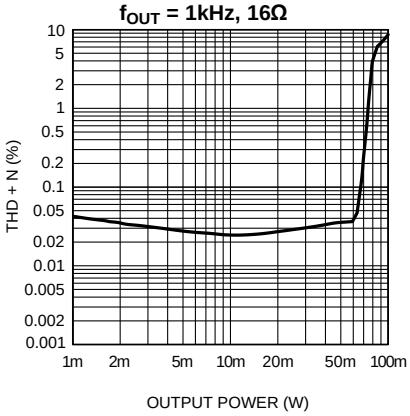


Figure 5-175.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 0dB AUX f_{OUT} = 1kHz, 32Ω

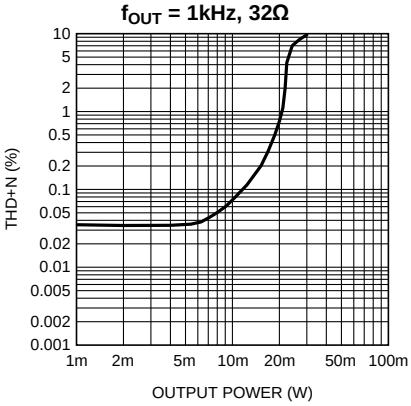


Figure 5-176.

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 0dB AUX f_{OUT} = 1kHz, 32Ω

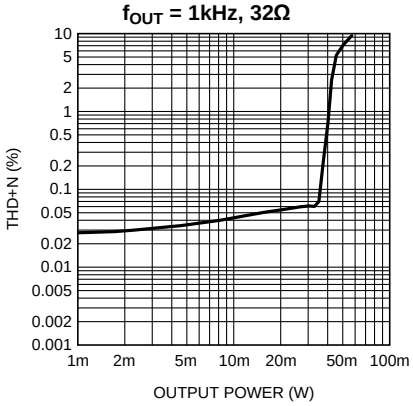


Figure 5-177.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 0dB CPI f_{OUT} = 1kHz, 16Ω

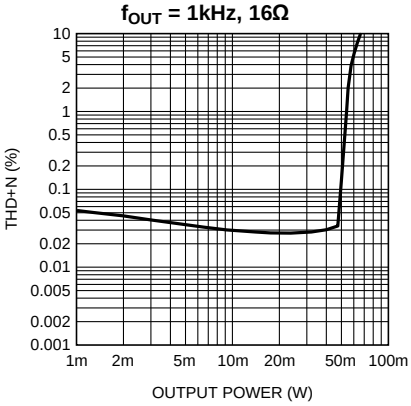


Figure 5-178.

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 0dB CPI f_{OUT} = 1kHz, 16Ω

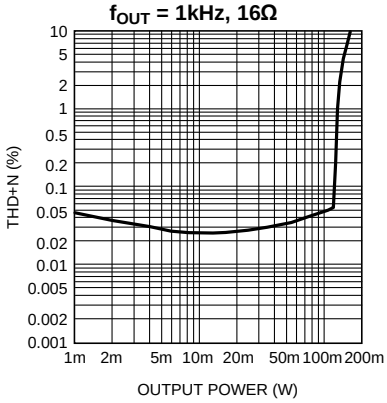


Figure 5-179.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 0dB CPI f_{OUT} = 1kHz, 32Ω

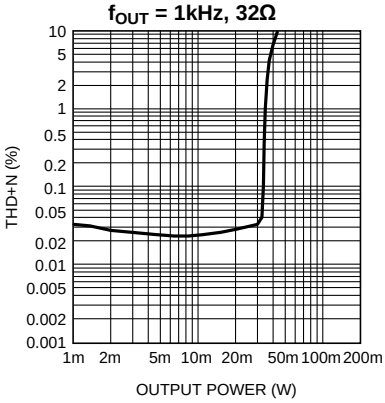


Figure 5-180.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 0dB CPI f_{OUT} = 1kHz, 32Ω

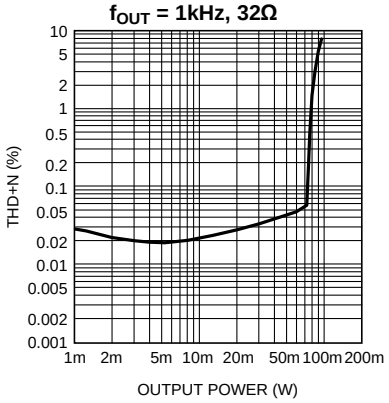


Figure 5-181.

Loudspeaker THD+N vs Output Power AV_{DD} = 3.3V, 0dB AUX f_{OUT} = 1kHz, 15µH+8Ω+15µH

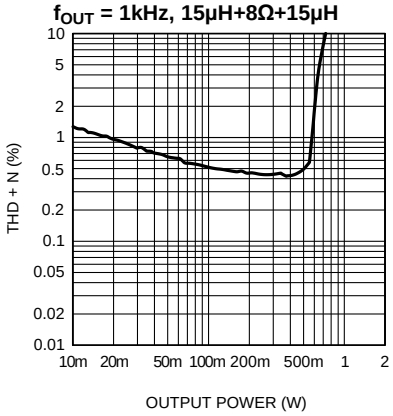


Figure 5-182.

Loudspeaker THD+N vs Output Power AV_{DD} = 4.2V, 0dB AUX f_{OUT} = 1kHz, 15µH+8Ω+15µH

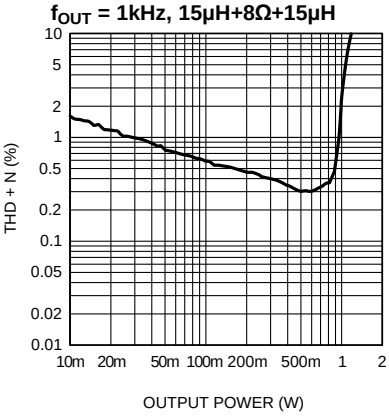


Figure 5-183.

Loudspeaker THD+N vs Output Power AV_{DD} = 5V, 0dB AUX f_{OUT} = 1kHz, 15µH+8Ω+15µH

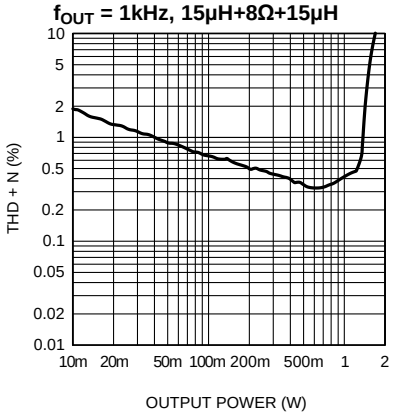


Figure 5-184.

Loudspeaker THD+N vs Output Power AV_{DD} = 3.3V, 0dB CPI f_{OUT} = 1kHz, 15µH+8Ω+15µH

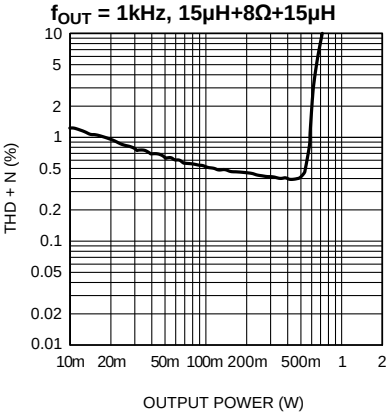


Figure 5-185.

Loudspeaker THD+N vs Output Power AV_{DD} = 4.2V, 0dB CPI f_{OUT} = 1kHz, 15µH+8Ω+15µH

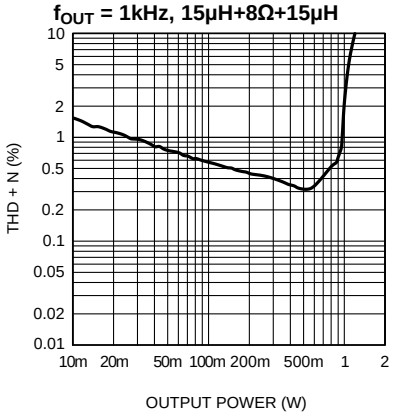


Figure 5-186.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

Loudspeaker THD+N vs Output Power
AV_{DD} = 5V, 0dB CPI
f_{OUT} = 1kHz, 15µH+8Ω+15µH

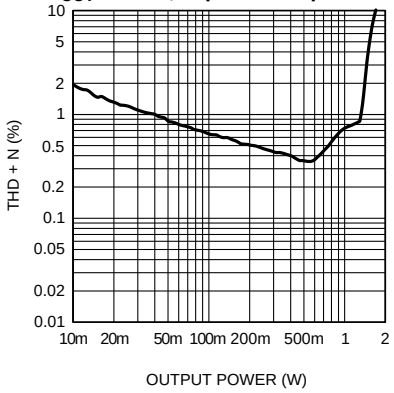


Figure 5-187.

Loudspeaker THD+N vs Output Power
AV_{DD} = 3.3V, 0dB DAC
f_{OUT} = 1kHz, 15µH+8Ω+15µH

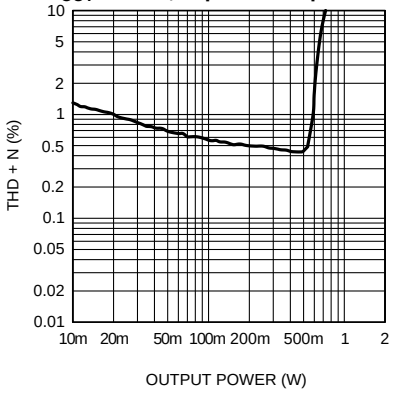


Figure 5-188.

Loudspeaker THD+N vs Output Power
AV_{DD} = 4.2V, 0dB DAC
f_{OUT} = 1kHz, 15µH+8Ω+15µH

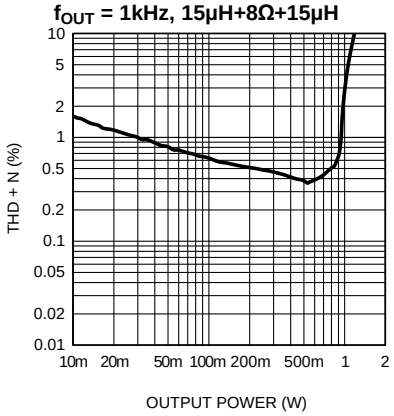


Figure 5-189.

Loudspeaker THD+N vs Output Power
AV_{DD} = 5V, 0dB DAC
f_{OUT} = 1kHz, 15µH+8Ω+15µH

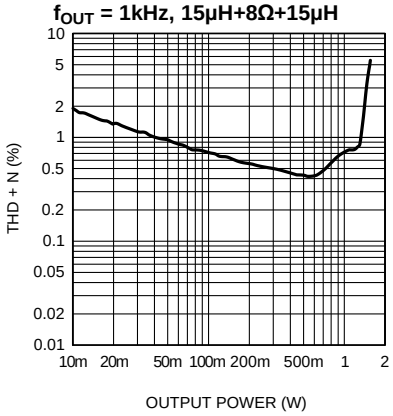


Figure 5-190.

AUXOUT THD+N vs Output Voltage
AV_{DD} = 3.3V, 0dB AUX
f_{OUT} = 1kHz, 5kΩ

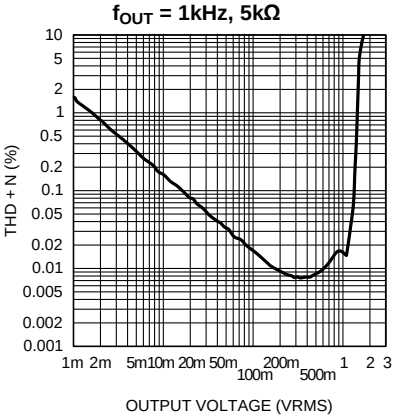


Figure 5-191.

AUXOUT THD+N vs Output Voltage
AV_{DD} = 5V, 0dB AUX
f_{OUT} = 1kHz, 5kΩ

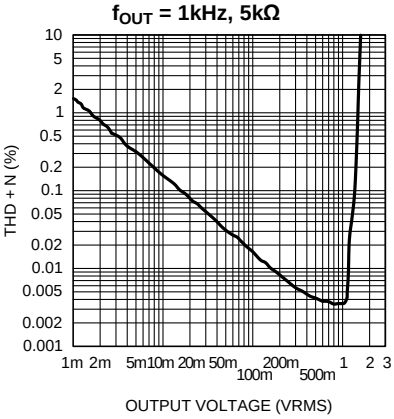


Figure 5-192.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

AUXOUT THD+N vs Output Voltage
AV_{DD} = 3.3V, 0dB CPI
f_{OUT} = 1kHz, 5kΩ

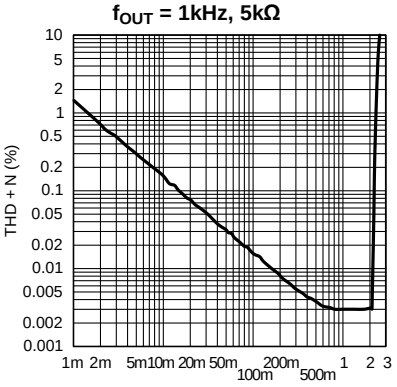


Figure 5-193.

AUXOUT THD+N vs Output Voltage
AV_{DD} = 5V, 0dB CPI
f_{OUT} = 1kHz, 5kΩ

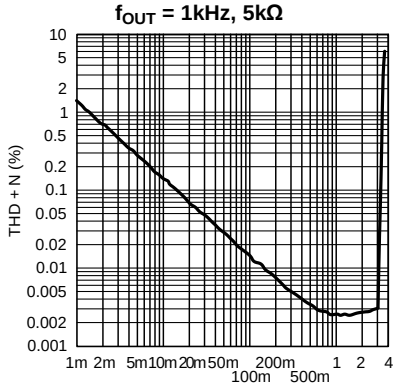


Figure 5-194.

AUXOUT THD+N vs Output Voltage
AV_{DD} = 3.3V, 0dB DAC
f_{OUT} = 1kHz, 5kΩ

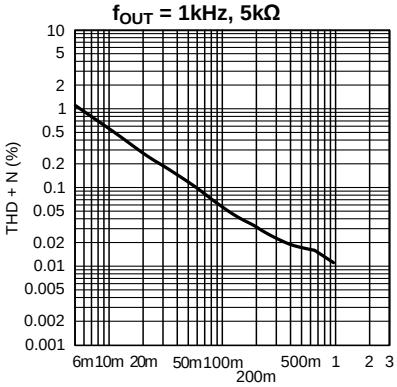


Figure 5-195.

AUXOUT THD+N vs Output Voltage
AV_{DD} = 5V, 0dB DAC
f_{OUT} = 1kHz, 5kΩ

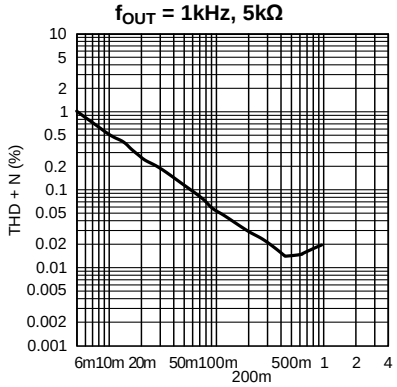


Figure 5-196.

AUXOUT THD+N vs Output Voltage
AV_{DD} = 3.3V, 12dB DAC
f_{OUT} = 1kHz, 5kΩ

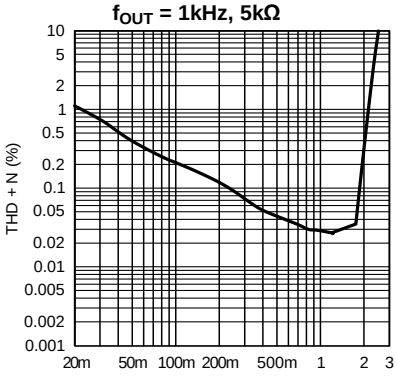


Figure 5-197.

AUXOUT THD+N vs Output Voltage
AV_{DD} = 5V, 12dB DAC
f_{OUT} = 1kHz, 5kΩ

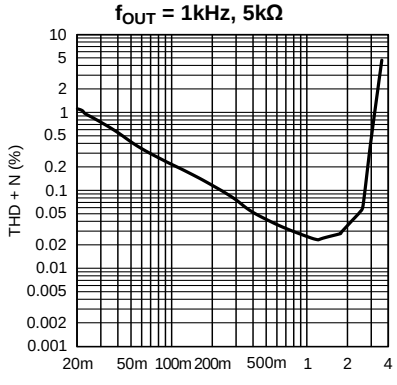


Figure 5-198.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

CPOUT THD+N vs Output Voltage
AV_{DD} = 3.3V, 0dB AUX
f_{OUT} = 1kHz, 5kΩ

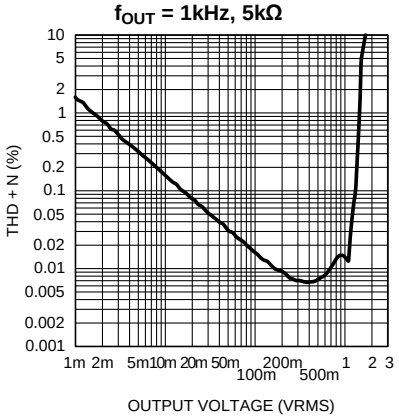


Figure 5-199.

CPOUT THD+N vs Output Voltage
AV_{DD} = 5V, 0dB AUX
f_{OUT} = 1kHz, 5kΩ

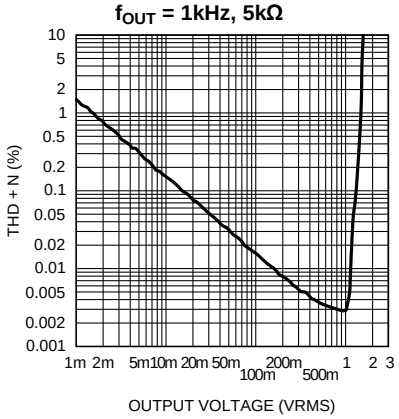


Figure 5-200.

CPOUT THD+N vs Output Voltage
AV_{DD} = 3.3V, 0dB DAC
f_{OUT} = 1kHz, 5kΩ

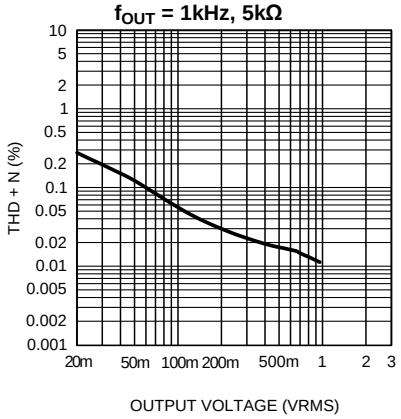


Figure 5-201.

CPOUT THD+N vs Output Voltage
AV_{DD} = 5V, 0dB DAC
f_{OUT} = 1kHz, 5kΩ

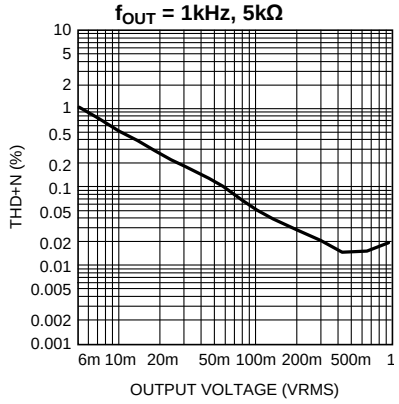


Figure 5-202.

CPOUT THD+N vs Output Voltage
AV_{DD} = 3.3V, 6dB MIC
f_{OUT} = 1kHz, 5kΩ

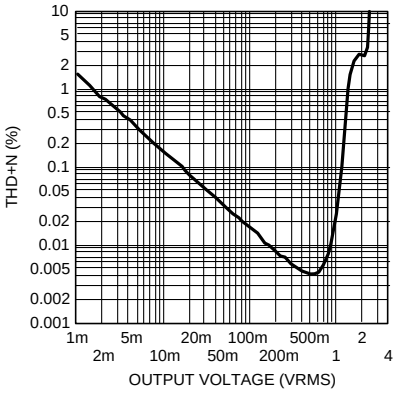


Figure 5-203.

CPOUT THD+N vs Output Voltage
AV_{DD} = 5V, 6dB MIC
f_{OUT} = 1kHz, 5kΩ

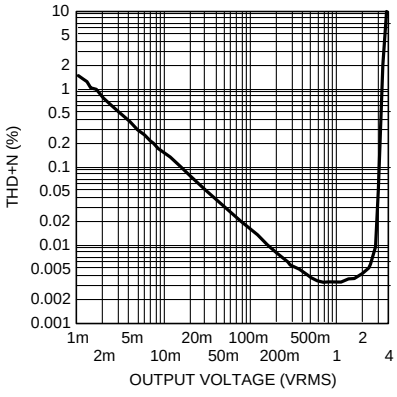


Figure 5-204.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

CPOUT THD+N vs Output Voltage AV_{DD} = 3.3V, 12dB DAC f_{OUT} = 1kHz, 5kΩ

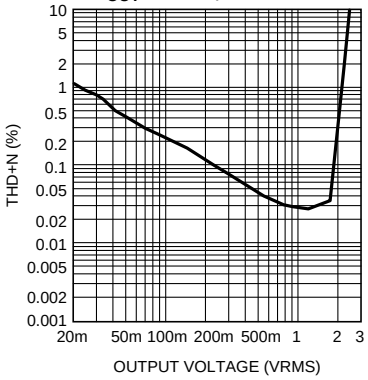


Figure 5-205.

CPOUT THD+N vs Output Voltage AV_{DD} = 5V, 12dB DAC f_{OUT} = 1kHz, 5kΩ

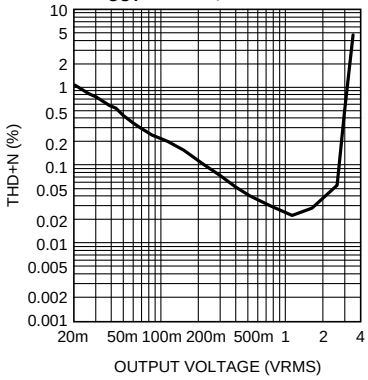


Figure 5-206.

CPOUT THD+N vs Output Voltage AV_{DD} = 3.3V, 36dB MIC f_{OUT} = 1kHz, 5kΩ

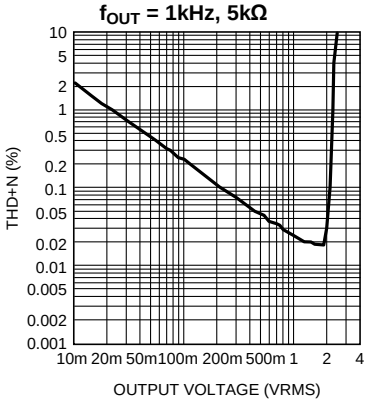


Figure 5-207.

CPOUT THD+N vs Output Voltage AV_{DD} = 5V, 36dB MIC f_{OUT} = 1kHz, 5kΩ

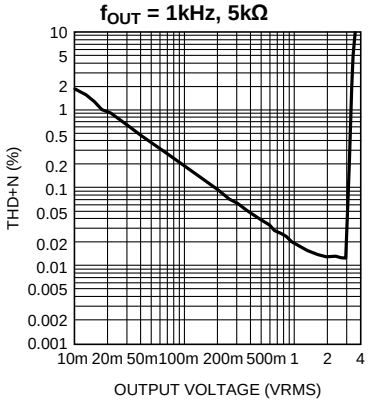


Figure 5-208.

Headphone Crosstalk vs Frequency OCL 1.2V, 0dB AUX, 32Ω

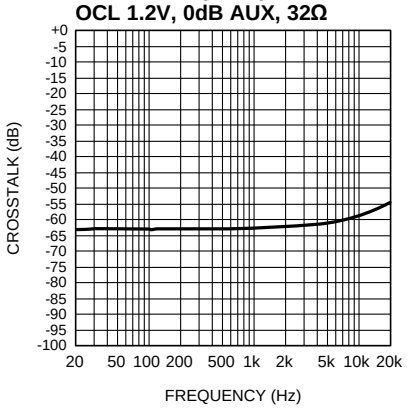


Figure 5-209.

Headphone Crosstalk vs Frequency OCL 1.5V, 0dB AUX, 32Ω

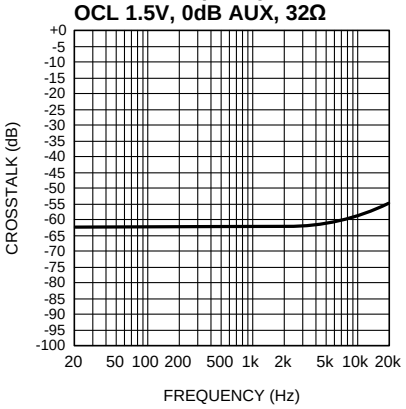


Figure 5-210.

Copyright © 2005–2013, Texas Instruments Incorporated

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified. (continued)

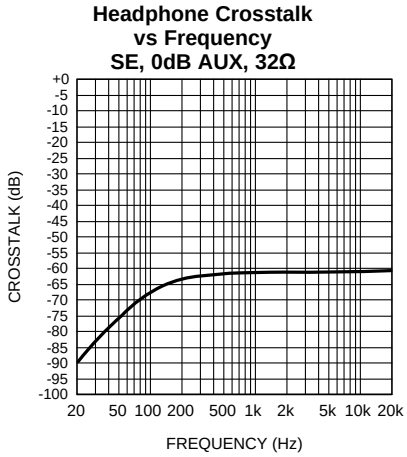
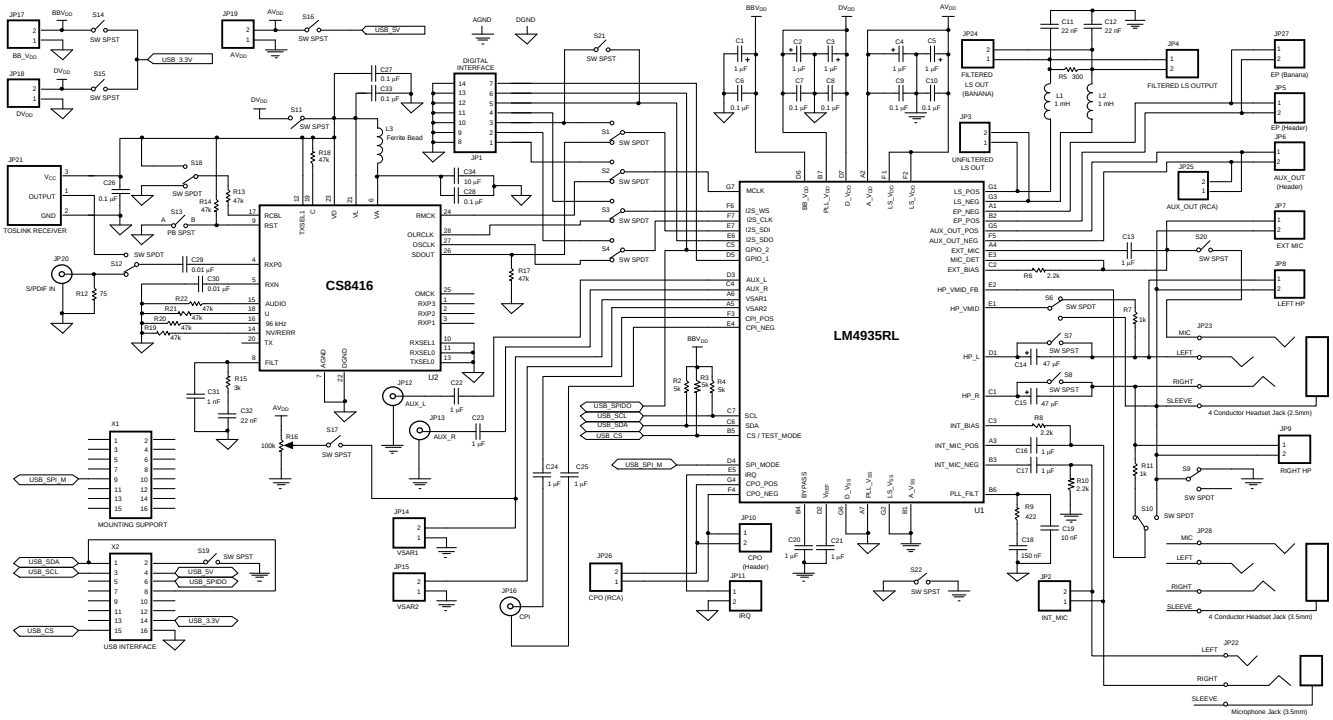


Figure 5-211.

6 Board Schematic Diagrams

6.1 LM4935 Demonstration Board Schematic Diagram



6.2 Demoboard PCB Layout

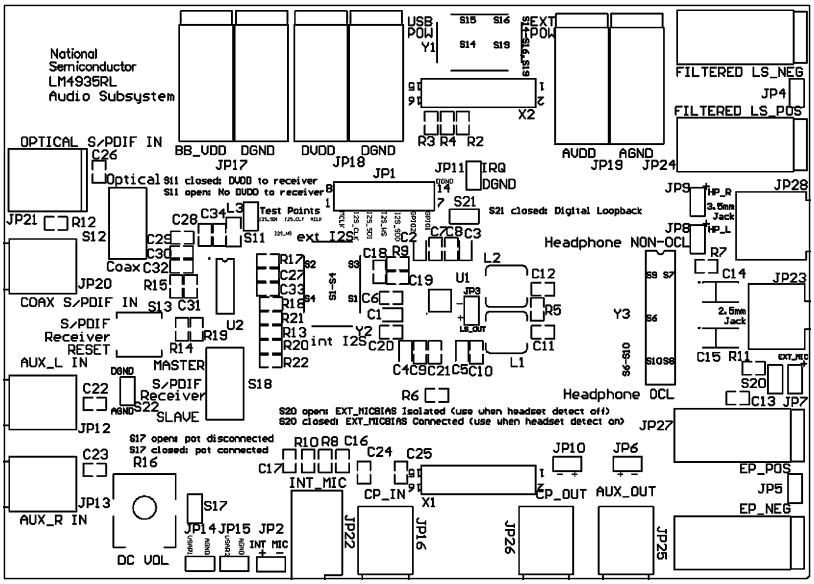


Figure 6-1. Top Silkscreen

Copyright © 2005–2013, Texas Instruments Incorporated

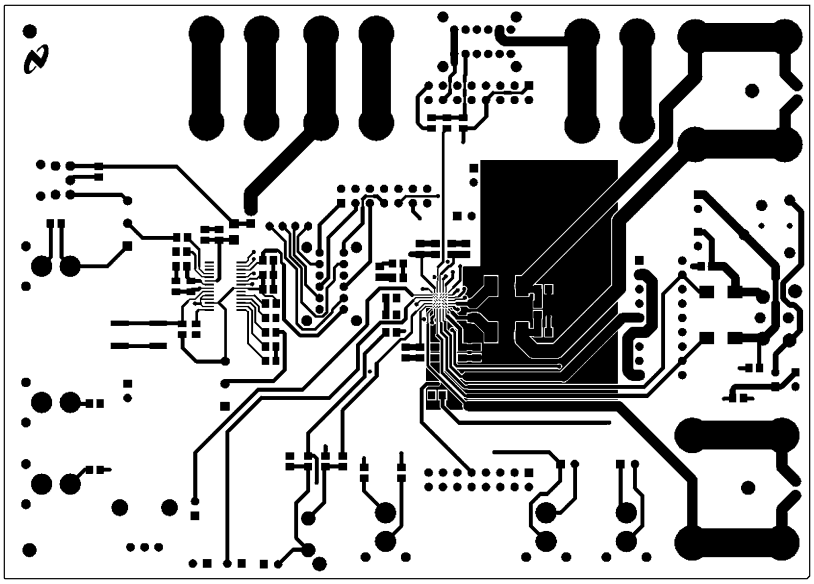


Figure 6-2. Top Layer

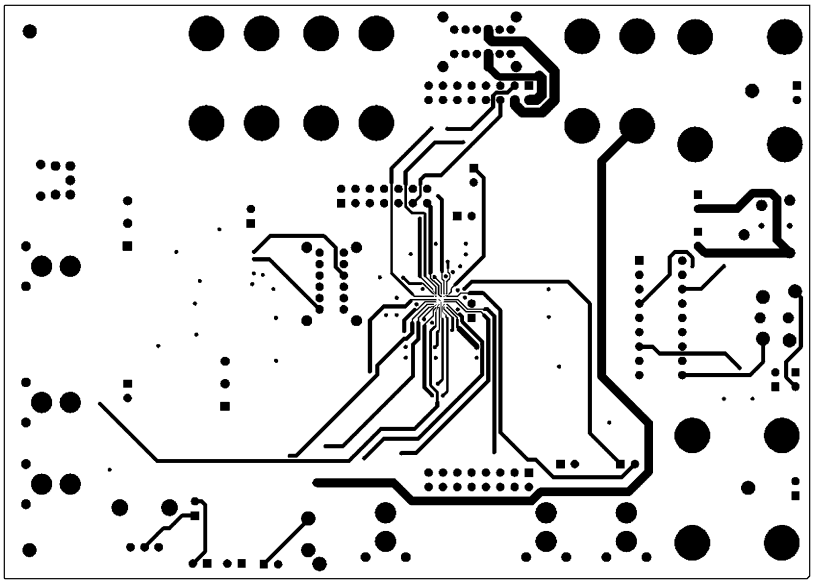


Figure 6-3. Mid Layer 1

Copyright © 2005–2013, Texas Instruments Incorporated

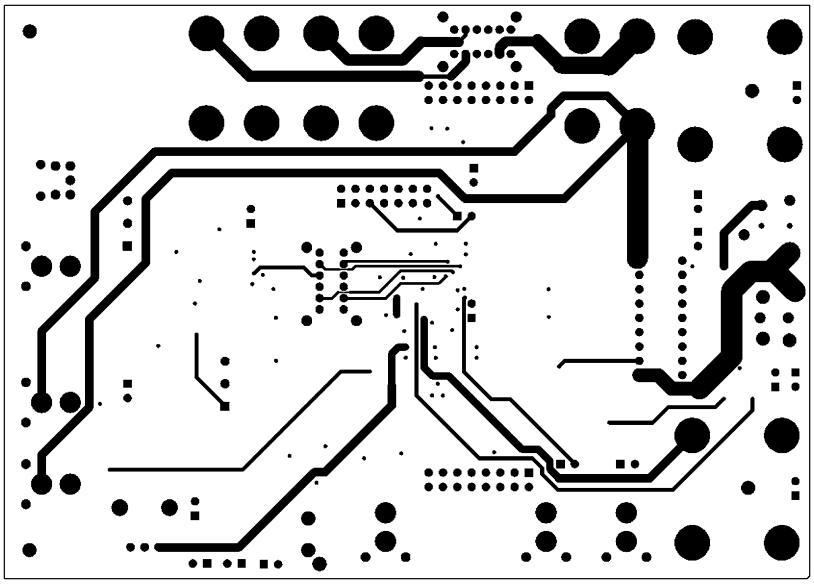


Figure 6-4. Mid Layer 2

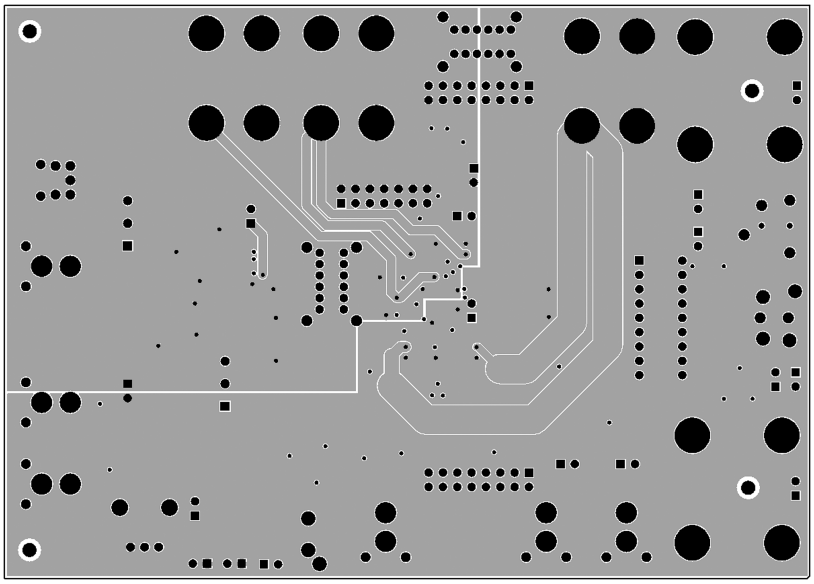


Figure 6-5. Bottom Layer

6.3 Product Status Definitions

Datasheet Status	Product Status	Definition
Advance Information	Formative or in Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data. Supplementary data will be published at a later date.
No Identification Noted	Full Production	This data sheet contains final specifications.
Obsolete	Not in Production	This data sheet contains specifications on a product that has been discontinued. The datasheet is printed for reference information only.

Copyright © 2005–2013, Texas Instruments Incorporated

6.4 Revision History

Rev	Date	Description
1.0	5/11/05	Filled in the actual limits (for TBDs) under Limit and edited few Typical values, all under the EC table. Edits from Alvin F.
1.1	7/29/05	Input more edits. Replaced the correct boards. Replaced the Schematic Diagram (pg 60).
1.2	9/8/05	Added the 1st set of Typ Perf curves.
1.3	9/21/05	Added a couple of tables.
1.4	9/30/05	Input text edits.
1.5	10/5/05	Input more edits.
1.6	10/11/05	More edits.
1.7	10/12/05	First D/S WEB release.
1.8	10/14/5	Input more text edits after the 1st released.
1.9	10/17/05	Input some text edits, then re-released D/S to the WEB.
2.0	10/18/05	More text edits. Also used graphic 20134107 back.
2.1	12/19/05	Added the RL package
2.2	12/20/05	Deleted the WL pkg and replaced with the RL pkg.
2.3	1/19/06	Fixed 20134132(top silkscreen) and 35 (schem layout) plus few text edits.
2.4	1/25/06	Fixed the value on X3 (mktg outline). Re-released D/S to the WEB.
E	5/03/13	Changed layout of National Data Sheet to TI format.

Copyright © 2005–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4935RL/NOPB	ACTIVE	DSBGA	YPG	49	250	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	-40 to 85	GG7	Samples
LM4935RLX/NOPB	ACTIVE	DSBGA	YPG	49	1000	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	-40 to 85	GG7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

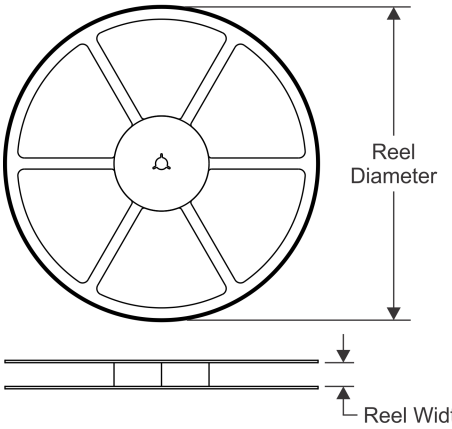
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

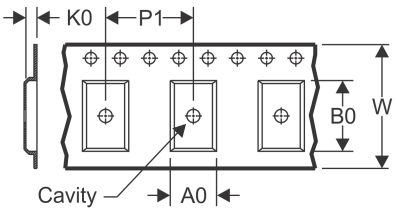
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

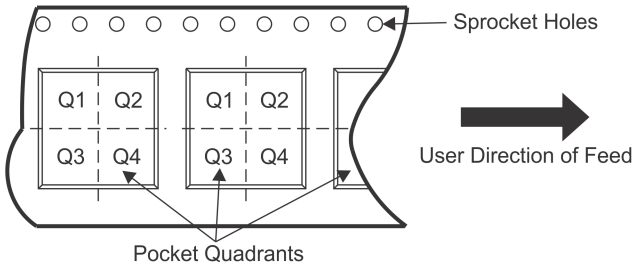


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

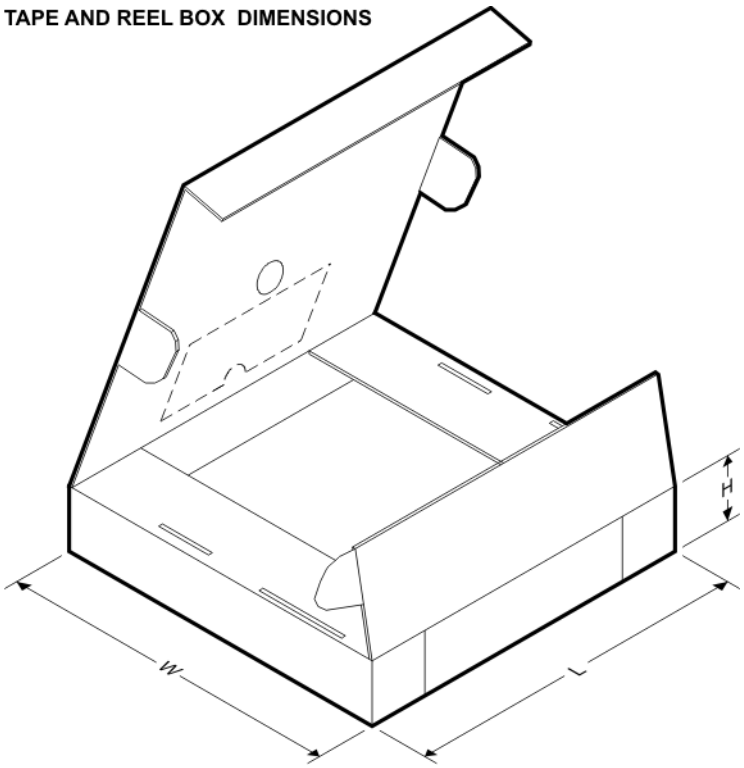
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4935RL/NOPB	DSBGA	YPG	49	250	178.0	12.4	4.19	4.19	0.76	8.0	12.0	Q1
LM4935RLX/NOPB	DSBGA	YPG	49	1000	178.0	12.4	4.19	4.19	0.76	8.0	12.0	Q1

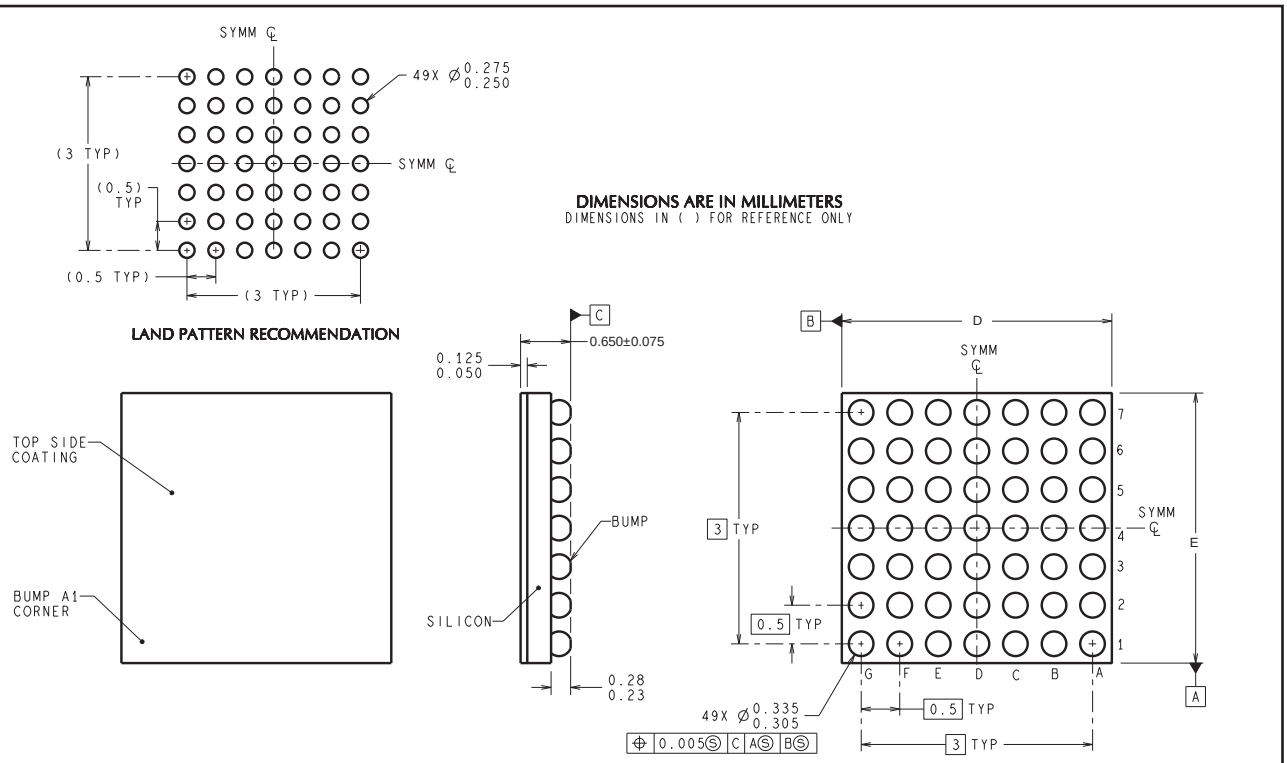
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4935RL/NOPB	DSBGA	YPG	49	250	210.0	185.0	35.0
LM4935RLX/NOPB	DSBGA	YPG	49	1000	210.0	185.0	35.0

YPG0049



D: Max = 3.94 mm, Min = 3.88 mm

E: Max = 3.94 mm, Min = 3.88 mm

4214898/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View LM4935RLX on WIN SOURCE
- Texas Instruments Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management