THE DATASHEET OF

LM4832M/NOPB

www.win-source.net 0086-755-83957316

LM4832 Boomer® Audio Power Amplifier Series Digitally Controlled Tone and Volume Circuit with Stereo Audio Power Amplifier, Microphone Preamp Stage and Texas Instruments 3D Sound

Check for Samples: LM4832

FEATURES

- **Independent Left and Right Output Volume Controls**
- **Treble and Bass Control**
- **Texas Instruments 3D Sound**
- **I²C Compatible Interface**
- **Two Microphone Inputs with Selector**
- **Software Controlled Shutdown Function**

APPLICATIONS

- **Multimedia Monitors**
- **Portable and Desktop Computers**

KEY SPECIFICATIONS

- **Output Power at 10% into 8Ω, 350mW (Typ)**
- **Output Power at 10% into 32Ω, 100mW (Typ)**
- **THD+N at 75mW into 32Ω at 1kHz, 0.5% (Max)**
- **Microphone Input Referred Noise, 7μV (Typ)**
- **Supply Current, 13mA (Typ)**
- **Shutdown Current, 4μA (Typ)**

DESCRIPTION

The LM4832 is a monolithic integrated circuit that provides volume and tone (bass and treble) controls as well as a stereo audio power amplifier capable of producing 250 mW (typ) into 8Ω or 90 mW (typ) into 32Ω with less than 1.0% THD. In addition, a two input microphone preamp stage, with volume control, capable of driving a 1 kΩ load is implemented on chip.

The LM4832 also features Texas Instruments' 3D Sound circuitry which can be externally adjusted via a simple RC network. For maximum system flexibility, the LM4832 has an externally controlled, low-power consumption shutdown mode, and an independent mute for power and microphone amplifiers .

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring few external components. Since the LM4832 incorporates tone and volume controls, a stereo audio power amplifier and a microphone preamp stage, it is optimally suited to multimedia monitors and desktop computer applications.

Block Diagram

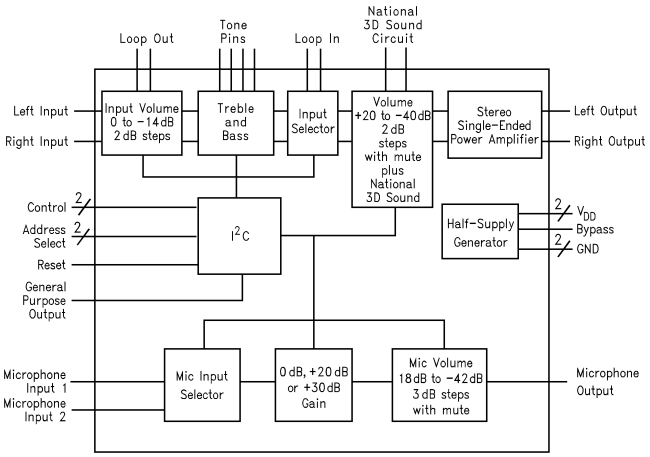

Figure 1. LM4832 Block Diagram

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation(3)		Internally limited
ESD Susceptibility(4)		2000V
ESD Susceptibility(5)		250V
Junction Temperature		150°C
Soldering Information	Small Outline Package Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
θ_{JC} (typ)—N28B		21°C/W
θ_{JA} (typ)—N28B		62°C/W
θ_{JC} (typ)—M28B		15°C/W
θ_{JA} (typ)—M28B		69°C/W
θ_{JC} (typ)—PW		20°C/W
θ_{JA} (typ)—PW		80°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$.For the LM4832, T_{JMAX} = 150°C, and the typical junction-to-ambient thermal resistance, when board mounted, is 69°C/W assuming the M28B package.

(4) Human body model, 100pF discharged through a 1.5kΩ resistor.

(5) Machine Model, 220pF–240pF discharged through all pins.

Operating Ratings

Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage	$4.5 \le V_{DD} \le 5.5V$

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Electrical Characteristics for Entire IC[1]

The following specifications apply for V_{DD} = 5V unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4832		Units (Limits)
			Typical[2]	Limit[3][4]	
V_{DD}	Supply Voltage	V_{IN} = 0V, I_O = 0A		4.5	V (min)
				5.5	V (max)
I_{DD}	Quiescent Power Supply Current		13	21	mA (max)
I_{SD}	Shutdown Current		2.5	9	µA (max)
INPUT ATTENUATORS					
A_R	Attenuator Range	Attenuation at 0 dB Setting Attenuation at −14 dB Setting		1 −15	dB (max) dB (min)
A_S	Step Size	0 dB to −14 dB	2		dB
	Gain Step Size Error		0.1		dB (max)
E_T	Channel to Channel Tracking Error		0.15		dB (max)
BASS CONTROL					
A_R	Bass Control Range	f = 100 Hz, V_{IN} = 0.25V	±12	−14	dB (min)
				14	dB (max)
A_S	Bass Step Size		2		dB
E_{SE}	Bass Step Size Error		0.5		dB (max)
E_T	Bass Tracking Error		0.15		dB (max)
TREBLE CONTROL					
A_R	Treble Control Range	f_{IN} = 10 kHz, V_{IN} = 0.25V	±12	−13	dB (min)
				13	dB (max)
A_S	Treble Step Size		2		dB
E_{SE}	Treble Step Size Error		0.1		dB (max)
E_T	Treble Tracking Error		0.15		dB (max)
OUTPUT ATTENUATORS					
A_R	Attenuator Range	Gain at +20 dB Setting Attenuation at −40 dB Setting +20 dB to −40 dB		21	dB (max)
				−42	dB (min)
A_S	Step Size		2		dB
	Step Size Error		0.1		dB (max)
E_T	Channel to Channel Tracking Error		0.1		dB (max)
AUDIO PATH					
V_{OS}	Output Offset Voltage	V_{IN} = 0V	3	50	mV (max)
P_O	Output Power	THD = 1.0% (max), f = 1 kHz, All controls at 0dB			
		R_L = 8Ω	250		mW (min)
		R_L = 32Ω	95	75	mW (min)
THD+N	Total Harmonic Distortion+Noise	All Controls at 0 dB, THD = 10%, f = 1 kHz R_L = 8Ω	350		mW
		P_O = 200 mW, R_L = 8Ω	0.15		%
		P_O = 75 mW, R_L = 32Ω	0.11		%
		V_O = 1 Vrms, R_L = 10Ω	0.08		%
PSRR	Power Supply Rejection Ratio	C_B = 1 µF, f = 100 Hz, V_{RIPPLE} = 100 mVrms, All Controls at 0 dB Setting	45		dB
A_M	Mute Attenuation	f = 1 kHz, V_{IN} = 1V	−75		dB

(1) All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical applications shown in Figure 1.
(2) Typicals are measured at 25°C and represent the parametric norm.
(3) Limits are ensured AOQL (Average Outgoing Quality Level).
(4) Data sheet min and max specification limits by design, test, or statistical analysis.

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Electrical Characteristics for Entire IC[1] (continued)

The following specifications apply for V_{DD} = 5V unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4832		Units (Limits)
			Typical[2]	Limit[3][4]	
X_{TALK}	Cross Talk	P_O = 200 mW, R_L = 8Ω, All controls at 0 dB setting, f = 1 kHz			
		Left to Right	−85		dB
		Right to Left	−72		dB
MICROPHONE PREAMP AND VOLUME CONTROL					
A_V	Preamp Gain	0 dB Gain	0	−1, 1	dB
		+20 dB Gain	20	19, 21	dB
		+30 dB Gain	30	29, 31	dB
A_R	Attenuator Range	Gain at +18 dB Setting		20	dB (max)
		Attenuation at −42 dB Setting		−43	dB (min)
A_S	Step Size	0 dB to −42 dB	3		dB
	Step Size Error		0.4		dB (max)
V_{SWING}	Output Voltage Swing	f = 1 kHz, THD < 1.0%, R_L = 1 kΩ	1.7		V_{rms}
E_{NO}	Input Referred Noise	A-Weighted, Attenuator at 0 dB	7		µV (min)
PSRR	Power Supply Rejection Ratio	f = 100 Hz, V_{RIPPLE} = 100 mVrms, C_B = 1 µF	35		dB
A_M	Mute Attenuation		−90		dB
X_{TALK}	Cross Talk	Power Amp P_O = 200 mW, f = 1 kHz	−90		dB
THD+N	Total Harmonic Distortion Plus Noise	All controls at 0 dB, f = 1 kHz, V_O = 1V			
		0 dB Setting	0.03		%
		+20 dB Gain	0.03		%
		+30 dB Gain	0.04		%
I^2C BUS TIMING					
f_{MAX}	Maximum Bus Frequency			400	kHz
$T_{START:HOLD}$	Start Signal: Hold Time before Clock/Data Transitions			0.6	µs
$T_{D;SETUP}$	Data Setup Time			0.1	µs
$T_{C;HIGH}$	Minimum High Clock Duration			0.6	µs
$T_{C;LOW}$	Minimum Low Clock Duration			1.3	µs
$T_{STOP;SETUP}$	Stop Signal: Setup Time before Clock/Data Transitions			0.6	µs
I^2C BUS INPUT AND OUTPUT					
V_{IL}	Input Low Voltage			1.5	V (max)
V_{IH}	Input High Voltage			3	V (min)
I_{IN}	Input Current		0.15		µA
V_O	Output Voltage—SDA Acknowledge			0.4	V (max)
V_{OL}	External Power Amp Disable Low			0.4	V (max)
V_{OH}	External Power Amp Disable High			4	V (min)

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Typical Application Circuit

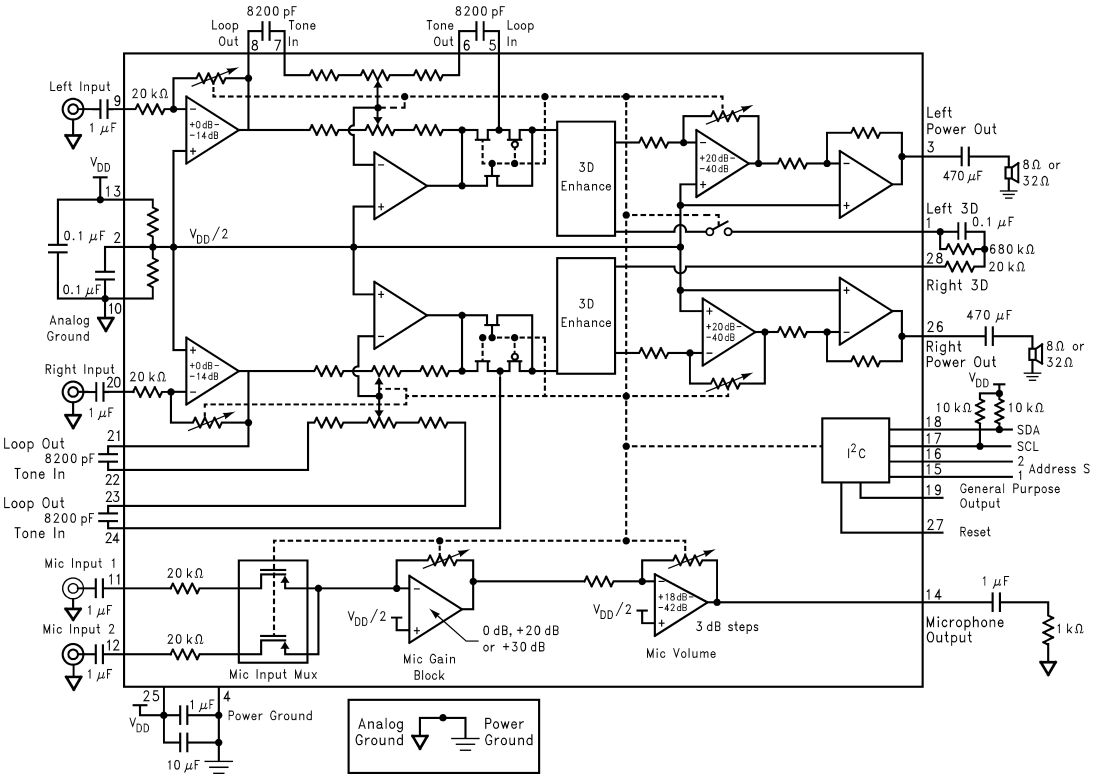
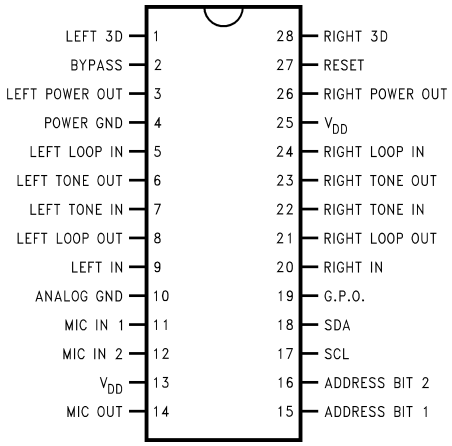


Figure 2. Typical Application Circuit

Connection Diagram
Top View



PIN FUNCTIONS

Pin Name	Description
LEFT 3D (1) RIGHT 3D (28)	An external RC network is connected across these pins. This function provides left-right channel cross coupling and cancellation to create an enhanced stereo channel separation effect.
BYPASS (2)	A 0.1 µF capacitor is placed between this pin and ground to provide an AC ground for the internal half-supply voltage reference. The capacitor at this pin affects “click-pop” and THD performance. Turn-on and turn-off times are also determined by this capacitor. Refer to the Application Information section for more information.
POWER AMP OUT LEFT (3) RIGHT (26)	These outputs are intended to drive 8Ω speakers or 32Ω headphones. These outputs should be AC-coupled to the loads. Refer to the Application Information section for more information.
POWER GND (4)	This pin provides the high current return for the power output stage MOSFETs and digital circuitry.
LOOP OUT (8, 21) LOOP IN (5, 24)	These pins allow an external signal processor access to the stereo signal. Please see the Application Information section for more information.
TONE OUT (6, 23)	These pins are connected to the tone control op amp outputs and drive the power amplifier inputs. Refer to the Application Information section for more information.
TONE IN (7, 22)	These pins are connected to the inputs of the tone control op amps. A capacitor between the Tone In and Tone Out pins sets the frequency response of the tone functions. Please refer to the Application Information section for more information.
INPUTS (9, 20)	These pins are the stereo inputs for the LM4832. These pins should be AC-coupled to the input signals.
ANALOG GND (10)	This pin is the AC analog ground for the line level AC signal inputs.
MIC INPUTS (11, 12)	These pins are the two independent selectable microphone inputs. These pins should be AC-coupled.
MIC OUT (14)	This pin is the output for the microphone amplifier and should be AC-coupled to the load.
V_{DD} (13, 25)	These pins are for the 5V supply. These pins should be separately bypassed by 0.1 µF, or higher, film capacitors. The 5V supply should be bypassed by a 10 µF, or higher, tantalum or aluminum electrolytic capacitor.
ADDRESS BITS (15, 16)	These pins are used to determine the I^2C address for the LM4832.
CLOCK (17)	This pin is the input for the I^2C clock signal.
DATA (18)	This pin is the input for the I^2C data signal.
GENERAL PURPOSE OUTPUT (19)	This pin provides a general purpose TTL/CMOS output. Please refer to the Application Information section for more information.
RESET (27)	This pin is a TTL/CMOS input which is used to reset the chip logic and states.

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Typical Performance Characteristics

THD+N vs Frequency, 8Ω

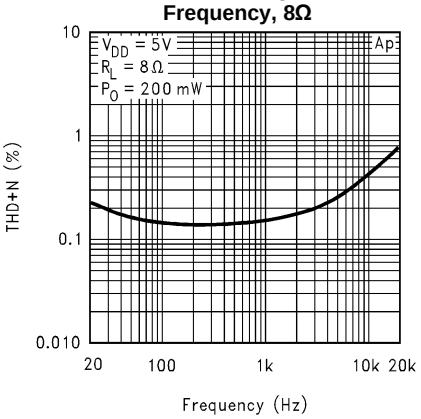

Figure 3.

THD+N vs Frequency, 32Ω

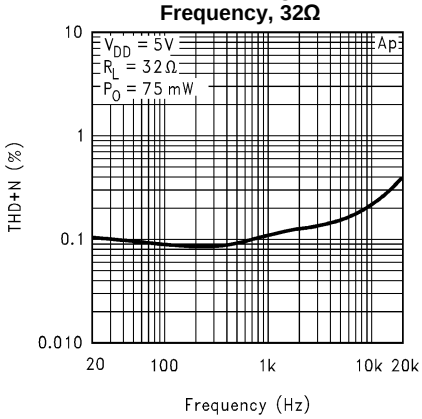

Figure 4.

THD+N vs Frequency, 1 kΩ

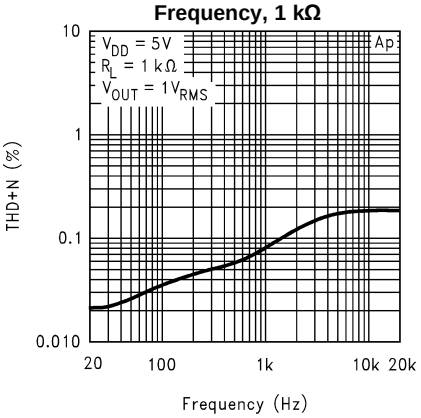

Figure 5.

THD+N vs Output Power

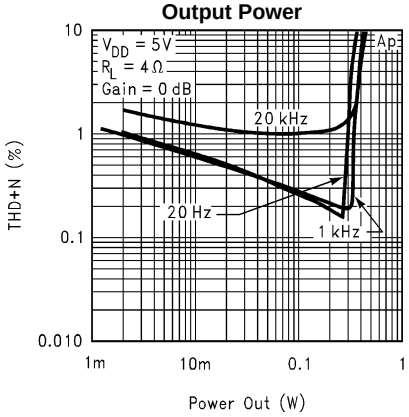

Figure 6.

THD+N vs Output Power

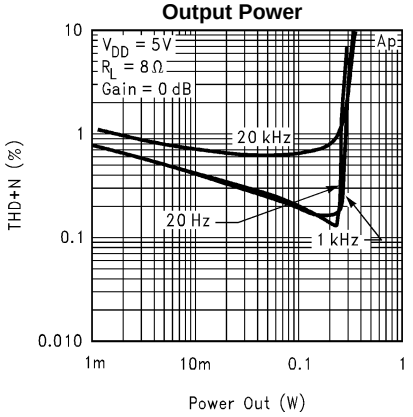

Figure 7.

THD+N vs Output Power

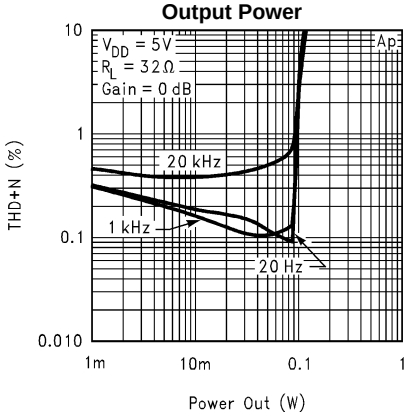

Figure 8.

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Typical Performance Characteristics (continued)

Power Amplifier Crosstalk

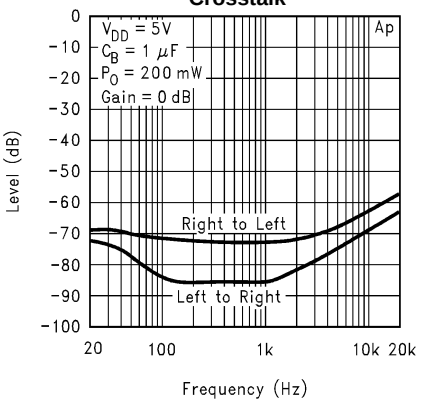

Figure 9.

Power Amplifier Noise Floor

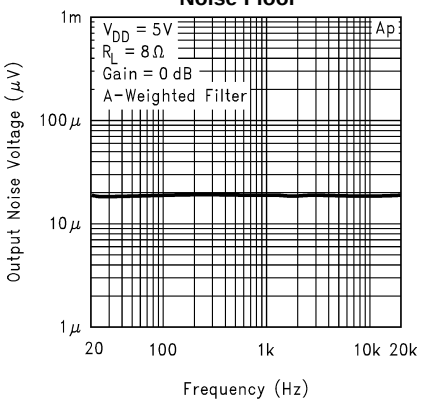

Figure 10.

Power Amplifier Attenuation vs Frequency

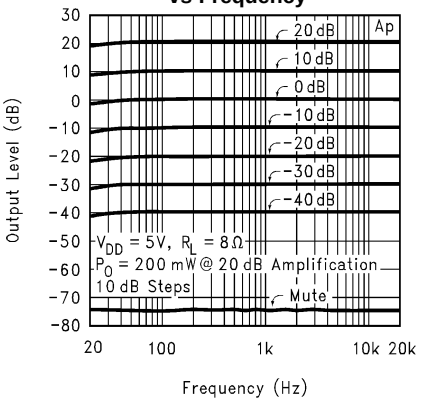

Figure 11.

Power Supply Rejection Ratio

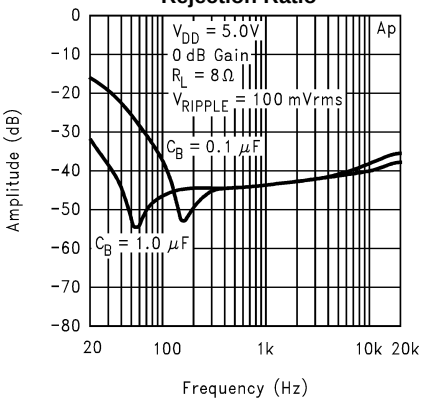

Figure 12.

Power Dissipation vs Output Power

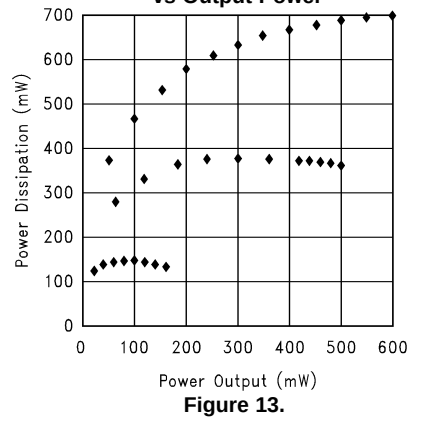

Figure 13.

Power Derating Curve

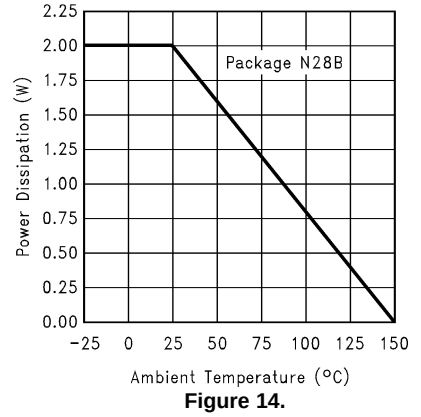

Figure 14.

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Typical Performance Characteristics (continued)

Mic Amplifer Crosstalk from Power Amplifier

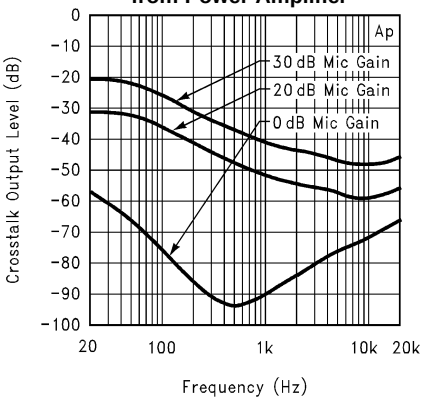

Figure 15.

Mic Amplifier Noise Floor

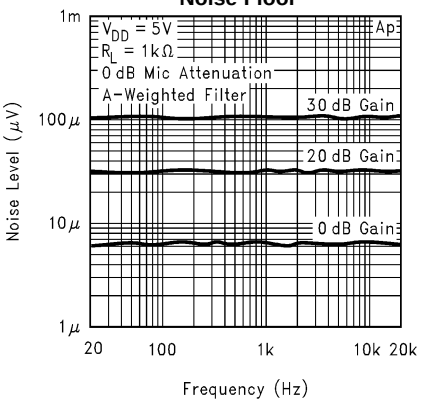

Figure 16.

Mic Amplifier Attenuation vs Frequency

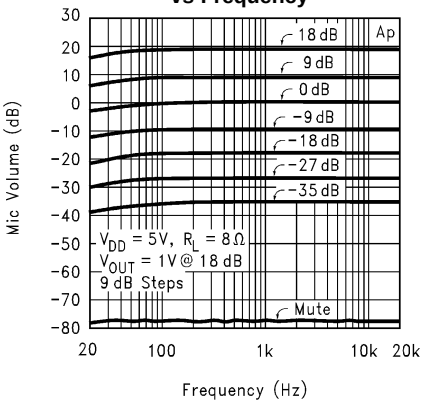

Figure 17.

Mic Amplifier Gain vs Frequency

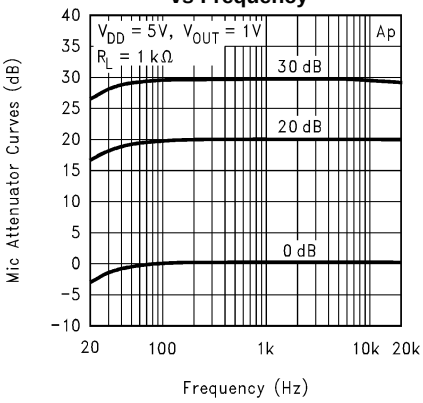

Figure 18.

Mic Amplifier THD+N vs Frequency

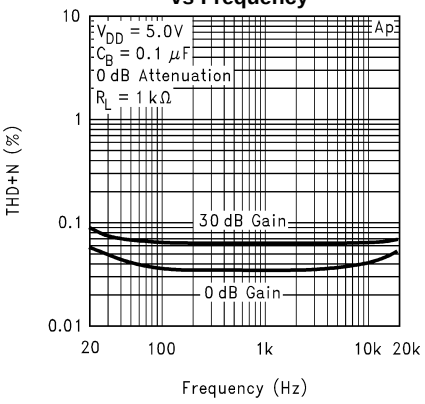

Figure 19.

Loop-out THD+N vs Frequency

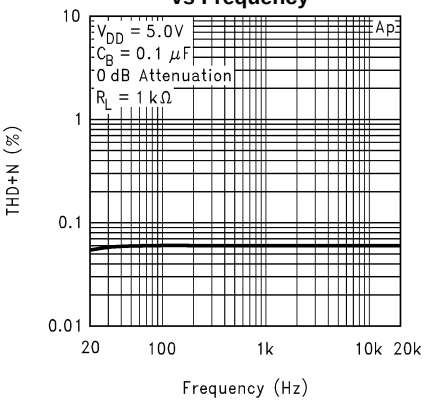

Figure 20.

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Typical Performance Characteristics (continued)

Bass Response vs Frequency

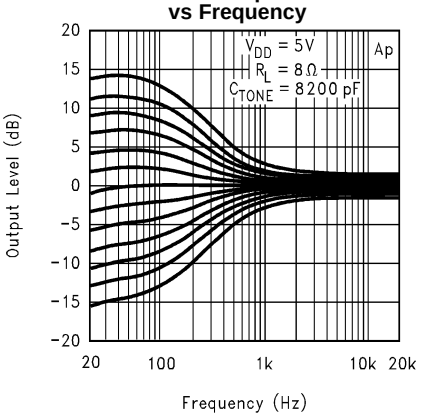

Figure 21.

Treble Response vs Frequency

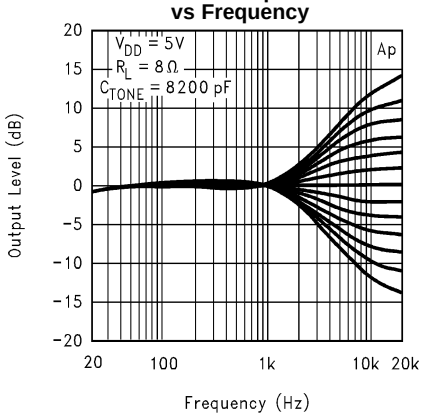

Figure 22.

Bass and Treble Response vs Frequency

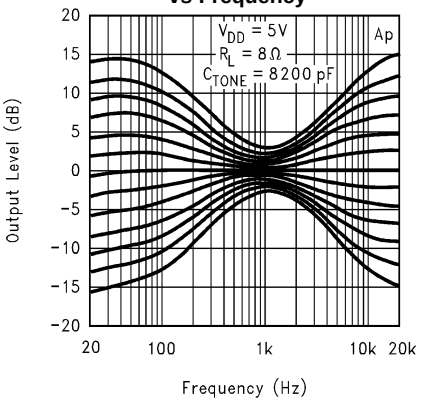

Figure 23.

Supply Current vs Temperature

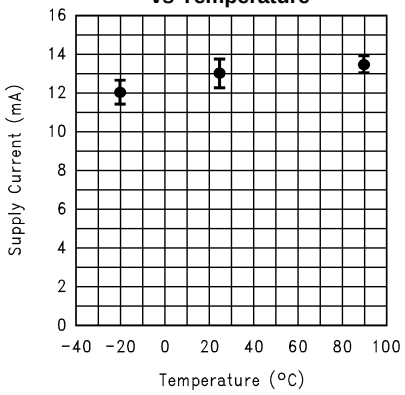

Figure 24.

TEST CIRCUIT DIAGRAMS

Timing Diagrams

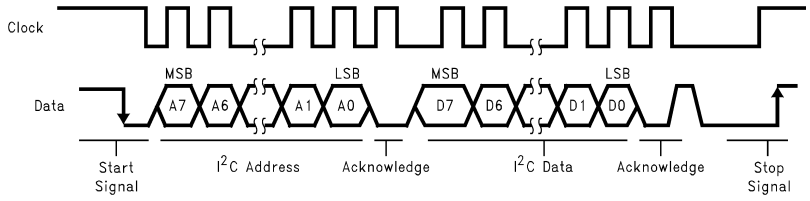

Figure 25. I^2C Bus Format

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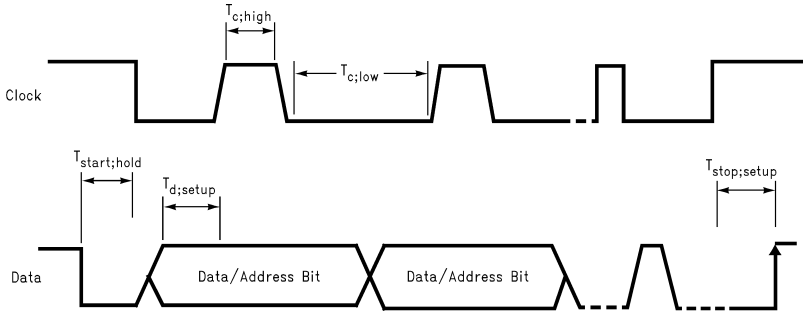
TEST CIRCUIT DIAGRAMS (continued)



See Electrical Characteristics section for timing specifications

Figure 26. I^2C Timing Diagram

Truth Tables

SOFTWARE SPECIFICATION

Table 1. Chip Address

MSB							LSB
1	0	0	0	0	*E.C.	*E.C.	0

*E.C. = Externally Configuarable

Table 2. Data Bytes (Brief Description)

MSB							LSB	Function
0	0	0	X	X	D2	D1	D0	Input Volume Control
0	0	1	X	D3	D2	D1	D0	Bass Control
0	1	0	X	D3	D2	D1	D0	Treble Control
0	1	1	D4	D3	D2	D1	D0	Right Output Vol./Mute
1	0	0	D4	D3	D2	D1	D0	Left Output Vol./Mute
1	0	1	X	$D_1$1	$D_1$0	$D_0$1	$D_0$0	Mic Input and Gain
1	1	0	D4	D3	D2	D1	D0	Microphone Volume
1	1	1	$D_4$0	$D_3$0	$D_2$0	$D_1$0	$D_0$0	General Control

Table 3. Input Volume Control

MSB							LSB	Attenuation (dB)
0	0	0	X	X	0	0	0	0
0	0	0	X	X	0	0	1	−2
0	0	0	X	X	0	1	0	−4
0	0	0	X	X	0	1	1	−6
0	0	0	X	X	1	0	0	−8
0	0	0	X	X	1	0	1	−10
0	0	0	X	X	1	1	0	−12
0	0	0	X	X	1	1	1	−14
Input Volume Control Power Up State			X	X	0	0	0	Input Volume Control at 0 dB Attenuation

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Table 4. Bass Control

MSB							LSB	Level (dB)
0	0	1	X	0	0	0	0	−12
0	0	1	X	0	0	0	1	−10
0	0	1	X	0	0	1	0	−8
0	0	1	X	0	0	1	1	−6
0	0	1	X	0	1	0	0	−4
0	0	1	X	0	1	0	1	−2
0	0	1	X	0	1	1	0	0
0	0	1	X	0	1	1	1	2
0	0	1	X	1	0	0	0	4
0	0	1	X	1	0	0	1	6
0	0	1	X	1	0	1	0	8
0	0	1	X	1	0	1	1	10
0	0	1	X	1	1	0	0	12
Bass Control Power Up State			X	0	1	1	0	Bass Control is Flat

Table 5. Treble Control

MSB							LSB	Level (dB)
0	1	0	X	0	0	0	0	−12
0	1	0	X	0	0	0	1	−10
0	1	0	X	0	0	1	0	−8
0	1	0	X	0	0	1	1	−6
0	1	0	X	0	1	0	0	−4
0	1	0	X	0	1	0	1	−2
0	1	0	X	0	1	1	0	0
0	1	0	X	0	1	1	1	2
0	1	0	X	1	0	0	0	4
0	1	0	X	1	0	0	1	6
0	1	0	X	1	0	1	0	8
0	1	0	X	1	0	1	1	10
0	1	0	X	1	1	0	0	12
Treble Control Power Up State			X	0	1	1	0	Treble Control is Flat

Table 6. Left Volume Control

MSB							LSB	Function
1	0	0	0	0	0	0	0	20
1	0	0	0	0	0	0	1	18
1	0	0	. . .	. . .	. . .	. . .	. . .	. . .
1	0	0	1	1	1	0	1	−38
1	0	0	1	1	1	1	0	−40
1	0	0	1	1	1	1	1	Left Channel Mute
Left Volume Control Power Up State			1	1	1	1	1	Left Channel is Muted

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Table 7. General Control

MSB							LSB	Function
1	1	1					0	Chip On
1	1	1					1	Chip Shutdown
1	1	1				0		G.P.O. Output Low
1	1	1				1		G.P.O. Output High
1	1	1			0			Stereo Enhance Off
1	1	1			1			Stereo Enhance On
1	1	1		0				Stereo Operation
1	1	1		1				Mono Force On
1	1	1	0					External Loop Disable
1	1	1	1					External Loop Enable
General Control Power Up State			0	0	0	0	0	

Table 8. Right Volume Control

MSB							LSB	Level (dB)
0	1	1	0	0	0	0	0	20
0	1	1	0	0	0	0	1	18
0	1	1	. . .	. . .	. . .	. . .	. . .	. . .
0	1	1	1	1	1	0	0	−38
0	1	1	1	1	1	1	0	−40
0	1	1	1	1	1	1	1	Right Channel Mute
Right Volume Control Power Up State			1	1	1	1	1	Right Channel Is Muted

Table 9. Microphone Input Selection and Gain

MSB							LSB	Function
1	0	1	X			0	0	Mic Input 1
1	0	1	X			0	1	Mic Input 2
1	0	1	X			1	X	Mic Input 1 and 2
1	0	1	X	0	0			Mic Gain (+0 dB)
1	0	1	X	0	1			Mic Gain (+20 dB)
1	0	1	X	1	0			Mic Gain (+30 dB)
Mic Input Sel. and Gain Power Up State			X	1	0	0	0	Mic 1 is selected with a +30 dB gain

Table 10. Microphone Volume Control

MSB							LSB	Function
1	1	0	0	0	0	0	0	18
1	1	0	0	0	0	0	1	15
1	1	0	. . .	. . .	. . .	. . .	. . .	. . .
1	1	0	1	0	1	0	0	−42
1	1	0	1	0	1	0	1	Microphone Muted
Mic Volume Control Power Up State			1	0	1	0	1	Microphone Muted

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APPLICATION INFORMATION

GROUNDING

In order to achieve the best possible performance, certain grounding techniques should be followed. All input reference grounds should be tied with their respective source grounds and brought back to the power supply ground separately from the output load ground returns. These input grounds should also be tied in with the half-supply bypass ground. Bringing the ground returns for the output loads back to the supply separately will keep large signal currents from interfering with the stable AC input ground references.

LAYOUT

As stated in the Grounding section, placement of ground return lines is critical for maintaining the highest level of system performance. It is not only important to route the correct ground return lines together, but also important to be aware of where those ground return lines are routed in conjunction with each other. The output load ground returns should be physically located as far as reasonably possible from low signal level lines and their ground return lines. Critical signal lines are those relating to the microphone amplifier section, since these lines generally work at very low signal levels.

SUPPLY BYPASSING

As with all op amps and power op amps, the LM4832 requires the supplies to be bypassed to avoid oscillation. To avoid high frequency instabilities, a 0.1 µF metallized-film or ceramic capacitor should be used to bypass the supplies as close to the chip as possible. For low frequency considerations, a 10 µF or greater tantalum or electrolytic capacitor should be paralleled with the high frequency bypass capacitor.

If power supply bypass capacitors are not sufficiently large, the current in the power supply leads, which is a rectified version of the output current, may be fed back into internal circuitry. This internal feedback signal can cause high frequency distortion and oscillation.

If power supply lines to the chip are long, larger bypass capacitors could be required. Long power supply leads have inductance and resistance associated with them, that could prevent peak low frequency current demands from being met. The extra bypass capacitance will reduce the peak current requirements from the power supply lines.

POWER-UP STATUS

On power-up or after a hard reset, the LM4832 registers will be initialized with the default values listed in the truth tables. By default, the LM4832 power and microphone outputs are muted, the tone controls are all flat, Texas Instruments 3D Enhance is off, the chip is in stereo mode, and the microphone input 1 is selected with +30 dB of gain.

CLICK AND POP CIRCUITRY

The LM4832 contains circuitry to minimize turn-on transients or “click and pops”. In this case, turn-on refers to either power supply turn-on or the device coming out of shutdown mode. When the deviceis turning on, the amplifiers are internally configured as unity gain buffers. An internal current source charges the bypass capacitor on the bypass pin. Both the inputs and outputs ideally track the voltage at the bypass pin. The device will remain in buffer mode until the bypass pin has reached its half supply voltage, 1/2 V_{DD}. As soon as the bypass node is stable, the device will become fully operational.

Although the bypass pin current source cannot be modified, the size of the bypass capacitor, C_B, can be changed to alter the device turn-on time and the amount of “click and pop”. By increasing C_B, the amount of turn-on pop can be reduced. However, the trade-off for using a larger bypass capacitor is an increase in the turn-on time for the device. Reducing C_B will decrease turn-on time and increase “click and pop”. If C_B is too small, the LM4832 can develop a low-frequency oscillation (“motorboat”) when used at high gains.

There is a linear relationship between the size of C_B and the turn-on time. Some typical turn-on times for different values of C_B are:

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C_b	T_{ON}
0.01 µF	20 ms
0.1 µF	200 ms
0.22 µF	420 ms

In order to eliminate “click and pop”, all capacitors must be discharged before turn-on. Rapid on/off switching of the device or shutdown function may cause the “click and pop” circuitry to not operate fully, resulting in increased “click and pop” noise. The output coupling cap, C_O, is of particular concern. This capacitor discharges through an internal 20 kΩ resistor. Depending on the size of C_O, the time constant can be quite large. To reduce transients, an external 1 kΩ–5 kΩ resistor can be placed in parallel with the internal 20 kΩ resistor. The tradeoff for using this resistor is an increase in quiescent current.

COUPLING CAPACITORS

Because the LM4832 is a single supply circuit, all audio signals must be capacitor coupled to the chip to remove the 2.5 V_{DC} bias. All audio inputs have 20 kΩ input impedances, so the AC-coupling capacitor will create a high-pass filter with

$$f_{-3dB} = 1/(2\pi * 20\ k\Omega * C_{IN}). \quad (1)$$

The amplifier outputs also need to be AC-coupled to the loads.The high-pass filter is comprised of the output load and the coupling capacitor,where the filter cutoff is at

$$f_{-3dB} = 1/(2\pi * R_{LOAD} * C_{OUT}). \quad (2)$$

POWER AMPLIFIER

The power amplifiers in the LM4832 are designed to drive 8Ω or 32Ω loads at 200 mW (continuous) and 75 mW (continuous), respectively, with 1% THD+N. As shown in the Typical Performance Characteristics, the power amplifiers typically drive 4Ω loads at 350 mW, but with a slight increase in high-frequency THD. As discussed above, these outputs should be AC-coupled to the output load.

MICROPHONE AMPLIFIER

The microphone preamplifier is intended to amplify low-level signals for signal conditioning. The microphone inputs can be directly connected to microphone networks. The microphone amplifier has enough output capability to drive a 1 kΩ load. All microphone inputs and outputs must be AC-coupled.

I^2C INTERFACE

The LM4832 uses a serial bus, which conforms to the I^2C protocol, to control the chip's functions with two wires: clock and data. The clock line is uni-directional. The data line is bi-directional(open-collector) with a pullup resistor (typically 10 kΩ).The maximum clock frequency specified by the I^2C standard is 400 kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4832.

The I^2C address for the LM4832 is determined using the Address Bit 1 and Address Bit 2 TTL/CMOS inputs on the chip. The LM4832's four possible I^2C chip addresses are of the form $10000X_2X_10$ (binary), where the X_2 and X_1bits are determined by the voltage levels at the Address Bit 2 and Address Bit 1 pins, respectively. If the I^2C interface is used to address a number of chips in a system and the LM4832's chip address can be changed to avoid address conflicts.

The timing diagram for the I^2C is shown in Figure 2. The data is latched in on the stable high level of the clock and the data line should be held high when not in use. The timing diagram is broken up into six major sections:

The “start” signal is generated by lowering the data signal while the clock signal is high. The start signal will alert all devices attached to the I^2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the clock level is high.

After the last bit of the address is sent, the master checks for the LM4832's acknowledge. The master releases the data line high (through a pullup resistor). Then the master sends a clock pulse. If the LM4832 has received the address correctly, then it holds the data line low during the clock pulse. If the data line is not low, then the master should send a “stop” signal (discussed later) and abort the transfer.

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The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable high.

After the data byte is sent, the master must generate another acknowledge to see if the LM4832 received the data.

If the master has more data bytes to send to the LM4832, then the master can repeat the previous two steps until all data bytes have been sent.

The “stop” signal ends the transfer. To signal “stop”, the data signal goes high while the clock signal is high.

3D AUDIO ENHANCEMENT

The LM4832 has a 3D audio enhancement effect that helps improve the apparent stereo channel separation when, because of cabinet or equipment limitations, the left and right speakers are closer to each other than optimal.

An external RC network, shown in Figure 25, is required to enable the effect. The amount of the effect is set by the 20 kΩ resistor. A 0.1 µF capacitor is used to reduce the effect at frequencies below 80 Hz. Decreasing the resistor size will make the 3D effect more pronounced and decreasing the capacitor size will raise the cutoff frequency for the effect.

The 680 kΩ resistor across the 0.1 µF capacitor reduces switching noise by discharging the capacitor when the effect is not in use.

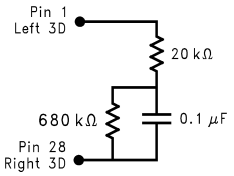

Figure 27. 3D Effect Components

TONE CONTROL RESPONSE

Bass and treble tone controls are included in the LM4832. The tone controls use two external capacitors for each stereo channel. Each has a corner frequency determined by the value of C2 and C3 (see Figure 26) and internal resistors in the feedback loop of the internal tone amplifier.

Typically, C2 = C3 and for 100 Hz and 10 kHz corner frequencies, C2 = C3 = 0.0082 µF. Altering the ratio between C2 and C3, changes the midrange gain. For example, if C2 = 2(C3), then the frequency response will be flat at 20 Hz and 20 kHz, but will have a 6 dB peak at 1 kHz.

With C = C2 = C3, the treble turn-over frequency is nominally

$$f_{TT} = 1/(2\pi C(14\ k\Omega)) \quad (3)$$

and the bass turn-over frequency is nominally

$$f_{BT} = 1/(2\pi C(30.4\ k\Omega)), \quad (4)$$

when maximum boost is chosen. The inflection points (the frequencies where the boost or cut is within 3 dB of the final value) are, for treble and bass respectively,

$$f_{TI} = 1/(2\pi C(1.9\ k\Omega)) \quad (5)$$

$$f_{BI} = 1/(2\pi C(169.6\ k\Omega)) \quad (6)$$

Increasing the values of C2 and C3 decreases the turnover and inflection frequencies: i.e., the Tone Control Response Curves shown in Typical Performance Characteristics will shift left when C2 and C3 are increased and shift right when C2 and C3 are decreased. With C2 = C3 = 0.0082 µF, 2 dB steps are achieved at 100 Hz and 10 kHz. Changing C2 and C3 to 0.01 µF shifts the 2 dB step frequency to 72 Hz and 8.3 kHz.If the tone control capacitors' size is decreased these frequencies will increase.With C2 = C3 = 0.0068 µF the 2 dB steps take place at 130 Hz and 11.2 kHz.

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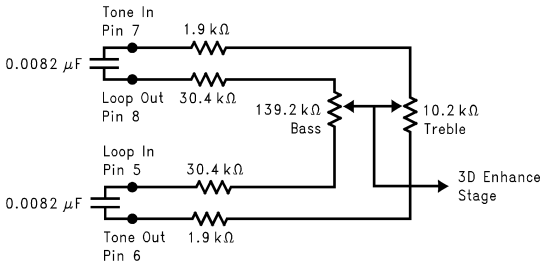

Figure 28. Tone Control Diagram

GENERAL PURPOSE OUTPUT PIN

The General Purpose Output pin is intended to be used as a control signal for other devices, such as an external power amplifier. This pin is controlled through the I^2C interface and is not relatedto any other functions within the LM4832. Refer to the Truth Tables section for the proper I^2C data bits to utilize this function.

Figure 29 shows an example of using the General Purpose Output to interface with an external power amp. In this case, the external power amp is the LM4755 stereo 10 watt per channel (rms) power amplifier with mute. AC-coupling capacitors must be used to remove the DC bias present between the LM4832 outputs and the external power amplifier inputs.

Prior to placing any of the preamp circuitry in shutdown, the General Purpose Output should be used to disable the external power amplifier.This will prevent any shutdown transients in the preamp circuitry from being amplified by the external power amplifier.

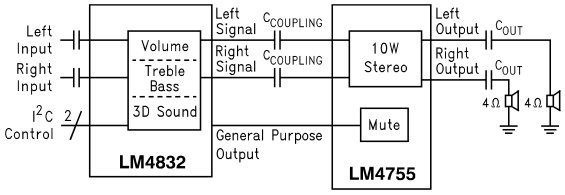

Figure 29. 10W/ch System with I^2C Controlled Tone,Volume and 3D Sound

LOOP IN/OUT PINS

The Loop In and Loop Out pins are used when an application requires a special function to be performed on the audio signal. As shown in Figure 30, the audio signal is taken from the Loop Out pin and sent to an external signal processor. After the signal is processed externally, it is fed back into the Loop In pin.

An example of where this functionality would be used is computer speakers. The external loop could be used to provide bass boost to counteract the speaker's natural or baffle-induced rolloff.

Since the Loop In pin goes directly to the input of a CMOS amplifier, the input impedance is very high. The Loop Out pin is driven by the input attenuation amplifier, which is capable of driving impedances as low as 1 kΩ.

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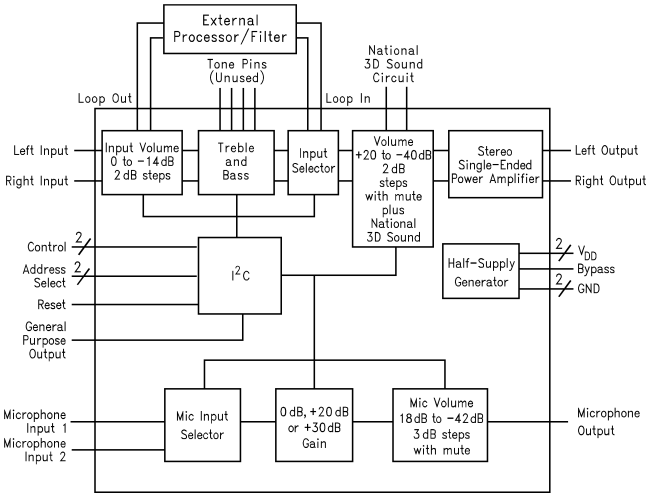

Figure 30.

LM4832 SAMPLE LAYOUT

LAYOUT PARTS LIST		
Name	**Type**	**Quantity**
Capacitors:		
C1	1µF, Tantalum, 16V, 10%	1
C2	0.1µF, Tantalum, 16V, 10%	1
C3	0.1µF, Tantalum, 16V, 10%	1
C4	1µF, Tantalum, 16V, 10%	1
C5	8200pF, Ceramic, 50V, 10%	1
C6	8200pF, Ceramic, 50V, 10%	1
C7	1µF, Tantalum, 16V, 10%	1
C8	1µF, Tantalum, 16V, 10%	1
C9	1µF, Tantalum, 16V, 10%	1
C10	10µF, Tantalum, 16V, 10%	1
C11	1µF, Tantalum, 16V, 10%	1
C12	470µF, Size D; or 300µF, 10V	1
C13	0.1µF, Tantalum, 50V, 10%	1
C14	470µF, Size D; 300µF, 10V	1
C15	8200pF, Ceramic, 50V, 10%	1
C16	8200pF, Ceramic, 50V, 10%	1
Resistors:		
RPD	1kΩ, 1/8W	1
RDGND	100Ω, 1/8W	1
R2	10kΩ, 1/8W	1
R3	10kΩ, 1/8W	1
R4	20kΩ, 1/8W	1
R5	680kΩ, 1/8W	1
Connectors:		
HDR 2X1	100mil	9
DB25SL connector - male		1

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Application Information

LAYOUT DESCRIPTION

The layout given in the following pages is meant to be connected to a PC by a parallel port (printer) cable. The board is controlled by software for a Windows PC. The parallel cable must be the standard type used for hooking up a printer to a PC: one end is a male DB-25 connector and the other end is a female DB-25 connector.

This layout is set up to allow the use of the internal tone-control circuitry or the external loop.

Typical Application PCB Layout

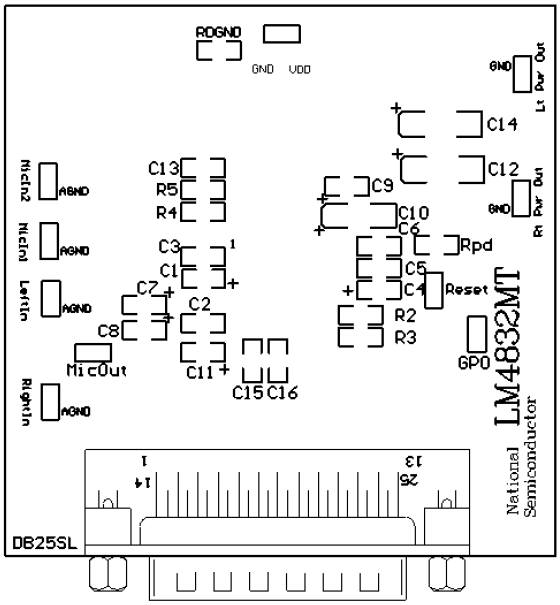

Figure 31. Top Silkscreen Layer

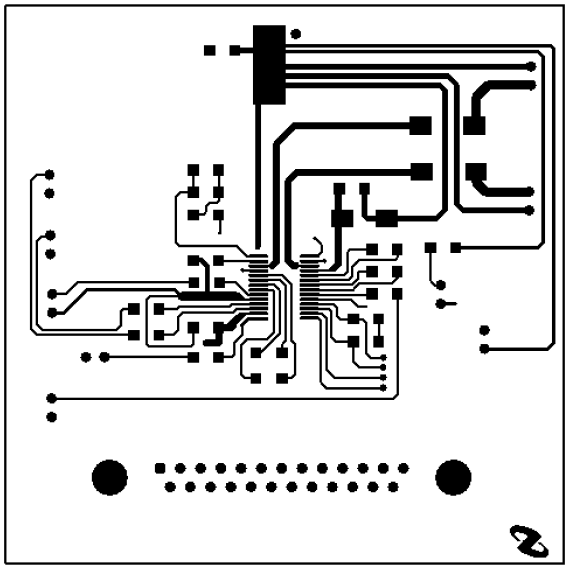

Figure 32. Top Layer

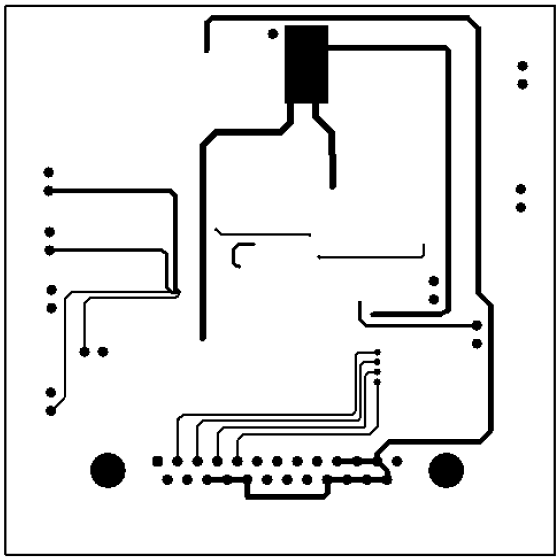

Figure 33. Bottom Layer

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	19

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