THE DATASHEET OF

LM4121IM5X-ADJ/NOPB

www.win-source.net 0086-755-83957316

LM4121 Precision Micropower Low Dropout Voltage Reference

Check for Samples: LM4121

FEATURES (LM4121-1.2)

- **Small SOT23-5 Package**
- **Low Voltage Operation**
- **High Output Voltage Accuracy: 0.2%**
- **Source and Sink Current Output: ±5 mA**
- **Supply current: 160 µA Typ.**
- **Low Temperature Coefficient: 50 ppm/°C**
- **Enable Pin**
- **Output Voltages: 1.25V and Adjustable**
- **Industrial Temperature Range: −40°C to +85°C**
- **(For Extended Temperature Range, −40°C to 125°C, Contact Texas Instruments)**

APPLICATIONS

- **Portable, Battery Powered Equipment**
- **Instrumentation and Process Control**
- **Automotive & Industrial**
- **Test Equipment**
- **Data Acquisition Systems**
- **Precision Regulators**
- **Battery Chargers**
- **Base Stations**
- **Communications**
- **Medical Equipment**

DESCRIPTION

The LM4121 is a precision bandgap voltage reference available in a fixed 1.25V and adjustable version with up to 5 mA current source and sink capability.

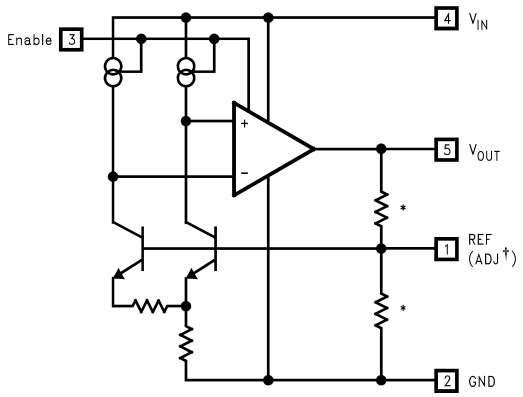
This series reference operates with input voltages as low as 1.8V and up to 12V consuming 160 µA (Typ.) supply current. In power down mode, device current drops to less than 2 µA.

The LM4121 comes in two grades A and Standard. The best grade devices (A) have an initial accuracy of 0.2%, while the standard have an initial accuracy of 0.5%, both with a tempco of 50ppm/°C ensured from −40°C to +125°C.

The very low operating voltage, low supply current and power-down capability of the LM4121 makes this product an ideal choice for battery powered and portable applications.

The device performance is ensured over the industrial temperature range (−40°C to +85°C), while certain specs are ensured over the extended temperature range (−40°C to +125°C). Please contact Texas Instruments for full specifications over the extended temperature range. The LM4121 is available in a standard 5-pin SOT-23 package.

Block Diagram



* Resistors are removed on the LM4121-ADJ
†LM4121-ADJ only

Figure 1. LM4121-1.2 Block Diagram

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Connection Diagrams

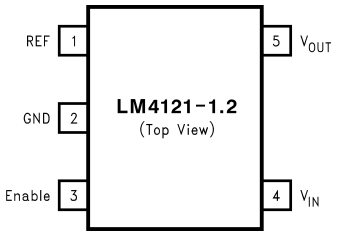

Figure 2. SOT23-5 Surface Mount Package

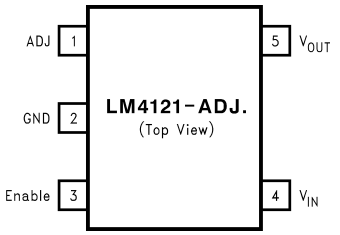

Figure 3. SOT23-5 Surface Mount Package

Table 1. SOT-23 Package Marking Information(1)

Field Information
First Field:
R = Reference
Second and third Field:
19 = 1.250V Voltage Option
20 = Adjustable
Fourth Field:
A-B = Initial Reference Voltage Tolerance
A = ±0.2%
B = ±0.5%

(1) Only four fields of marking are possible on the SOT-23's small surface. This table gives the meaning of the four fields.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Maximum Voltage on input or enable pins	−0.3V to 14V
Output Short-Circuit Duration	Indefinite
Power Dissipation (T_A = 25°C) (3):	
DBV0005B package − θ_{JA}	280°C/W
Power Dissipation	350 mW
ESD Susceptibility (4) Human Body Model Machine Model	 2 kV 200V
Lead Temperature:	
Soldering, (10 sec.)	+260°C
Vapor Phase (60 sec.)	+215°C
Infrared (15 sec.)	+220°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see Electrical Characteristics - LM4121-1.250V and Electrical Characteristics - LM4121-ADJ tables. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) Without PCB copper enhancements. The maximum power dissipation must be de-rated at elevated temperatures and is limited by T_{JMAX} (maximum junction temperature), θ_{J-A} (junction to ambient thermal resistance) and T_A (ambient temperature). The maximum power dissipation at any temperature is: $PDiss_{MAX} = (T_{JMAX} - T_A)/\theta_{J-A}$ up to the value listed in the Absolute Maximum Ratings.

(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

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Operating Range (1)

Storage Temperature Range	−65°C to +150°C
Ambient Temperature Range	−40°C to +85°C
Junction Temperature Range	−40°C to +125°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see Electrical Characteristics - LM4121-1.250V and Electrical Characteristics - LM4121-ADJ tables. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics LM4121-1.250V

Unless otherwise specified V_{IN} = 3.3V, I_{LOAD} = 0, C_{OUT} = 0.01µF, $T_A = T_j$ = 25°C. Limits with standard typeface are for T_j = 25°C, and limits in **boldface type** apply over the −40°C ≤ T_A ≤ +85°C temperature range.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OUT}	Output Voltage Initial Accuracy LM4121A-1.250			1.250	±0.2	%
	LM4121-1.250				±0.5	
TCV_{OUT}/°C	Temperature Coefficient	−40°C ≤ T_A ≤ +125°C		14	50	ppm/°c
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	1.8V ≤ V_{IN} ≤ 12V		0.0007	0.009 **0.012**	%/V
$\Delta V_{OUT}/\Delta I_{LOAD}$	Load Regulation	0 mA ≤ I_{LOAD} ≤ 1 mA		0.03	0.08 **0.17**	%/mA
		1 mA ≤ I_{LOAD} ≤ 5 mA		0.01	0.04 **0.1**	
		−1 mA ≤ I_{LOAD} ≤ 0 mA		0.04	0.12	
		−5 mA ≤ I_{LOAD} ≤ −1 mA		0.01		
Min-V_{IN}	Minimum Operating Voltage	I_{LOAD} = 5mA		1.5	**1.8**	V
V_N	Output Noise Voltage	0.1 Hz to 10 Hz		20		μV_{PP}
		10 Hz to 10 kHz		30		μV_{RMS}
I_S	Supply Current			160	250 **275**	µA
I_{SS}	Power-down Supply Current	V_{IN} = 12V Enable = 0.4V **Enable = 0.2V**			1 **2**	µA
V_H	Logic High Input Voltage		**1.6**	1.5		V
V_L	Logic Low Input Voltage			0.4	 **0.2**	V
I_H	Logic High Input Current			7	**15**	µA
I_L	Logic Low Input Current			0.1		µA
I_{SC}	Short Circuit Current	V_{IN} = 3.3V, V_{OUT} = 0		15		mA
			6		**30**	
		V_{IN} = 12V, V_{OUT} = 0		17		
			6		**30**	
Hyst	Thermal Hysteresis (3)	−40°C ≤ T_A ≤ 125°C		0.5		mV/V

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Averaging Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) Thermal hysteresis is defined as the change in +25°C output voltage before and after exposing the device to temperature extremes.

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Electrical Characteristics LM4121-1.250V (continued)

Unless otherwise specified V_{IN} = 3.3V, I_{LOAD} = 0, C_{OUT} = 0.01µF, T_A = T_j = 25°C. Limits with standard typeface are for T_j = 25°C, and limits in **boldface type** apply over the −40°C ≤ T_A ≤ +85°C temperature range.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
ΔV_{OUT}	Long Term Stability (4)	1000 hrs. @ 25°C		100		ppm

(4) Long term stability is change in V_{REF} at 25°C measured continuously during 1000 hrs.

Electrical Characteristics LM4121-ADJ

Unless otherwise specified V_{IN} = 3.3V, V_{OUT} = V_{REF}, I_{LOAD} = 0, C_{OUT} = 0.01µF, T_A = T_j = 25°C. Limits with standard typeface are for T_j = 25°C, and limits in **boldface type** apply over the −40°C ≤ T_A ≤ +85°C temperature range.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OUT} = V_{REF}	Output Voltage Initial Accuracy LM4121A-ADJ			1.216	±0.2	%
	LM4121-ADJ				±0.5	
TCV_{REF}/°C	Temperature Coefficient	−40°C ≤ T_A ≤ +125°C		14	50	ppm/°c
$\Delta V_{REF}/\Delta V_{IN}$	Line Regulation	1.8V ≤ V_{IN} ≤ 12V		0.0007	0.009 **0.012**	%/V
$\Delta V_{OUT}/\Delta I_{LOAD}$	Load Regulation	0 mA ≤ I_{LOAD} ≤ 1 mA		0.03	0.08 **0.17**	%/mA
		1 mA ≤ I_{LOAD} ≤ 5 mA		0.01	0.04 **0.1**	
		−1 mA ≤ I_{LOAD} ≤ 0 mA		0.04	0.12	
		−5 mA ≤ I_{LOAD} ≤ −1 mA		0.01		
Min-V_{IN}	Minimum Operating Voltage	I_{LOAD} = 5 mA		1.5	**1.8**	V
V_N	Output Noise Voltage (3)	0.1 Hz to 10 Hz		20		μV_{PP}
		10 Hz to 10 kHz		30		μV_{RMS}
I_S	Supply Current			160	250 **275**	µA
I_{SS}	Power-down Supply Current	V_{IN} = 12V Enable = 0.4V **Enable = 0.2V**			1 **2**	µA
I_{BIAS}	Reference Pin Bias Current	(4)	15	**40**		nA
V_H	Logic High Input Voltage		**1.6**	1.5		V
V_L	Logic Low Input Voltage			0.4	 **0.2**	V
I_H	Logic High Input Current			7	**15**	µA
I_L	Logic Low Input Current			0.1		µA
I_{SC}	Short Circuit Current	V_{OUT} = 0		15		mA
			6		**30**	
		V_{IN} = 12V, V_{OUT} = 0		17		
			6		**30**	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Averaging Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) Output noise for 1.25V option. Noise is proportional to V_{OUT}.
(4) Bias Current flows out of the Adjust pin.

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Electrical Characteristics
LM4121-ADJ (continued)

Unless otherwise specified V_{IN} = 3.3V, V_{OUT} = V_{REF}, I_{LOAD} = 0, C_{OUT} = 0.01µF, T_A = T_j = 25°C. Limits with standard typeface are for T_j = 25°C, and limits in **boldface type** apply over the −40°C ≤ T_A ≤ +85°C temperature range.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Hyst	Thermal Hysteresis (5)	−40°C ≤ T_A ≤ 125°C		0.5		mV/V
ΔV_{OUT}	Long Term Stability (6)	1000 hrs. @ 25°C		100		ppm

(5) Thermal hysteresis is defined as the change in +25°C output voltage before and after exposing the device to temperature extremes.
(6) Long term stability is change in V_{REF} at 25°C measured continuously during 1000 hrs.

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LM4121- (All Options) Typical Operating Characteristics

Unless otherwise specified, V_{IN} = 3.3V, V_{OUT} = 1.25V, I_{LOAD} = 0, C_{OUT} = 0.022µF, T_A = 25°C and V_{EN} = V_{IN}.

Minimum Input Voltage vs Temperature

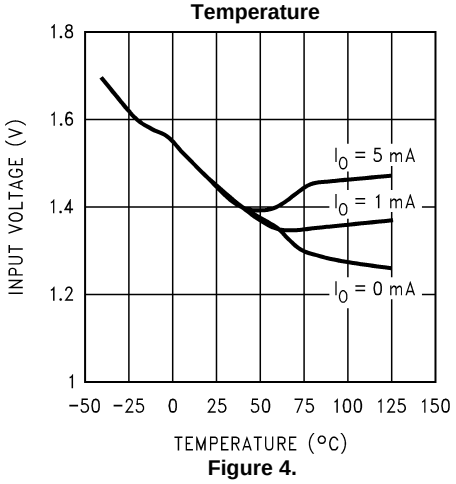

Figure 4.

GND Pin Current vs V_{IN}

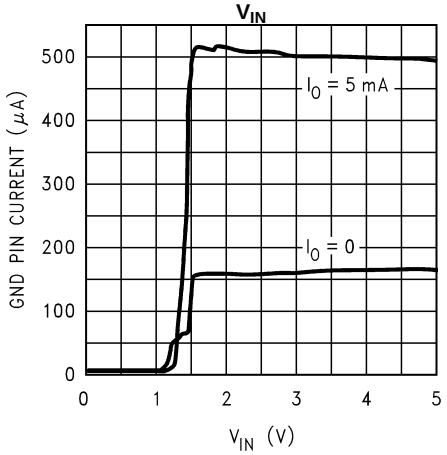

Figure 5.

GND Pin Current at No Load vs Temperature

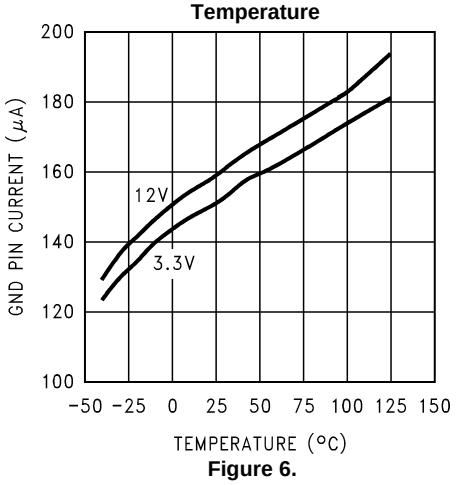

Figure 6.

GND Pin Current vs Load

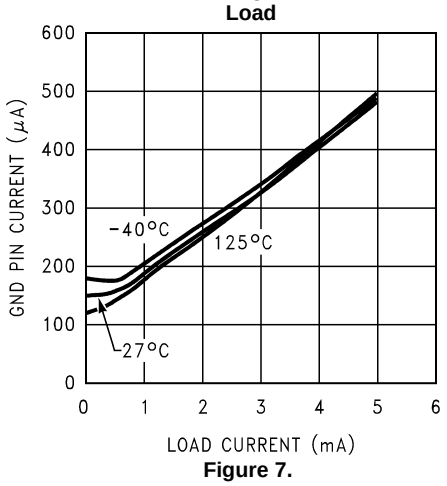

Figure 7.

Short Circuit vs Temperature

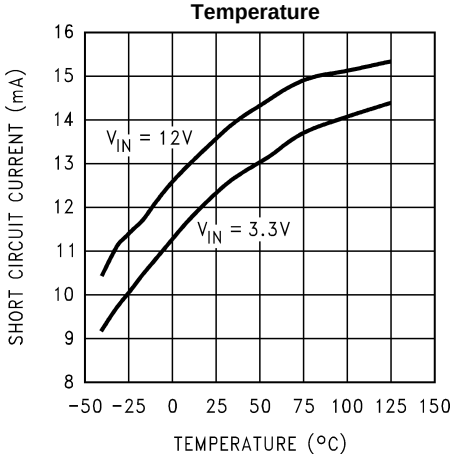

Figure 8.

Output Impedance vs Frequency

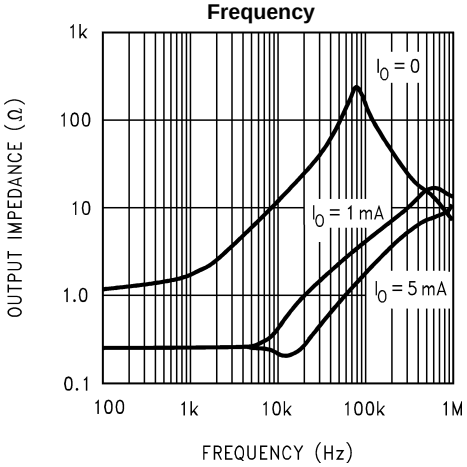

Figure 9.

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LM4121- (All Options) Typical Operating Characteristics (continued)

Unless otherwise specified, V_{IN} = 3.3V, V_{OUT} = 1.25V, I_{LOAD} = 0, C_{OUT} = 0.022µF, T_A = 25°C and V_{EN} = V_{IN}.

PSRR vs Frequency

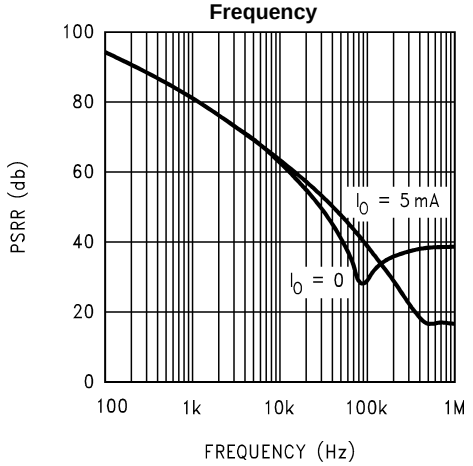

Figure 10.

Enable Pin Current

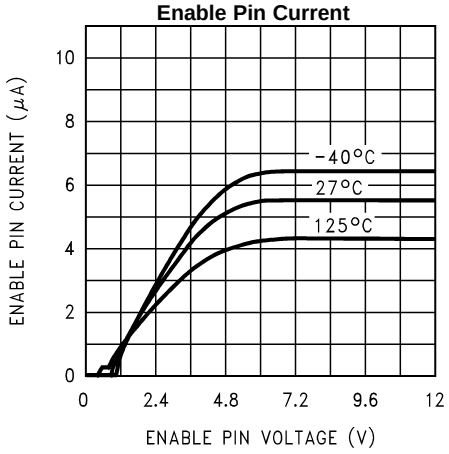

Figure 11.

Start-Up Response

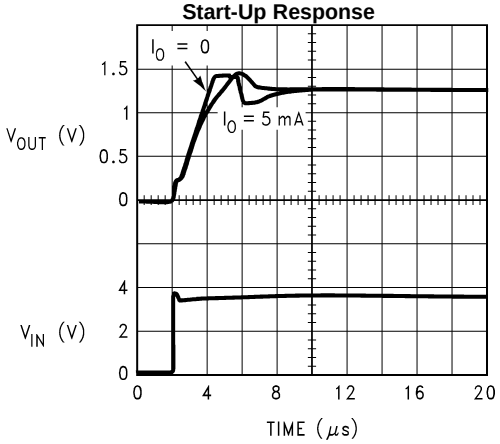

Figure 12.

Enable Response

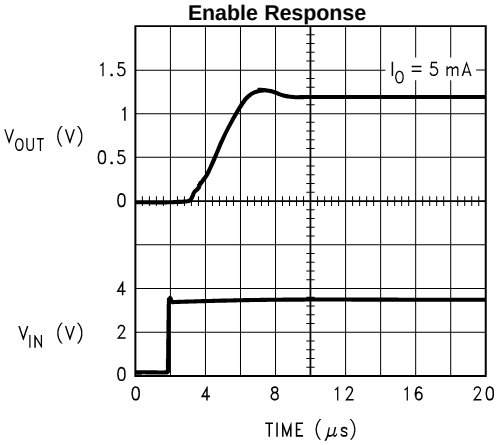

Figure 13.

Load Step Response

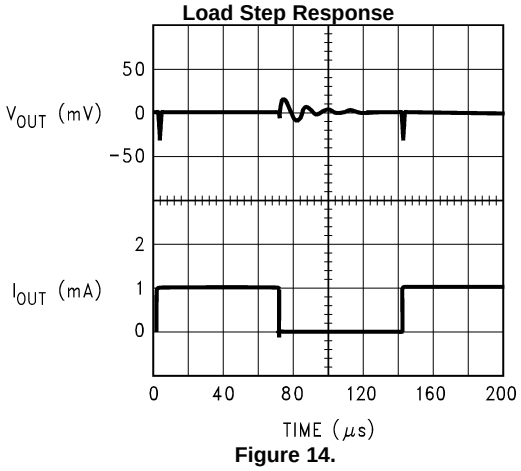

Figure 14.

Load Step Response

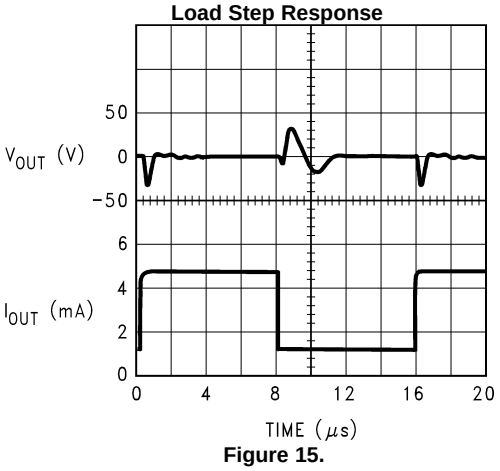

Figure 15.

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LM4121- (All Options) Typical Operating Characteristics (continued)

Unless otherwise specified, V_{IN} = 3.3V, V_{OUT} = 1.25V, I_{LOAD} = 0, C_{OUT} = 0.022µF, T_A = 25°C and V_{EN} = V_{IN}.

Line Step Response

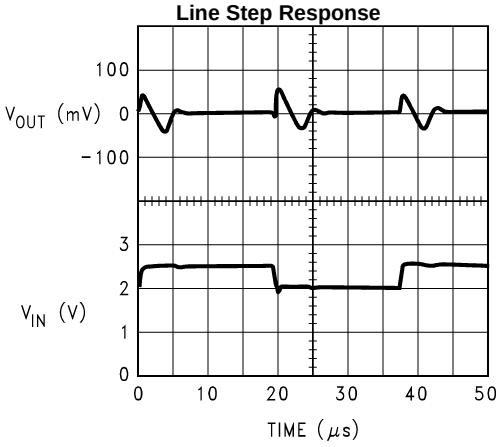

Figure 16.

Noise Spectural Density (0.1Hz-10Hz)

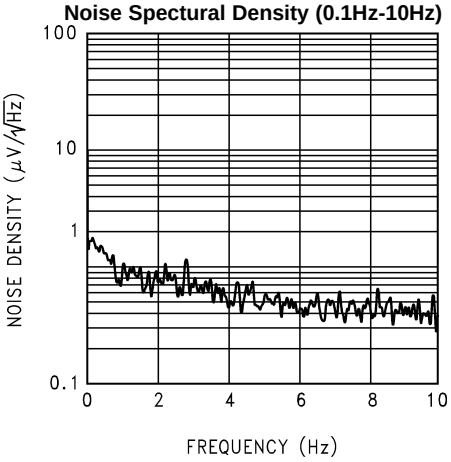

Figure 17.

Noise Spectural Density (10Hz-10kHz)

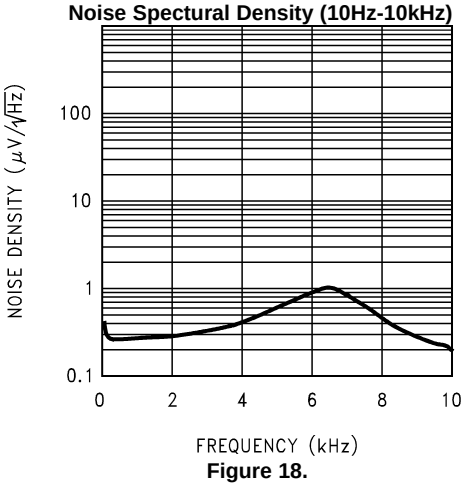

Figure 18.

Thermal Hysteresis

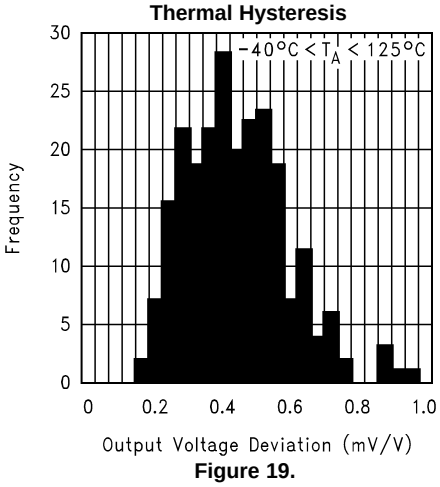

Figure 19.

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LM4121-1.25 Typical Operating Characteristics

Unless otherwise specified, V_{IN} = 3.3V, V_{OUT} = 1.25V, I_{LOAD} = 0, C_{OUT} = 0.022µF, T_A = 25°C and V_{EN} = V_{IN}.

Typical Temperature Drift

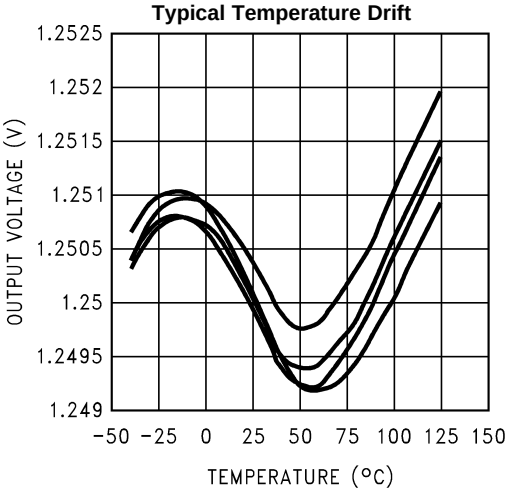

Figure 20.

Long Term Drift

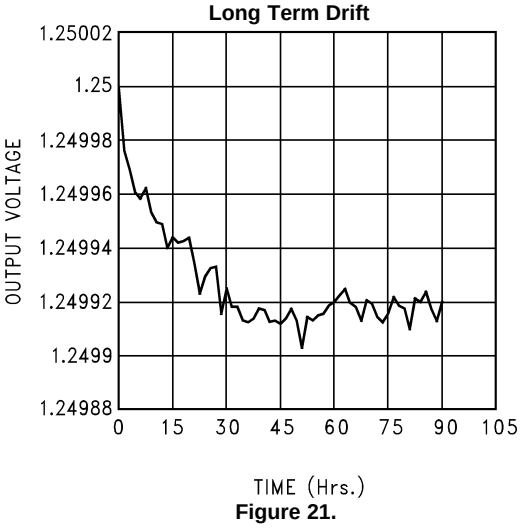

Figure 21.

Line Regulation

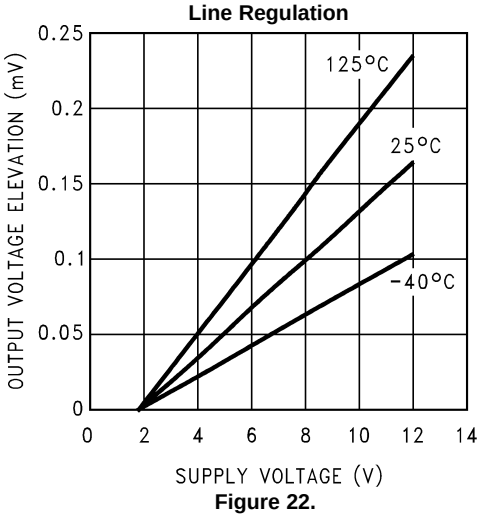

Figure 22.

Load Regulation

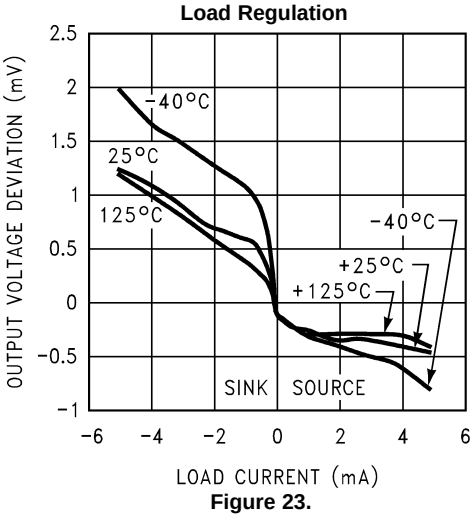

Figure 23.

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LM4121-ADJ Typical Operating Characteristics

Unless otherwise specified, V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{LOAD} = 0, C_{OUT} = 0.022µF, T_A = 25°C and V_{EN} = V_{IN}.

Typical Temperature Drift

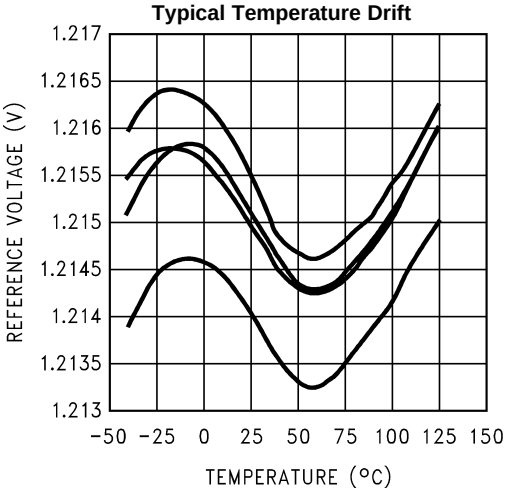

Figure 24.

Long Term Drift

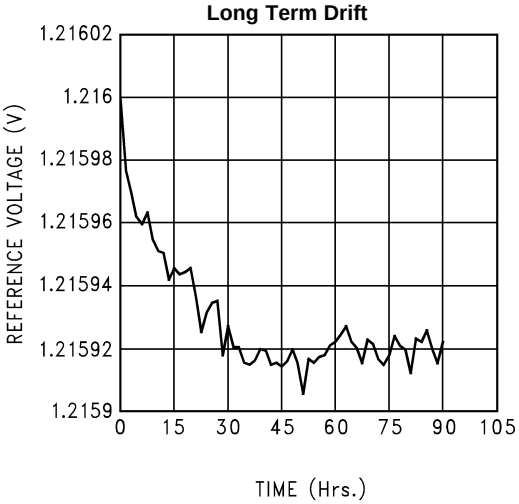

Figure 25.

Dropout Voltage vs Output Error

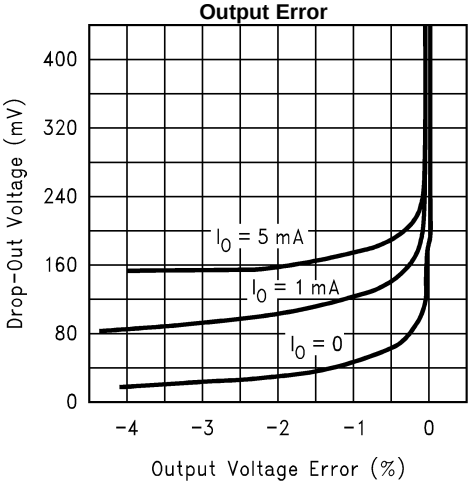

Figure 26.

Dropout Voltage vs Load Current

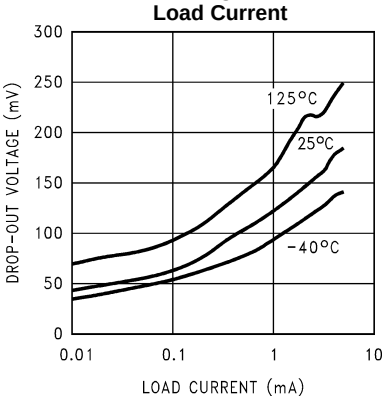

Figure 27.

Line Regulation

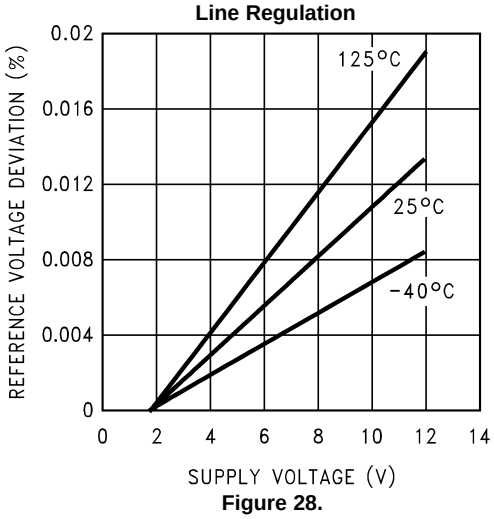

Figure 28.

Load Regulation

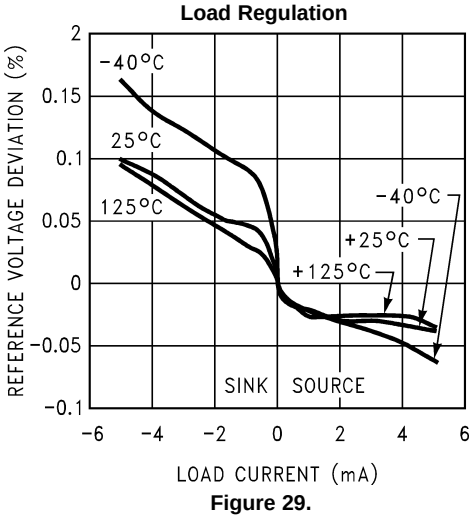

Figure 29.

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LM4121-ADJ Typical Operating Characteristics (continued)

Unless otherwise specified, V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{LOAD} = 0, C_{OUT} = 0.022µF, T_A = 25°C and V_{EN} = V_{IN}.

Adjust Pin Bias Current

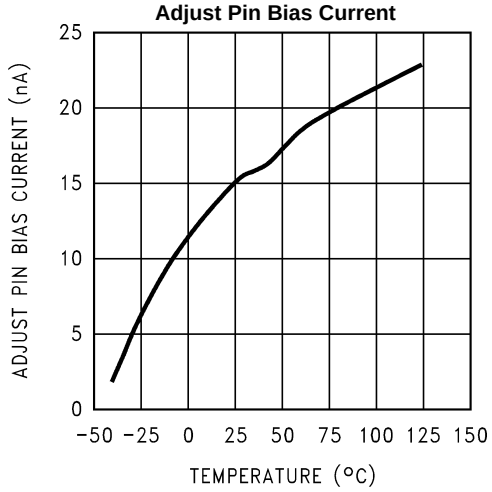

Figure 30.

Change In Reference Voltage vs Output Voltage

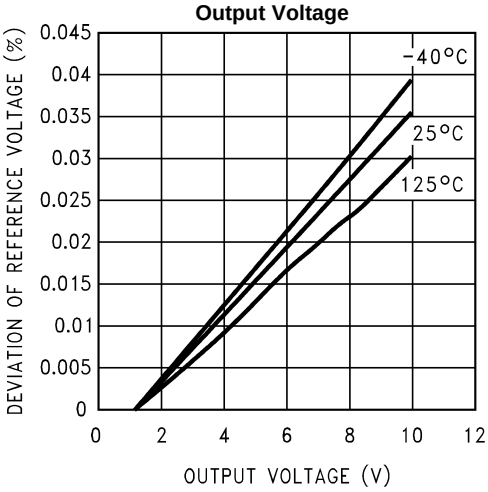

Figure 31.

Bode Plot

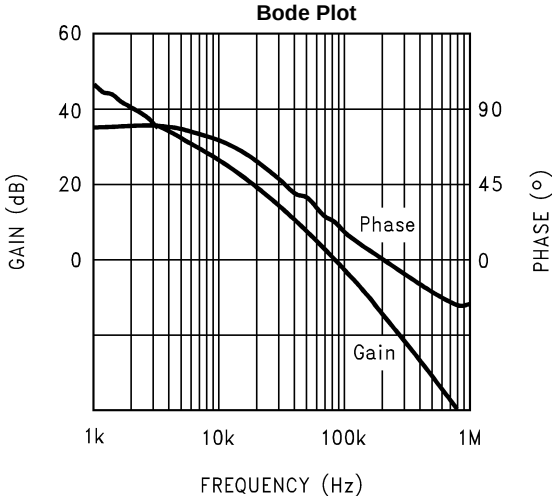

Figure 32.

Bode Plot

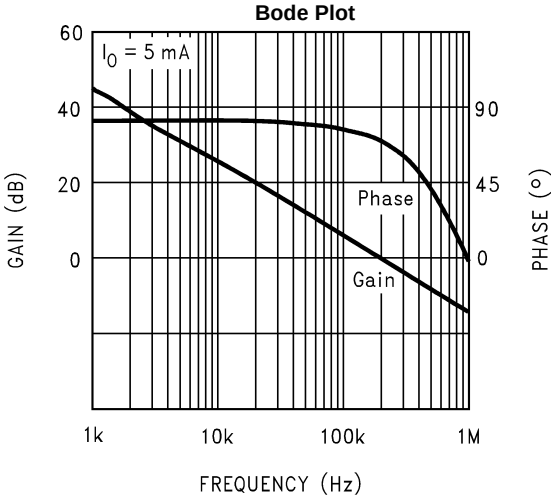

Figure 33.

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PIN DESCRIPTIONS

Output (Pin 5)	Reference Output.
Input (Pin 4)	Positive Supply.
Ground (Pin 2)	Negative Supply or Ground Connection
Enable (Pin 3)	Pulled to input for normal operation. Forcing this pin to ground will turn-off the output.
REF (Pin 1)	REF Pin (1.25V option only). This pin should be left unconnected for 1.25V option.
Adj (Pin 1)	V_{OUT} Adj Pin (Adjustable option only). See Application Hints section.

APPLICATION HINTS

The standard application circuit for the LM4121 is shown in Figure 34. The output voltage is set with the two feedback resistors, according to the following formula:

$$V_{OUT} = [V_{ref}(1+ R1/R2] - I_{bias} \bullet R1 \quad (1)$$

Values for R1 and R2 should be chosen to be less than 1 MΩ. I_{bias} typically flows out of the adjust pin. Values for V_{ref} and I_{bias} are found in the Electrical Characteristics - LM4121-1.250V and Electrical Characteristics - LM4121-ADJ tables. For best accuracy, be sure to take into account the variation of V_{REF} with input voltage, load and output voltage.

The LM4121 is designed to be stable with ceramic output capacitors in the range of 0.022µF to 0.047µF. Note that 0.022µF is the minimum required output capacitor. These capacitors typically have an ESR of about 0.1 to 0.5Ω. Smaller ESR can be tolerated, however larger ESR can not. The output capacitor can be increased to improve load transient response, up to about 1µF. However, values above 0.047µF must be tantalum. With tantalum capacitors, in the 1µF range, a small capacitor between the output and the reference (Adj) pin is required. This capacitor will typically be in the 50pF range. Care must be taken when using output capacitors of 1µF or larger. These application must be thoroughly tested over temperature, line and load. Also, when the LM4121 is used as a controller, with external active components, each application must be carefully tested to ensure a stable design. The adjust pin is sensitive to noise and capacitive loading. The trace to this pin must be as short as possible and the feedback resistors should be close to this pin. Also, a single point ground to the LM4121 will help ensure good accuracy at high load currents.

An input capacitor is typically not required. However, a 0.1µF ceramic can be used to help prevent line transients from entering the LM4121. Larger input capacitors should be tantalum or aluminium.

The enable pin is an analog input with very little hysteresis. About 6µA into this pin is required to turn the part on, and it must be taken close to GND to turn the part off (see Electrical Characteristics - LM4121-1.250V and Electrical Characteristics - LM4121-ADJ tables for thresholds). There is a *minimum* slew rate on this pin of about 0.003V/µS to prevent glitches on the output. All of these conditions can easily be met with ordinary CMOS or TTL logic. If the shutdown feature is not required, then this pin can safely be connected directly to the input supply. Floating this pin is not recommended.

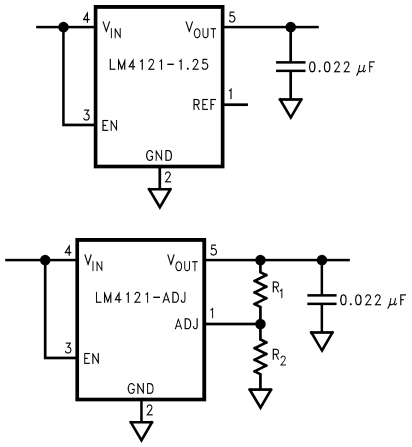

Figure 34. Standard Application Circuit

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PRINTED CIRCUIT BOARD LAYOUT CONSIDERATION

The mechanical stress due to PC board mounting can cause the output voltage to shift from its initial value. References in SOT packages are generally less prone to assembly stress than devices in Small Outline (SOIC) package.

To reduce the stress-related output voltage shifts, mount the reference on the low flex areas of the PC board such as near to the edge or the corner of the PC board.

Typical Application Circuits

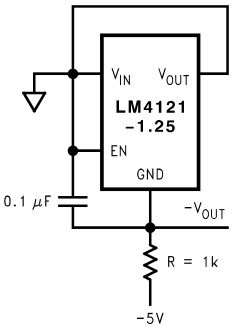

Figure 35. Voltage Reference with Negative Output

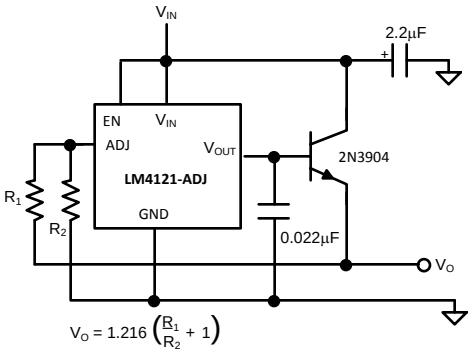

Figure 36. 100mA Quasi-LDO Regulator

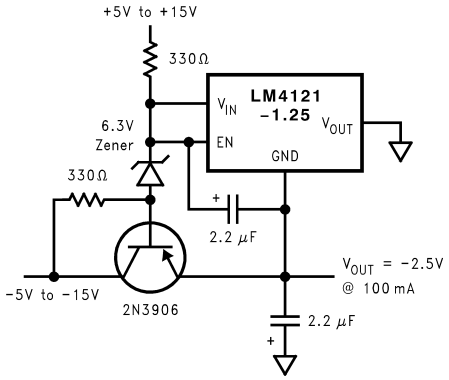

Figure 37. Boosted Output Current with Negative Voltage Reference

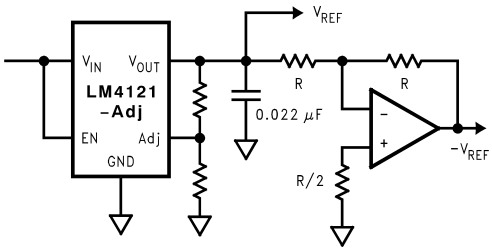

Figure 38. Voltage Reference with Complimentary Output

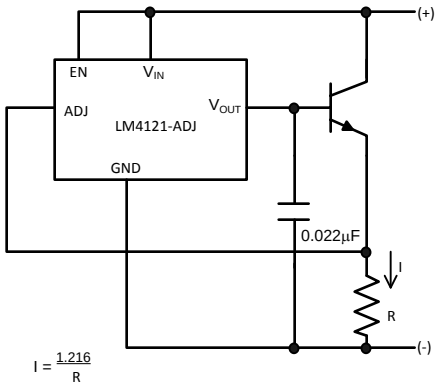

Figure 39. Two Terminal Constant Current Source

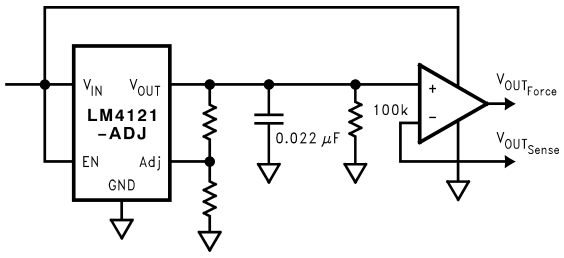

Figure 40. Precision Voltage Reference with Force and Sense Output

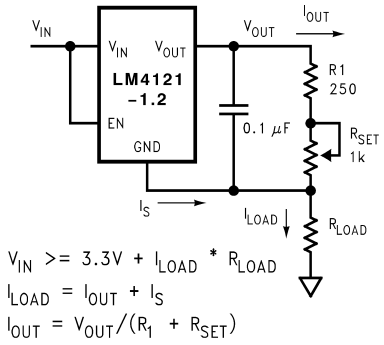

Figure 41. Programmable Current Source

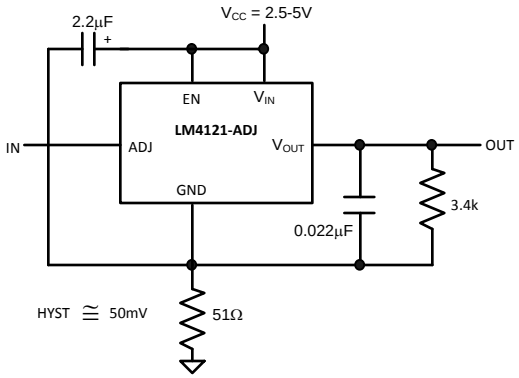

Figure 42. Precision Comparator with Hysteresis

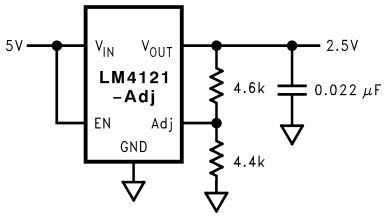

Figure 43. Power Supply Splitter

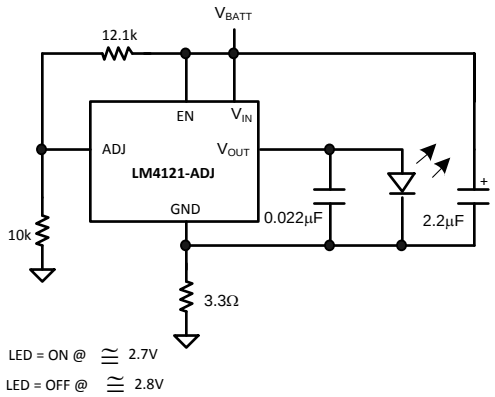

Figure 44. Li + Low Battery Detector

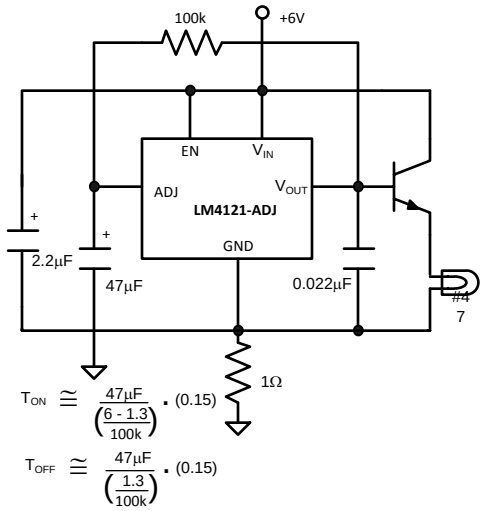

Figure 45. Flasher Circuit

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REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	14

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4121AIM5-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	R20A	Samples
LM4121AIM5X-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	R20A	Samples
LM4121IM5-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	R20B	Samples
LM4121IM5X-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	R20B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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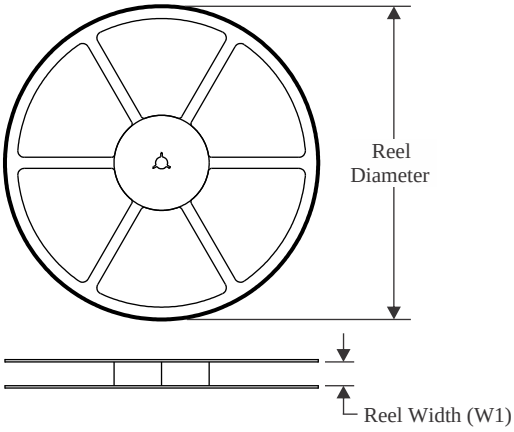
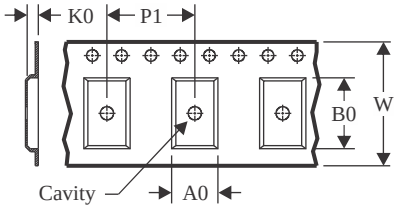
TAPE AND REEL INFORMATION

REEL DIMENSIONS

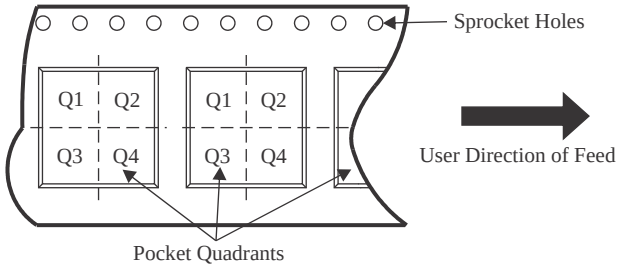


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

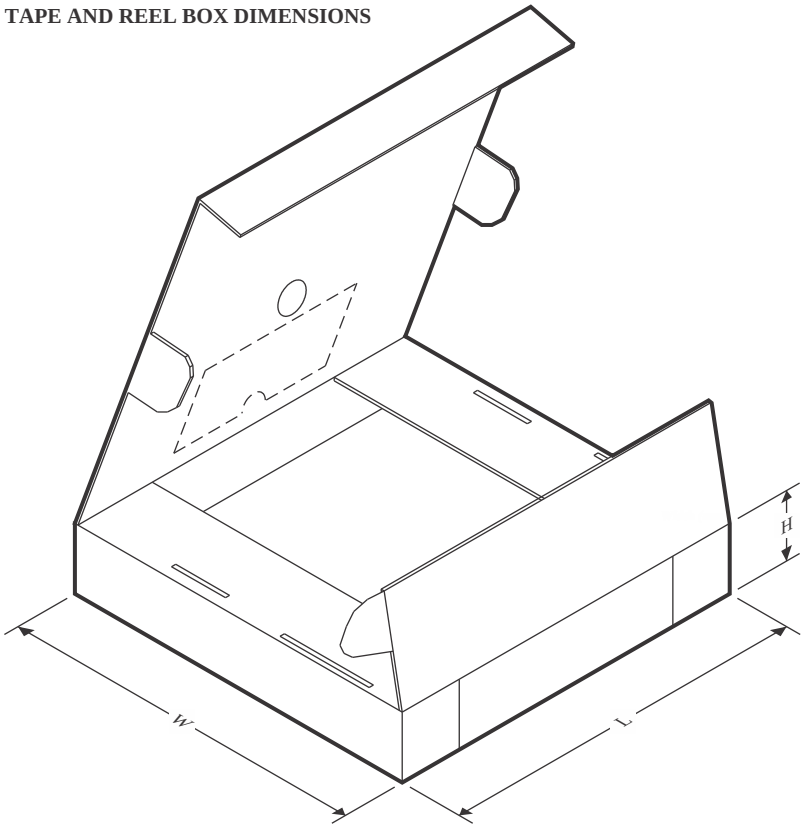
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4121AIM5-ADJ/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM4121AIM5X-ADJ/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM4121IM5-ADJ/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM4121IM5X-ADJ/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

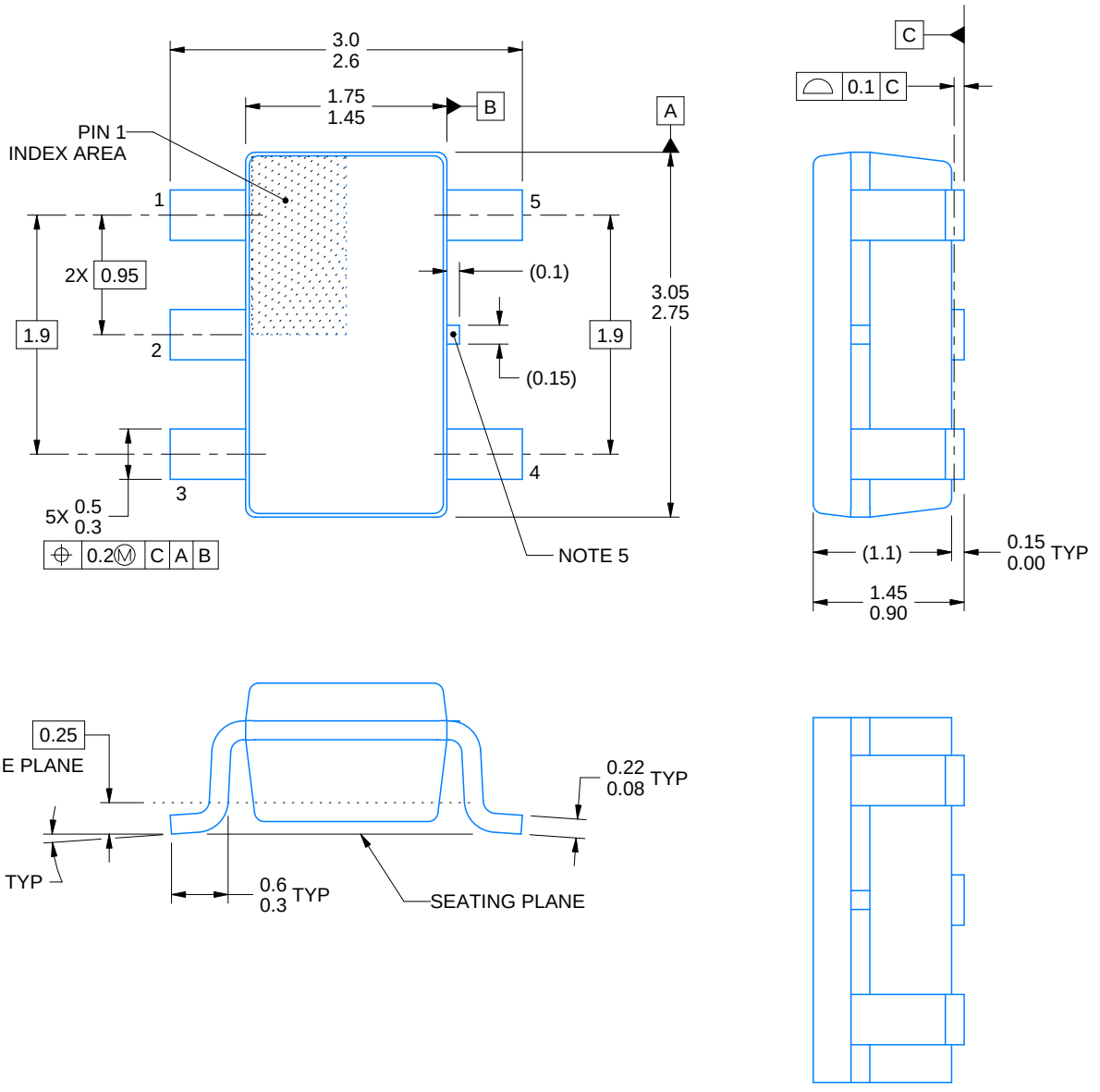
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4121AIM5-ADJ/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM4121AIM5X-ADJ/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM4121IM5-ADJ/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM4121IM5X-ADJ/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

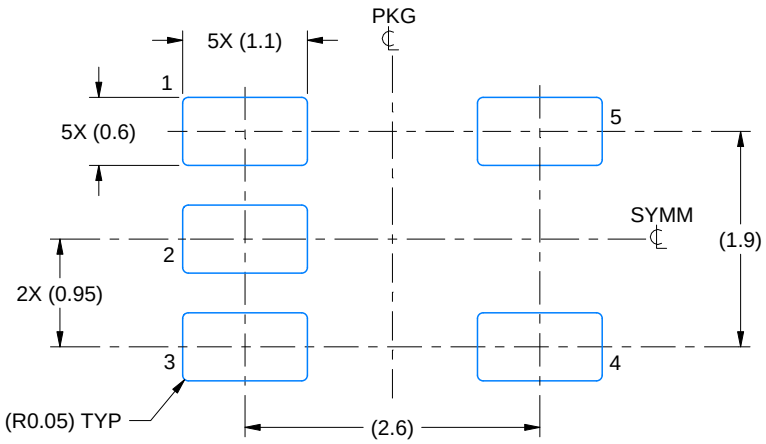


ALTERNATIVE PACKAGE SINGULATION VIEW

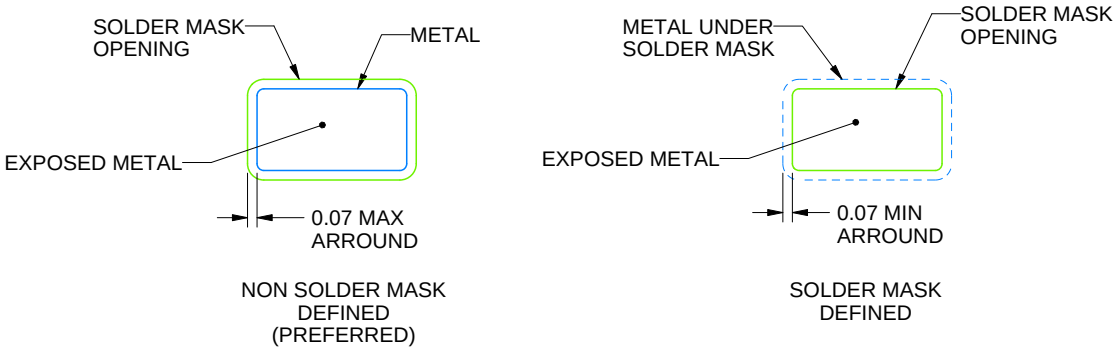
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

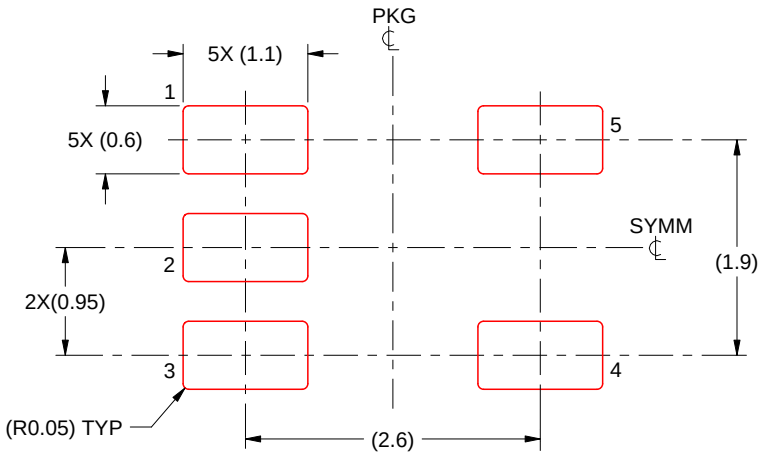


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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